Ultra-Low-Cost Printed Electronics

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by

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Abstract

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Ultra-low-cost printed electronics seek to reduce the manufacturing cost of electronics with less expensive, all-additive printing methods that conventional silicon manufacturing cannot replicate. But, in order to print these electronics, there is a trade-off in performance. Despite this, there are several applications for low-cost printed electronics including radio frequency identification (RFID) tags, electronic sensors, displays, smart cards, packaging, and printed circuit boards (PCB). In this work, inkjet and gravure printing are used to fabricate electronic devices. Particular emphasis is placed on inkjet printing. Based on performance requirements for the above applications, suitable electronic materials for printing are examined, including a soluble gold nanoparticle ink for metallization, printable organic dielectrics including polyimide and PVP, and a high performance pentacene precursor semiconductor ink. All of these materials have plastic substrate compatible activation temperatures (<200°C). Due to the "donut effect", and other complex inkjet phenomena such as differential wetting, each ink must be optimized to allow printing of smooth, well-defined structures and lines. The processing techniques developed for each ink are presented. Using these techniques,

printed high-Q passive components and transistors were fabricated on plastic. The resulting devices represent some of the highest performance printed devices published to date and both their AC and DC properties are studied in-depth. Finally, based on the fabricated transistors, a manufacturing route to achieve the necessary performance, f_t > 500 kHz, for the discussed applications is proposed.

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Chapter 1

Introduction to Low Cost Printed Electronics

Low cost printed electronics have gained a great deal of interest over the past 5 years because of their promise to greatly reduce the cost of many electronic applications. In particular these applications include radio frequency identification (RFID) tags, displays, printed circuit boards (PCB)/keypads, chemical sensors, etc. In the end, if the cost goals are achieved, the ubiquity of these electronics would be greatly increased. However, before manufacturing these products, basic research must be carried out to determine feasibility and performance limitations. Therefore it is the goal of this work to determine the best materials, develop printing processes for those materials, and investigate performance limitations. This chapter describes the reasons why printing has such a large cost advantage over conventional silicon processing and describes some of the applications in greater detail. The methodology, motivation, and organization of this entire work are also discussed.

1.1 Introduction

Many engineering achievements have helped fundamentally alter the world. The development of the printing press in Europe by Johann Gutenberg is one such achievement that many historians credit for bringing the European continent out of the medieval period [1]. The printing press created the ability to quickly mass produce information in the form of books, journals, periodicals, etc. By quickly replicating this

information, the spread of knowledge was enhanced. This greater sharing of knowledge thus helped end the medieval period in Europe.

Although an interesting historical development in itself, more relevant to this work is the manner in which the printing press quickly replicates text. For example, a master pattern with protruding text is dipped in ink. The wet master is then pressed onto the media, usually paper, and the copy is made. This is repeated many times until the desired number of copies are made [2].

In many ways the idea of the printing press represents an ideal method of manufacturing as there are numerous cost advantages. Once the master pattern is made, there are only small incremental costs resulting from the use of paper and ink. Furthermore, there is very little waste generated within the printing process and this has two distinct advantages. First, since the only ink used is the ink deposited onto the paper, there is little cost associated with the use of excess ink. Second, because there is little excess ink, there is little excess material that requires costly disposal. Since there is no major disposal this process is also friendlier to the environment. Along with the previous cost advantages there is also an inherent advantage of the high throughput associated with printing. The master pattern does take some time to fabricate, however once made it can replicate copies many times.

Furthermore, by printing multiple layers of different colors, color copies can be fabricated. These additional steps have all the advantages associated with the advantages of the first layer as described. Because this process of making color copies involves the "addition" of multiple layers and does not involve removal of any previously added material, this type of manufacturing is quite often termed "all additive."

In a cost analysis of printing, the product's price includes the materials, the depreciation of the equipment, and labor, which is minimal as long as the process is automated. As long as throughput is high the depreciation is minimal per product, thus a printing system is among the cheapest manufacturing methods available. If these principals could be applied to semiconductor manufacturing processes, prices for these products could be minimized as well.

1.2 Silicon's Shortfalls

In many aspects silicon processing uses many of the ideas in printing to achieve low costs and rapid manufacturing, however it is in the differences where it is rather difficult to reduce costs further. Some of the high costs associated with silicon processing include energy, the limited availability of area, and the pattern transfer or photolithography itself. Energy costs remain high because of the high temperatures needed and the energy required to purify and keep the processing clean.

Another area where silicon processing is fundamentally different from printing is in the fact that there is a limited area on which the circuits can be "printed." In contemporary printing of newspapers or magazines the printing is done in reel-to-reel processes. In these processes the paper is rolled down the line as the graphics are printed onto it. Because of this large area, continuous printing is done; both result in reduced costs. But in silicon processing the method is different. The cost of processing is mainly dictated by the number of processing steps required for each wafer. Furthermore, because the size of a silicon wafer is limited due to mechanical stability and equipment size/cost restrictions, it is difficult to achieve cheaper dies by scaling up the wafers. Thus it is

difficult to lower the cost per die except through reduction of feature size (i.e. scaling creates more die per wafer) [3].

In the final issue, pattern transfer or photolithography, silicon processing benefits from its similarities to printing. But, similar to the previous issues described, it suffers from its differences. Photolithography is a modern term associated with silicon integrated circuit manufacturing that refers to the use of light imaging in photopolymers and pattern transfer [4]. This particular technology could be considered to be at the intersection of pattern transfer and printing. The printing is done when the pattern on a mask is transferred using light onto a light sensitive polymer. Upon development of the polymer the polymer now acts as a mask to transfer its pattern to the layers beneath it. The imaging of the polymer can be done almost simultaneously over the whole wafer. Thus silicon processing can achieve relatively high manufacturing speeds. At the same time, though, the pattern transfer adds costs and time to the process. This is because each layer is added as a full sheet (thin film). This is a time consuming and costly process in itself, sometimes requiring high vacuum. Then, the film is etched using the photopolymer as a mask. Thus material, often >90%, is wasted. This adds costs from both the excess material and disposal of the waste material.

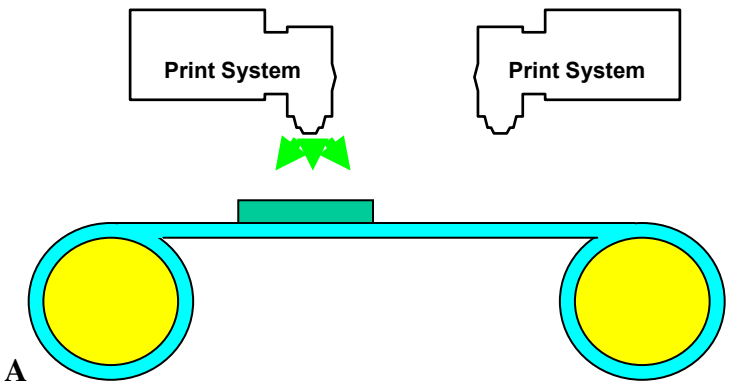
There are also many steps involved with “printing” the image onto the photoresist. These include 1) spinning the photoresist, 2) exposing the photoresist, 3) developing the photoresist, 4) etching the underlying material, and 5) striping the photoresist. Overall, there are many more steps required in silicon processing - to both “print” the image in the photoresist and transfer the pattern into the underlying material - than there is in all-additive printing process that simply has one step: 1) print. Because

cost generally scales with the number of steps, there is a substantial cost savings in direct printing, and, if silicon processing could more purely resemble printing, it could achieve much lower costs.

1.3 The Cost Solution: All-Printed Electronics

If electronics manufacturing could shift to a process resembling more of a purely printed technique, then the cost could be greatly reduced. This is essentially true for all the reasons mentioned above. This printing process would be all-additive; thus material cost and waste disposal are reduced. Furthermore there would be no need for expensive equipment needed for vacuum processing, photoimaging, etching, etc.

Additionally, a larger sized substrate could be processed since both the substrate and the printers are not limited in size as silicon equipment and wafers are. An even bigger advantage is the fact that the use of plastic would facilitate reel-to-reel printing so throughput could be increased further (Figure 1.1).



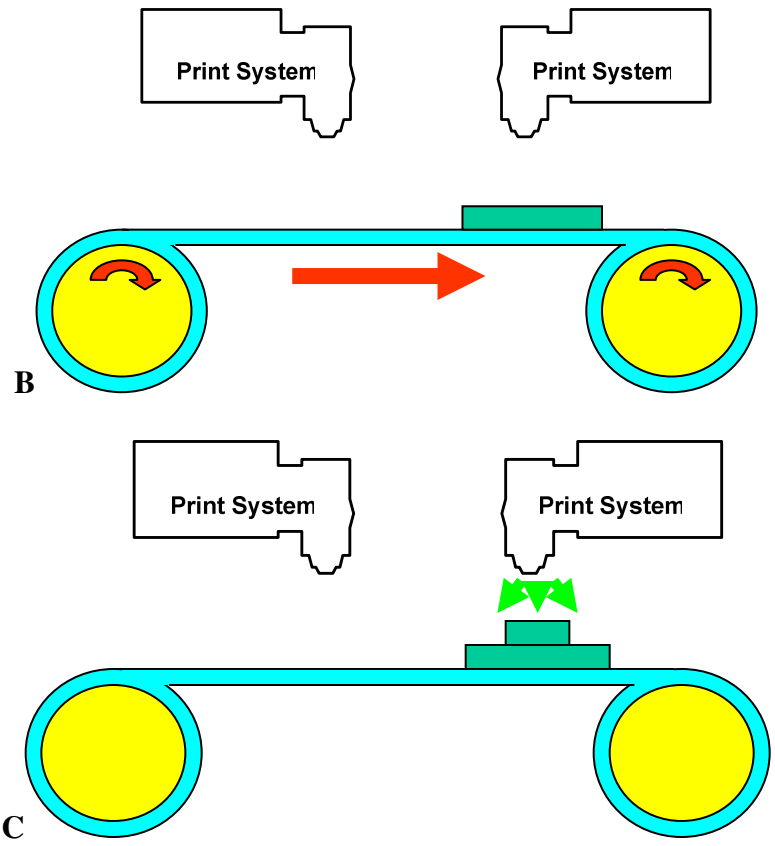


Figure 1.1: Example of an all-additive, reel-to-reel, printed manufacturing process. The first layer is deposited (A) and the substrate is reeled to the next station (B) where the next layer is deposited (C).

Since plastic substrates are used the temperatures are limited to <200°C. Also clean rooms are no longer needed since individual printers could be encased in clean boxes. These two issues would reduce energy costs.

However, it is important to note that in order to facilitate this technology only certain materials can be used. In particular, these materials must be solution processable so that they can be printed and they must have processing temperatures <200°C so that they are compatible with the plastic substrates. Because of these two properties, quite often these materials have inferior performance than those in silicon manufacturing [5].

Furthermore there are also performance reductions because the minimum feature sizes are much larger as a result of the limitations of the printers. For example, sub-micron all-additive printing has yet to be realized. Because the minimum feature size is larger, printed electronics have a higher cost per logic function than silicon.

As a result of the material and printer limitations, low-cost electronics have substantially reduced performance, but as a tradeoff, offer substantially reduced cost per unit area than silicon electronics.

1.4 Applications

Electronics made using printing techniques would have greatly reduced cost over conventional silicon electronics, and, as a result these electronics are typically referred to as low-cost printed electronics. Despite the reduction in performance, there are still a wide variety of applications where low-cost printed electronics could be used. Some of the more obvious applications include displays [6], radio frequency identification (RFID) tags [7], smart cards, electronic sensors [8], packaging, and printed circuit boards (PCB)/key pads used in cell phones, remote controls, car keys, etc. The common element among all these applications is the fact that all of these applications do not need either ultra fast circuitry or ultra dense circuitry like that in CPUs used today.

RFID tags represent the largest technical challenge to low cost electronics. The idea behind this technology is that product level bar codes could be replaced by active circuit tags as long as the tags are cheap enough; <2 cents per tag. The advantage to this is that mundane tasks such as inventory and checkout could be greatly sped up and labor

would be minimized. Other features such as real time pricing updates could also be implemented easily.

This application represents the largest technical challenge to this field of research because the circuit speed required is relatively high. The circuit speed is dictated by the communication frequency and, given the preferred reading distance along with the available band/power output (mandated by the FCC), RFID will likely occur at 13.56 MHz [9, 10]. On chip clock frequencies for such circuits are in the range of 200 kHz. Few low cost semiconductors can achieve a mobility of 1 cm^2/V-s or greater, but the transistors made with these materials will likely result in devices with transition frequencies in the range of approximately 500 kHz. Thus this technology tests the current limits of what is achievable with low cost electronics. As a result, quite often the required specifications for RFID are quoted without loss of generality because if a device will work in an RFID application, it will function in most other low cost applications.

Low cost display manufacturing seeks to capitalize on the fact that low cost manufacturing can easily print over large areas with a sparse number of transistors. Because of this ability, low cost, printed manufacturing may be able to reduce the cost of active matrix displays by 10-200X. On-state performance is a non-issue since several hundred kHz is more than adequate for these applications. Note that off-state performance will be an issue, however, since the "blackness" of black is typically determined by leakage current through pixel transistors.

There are also a wide variety of applications that spin-off from the previously mentioned applications. For example, the passive component technologies developed (inductors, capacitors, and interconnects) could be used in PCB/key pad applications

such as cell phones, remote controls, car keys, etc. By using low cost manufacturing, the use of expensive photolithography to make PCB's could be eliminated and the throughput could be greatly increased.

Another application is to use printing to make electronic noses. Electronic noses use a variety of active devices as sensing elements. When exposed to a chemical or chemicals, each element produces a unique response. By using pattern recognition algorithms to decode the response from a matrix of sensors, the chemical or chemicals can be identified. Typically, the larger the matrix, the better the sensitivity and the higher the guarantee of correct recognition. Typically these sensors are made as individual components and connected to a central processor. This is quite costly - thousands of dollars to tens of thousands of dollars. By using printing techniques and integrating the sensor onto a single chip, these low cost manufacturing methods seek to reduce the cost well below $1. With such low costs these devices could be made much more available and sensors could be used to detect spoiled food or contaminated air.

1.5 Methodology

While the promise of these low cost applications has generated great interest over the last five years, in general, there have been few extensive studies detailing the requirements of the materials, equipment, and printing techniques needed for these electronic applications. It is necessary to view these items as a whole since all are interdependent. To date many of the studies have focused on a particular material or material set. As a result, these studies have not addressed many of the integration

problems with these electronic materials and, furthermore, they have been unable to provide a larger picture detailing the performance limitations of the materials.

Therefore, the purpose of this work is to create a more extensive study that will form the starting point for the realization of fully-printed low-cost electronic systems. It will identify materials that may be suitable for low cost printed electronics, and it will study and develop different printing methods available for these materials. Furthermore, this work will identify any limits to this technology and project what performance may actually be achievable.

1.6 Organization

Chapter 2 begins with an introduction to inkjet technology and contrasts it with another competing manufacturing technology - gravure printing. It goes on to identify the components important to an inkjet printer. It motivates the need for a custom built inkjet testbed and describes the design methodology of the testbed. A discussion of inkjet dispensing theory is also discussed in this chapter.

Chapter 3 begins by motivating the need for high quality interconnect materials in the context of passive components. It then identifies a gold nanoparticle ink as the best candidate for inkjetting high performance interconnects. Printing techniques are developed for this material as well as polyimide and PVP dielectric materials. Finally, these techniques are used to create high performance multilevel interconnects and passive components.

Chapter 4 discusses organic semiconductors and printing techniques to optimize performance. It begins by introducing electron transport in the context of molecular

structure. Printable organic semiconductor candidates are identified and, finally, the optimization schemes for a pentacene precursor are described.

Chapter 5 develops a baseline all-printed transistor technology based on the work in the previous chapters. The performance limitations of these devices are discussed. These limitations are addressed and solved in Chapter 6.

Chapter 7 discusses f_t and f_{max} and the frequency performance requirements for RFID circuits. It goes on to develop a method to characterize the frequency performance, f_t, of the optimized devices made in Chapter 6.

In Chapter 8, gravure printing is discussed along with its advantages over inkjet printing. Some initial experiments are described and the need for an ink tailored for gravure printing, versus inkjet, is discussed. Future work is also described in this chapter. Finally, the conclusions are in Chapter 9.

Chapter 2

Inkjet Printing Technology and Experimental Testbed

Two of the most promising printing technologies for fabricating low-cost printed electronics include inkjet printing and gravure printing. Inkjet printing is a well known technology that makes use of individual droplet dispensers. Inkjet heads are composed of several dispensers that deposit individual drops to form patterns. By properly placing each drop, coherent patterns can be made on a substrate. Gravure printing is a lesser known technology that uses a cylinder with an etched pattern on it. Ink is deposited into the pattern on the cylinder and when the cylinder is rolled over a substrate, the pattern on the cylinder is transferred to the substrate. Because of the fundamental methods of pattern transfer, each technology offers distinct advantages over the other. In general, inkjet printing offers both easier and more flexible alignment capabilities because of its ability to deposit individual drops onto any location on the substrate. Gravure printing is more difficult to align patterns because the whole cylinder must be properly aligned to the underlying substrate. This is cumbersome due to the size of the cylinder and is exacerbated by flexible substrates that can distort. Gravure printing, however, offers much better throughput since the whole pattern can be transferred in a single roll of the cylinder.

Given these general characteristics, this chapter provides an in-depth discussion of inkjet technology along with a discussion of its advantages over gravure printing. An in-depth discussion of gravure printing is in Chapter 8. Also, the development of an inkjet testbed for use in the experiments in this thesis is discussed in this chapter.

2.1 Inkjet Technology Background

While inkjet printing can offer higher throughput then conventional silicon processing, it generally has much less throughput than gravure printing. This is due to the serial nature of the printing dispenser - each drop much be deposited in sequential fashion. There are many on going efforts, however, to increase throughput by using arrays of dispensers numbering in the hundreds [1, 2]. The typical commercial printer (for example the Epson Stylus) has 100-300 dispensers and thus does not have throughput issues given its application (household printing). However, it does not have precise droplet volumes and thus this makes its use in low-cost electronics printing impractical.

Despite this throughput disadvantage, inkjet printing offers several advantages that gravure printing does not. Inkjet printing offers extremely flexible pattern making abilities. This is because inkjet printing is fundamentally an all-additive process where the pattern is made from the commands given to the printer from the computer. Since the computer's commands are generated from the software, updates can be made in real-time to the patterns. This is in contrast to gravure printing where the patterns are engraved into rollers.

Inkjet printing also offers real-time dynamic alignment [3]. Alignment is critical when printing multiple patterns or when printing onto a prepatterned substrate. Generally speaking, alignment with inkjet can be done by using a camera with a fixed distance from the printer's dispenser. For example, a drop can be dispensed onto the substrate and the amount that the drop is offset from a desired location can be input into the computer. The

computer then re-zeros the position taking into account this offset. X and Y offsets can be found using this technique while rotational error requires two desired locations (i.e. grids) on the substrate. How rotational alignment is accomplished is discussed in greater detail later in this chapter.

The concept of alignment can be split to include global alignment across an entire substrate and local alignment on an individual transistor. Both types of alignment can be programmed into the software such that the pattern placement is altered to correctly place the current layer over the already deposited layer. This software update is essentiality the same as altering a pattern.

While global alignment is necessary to print multiple layer patterns, local alignment is particularly applicable to low cost electronics when cheap substrates made of plastic are used. Most plastic substrates in the experiments in this work were susceptible to considerable shrinking (5 – 500μm) [3]. As a result, local alignment is quite useful while printing onto these substrates, especially in critical areas such as electrode overlap in transistors. For example, if the electrodes do not overlap the gate, the transistor will not function at all, while if there is too much overlap, the added parasitic capacitance will degrade frequency response. An example of how this might occur is the following. If a substrate underwent a certain amount of distortion such that two transistors were closer together than planned for in the original pattern then, without local alignment, the printer would print the source and drain electrodes on one transistor correctly, but on the other transistor, one electrode would have too much overlap over the gate while the other electrode would not even cover the gate. This error can be corrected by printing the last 50 μm using local alignment where a camera images the gate. Then,

since the distance from the camera to the dispenser is known, the last 50μm of the electrodes could be printed with equal overlap over the gate. This ensures an optimally performing device, and, in this manner, local alignment would correct these alignment errors resulting from substrate distortion.

It is also valuable to point out how local alignment and real-time pattern altering can become a very useful tool in combination. For instance, given the above example where local alignment is used to print source and drain electrodes, the pattern for the interconnects used to connect the electrodes will not be identical on every chip. As a result, the pattern will need to be modified to fabricate the correct dimensions of the interconnects. With the proper software this can all be accomplished in real time.

2.2 General Inkjet Printer Components

The main components of most inkjet printers are generally the same. They include the printer dispenser (head), the ink reservoir and ink delivery path, the motion stages, and the driver and controllers for the head and stages. The two most common types of inkjet dispensers available today are piezoelectric crystal dispensers (piezoheads), and thermoelectric dispensers (bubble jet heads). Fluid ejection occurs in a similar manner in both cases; a pressure wave is created in an ink chamber that expels the ink through an orifice. However, the dispensers differ in the manner that they create the pressure wave and how the pressure wave causes ejection.

2.2.1 Bubble Jet Dispensers

The bubble jet type dispenser (Figure 2.1) uses a heater in the form of a resister to super heat the ink to its spinodalian limit, 312° C for water, whereby the ink boils and a bubble is created. The bubble is created in the time span of microseconds and causes pressures typically >1 MPa that cause droplet ejection [4, 5]. The advantage to this type of technology is its simplicity to manufacture, which translates into lower cost. The heaters are typically made from polysilicon or platinum and thus these dispensers can be made using conventional silicon and MEMs processing techniques. Due to the low cost, the heads can also be disposable such as those made by Hewlett-Packard. The added advantage to this disposability is that if the head clogs due to dust or debris it can be discarded. This is a concern in all print heads since orifice diameters are typically in the range of 100µm down to as low as 5µm.

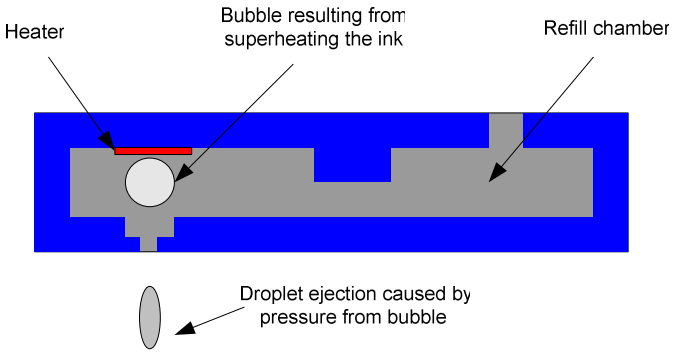


Figure 2.1: Cross section of a typical bubble jet dispenser showing how droplet generation occurs.

However, the drawback to these heads is that this heating step poses concern to low-cost electronics printing where the inks are usually temperature sensitive. For example, gold nanoparticles that sinter at ~120°C have been demonstrated for use in interconnects [6]. Since they sinter at such low temperatures, the heat required to boil the

ink causes the nanoparticles to sinter onto the heater. After a thick enough metal layer is sintered onto the heater, the heater's resistance drops, and it no longer produces high enough temperatures to cause droplet ejection.

2.2.2 Piezoelectric Dispensers

Piezoelectric heads (Figure 2.2) work through use of a piezoelectric crystal. By applying a potential across the crystal, the crystal deforms or contracts, and, if properly oriented onto the chamber of a dispenser, it will create a pressure wave that expels ink droplets [7]. This ejection process will be described in-depth later in this chapter. The main disadvantage to this technology it that it is harder to integrate the crystal using conventional silicon processing and thus these types of heads are usually more costly. Because of this, they are almost never disposable and thus in the event of a clog the head will need to be replaced. Most important, though, is that ink degradation is no longer a concern since the pressure wave is generated strictly through mechanical deformation. For this reason, the inkjet testbed designed for all of the experiments in this work uses a piezo head.

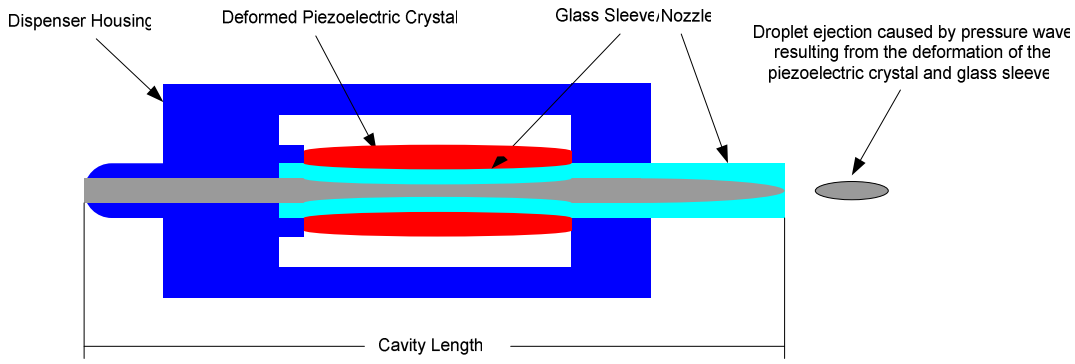


Figure 2.2: Cross section of a piezoelectric inkjet dispenser showing how droplet ejection occurs.

2.3 Experimental Inkjet Testbed and Specifications

Commercial inkjet printers are not adequate for low-cost electronics fabrication for a variety of reasons. First, the ink deposition volume can vary as much as 50%, while electronics fabrication require minimal variation (<10-20%) to ensure that the smallest possible lines and gaps can be repeatably and precisely made. Second, structure size is inherently coupled to the precision of the motion stages and most commercial printers do not have adequate precision for electronics fabrication. Third, most commercial printers are made for water based inks and as a result, cheap plastics are used for the ink delivery pathways. Because of this, the ink delivery pathways in commercial printers are not resistant to aggressive solvents such as acetone or toluene. This is critical since many of the inks used in low-cost electronics fabrication require these as solvents. Due to these inadequacies an inkjet testbed had to be designed and assembled to carry out the low-cost electronics experiments for this thesis.

Most commercial printers are designed so that the printer's head moves while the substrate stays stationary. This is practical since the motors needed to move the head can be small because the heads are lightweight, and it is also difficult to move the entire sheet of paper. However, for the purposes of a testbed that will print onto a 6 inch radius (the maximum size of easily available wafers) or smaller, it is much simpler to design a system with a stationary head and a moving substrate. Thus the testbed was designed so that the ink dispenser remains fixed while the substrate below it moves on X and Y translation stages. The testbed also incorporates a rotational stage so that proper alignment can be achieved on prepatterned substrates.

2.3.1 Motion Stages

The motion stages used have 1.3μm precision in the X and Y directions, and 0.5 arc minutes of angular precision. Despite this precision, the drop placement varies 10μm or more due to drift in flight. However, because of the precision of the motion stages, it is ensured that the drop placement is limited to the precision of the dispenser and not the stages.

2.3.2 Dispenser and Dispensing Theory

In order to fabricate low-cost electronics a dispenser must be able to print lines <100μm, it must be tunable to a wide range of inks, and it must be able to print aggressive solvents. Inkjet dispensers manufactured by MicroFab fit these criteria. The orifice diameter is 100μm which allows them to print the requisite ~100μm sized lines. These dispensers can operate in continuous or drop-on-on demand mode. Continuous mode is where the drops are continuously ejected at a given frequency while drop-on-demand mode is where each individual droplet ejection event is specified. The voltage waveform used to drive these dispensers can be tuned and thus these dispensers can be used with a wide variety of inks with different fluid properties. This is discussed more in-depth below. These dispensers are also made of tiny glass tubes (D~500μm and L~0.75 cm) with a piezocrystal epoxied around the circumference of the tube. The epoxy is semi resistant to solvents and thus as long as the solvents only contact the inside of the tube (minimal exposure to the outside is tolerated) as in normal operating conditions, the head is resistant to most solvents encountered in the inks.

A generic head schematic for piezoelectric inkjet dispensers is shown in Figure 2.2. These dispensers use either a unipolar or bipolar voltage waveform to inkjet the material. The bipolar wave is shown in Figure 2.3. The proper model describing droplet ejection for this type of waveform was first described by Bogy and Talke [7]. This was the first published analysis that assumed fluid compression in the dispenser. By allowing this assumption, they were able to use linear acoustics theory to describe the wave propagation phenomena. The theory of ejection is as follows (Figure 2.4). Upon initial contraction of the piezo crystal, two negative pressure waves propagate in opposite directions away from the crystal located at the center of the dispenser. When one pressure wave reaches the end of the dispenser at the supply side it reflects and changes to a positive pressure wave. Conversely, when the pressure wave hits the closed end or dispenser side it reflects with the same sign or negative pressure. After time L/C where L

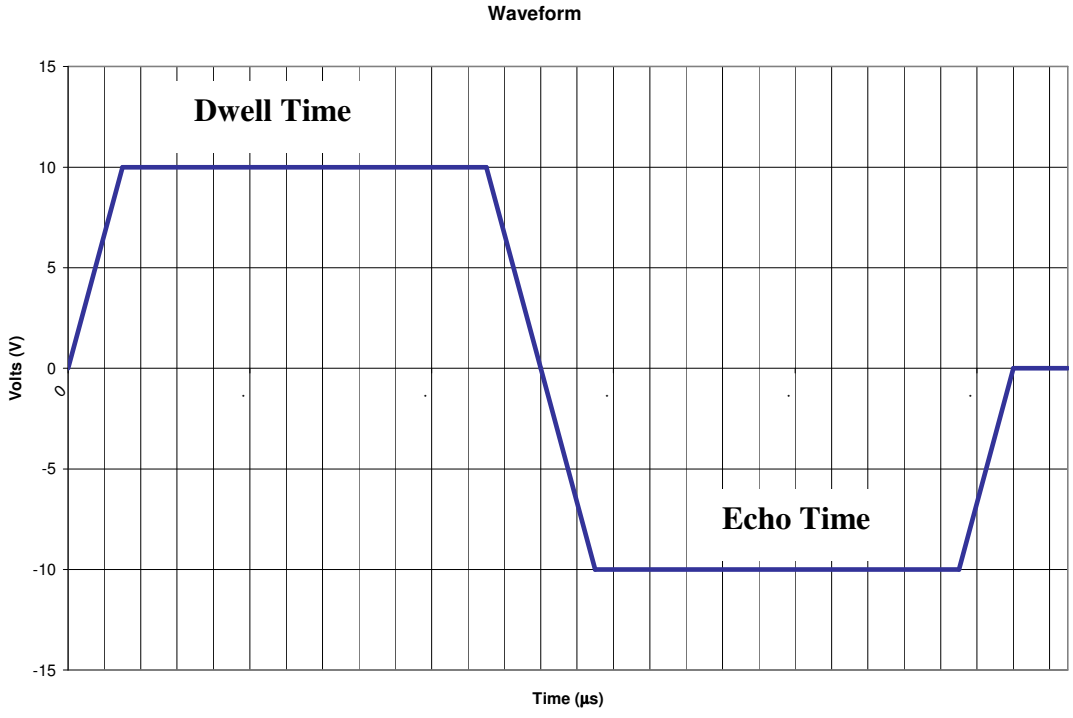


Figure 2.3: Bipolar voltage waveform.

is the length of the dispenser and C is the speed of sound in the fluid, the pressure waves meet at the center. This is the optimum time at which to apply the negative voltage step because the contraction will annihilate the reflected negative pressure wave and double the reflected positive pressure wave. This optimum time is referred to as the dwell time as shown in Figure 2.3. After another L/2C this positive pressure wave reaches the tip and fluid is ejected out. Thus the total time from initial contraction to ejection is 3L/2C. As the pressure wave continues, it is again reflected at the tip and then again at the open end. At this point is has changed sign to a negative pressure wave and will reach the middle of the dispenser at 3L/C after initial contraction. This negative pressure wave can be damped out with the final positive contraction so that it will not cause further ejections from the tip. The time between the last negative contraction and this final positive contraction is known as the echo time (Figure 2.3).

In practice the dwell time optimization is carried out by changing the dwell time with a fixed strobe delay until the drops are farthest from the dispenser (the drops are viewed using a strobe LED, a camera, and a monitor). At this point the drops are moving with the fastest velocity for any voltage and thus the optimal driving condition is achieved. As previously stated, the echo time or the length of the negative pulse parameter helps to damp out some of the pressure waves in the dispenser. This non-critical parameter is usually about twice as long as the dwell time, but is not necessary for higher viscosity materials.

All of the parameters (positive and negative voltage, dwell time, echo time, and ramp rates) of the voltage waveform can be adjusted. As a result these heads have a high degree of tunability, which allows them to work well with a variety of different inks with

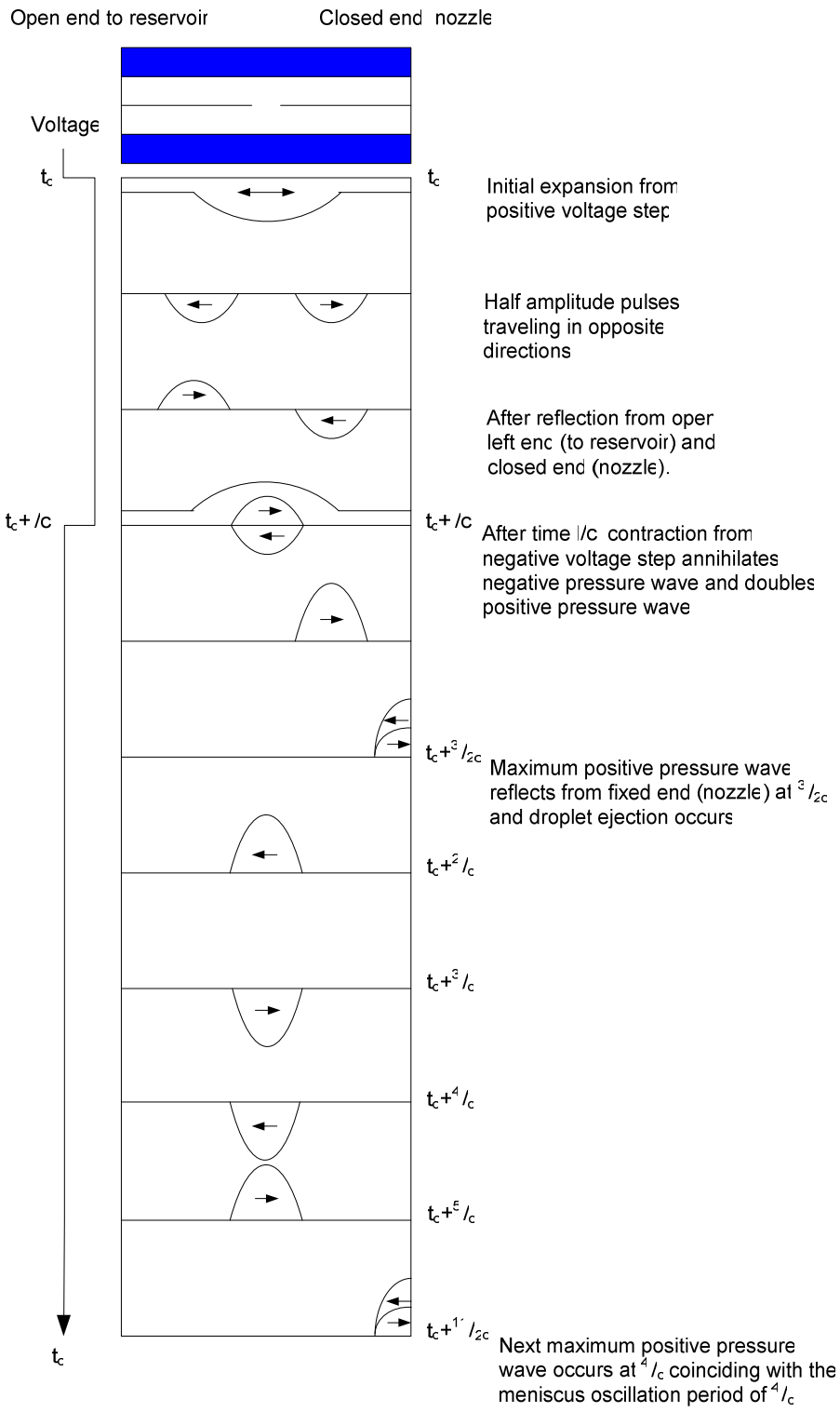


Figure 2.4: Illustration of pressure wave propagation in a piezoelectric dispenser.

varying fluid properties. In conjunction with the relatively high resistance to solvents, this makes these heads an ideal choice for the testbed. However, it is important to note that although extremely flexible they are not optimized for any particular material. The heads are made of glass and each solvent wets the orifice differently. As a result accurate pressure control is required for each ink so that the proper meniscus is created. The way this is accomplished is discussed in the pressure control section. Ideally, though, in an industrial application, the dispensers will be tailored for the specific ink they print and the same pressure can be maintained on all the dispensers. This can be done by using the proper metal that has the proper surface energy and thus achieves the desired wetability. Furthermore, some heads need to withstand higher temperatures when substrate heating is used. The reasons for substrate heating are discussed in Chapter 3. Despite these drawbacks, the flexibility of these MicroFab dispensers allows them to work well in a research environment.

2.3.3 Pressure and Meniscus Control

In most commercial inkjet systems pressure control is not a critical issue since the specifications on droplet variation are relaxed. Furthermore, the inks are mostly water-based, having similar wetting properties, and thus the heads are inherently easier to design since there are less types of inks to design for. The reservoir usually sits directly above the head and pressure is maintained via gravity and wetting. In these MicroFab heads a variety of different inks are used with different wetting properties. Therefore, pressure control at the tip of the dispenser is crucial in order to maintain the proper meniscus for jetting. If the meniscus wets the bottom of the dispenser (higher pressure)

the required jetting voltage will be too high. On the other hand, if the meniscus is to far into the head (lower pressure), then there is a risk the fluid will get siphoned out of the head and back into the reservoir.

In this system (Figure 2.5) the reservoir sits ~4 inches below the dispenser and thus a small positive pressure is required for meniscus formation. The pressure is controlled by a pressure regulator and two needle valves. The pressure regulator controls pressure from 2psi to 40psi and therefore serves as a coarse pressure control. It also dampens out pressure variations in the house nitrogen line. One needle valve is used to bleed off the extra 2 psi of pressure and is kept fully open while printing. The other needle valve acts a fine pressure control. With this setup pressure can be controlled down to less than one inch of water.

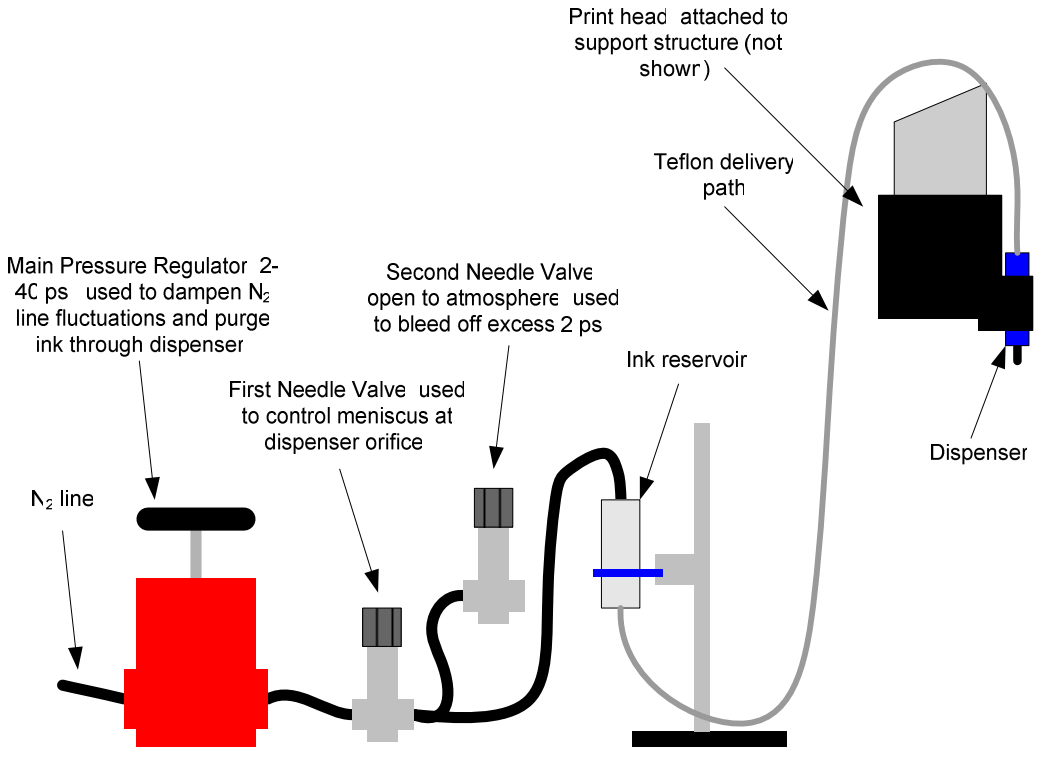


Figure 2.5: Side view of the pressure control system and the ink delivery pathway.

2.3.4 Solvent Delivery Path

As previously stated, commercial printers are not required to be solvent resistant since they mainly use water based inks. Also, since the reservoir is directly above the head, the delivery path is usually integrated into the head itself. In this testbed (Figure 2.5) the reservoir sits ~1-2 feet away from the head. This allows height adjustment of the reservoir along with easier removal for cleaning and replacement. The Teflon delivery path consists of a machined Teflon reservoir connected to 2 ½ feet of 0.062" Teflon tubing. The tubing and reservoir are connected using adapters. The reservoir rests about 4 inches below the dispenser therefore a positive pressure must be maintained in the reservoir in order to keep the proper meniscus in the dispensing device.

It is crucial to keep the delivery path ultra clean since particles can cause adverse jetting and even clogs. To clean the delivery path the Teflon tubing is flushed with 20 mL of acetone filtered though a 0.2 μm membrane while the Teflon reservoir is sonicated in acetone for at least 10 minutes. After sonication, the reservoir is rinsed with filtered acetone. To ensure that this delivery path is clean, the tubing is connected to the dispenser and flushed with more filtered acetone. Then the reservoir is connected and filled with 2 mL of filtered acetone. The nitrogen pressure line is connected and turned on so that the acetone flushes completely through the system. The stream emanating from the dispenser is monitored to make sure there are no obstructions. This process ensures that the full delivery path is free of particles before filling with ink. Note that there is no filter in the delivery path once the ink is in the reservoir. The absence of a filter ensures

that the pressure at the inkjet head is accurately controlled by the pressure applied to the reservoir (since the pressure loss downstream of the filter is avoided).

2.3.5 Substrate Chuck

Commercial inkjet printers only require the ability to print onto paper, but this testbed requires the ability to print onto a variety of substrates including plastic and silicon substrates. Furthermore, the testbed requires a way to control substrate heating. The reasons for this will be discussed in Chapter 3. In order to provide vacuum and substrate heating with relatively good uniformity a hot chuck was used that was controlled by a custom-built temperature controller.

2.3.6 Software and Computer Interface

The main control program for the testbed is run off of a PC. Its basic function is to synchronize the motion of the stages with the deposition of droplets. It also incorporates some added features such as wafer alignment, printing onto multiple dies with the same pattern, and pattern file input. The PC interfaces with the MicroFab driver via a serial cable. The Printer program sends digital signals through the serial cable to the driver specifying the parameters of the voltage waveform and when to fire. The driver for the translation stages fits into a PCI slot in the PC and the PCI card driver sends digital signals to the stepper motor drivers specifying direction, number of steps, speed, and acceleration. A schematic of these electrical connections is shown in Figure 2.6.

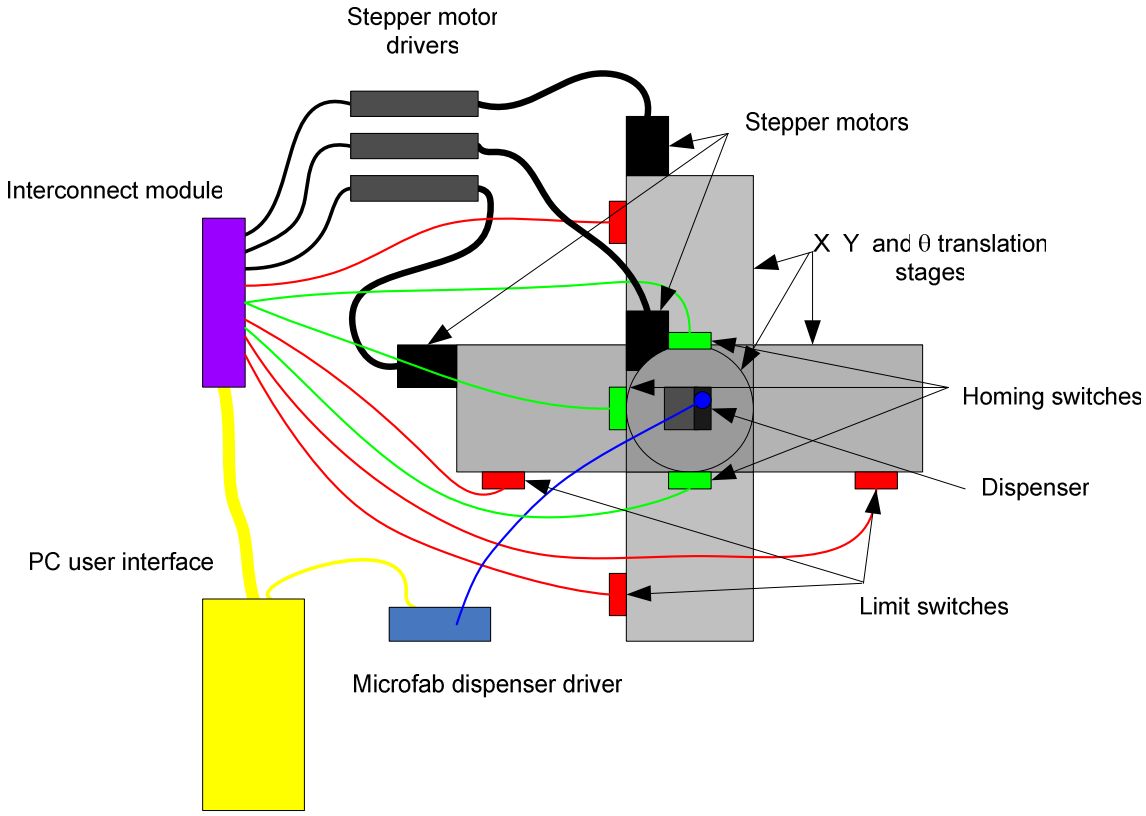


Figure 2.6: Top view schematic of the inkjet testbed electrical connections.

The pattern file inputs are read in as text files and assume the dispenser is in drop on demand mode. These files specify individual Cartesian coordinates for each drop location and the number of drops for that location. A separate program generates these text files from specified shape functions including lines, squares, rectangles, inductors, etc. All functions allow the user to tune the parameters including dimensions, drop spacing, wait state, number of layers, etc. The reason for the wait state will be discussed later.

2.3.7 Alignment Algorithm

The testbed uses an automated alignment routine to align the printer head to the substrate. This routine works by dispensing a drop in two grids in opposite corners of the substrate. Each grid is then viewed in a camera where the user types in the offset of each drop relative to the center of each grid. The software then calculates the offset and centers the wafer. The algorithm in this software works by first calculating the x offset as follows:

$$x_{error} = \frac{(x_1 + x_2)}{2} \qquad \textbf{Eqn (2.1)}$$

where x_1 and x_2 represent the offsets of each drop in their respective grid. Similarly the y offset is calculated as:

$$y_{error} = \frac{(y_1 + y_2)}{2} \qquad \textbf{Eqn (2.2)}$$

where y_1 and y_2 represent the offsets of each drop in their respective grid. For both of these errors, the sign of the error will indicate the direction of substrate movement; a positive error will mean the substrate must move positive with respect to the head and vice versa for the negative.

After correcting for these errors, only the rotational error remains. This is calculated by finding the distance between the corrected offset coordinate and the line passing through the center of the grid as shown in Figure 2.7. This is found using the formula:

$$h = z * \sin(\alpha) \qquad \textbf{Eqn (2.3)}$$

where z is a straight forward calculation using the Pythagorean Theorem, x_1, and y_1:

$$z = \sqrt{x_1^{\,2} + y_1^{\,2}} \qquad \textbf{Eqn (2.4)}$$

However, α requires more calculation. α can be found based on the law of cosines if x and y are known as shown in Figure 2.7:

$$\alpha = \cos^{-1}\left\{\frac{y^2 - x^2 - z^2}{-2xz})\right\} \qquad \textbf{Eqn (2.5)}$$

The length of x and y are found as follows. For x:

$$|x| = \sqrt{\left\{\left(\frac{y_g}{x_g} * x_1\right)^2 + x_1^2\right\}} \qquad \textbf{Eqn (2.6)}$$

where y_g is the y coordinate of the grid on the wafer and similarly x_g is the x coordinate of the grid on the wafer. Thus y_g/x_g is the slope of the line passing though the center of the wafer and center of the grid. The length of y is:

$$|y| = \left| y_1 - \frac{y_g}{x_g} * x_1 \right| \qquad \textbf{Eqn (2.7)}$$

Therefore α is found and h can be calculated. In order to convert h to radians, h is divided by the radius of the circle passing through the center of the grid:

$$r = \sqrt{\left(x_g^2 + y_g^2\right)} \qquad \textbf{Eqn (2.8)}$$

The direction of rotation is found based on the sign of Equation 2.7 inside the absolute value parenthesis. If this is less than 0 then the rotation is clockwise and vice versa for a value larger than zero.

After calculating these errors the stages move to the current zero position, then the stages move the corrected offset, and finally the position is re-zeroed. Thus, the dispenser is at the center of the pattern on the substrate. Overall, this alignment allows accuracy to less than 5μm based on the user's ability to accurately determine the position of the drop

in the grids. However, in practice the accuracy is limited to 5μm to 10 μm due to variations in drop placement.

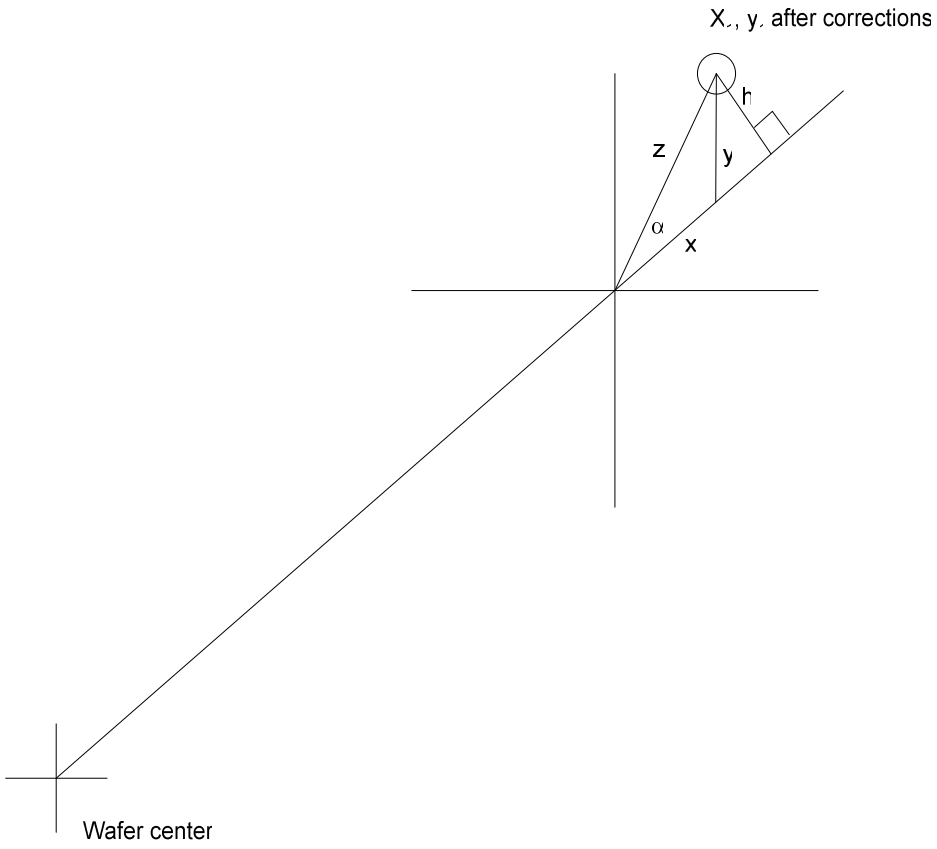


Figure 2.7: Alignment geometry.

2.3.8 Support Structure

The support structure of the inkjet testbed supports both the print head dispenser and the optics system and was custom machined. The optics system includes a camera for use with the alignment function and in-situ viewing of the drops during printing and another camera for droplet calibration (Figure 2.8).

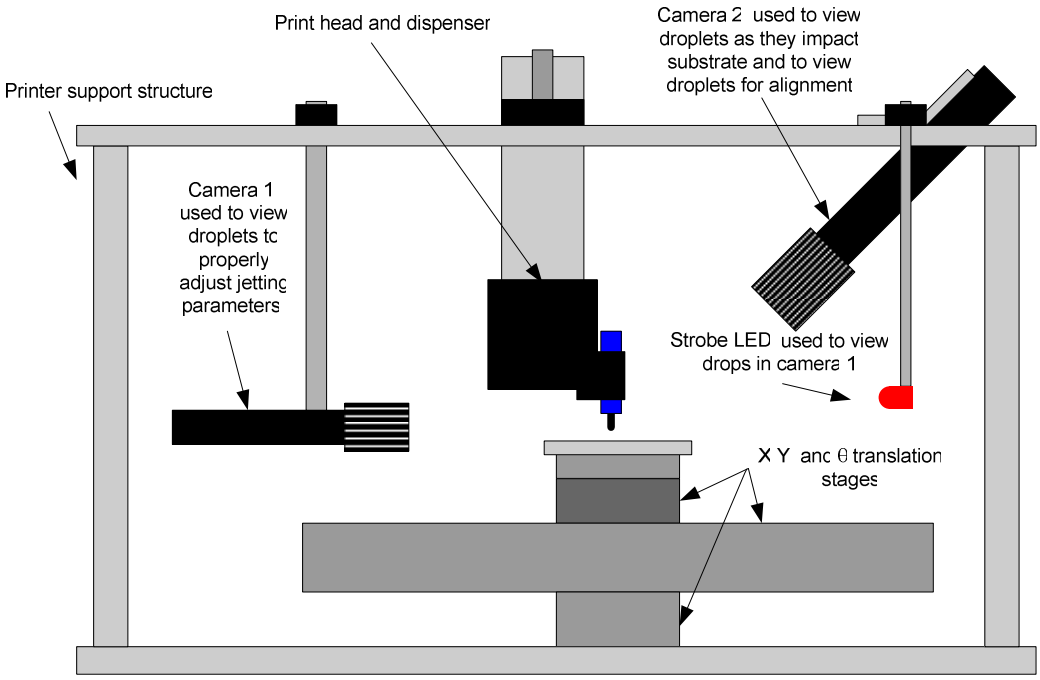


Figure 2.8: Side view schematic of the inkjet testbed support structure and optics system.

The printer is enclosed in an acrylic box. This box allows the user to purge the oxygen and creates a nitrogen atmosphere with less than ~10 ppm oxygen. This is required for various electronic materials that are sensitive to oxygen or for performing anneals that require an oxygen free atmosphere. The testbed with the acrylic enclosure is shown in Figure 2.9.

2.4 Conclusions

In comparison to gravure printing inkjet printing has much less throughput, but has advantages in both pattern making flexibility and ease of alignment. Patterns can be changed as well as aligned in real-time by updating the pattern software. Most

commercial printers have an array of dispensers to speed up throughput since the printing speed is limited by the serial nature of inkjet dispensers. Dispenser technologies include both bubble jet and piezoelectric. Bubble jet dispensers work by generation of a pressure wave via rapid boiling while piezoelectric heads generate the pressure wave via a mechanical deformation.

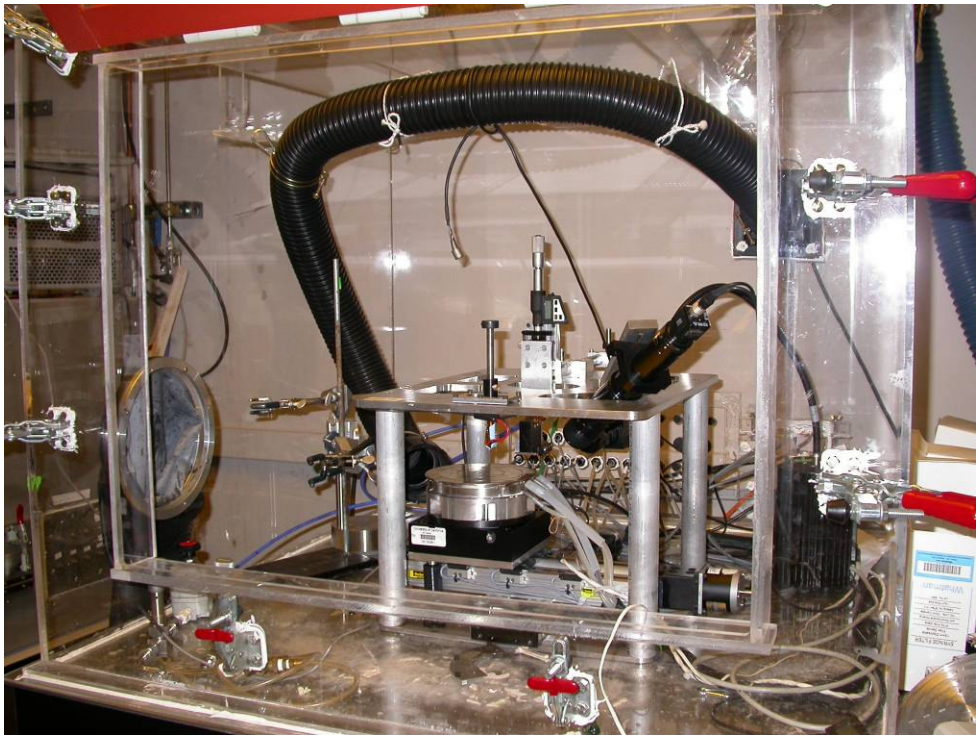


Figure 2.9: Custom built inkjet testbed.

Commercially available printers are deficient in their droplet placement accuracy, motion precision, solvent compatibility, and substrate accommodations for use in electronics fabrication. As a result a custom testbed was designed and assembled that had all the necessary characteristics. For the testbed designed here, it uses one dispenser for each material. Because of the stringent requirements in electronics fabrication, careful attention and design was carried out for each of the subsystems. This includes the choice

of motion stages, the choice of dispenser, pressure system design, ink delivery path design, the choice of substrate chuck, software design, and alignment routine design.

The piezoelectric dispensers from MicroFab facilitate the printing of ~100μm lines, are compatible with a variety of inks, and are resistant to aggressive solvents. The functional theory of these dispensers is based on the original work by Bogy and Talke and relies on the assumption that the fluid in the dispenser is compressible.

The printer includes an acrylic box to allow printing in a nitrogen atmosphere. It will be used in the majority of experiments in the following chapters to fabricate printed interconnects, capacitors, inductors, and transistors.

Chapter 3

Inkjet Processing Techniques and Passive Components

3.1 Introduction to Passive Components

Although they are the simplest components to fabricate, inductors and capacitors consume the most area on a typical silicon integrated circuit that incorporates them. It is for this reason that the printing of passive components has a huge area cost advantage over silicon. By design, printers enable printing over large areas and greatly increase throughput through all-additive roll-to-roll processes. Because of this, large area components are much cheaper to fabricate with printers. This contrasts with silicon where chip area is relatively expensive and limited due to the finite wafer size. Because the passive components are so area intensive it is impossible to fabricate these on chip for an RFID circuit. Thus these components must be made through low-cost processes and then attached to the chip. However, because of this attachment cost, it is very difficult to break the 5 cent cost barrier for a silicon RFID chip. For this reason it is necessary to print the whole RFID chip through low cost processes, and, hence the passive components form one of the critical components for ultra-low-cost electronics. [1]

The performance of inductors and capacitors are quantified by a term known as the quality factor, Q [2]. For an in-depth derivation and discussion of Q for both passive components and tank circuits see Appendix A. A high passive component Q is beneficial since more power is coupled into the circuit instead of being dissipated through parasitic losses (resistances) in the component. Thus, longer operating distances are achievable in RFID circuits with higher Q passive components.

Aside from requiring a high passive component Q it is also desirable to be able to design the proper parallel tank circuit Q (Appendix A). A high tank circuit Q is desirable since more power is coupled into the circuit. However, too high a Q will not allow proper circuit function because of manufacturing tolerances. For example, if the tank Q is too high, the bandwidth is more limited because of the steeper gain vs. frequency roll off (Figure A.4) [3, 4]. As a result the resonance frequency of the tank must be exactly tuned to allow proper communication. Given the abilities of printing it is not clear that the precise tuning could be achieved. Thus too high a Q is also undesirable and, in fact, an optimal tank Q is in the range of 20-30. [1]

To design the maximum component Q and the proper tank Q it is important to understand what dictates these parameters. The tank Q is dictated by the value of the inductor, L, capacitor, C, and load of the circuit, R_L. Thus it is critical that L and C be controllable values in the printing process. Furthermore, since the Q of an inductor is $\omega L/R_s$ (Equation A.1), and the Q of a capacitor is $1/\omega CR_s$ (Equation A.2), it is also important to minimize the resistance, R_s in both components.

In general, the equation to calculate the inductance for a flat spiral inductor is complicated and simulators such as ASITIC are used [5]. However, the relevant concepts can be understood using this approximation for a spiral:

$$L = \frac{r^2 N^2}{(2r + 2d) * 10^5} \qquad \textbf{Eqn 3.1}$$

where r is the average radius of the spiral, N is the number of turns, and d is the outer radius minus the inner radius. The inductance is directly related to the number of windings, and, though not obvious, the inductance is also related to the winding pitch.

This comes from the fact that for a given r and d the number of windings is determined by the pitch. Also, the resistance is the following:

$$R_s = \frac{\rho}{t} * \text{number of squares} = \frac{\rho}{t} * \frac{l}{w} \qquad \textbf{Eqn (3.2)}$$

where ρ is interconnect resistively, t is the interconnect thickness, l is the total inductor length, and w is the winding width. And, because a given resistance is dependant on the winding width, it couples into the pitch and therefore affects the inductance. Thus there is a complex interplay between the inductor resistance and inductor geometry. Furthermore, optimization is required to find the geometry for the highest inductor Q for a given tank Q [6]. Despite these complexities the important factors to this work are that the resistivity must be minimized, and the inductance must be controllable through the proper number of windings, winding width, and winding spacing.

The resistance in a capacitor is generally very low since it is dictated by the short interconnect leads. As a result the Q's in capacitors are generally higher than inductors. Because of this, the only important design feature of a capacitor is the value of the capacitance:

$$C = \frac{A\varepsilon}{t} \qquad \textbf{Eqn (3.3)}$$

where A is the capacitors area, ε is the dielectric constant of the insulator, and t is the capacitor thickness. Thus the fabrication of the proper capacitance requires the proper area and thickness control.

Given these fabrication requirements for inductors and capacitors, development of a printing technology requires the ability to print finely/uniformly spaced lines, to minimize the resistance of those lines, and the ability to control the dielectric thickness in

a capacitor or interconnect bridge. Despite this perceived simplicity the processing techniques can be rather complicated and this chapter seeks to explain the different techniques and strategies for printing each component.

3.2 Introduction to Printing

Electronic component fabrication using inkjet printing is completely different than the inkjet printing of pictographs. Image printing requires the control of two-dimensional drop placement to ensure the correct color droplet is placed in the correct location. Also, the jetting parameters are simplified because of the use of generally similar water based solvents. Electronic component fabrication requires three-dimensional droplet control, and to achieve this, the jetting parameters are usually more complicated [7]. For example, when printing interconnects, careful technique must be used in order to print lines with uniform cross sectional areas. The uniform cross sections minimize current crowding effects. Furthermore, capacitors and bridges require ultra smooth under layers to avoid pinholes and shorts. In order to fabricate uniform cross sections and smooth layers, careful control over drop morphology is necessary. Drop morphology control is accomplished through proper selection of the jetting parameters.

The jetting parameters for printing electronic materials tend to be widely varying because the solvents and inks used have a wide range of properties. In addition, it is important that the materials being printed have suitable properties to ensure proper jetting. Some of the relevant properties include boiling point, evaporation rate, surface energy, and viscosity. Typically if a solvent has a low boiling point it also has a fast evaporation rate. This is important because a solvent with a low boiling point and fast

evaporation rate will tend to clog the orifice of the dispenser or cause unstable jetting. This can lead to erratic droplet positioning that could cause shorts in interconnects or inductors where metallic ink drops have crossed lines. The surface energy of the solvent is important because if it has a low affinity towards a surface it will tend to ball up too much and create a rough line. In contrast, if it has a large affinity, then it will spread too much creating too thin a line. The viscosity is important because this will affect the voltage needed to eject it; higher viscosity solvents require higher jetting voltages and thus typically result in larger droplet volumes. The viscosity also affects the splashing of the drop because higher viscosity solvents typically resist splashing.

Along with the wide range of ink properties, another problem that earlier work by other research groups investigated was a phenomenon known as the "donut effect" or "coffee ring" [7-9]. This is a significant concern because it adversely affects line morphologies. This effect occurs as a droplet impinges at high velocity onto a flat surface. As the drop hits the surface the momentum is deflected outwardly from the center of the drop. The soluble material in the ink generally stays in solution and if the solvent dries too fast, there will not be adequate time for the drop to coalesce into a Gaussian shape.

Indeed this mechanism has been investigated by others through simulation and verified experimentally [10, 11]. These results are conceptually depicted in Figures 3.1A-D. These pictures show the changing drop morphology as it impinges on a surface. As the drop hits the surface the momentum is directed outward (Figure 3.1B) and already the outer ring begins to form. At some point in time the drop will have spread to it maximum (Figure 3.1C), and, at this point, the outer material in the ring will begin to pull back in. If

the solvent does not dry immediately then the droplet will rest in a final shape resembling that in Figure 3.1D. However, if the solvent does dry too fast, the droplet will remain frozen in the shape, resembling a coffee ring, as that in Figure 3.1C. This significant mass accumulation at the edges is due to the unsteady flow that is a result of the high speeds of the impinging drop. It is thus concluded that if a solution dries before achieving its surface tension dominated shape, then it will have significant mass pile up at the edges. This is detrimental to this work since it will result in rough morphologies.

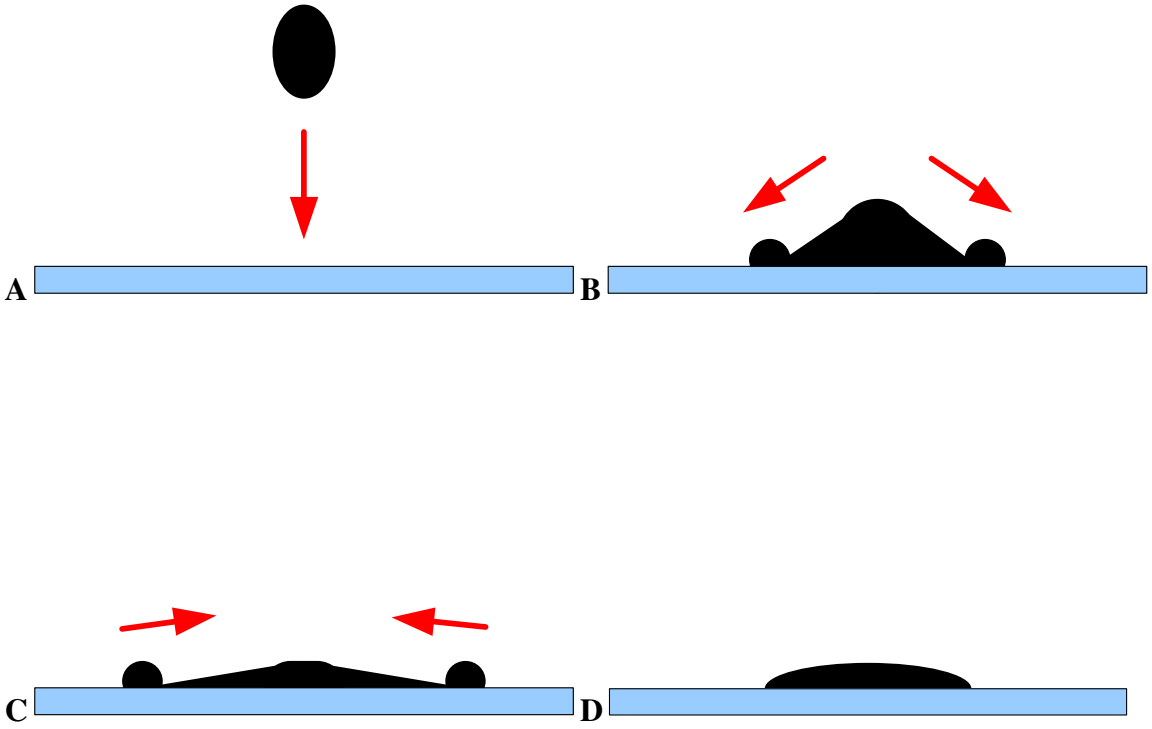


Figure 3.1: A-C; Cross sectional, conceptual depiction of a droplet impinging on a surface.

This impingement process suggests that there is also strong interaction between the properties of the solvent in the ink and the ambient temperatures around the droplet; further complicating this is the fact that clogging at the dispenser orifice can be a problem

that is strongly correlated to those same parameters. This chapter seeks to investigate this phenomenon further and find optimized inks and processing conditions for the fabrication of passive components including inductors and capacitors.

3.3 Introduction to Low Cost Electronic Inks

Because of the recent interest in low cost electronics there have been many different electronic inks developed specifically for this application. Over the past 5-10 years the performance of these inks has increased significantly such that they are now adequate to be used in electronics applications. The ink types can be divided into three main categories: semiconductor and interlayer inks, interconnect and contact inks, and dielectric inks. Over the past several years the majority of the work has focused on semiconductor development since this is generally the most difficult and gained the most notoriety. The interconnect inks have also gained a large amount of work, although not as much, and some inks are already being used in industrial applications. The dielectric inks have been researched the least because low cost transistors have yet to enter the market place and, generally speaking, it is easier to use conventional silicon methodologies to form dielectrics in test structures. This chapter will primarily focus on interconnect inks and lower performance dielectric inks for use in bridging technologies. Higher performance dielectrics are discussed in Chapters 5 and 6, while semiconductors are discussed in Chapter 4.

3.3.1 Interconnect Inks

Interconnects can be either organic or a combination inorganic/organic (these will be referred to as inorganic from now on) with the latter usually being of superior performance since they are generally metallic in form. The two most often used organic interconnects include poly(3,4-ethylenedioxythiophene) doped with poly (styrenesulfonate), PEDOT:PSS, and polyaniline, PANI [12-14]. These offer conductivities ranging from 10^{-1} S/cm up to $2*10^{2}$ S/cm and are also soluble in water making them ideal and simple to use inks for inkjetting. Water soluble polyaniline is a more recent development, where the polyaniline is protanated with a polymeric acid that induces water solubility [14]. The electrical properties of these organic interconnect inks are rather well studied. However, as already discussed, conductivities need to be maximized, and, because their conductivities remain too low, <200 S/cm, they are not very useful as interconnects.

There are generally two types of inorganic interconnect inks. First there are inks where metallic particles are added to a soluble binder. The mixture is mixed with a solvent that allows solution processing. Second, there are nanoparticle-based inks where nanosized metallic crystals are encapsulated with an organic molecule. This encapsulation creates solubility in common organic solvents that also allow solution processing.

Both of these inorganic inks require an anneal process to achieve maximum conductivity. For the particle/binder inks this anneal process drives out the solvent and solidifies the polymer binder. In the nanoparticle inks this anneal process drives out the solvent, de-encapsulates the nanoparticles, and sinters these particles together (Figure 3.2). These nanoparticle inks are particularly interesting because when they sinter, they

actually melt together and regain the bulk metallic properties of the material. This is because their high surface energy to volume ratio causes these nanoparticles to experience a reduction, ~500-1000°C, in melting temperature [15, 16]. This sintering temperature is strongly dependant on size and encapsulate. Generally speaking the easier the encapsulate boils off, the lower the temperature, and the smaller the particle, the lower the temperature.

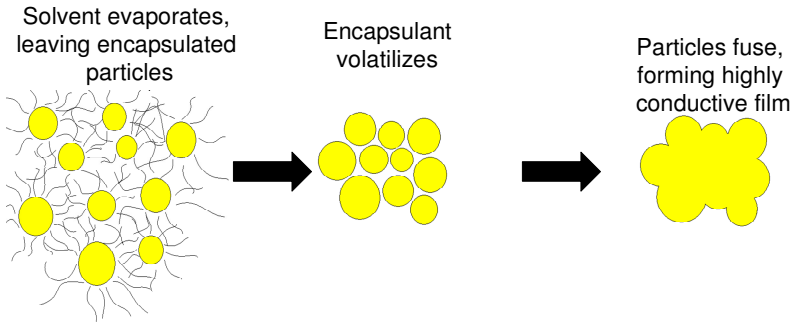


Figure 3.2: Nanoparticle annealing process.

Nanoparticle-based inks are generally the best materials for interconnects. Their properties, mainly conductivity, after annealing are superior since they closely resemble their bulk counterparts. Nanoparticle syntheses for gold, silver, and copper have been demonstrated and printed performance as high as $3*10^5$ S/cm has been achieved for gold [7, 17]. However, they are generally the most expensive materials because of the cost for raw materials and the chemistry required to make them. The raw materials generally include an ionic form of the metal, and the nanoparticles are generally synthesized through a reduction reaction in conjunction with encapsulation.

Metallic/binder inks generally have lower performance, ~$4*10^4$ S/cm, than the nanoparticle based inks [18]. This is because they are basically micron sized metallic

particles loosely bound by polymer binders. Furthermore, their fundamental make-up restricts their use in inkjet printing. The micron sized particles are generally not suited to inkjet printing because dispenser orifice diameters range from 20-60 μm. Thus, clogging is an issue. These inks also have surface roughness similar to the particle size. Hence, interconnects made with these inks cannot be too thin otherwise current crowding will significantly degrade performance. Because of these factors, these inks are more suited to gravure printing where large area and thick lines can easily be printed. This is further discussed in Chapter 8.

Out of the interconnect inks, the nanoparticle inks generally have the highest performance, followed by the metallic/binder inks, and then the organic inks (Table 3.1). Conductivities as high as 10^2 have been reported for variations of PEDOT. Thus adequate Q's for inductors are clearly not possible using these materials. However these materials do offer some advantages. They are easily inkjettable since many of them use water as a solvent. More so, they generally form better contacts to organic semiconductors than inorganic materials [14]. This issue could have significant performance enhancements for transistors.

Ink	Organic Printable Ink	Metallic/Binder Ink	Nanocrystal Ink (Au)
Conductivity Range	$0.3\text{-}2*10^2$ S/cm	$8*10^3\text{-}4*10^4$ S/cm	$1\text{-}3*10^5$ S/cm

Table 3.1: Summary of the performance range of the three main ink families.

Given the available materials and their properties, the nanoparticle inks are the best candidates for interconnect fabrication via inkjet. However most commercially

available nanoparticles are rather large, ~100-500nm, and therefore do not meet the requisite processing temperatures for plastic compatibility, <200°C. As a result, custom synthesized nanoparticles had to be engineered along with the development of a suitable ink for printing [16]. Appendix B describes the recipe for making these nanoparticles.

Beyond a certain size, ~5nm, smaller particles do not result in lower sintering temperatures. Instead, the temperature is controlled by the boiling point of the encapsulant. For this work, 1.5 nm gold nanoparticles encapsulated in butane thiol or hexane thiol are suitable candidates for plastic compatibility since their sintering temperatures are <120°C. However butane thiol encapsulation is found to be unstable as prolonged exposure to ambient temperatures, ~1-5 days, is enough to cause de-encapsulation. Thus 1.5 nm hexane thiol encapsulated Au nanoparticles were chosen as the basis for ink development. A TEM image of these nanoparticles is shown in Figure 3.3. These nanoparticles are used in all experiments referenced in this work.

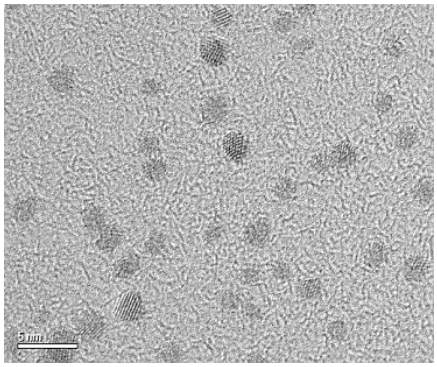


Figure 3.3: TEM of 1.5 nm Au particles used for interconnects and metal contacts.

3.3.2 Dielectric Inks

Similar to interconnect inks, there also exist organic and inorganic dielectric inks. However, the use of organic dielectrics is much more widespread than the inorganic inks. Inorganic inks can also be nanoparticle form; however they can also be selectively

deposited in low cost form via chemical bath deposition (CBD) [19-22]. CBD processes are still under development for use in low cost manufacturing and there exist very few if any publications about these processes in devices. A further, brief discussion of inorganic dielectrics will be provided in Chapters 6 and 8. Instead, the organic dielectrics have dominated the literature due to their ease of printing, availability, and adequate performance.

Polyimide is one such organic dielectric ink. Polyimide works well as a low cost electronic ink due to its liquid state before conversion. Furthermore, the viscosity can be controlled by the addition of thinner. However, most polyimides cure above 200°C while most plastic substrates cannot withstand temperatures above 200°C. As a result there exist very few polyimides with low enough conversion temperatures. More so, quite often those that convert under 200°C are not fully converted. Despite this, these inks can still be used in passive components [7, 23]. The methods to print one such polyimide are described below.

Another better performing dielectric, PVP or poly-4-vinylphenol, is a widely used organic dielectric. Infineon reported its practical use as a solution processable gate dielectric in 2002 [24, 25]. They reported that the leakage could be decreased by more than $2\mu A/cm^2$ at an equivalent electric field by using the correct amount of a cross-linking reagent, poly(melamine-co-formaldehyde). This was the most comprehensive study for this material and showed that this material could be a candidate for low cost printed transistors. While printing techniques for this material are briefly discussed below, the majority of discussion about printing this material can be found in Chapters 5 and 6.

3.4 Experimental Setup

All experiments were performed using the custom inkjet system, previously described. To develop the processes for forming inductive components and multilevel interconnects, the experiments were performed using the metallic nanoparticles previously described for conductor formation. A commercial polyimide and PVP were also used for dielectric formation. The droplet jetting waveform parameters, droplet spacing, choice of solvent, and substrate temperature during printing were varied. Resultant film morphology (as measured using optical micrography, profilometry, and AFM) and electrical conductivity were correlated to these parameters and used to drive the optimization of the processes. These parameters were used to demonstrate inductors and multilevel interconnects.

3.5 Results and Discussion

The piezo-head waveform parameters were optimized to maximize jetting velocity while ensuring good drop-to-drop stability and the absence of satellite droplets. By standardizing all experimental runs to this baseline, it was possible to specifically examine the impact of various process and materials parameters on film quality, for both the conductor and dielectric films.

3.5.1 Conductor Film Development

10 wt% hexanethiol-encapsulated 1.5 nm gold nanoparticles were dissolved in toluene. This was inkjet printed onto polyester substrates at room temperature. Due to the

velocity of inkjet-printed droplets, the "donut" effect resulted upon impact of the droplet. After the evolution of the splash wave, the evaporation of the toluene resulted in the formation of a coffee-ring or donut structure. As described, this is a known problem with inkjet printing. For conductor development, this is a crucial issue, since it results in the production of rough films with high sheet resistance. Owing to their roughness, these films are generally unsuitable for use in multilayer interconnect structures, since overlying dielectrics are prone to pin-holes due to the poor coverage of the numerous ridges and valleys. The structure of a typical film showing the coffee-ring effect is presented in Figure 3.4.

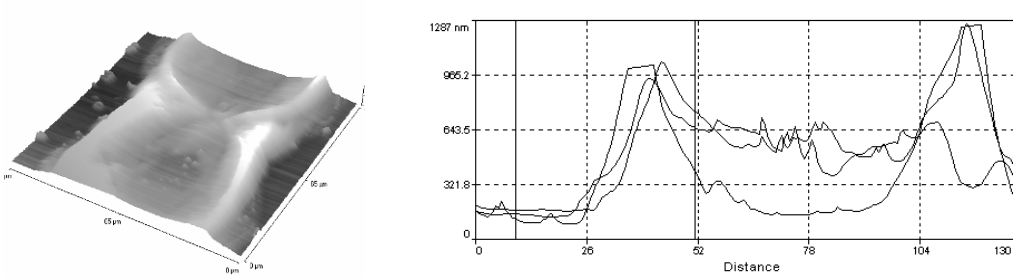


Figure 3.4: (left) Atomic force micrograph showing the characteristic "coffee-ring" structure that results from splashing during droplet deposition, and (right) profilometry of a typical film formed using this process, showing the substantial roughness.

One solution to this problem is to increase the evaporation rate of the solvent upon droplet deposition on the surface, preventing the splash wave from traveling, and hence eliminating the formation of the coffee-ring. This is achieved using substrate heating to enhance the evaporation rate of the solvent at the droplet surface. Indeed, upon raising the substrate temperature to 130°C, the toluene solvent evaporates almost instantaneously

upon droplet deposition, eliminating more than 80% of the coffee-ring. This is apparent in Figure 3.5.

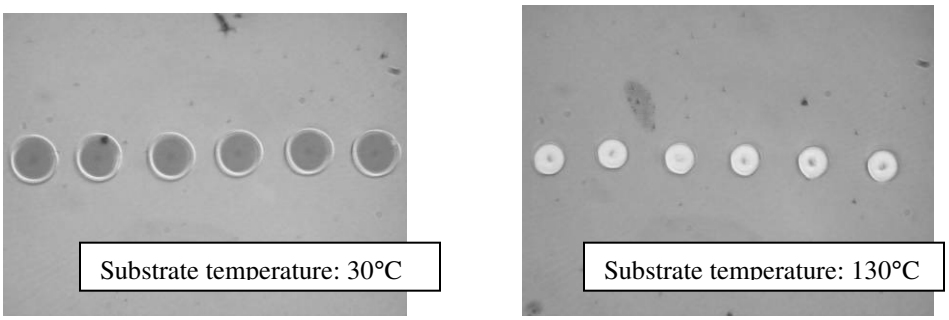


Figure 3.5: Effect of substrate temperature during deposition on coffee-ring splash effect. Notice the dramatic reduction in the central coffee ring hole in the droplets on the right.

By overlaying droplets with a spacing substantially less than the droplet diameter, it is possible to use successive droplets to "fill" the coffee-ring produced by previous droplets. This results in the formation of films with improved smoothness, and almost complete elimination of the ridges at the edges of the film. Due to the small coffee-ring contribution from each drop, however, the center of a printed line is somewhat thinner than the edges, as shown in Figure 3.6.

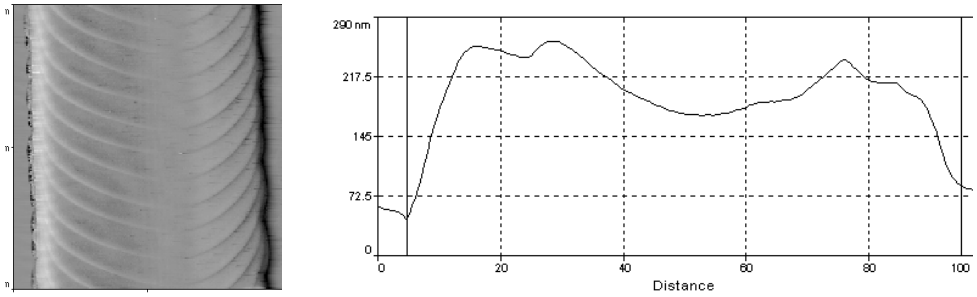


Figure 3.6: Overlaying of successive drops to reduce the coffee-ring splash effect.

There is a disadvantage to using substrate heating to reduce the coffee-ring effect, however. To achieve good control on droplet placement, typical inkjet systems maintain a head-to-substrate distance of less than 2 mm. This results in substantial convective heat transfer to the head, which in turn results in enhanced evaporation of solvent at the nozzle tip. Consequently, there is an increased likelihood of partial and complete clogging of the head, resulting in tremendous process stability and reliability concerns while inkjetting. To solve this problem, several experiments with a variety of lower-evaporation rate solvents were attempted. In particular, there was excellent success using α-terpineol. The use of this solvent has several advantages. First, due to the slower evaporation rate of the solvent at the nozzle, it offers excellent clog resistance. Second, due to its higher viscosity compared to toluene, it provides a larger optimization window for substrate-heating-based control of the coffee-ring, and enables complete elimination of the coffee-ring effect at 160°C. By syncopating droplets, it is possible to produce extremely smooth lines, with no ridges and negligible cross-sectional thickness variation, as shown in Figure 3.7.

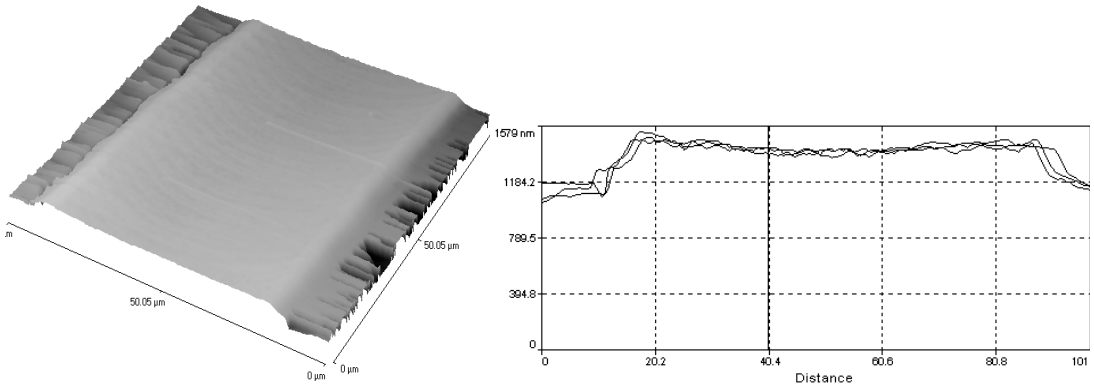


Figure 3.7: Smooth conductor lines obtained by printing gold nanoparticles dissolved in α-terpineol at a substrate temperature of 160°C.

By using a combination of solvents and substrate heating, α-terpineol and toluene, conductivities as high as 70% of bulk gold have been obtained in thinner films. This was believed to be a result of efficient evaporation of both solvent and encapsulate. Because of the addition of the lower boiling point toluene the overall solvent content is less after conversion. Further data supports this below (Figure 3.8). However, due to the differential evaporation of the solvent at the orifice the mixture was found to jet extremely unstable and thus future experiments used α-terpineol exclusively due to its stability in jetting.

Printing at elevated temperatures using α-terpineol has an additional advantage [23]. Due to the higher-temperatures, the alkanethiol is removed more efficiently, resulting in lower sheet resistance, as shown in Figure 3.8. This removal of the alkanethiol has been previously identified as an important requirement for producing low-resistance films. Sheet resistances as low as 23mΩ/square have been obtained in 1μm thick films.

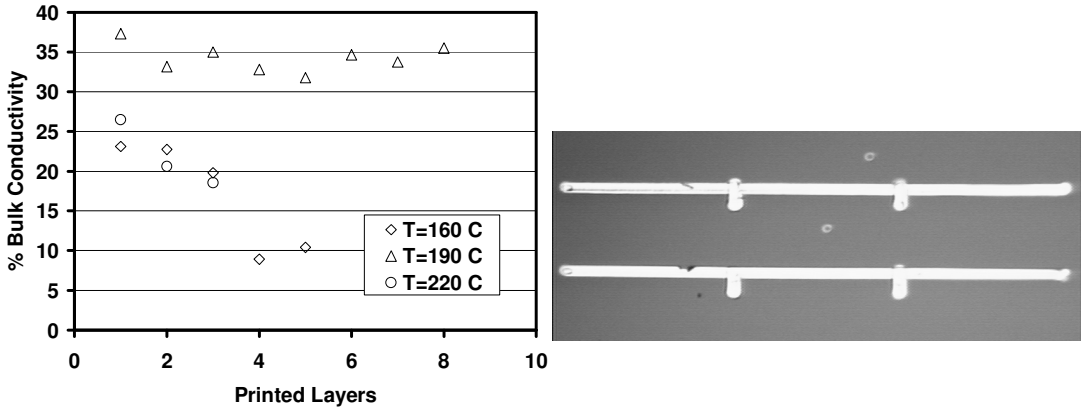


Figure 3.8: Variation in conductivity with temperature and number of syncopated layers (left) [23], as measured using a four-point sheet resistance structure (right).

While this technique of printing onto elevated surface temperatures produces both high conductive and well defined lines and structures, it does not produce completely smooth surfaces. As seen in Figure 3.7, although the line has a relatively uniform cross-sectional area, there still exist small ridges approximately several 100 nm large in the lines. Furthermore, it has been found that the "flash evaporation" also causes roughness ~0.1-0.5μm in the films. This is discussed in Chapters 5 and 6.

This roughness is especially detrimental to gate stack structures where any roughness in bottom layers necessitates thicker dielectric films to prevent pinholes and leakage. As a result ultra-smoothness is desired for transistors and another technique has been developed to address this issue. Instead of using higher substrate temperatures to prevent donut formation, lower substrates temperatures, 30°C, in conjunction with slower evaporating solvents, i.e. α- terpineol, can be used. In this case the drops are allowed to "pool up" or coalesce and thus allow the surface tension of the ink to smooth the film. This is the case where the drop in the simulation is allowed to completely reflow (Figure 3.1D). After, the solvent is slowly evaporated off at 55°C for an hour. This creates the smoothest possible film. After drying the solvent the dry gold nanoparticles are annealed at 200°C to form the bulk gold. However, the main disadvantage to this technique is that because the drops are allowed to "pool up" there is little or no control over the shape definition of the patterned being printed. This technique is further discussed in Chapter 5.

3.5.2 Dielectric Film Development

Dielectric film development proceeded in an analogous way to the development of the conductor films above, i.e., higher substrate temperatures will create well defined

shapes but rougher films, while lower temperatures create smoother films, both being relative to the solvent evaporation properties. However, an additional constraint is applied to dielectric films that is less critical for the conductors; in dielectrics, it is desirable to always allow some reflow of the individual drops to eliminate pinholes and voids formed between drops, and also improve step coverage. Temperature therefore plays an important role in this optimization; polyimide films deposited at room temperature may flow too much, and produce highly distorted films, while films deposited at temperatures that are too high produce films that have numerous pinholes, which must be subsequently filled using multiple layers. This distortion due to reflow is believed to be exacerbated due to the high surface tension of the polyimide, i.e., it is more energetically favorable to ball up rather than form a smooth film. This process could be likened to Volmer-Weber thin film growth where islands form immediately due to the large surface energy difference. This is unacceptable for capacitors, since it results in an increase in the dielectric thickness and a consequent reduction in specific capacitance. At intermediate temperatures (the specific values of which depend greatly on the polyimide used and the concentration of the printing solution), it is possible to form films that reflow enough to fill pinholes but do not result in the formation of distorted and agglomerated films. This is shown in Figure 3.9. These elevated temperature prints also produced relatively thick films >0.5μm.

Although the polyimide reflowed too much at low temperatures, the PVP was found not to have the same problems. The solution was found to wet the surface extremely well, resulting in ultra smooth, continuous films. Thus no elevated temperatures were required

to print the PVP and as a result much thinner films were obtainable with this solution. An in depth discussion of this material is discussed in Chapters 5 and 6.

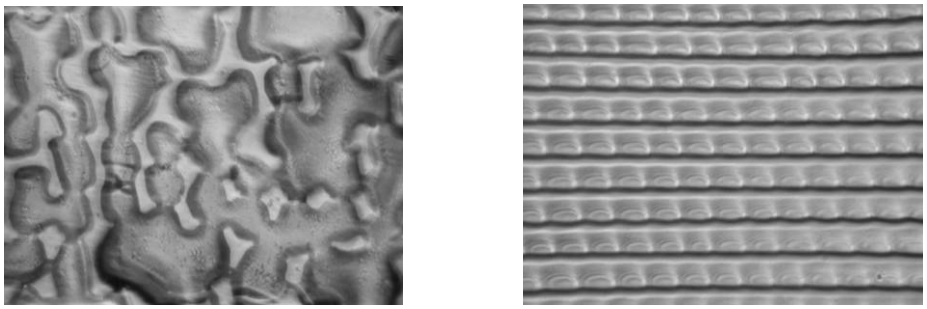


Figure 3.9: Printed dielectric layers showing the agglomeration that results at low temperatures (left), and the smooth films achieved at intermediate temperatures (right). At high temperatures, the lack of reflow results in pinholes.

3.5.3 Multilayer Interconnect and Inductive Component Demonstration

To form multilayer interconnects, the conductor and dielectric technologies described above are integrated. As a representative structure, perpendicular crossing interconnects separated by a dielectric layer were made. To ensure good step coverage by the dielectric layer, high substrate temperatures are used, with multiple passes to ensure absence of pinholes and reduced cross-talk between layers. The use of lower temperatures results in reflow off the step, increasing the likelihood of shorts between the conductor layers. Combining the dielectric and conductor technologies, a variety of inductors with bridges were demonstrated (Figure 3.10).

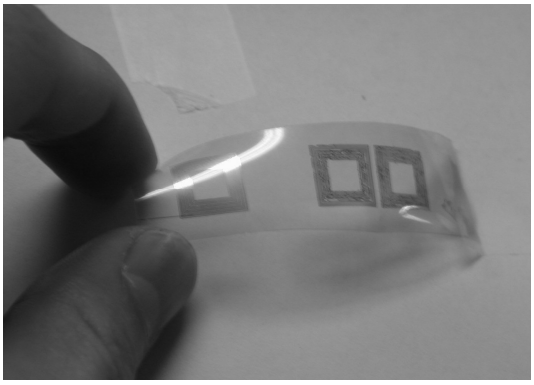


Figure 3.10: The conductor and dielectric technologies developed herein allow us to demonstrate multilevel interconnects with few shorts, and also demonstrate inductors with high Q's.

3.6 Conclusions

High-quality passive components are a crucial component technology required for the demonstration of low-cost all-printed electronics and in particular RFID. Precise fabrication of the Q factor of the tank circuit (~20-30) is crucial to allow proper function of a RF circuit. Furthermore, circuit operation is optimized for higher passive component Q's. These items can be accomplished by minimizing the resistivity of the interconnect material, and controlling the line width, spacing, and film thickness.

Inkjet printing of electronic components is much more complicated than that of pictographs. This is mainly because of the wide variety of inks and associated solvent properties. Of particular concern is a phenomenon known as the "donut effect." This effect was shown to be a result of the droplet freezing as is impinges the substrate's surface. In these experiments the freezing was due to rapid solvent evaporation.

Because of these printing effects, proper ink selection and formulation are critical. There are a wide variety of inks including organic and inorganic. For inkjet printing the best metallic inks are nanoparticle-based inks. The best dielectric inks include polyimide and PVP.

Using gold nanoparticle-based conductors and polyimide and PVP dielectrics, inkjet printing has demonstrated a high-quality interconnect and inductive component technology that offers high levels of conductivity in a printed film, enabling the demonstration of high quality inductors and a robust multilevel interconnect scheme. By optimizing the deposition parameters, the most important of which are substrate temperature and choice of solvent, it is possible to produce low-resistance conductor lines and dielectrics with excellent surface morphology and electrical characteristics. The processing parameters used for the materials in this chapter are used in the remainder of this work. Furthermore, the technical knowledge gained in the process development for the inks in this chapter is applied to the process development of newer inks in later chapters.

Chapter 4

Low Cost Semiconductors and Printing

4.1 Introduction to Low Cost Semiconductors and Transport Processes

While there has been a great deal of interest in low-cost electronics, the majority of work over the past ten years has focused on organic semiconductor development [1]. This is because they are the one of the main performance limitations in low-cost devices. Thus, much of the work is focused on improving performance while maintaining their solution processability. Although these materials don't yet offer superior performance over inorganic semiconductors at equivalent low processing temperatures, they offer some unique advantages that inorganic materials have yet to show. Organic semiconductors have a relative low degree of crystalinity, and because of this they generally have two distinct properties. They are relatively easy to solution process or make solution processable and they have a large amount of mechanical flexibility. The tradeoff to these properties is that these materials generally have lower mobility in transistors. Despite this, the solution processability and flexibility make them ideal candidates for low cost flexible electronics [2].

There have been several examples of silicon based thin film transistors (TFT) in large area flexible electronics but these do not necessarily include an all-additive process [3-5]. Thus, the main problem with low cost inorganic semiconductors is that they generally are not as easily solution processed. And, if they can be solution processed,

they generally do not have the high purities required to achieve the high performance of conventional electronics. This is in contrast to organic semiconductors where there are a variety of solution purification techniques available for soluble semiconductor materials. These techniques cannot be used with inorganic semiconductors because they are insoluble after synthesis.

Some low cost inorganic semiconductor manufacturing methods include soluble chalcogenides [6], nanoparticle-based materials [7, 8], or using chemical bath deposition [9], CBD. The fundamental problem for these types of materials is that low-cost solution processing techniques are inherently unclean. The problem is exacerbated in nanoparticles that use organic encapsulates to induce solubility. Although all these materials promise superior performance over organics, it remains to be seen if this is obtainable, especially since the crystallinity needed to reach high performance is disrupted by these inherently unclean techniques. Another issue is that due to the low processing temperatures the inorganic semiconductors typically have small grains which further reduce performance [10].

Furthermore, the low processing temperatures not only cause many traps at grain boundaries in thin films but also at the semiconductor/dielectric interface [11]. These traps make threshold voltage control a challenge. This issue can be improved by using the proper inorganic dielectric but the development of these dielectrics is difficult and these low cost processed materials have yet to be incorporated into devices [12-15]. This issue will be discussed a little more in Chapter 6 with respect to high k dielectrics. Overall, it remains to be seen whether using inorganic semiconductors can achieve significantly

better performance than their organic counterparts with respect to a low-cost solution process and flexibility.

Because of the difficulties with inorganic semiconductors and the very large body of work already developed in organic synthesis, the majority of work to develop semiconductors for low-cost electronics has focused on organic semiconductors. Although this class of materials offers a wide variety of types there are many common features in their structure that allow for conducting/semiconducting behavior. In general, molecules that show good conduction or mobility have aromatic rings. The aromatic rings are essential due to the electronic overlapping π orbitals that form a continuous electron cloud (Figure 4.1). In these continuous clouds the electrons are free to move and are not associated with any particular atom. Thus, the delocalized electrons in these orbitals are able to freely traverse the molecule as long as there are overlapping π orbitals with which to cross. Because the orbitals are delocalized they also increase the interactions with neighboring molecules. When these delocalized orbitals overlap with adjacent molecules, they allow the electrons to jump intermolecularly. [16]

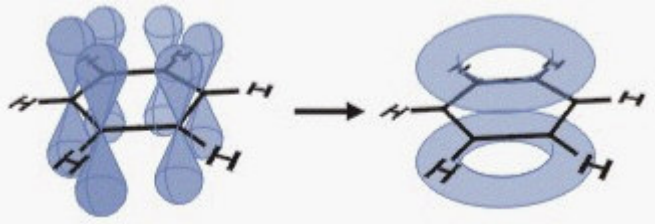


Figure 4.1: Delocalized π orbitals (left) form a continuous electron cloud (right) where electrons are free to move.

Aside from some of these conduction mechanisms, there is still much debate about the specific models used to describe the conduction processes. In particular there

are two different models that most believe describe the conduction. The first model is known as the variable range hopping (VRH) model [17]. An in depth description of this model is in Appendix C, however the main ideas are described here. The basic idea is that there are too many deep traps to allow conventional band transport. As a result electron conduction occurs as electrons hop from trap to trap. There are a few unique properties of this conduction mode. First, mobility will increase with an increase in temperature. This happens as the carriers have more energy to jump from trap to trap. This contrasts with conventional inorganic semiconductors, where mobility decreases with temperature due to an increase in phonon scattering. Another unique characteristic is that there is an electric field dependant mobility. This occurs because as the field increases, the deep trap states are filled and hence the energy of the states contributing to conduction is raised. Thus the energy required to hop is lowered.

The other transport model is known as the multiple trap and release (MTR) model [18]. This model is also described in Appendix C, but the main idea is that there are extended states at and above the band edges and there are localized states within the band gap that periodically trap and release carriers from the extended states. Thus the carriers spend their time moving in the extended states or trapped in the localized states. This model will have the same mobility enhancement, but these models differ in their temperature dependence. The MTR model can have three temperature gradients. First, similar to above, the mobility will increase with temperature as the carriers are more easily released from the localized states. Second, as the temperature lowers, the carriers are unable to release form the localized states and instead hop between them. Third, at even lower temperatures, the carriers do not populate the localized stares and instead hop

through states near the Fermi level. This hopping between sates near the Fermi level is believed to be a mechanism similar to the VRH model. It is believed that the MTR model applies to the more crystalline semiconductors while the VRH model applies to the crystalline materials at low temperatures and also the less ordered materials that cannot display MTR transport (Appendix C).

4.2 Common Organic Semiconductors

As previously stated the important property of these organic semiconductors is that they are usually made with aromatic rings. In particular, it is generally best if the molecular backbone is made of these aromatic rings. Some common aromatic rings are benzene and thiophene. Two organic semiconductor examples composed of these rings are pentacene that is made up of five benzene rings and the polythiophene class of semiconductors that has thiophene rings throughout the backbone (Figure 4.2). These make good organic semiconductors because the benzene and thiophene rings are aromatic and thus the electrons can easily move across these molecules. In addition to this backbone, organic semiconductor molecules typically also contain functional groups at the ends of the molecule to increase ordering, interactions with the substrate, and induce solubility (Figure 4.2D) [19]. The easy addition of these functional groups through organic synthesis offers great flexibility and thus is another major reason why organic semiconductors have gained such interest. For example, consider the case of polythiophene (Figure 4.2D). It can be made with several different alkyl chain lengths and the alkyl chains can be capped with a wide variety of functional groups. The end caps

can promote adhesion to certain a substrate which aids in assembly while the alkyl chains, too, aid in assembly and orientation.

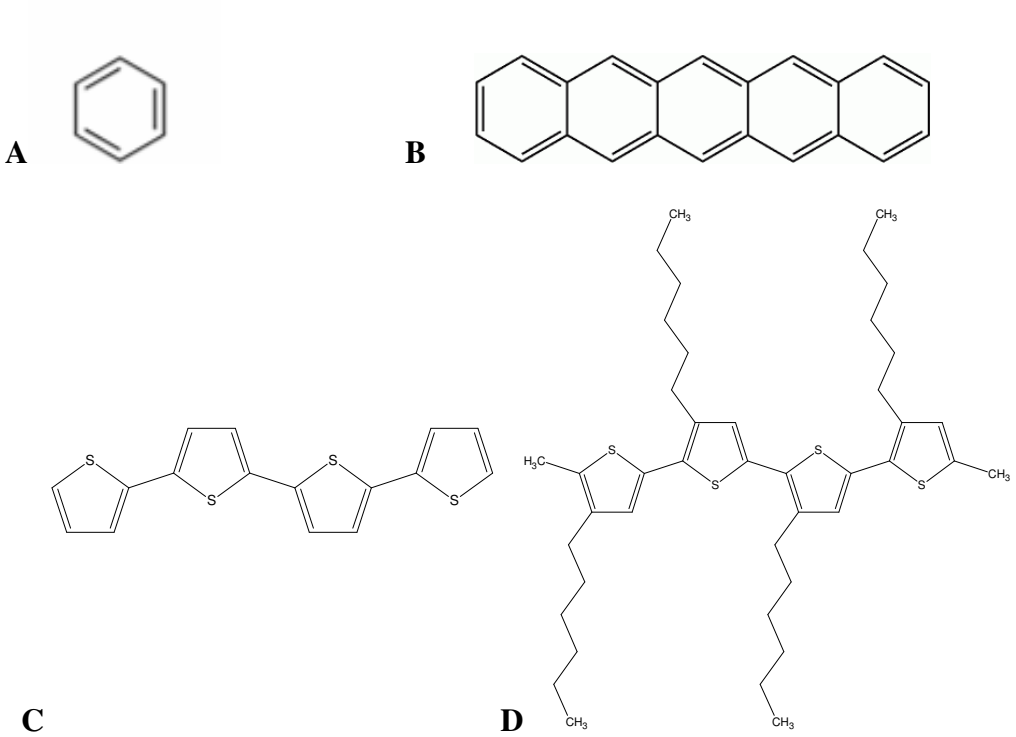


Figure 4.2: Benzene molecule (A) is the basic building block of pentacene (B). The thiophene backbone of the tetrathiophene molecule (C) has the same backbone as regioregular polyhexylthiophene (D). The functional groups in polyhexylthiophene help induce solubility.

The length of the backbone also has implications on the properties of the semiconductor. In general if a molecule has a short backbone, 1-10 units long, it can be classified as a small molecule or oligimer. If a backbone has an "infinite chain" it is referred to as a polymer. Thus, in general, organic semiconductors can be classified into two categories- small molecule and polymer semiconductors. Each has its own advantages and disadvantages. The main advantage of polymer semiconductors is that

they tend to be more easily solution processed because their long chain lengths aid in solubility. This occurs as the long molecules tend to fold over one another and break up packing and crystallinity. This is also a disadvantage since degraded packing will be detrimental to mobility and air stability. Mobility is degraded since the less tightly packed material will have larger distances for the electrons to traverse between molecules. It is also important to note that the mobility in these polymers also suffers as a result of the generally impure solution processes used to synthesize them. And because of their large size they are hard to purify. The looser packing also allows oxygen to permeate more easily into the thin film. Oxygen doped polythiophene does not allow good transistor action as devices are not able to turn off. It is rather easy to add functional groups to the backbone to enhance assembly and packing further but this only helps mobility to a limited extent. [20]

The small molecules in contrast generally show better semiconductor performance at the cost of processing simplicity. This is a result of the fact that they can generally pack better and have higher crystalinity due to their smaller size and interactions of the aromatic rings. Consider pentacene that packs edge to face. There are no folding issues associated with the molecules and with the high degree of interactions among the π orbitals in adjacent molecules electrons are able to easily traverse intra- and inter- molecularly. [20]

Along with the better overall semiconductor performance due to the better packing and crystalinity, this class of molecules also demonstrates better air stability, but lacks the ease in solution processing. Because of the tight packing resulting from the aromatic interactions, air has a more difficult time permeating thin films made of these

small molecules in contrast to polymers. As a result, this class of materials is also much more air stable. The disadvantage of this is that solvents also have a harder time dissolving the material. This is for essentially the same reason; the tighter packing does not easily allow the solvent molecules to work themselves in between the tightly packed molecules. Because of this, these small molecules are sometimes evaporated. This has the advantage of a purer deposition technique, but clearly this is not compatible with a high throughput low cost process. [20]

Overall, it can be seen that there is a trade off between better packing for better performance and air stability versus ease of solution processing. However, progress is being made to overcome this tendency. One example is to use a small molecule precursor [21, 22]. The idea being that the precursor molecule is functionalized such that it does not pack well. One deposited, it can be annealed so that the functional group boils off and the pure small molecule is left. It thus has the same properties of the pure form with high performance and air stability. One such molecule is a pentacene precursor described below and is used in the experiments in this chapter [22].

Another idea is to engineer molecules with the exact shape needed to allow good packing but also allow for solubility. It is analogous to building blocks. One example of this is triisopropylsilyl pentacene or TIPS pentacene as shown in Figure 4.3 [23].

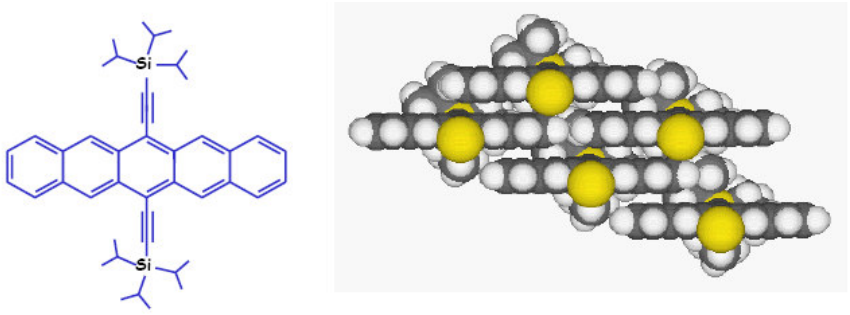


Figure 4.3: TIPS pentacene (left) and its packing configuration (right).

This molecule packs very well as shown but because of bulky TIPS functional groups, solvent molecules can penetrate and thus this material can be solution processed.

4.3 Introduction to Printed Thin Film Transistors

In recent years, there have been many studies of spin coated organic transistors [24, 25]. Although this type of manufacturing simplifies characterization, it is not usable for full circuit fabrication due to the necessity for isolation, which is problematic in organic semiconductors. Because of this, a more desirable type of manufacturing, inkjet printing, has been studied. Some of these studies have used polythiophene [26], a commonly available commercial organic semiconductor. One of the only solvents polythiophene is soluble in is chloroform, which evaporates very rapidly. Thus it is extremely difficult to inkjet, and furthermore it is well known that it is very sensitive to oxygen. One other semiconductor that has been inkjetted is F8T2 [27]. Although this material has been successfully inkjetted it has yielded performance less than that of polythiophene. In fact, both semiconductors, when inkjetted and without the aid of interlayers, have mobilities less then 10^{-2} and $I_{on/off}$ less then 10^{4}. Such characteristics are not sufficient for many low cost electronic applications since the maximum operating frequency will be in the range of a few kilohertz. For example, FCC-mandates will likely necessitate RFID operation at 135 kHz or 13.56 MHz (higher frequencies, such as 900 MHz and 2.4 GHz are also being investigated for silicon-based RFID, but are likely out of the realm of realistic printed RFID technology). A further, in-depth discussion of frequency requirements is in Chapter 7.

For many years it has been known that pentacene is the best organic semiconductor with mobilities >2 cm^2/V-s [28]. This is primarily due to its highly crystalline structure. However, this crystalline structure is also responsible for its insolubility. Recently, Afzali, *et al.* has developed a synthesis whereby a bulky side chain is added to pentacene and therefore creates solubility [22]. After the precursor is deposited, it is annealed, and pure crystalline pentacene is left. Here, optimization schemes for inkjetting this material will be investigated [29].

4.4 Precursor Optimization Experimental Setup

Pentacene precursor was manufactured in house by reacting pentacene with N-sulfinylacetamide via a Diels-Alder reaction as shown in Figure 4.4. For a detailed synthesis see Appendix D. This compound breaks the aromaticity of the pentacene and dramatically increases solubility. After reacting, the precursor is purified using an ethyl acetate/hexanes flash column. After purification the precursor is converted back to pentacene by annealing for approximately 2 minutes at 120°C to 200°C in a pure nitrogen atmosphere.

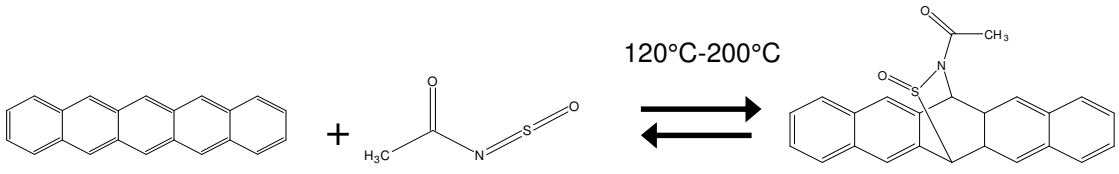


Figure 4.4: Diels-Alder pentacene precursor formation.

The performance of this pentacene precursor was evaluated by inkjetting various numbers of drops onto a silicon-based test substrate. The test substrate was prepared as follows:

A heavily doped silicon wafer was oxidized to form 120nm of thermal SiO_2. Gold source/drain pads were formed using conventional lithography, evaporation, and lift-off. During this step, alignment marks were also formed on the wafer to enable alignment of the printed organic semiconductor to the lithographically patterned electrodes. The net result of this fabrication process was the formation of a substrate-gated TFT structure with a high-quality thermal oxide gate dielectric. This is advantageous for materials screening, since it ensures a uniform comparison of materials characteristics independent of gate-dielectric-induced performance degradation.

4.4.1 Experimental Parameters

As discussed in Chapter 3 the ink formulation is critical to successful inkjetting. In order to properly inkjet the precursor, a relatively slow drying solvent had to be found that was able to dissolve a sufficient amount of material. This ensures that the material does not dry and clog the dispenser and also dries slowly enough to avoid donut shaped structures on the wafer. Anisole was found to satisfy these requirements where the precursor can be dissolved up to 2.1 wt. % at room temperature.

The precursor was printed at concentrations of 1.7 wt. % and 2.1 wt. % in anisole. Using the alignment routine the precursor was dispensed onto devices with sizes of 100μm x 5, 8, 10, 15, and 20 μm. A cross section of the device is structure shown in Figure 4.5. For each device the number of drops was varied from one to three. Large areas of films were also made by dispensing thousands of drops. Drops were dispensed on to the electrodes over the whole wafer so that the wafer could be split in half. One half was annealed at 160^{o}C and the other half was annealed at 180^{o}C. Both anneals were 2

minutes long and preformed in a dry nitrogen atmosphere with less than 20 ppm oxygen. These experimental parameters are summarized in Table 4.1.

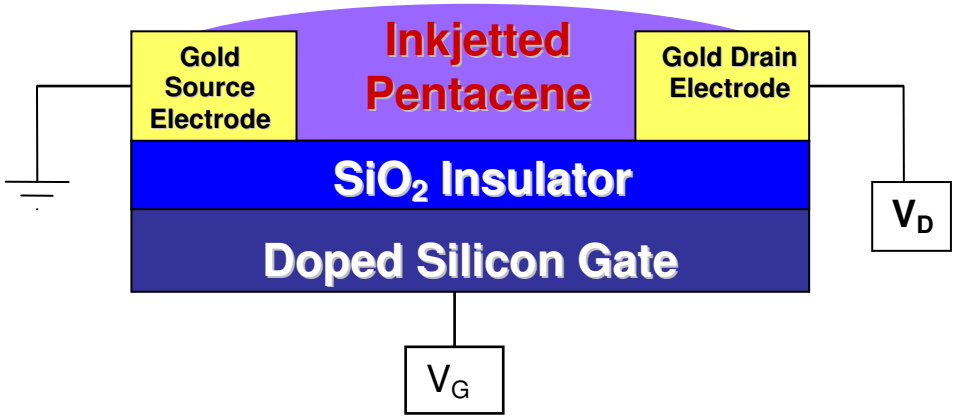


Figure 4.5: Device structure cross section.

Temperature and Time	Drops	Concentration	Device Size
160°C, 2 min 180°C, 2 min	1,2,3	1.7%,2.1%	100x 5,8,10 µm

Table 4.1: Experimental parameters.

I_D-V_G and I_D-V_D curves were obtained for each device using a HP 4156 in a nitrogen atmosphere. This nitrogen atmosphere avoids contamination of the organic semiconductor by oxygen. AFM measurements were also obtained to correlate the number of drops to the thickness of the film.

4.4.2 Results and Discussion

Field effect mobilities were extracted from the I_D-V_G curve using the following relation derived from the square law:

$$\mu_{SAT} = \frac{g_m^{\ 2}}{2I_D C_{OX}\left(\frac{W}{L}\right)} \qquad \textbf{Eqn 4.1}$$

Using this formula ensures that the mobility is independent of threshold voltage. This is important because of the variability in threshold voltage of organic devices. $I_{on/off}$ ratio data was extracted by taking the current at V_D=40V and V_G=40V and dividing it by the current at V_D=40V and V_G=0V.

Typical I_D-V_D and I_D-V_G curves are shown in Figure 4.6. The I_D-V_G curves are well behaved without any threshold shifts or DIBL. The I_D-V_D curve, however, does show indications of a significant barrier at the source and drain contacts as seen by the concavity of the I_D curve at low V_D. This is attributed to a contact barrier between the pentacene and the gold electrodes [30].

The average performance data for the annealed sample carried out at 160^{o}C is shown in Figure 4.7. Inkjetting one drop yielded no working transistors because there is not enough material in one drop to cover the channel of a device. The dashed line in the graph represents the films produced by inkjetting several thousand drops in one spot on the wafer.

There are two important trends in the graph. First, as the number of drops increases so does the average mobility of the devices. Secondly, as the number of drops increases the $I_{on/off}$ ratio decreases. These trends are attributed to the fact that as the number of drops increases, the film thicknesses also increase. Thus, greater film thickness creates higher mobility, but also creates more leakage current that lowers the

$I_{on/off}$ ratio. The result is similar to polysilicon TFTs and the reasons for this are the same. As the thickness increases the gate has less control over the thicker region since the gate controls the film through capacitive coupling. Since the thicker films weaken the capacitive coupling, the leakage increases.

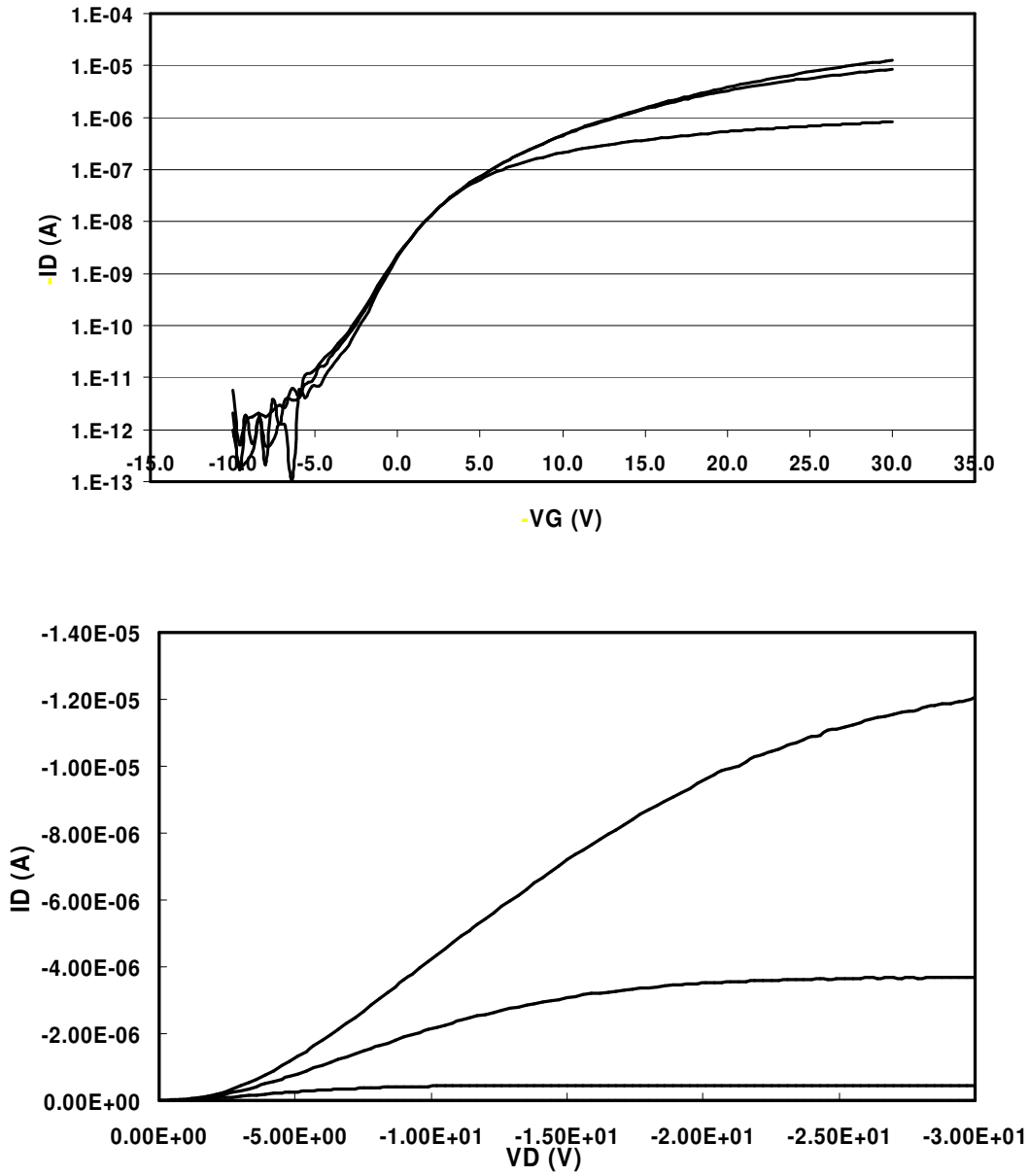


Figure 4.6: Typical I_D-V_G (top) and I_D-V_D (bottom) curves; W/L=100/5 μm, μ=0.099cm^2/V-s, $I_{on/off}$=10^4.

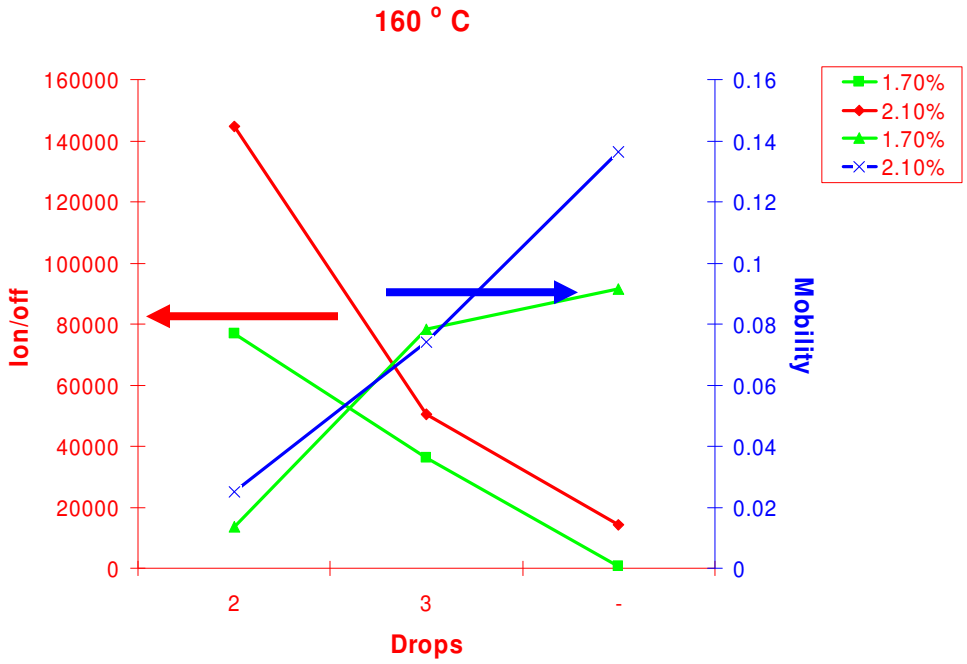


Figure 4.7: Average performance of transistors annealed at 160°C.

These trends also hold when comparing the different concentrations of precursor. For the higher concentration (2.1 wt. %) there is a higher mobility, but lower $I_{on/off}$. This is also attributed to the fact that the higher concentration will create a thicker film.

It can also be seen that annealing at 160°C has superior performance for both mobility and $I_{on/off}$ (Table 4.2). The average mobility is twice as good while the average $I_{on/off}$ is four times as good. This is believed to be because the semiconductor de-wets from the substrate at higher temperatures and thus degrades the performance of the film.

	160° C	180° C
Best Mobility $cm^2/V\text{-}s$	0.193	0.102
Best $I_{on/off}$	$3.9*10^5$	$1.0*10^5$

Table 4.2: Comparison of best transistors at 160°C and 180°C anneals.

Analysis of the AFM data of these drops does confirm that more drops do indeed create thicker films. As shown in Table 4.3, 2 drops is equivalent to a film thickness of 1000Å over the channel, while 3 drops is 2500Å, and the continuous film made by several thousand drops is 3300Å.

Drops	Thickness
1	--
2	1000Å
3	2500Å
film	3300Å

Table 4.3: Thickness vs. number of drops.

4.5 Material Improvements

There are several techniques, including chemical, fabrication, and structural, that can improve and optimize the performance of this material. One chemical technique is further purification that can be done to increase the intrinsic mobility of the material. For example, many of the solvents used to purify this precursor, in particular, hexanes, often contain plasticizers. These plasticizers will have a detrimental effect both on packing and the electron transport itself. Thus their presence will result in a marked decrease in performance. The plasticizers are removed by distilling the solvents.

4.5.1 Solvent Distillation Experiment

As an example, a short experiment was carried out to test if indeed the solvents contain these plasticizers. The precursor was purified using flash column chromatography with fresh solvents. Wafers were prepared by the exact same method as above. After the

column, both a precursor sample rinsed in distilled hexanes and one not rinsed (control) were spun onto a wafer at 2 wt % and 6000 rpm. The wafers were annealed at three different temperatures (150, 165, and 180 ºC) for 2 min in a nitrogen atmosphere. The resulting devices were tested and performance parameters were extracted identically to the above devices.

4.5.2 Results

The results of the experiment are summarized in Table 4.4. Clearly, the distilled purification solvents had a marked increase in mobility. At all temperatures, the distilled rinse has a higher performance with an increase as much as 50% in mobility. Except for the 165 ºC anneal, the samples also showed >2X improvement in $I_{on/off}$ ratio. The hexane rinse still showed a higher $I_{on/off}$ in the 165 ºC sample but not quite 2X. This slightly less increase is most likely due to data scatter. A larger experiment would be necessary to verify this. Overall, though, the increase in performance is due to the removal of impurities introduced by the hexanes.

Anneal Temp. (ºC)	Rinse	Ave. μ (cm^2/V-s)	Ave. $I_{on/off}$
150	N	0.10	$3.6 * 10^6$
150	Y	0.14	$1.3 * 10^7$
165	N	0.088	$3.0 * 10^6$
165	Y	0.12	$3.4 * 10^6$
180	N	0.047	$2.5 * 10^6$
180	Y	0.076	$6.9 * 10^6$

Table 4.4: Results of distilled hexane rinse experiment.

4.5.3 Further Improvements

Along with this, more research needs to be done focused on the ideal fabrication conditions including anneal temperature and time. Higher anneal temperature may yield better crystallinity but this may also breakdown the impurities or cause dewetting of the material from the substrate. Both effects degrade the performance of the devices made with this material [19].

The performance of this material in a device is also highly dependant on the type of structure it is integrated into. For example, it has been shown that a top contact device performs better than a bottom contact device when using organic semiconductors [20, 31]. This is attributed to the fact that by evaporating onto the organic layer, a better interface can be formed between the two materials.

Another way to improve the quality of these interfaces is by using interlayers. Interlayers can help for two reasons. First, the interlayers can help improve ordering between an inorganic material (i.e. the electrode or dielectric) and the organic semiconductor. Second, the interlayers can help buffer energy drops and barriers between dissimilar bands. This has an added effect of preserving the interface since the carriers lose less energy, but normally this excess energy aids in interface degradation. This results in improved reliability.

The data in Figure 4.6 shows that there is a significant barrier at the source and drain as seen by the concavity of the I_D-V_D curve. It has been shown that this barrier can be reduced with the use of interlayers including HMDS and OTS [20, 32, 33]. This will increase the mobility of this material further.

4.6 Conclusions

Organic semiconductors are particularly applicable to low cost flexible electronics for several reasons. Because of their organic nature they are inherently flexible, can be easily solution processed, and the large body of knowledge in organic synthesis allows specific tailoring and great flexibility of their properties. The delocalized π orbitals allow electronic transport both intra- and inter-molecularly. The two models used to quantify the transport are the variable range hopping model and the multiple trap and release model. The latter is believed to be more applicable to higher crystalline organic semiconductors.

Some of the more common organic semiconductors include derivatives of pentacene and polythiophene with the former being higher performance. One such material is a pentacene precursor developed by Afzali *et al.* This particular material is well suited to inkjetting as it offers both high performance and solution processing. An ink formulation was developed for this material and optimization schemes for characterization and performance have been obtained showing that as the thickness increases so does the mobility. However, with thicker films, the $I_{on/off}$ ratio decreases, thus the appropriate thickness must be chosen for the correct application. By obtaining mobilities of 0.1-0.2 cm^2/V-s the intrinsic performance of this material suggests that these devices may be suitable for many electronic applications.

Further optimization of this material is required. This includes both intrinsic material performance and device structure. Using distilled solvents yielded higher performance by as much as 50% demonstrating that better purification creates higher

intrinsic performance. With better device structures and interlayers higher performance is also possible.

Chapter 5

A Baseline Process for All-Printed Transistors

5.1 Introduction

The motivation for the development of low cost and, in particular, printed electronics has already been addressed in the previous sections and thus will not be repeated. The required inks for all-printed transistors include an electrode/interconnect ink, a dielectric ink, and a semiconductor ink. The previous sections detailed the minimum required performance for the electrode and semiconductor inks. However, little was discussed about dielectric performance requirements especially in the context of printed transistors. This is because the performance requirements for transistors far exceed that of other components such as passive component capacitors. Thus, in order to gauge the requirements of the dielectric and evaluate the overall materials integration, transistors must be fabricated and tested. Indeed, there have been many examples of low-cost transistors (not necessarily printed) [1-4]. However, these examples suffer from either an inferior semiconductor, an inferior interconnect technology, or are not fully additive. This chapter seeks to develop a baseline all-printed process flow using the high quality materials previously discussed and to evaluate the overall integration of these materials [5].

5.2 Experimental Setup

The transistors described in this paper were fabricated using the custom formulated, in-house synthesized inks. These inks were printed using the custom built inkjet testbed and were deposited onto PET substrates that can withstand temperatures up to 200°C. A short summary of the inks is provided here.

I_D-V_G and I_D-V_D curves were obtained for each device using a HP 4156 in a nitrogen atmosphere. This nitrogen atmosphere avoids contamination of the organic semiconductor by oxygen. Performance parameters were exacted using same process as used in Chapter 4.

5.2.1 Ink Formulation

The inks used to fabricate the devices were custom formulated and synthesized in-house as previously described. Metal contacts were printed using the gold nanoparticle-based inks using processing techniques previously described. The average diameter of the nanoparticles was ~1.5 nm, resulting in a sintering temperature of ~120ºC, which is compatible with many low-cost plastics. The ink used to fabricate these devices was a ~10 wt. % solution of hexanethiol encapsulated nanoparticles in α-terpineol.

Significant development was required to find a suitable gate dielectric. Initially the previous polyimide was used as a gate dielectric, however this was found not to work because of a differential wetting effect. As seen in Figure 5.1A the polyimide prefers to wet the gold gate electrode instead of the plastic substrate. As a result the dielectric covering the gate was too thick (>0.5μm). The previously reported PVP dielectric [6, 7] was also printed. However, when using the initial formulation with the PGMEA solvent, the solution did not produce uniform films as the solvent dried too fast and seemed

"sticky" as it coated the substrate, Figure 5.1B. Thus, the gate dielectric used was based on the original PVP based ink; however, the solvent chemistry was modified to be suitable for inkjet printing. The dielectric solution used in the fabrication was a 7.6 wt % solution of PVP in hexanol with 0.625 % by volume of the cross-linking reagent added as previously described (Figure 5.1C).

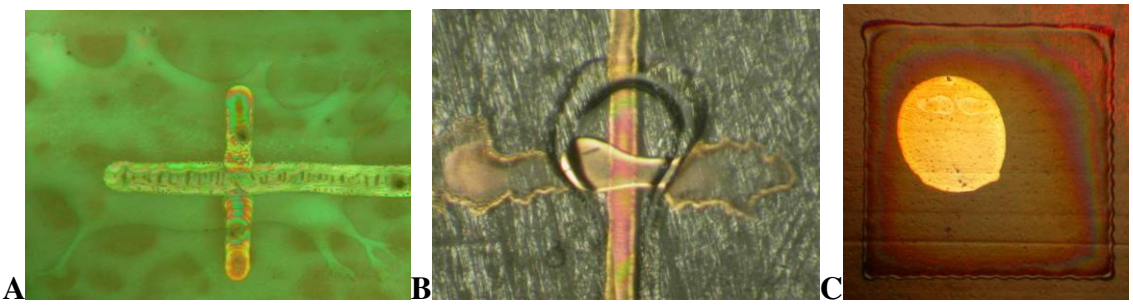


Figure 5.1: A; Printed polyimide gate dielectric. B; Printed PVP dielectric with PGMEA solvent. C; Printed PVP dielectric with hexanol solvent.

The semiconductor ink was formulated using the previously described soluble pentacene precursor. Upon annealing at plastic-compatible temperatures (~160ºC), the precursor converts to pentacene, which offers substantially improved performance and air stability over most other printable semiconductors. The ink formulation was a 1.8 wt. % solution of the precursor in anisole as described in Chapter 4.

5.2.2 Baseline Process Flow

The process flow for device fabrication is shown in Figure 5.2. The overall transistor structure is a bottom gate structure. The dielectric is deposited on top of the gate, followed by the source and drain electrodes, and then finally, the organic

semiconductor on top. The entire process was performed in a custom inkjet printing system using commercial piezoelectric heads from MicroFab, Inc. A commercial PET plastic was used as the substrate. Note that all plastic substrates used herein were preshrunk at or above the peak process temperature to minimize substrate compaction and enable proper layer-to-layer registration.

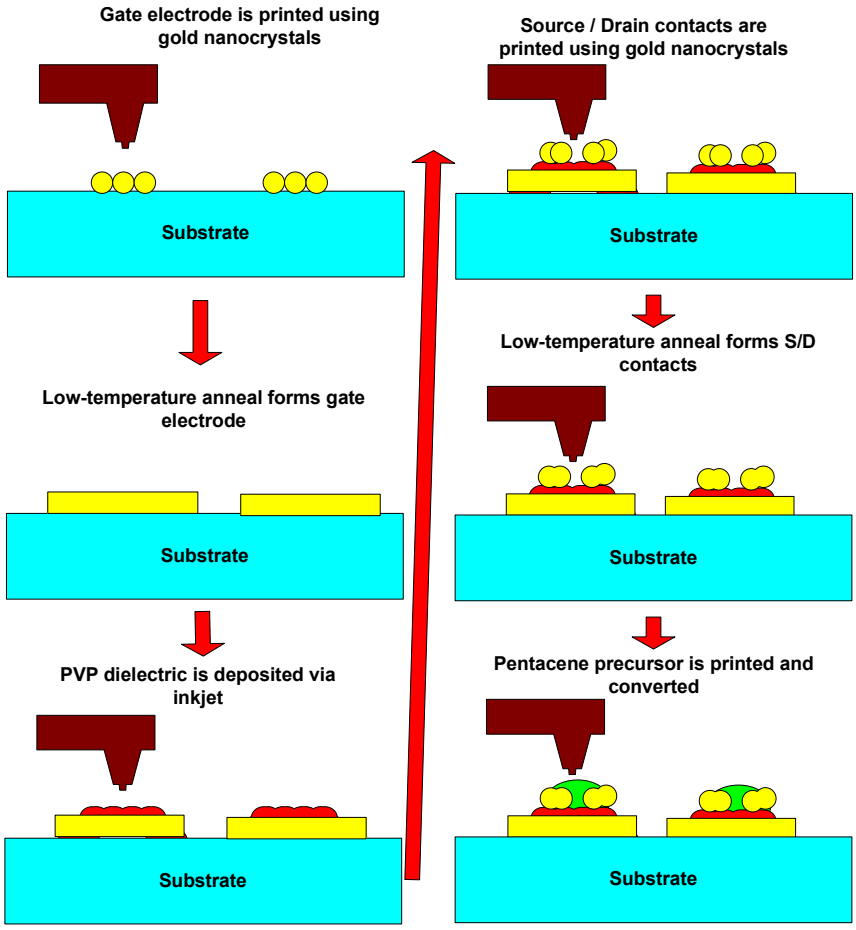


Figure 5.2: Process flow for formation of printed FETs.

The gate electrode was printed at near-ambient temperatures, and dried at 55°C for 1 hour. Subsequently the nanoparticle pattern was converted at 200°C to form high-quality polycrystalline gold. Due to the limits of the testbed, quasi-annular test devices

had to be fabricated. Next, a PVP gate dielectric was printed. The solution was annealed at 100°C for 1 min to drive out the solvent and at 200°C for 10 min to thermally cross-link it. Various gate dielectric thicknesses were investigated (Figure 5.3). To achieve adequate yield with low gate leakage, it was necessary to use relatively thick gate dielectrics resulting in high device operating voltages. This is due to the roughness of the bottom gate layer. Suitable optimization of the materials and printing processes should allow the use of thinner gate dielectrics, thus resulting in reducing operating voltages. This is discussed in the next chapter, 6.

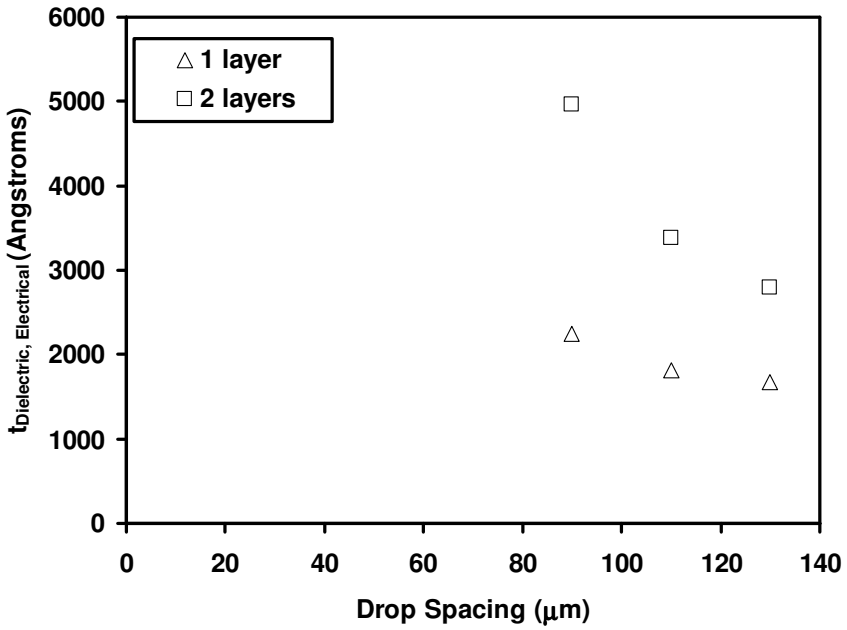


Figure 5.3: Effect of jetting parameters on thickness of inkjetted dielectric.

Gold source/drain electrodes were printed and were simultaneously annealed at 165°C. The S/D electrodes were printed at elevated temperatures to ensure instantaneous curing. This enabled precise control of line width, enabling the reliable realization of lines separated by gaps as short as 15μm (Figure 5.4). Other gate lengths were also made,

as shown in Figure 5.4. Based on the line width limitations of the gate electrode, a fully-overlapped gate structure was necessary. This is primarily a limitation of the print-head used for this work; several groups have demonstrated inkjetted features as small as 20µm, so use of a suitable head technology should eliminate this problem.

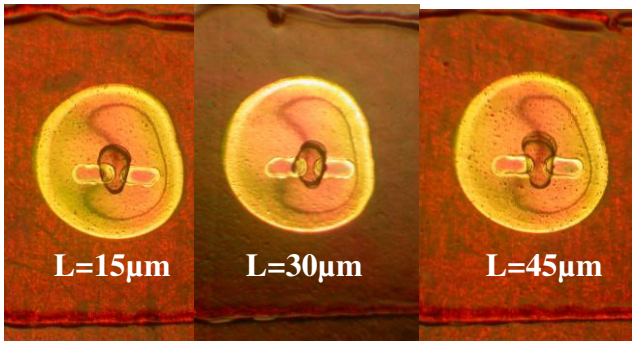


Figure 5.4: Optical micrographs of various printed FETs.

Finally, the semiconductor solution was deposited at room temperature and annealed at 165°C for 2 min in a nitrogen atmosphere with <12ppm oxygen. As a control, devices were also fabricated using a substrate-gated architecture: heavily-doped silicon wafers with thermal SiO_2 gate dielectrics and evaporated gold S/D electrodes.

5.3 Jetting Techniques

During fabrication of these devices the proper processing parameters must be tuned in the ink formulation and ink processing conditions to ensure proper smoothness and drop morphology. By using some of the techniques described in Chapter 3 these baseline devices were fabricated. The techniques to print the higher performance PVP dielectric are also described here.

5.3.1 Electrodes

Due to the "donut effect" as described earlier, the gold gate electrodes for the baseline process were printed at low temperatures ~30°C. Then, by slowly evaporating off the solvent at 55°C for an hour, the smoothest possible film was created. After drying the solvent, the dry gold nanoparticles are annealed at 200°C to form the bulk gold. Since the films are ~2000Å and are smoothed via surface tension, the thick gold film also tended to smooth out roughness in the plastic. However, the disadvantage to this technique is that because the drops are allowed to "pool up," there is little or no control over the shape definition of the pattern being printed. As a result, the gates form large annular shapes (Figure 5.4) and overlap capacitance lowers AC performance. Eliminating these problems is addressed in the next chapter, 6.

The source and drain electrodes were printed onto a surface with elevated temperatures. By creating a situation were the solvent "flash evaporates," the material in the solution is not given a chance to spread and create the ring structure. Using this technique well defined electrodes were fabricated (Figure 5.4). However, the drawback to this technique is that the surfaces of these structures are rough both on large (~50μm) and small scales (~0.1-0.2μm). As a result, this technique is not suited for bottom structures where pinholes are concerns in bridges and capacitors.

5.3.2 Dielectric

By changing the drop spacing and solution concentration, very accurate PVP dielectric thickness can be printed (Figure 5.3). Printing is done at room temperature

(30°C) and the layers are inkjetted using a technique similar to that used to make the gate electrode where the drops are allowed to congeal. Again, the smoothest possible films are made.

5.3.3 Semiconductor

Printing the pentacene precursor also requires the proper technique. Several drops, at least 5, were required in order to cover the channel completely, however depositing the drops in immediate succession caused them to "pool up" and roll off the relatively thick (~2000Å) electrodes as shown in Figure 5.5. To get proper coverage individual drops were deposited along with a small wait state in between each deposition to allow each drop to dry completely (Figure 5.4).

Figure 5.5: Discontinuous semiconductor film resulting from thick electrodes and "pooling" of drops.

5.4 Results and Discussion

Transfer characteristics and output characteristic I-V curves are shown for the devices made with an inkjetted gate in Figures 5.6-5.9 with W=120µm and L=45µm, L=15µm. Because the gold gates are printed onto bare plastic, a thick gate dielectric had

to be used, 1000-5000Å, to overcome the roughness of the plastic. As a result, large operating voltages had to be used (40V-100V). Despite this, the maximum observed mobility was 0.17cm^2/V-s (Figures 5.6 and 5.7), with a maximum gate field of 2MV/cm, and on-off ratios as high as 10^4 were obtained. It is important to note that although a high mobility was obtained, the electric field was not sufficient to saturate the field dependant mobility of the organic semiconductor.

In comparison to the control devices made on silicon, at similar gate fields, the Si-based devices (Figure 5.10) showed similar mobilities ~0.2 cm^2/V-s. Also, in the output characteristics of the inkjetted devices vs. the control devices there is much less concavity in the linear region indicating a much smaller contact barrier at the source and drain contacts.

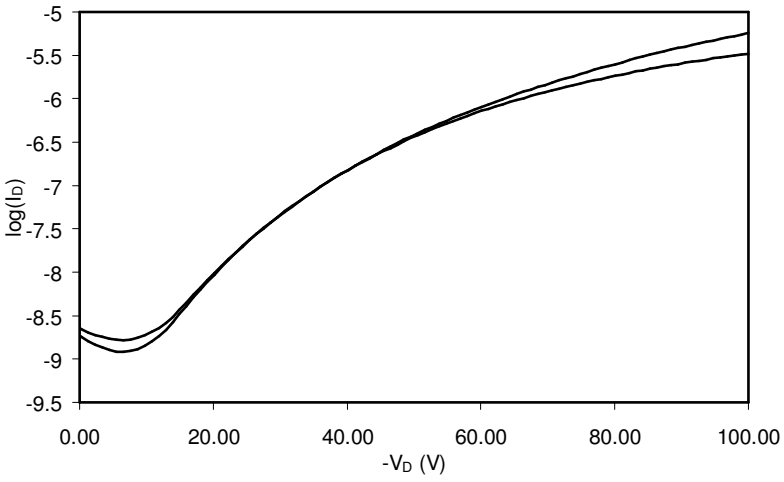


Figure 5.6: Transfer characteristics for a 120µm/45µm device, $t_{dielectric}$ ~ 5000Å; µ ~0.17cm^2/V-s.

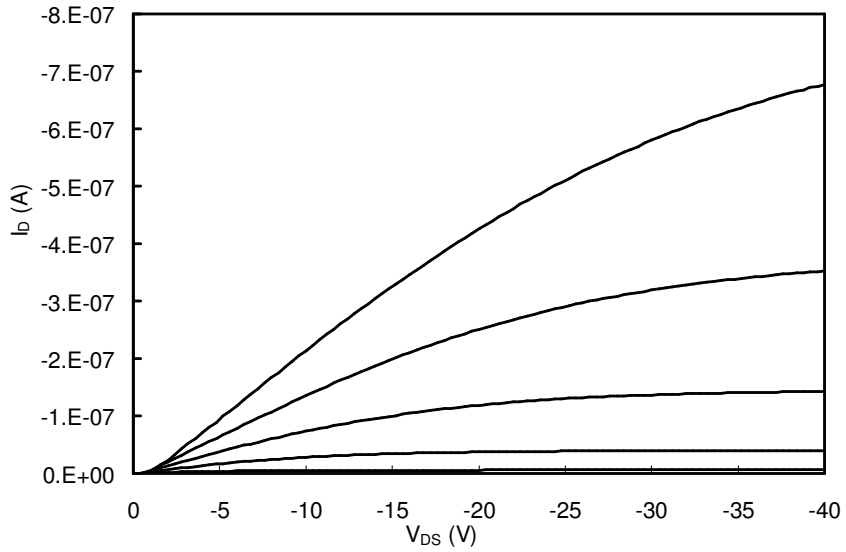


Figure 5.7: Output characteristics for a 120µm/45µm device, $t_{dielectric}$ ~ 5000Å (µ ~0.17cm^2/V-s).

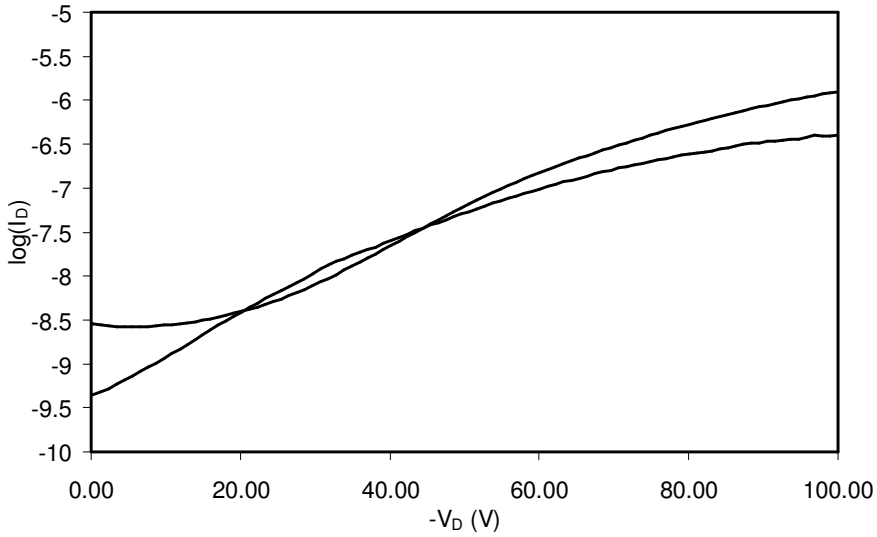


Figure 5.8: Transfer characteristics for a 100µm/15µm device, $t_{dielectric}$ ~ 5000Å; µ ~0.1cm^2/V-s.

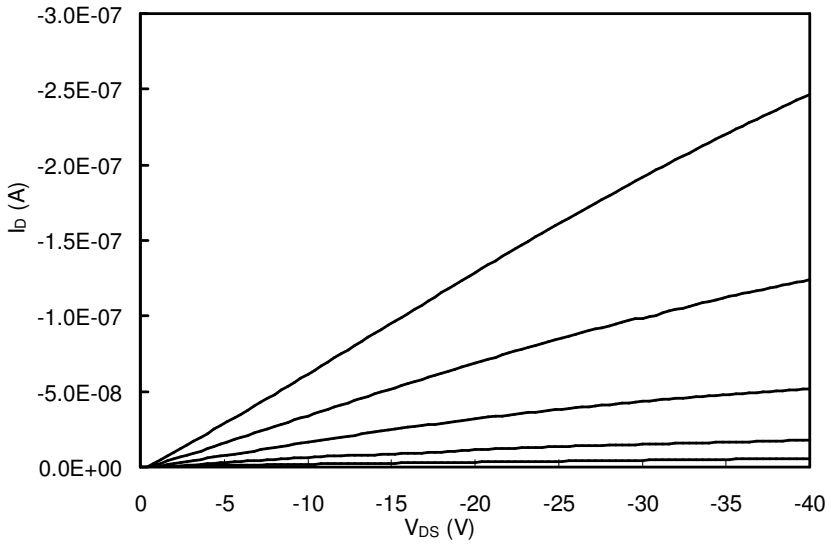


Figure 5.9: Output characteristics for a 120µm/15µm device, $t_{dielectric}$ ~ 5000Å (µ ~0.1cm^2/V-s).

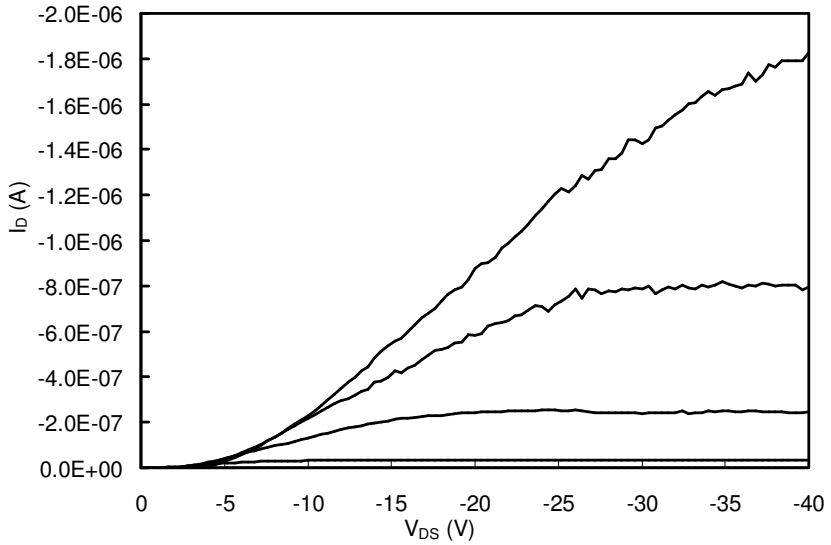


Figure 5.10: Output Characteristics of OFET on Si/100nm SiO_2 stack, showing similar characteristics to printed FET at equivalent fields.

Due to the roughness of the plastic it is clearly seen that there is a limit to dielectric scaling. Figure 5.11 shows the reduction in $I_{on/off}$ due to gate leakage. This data was exacted from the I-V curves at low V_{DS} bias and high gate bias. The low V_{DS} ensures a uniform electric field across the length of the channel. In general, while thinner dielectrics were found to improve on-current and reduce operating voltage, defects in the thinner dielectrics were found to dramatically increase gate leakage, resulting in a reduction in on-off ratio with decreasing $t_{dielectric}$ (Figure 5.11). Optimization of the gate dielectric is therefore a crucial issue and is discussed further in Chapter 6.

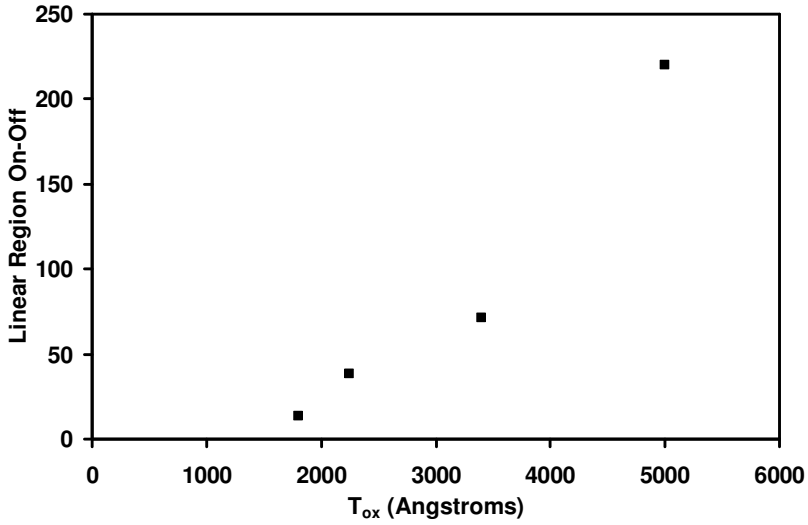


Figure 5.11: Variation in on-off ratio (in linear regime, at low S/D bias, to ensure uniform gate leakage) with dielectric thickness. Despite an increase in drive-current, on-off ratios decreases due to substantially enhanced gate leakage.

5.5 Conclusions

A baseline process for an all-printed transistor was developed. This demonstrates all-inkjet-printed transistors are feasible to make. In order to make these devices, the

proper ink formulations and printing techniques must be used for each layer in order to obtain the proper smoothness, shape definition, and thickness. For the case of a gold gate the smoothest possible patterns are necessary and thus require the use of low temperature printing. This allows the ink's surface tension to promote smoothness. The dielectric is printed in the same manner, and thickness can be controlled by drop spacing and concentration. It is more important for the source and drain electrodes to have well-defined shapes to ensure the smallest possible channel length and hence high temperature printing is used. A wait state is required between drop depositions of the organic semiconductor to ensure that the drops cover the channel of the devices.

The overall performance of these devices is rather good, especially the DC parameters of the baseline devices. Despite the fact that the electric fields were only 2MV/cm in these devices they still obtained mobilities approaching 0.2 cm^2/V-s.

The two major shortcomings of these devices is the high operating voltages required to run the devices and the non-optimal structure (annular) for high frequency operation. This was a result of two issues. First, the roughness of the substrate caused rough gate electrodes. Second, the limits of the minimum line widths of the testbed combined with the required smoothness of the electrodes required a large gate electrode. Using a large gate pad eliminated the possibility of pinholes at the edges of a thin electrode and simplified the baseline process. These issues are addressed in the next chapter, 6.

Chapter 6

Gate Dielectric Scaling

6.1 Introduction

The baseline process developed in the previous chapter suffers from both high minimum operating voltage requirements and low maximum operating frequency. This chapter seeks to optimize the device structure and fabrication in an effort to address these issues. In the previous chapter, the minimum operating voltage remained high because the gate dielectric could not be scaled. In particular, as the dielectric thickness decreased the gate leakage increased and lowered the $I_{on/off}$ ratio (Figure 5.11). In general, this phenomenon occurs often in organic dielectrics especially in conjunction with low cost plastic substrates that are relatively rough [1, 2]. With low mobilities, ~0.1 cm^2/V-s, the problem is exacerbated further and normal operation is difficult to achieve. This is because leakage becomes a higher percent of the drain current with the lower transconductance values. This is in contrast to conventional silicon transistors where mobilities are > 300 cm^2/V-s and thus the 3000X increase in mobility will allow a 3000X increase in gate leakage. Therefore, to achieve low voltage operation, these materials must be integrated into structures with relatively low gate leakage that is significantly lower than an equivalent silicon device. Since the target is an ultra-low-cost device the dielectric must also be deposited using some form of printing. Given these issues there are two routes to take to develop these low operating volt devices [3].

Currently most dielectrics that can be solution processed are polymers such as PVP and polyimide. These materials typically have a dielectric constant of 3.6. Given

this, the devices need gate dielectric thicknesses well below 500 Å in order to achieve sub 10 V operation required for most electronic applications. As demonstrated in the previous chapter by the dielectric scaling, this puts very tight tolerances on the roughness of the bottom layers. However, it may be possible to achieve such tolerance with the use of a smoothing layer or using extremely smooth plastic [4].

Another solution to this problem is to use high k dielectrics. By implementing these materials, thick dielectrics can be used to reduce leakage and pinholes while operating voltages <10 V can be maintained. The main obstacle is developing low cost processing techniques, but there are ideas that do exist including using organometallics, chemical bath deposition techniques, or nanoparticles [3, 5-8]. The chemistry is rather difficult to synthesize these inorganic materials especially when high purities are necessary. To date these materials have produced little or no publications related to devices. This chapter investigates the feasibility of the first method mentioned above.

6.2 Experimental Setup

The transistors described in this paper were fabricated using the same custom formulated, in-house synthesized inks as previously described. By refining the previous baseline process flow sub 10V structures with minimal overlap capacitance necessary for higher frequency operation were fabricated onto plastic substrates, PEN, which can withstand temperatures up to 200°C. Commercial inkjet systems can achieve line widths <20μm with good smoothness [9, 10]. However, in the last chapter the baseline process involved printing a large gate electrode at low (near-ambient) temperatures to create the smoothest possible surface. Because of this low temperature printing, the gate structure

was poorly defined due to ink reflow prior to drying. Thus source and drain electrodes completely overlapped the gate. This resulted in large overlap capacitances.

With the current inkjet platform the desired <20μm dimensions realized by state of the art inkjet systems cannot achieved. Therefore, to simulate state of the art inkjet, the gate was evaporated with smooth profiles required for pinhole free films. All other processes were performed using inkjet to enable evaluation of thickness scaling and material performance.

Identical ink formulations were used as in Chapter 5 (gold nanoparticle ink, pentacene precursor ink, and PVP dielectric ink) with the exception that two different PVP concentrations were used for this ink, 7.6 wt. % and 3.9 wt. %, instead of one.

Device characterization was carried out by extracting capacitance and I-V data from gate stack structures. ID-VG and ID-VD curves were obtained for the optimized transistors using a HP 4156 in a nitrogen atmosphere.

6.3 Substrate Engineering

All commercially available plastics evaluated, PET and PEN, were found to have significant roughness with peaks as high as 5000Å. In the baseline fabrication process, as described in the previous chapter, 5, this issue was neglected. However, upon scaling of the gate dielectric this issue was found to be critical. To address this issue, a PEN plastic substrate was used as the substrate and 2 layers of 12 wt. % PVP in PGMEA with cross-linking reagent were spun onto the substrate. Anneals were performed after each deposition. The resulting layer was ~1 μm thick. The PVP acted as a smoothing layer, and allows for more aggressive scaling of dielectric thickness, as will be discussed below.

6.4 Process Flow

The process flow for device fabrication is shown in Figure 6.1. A pre-shrunk PEN plastic substrate was used. First, two ~0.5 µm thick PVP smoothing layers are spun onto the plastic. Anneals are performed between each spin. The gold gate electrode was next evaporated (~150Å) onto the plastic through a shadow mask to simulate commercially inkjetted lines as discussed above.

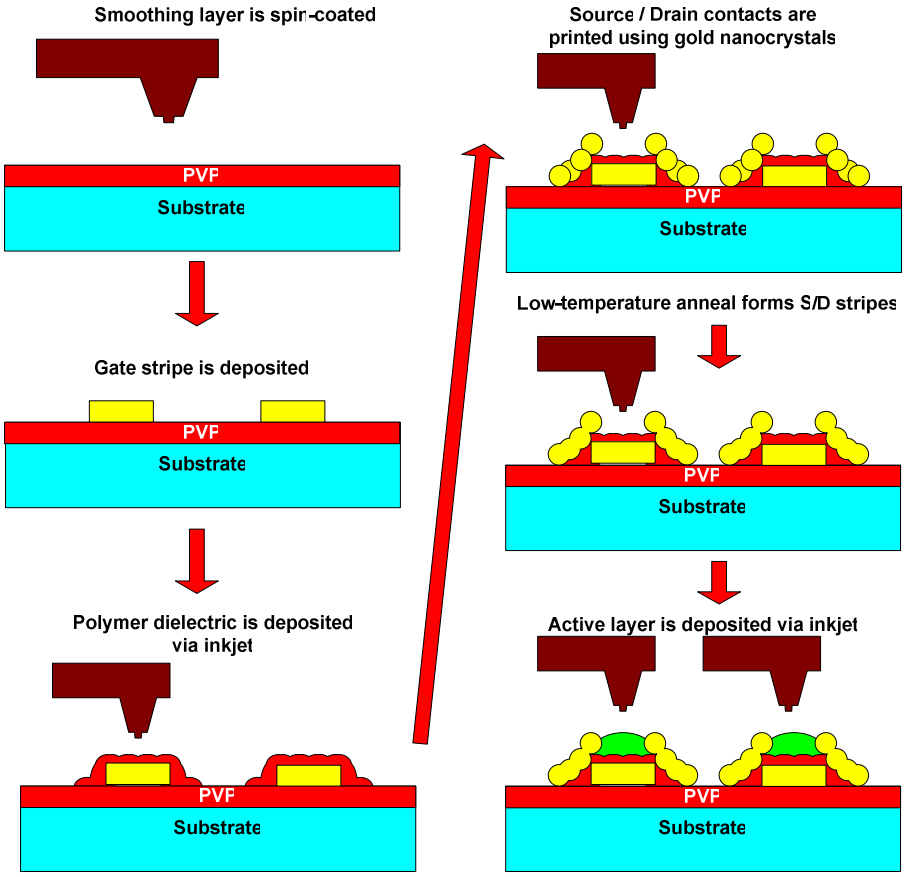


Figure 6.1: Process flow for formation of printed FETs.

A PVP gate dielectric was then printed and cross-linked through a two step anneal process. First, the solution is annealed for 1 min at 100°C to drive out solvent. Second, the dielectric is annealed at 200°C for 5 min to cross link the PVP. Various gate dielectric

thicknesses were investigated by changing the drop spacing and concentration of the ink (Figure 6.2). In conjunction with the smoothing layer (which prevents shorts due to surface roughness), it is possible to achieve gate dielectrics as thin as 20nm without shorting.

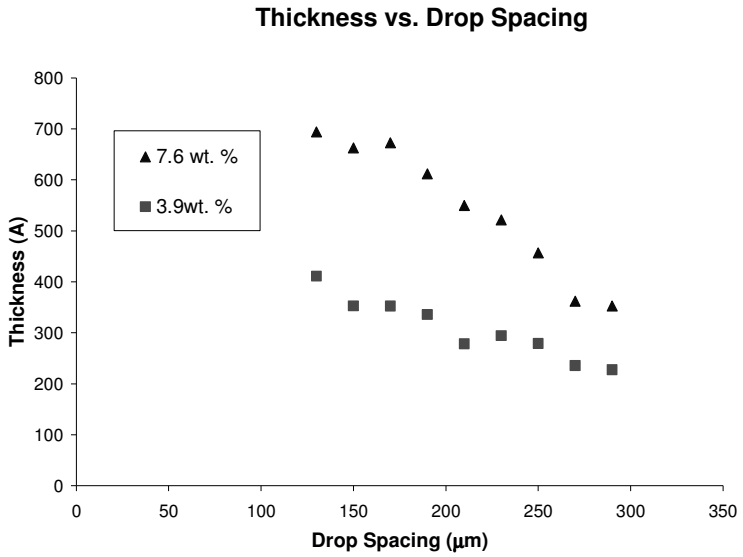


Figure 6.2: Effect of jetting parameters on thickness of inkjetted dielectric for two PVP solution concentrations.

Gold source/drain electrodes were next printed and annealed. The electrodes were printed onto a heated substrate (~165°C) to facilitate optimal shape definition. The registration achievable using inkjet, along with the scaled gate linewidth, allows the realization of structures with minimal overlap capacitance (Figure 6.3), necessary for high device switching speed. Using an advanced head, this process should be realizable using a fully-inkjetted flow. Finally, the semiconductor was printed and annealed under nitrogen for 3 min. The minimum reliably printable gap, corresponding to L, was 8 μm. At this dimension, overlap was approximately 6-10 μm.

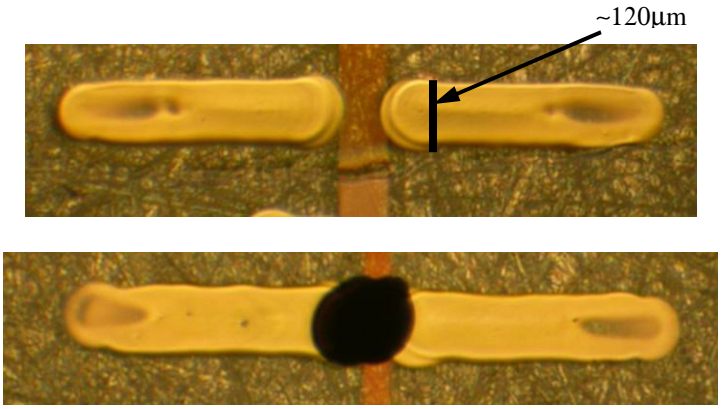


Figure 6.3: Optical micrographs of (top) low overlap gate stack structure and (bottom) final printed FET. The maximum electrode widths are ~120µm.

6.4.1 Gate Stack Structures

To enable optimization of the gate stack, gate stack capacitors were fabricated by the same process flow as above except for the printing of a continuous line (instead of two electrodes) over the simulated gate electrodes and the omission of the organic semiconductor. These capacitors were used to get effective capacitance measurements and this data was used in conjunction with area measurements to calculate the effective thickness of the gate dielectric and determine dielectric reliability. This data was used to compare the breakdown voltages and hence critical electric fields of devices made with and without a smoothing layer.

6.5 Jetting Techniques

The jetting techniques for the PVP gate dielectric, gold source and drain electrodes, and organic semiconductor were identical as in Chapter 5. The gate electrodes were deposited using evaporative techniques as described above.

6.6 Results and Discussion

6.6.1 Gate Stack Optimization

A comparison of breakdown voltage vs. thickness for capacitors made on bare PET plastic and PVP smoothed PEN plastic is shown in Figure 6.4. Before smoothing the PVP has an average electric field breakdown of 0.38-2.3MV/cm and after smoothing 7.3-10.5MV/cm. This dramatic improvement in breakdown strength demonstrates the importance of the smoothing layer. These fields are similar to what others report for PVP [11]. There is also a dramatic reduction in gate leakage which will be discussed in the next sections.

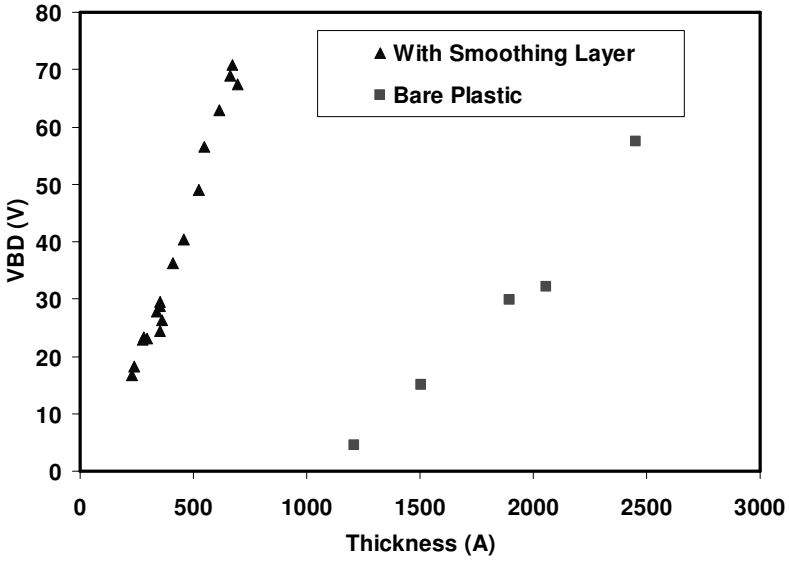


Figure 6.4: Breakdown voltages of capacitors made on smoothed plastic and bare plastic.

6.6.2 Scaled Device DC Performance

Transfer characteristic and output characteristic I-V curves are shown in Figures 6.5 - 6.8 for devices with W/L = 26µm/27µm, t_{ox} ~45nm, and W/L = 75µm/10µm, t_{ox}

~25nm. These devices were made with both the smoothed plastic and with a simulated inkjetted gate. Since the average breakdown for these gate stack structures are much higher, 7.3-10.5MV/cm, than the inkjetted gate devices this allowed the use of aggressive dielectric scaling to achieve operating voltages of 18V and 9V respectively. Unfortunately, the organic semiconductor was not as optimized as the previous devices and thus the highest mobility was >0.05cm^2/V-s. However, on-off ratios of 10^5 were obtained which was a result of less gate leakage due to the improved gate stack structure. It is also important to note that these devices also show no contact barrier as seen by the absence of concavity in the output characteristics.

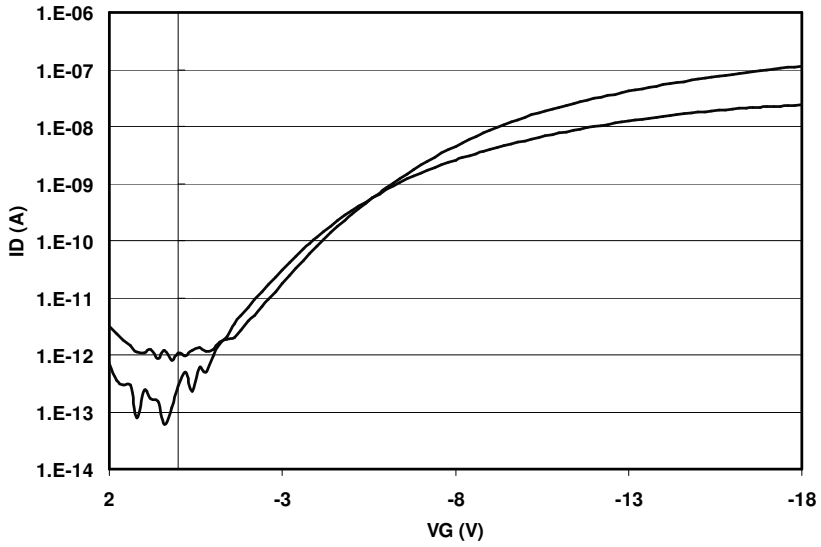


Figure 6.5: Transfer characteristics for a 26µm/27µm device with t_{ox} ~45nm. µ=0.051cm^2/V-s and Ion/I_{off} ~ 10^5.

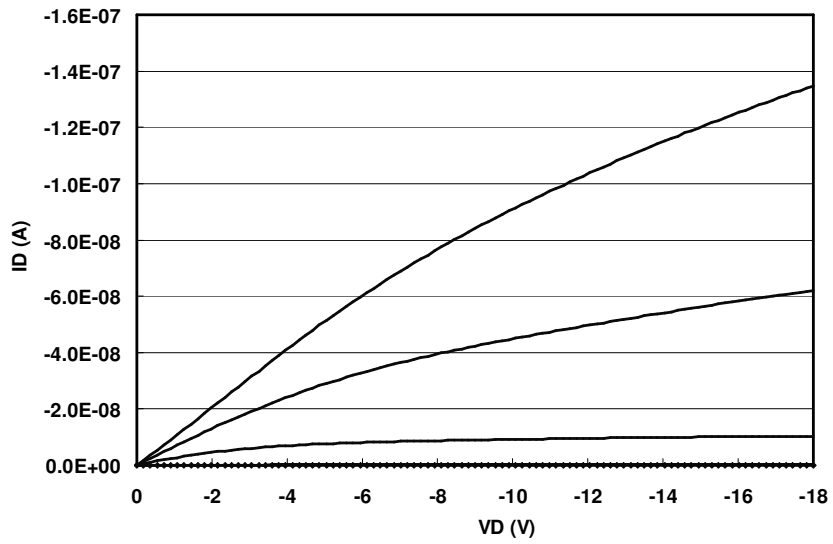


Figure 6.6: Output characteristics for a 26µm/27µm device with t_{ox} ~45nm (µ =0.051cm^2/V-s).

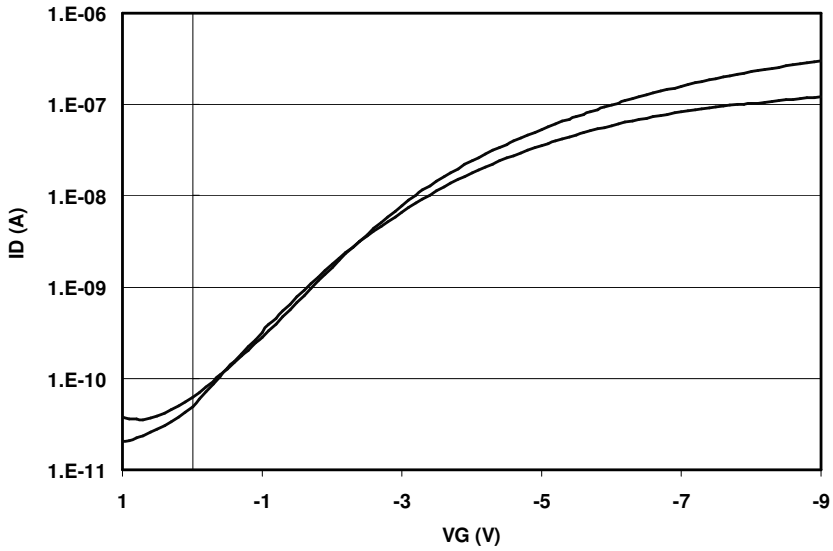


Figure 6.7: Transfer characteristics for a 75µm/10µm device with t_{ox} ~25nm. µ =0.043cm^2/V-s and $I_{on/off}$=3*10^3.

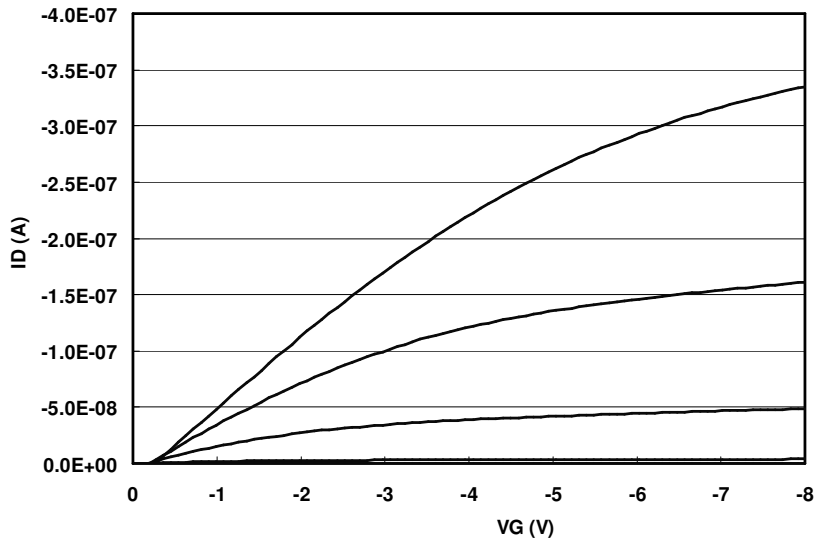


Figure 6.8: Output characteristics for a 75µm/10µm device with t_{ox} ~25nm (µ =0.043cm^2/V-s).

Despite the lower mobility, the overall electrostatics of these devices was dramatically improved. Organic semiconductors have a field dependant mobility [12-14], and, once a sufficient gate electric field has been achieved in a transistor, the mobility will saturate. At this point higher voltages will not increase transconductance. Using the aggressively scaled gate dielectrics, the transconductance saturated (as a result of the mobility) at 18 and 9 volts respectively (Figure 6.9). This corresponds to a vertical electric filed of 3-5 MV/cm which is 50% of the measured breakdown. This is promising for high device reliability. Also important to note is that these devices show excellent square law behavior as shown in the square root I_D curve in Figure 6.10.

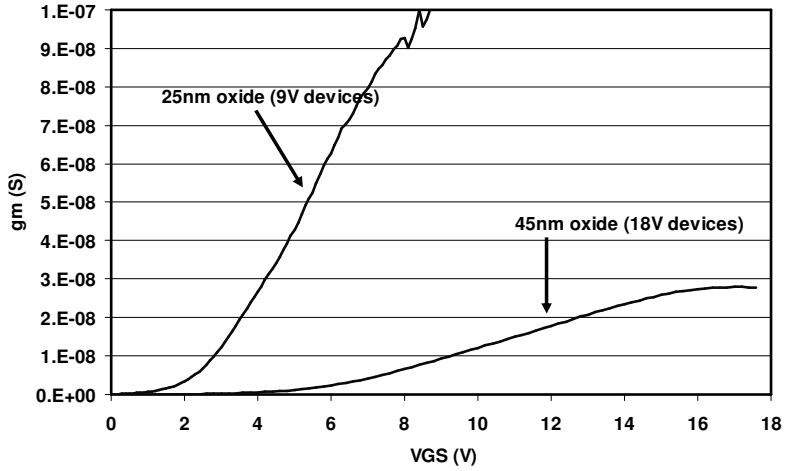


Figure 6.9: Transconductance as a function of gate voltage demonstrating that sufficient electric fields are achieved (max field is less than 50% of dielectric breakdown strength).

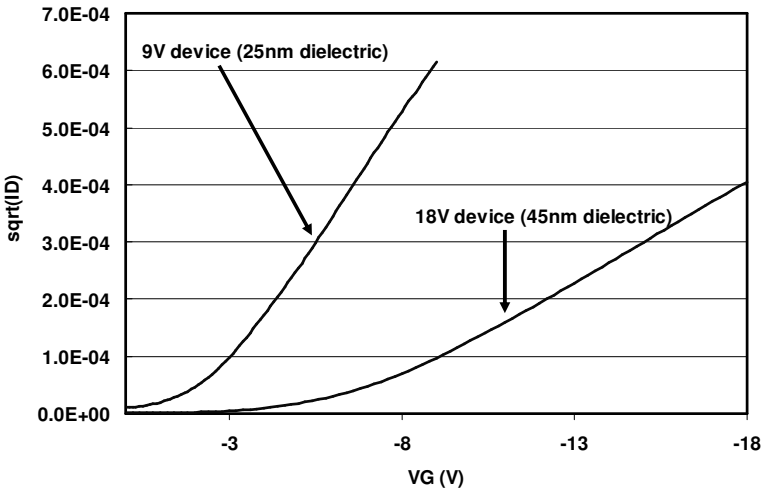


Figure 6.10: Square root drain current vs. gate voltage showing excellent square law behavior.

The scalability of channel length in these devices was also investigated. As the channel length shrinks (i.e. the gap between the electrodes) the width of these devices increases due to the round shape of the source and drain electrodes. As a result the transconductance was normalized with respect to width. After normalizing there is a roughly inverse linear relationship between transconductance and channel length (Figure 6.11). This inverse linear relationship demonstrates the scalability and lack of source drain resistance of these devices.

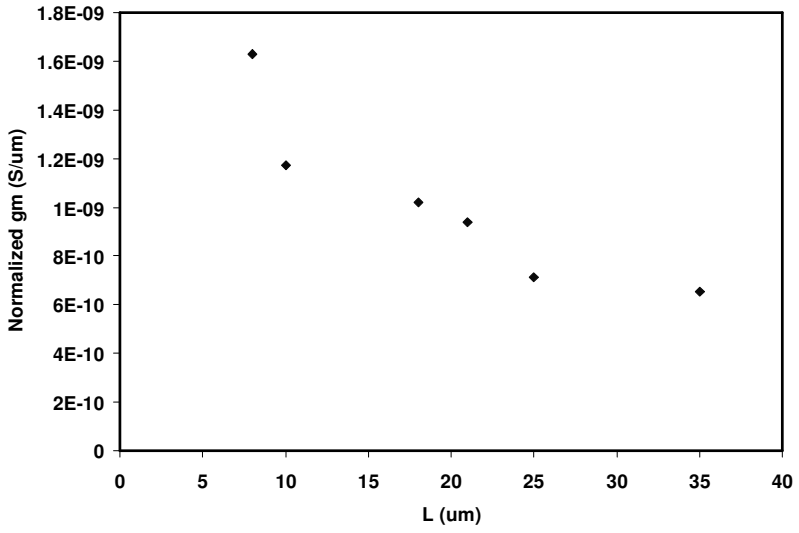


Figure 6.11: Normalized transconductance measured at 4.4MV/cm vs. channel length demonstrating the predicted inverse linear behavior.

6.7 Conclusions

This chapter optimizes the previously fabricated baseline transistors and demonstrates that high-performance transistors with low operating voltages can be fabricated using inkjet printing. A custom-built inkjet testbed and in-house synthesized inks were used to make these devices. Appropriate printing techniques were also

implemented to print the various inks, ensuring the formation of smooth layers and well defined patterns. The dielectric is printed in a manner such that the ink's surface tension promotes smoothness and the thickness is controlled by drop spacing and ink concentration. It is more important for the source and drain electrodes to have well-defined shapes to ensure the smallest possible channel length and hence high temperature printing is used. A wait state is required between drop depositions of the organic semiconductor to ensure that the drops cover the channel of the devices.

Because the test bed cannot print both smooth and well-defined gates, simulated gates were made through use of evaporative techniques. Using this process along with the substrate engineering the gate dielectric was aggressively scaled as thin as ~200Å while retaining a dielectric strength of 7.3 MV/cm and minimized overlap capacitance. This dielectric technology allowed the realization of transistors with operating voltages <10V. Optimized gate-source and gate-drain overlap was also realized, which is expected to result in improved AC performance. The frequency operation of these devices is discussed in-depth in the next chapter.

Clearly, in an all-printed-device a simulated gate will not work. In future work the orifice of the dispenser must be reduced so that 5-20 μm drops can be printed. But also a printing technique with the proper solvents, concentrations, and temperatures must be developed to print ultra smooth gates.

Chapter 7

Frequency Performance and Characterization

7.1 Introduction

RFID or radio frequency identification is the most changing technical application for low cost electronics, but despite this, over the past few years, RFID has received the majority of interest as an ultra-low-cost electronics application [1]. This is primarily because the advantages of implementing this technology in low cost form are numerous. RFID is a technology that seeks to eliminate passive barcodes with active circuitry, and by doing this, substantial improvement in workflow efficiency is expected [2, 3]. For example, inventory could be done by pulling the trigger on a reader and then walking within a short range of the product. Similarly, rather than having to wait in line for the cashier to scan each product, one could simply walk through a gate and have the products charged to his or her account.

State of the art RFID makes use of silicon-based RFID circuitry attached to a paper or plastic-based antenna. The cheapest state-of-the-art silicon RFID tags still cost > 10 cents per tag, which is too expensive for use in most item-level tagging applications. While costs are expected to decrease in the future, it isn't clear that tags substantially cheaper than 5-cents are feasible using conventional silicon-based RFID technologies, due to poor cost-scaling in the attachment and assembly costs. Therefore an ultra-low-cost manufacturing process as previously described could penetrate this cost-barrier imposed on conventional microelectronics technology.

Furthermore, the area of communication-circuits is largely set by the passive components and is therefore fairly fixed for a given operating frequency. Thus use of printed electronics should reduce tag costs substantially at a given operating frequency. This is particularly true for the lower RFID frequencies (135 kHz and 13.56 MHz) due to the large passive components required for these frequencies.

These frequencies are relevant to RFID for a number of reasons. Most importantly, at these frequencies there is allowable bandwidth for communication as mandated by the FCC. Higher frequencies, such as 900MHz, are not considered because organic semiconductors most likely cannot perform at these frequencies. 135 kHz and 13.56 MHz are also attractive as they work well in metal and liquid contaminated environments. Since they are relatively lower frequencies the electromagnetic energy is absorbed less into liquids and metals. Overall, 13.56 MHz is more favored over 135 kHz for two reasons. First, because it is a higher frequency, the passive components are smaller. In fact they have an ideal form factor (2 cm on side) at this frequency and that makes them similar sizes to current passive barcodes. Second, the FCC allows more energy to be broadcast at this frequency. This lengthens the reading distance. [2, 4]

It is important to note that these are carrier frequencies, and these are critical since power coupling will take place at these frequencies. Furthermore, FCC-mandates and likely communication protocols will likely necessitate clock frequencies in the hundreds of kilohertz range assuming modulation on a 13.56 carrier wave. Thus it is critical to fabricate low cost devices that can work up to several hundred kilohertz [5]. Because of this performance requirement, RFID is the most challenging low cost electronic application. If the performance of this application can be achieved, then most of the

applications cited earlier as well as more can be fabricated in a low cost fashion. The purposes of this chapter are to explain the proper frequency characterization of the devices, to present frequency data on devices made in this work, and then to propose optimization routines to achieve the performance requirements for RFID.

7.2 f_t: Transition Frequency

The most fundamental merits of frequency operation for a transistor are the transition frequency, f_t, and the maximum oscillation frequency, f_{max}. f_t is known as the frequency of unity current gain while f_{max} is known as the frequency of unity power gain. A schematic representation of how these values are found is in Figure 7.1. Note that the transistor shown is a NMOS device, but the devices fabricated in this work are PMOS devices. The device is biased in a common source configuration with no load at the drain. i_{in} is driven at frequency *f* and as *f* increases the current gain i_{out}/i_{in} falls. The frequency at which it reaches 1 is f_t. f_{max} is done in the same manner except that the power gain is now the measured parameter. [6, 7]

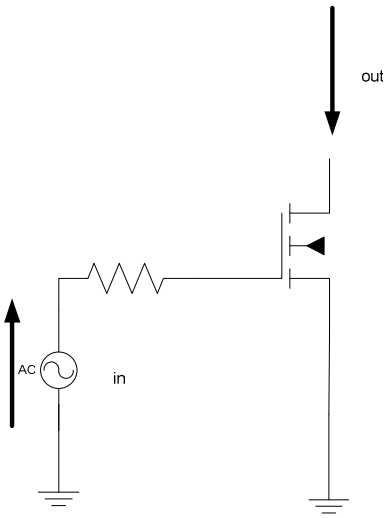


Figure 7.1: Common source circuit configuration used to measure f_t and f_{max}.

The importance of these parameters is that they represent the maximum possible frequency operation of the transistor. For example f_t is the maximum frequency a transistor can operate without load if a gain slightly greater than or equal to one is desired. Thus no gain can be extracted if frequencies higher than f_t are used. However, in logic circuits, little gain (at most 2) is required for proper operation. As result, logic circuits can operate rather close to f_t; clock frequencies can sometimes operate close to half of f_t. It is important to note that introduction of a load for voltage gain will result in degraded frequency performance because the output pole will lower as the gain is increased due to the higher resistance.

f_t can be theoretically calculated using the small signal model shown in Figure 7.2 and the equations below.

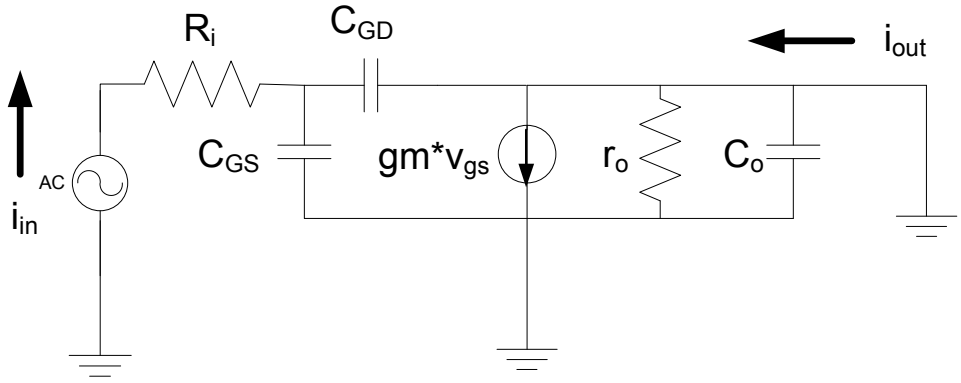


Figure 7.2: Small signal model of a common source circuit.

$$v_g(\omega) = \frac{i_{in}}{j\omega(C_{GS}+C_{GD})}; i_o(\omega) = gm * v_g(\omega) \Rightarrow \frac{i_o}{i_{in}}(\omega) = \frac{gm}{j\omega(C_{GS}+C_{GD})} \quad \textbf{Eqn 7.1}$$

$$1 = \frac{i_o}{i_{in}}(\omega) = \frac{gm}{j\omega(C_{GS}+C_{GD})} \Rightarrow \omega_t = \frac{gm}{(C_{GS}+C_{GD})} \Rightarrow f_t = \frac{gm}{2\pi(C_{GS}+C_{GD})} \approx \frac{gm}{2\pi(C_{in})} \quad \textbf{Eqn 7.2}$$

f_{max} represents the maximum frequency at which an oscillator made from these transistors can operate. Its importance derives from the fact that if these low cost transistors are used to make a clock oscillator, then the ability to drive other transistors will be necessary. This is obviously critical if the clock is generated on chip. However, an on chip clock is not critical since the carrier wave, 13.56 MHz, could be divided down using a frequency divider. Thus the transistors could be driven at frequencies higher than f_t as long as gain is not required.

f_{max} is related to f_t through the following relation:

$$f_{\max} = \sqrt{\frac{f_t}{8\pi * C_{GD} * R_i}} \qquad \textbf{Eqn 7.3}$$

Important to note is the dependence on R_i or the input resistance. Because R_i falls in the denominator of the radical, f_{max} decreases as R_i increases. This is another reason why high performance, low resistance interconnects are required.

7.3 Measurement Technique

Typically, in a normal silicon device, a network analyzer extracts f_t and f_{max} through measurement of the scattering parameters. Electromagnetic scattering can be significant at average CPU clock frequencies, hundreds of MHz to several GHz, and, as a result, the measurement of the scattering parameters is critical [7]. However at the frequencies of interest to RFID, hundreds of kHz, network analyzers are very difficult to find that operate at such low frequencies. Most importantly, though, is that scattering is not substantial at these frequencies and thus S parameters are not necessary to measure.

In an analogous fashion to the network analyzer, the admittance parameters of a given circuit can be measured [8]. The circuit elements can then be deconvoluted and the admittance parameters of the single transistor can be converted to scattering parameters. These scattering parameters then give both f_t and f_{max}. This method is quite tedious and a much simpler method can be used that directly measures f_t. The only drawback to this simpler method is that it does not give a direct f_{max} measurement. This is not a problem, however, since f_{max} can be calculated from f_t.

This simpler method works as follows. First, a measurement is taken to find the input current, $i_{in}(f)$, of the transistor as a function of frequency. Second, a measurement is done to find the output current, $i_o(f)$, as a function of frequency. Current gain is found by dividing $i_o(f)/i_{in}(f)$. The point on this graph at which $i_o(f)/i_{in}(f) = 1$ is f_t.

Measuring $i_{in}(f)$ is a rather straightforward measurement and can be accomplished by measuring the input impedance using a HP 4184A LCR meter. This is done by biasing the gate in an identical fashion to how it is biased when measuring $i_o(f)$. Then, the total input impedance (the total input capacitance) of both C_{gs} and C_{gd} are measured simultaneously. This will give a slight overestimate of C_{in} since C_{gs} will be slightly lower when the drain is biased (due to the "pinch off" of the accumulation layer); however, for the purposes of approximating f_t in this work, this is accurate enough. Using C_{in}, $i_{in}(f)$ is found through the following relation:

$$i_{in}(f) = v_{in} * 2\pi f * C_{in} \qquad \textbf{Eqn 7.4}$$

Measuring $i_o(f)$ is accomplished by biasing the transistor in a common source configuration as shown in Figure 7.3. It is critical that that the output resistor R_o be much smaller than the output resistance of the transistor, r_o. In particular, the voltage gain of the

circuit needs to be much less than one so that the parasitic output poles will be much higher in frequency than the f_t of the transistor. This is fine since R_o is there simply to measure the output current, i_o. The DC bias and small signal voltage, V_{in}, are applied using a HP 33120A function generator. The drain bias is applied using a 15V power supply. The output node voltage, V_o, is measured using a Burr-Brown OPA602BP operational amplifier in unity feedback. This buffer circuit is critical since it has 10^{13} Ω of input impedance and thus will not load the circuit in any manner. The output voltage is read from a digital oscilloscope and the output current is calculated using the relation:

$$i_o = \frac{V_{out,peak-to-peak}}{R_o} \qquad \textbf{Eqn 7.5}$$

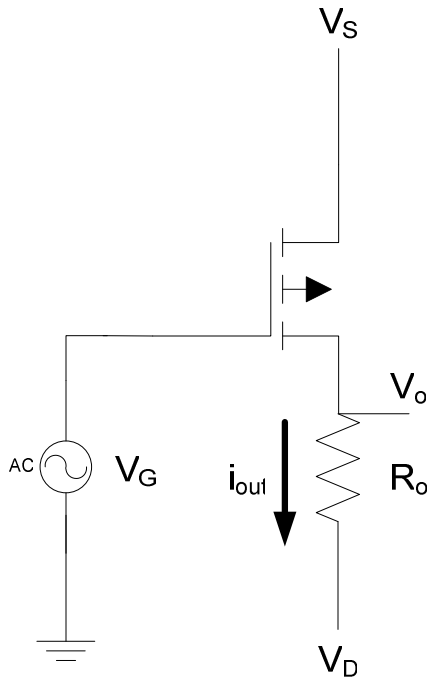


Figure 7.3: Common source measurement circuit used to measure f_t.

7.4 Results and Discussion

A plot of the transconductance versus gate bias for the transistor chosen for the f_t measurement is shown in Figure 7.4. For this particular transistor, the transconductance reaches its peak value at V_{GS}= -13V. It is important to bias the device at this peak value for two reasons. First, the maximum transconductance ensures the maximum f_t is obtained for this device as a result of Equation 7.2. Second, at this region of bias the transconductance is relatively constant with bias. Thus when applying a small signal, for example ±2V, the signal will not undergo any gain expansion or compression. Or, in other words, it will have minimal distortion. For these reasons, the device was biased with V_{GS}= -13V and V_{DS} = -15V for the $i_o(f)$ measurement.

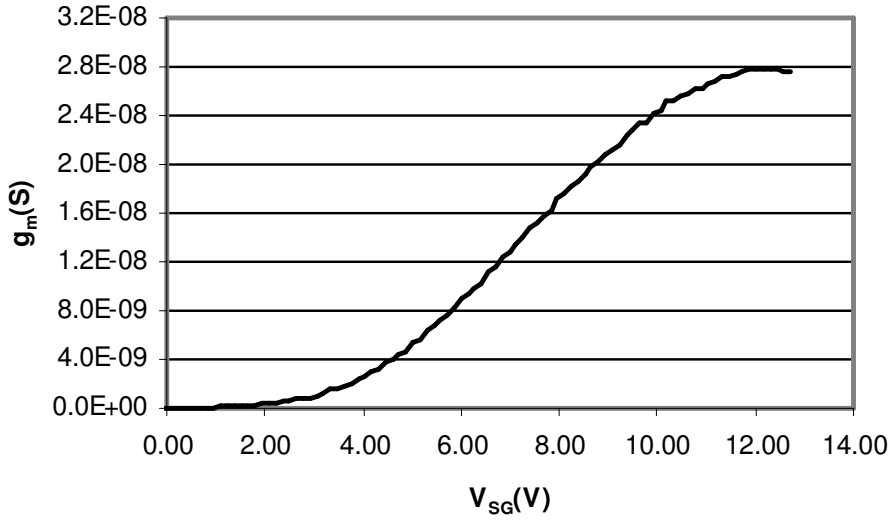


Figure 7.4: Transconductance as a function of gate bias for the device used to measure f_t. $t_{dielectric}$= 507Å, W/L=100μm/11μm, and μ = 0.015cm^2/V-s.

Using a R_o of 500kΩ and a 4V peak-to-peak input, the low frequency peak-to-peak output voltage, V_o, was 60 mV. Assuming $R_o << r_o$, the theoretical gain, A, of this circuit is:

$$A = g_m * R_o \qquad \textbf{Eqn 7.6}$$

Thus for this device at a bias of V_{GS}=-13V, the gain is 0.014 and with a 4V peak-to-peak input, the output voltage is predicted as 56mV. Thus the actual value is in excellent agreement with the predicted value, and, more importantly, this demonstrates that the DC parameters are accurate in predicting the AC performance.

C_{in} was measured as 10 pF and, using Equation 7.4, the extrapolated $i_{in}(f)$ is shown in Figure 7.5. Also shown in Figure 7.5 is $i_o(f)$ that remains relatively constant past f_t as predicted. Notice that $i_{in}(f)$ increases linearly with frequency as a result of the shunting of current through C_{in}. f_t is the frequency at which $i_{in}(f) = i_o(f)$ (Figure 7.5), or, as shown in Figure 7.6 it is the frequency at which $i_o(f)/i_{in}(f)=1$. Thus the f_t of this device is 477Hz.

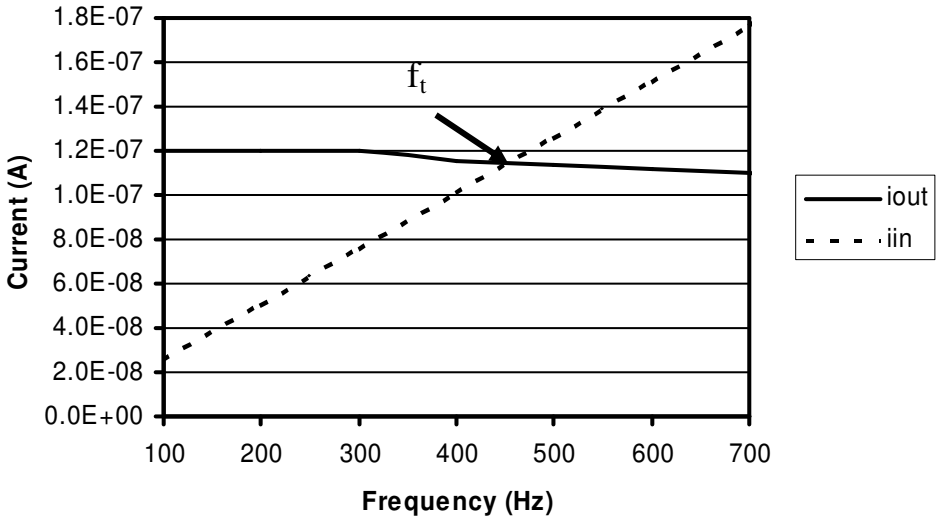


Figure 7.5: i_{out} and i_{in} as a function of frequency.

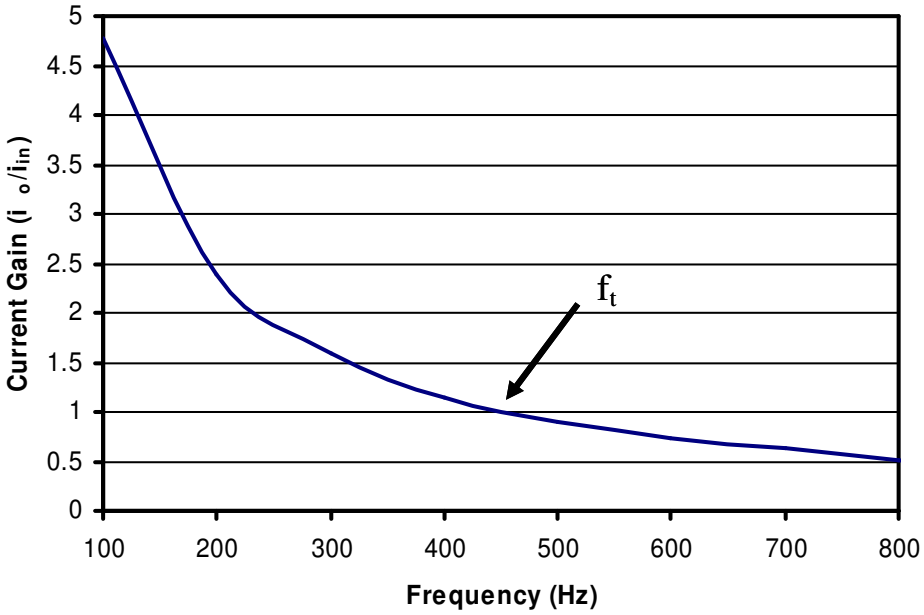


Figure 7.6: Current gain (i_o/i_{in}) as a function of frequency.

7.4.1 Improving f_t

Despite this rather low frequency performance, more important is the fact that this structure gives a manufacturing route to develop transistors with f_t>200 kHz required for RFID. By expanding the relationship of f_t to the transconductance and input capacitance, the dependences of f_t on device structure can be seen more clearly:

$$f_t \approx \frac{gm}{2\pi(C_{in})} = \frac{\mu C_{dielectric}\frac{W_{channel}}{L_{channel}}V_{DSAT}}{2\pi C_{dielectric}W_{S/D}L_{GATE}} \qquad \textbf{Eqn 7.7}$$

Note that $W_{channel}$ /$L_{channel}$ are the dimensions of the physical device channel where conduction occurs. This is in contrast to $W_{S/D}$*L_{GATE}, which is the width of the electrodes overlapping the gate and the length of the gate itself. This distinction is important

because it quantifies the amount of electrode overlap in the device which directly couples to the amount of input capacitance, C_{in}.

7.4.1.1 Mobility Effects

With the current mobility of these devices, 0.015cm^2/V-s, the f_t is 477Hz. Since f_t is linearly proportional to the mobility (Equation 7.7), by increasing the mobility to 1 cm^2/V-s the f_t increases to 32kHz. This type of performance increase seems large, but there have already been demonstrations of organic semiconductors with this performance [9, 10].

7.4.1.2 Electrode Overlap Capacitance

Further improvements can be achieved by improving device structure through minimization of overlap capacitance. It would be ideal if transistors could be made without any electrode overlap capacitance. In such a case the input capacitance is simply the dimensions of the conduction channel, $C_{dielectric}*W_{channel}*L_{channel}$. This is the minimum possible achievable input capacitance for any transistor. However, because of manufacturing limits and tolerances, there is a minimum achievable electrode overlap that is dictated by the manufacturing process. For printing, this minimum overlap is achieved through better alignment and better drop placement control. Both of these are determined by the limits of the printing system. Recent developments in the past couple of years show that printers are able to achieve both thin line widths <20μm and better placement, sub 5μm [11, 12].

For these particular devices the overlap is excessive because of the rounded shape of the electrodes (Figure 7.7). As a result, in order to maximize the transconductance, the whole rounded end needed to overlap the gate. This maximizes the transconductance because the width is maximized. In order to fabricate a faster device, the electrodes could be printed vertically and made longer. Such a case would minimize the gate overlap as shown in Figure 7.8.

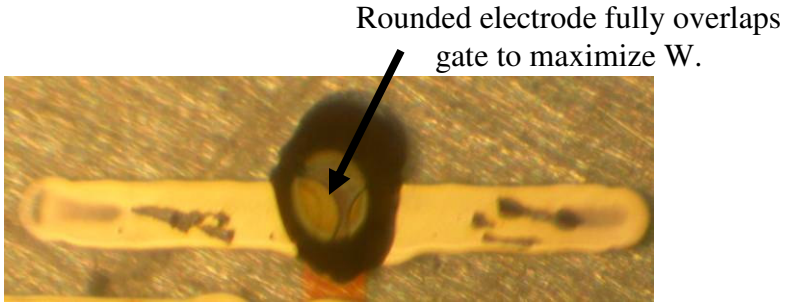


Figure 7.7: Transistor used to measure f_t showing the electrode overlap.

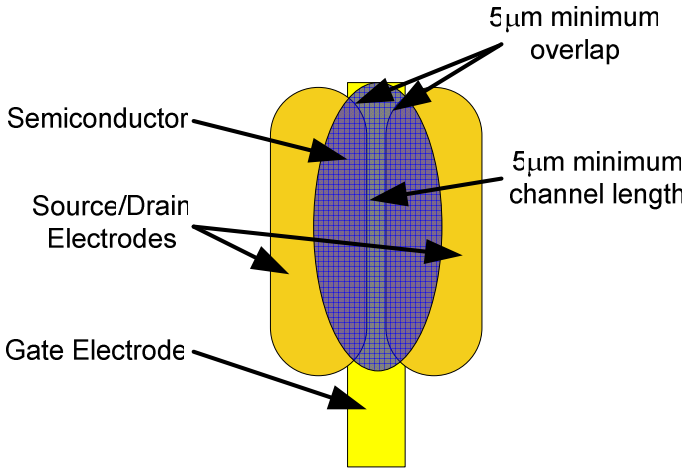


Figure 7.8: Example of an optimized device structure with minimum overlap and channel length.

With these improvements and better printing technologies, devices with 5 μm overlap and 5μm channel lengths are possible. Thus, as an example, new device dimensions could be $W_{channel}/L_{channel}$ = 200μm/5μm and $W_{S/D}*L_{GATE}$ = 200μm* 15μm (Figure 7.8). Normalizing the transconductance of the device measured here and then factoring these new dimensions would give a new transconductance value of $1.32*10^{-7}$ S. The new input capacitance, C_{in}, value is 1.89pF. Thus, with overlap minimization through structure optimization, the new f_t is 11.1 kHz. Combining this with the mobility improvements it is possible to achieve performance as high as 741 kHz. Note that this is still a conservative estimate since the normalized transconductance was based on the rounded electrodes and the minimum distance between them. The average channel length was actually larger then this minimum distance and thus there would be an improvement as a result of eliminating this effect as well. Most important is that these improvements now put the performance well into the realm of what is required for RFID operation.

7.5 Conclusions

RFID is a very desirable technology due to it numerous advantages in workflow efficiency related to checkout and inventory. However, RFID is also the most challenging lost cost electronics application due to the necessity for relative high speed >200 kHz operation. However, if RFID can be manufactured in a low cost fashion, a whole host of other lost cost technologies are also available. RFID will likely require a carrier frequency of 13.56 MHz and a modulated sideband of ~200 kHz. It is not critical that that the transistors be able to function at the carrier frequency, which is $>>f_t$, because a frequency divider can be used where gain is not required. It is still necessary for the

transistors to function at ~200 kHz which is the sideband frequency, and, as a result, the required f_t is >200 kHz.

A simple measurement was developed to measure the f_t of the transistors fabricated in the previous chapter. The f_t of the transistor measured for this work is 477 Hz. While this is far from the performance necessary for RFID, further improvements in both semiconductor mobility and minimizing overlap capacitance will provide the necessary performance, >500kHz. Thus this work provides a manufacturing route to achieve the performance required for RFID and, indeed, RFID is becoming tantalizingly near.

Chapter 8

Gravure Printing and Future Work

The previous chapters discussed the processing to fabricate low cost electronic components using inkjet printing. Inkjet printing served as an excellent research tool because of its high degree of pattern flexibility and ability to rapidly prototype devices. However, in going forward, and developing this technology for manufacturing there are several issues that need to be addressed. Some of these issues include finding higher throughput printing technologies (i.e. gravure printing), developing better low cost semiconductors, developing better dielectrics, developing better materials integration to improve device reliability, and developing circuits. These are all issues that need to be addressed in future work. This chapter will discuss all of these issues and describe initial gravure printing screening experiments.

8.1 Introduction to Gravure Printing

While the majority of work in this thesis has used inkjet printing to fabricate low cost electronic components, gravure printing is another form of printing that may be used to make low cost electronics [1]. Inkjet is an excellent research tool due to its extreme flexibility but gravure offers many advantages over inkjet; especially in manufacturing. Specifically, gravure printing generally has a much higher throughput than inkjet, and, furthermore, the mechanics of the printing process itself tend to be simpler than inkjet.

Gravure printing can be compared to a normal ink stamp; ink is deposited onto a pattern and then pressed onto the substrate. The main difference from a stamp is that the

patterns on a gravure roller are etched into the drum and the drum is rolled over the substrate. As a result the ink is held in the indentations rather then on the extrusions and, because it rolls over the substrate, it can operate in a continuous mode where the ink is continuously deposited onto a rolling drum. This makes it well suited to roll-to-roll fabrication and hence low cost fabrication in general. (Figure 8.1). [2]

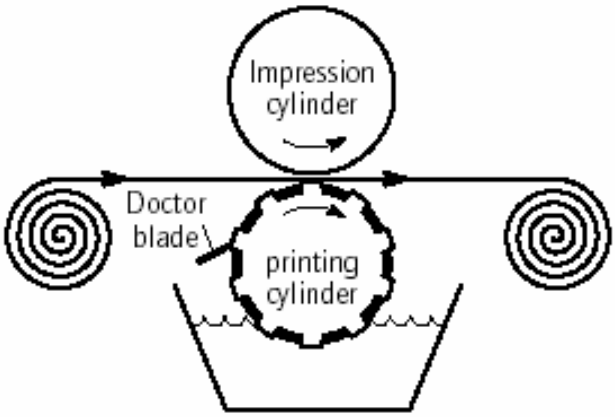


Figure 8.1: Roll-to-roll gravure printer.

The drums are usually made out of metal and the patterns must be etched into them using a laser or photolithography. Because of this, gravure printing is more expensive to develop masks and less flexible. However, there are huge advantages in terms of throughput and quality of pattern transfer. Thus gravure printing is reserved mainly for high end glossy magazines, but it also has a unique application to low cost electronics manufacturing. [2]

Because the ink is held in precisely made indentations in the drum and the drums do not distort, the ink deposition is well controlled and accurate. However, the amount of ink deposited is a complex function of the differential wetting of the ink between the drum and the substrate. Some of the parameters that govern this include the surface

tension of the ink, any particulates or binders in the ink, the surface energy of the substrate (including roughness), and the surface energy of the drum (including the shape and roughness of the well). Because of this complexity, few if any theoretical predictions are ever carried out to predict the behavior. Instead, most information is gathered empirically. [3]

Furthermore, in comparison to inkjet, much of the technology used to deposit the ink is transferred from the inkjet processing techniques into simply drum and ink design (i.e. the processing is simpler). Gravure drums must be properly engineered with shapes in the sub 10 μm ranges and also the contour of the wells must be properly shaped to facilitate proper wetting. Gravure inks are also much higher viscosity and as a result inkjet inks cannot simply be transferred to gravure. The ink formulation itself must be altered or a binder must be added to increase viscosity. Overall, the inks tend to be more complex than inkjet inks.

In assessing the abilities of gravure printing for low-cost electronics fabrication it is necessary to perform screening experiments to identify problems and identify suitable materials. These initial experiments were carried out to identify suitable inks and to determine the minimum shapes that can be fabricated with gravure printing. The first major goal was to develop an ink and suitable process to gravure print highly conductive nanoparticle based inks that were previously used in the inkjet experiments.

8.2 Experimental Setup

Experiments were carried out using with 35 different ink formulations summarized in Table 8.1. Each ink was printed onto a PET substrate using an IGT

gravure printer. The printed patterns were 4 lines with widths of 100, 250, 500, and 750 μm with lengths of about 10 cm. For each ink, 2 speeds, 0.4 m/s and 0.8 m/s, and 2 pressures, 250 N and 750 N, were used for a total of 4 samples. Films were annealed in an oven at 200° C for 30 minutes.

Number	Label	Solvent 1	Amt. sol. 1 (uL)	Solvent 2	Amt. sol. 2 (mL)	Wt. nxtal (mg)	Wt. % nxtal	Other (mg)	Group
1	I	hexanol	1000			100	10		A
2	II	apha-terpineol	250	toluene	750	100	10		B
3	III	apha-terpineol	500	toluene	500	100	10		B
4	IV	apha-terpineol	750	toluene	250	100	10		B
5	V	apha-terpineol	2000			100	5		B
6	VI	apha-terpineol	2000			200	10		B
7	VII	toluene	2000			400	20		B
8	VIII	tert butanol	1000			100	10		A
9	IX	butyl benzene	1000			100	10		B
10	X	hexane thiol	500			130	26		B
11	XI	chloroform	125	anisole	375	125	20		B
12	XII	chloroform	250	anisole	250	125	20		B
13	XIII	chloroform	375	anisole	125	125	20		B
14	XIV	chloroform	500			125	20		B
15	XV	anisole	500			125	20		B
16	XVI	polyethylene glycol	500			125	20		A
17	XVII	toluene	300			6	20 (without Ag)	300 Ag 2.5um	B/A
18	XXIII	toluene	1000			200	20 (without Ag)	100 Ag ~300nm	B/A
19	XXIV	toluene	500			100	20	100 (nm)	B
20	XXV	chloroform	500			100	20	50 (nm)	B
21	XXVI	chloroform	500			100	20	100 (nm)	B
22	XXVII	chloroform	500			100	20	250 (um)	B
23	XXVIII	chloroform	500			100	20	100 (um)	B
24	XXIX	chloroform	500			100	20	50 (um)	B
25	Au 30	chloroform	750			150	20	0.01g/ml binder	B
26	Au 31	anisole	750			150	20	0.01g/ml binder	B
27	Au 32	chloroform	1000			200	20	0.02g/ml binder	B
28	Au 33	anisole	1000			200	20	0.02g/ml binder	B
29	Au 34	chloroform	250	anisole	750	200	20	0.02g/ml binder	B
30	Au 35	chloroform	500	anisole	500	200	20	0.02g/ml binder	B
31	Au 36	chloroform	750	anisole	250	200	20	0.02g/ml binder	B
32	Au 37	toluene	640			128	20	0.01g/ml binder	B
33	Au 38	toluene	250	hexanol	750	200	20	0.02g/ml binder	B
34	Au 39	toluene	500	hexanol	500	200	20	0.02g/ml binder	B
35	Au 40	toluene	750	hexanol	250	200	20	0.02g/ml binder	B

Table 8.1: Summary of conductor ink formulation.

8.3 Results and Discussion

8.3.1 Incomplete Dissolution

As shown in Table 8.1 the inks are divided into two groups, A and B. Group A inks are inks where the nanoparticles do not truly dissolve. In these types of inks the nanoparticles are somewhat soluble, disperse well, and individual particles cannot be

seen, but the particles do not dissolve down to individual nanoparticles and form a true solution. The group B solutions are solutions where the nanoparticles do truly dissolve down to individual particles. The significance of this distinction is that films made with group A solutions do not conduct. This is because the particles do not form a continuous film for conduction, but rather stay in agglomerated particles. This can be seen in the post annealed film shown in Figure 8.2 versus the continuous film in Figure 8.3.

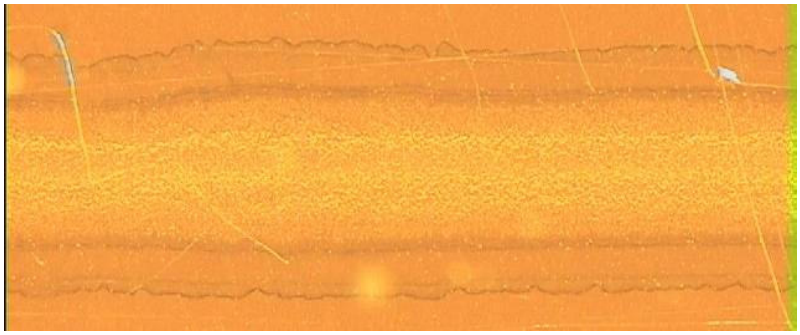


Figure 8.2: Ink I, group A ink, forms a discontinuous film.

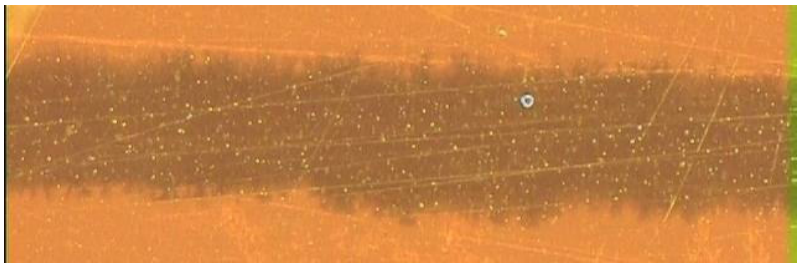


Figure 8.3: Ink IV, group B ink, forms a continuous film, but the edges are deformed and there is a high degree of spreading.

8.3.2 Spreading and Distortion

Another major problem encountered was a high degree of spreading and wetting of the inks. The amount of spreading is summarized in Table 8.2. This problem came from two fundamental problems. First, although solvents such as toluene, thiol, and

butylbenzene, evaporate quickly, they do not evaporate quickly enough to prevent the spreading that comes from the high degree of preferential wetting the solvents have on the PET substrates. Second, in the case of α-terpineol (VI), it was found that this solvent initially has good shape fidelity with low spreading but since α-terpineol has such a high boiling point, it has adequate time to distort before drying as shown in Figure 8.4. Because of this distortion lines smaller than 500 μm on the drum were found to be discontinuous, and thus, data for a wider line, without discontinuities, was quoted in Table 8.2.

Ink	Line width on drum (um)	Average printed width (um)	Ratio
I	100	1470	14.7
II	100	734	7.34
III	100	1280	12.8
IV	100	818	8.18
VI	500	925	1.85
VII	100	1530	15.3

Table 8.2: Summary of spreading for various inks.

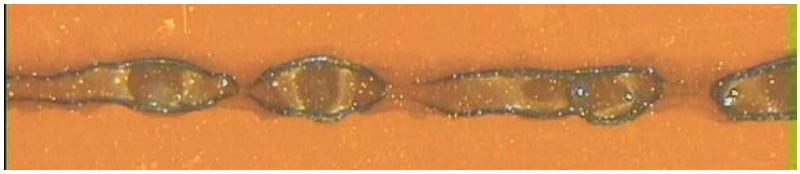


Figure 8.4: Gravure printed α-terpineol ink showing the distortion that occurs before drying.

8.3.3 Directional Printing

One printing method used extremely fast drying solvents such as chloroform. As shown in Figure 8.5, an ink made from a nanoparticle solution using chloroform and anisole as the solvents form relatively well defined lines. Furthermore, the spreading is

minimal since the chloroform solvent dries so fast. However, as shown in Figure 8.6, the lines do not print well in multidirectional shapes. These distorted shapes are a result of the low relative viscosity of the solvent. As the roller moves, the ink tends to "splash" out and as a result the ink moves towards the end of the shape (with respect to the direction of rolling).

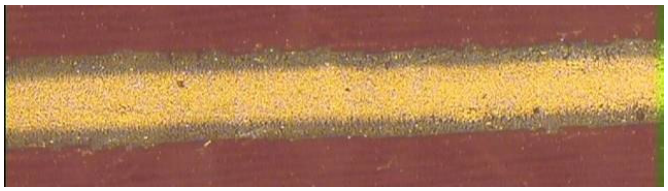


Figure 8.5: Gravure printed nanoparticle ink with chloroform/anisole solvent showing the well-defined line.

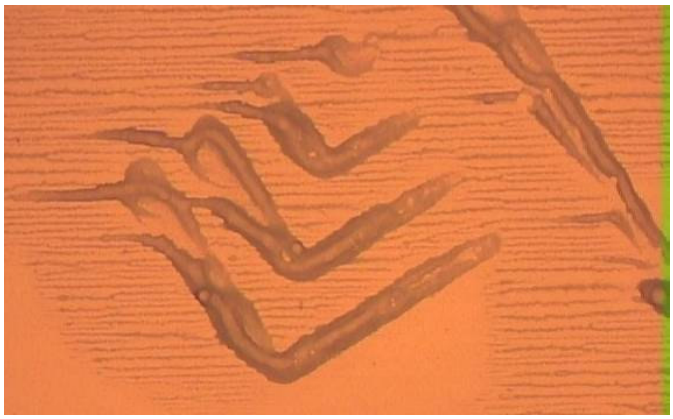


Figure 8.6: Gravure printed nanoparticle ink with chloroform/anisole solvent showing the poor multi-directional printing.

8.3.4 Solvent Mixture and Binders

When mixing two solvents together it was quite common to see a leaching and branching effect. What occurs is that the lower viscosity, also the faster evaporating,

solvent first leaches out of the solution. Then the more viscous slower evaporating solvent slowly branches out were the other solvent wet the substrate. As a result the line edge roughness is poor due to the fingers. This is shown for a toluene and α-terpineol solution, and a chloroform and anisole solution in Figure 8.7.

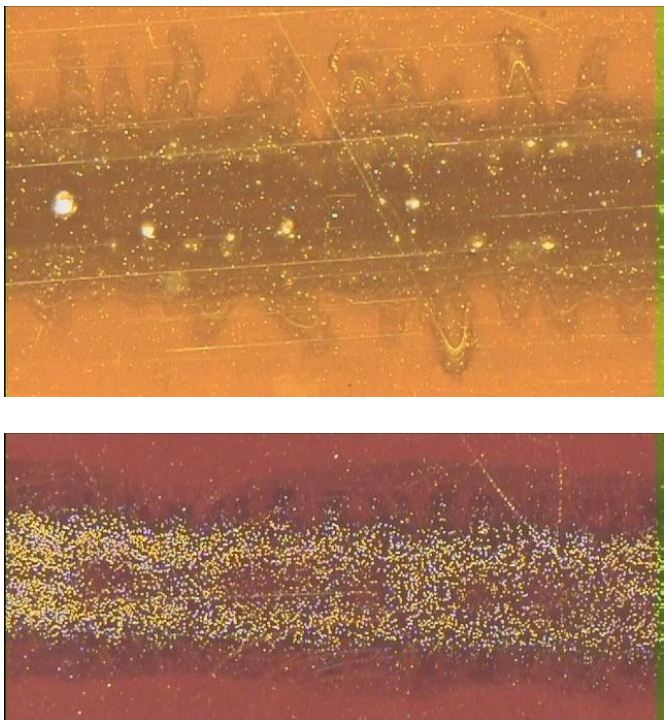


Figure 8.7: Leaching and branching effect for toluene and α-terpineol (top), and chloroform and anisole (bottom).

Most of the previous problems were a result of the fact that these nanoparticle inks are not viscous enough to be used with gravure printing. As result, the viscosity of the inks was increased using chemical binder, PMMA. This did have a positive effect on the inks as the shape fidelity was better (Figure 8.8). However, an adverse side effect of increased surface tension was also observed. This caused the lines to "ball up" and form discontinuous structures.

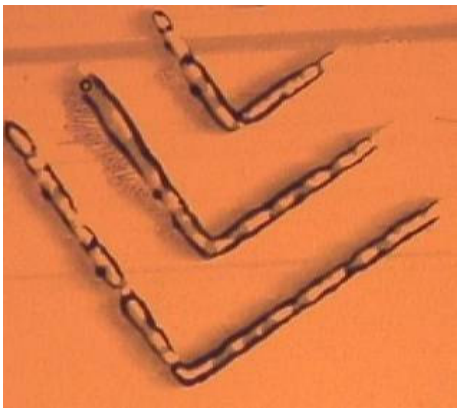


Figure 8.8: Gravure printed ink consisting of nanoparticle gold, chloroform, and PMMA binder. The binder improved line quality but caused discontinuities.

Nanoparticle solutions with silver powder mixtures also showed improved line fidelity, Figure 8.9. The spreading in these inks is greatly reduced because the solvent preferentially wets the silver particles because of the high surface area/energy. After annealing these inks, a matrix is formed where the gold nanoparticles act as a binder to the silver particles. The problem with these mixtures is that the lines are too rough to be useful. The roughness was several microns due to the micron sized silver particles.

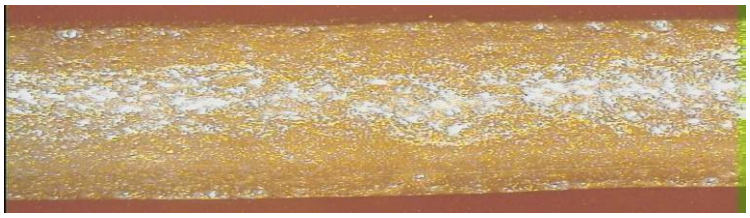


Figure 8.9: Gravure printed nanoparticle ink with silver powder. This ink shows improved line fidelity but is too rough to be useful in interconnects.

8.4 Future Work

8.4.1 Gravure Printing

So far an adequate gold nanoparticle ink has yet to be realized for gravure printing. The biggest problem is that all of the basic nanoparticle inks have a viscosity that is too low. This is the cause all of the undesirable traits as seen thus far: spreading, splashing, branching, etc. These preliminary experiments clearly show that these nanoparticle based inks used in the inkjet process need to be fundamentally modified for use in gravure printing. This may include adding OH capping groups to the thiol ends that increase particle interaction and hence increase viscosity. Another idea may be to polymerize the nanoparticles which would also increase the viscosity.

Another method that may work is to modify existing gravure inks. As discussed in Chapter 3 there are a wide variety of interconnect inks available and, furthermore, many of the particle based inks are tailored for gravure printing. Their performance may be enhanced by addition of gold nanoparticles. Instead of having the loosely bonded particles held together by a polymer binder, they would be held together by a metallic bond. Thus, the overall resistance may be lowered. There is still concern that the interconnects will be too rough since there are still micron sized particles. This would have a detrimental affect on AC performance and would not be useable where smoothness is critical such gate stacks and capacitors.

Another area that remains largely unexplored in gravure printing is minimum shape limits. Ideally it would be beneficial to print sub 5 μm shapes along with sub 5 μm spacing. This would allow the required performance for the transistors and ensure adequate density to fit the necessary amount of transistors onto the form factor of current barcodes, 2cm. It is unknown how these small dimensions would affect printing. In

particular the wetting, spreading, and capillary forces in the drums would be significantly different.

The last major issue, mostly unexplored, with respect to gravure printing is alignment and the limits thereof. Alignment is significantly more complicated in gravure printing than it is in inkjet printing. This is for several reasons. First, the drum is hard to align to a prepatterned substrate because the pattern is on the bottom of the drum and thus in order to see the drum align to the substrate either transparency is required or it must be done indirectly with alignment marks. The difficultly in using alignment marks is that they are subject to distortion including thermal distortion of the drum and support structure. Also the bearings supporting the drum must be extremely precise to accommodate the alignment. Complicating this is the fact that distortion of plastic substrate is a well known problem in flexible electronics. Both shrinkage from prolonged heat exposure along with thermal expansion make alignment difficult over large areas.

8.4.2 Hybrid Printing

Because of the trade offs associated with both inkjet and gravure printing it is not known which is best or will produce both the highest throughput and maximum yield. In fact, the best solution will probably be some form of hybrid printing manufacturing process. For instance the large area components, capacitors, inductors, and interconnects, benefit most from gravure printing where alignment is not critical. Within 50 μm accuracy they can be printed extremely fast with one roll of a gravure drum. At the same time, however, it will be extremely difficult to achieve sub 5 μm alignments over the whole circuit especially considering the shrinkage of the plastic substrate. This is

especially crucial for transistor alignment and gate definition to ensure proper performance. Inkjet printing these components may be especially useful as alignment could be done in real-time. Furthermore, throughput would not be diminished since less than 50 drops per transistor would be needed. Similarly, inkjet printing of the semiconductor may also be easier. This is due to the fact that the drops could be properly aligned to each transistor. Also, the inkjet droplet volume is very precise and thus the exact amount of semiconductor required could be used. Thus, this minimizes the amount used of this expensive material. It is not known what type of printing will be used for each component but these examples provide insight into how a manufacturing process might happen.

8.4.3 Semiconductors

While the actual manufacturing process remains to be seen, it will obviously be dependent on the type of materials being printed. Furthermore, while the body of work presented here gives several examples of what could be used to make circuits, better materials are always being sought to improve performance, ease manufacturing methodologies, and increase material libraries. The material that has the largest consequences for performance is the semiconductor. As a result, the majority of research continues to focus on developing better solution processable semiconductors. New organic semiconductors are constant being synthesized. The most recent example includes the TIPS pentacene [4]. This material suggests an air stable organic semiconductor with relatively high mobility may be obtainable. As a different route there have also been studies on inorganic semiconductors [5-7]. The main advantage to these is

their inherent air stability. However, it is not known if these will be better since trap states are prevalent at low processing temperatures tend to degrade their performance. Overall, as long as low-cost printed electronics continue to show promise, low processing temperature, solution processable semiconductor research will continue to be the main focus of research.

8.4.4 Dielectrics

The dielectric material is another critical component in active devices that requires further research. It is not known whether an organic route or an inorganic route will be best. The stability of organic dielectrics is completely unknown, and furthermore, the dielectric constant of these materials is generally no more than 4. As result, extreme smoothness is required in manufacturing in order to make sub 20V operation. As previously discussed, another route is to use inorganic dielectrics [8-11]. These could potentially provide a high k solution, however they have yet to be proven to work well in a low cost process. Additionally these may not be easily integrated with organic materials.

8.4.5 Improving Integration

Another issue that requires a great deal of work is the integration of these materials. Although proper integration is critical for some of the materials to function, it is also critical for optimization and long term reliability. For example, it is already known that interlayers will be required for organic semiconductors in order to minimize contact barriers and also to minimize bias stress effects that degrade performance [12]. More so,

energy band discontinuities tend to degrade interfaces because excess carrier energy causes bonds to break. An interlayer will help minimize these energy drops and thus improve long term reliability. Also, the dielectric, semiconductor interface is another interface that requires careful attention to proper material compatibility [13]. All of these issues are critical to better performance and long term reliability.

8.4.6 Circuit Prototyping

Finally, it is critical to start integrating low cost devices into full circuits to get an idea of how these devices will perform in real circuits instead of DC testing [14]. Initial AC tests were performed in this body of work to characterize the f_t of these devices. This gives an idea of the maximum frequency performance to expect from a circuit. However, it is no substitute for actual circuits. Also relevant are investigations that identify the minimum device performance needed for a given circuit topology and clock frequency.

8.5 Conclusions

Gravure printing is a complimentary printing technology to inkjet that can increase throughput of the overall printing manufacturing process. However, due to its difficultly with alignment, inkjet is still a very useful technology that can align in real-time.

Before undertaking full scale gravure printing research, initial screening experiments were required to identify suitable materials and other printing concerns. These experiments showed that the previously used inkjet inks cannot simply be transferred to gravure printing. Instead they will have to be modified to increase their

viscosity. Other effects such as minimum printable dimensions remain largely unexplored.

Before low cost electronics can be considered manufactureable, clearly there is a very large amount of work required. Some of the issues that require further research include advanced printing methodologies, semiconductor development, dielectric development, better integration techniques, and circuit prototyping. However, still completely unknown is the reliability of these devices. This is particularly difficult because of the air sensitivity of many organic semiconductors. Despite this large amount of work still needed, this body of work serves as a starting point to identify the progress, as well as what is needed, to get low-cost printed electronics to a point where they can be considered manufacturable and these reliability tests can be carried out in depth.

Chapter 9

Summary and Conclusions

In this work the idea of low-cost printed electronics was presented as a means to substantially reduce the cost of conventional electronics manufacturing. Based on this idea an inkjet testbed was custom built to overcome the deficiencies associated with commercial inkjet printers. Using this printer and custom synthesized inks, processing techniques were developed to print interconnects, dielectrics, and organic semiconductors. By combing these materials and techniques, all-printed transistors were fabricated. The design of these transistors was optimized and the measured f_t of these devices was 477 Hz. Through materials and structure improvements, devices with a f_t of >500kHz is possible and thus the performance requirements for RFID can be met. However, in order to manufacture these electronics with a high enough throughput, another form of printing, gravure printing, will likely be required. As a result, initial investigations of this technology were carried out.

9.1 Summary

9.1.1 Introduction to Low Cost Printed Electronics

Low-cost printed electronics seek to reduce the cost of conventional electronics manufacturing by employing all-additive printing process techniques. The advantages of this include elimination of photolithography, elimination of vacuum processing, reduced abatement cost, and higher throughput. All of these advantages lower the manufacturing

costs for applications such as RFID tags, displays, PCB/keypads, chemical sensors, etc. And, in the end, if the cost goals are achieved, the ubiquity of these electronics would be greatly increased. However, before manufacturing these products, basic research must be carried out to determined feasibility and performance limitations. The goal of this work was to create a more extensive study that will form the starting point of a larger picture for future studies in low-cost printed electronics.

9.1.2 Inkjet Printing Technology and Experimental Testbed

In comparison to gravure printing, inkjet printing has much less throughput, but has advantages in both pattern making flexibility and ease of alignment. Commercially available printers are deficient in their droplet placement accuracy, motion precision, solvent compatibility, and substrate accommodations for use in electronics fabrication. As a result a custom testbed was designed and assembled that had all the necessary characteristics. For the testbed designed here, it uses one dispenser for each material. Though throughput is limited, this is adequate for research since the goal is prototyping and thus flexibility is required. Because of the stringent requirements in electronic fabrication, careful attention and design had to be taken for each of the subsystems. This includes the choice of motion stages, choice of dispenser, pressure system design, delivery path design, choice of substrate chuck, software design, and alignment routine design.

9.1.3 Inkjet Processing Techniques and Passive Components

High-quality passive components are a crucial component technology required for the demonstration of low-cost all-printed electronics and in particular RFID. In printing these components a phenomenon known as the “donut effect” is a significant challenge. Because of these printing effects, proper ink selection and formulation are critical. There are a wide variety of ink candidates including organic and inorganic, however gold nanoparticles are the best. Using gold nanoparticle-based conductors and polyimide and PVP dielectrics, inkjet printing has demonstrated a high-quality interconnect and inductive component technology. It offers high levels of conductivity in a printed film, and enables high quality inductors and a robust multilevel interconnect scheme. By optimizing the jetting parameters, the most important of which are substrate temperature and choice of solvent, it is possible to produce low-resistance conductor lines and dielectrics with excellent surface morphology and electrical characteristics.

9.1.4 Low Cost Semiconductors and Printing

Organic semiconductors are particularly applicable to low cost flexible electronics because they are inherently flexible, can be easily solution processed, and the large body of knowledge in organic synthesis allows specific tailoring and flexibility of their properties. The two models used to quantify the transport are the variable range hopping model and the multiple trap and release model. The latter is believed to be more applicable to higher crystalline organic semiconductors. A pentacene precursor developed is well suited to inkjetting as it offers both high performance and solution processing. An ink formulation was developed for this material and optimization schemes for characterization and performance have been obtained showing that as the thickness

increases so does the mobility. By obtaining mobilities of 0.1-0.2 cm^2/V-s the intrinsic performance of this material suggests that these devices may be suitable for many electronic applications. However, further optimization of this material is required.

9.1.5 A Baseline Process for All-Printed Transistors

A baseline process for an all-printed transistor was developed. In order to make these devices the proper ink formulations and printing techniques must be used for each layer in order to obtain the proper smoothness, shape definition, and thickness. The overall performance of these devices was rather good, especially the DC parameters of the baseline devices. Despite the fact that the electric fields were only 2MV/cm in these devices, they still obtained mobilities approaching 0.2 cm^2/V-s. The two major shortcomings of these devices was the high operating voltages required to run the devices and the non-optimal structure (annular) for high frequency operation.

9.1.6 Gate Dielectric Scaling

The baseline transistors were optimized to produce low operating volt devices along with better frequency operation. Because the test bed cannot print both smooth and well-defined gates, simulated gates were made through use of evaporative techniques. Using this process, along with substrate engineering, the gate dielectric was aggressively scaled as thin as ~200Å while retaining a dielectric strength of 7.3 MV/cm. This dielectric technology allowed the realization of transistors with operating voltages <10V. Optimized gate-source and gate-drain overlap was also realized, which is expected to result in improved AC performance.

9.1.7 Frequency Performance and Characterization

RFID is also the most challenging lost cost electronics application due to the necessity for relative high speed >200 kHz operation. However, if RFID can be manufactured in a low cost fashion, a whole host of other lost cost technologies are also available. To facilitate this technology, it is necessary for the transistors to function at a ~200 kHz sideband frequency, and, as a result, the required f_t is >200 kHz.

A simple measurement was developed to measure the f_t of the transistors fabricated in Chapter 6. The f_t of the transistor measured for this work is 477Hz. While this is far from the performance necessary for RFID, further improvements in both semiconductor mobility and minimizing overlap capacitance will provide the necessary performance, >500 kHz. Thus this work provides a manufacturing route to achieve the performance required for RFID and, indeed, RFID is becoming tantalizingly near.

9.1.8 Gravure Printing and Future Work

Gravure printing is ideal method of printing to enhance throughput. However, its disadvantages suggest that it is not the best solution for low cost manufacturing. Rather, a hybrid manufacturing process combining both inkjet and gravure may be best. Initial investigations in gravure printing revealed that a new ink is required for further development. The majority of the problems encountered stem from the fact that the nanoparticle inks are too low in viscosity. Along with this problem there are still many issues that need to be explored in this technology including, alignment and minimum shape size.

Further research required in low cost electronics includes better semiconductors, better dielectrics, better material integration schemes, and circuit prototyping.

9.2 Concluding Comments

Over the past 5-10 years interest in low cost electronics has increased dramatically. Low cost printed electronics seek to minimize the area limitations and number of steps associated with conventional silicon processing. As an example, low-cost printed electronics could reduce the cost per RFID chip below 2 cents per tag. This is done primarily through the use of printing technologies such as inkjet and gravure. By using these technologies, the processing now becomes all-additive, there is no expensive lithography or vacuum processing, and there are reduced abatement costs. All contribute to cost savings.

There has been progress on two fronts that have allowed this research to grow and flourish: materials development and better printing technologies. Organic semiconductors have long been a fascinating research subject but recently they have started to become considered manufacturable due to their performance increases and ease of manufacturability. Some semiconductors that are being considered include pentacene and TIPS. These are attractive because they offer good air stability, solution processing, and adequate performance.

There are a variety of interconnect materials that are already being used in low-cost applications. However to achieve high performance and allow compatibility with printing there are fewer relevant materials. Among them are the nanoparticle based inks. These are especially attractive since a wide variety of metals can be synthesized.

Although there are existing inks, the least amount of work has focused on low cost dielectrics. Some of these inks include low temperature polyimide and PVP. An active area of research in this field includes inorganic nanoparticle and chemical bath deposited dielectrics.

Another area of research that has facilitated research in low cost electronics is printing technology. More precise inkjet printers are constantly being sought in this field. This includes smaller drops, more accurate and precise drop placement, better motion precision, better alignment routines, and larger dispenser arrays. All of these factors contribute to higher performance electronic circuits. Gravure printing is less widely studied for a couple reasons. It is relatively new in its application to low cost electronics fabrication and it is better suited to manufacturing rather than research. Despite this it is still necessary to carry out gravure based investigations. This area will grow dramatically as low cost electronic comes closer to manufacturing.

Overall, there is a very large amount of work required before these low cost circuits can even be considered manufacturable. Despite this, tremendous progress has already been made in the past five years. Although this work primarily deals with device fabrication and optimization, much research is required in circuit design. Particularly challenging is the design of circuits with minimally performing devices. This is in contrast to conventional silicon design. Despite this, as the area of research continues to grow, circuit design in this area will become more prevalent. Ultimately widespread manufacturing is not far off, 5-10 years, and once they become manufacturable they will be cheaper per unit area than silicon. Because of this they will greatly increase the ubiquity of electronics in everyday life.

Appendix A

Passive Components and Tank Circuit Theory

A.1 Passive Component Quality Factor, Q

The quality factor, Q, of a passive component is important because it represents the inherent losses of that component. A higher Q in a particular passive component indicates fewer losses in that component. Less losses are better because this means more power is coupled into the circuit rather than being dissipated in the component. Thus it is ideal to achieve the maximum component Q possible in a given manufacturing process. [1]

A.1.1 Inductor Q

The Q of an inductor is defined as the Q an LC tank would have if the capacitor is ideal and lossless. An inductor with losses is modeled as shown below (FigureA.1) [2]:

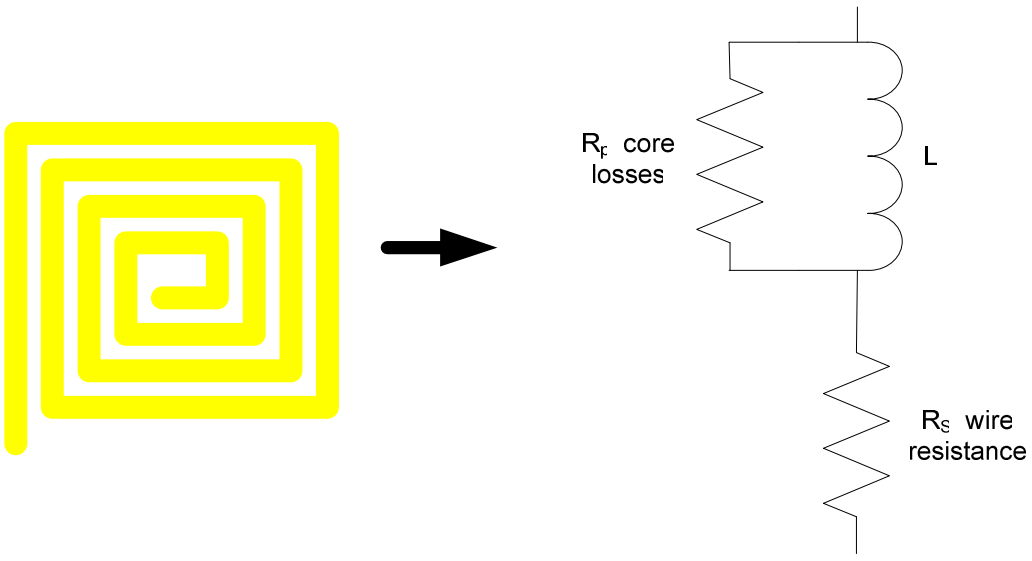


Figure A.1: Model of losses in an inductor.

R_p represents losses of the magnetic flux around the windings while R_s represents losses from the resistance of the windings. Assuming the frequencies are not too high, R_p can be neglected (the maximum low cost frequencies, 13.56 MHz, do not approach this limit). Thus the Q of a single inductor is:

$$Q_L = \frac{\omega L}{R_s} \qquad \textbf{Eqn (A.1)}$$

A.1.2 Capacitor Q

Analogous to the inductor, the Q of a capacitor is defined as the Q of a tank with an ideal, lossless inductor across the capacitor. Similarly, a capacitor can be modeled with the losses as shown below (Figure A.2) [2]:

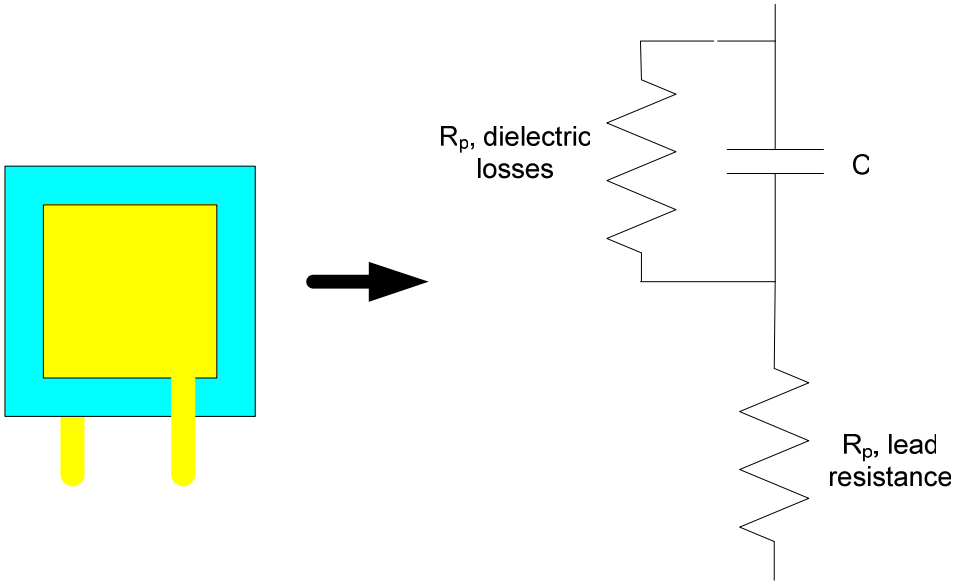


Figure A.2: Model of losses in a capacitor.

Analogously, R_p represents losses of the dielectric while R_s represents losses from the resistance of the lead. Also again, assuming the frequencies are too high, R_p can be neglected. Thus the Q of a single capacitor is:

$$Q_C = \frac{1}{\omega C R_S} \qquad \textbf{Eqn (A.2)}$$

It is important to note that this quality factor is generally not as important as the quality factor of the inductor. This is because the losses in a capacitor are generally much less than that of an inductor since the capacitor's leads are short and thus have low resistance. This is in contrast to long windings in an inductor that have a much higher resistance.

A.2 Tank Circuit Theory

Typically the passive components, inductors and capacitors, are found together in a "tank" circuit. Such a circuit is shown in Figure A.3. This particular circuit is stimulated with current source I at various frequencies.

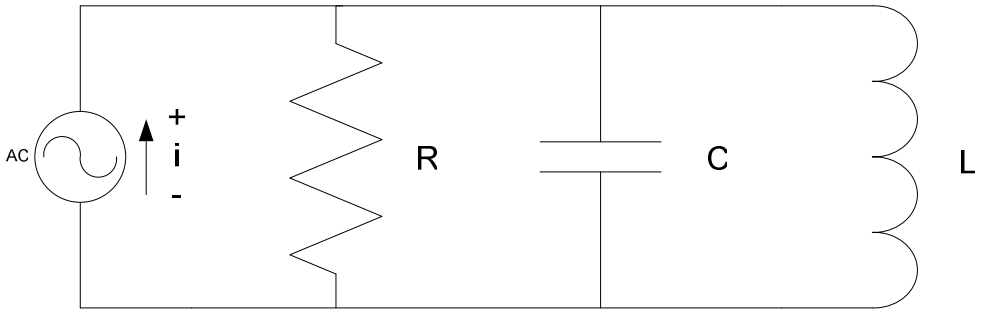


Figure A.3: Electrical schematic of a tank circuit.

The following analysis describes how to find the magnitude of the impedance and the phase of the impedance. This gives all the relevant information needed to calculate the voltage across the current source [3, 4]:

$$Z_i(j\omega) = \frac{v_i}{i_i}(j\omega) = \frac{1}{\frac{1}{R} + j\omega C + \frac{1}{j\omega L}} = \frac{1}{\frac{1}{R} + j(\omega C - \frac{1}{\omega L})} \qquad \textbf{Eqn (A.3)}$$

$$|Z_i(j\omega)| = \sqrt{|Z_i(j\omega)||Z_i(j\omega)|^*} = \frac{1}{\sqrt{\frac{1}{R^2} + j(\omega C - \frac{1}{\omega L})^2}} \qquad \textbf{Eqn (A.4)}$$

$$\angle Z_i(j\omega) = -\arctan\frac{\omega C - \frac{1}{\omega L}}{1/R} \qquad \textbf{Eqn (A.5)}$$

At resonance both L and C oscillate at the same frequency, ω_o:

$$\frac{1}{\omega_o C} = \omega_o L \Rightarrow \omega_o = \frac{1}{\sqrt{LC}} \Rightarrow |Z_i(\omega_o)| = R \qquad \textbf{Eqn (A.6)}$$

The impedance and phase can be plotted as a function of frequency as seen in Figure A.4 [3, 4].

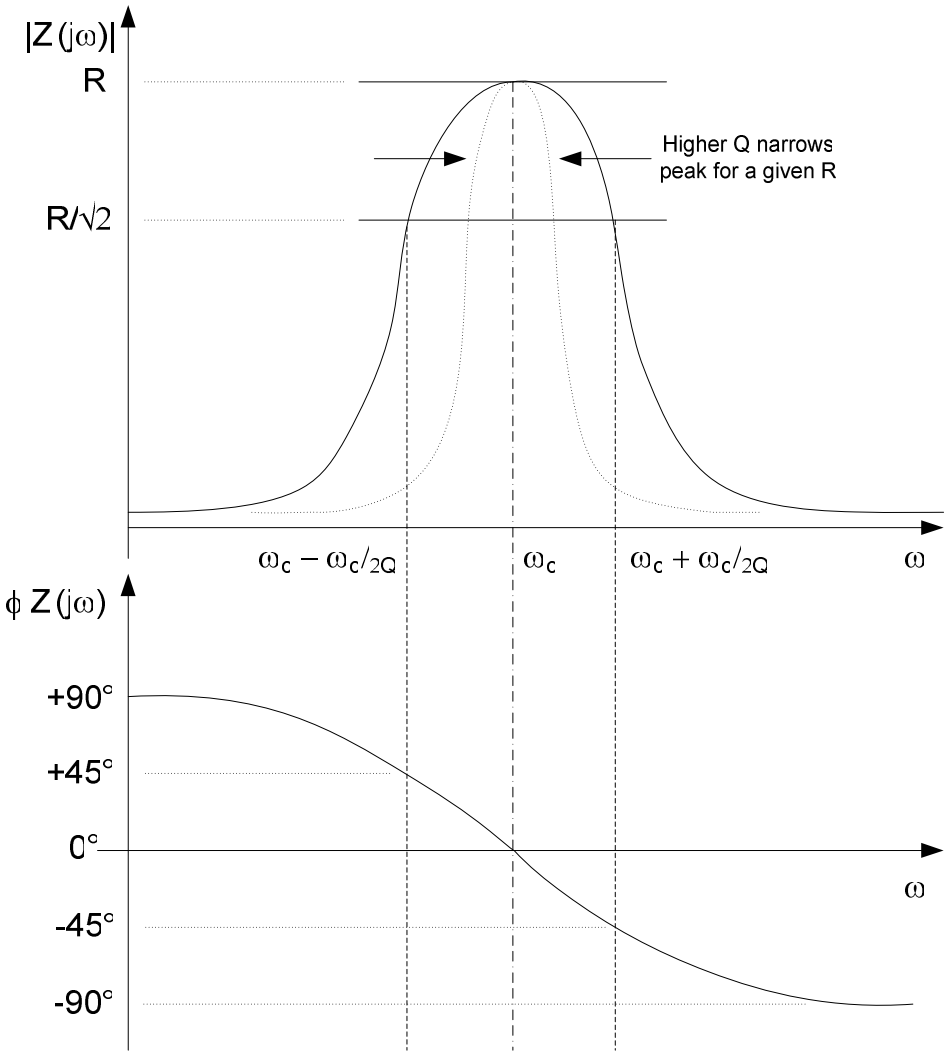


Figure A.4: Impedance and phase as a function of frequency for a tank circuit.

Furthermore, as an example, consider the following:

$$v_i(j\omega) = Z_i(j\omega) i_i(j\omega) \qquad \textbf{Eqn (A.7)}$$

$$i_i(t) = I_1 \sin(\omega t) \Rightarrow | i_i(j\omega) | = I_1 \qquad \textbf{Eqn (A.8)}$$

And

$$\angle i_i(j\omega) = 0 \qquad \textbf{Eqn (A.9)}$$

Thus

$$|v_i(j\omega)| = |Z_i(j\omega)| \, x \, |i_i(j\omega)| \qquad \textbf{Eqn (A.10)}$$

And

$$\angle v_i(j\omega) = \angle i_i(j\omega) + \angle Z_i(j\omega) = \angle Z_i(j\omega) = \phi \qquad \textbf{Eqn (A.11)}$$

Therefore

$$v_i(t) = I_1 \, |Z_i(j\omega)| \sin(\omega t + \phi) \qquad \textbf{Eqn (A.12)}$$

A.3 Tank Circuit Quality Factor

The quality factor, Q, of the tank is defined as [4]:

$$Q = \frac{\text{Resistance of R (shunt)}}{\text{Impedance of L or C at resonance}} = \frac{R}{\omega_o L} = \omega_o CR \qquad \textbf{Eqn (A.13)}$$

For higher Q's the peak of the impedance gets sharper and higher, assuming R increases as well (Figure A.2 assumes constant R). This parameter is extremely important for LC tanks because it is a measure of the multiplication factor of the tank. Consider a tank circuit where a RF signal is input into the inductor at the tank's resonance frequency. This signal generates some voltage V_L in the inductor:

$$\frac{v_L}{\text{Inductor Impedance}} * \text{Resistance, R} = \text{v}_\text{L} * \frac{1}{\omega_\text{o}\text{L}} * R = v_L * Q = v_{coupled} \qquad \textbf{Eqn (A.14)}$$

Hence the voltage coupled into the circuit is the voltage coupled into the inductor multiplied by Q. Thus the Q factor is a multiplication factor of the tank circuit. This is important because the higher the output voltage, the more energy/power that gets coupled into a power harvested circuit. Thus a reader sending the power signal can be operated at longer distances with use of higher Q tanks in the receiving circuitry.

Appendix B

Gold Nanoparticle Synthesis

B.1 Introduction

The gold nanoparticle synthesis described here was originally created by Hostetler, *et al.* [1]. The process was developed further by Huang, *et al.* to make the nanoparticles suitable for printed electronics [2]. For the purposes of this work the nanoparticles were made using the following recipe. Also described is how to change the surfactant. In virtually all experiments in this work 1.5 nm hexanethiol encapsulated nanoparticles were used.

B.2 Chemicals Required

Hydrogen tetrachloroaurate(III) hydrate ($HAuCl_4 \cdot xH_2O$)

1-Dodecanethiol ($C_{12}H_{26}S$)

1-Octanethiol ($C_8H_{17}SH$)

1-Hexanethiol ($C_6H_{13}SH$)

1-Butanethiol (C_4H_9SH)

Sodium borohydride ($NaBH_4$)

Tetraoctylammonium Bromide ($C_{32}H_{68}BrN$)

Toluene (C_7H_8)

Deionized water

Ethanol (C_2H_5OH)

Acetone ($(CH_3)_2CO$)

Dry Ice (CO_2)

B.3 Laboratory Equipment

1000 mL Erlenmeyer Flask

400 mL Glass Cup

1000 mL Titration Flask

Rotary Evaporator

High-Frequency Sound Wave Generator

Fine Glass Filtration Frit

Magnetic Stir Bar and Stirrer

Pipette capable of measuring up to 5mL

1000 mL Vacuum Flask

B.4 General Process

The general process is divided into two steps, synthesis and purification, and proceeds as follows. Ionic gold dissolved in water is transferred into toluene using an organic transfer reagent, tetraoctylammonium bromide. The two phase solution is separated. Next, an alkyl thiol encapsulate is added to this solution where the length of the alkyl chain is chosen to achieve the desired sintering temperature of the nanoparticle. The molar ratio of the thiol to ionic gold determines the size of the nanoparticles. This solution is then reduced using sodium borohydride. The solvent is then evaporated off the

solution and the resulting nanoparticles are clean and purified. The chemical properties for reactants are given in Table B.1.

B.5 Detailed Synthesis

The detailed process is described below along with the equipment used for each step.

B.5.1 Synthesis

1) Using a 1000 mL Erlenmeyer flask and a large stir bar, add 12.10g of tetraoctylammonium bromide to vigorously stirred (700-800 rpm) 645mL toluene. (Organic phase)
2) Using a 400 mL glass cup, add 2.5g (see note below) of $HAuCl_4 \cdot xH_2O$ to 200mL of deionized water. This will be a yellow solution. (Aqueous phase)
3) Mix the two solutions together - the aqueous phase in the vigorously stirred organic phase. After mixing turn off the stir bar. The two phases will now separate and the aqueous phase will be clear while the organic phase will be orange-brown.
4) Using a titration flask, isolate the organic phase by draining off the aqueous phase into a separate flask. After, drain the organic phase back into a 1000 mL Erlenmeyer flask. The organic phase is now ready for the final steps.
5) Using the pipette add the desired molar ratio amount of thiol, 4 moles of thiol to 1 mole of gold, 4.152mL of hexanethiol (this will make 1.5 nm crystals). The solution must be stirred for at least 15 minutes at room temperature (700-800 rpm). The

solution will become pale yellow or colorless. Table B.2 gives ratios for other encapsulates.

6) Using the 400 mL glass flask mix 3.065g of $NaBH_4$ in 200mL of deionized water. (Reduction solution)
7) Vigorously stir (700-800 rpm) the organic phase as the reduction solution is added in. Pour the reduction solution into the organic phase over 20 seconds. The solution will become very dark.
8) Stir the solution for at least 3 hours and 30 min at room temperature.

B.5.2 Purification

1) Using the same technique as above, isolate the organic phase from the aqueous phase using the titration flask and the 1000 mL Erlenmeyer flask.
2) Pour the organic phase in a 1000 mL rotary flask and evaporate all the solvent from the organic phase using the rotary evaporator and dry ice. Do not allow the temperature to exceed 35°C to prevent partial decomposition of large gold cluster and removal of surfactant.
3) Suspend the particles in 242mL of ethanol in the rotary flask and sonicate the suspension briefly using the high-frequency sound wave generator for complete dissolution of the products.
4) Collect particles with fine glass filtration frit, a 1000 mL vacuum flask, and vacuum line hooked up to the flask. Rinse the collected particles with at least 645mL of ethanol and 1210mL of acetone.
5) Dry the particles by leaving on the frit for at least 10 minutes.

Chemical	Formula	MW (amu)	Mp (°C)	Bp (°C)	d (g/mL)
Hydrogen tetrachloroaurate(III) hydrate	$HAuCl_4 \cdot xH_2O$	339.79	--	--	3.900
1-Dodecanethiol	$C_{12}H_{25}SH$	202.40	-7	266-283	0.845
1-Octanethiol	$C_8H_{17}SH$	146.30	-49	197-200	0.843
1-Hexanethiol	$C_6H_{13}SH$	118.24	-80	150-154	0.838
1-Butanethiol	C_4H_9SH	90.19	-116	98	0.842
Sodium borohydride	$NaBH_4$	37.83	36	400	0.945
Tetraoctylammonium Bromide	$(C_8H_{17})_4BrN$	546.82	97-99	--	--
Toluene	$C_6H_5CH_3$	92.1402	-93	110.6	0.867
Deionized water	H_2O	18.0152	0	100	0.955
Ethanol	C_2H_5OH	58.0798	-94.3	56.2	0.7857
Acetone	C_3H_6O	46.0688	-114.1	78.3	0.789

Table B.1: Properties of chemicals used in nanoparticle synthesis.

Hydrogen tetrachloroaurate(III) hydrate-2.00g (0.005886 mol)

Chemical	1:1		3:1		4:1		1/12:1	
Dodecanethiol	1.1908g	1.4092mL	3.5724g	4.2276mL	4.7632g	5.6368mL	0.09924g	0.11744mL
Octanethiol	0.8608g	1.0212mL	2.5824g	3.0636mL	3.4432g	4.0848mL	0.07172g	0.08512mL
Hexanethiol	0.6956g	0.8304mL	2.0868g	2.4912mL	2.7824g	3.3216mL	0.5796g	0.0692mL
Butanethiol	0.5308g	0.6304mL	1.5924g	1.8912mL	2.1232g	2.5216mL	0.04424g	0.05252mL

Table B.2: Surfactant ratios for Au nanoparticles.

NOTE: Ionic gold chloride is light sensitive and air sensitive. Once the vial is opened, dissolve the gold into water immediately. Once in solution the gold is relatively stable. In order to make sure all the gold is used, pour out the entire content of the 5g vial into a beaker. Then pour water into the vial to dissolve all left over gold. Wash out the vial about 2-3 times to ensure all the gold is used. Measuring the amount of gold can be difficult. To do this, dissolve all 5g in 400mL of water. Mix the solution well to ensure that the concentration is evenly distributed in the solution. Measure out 200mL of the solution for 2.5g of gold. Run two reactions simultaneously to use up all 5g and ensure freshness of the gold solution.

Appendix C

Electronic Transport in Organic Semiconductors

C.1 Introduction

The electronic transport theories developed for conventional inorganic (i.e. silicon, gallium arsenide, etc.) semiconductors all well understood and characterized. The transport theories for organic semiconductors, however, are still being developed and refined. The difficulty in developing a unified theory is that organic semiconductors exhibit a rather large amount of disorder in comparison to inorganic semiconductors, which are mostly well ordered. Furthermore, there is a very large range in the amount of disorder in these materials; some show a large amount of crystallinity and others, being polymers, show only minimal crystallinity that is basically only localized to immediate molecular chains. Because of this large range in the amount of order there have been models developed that characterize the better ordered materials while other models better describe the poorly ordered materials.

The models developed for these materials seek to describe the electronic behavior of the materials in the context of outside influences. The most important merit to characterize semiconductors is the mobility of the carriers. The mobility describes the speed of the carriers in the presence of an electric field. In particular, the current density, J (A/cm^2), flowing through a semiconductor is equal to the product of the number of available carriers, n ($/cm^3$), the fundamental constant, q (C), the mobility, μ ($cm^2/V\text{-}s$), and the electric field, ε (V/cm) :

$$J = n * q * \mu * \varepsilon \qquad \textbf{Eqn C.1}$$

In devices, higher currents typically mean faster, higher performance devices, and as a result, the mobility is directly related to the speed and performance of a device (see Chapter 7 for more explanation). Thus it is critical to understand the fundamental physics that govern mobility. Ideally this would facilitate methods to optimize the mobility of materials as well as predict how it is affected by external factors.

The field of organic semiconductors is relatively new compared to inorganic semiconductors and as a result there is still much debate and discussion of the fundamental models that govern transport in organic materials. Despite this, there are some common ideas that many scientists agree on. Furthermore, most of the newer theories build upon the older, basic theories. Generally speaking, the mobility in organic semiconductors is affected by the amount of order in the material, the temperature, and the electric field applied to the material. As a result, there are theories developed to the express the dependence of temperature on mobility as well as theories that explain the electric field dependence. However, these separate dependencies are not exclusive and can usually be combined to form one theory. Particular to this discussion is that there are two different theories for temperature dependence and thus breaking up the discussion based on temperature and electric field dependencies makes it easier to explain the separate theories. This section will describe the prevailing theories of transport in organic semiconductors separated into their dependencies on temperature and electric field. This is done in the context of conventional semiconductor band transport theory and how the large degree of disorder causes deviations from band transport theory.

C.2 Introduction to Band Transport Theory

Traditional band transport theory describes carrier transport through the use of bands that the carriers occupy. These bands arise for the following reason. As two semiconductor atoms are brought together, the energy levels of the electrons split due to the Pauli Exclusion Principle. As more atoms are brought into the system the energy levels continue to split. In a large enough sample all the atoms are ordered through the crystallinity of the lattice. This order allows long range interactions and thus there are so many energy levels that the levels tend to smear together and form bands of energy levels. [1]

Then conduction occurs as follows. The highest occupied band is known as the valence band while the lowest unoccupied band is known as the conduction band. Electrons in the valence band are not free to move within the lattice. However upon excitation the electrons are excited into the conduction band where they are free to move around. They leave a hole in the valence band which is also free to move around and also contributes to conduction. With application of an electric field the electrons and holes traverse across the crystal in the opposite directions. However, these carriers are scattered off of ionized impurities and lattice vibrations or phonons. Both of these factors lower the mobility of these carriers. The phonons generally increase with temperature. For the purpose of this discussion these factors cause two critical dependencies in this model. First, generally speaking, the mobility is constant with the application of an electric field (not considering surface scattering in field effect transistors). Second, because an increase in temperature will increase the number of phonons, more carrier scattering will result, and thus the mobility will decrease. [1]

Organic semiconductors have energy levels that are analogous to the bands in inorganic semiconductors. They are the HOMO (highest occupied molecular orbital) and the LUMO (lowest unoccupied molecular orbital). However, because the large degree of disorder in these materials gives rise to numerous trap states, band transport theory does not properly model transport in organic semiconductors.

C.3 Temperature Effects on Organic Semiconductor Transport

There are two prevailing theories describing the effect temperature has on the mobility of an organic semiconductor. The theories are known as the multiple trap and release model (MTR) and the variable range hopping model (VRH).

C.3.1 MTR Model

The first theory, MTR, was originally developed to describe behavior in amorphous silicon and other systems displaying a much higher degree of disorder than inorganic semiconductors [2]. The basic idea is that the density of states equation does not reach zero at the conduction band edge. Instead, because of the disorder and hence large amount of trap states of the material, there are localized states that cause an exponential band tail to extend past the conduction and valence bands.

This particular model has three distinct temperature regions of operation. At high temperatures (room temperatures) the carriers can move in the extended states near the conduction band, but still interact with the localized states through trapping and thermal release. This trap controlled mobility can be modeled as [2]:

$$\mu_1 = \mu_o \alpha \exp(\frac{-(Ec - E)}{kT}) \qquad \textbf{Eqn C.2}$$

Where E_c is the energy of the conduction band and E represents a single level of trap states with corresponding energy. The exponent can be likened to the rate of thermally activated release from trap states. α is the ratio of extended states to trap states and μ_o is a type of intrinsic mobility equal to mobility of the carrier near the bottom of the extended states. μ_o can be modeled as [2]:

$$\mu_o \approx (\frac{qa^2}{6kt})v_{e1} \qquad \textbf{Eqn C.3}$$

where this mechanism occurs through delocalized states near E_c such that the mean free path is close to the interatomic spacing, a. This is likened to Brownian motion where v_{e1} is the electronic frequency.

At lower temperatures the carriers do not obtain enough energy to release from the localized trap states and the transport enters another region of operation. In this region transport becomes phonon assisted hopping between the localized trap states. This can be modeled as [2]:

$$\mu_2 \approx (\frac{qa^2}{kT})v_{ph} \exp(\frac{-W}{kT}) \qquad \textbf{Eqn C.4}$$

where v_{ph} is the phonon frequency and W is the activation energy for hopping.

At even lower temperatures the transport is believed to occur through hopping between traps states near the Fermi level. This type of transport is similar to that of the VRH model and will be described in the next section.

C.3.2 VRH Model

The VRH model was developed as a result of the fact that many organic semiconductors are too disordered to demonstrate any resemblance of band transport. Therefore the major difference between the MTR and VRH models is that the VRH model does not include any extended states and transport occurs strictly through hopping between trap states. Thus the density of states is similar to that of the MTR model except that the extended states are not included. At low biases the hopping between traps can be modeled as a resistor network using percolation theory where the conductance between states i and j is [3]:

$$G_{ij} = G_o \exp(-s_{ij}) \qquad \textbf{Eqn C.5}$$

Where s_{ij} is the following:

$$s_{ij} = 2\alpha R_{ij} + \frac{\left|E_i - E_F\right| + \left|E_j - E_F\right| + \left|E_i - E_F\right|}{2k_B T} \qquad \textbf{Eqn C.6}$$

where E_x is the energy of the respective energy level and E_F is the Fermi level. The first term on the right hand side of this equation describes the tunneling of the carrier with R_{ij} representing the distance between states and α represents the wave function overlap. The second term represents the difference in energy of the state that the carrier is hopping to and the occupational probability of the states.

Using percolation theory, the exponential density of states is combined with the previously described conductance to calculate the following conductivity [3]:

$$\sigma(\delta,T) = \sigma_o \left(\frac{\pi N_t \delta (T_o/T)^3}{(2\alpha)^3 B_c \Gamma(1-T/T_o)\Gamma(1+T/T_o)}\right)^{To/T} \qquad \textbf{Eqn C.7}$$

where δ is the fractional site occupancy, $\Gamma(z)$ is:

$$\Gamma(z) \equiv \int_0^\infty dy \exp(-y) y^{z-1} \qquad \textbf{Eqn C.8}$$

and B_c, the percolation criterion is:

$$B_c \approx \pi(\frac{T_o}{2\alpha T})^3 N_t \exp(\frac{E_F + s_c k_B T}{k_B T_o}) \qquad \textbf{Eqn C.9}$$

Coupling the conductivity equation to the gate voltage controlled occupancy factor and Poisson's equation, the field effect mobility is calculated [3]:

$$\mu_{FE} = \frac{\sigma_o}{e}(\frac{\pi(T_o/T)^3}{(2\alpha)^3 B_c \Gamma(1-T/T_o)\Gamma(1+T/T_o)})^{To/T} * (\frac{(C_i V_G)^2}{2k_B T_o E_s})^{To/T-1} \qquad \textbf{Eqn C.10}$$

Buried in this equation is the fact that the mobility has a Arrhenius like dependency, $\mu \sim \exp(-E_a/kT)$. As a result, just like the MTR theory, the mobility increases with temperature. This is in stark contrast to band transport theory. Also this equation shows a V_G dependant mobility. This is a result of the fact that as the V_G bias increases the state occupancy factor increases. Although not explicitly defined in the MTR model, the MTR model also shows a voltage dependent mobility. These reasons for this are described in the next section.

The MTR and VRH models are quite similar, indeed, with both showing Arrhenius behavior [2-5] and, using the correct fitting parameters, either model can be fitted to experimental data. In fact, within accessible temperatures ranges the two models cannot even be distinguished [4]. However, it may be suggested that materials that do exhibit MTR behavior are more ordered and crystalline. The MTR theory itself is based on "disordered" inorganic semiconductors and the theory suggests that at low enough temperatures the carriers in these materials convert to a VRH mechanism. Thus one could conclude that the theories coincide. Materials that are ordered enough to demonstrate

MTR also demonstrate VRH at lower temperatures while some materials are too disordered to exhibit any sort of MTR behavior.

C.4 Electric Field Effects on Organic Semiconductor Transport

All organic semiconductors have a voltage dependent mobility. In field effect transistors these effects show up as a gate voltage dependent mobility, while in two terminal diode devices the effect is known as space charge limited current. Since the majority of work in this thesis relates to FETs, only the gate dependent mobility will be discussed. However, the fundamental reason for both phenomena are the same: at room temperature the number of thermally generated carriers is small, and as the external applied voltage increases, the Fermi level moves closer to the valence band (assuming p-type materials) filling deep trap states and thus activating shallower traps for which hopping and release can more easily occur (i.e. the trap and release rates are faster).

C.4.1 Gate Dependent Mobility in FETs

In accumulation mode FETs the thickness of the conduction layer is difficult to measure and quite often is modeled as a sheet of charge. As a result it does not make sense to talk about space charge limited conduction based on charge density. Thus the space charge formulation used for diodes does not apply to FETs even though the fundamental reason for each is similar.

Both the MTR and VRH models use a power series relationship of the following form to model the mobility [4-6].

$$\mu_{FET} = K(V_{GS} - V_T)^{\alpha} \qquad \textbf{Eqn C.11}$$

where α falls between 0 and 1. Because of the α and K fitting parameters this equation can be fit to a wide variety of data assuming the data fits a power series relationship [7]. Thus the weakness of these models is that these parameters are usually found empirically.

Typically, in FETs the drain voltage is constant (i.e common source circuit) and the gate voltage is modulated. As a result the field dependant mobility increases with increasing gate voltage. Thus the field increasing the mobility is perpendicular to the direction of current. This is different from diode where the field and current direction are parallel. Because of this, the mobility will increase with increasing gate voltage until it saturates and decreases due to carrier scattering at the interface. This scattering effect also occurs in conventional inorganic FETs and shows itself as a saturation and then decreases in transconductance (see Chapter 6 for example).

Appendix D

Pentacene Precursor Synthesis

D.1 Introduction

The pentacene precursor synthesis was originally created by Afzali, *et al.* [1]. It was then formulated in house with slight modification by Volkman [2]. For the purposes of this work the precursor is made using the following recipe.

D.2 Chemicals Required

Pentacene $C_{22}H_{14}$

N,O-Bis(trimethylsiyl)-acetamide $CH_3C[=NSi(CH_3)_3]OSi(CH_3)_3$

Thionyl Chloride Cl_2OS

Methyltrioxorhenium(VII) CH_3ReO_3

Chloroform $CHCl_3$

Hexanes C_6H_{14}

Ethyl Acetate $C_4H_8O_2$

Dry Ice CO_2

D.3 Laboratory Equipment

Sublimation Tube (Quartz)

Sublimation Heater System (3 zones with thermocouples and controllers)

Forming Gas Cylinder

Mass Flow Controller and Valve

Vacuum Pump

Bunsen Burner

250 mL Round Bottom Flask

Distillation Apparatus

100 mL Round Bottle

Schlenk Flask

Hot Air Dryer

50 mL Round Bottom Flask

Glass Reflux Tube for 50 mL Round Bottom Flask

Magnetic Stir Bar and Stirrer

High-Frequency Sound Wave Generator

2000 mL Erlenmeyer Flask

Glass Column

Silica Glass

Silica Gel

Ultra Violet Light Source

Various other common synthesis equipment including oven, ring stands, nitrogen manifold, low pressure N_2 source, vacuum pump, Teflon grease, septums, etc.

D.4 General Process

The general process consists of 4 main parts including pentacene purification, N-sulfinylacetamide precursor synthesis, pentacene precursor reaction, and precursor

purification. The pentacene is first purified through sublimation using a quartz tube, 3 zone heater, forming gas, vacuum pump, and mass flow controller. The N-sulfinylacetamide (NSO) precursor is then synthesized by slowing mixing the N,O-Bis(trimethylsiyl)-acetamide and the thionyl chloride. The NSO is then purified via a distillation. After both the pentacene and NSO are purified, they are mixed together in chloroform along with the Methyltrioxorhenium (VII) catalyst. The precursor is made by refluxing these reactants for 12 hours. The NSO reacts with the pentacene through a Diels-Alder reaction. Finally the precursor is purified through flash column chromatography. The chemical properties for reactants are given in Table D.1.

D.5 Detailed Synthesis

The detailed process is described below along with the equipment used for each step.

D.5.1 Pentacene Sublimation Purification

1) Preheat the three zone sublimation heater so that the 1st temperature zone is 260°C, the 2nd is 190°C, and the 3rd 160°C.
2) Thoroughly clean a quartz tube using methanol and the hot air dryer.
3) Place 1g of pentacene in one end of the quartz tube and place in the sublimation heater so that the pentacene rests within heater zone one.
4) Close the chamber, turn on the vacuum pump, and open the valve slowly so that the pentacene does not get sucked into the pump. Turn on the forming gas and set the mass flow controller so that 3.1 ccm/min flow. Leave for 36 hours.

5) Turn off the heaters and the forming gas. Remove the quartz tube and scrape off the purified pentacene into a glass vial. The purified pentacene will be purple and will be closest to zone 1 while the impurities will have a greenish tint and will be the farthest from zone 1. Seal the vial with Teflon tape and store in a freezer for use later.

D.5.2 NSO Synthesis

1) Flame dry a 250 mL round bottom flask and magnetic stir bar using a septum and flowing nitrogen through the septum. Do this three times, letting flask cool to room temperature between each cycle. This ensures the flask is completely dry and void of oxygen.
2) Leave the septum on and place the flask over a magnetic stirrer and add 20 mL of N,O-Bis(trimethylsiyl)-acetamide making sure the acetamide does not contact the air.
3) Slowly add 8 mL of thionyl chloride over 20+ minutes. Make sure the solution does not get too hot and boil.
4) Bake the distillation apparatus in the oven overnight. Remove the apparatus from the oven and using a nitrogen manifold flow copious amounts of nitrogen through it. This ensures the apparatus is dry and void of oxygen. Once cool, hook up the NSO filled flask onto the source side. Hook up a 100 mL round bottom flask to the waste side. Use Teflon grease where applicable. Also, flow water through the apparatus to allow product condensation.
5) Place a crystallization dish with dry ice and acetone under the waste flask. Hook up vacuum but do not turn on. Using a two way valve also keep the nitrogen hooked up.

6) Slowing turn the two way valve to the vacuum. The NSO may start to boil. If it boils turn the valve back to nitrogen. Repeat this process until the NSO no longer boils.
7) Once finished boiling, slowly apply heat using the hot air dryer. The NSO will start to boil again. The waste in the flask will be clear and may partially crystallize. Remove the heat as the NSO boils, but repeat this cycle until the waste starts to turn yellow.
8) The yellow fluid is pure NSO. Once this begins to flow into the waste flask, remove the waste flask and place the schlenk flask onto apparatus while trying not to expose anything to air. Continue applying heat until the reactant flask completely dries and the product filters into schlenk flask. Seal and remove the schlenk flask. Store in a freezer and cover with aluminum foil to avoid light exposure. There will be enough NSO for several reactions.

D.5.3 Reflux Reaction (Diels-Alder)

1) Flame dry a 50 mL round bottom flask with magnetic stir bar using a septum and flowing nitrogen through the septum. Do this three times letting the flask cool to room temperature between each cycle. This ensures the flask is completely dry and void of oxygen.
2) Get the NSO and the pentacene out of the freezer. If the vial of pentacene has large flakes gently tap the vial to break up the flakes.
3) After baking the reflux tube overnight connect it to the nitrogen manifold and flow copious amounts of nitrogen through it to keep it void of moisture and oxygen.
4) Place the round bottom flask on ring stand over stirrer and add 15 mL of anhydrous chloroform. Weigh the pentacene and pour it into the flask. Based on Table D.2

weigh out the proper amount of catalyst and pour it into the flask. Try to minimize exposure to air when opening the septum.

5) Sonicate this mixture for 1-3 minutes to remove large pentacene flakes.
6) Measure out the proper amount of NSO (Table D.2) using a long needle and a syringe. Squirt it into the reactants flask through the septum.
7) Connect the reflux tube and connect a two way valve. Connect the vacuum and nitrogen to the two way valve.
8) Turn valve to vacuum until mixture boils. Once boiling, turn valve back to nitrogen and repeat this at least ten times to bubble out all of the oxygen in the mixture.
9) Place the round bottom flask in a mineral bath so that oil just covers solvent. Bake it for 6 hours at 71-72° C. The precursor is now ready for purification.

D.5.4 Flash Column Purification

1) Mix a 4 L solution of 20% ethyl acetate and 80% hexanes. Pour 500 mL of silica gel into a 2000 mL Erlenmeyer flask. Fully wet with the 20/80 solution and pour into large column. Pack the column with air and let excess solution dry. Do not let the top of the column go dry. After packing the column, it should be about 1/3 -1/2 full.
2) Carefully load the column with precursor. Make sure to form a smooth, even layer on the top of the silica gel.
3) Add 100-200 mL of the 20/80 solution to the column being careful not to disrupt the precursor. This is easily done be squirting the solution onto the side of the column. Drain the column being careful not to dry out the precursor. Repeat this fill and drain cycle at least five times. The column is now loaded and ready to run.

4) Fill the column to the top with 20/80. Add the 100 mL reservoir to the top and continue filling. Drain the column by applying nitrogen pressure and collecting the solution at the bottom. Fill as needed and once done with the 20/80 solution switch to a 30/70 solution.
5) Periodically test the collected samples using silica glass and the following method. Using a pencil draw several dots across the bottom of the glass. Place a drop of each collection flask onto each pencil mark. Place the sample into a beaker with a little 30/70 solution on the bottom such that the marks are not submerged. Make sure to place a piece of filter paper that reaches the top of the beaker. This ensures that the silica glass wets all the way to the top. Cover the beaker and let it sit until the silica glass is sufficiently wet. Once finished remove the silica glass and let it dry. Once dry view the sample under ultra violet light. The precursor will be purple.
6) Choose the purest samples and discard the rest. Rotary evaporate the solvent. Transfer the precursor to a smaller flask, if necessary, by mixing with chloroform and then evaporating again.

Chemical	Formula	MW (amu)	Mp (°C)	Bp (°C)	d (g/mL)
Pentacene	$C_{22}H_{14}$	278.34	--	--	--
N,O-Bis(trimethylsinyl)-acetamide	$CH_3C[=NSi(CH_3)_3]OSi(CH_3)_3$	203.43	24	71-73	0.832
Thionyl Chloride	Cl_2OS	118.97	-105	78-79	1.635
Methyltrioxorhenium(VII)	CH_3ReO_3	249.23	111	--	--
Chloroform	$CHCl_3$	119.38	-64	62	1.498
Hexanes	C_6H_{14}	86.18	-95	69	0.659
Ethyl Acetate	$C_4H_8O_2$	88.12	-84	77	0.895

Table D.1: Properties of chemicals used in pentacene precursor synthesis.

Chemical	Formula	MW (amu)	Density (g/mL)	Molar ratio
Pentacene	$C_{22}H_{14}$	278.34	--	1.0
NSO	$C_2NO_2SH_3$	105.2	1.327g/mL	1.5
Methyltrioxorhenium(VII)	CH_3ReO_3	249.23	--	0.01

Table D.2: Chemical ratios in pentacene precursor synthesis.

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