Ultra Low Power Clock Generation

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Research is such a luxury in my life, and I appreciate UC Berkley to give me this opportunity to conduct this research. First of all, I heartedly appreciate the warm support by my research adviser prof. Jan Rabaey. He always inspires us, and pushes me forward to the next stage. My group mates, Davide, Nate, Simonne, Mike, Louis, Zong-de gave me valuable advices to show me new directions in my research. Mr. Dan Burke and Debo taught me how to use board design tool. I could not finish this report without their help.
I also thank ST Microelectronics for providing their 90nm process and GSRC (Giga Scale Research Center) and ERSO (UC Berkeley Engineering Research Support Organization) for funding my research.

Thank you very much

Ultra Low Power Clock Generation

using Sub-threshold MOS Current Mode Logic

by Asako Toda

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

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Date

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Second Reader

Date

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Abstract

In this research, MOS Current Mode Logic (MCML) in sub-threshold (sub-Vth) operation has been fist time investigated and applied to clock generation circuitry.

Sub-threshold operation is known to be the optimum point of operation in terms of power-speed metric, however, it is sensitive to temperature and voltage variation due to the exponential nature of this region. In order to achieve robust logic operation over PVT variation, voltage swing from high to low logic level is controlled both statically and dynamically : The static control has been done by setting enough voltage swing to convey logic level to the next stage. A DC input-output model is proposed to analyze process variation and mismatch effect, and together with Monte Carlo simulation result, the necessary voltage swing was specified. The voltage swing is also controlled dynamically by replica bias circuit and a proposed current bias circuit .

A study on coupling phenomena of ring oscillators stemmed from phase noise analysis, and mathematical behavior model was validated by Spectre simulation.

In the end of research, sub-threshold MCML is applied to 3-stage ring oscillators to generate 2G-Hz clock signal with 40uA and 1.25V power consumption.One hundred ring oscillators were implemented on a same die of 90nm CMOS process to collect the data of not only variation effect but also coupling effect of oscillators.

Contents

List of Figures

List of Tables

1 Introduction

Sub-threshold or weak inversion operation which uses leakage current has been regarded as the most power-efficient region. Our research is ultra low power clock generation, and this region, where the gm/Id hits the maximum value, is the choice taken. However, it has been unattractive for many applications that require fast processing times since MOS transistors are slow when they are operating in this region. Currently, it is applied to some low-power applications ; watches, pace-makers, and hearing aids. Also, emerging ultra low-power applications such as distributed sensor networks are a natural fit for sub-threshold circuits [3].

It is well known that in CMOS technologies beyond 90nm, leakage power is one of the most crucial design components for CMOS static logic [4]. However, the good news for the sub-threshold region is that gate current is negligible relative to sub-threshold current because it rolls off much faster with VDD. Other leakage components such as gate-induced drain leakage (GIDL) and pn-junction leakage are also negligible in sub-threshold region.
The bad news is that the sub-threshold current is very sensitive to temperature and process variation, which, in turn, limits the robustness of the sub-threshold logic [5]. These variations cause fluctuations in the voltages which have exponential effect on the sub-threshold currents.

In order to alleviate this problem, a fully differential structured CMOS Current Mode Logic (MCML) can be utilized. It brings higher immunity to supply noise and process variation. Other advantageous characteristics of MCML are lower crosstalk owing to the reduced output voltage swing, and lower generated noise level owing to the constant current flowing through the supply rails [6]. Especially, for the clock generation, differential clock outputs can be distributed as a twisted pair which magnetically decoupled to adjacent signal lines. Furthermore, low-swing differential clock trees are seen to have 25-42 $\%$ less sensitivity to power supply noise and 6% less sensitivity to manufacturing variation than single ended clock trees [4]

If we are allowed to implement some feedback tricks to the circuits, there are several stabilization schemes to look into. Replica Bias Circuit proposed by [7] stabilized operating frequency of a processor over corner cases of devices, supply voltage, and temperature by controlling current source of MCML with PLL [8]. Recently, [9] showed that MCML can dynamically control PVT variation in 0.5-GHz to 2.5-GHz frequency-range. The on-going researches are targeting MCML functioning in the active region, and MCML operating in sub-threshold region has not yet been fully explored. A paper by Canillo and Toumazou [6] is the first one which discusses subthreshold MCML. However, no further research results have been reported since then. This research first time investigates sub-Vth MCML in an application.

In this paper, we first explore the nature of sub-threshold MOS current mode logic (Sub-Vth

MCML) to show necessary voltage swing, logic structure, and bias circuitries for safe logic operation over PVT variation. Together with dynamical control by Replica Bias Circuit, this static control guarantees safe operation of sub-Vth MCML.

As a part of UWB project, ultra low power clock generation was attempted, and 2G-Hz ring oscillators with 1.25V, 10uA power consumption was fabricated in 90 nm process. A study on the coupling phenomena of oscillators stemmed from phase noise study of oscillators, and added at the end of this research.

2 Sub-threshold MOS Current Model Logic

2.1 CMOS Characteristics in Subthreshold Region

The MOS in sub-threshold region is known to follow exponential law like a bipolar transistor does [6];

$$I_{sub} = I_o \cdot e^{\frac{|V_{gs}|}{nV_t}} \cdot e^{\eta\frac{|V_{ds}|}{nV_t}}(1 - e^{\frac{|V_{ds}|}{V_t}}) \tag{1}$$

where,

$$I_o = \mu\frac{W_n}{L_n}(\frac{kT}{q})^2 \tag{2}$$

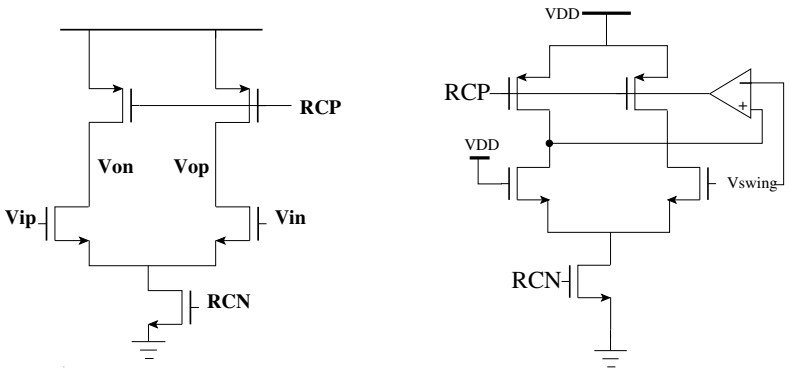
$$n = 1 + \frac{C_d}{C_{ox}} \tag{3}$$

η = DIBL Coefficient

Due to the exponential nature of (1), this operational region needs to be carefully used. From this equation, we can also notice that temperature, V_t, and aspect ratio $\frac{W_n}{L_n}$ should be considered as main variation and mismatch factors. As explained in the following section, NMOS differential pair in sub-Vth MCML needs to be designed to stay in this region throughout the entire logic operation.

2.2 Design of Sub-threshold MOS Current Mode Logic

MCML is structured as a differential pair as shown in Fig.5.6.2. This is current steering type of logic: when one input voltage is higher than the other, whole current drawn by the bottom current source goes through that branch, and the other branch does not conduct any current. Therefore, high state of the logic is VDD, and low state is $VDD - Vswing$. In sub-threshold MCML, the NMOS differential pair is designed to operate in sub-threshold region, and the bottom NMOS current source is in saturation region. The operation region of PMOS load depends on the amount of source current required. Since sub-threshold region of CMOS resembles that of Bipolar, MCML operating in sub-threshold region is somewhat analogous to Emitter Coupled Logic (ECL) of Bipolar technology which is pretty mature technique and has been used in high-speed logic for almost three decade. The PMOS load is equivalent to a resistance which has impedance of $Rp = \Delta V_{in,max}/I_{ss}$. We control the resistivity of the PMOS load with a *Replica Bias Circuit*,



(a) MOS Current Mode Logic (MCML)

(b) Replica Bias Circuit

Figure 1: MCML

Fig.1(b), as proposed in [7]. In order to keep parasitic capacitance at the output as small as possible, the size of PMOS load is sized to be minimum which is good in terms of PDP metric.
One difference between MCML operating in strong inversion and sub-threshold region is that sub-threshold MCML has constant switching threshold voltage defined by thermal voltage $V_t = kT/q$ from the same mechanism as bipolar Emitter Coupled Logic, ECL, where n is the slope factor defined in (3).

$$\Delta V_{in} \geq 3nV_t = 117mV \quad (n \approx 1.5) \tag{4}$$

In contrast, the switching threshold voltage of strong inversion MCML is defined by the over-drive voltage, Vdsat, and it requires more care to maintain proper input signal level.

$$\Delta V_{in} \geq V_{dsat} = \sqrt{\frac{2I_{ss}}{k(W/L)}} \tag{5}$$

The bias point and sizing of devices are decided by the following condition, and the sizing of devices is shown in Table 1;

1 : Input Voltage Swing: $\Delta V_{in,min} = 200mV$ from (4)
2 : Current Source: $I_{ss} = 1uA$ for 2GHz oscillation for 3-stage ring oscillator

PMOS Load	NMOS Differential Pair	NMOS Current Source
$0.1/0.12$	$0.1/0.12$	$1.4/6.5$

Table 1: Size of device $[um/um]$ in 90nm CMOS Process

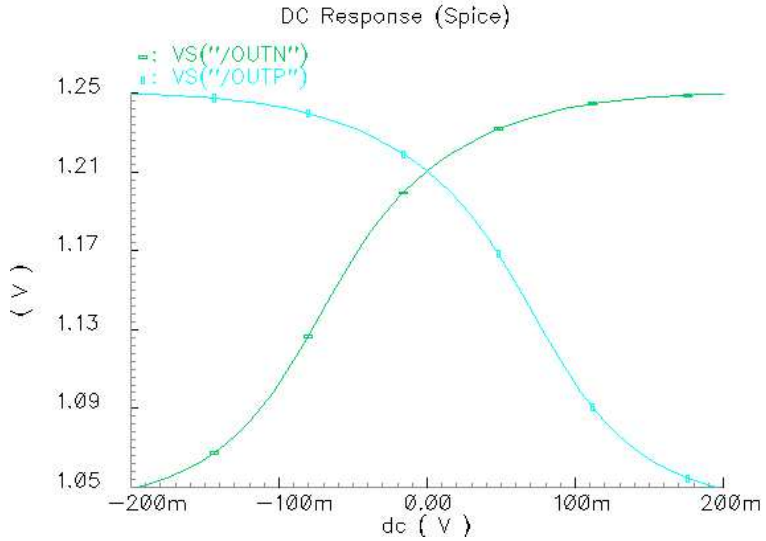


Figure 2: DC Response of MCML

Input-Output response of the sub-Vth MCML is plotted by HSPICE in Fig.2. We have found this response is not symmetric in output magnitude wise which is different from CMOS inverter response. The reason of this asymmetry will be explained in the subsection 2.5

The maximum speed is the main concern when sub-Vth MCML is used in clock generation circuits. In order to verify the maximum speed of operation, We can check AC simulation. A setting of simulation can go like this;

1: Set input signal magnitude as 200mV, since we have to maintain the output swing to be over 117mV in the operation frequency.
2: Put appropriate loading, for example FO4 loading.
3: Do AC analysis on the assumption that small input and output swing of MCML can be regarded as small signal.
4: Seek for upper limit which is the frequency where the gain drops to unity on the assumption that there's next stage.

In this setting, the maximum frequency is extracted as around 1GHz from Fig.3. In order to achieve 2-GHz oscillation frequency, we need to put two current sources in parallel at the tail current source.

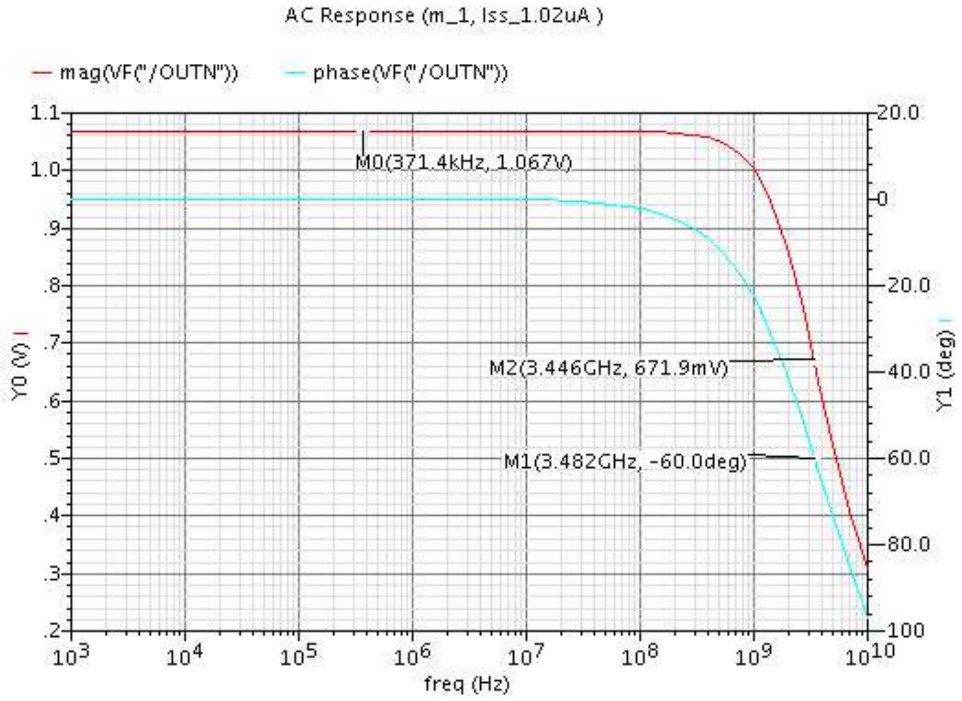


Figure 3: AC Response of MCML

2.3 Delay Energy Metric of MCML vs CMOS Static Logic

We are now going to discuss delay and power scenario. Delay, Power, and Power Delay Product of MCML are known to have dependency on VDD, output device size, and source current [10];

$$D_{MCML} = N \cdot R \cdot C = \frac{N \cdot C \cdot \Delta V}{I} \tag{6}$$

$$P_{MCML} = N \cdot I \cdot VDD \tag{7}$$

$$E_{MCML} = N^2 \cdot C \cdot \Delta V \cdot VDD \tag{8}$$

$$PD_{MCML} = N \cdot I \cdot VDD \cdot \frac{N \cdot C \cdot \Delta V}{I} = N^2 \cdot C \cdot VDD \cdot \Delta V \tag{9}$$

$$ED_{MCML} = \frac{N^3 \cdot C^2 \cdot VDD \cdot \Delta V^2}{I} \tag{10}$$

,where N is the number of the stages in the critical path, ΔV is the output voltage swing, C is the total output capacitance, and I is the bias current. In contrast, those of CMOS static logic depends also on Vth, and therefore there is an optimal VDD and Vth combination exists [11];

$$D_{CMOS} = \frac{N \cdot C \cdot VDD}{\frac{k}{2}(VDD - Vth)^{\alpha}} \tag{11}$$

$$P_{CMOS} = N \cdot C \cdot VDD^2 \cdot \frac{1}{D_{CMOS}} \tag{12}$$

$$PD_{CMOS} = N \cdot C \cdot VDD^2 \tag{13}$$

$$ED_{CMOS} = \frac{N^2 \cdot 2 \cdot C^2 \cdot VDD^2}{k(VDD - Vth)^{\alpha}} \tag{14}$$

where α is defined as the ratio of wiring plus junction capacitances, C_p, to the input capacitance of the gate, C_{ref}, and K represents terms independent of device width and voltage. Simulation gives EDP's of CMOS inverter and sub-Vth MCML as in Fig. 4.

The dependency of VDD is as predicted by the model in Eq. (6) - (14), and the crossing point of two curves is approximately around 0.6V.

Now, we are interested in the quantitative value of the crossing section of two curves. When we plot EDP for both cases for different value of α, we will find an interesting fact on MCML. The following is the EDP for $\alpha = 0.6$ (Fig. 5(a)) and 1.5 (Fig. 5(b)). (Dashed line : Sub-Vth MCML, solid line : CMOS Inverter) The physical meaning of α is the factor showing the short channel effect

$$Id \propto (V_{gs} - V_{th})^{1/\alpha} (\alpha \leq 2) \tag{15}$$

In the modern processes, α is estimated to be less than one, and Fig.5(a) shows that case. Recently Heydari [5] showed MCML in active region has better EDP in higher frequency region, and this is pointing at the upper crossing point of Fig. 5(a). When we also shift our eyes to the lower VDD side, we find that there is another crossing point which indicates that MCML has superior EDP

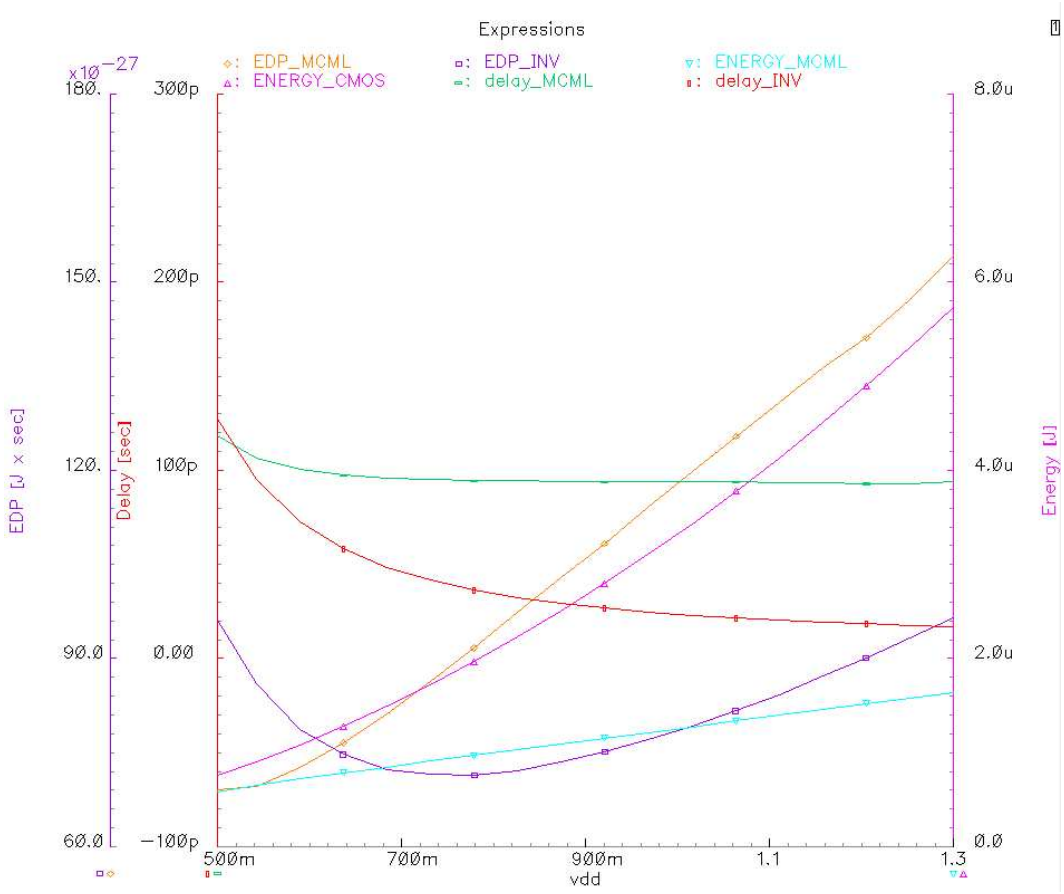


Figure 4: Energy Delay Product (EDP) of MCML vs Static CMOS (FO4)

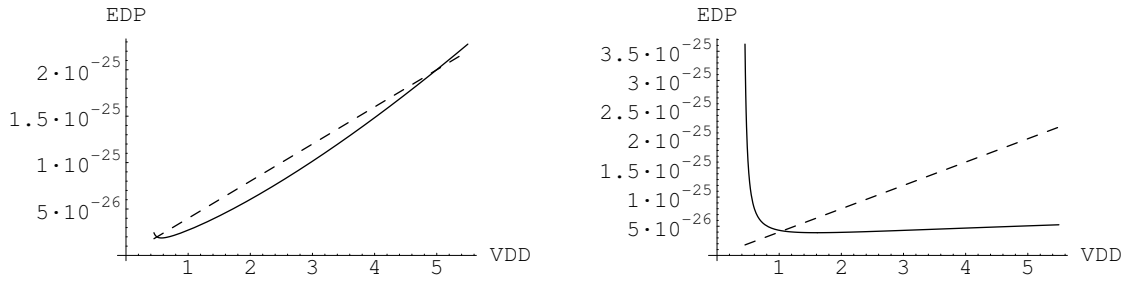
when the VDD goes down. At this point, the counterpart CMOS inverter slows down enough, and MCML is more advantageous.

Now we try to estimate where the lower crossing point will be. By equating Eq.(14) and Eq.(10), we get

$$VDD - V_{th} = (\frac{2 \cdot I \cdot VDD}{K})^{1/\alpha} \approx \Delta \tag{16}$$

when we assume reasonable values of $I = 1uA, VDD < 1V, K = 100u$.

This result ultimately concludes the same fact as what g_m/I_d curve of CMOS transistor is showing; g_m/I_d curve is the metric of power-speed efficiency, and it hits the maximum point at sub-threshold region. In our calculation, VDD lower than V_{th} is more or less the region where MCML is more efficient than CMOS static logic, and in this situation, MCML falls on the category of sub-Vth MCML. Thus, from the two cases of α, we can conclude that using MCML for low frequency usage is advantageous over CMOS static logic either it is operating in short channel or long channel model. This can be understood intuitively. Since MCML flips its logic state immediately after there is slight difference between two inputs, it is astable logic. Astable logic is analogous to seesaw. A quite subtle change in the weight balance brings the system to the opposite state. The power to cause this sudden change is ”current” in MCML. Sub-Vth MCML is using ”leakage current”



(a) $\alpha = 0.6$ (b) $\alpha = 1.5$

Figure 5: EDP of CMOS Inverter and Sub-Vth MCML

to cause this change, and therefore it is never wasting even leakage current. Thus, this sub-Vth MCML takes the advantage of recent leaky process, and can realize power efficient logic in middle to low frequency operation.

2.4 Delay of Cascaded Logic of Sub-Vth MCML

Next, we would like to discuss the cascaded effect on Sub-Vth MCML. The delay of MCML is modeled as RC delay model exactly same as Static CMOS logics where R is controlled by the replica bias circuit, and C is parasitic capacitance in the output nodes. Therefore, we can use same technique to control delay such as "Logical Effort" or "Elmore delay model".

Delay is expected to decrease by controlling back gate voltage. Back gate plays a role as the second gate and it basically helps to increase the gm of a transistor. Another current model of sub-threshold transistor is shown and it includes the factor of V_{bs} as a gate.

$$I_{sub} = \frac{W}{L}\left(\frac{kT}{q}\right)^2 e^{\frac{(1-n)V_{bs}}{U_t}} e^{\frac{nV_{gs}}{U_t}} \left(1 - e^{\frac{|V_{ds}|}{U_t}}\right) \tag{17}$$

Eventually, [12] proved that a transistor whose back gate is connected to the gate of itself has smaller delay than normal topology on the condition that triple well process is available. It means that increase in current drive overweights the increase in gate capacitance. However, we cannot expect this benefit from Vbs in the generic sub-threshold MCML logics because there will be multi layered parasitic capacitance in more complex logics.

2.5 Generic DC Input-Output Model

The DC characteristic of MCML in sub-threshold region has not been modeled in the literature. In order to analyze process variation and mismatch effect on the logic, the model for both NMOS differential pair and PMOS loading are indispensable. In this section, we will show a model which is precise enough to determine the design specification and simple enough to grasp the phenomena intuitively.

Due to the differential nature of MCML, the summation of current from two branches is constant ;

$$I1 + I2 = I_{ss}(Const) \tag{18}$$

Here, we propose a resistance model of PMOS loading as a variable resistance, and the input-output expression is going to be derived from this resistance model and the current equations, Eq.(3) and Eq.(18). The following is the proposed resistance model which nearly depends on voltage drop across a transistor;

$$R(V_{ds}) = a \cdot V_{ds} + b \tag{19}$$

In reality, $R(V_{ds})$ is not really a straight line as shown in Fig.6, however, in order to facilitate the following calculation, we assume this model for now. Ohm's law should hold for the current I_d

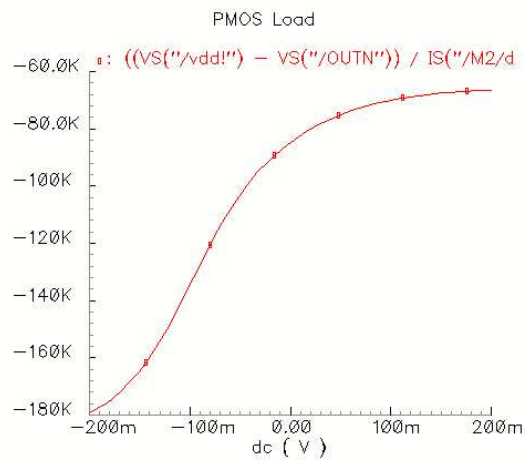


Figure 6: Impedance of PMOS Load

and voltage drop across the PMOS loading V_{ds}:

$$R(V_{ds}) = \frac{V_{ds}}{I_d} \tag{20}$$

From the above two equations, we get,

$$I_d = \frac{1}{a} - \frac{\frac{b}{a}}{a \cdot V_{ds} + b} \tag{21}$$

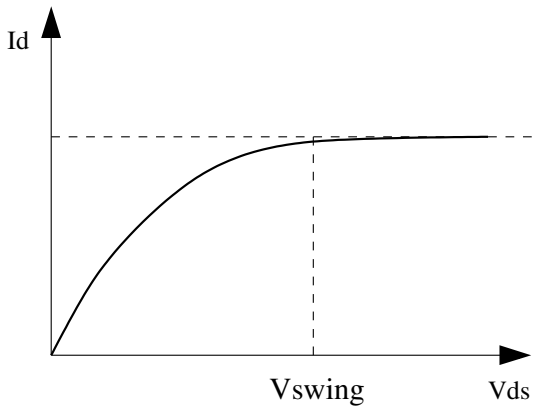


Figure 7: Id-Vds Curve of PMOS loading of MCML

We compare this equation to the real behavior of Id-Vds curve of PMOS loading depicted in Fig.7 When the output of the branch is high, $V_{ds} = 0$, and all the current drawn by the current source flows in the other branch. Therefore, I_d is zero, and this model shows that situation. On the other hand, when V_{ds} becomes sufficiently large toward low logic level, all the current drawn by the current source flows in this branch; I_d should converge into constant value I_{ss}. Thus, $1/a$ should converge to the value of current source, I_{ss}. b is interpretted as resistive value of PMOS loading when $V_{ds} = 0$. Hence, we call this b as "residue resistance".

From Eq.(1) and (21), we obtain the input-output model of sub-threshold MCML.

$$Von = VDD - \frac{b}{\frac{1}{I1} + a} \tag{22}$$

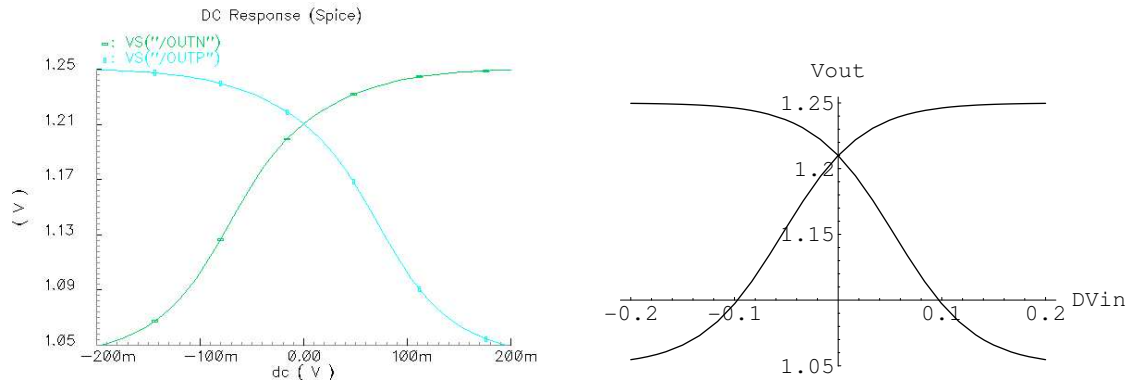
$$Vop = VDD - \frac{b}{\frac{1}{I2} + a} \tag{23}$$

where,

$$I1 = \frac{I_{ss}}{1 + e^{\frac{-2\Delta V_{in}}{nV_t}}} \tag{24}$$

$$I2 = \frac{I_{ss}}{1 + e^{\frac{+2\Delta V_{in}}{nV_t}}} \tag{25}$$

The plot of Eq.(23) and (22) are shown in Fig. 8(b), and we can verify that the proposed model is a good approximation of the HSPICE simulation result in Fig.8(a).



(a) Spice Simulation

(b) matlab model

Figure 8: Positive/Negative Input-Output Response of MCML

2.6 Input Output Model with Replica Bias Circuit

Under the condition of using Replica Bias Circuit [7],we can control voltage swing of MCML from outside of the IC. Suppose that the controlled voltage swing down to $VDD - V_{swing}$, and one of the differential nodes swing to V_{swing} when all the current from the current source I_{ss} flows only to that branch. This condition is reflected to the Eq.(21),

$$I_{ss} = \frac{1}{a} - \frac{\frac{b}{a}}{a \cdot V_{swing} + b} \tag{26}$$

and transformed to,

$$a = \frac{1}{I_{ss}} - \frac{b}{V_{swing}} \tag{27}$$

Substituting Eq. (27) to Eq.(23) and (22), the input-output response with Replica Bias Circuit turn out to be as follows;

$$V_{on} = VDD - \frac{b}{\frac{e^{\frac{-2\Delta V_{in}}{nV_t}}}{I_{ss}} + V_{swing}} \tag{28}$$

$$V_{op} = VDD - \frac{b}{\frac{e^{\frac{+2\Delta V_{in}}{nV_t}}}{I_{ss}} + V_{swing}} \tag{29}$$

The resulting differential output can be expressed with V_t, I_{ss}, and b in the end;

$$V_{od} = b \cdot I_{ss} \cdot \left(\frac{-1}{1 - a \cdot I_{ss} + e^{\frac{-2\Delta V_{in}}{nV_t}}} + \frac{-1}{1 - a \cdot I_{ss} + e^{\frac{+2\Delta V_{in}}{nV_t}}}\right) \tag{30}$$

$$= \frac{b \cdot I_{ss} \cdot {V_{swing}}^2 \cdot (-1 + e^{\frac{4\Delta V_{in}}{nV_t}})}{(be^{\frac{2\Delta V_{in}}{nV_t}} I_{ss} + V_{swing})(bI_{ss} + e^{\frac{-2\Delta V_{in}}{nV_t}} V_{swing})} \tag{31}$$

3 Robust Design Scheme for Sub-Vth MCML

In order to secure the logic operation of Sub-Vth MCML, the voltage swing V_{swing} and bias current I_{ss} play main roles. In the following chapters, first, mismatch and variation analysis determines voltage swing V_{swing}, and subsequently, a new current reference circuit is proposed to stabilize I_{ss} over voltage and temperature variation.

3.1 Variation and Mismatch

Process variation is categorized into two types in differential mode logic. One is the common mode variation which is referred as "variation"; the other is the differential mode variation which is called "mismatch" in this paper. Due to the exponential nature of subthreshold operation, process variation and device mismatch are to be carefully concerned in sub-Vth MCML. Thanks to the common mode nature of MCML, variation of power supply VDD does not come into play. Variation and mismatch will be analyzed separately.

In this section, we are going to mathematically analyze variation and mismatch contribution with Mathematica, and these results will be compared to the circuit simulation results by Spectre including Monte Carlo simulation.

3.1.1 Variation Effect

The variation effect of differential output Eq.(30) is evaluated as its derivatives on b, I_{ss}, and V_t.

Variation Effect by b

$$\frac{\Delta Vod}{\Delta b} = -\frac{e^{\frac{2\Delta Vin}{nV_t}} \cdot (-1 + e^{\frac{4\Delta Vin}{nV_t}}) I_{ss} {V_{swing}}^2 \dot{(} b^2 I_{ss}^2 - V_{swing}^2)}{(be^{\frac{2\Delta Vin}{nV_t}} I_{ss} + V_{swing})^2 \dot{(} bI_{ss} + e^{\frac{2\Delta Vin}{nV_t}} V_{swing})^2} \tag{32}$$

Variation Effect by I_{ss}

$$\frac{\Delta Vod}{\Delta I_{ss}} = -\frac{b \cdot e^{\frac{2\Delta Vin}{nV_t}} \cdot (-1 + e^{\frac{4\Delta Vin}{nV_t}}) {V_{swing}}^2 (b^2 I_{ss}^2 - V_{swing}^2)}{(be^{\frac{2\Delta Vin}{nV_t}} I_{ss} + V_{swing})^2 \cdot (bI_{ss} + e^{\frac{2\Delta Vin}{nV_t}} V_{swing})^2} \tag{33}$$

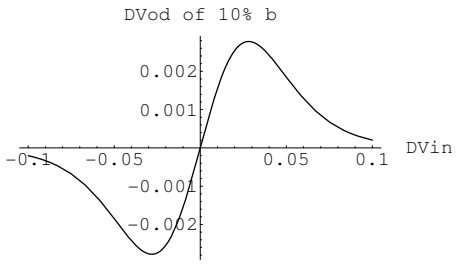
Variation Effect by Vt

$$\frac{\Delta Vod}{\Delta Vt} = -\frac{2be^{\frac{2\Delta Vin}{nV_t}} \cdot I_{ss} V_{swing}^2 (b^2 I_{ss}^2 \cdot (1 + e^{\frac{4\Delta Vin}{nV_t}}) + 4be^{\frac{2\Delta Vin}{nV_t}} I_{ss} V_{swing} + (1 + e^{\frac{4\Delta Vin}{nV_t}}) V_{swing}^2) \Delta V_{in}}{nV_t^2 (be^{\frac{2\Delta Vin}{nV_t}} I_{ss} + V_{swing})^2 \cdot (bI_{ss} + e^{\frac{2\Delta Vin}{nV_t}} V_{swing})^2} \tag{34}$$

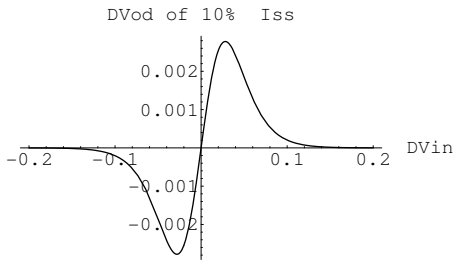
Variation Effect by V_{swing}

$$\frac{\Delta Vod}{\Delta V_{swing}} = \frac{b^2 * (-1 + \frac{4\Delta Vin}{nV_t}) I_{ss}^2 V_{swing} (2b\frac{2\Delta Vin}{nV_t} I_{ss} + V_{swing} + \frac{4\Delta Vin}{nV_t} V_{swing})}{(b\frac{2\Delta Vin}{nV_t} I_{ss} + V_{swing})^2 (bI_{ss} + \frac{2\Delta Vin}{nV_t} V_{swing})^2} \tag{35}$$

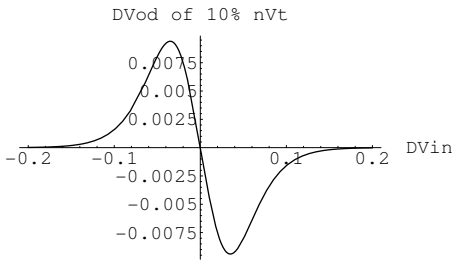
Based on these model equations, now we can plot the variation of output voltage V_{od} with maximum 10% variation from each factors, namely $b, I_{ss}, V_t, V_{swing}$.



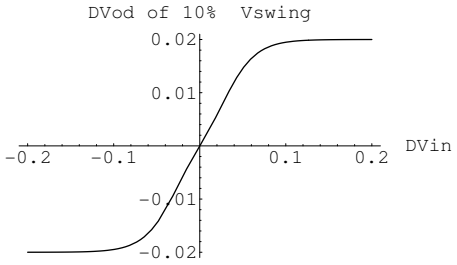
(a) ΔV_{od} with 10% b Variation



(b) ΔV_{od} with 10% Iss Variation



(c) ΔV_{od} with 10% Vt Variation



(d) ΔV_{od} with 10% Vswing Variation

Figure 9: Variation Effect for Each Factor

What we can clearly see from these plots in Fig.3.1.1 is the effect of V_{swing} is the dominant factor in variation effect which changes maximum voltage swing. This variation stems from not only

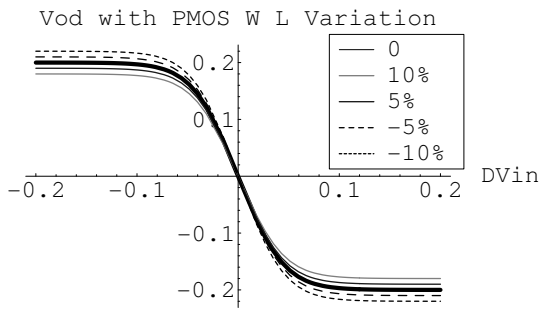
the size variation of PMOS loading, but also from the variation from strength of feedback loop of Replica Bias Circuit.The other factors produce the gain difference in switching activity, but the data is showing that their influence is quite subtle.
The worst case situation can be realized by summing the previously derived variation effects toward the same polarity.

$$V_{od}|_{with_all_variations} = \Delta I_{ss}\frac{\Delta V_{od}}{\Delta I_{ss}} + \Delta V_t\frac{\Delta V_{od}}{\Delta V_t} + \Delta b\frac{\Delta V_{od}}{\Delta b} + \Delta b\frac{\Delta V_{od}}{\Delta V_{swing}} \tag{36}$$

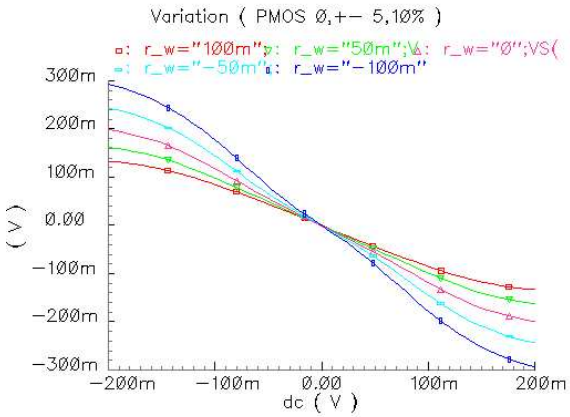
The worst case input-output responses with $\pm 0, 5, 10\%$ variation of b, I_{ss},V_t are shown to be compared to the circuit simulation result by Spectre. In this comparison, W/L variation of PMOS is assumed to reciprocal to the b and also V_{swing}. i.e. In order to express $+10\%$ variation of W/L in schematics, we set $b : -10\%, V_{swing} : -10\%$. On the other hand, W/L variation of NMOS is proportional to I_{ss}. On top of I_{ss} variation, V_t variation which has opposite polarity of W/L variation has been added in Mathematica simulation to emphasize the worst effect of variation from NMOS differential pair.

In this process, overall tendency caused by the variation of NMOS differential pair and PMOS loading is similar: Variation of PMOS loading causes significant voltage swing variation in the output. However, the model calculated by Mathematica has four times less influence on voltage swing than one by Spectre, which shows that linear impedance model of PMOS load is not good enough. We have examined this model in another process, and in that process this mathematical model showed good matching to simulation model. Due to the immaturity of sub-threshold model in Spectre simulation, we may have seen this discrepancy from a process to the other.
Though one can come up with the solution of increasing the size of PMOS loading in order to suppress the variation effect of PMOS loading, increasing size of PMOS loading will cause increase the capacitive loading of MCML. In this sub-threshold MCML, loading effect has a great influence to slow down the logic, and sizing is not a good solution. Considering the fact that we have Replica Bias Circuit to control the voltage swing, the simple and best solution renders itself to set up the voltage swing with enough margin.

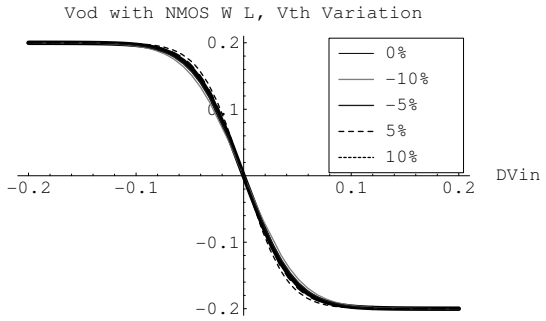
From Fig.3.1.1, we can conclude that $\pm 10\%$ variation of critical parameters do not bring detrimental effect on MCML if we put enough margin to the voltage swing controlled by Replica Bias Circuit. From the data of Spectre, the worst case voltage swing is about half of the center value, and therefore, the appropriate voltage swing given to the Replica Bias Circuit should be double the nVt which is around 400mV. Shortly, we will be led to the same conclusion from the result of



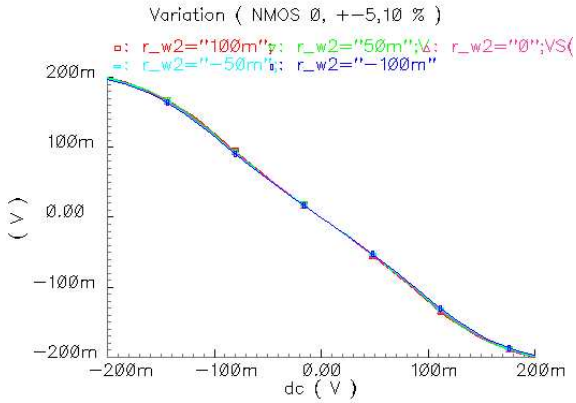
(a) Variation Effect from PMOS (M)



(b) Variation Effect from PMOS (S)



(c) Variation Effect from NMOS (M)



(d) Variation Effect from NMOS (S)

Figure 10: Variation Effect Analysis by Mathematica and Spectre

Monte Carlo simulation.

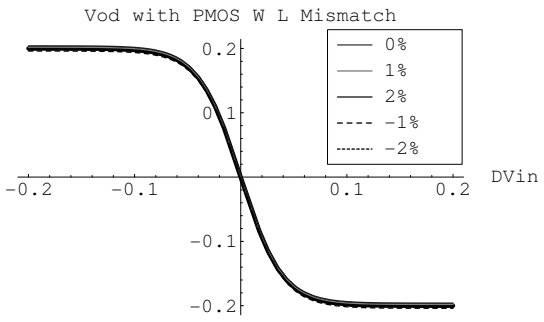
3.1.2 Mismatch Effect

Mismatch effects from PMOS loading and NMOS differential pair are going to be studied in this section. From the same mechanism as in the variation analysis, mismatch of PMOS loading is characterized with b and V_{swing}, whereas one of NMOS differential pair is with I_{ss} and V_t. Mismatch appears as offset of zero-crossing point of differential ouput of an MCML. The critical situation occurs when this mismatch is too large, and the differential outputs remain in the same level even if $\Delta Vin \neq 0$ The mismatch effect estimated by the proposed model is plotted by Mathematica, and compared to the schematic simulation by Spectre. The differential output voltage with

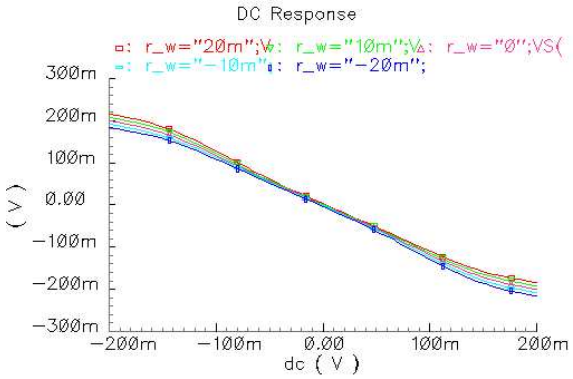
mismatch is calculated as (23) minus (22), and reduced to the following expression ;

$$V_{os} = -\frac{b1}{\frac{e^{-\frac{2\Delta V_{in}}{nV_{t1}}}}{I_{ss1}} + \frac{b_1}{V_{swing1}}} + \frac{b_2 \cdot I_{ss2} \cdot V_{swing2}}{b_2 \cdot I_{ss2} + e^{\frac{2\Delta V_{in}}{nV_{t2}}} V_{swing2}} \tag{37}$$

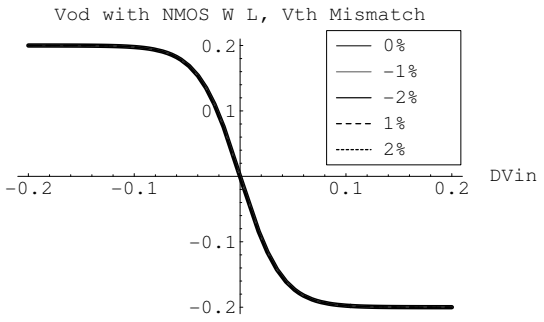
The worst settings of four parameters for NMOS and PMOS are substituted to the (37) and compared to the schematic simulation:



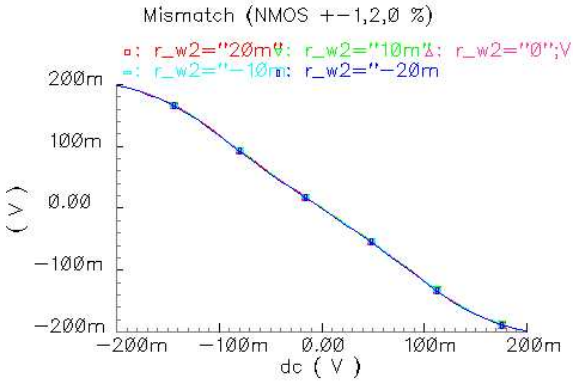
(a) Mismatch Effect from PMOS (M)



(b) Mismatch Effect from PMOS (S)



(c) Mismatch Effect from NMOS (M)



(d) Mismatch Effect from NMOS (S)

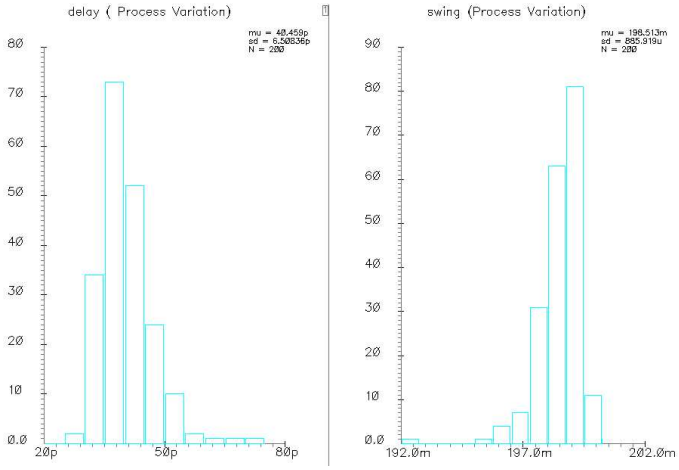
Figure 11: Mismatch Effect Analysis by Mathematica and Spectre

From these data, we can conclude that the proposed model is well expressing the mismatching effect of the real circuit, and the mismatch of maximum 2% does not produce significant effect on the MCML operation.

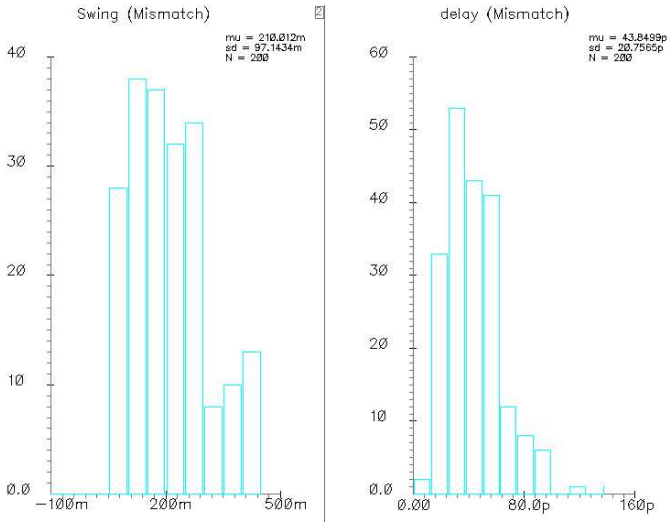
3.1.3 Monte Carlo Simulation of Delay and Swing

In order to grasp statistical data of mismatch and variation effect, Monte Carlo simulation has been attempted. The test-bench is including MCML buffer, Replica Bias Circuit, and Current Bias Circuit which is going to be explained in the following section. The datum observed were output voltage swing and delay. Delay is directly corresponded to the process variation of oscillation frequency of ring oscillator discussed in the later sections.

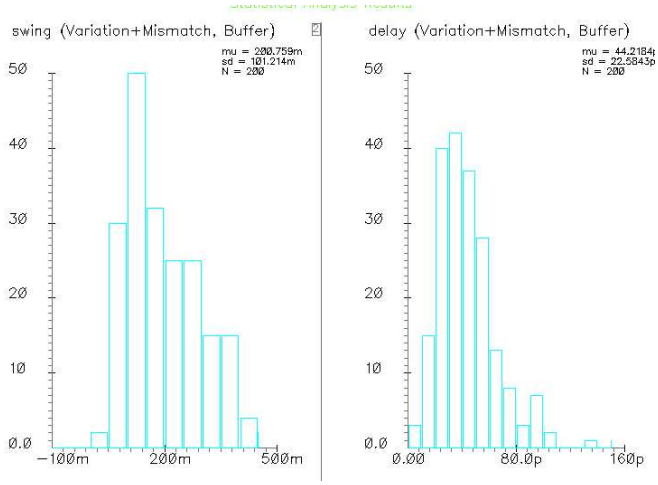
Variation [Fig.12(a)]
Variation does not have as much as influence on swing compared to what we have seen in the Spectre simulation in the previous chapter. This is because this Monte Carlo simulation is including the replica bias circuit. As far as feedback function is working, swing is controlled to be the reference swing value. Whereas, the delay is influenced by variation with 16% standard deviation since the bias current, which is proportional to the speed, changes with variation of devices. This variation is expected to be mended by post-process resistor trimming.
Mismatch [Fig.12(b)]
Mismatch simulation result from Monte Carlo simulation seems to be problematic compared to the good result from Spectre simulation in the previous section. The reason is, Monte Carlo simulation includes mismatch in the all circuits whereas the previous mismatch simulation only include mismatches in a buffer. Swing has 50% standard deviation, and it is necessary to set the voltage swing to be double. Delay can be rescued by post-preocess resistor trimming from the same argument in variation.
Mismatch + Variation [Fig.12(c)]
The last graph is showing the result where the circuit experiences both mismatch and variation, and it shows almost same result as in mismatch. Therefore, we can say that under the feedback function of replica bias circuit, variation effect is suppressed, and mismatch is going to be a critical factor in MCML. However, setting voltage swing with enough margin and post-process resistor trimming to control bias current will greatly enhance yielding.



(a) Variation



(b) Mismatch



(c) Variation + Mismatch

Figure 12: Monte Carlo Simulation Result

3.2 Robustness to VDD and Temperature Variation

We now switch our focus to the dynamic control scheme of the sub-Vth MCML.
In the current mode logic, reference current I_{ss} is one of the main factors to decide one stage delay from (6), which is different from the case of CMOS static logic whose delay is decided by VDD (11). Once we can obtain robust I_{ss}, then the voltage swing of MCML is dynamically controlled by Replica Bias Circuit [7]. Thus, reference current generation is the key to the success in this research. Robustness to the external environment, especially voltage supply fluctuation and temperature change, is critical characteristic for integrated circuits. MCML operates based on the source current, I_{ss}, which controlled by the gate voltage of current source. There are two schemes for robust clock generation in MCML circuits. In the case where the frequency is supposed to lock to a reference signal, negative feedback structure of PLL will force the loop to be locked to the reference signal disregarding PVT variation factors in the circuit itself. However, in the other case where the MCML circuit is to generate a reference clock frequency, stabilizing current source I_{ss} over PVT variation is required. In this section, we propose a current bias circuit which can minimize the effect of voltage supply and temperature variation while keeping power consumption as low as 10uA and voltage supply as 1.25V.

3.2.1 Supply Voltage and Process

It is well-known scenario that as CMOS process shrinks, voltage supply lowers down. The conventional regulation technique of supply voltage is band-gap reference circuitry which uses V_{be} of Bipolor device. In band-gap reference circuit, V_{be} stays around 0.7 V over process to process, and it is not simple to implement this circuit for sub-1V voltage supply. As a natural fit to the sub-1V voltage supply, sub-Vth CMOS reference circuit has emerged. Recently, several methods to produce sub-1V voltage supply have been published as in the Table.2 shows. As proposed in

Ref	Publication	VDD[V]	Power[A]	Tempco [ppm/deg]	Line Reg[ppm/V]
[13]	ISCAS ‘97	0.9	42u	120	571K
[14]	JSSC ‘03	1	3.6u	50	38K
[15]	JSSC ‘97	1.2	100n	$T^{0.4}$	100K
[16]	ISCAS ’04	1	100u	1.3K	100K
[17]	JSSC ‘03	0.9	5u	3K	NA

Table 2: Sub-1V Current Reference Circuits

[9], the ring oscillator consisting of CMOS inverters can secure PVT variation robust signal since the frequency of this type of ring oscillator is proportional to the rail to rail voltage amount. However, the output reference voltage of reference bias circuit goes down to almost half of the original supply voltage, and the oscillation frequency is constrained by this reference voltage. On the other hand, the speed of the ring oscillator structured with MCML does not depend on the supply voltage VDD but on the current source I_{ss}. If there is a current reference circuit which works sub-1V voltage supply, MCML has possibility to easily generate robust clock signal under sub-1V VDD. In the modern process, one stage delay of static CMOS logic has seen dramatical changes with both temperature and voltage supply variation. Table 3 is showing the influence of temperature and voltage supply variation on one buffer stage delay for two different voltage supply in a 90 nm process. As the voltage supply lowers, influence of PVT variation becomes more and more significant, and it is necessary to compensate both environmental factors in real time. In this section, we propose an ultra low power current reference circuit with function of temperature and voltage supply rejection.

VDD	Δ VDD	Δ td	Δ temp	Δ td
1.0	$\pm$ 10%	$\pm$ 10 %	-40$\rightleftharpoons$ 85	$\pm$8%
0.5	$\pm$10%	$\pm$25%	-40$\rightleftharpoons$ 85	$\pm$ 39%

Table 3: VDD, Temp Variation Influence on Inverter Delay for VDD=0.5-V and 1-V

3.2.2 Current Bias Circuit

We proposed the current reference circuit shown in the fig. 13 to produce the controlled gate voltage RCN to MCML circuits. We now derive the temperature and VDD dependence of the propose current reference circuit in the following subsections.

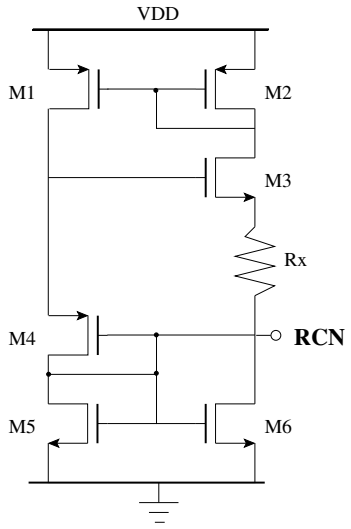


Figure 13: Current Reference Circuit

Temperature Dependence of Current Bias Circuit

The sub-threshold voltage of CMOS has temperature dependency as shown in Fig.14.

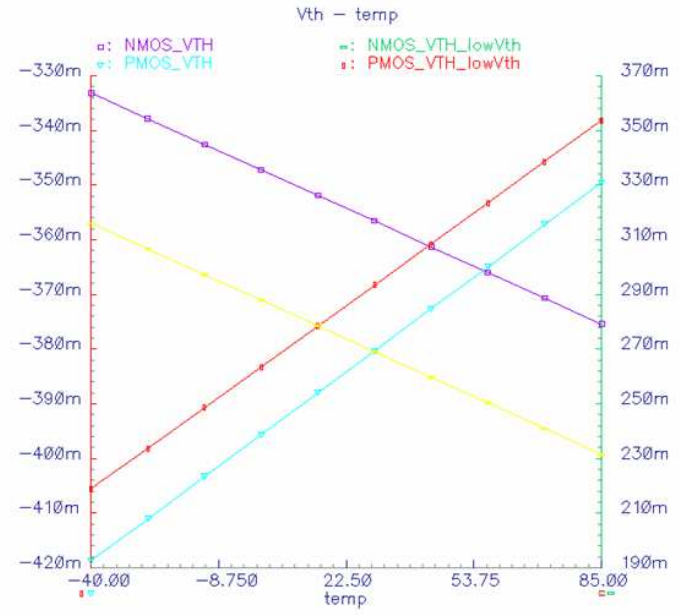


Figure 14: CMOS Vth Temperature Dependency

If we can generate the difference of NMOS and PMOS Vth's, and its temperature dependence looks like as in Fig. 15.

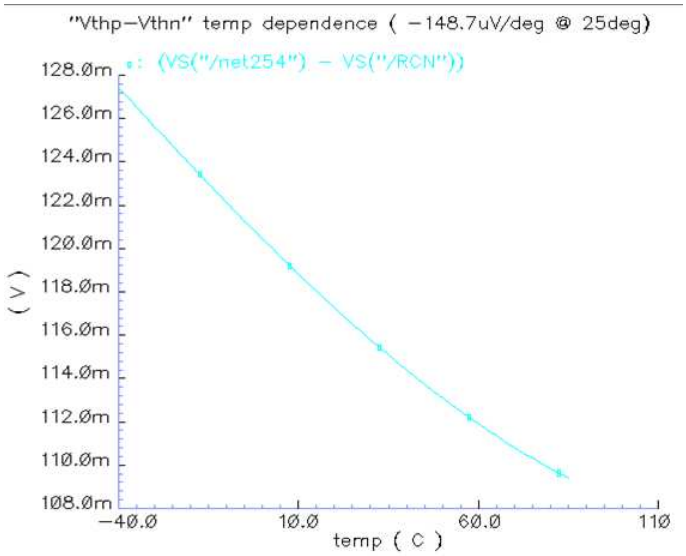


Figure 15: CMOS Vth difference of Temperature Dependency

The circuit in Fig.13 brings the difference between threshold voltage of NMOS and one of PMOS, $V_R = |Vthp| - Vthn$, across the resistor Rx under the condition that two horizontal current paths have same amount of current when the condition in (38) is satisfied.

$$\mu_n \frac{W_{n3}}{L_{n3}} = \mu_p \frac{W_{p4}}{L_{p4}} \tag{38}$$

The value of this voltage drop is constant in DC with negative temperature dependence. Therefore, if we can prepare appropriate resistance with negative temperature dependence, then the current going through this resistance become more or less temperature independent. Desired temperature dependence across the resistance Rx can be derived from Ohm's law (20);

$$\Delta I = \frac{\delta I}{\delta V}\frac{\delta V}{\delta T}\Delta T + \frac{\delta I}{\delta R}\frac{\delta R}{\delta T}\Delta T \tag{39}$$

$$= \frac{1}{R}\frac{\delta V}{\delta T}\Delta T + \frac{-1}{R^2}\frac{\delta R}{\delta T}\Delta T \tag{40}$$

In order to nullify the temperature dependence of current,

$$\frac{\delta I}{\delta T} = \frac{1}{R}\left(\frac{\delta V}{\delta T} - \frac{V}{R}\frac{\delta R}{\delta T}\right)\Delta T = 0 \tag{41}$$

Thus, the required temperature dependence of the resistor Rx is,

$$\frac{\delta R}{\delta T} = \frac{1}{I}\frac{\delta V}{\delta T} \tag{42}$$

In the process available, Vth of PMOS and NMOS have the following characteristics in Table 4; The delay condition for the three stage ring oscillator of 2GHz oscillation requires $I = 2uA$ and

	Vth[V]	tempco [V/deg]
PMOS	-369.6m	539.1u
NMOS	270.8m	-676.4u

Table 4: Vth characteristic of CMOS

Rx is decided according to I.

$$V_R = |Vthp| - Vthn = 0.1V \tag{43}$$

$$R_x = \frac{V_R}{I} = 100KOhm \tag{44}$$

The require temperature coefficient is calculated as follows from (42),

$$\frac{\Delta V_R}{\Delta T} = \frac{\Delta Vthp}{\Delta T} - \frac{\Delta Vthn}{\Delta T} \tag{45}$$

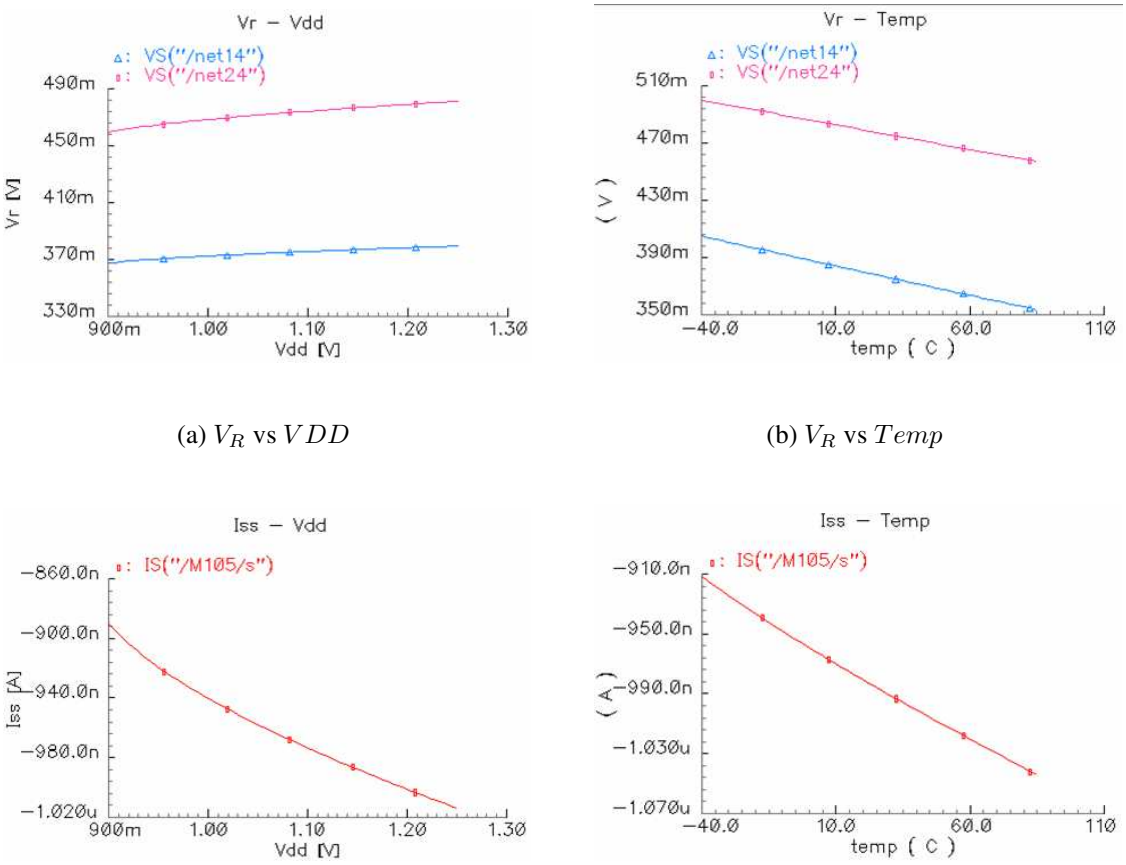
$$= (-676.4u) - 539.1u = -137.7u[V/deg] \tag{46}$$

$$\frac{\Delta R}{\Delta T} = \frac{\Delta V_R}{\Delta T}/I = -137.7uV/1uA = -137.7[Ohm/deg] \tag{47}$$

Unfortunately, we could achieve only 14% of cancellation in the available resistors. Unsicillicide P+ poly resistor has negative temperature coefficient, but because R_x needs to suffice (44), it can not perfectly suffice (47) at the same time.

Simulation Results of Current Bias Circuit

Fig.16 are the simulation results of the current reference circuit with VDD and Temperature swept.



(a) V_R vs VDD

(b) V_R vs $Temp$

(c) I_{ss} vs VDD

(d) I_{ss} vs $Temp$

Figure 16: DC Simulation of Current Reference Circuit

Numerical result from the Fig.16 is summarized in Table 5.

Temp	-40 85 $C°$	Iss	$\pm 6.7\%$	1.072K ppm/deg
VDD	$\pm 10\%$	Iss	$\pm 2\%$	160K ppm/V

Table 5: Iss with Temp, VDD variation

When we put this result to the previous works, the work by [14] is superior to ours. However, the simplicity of our circuit might be still attractive to a certain application.

Ref	Publication	VDD[V]	Power[A]	Tempco [ppm/deg]	Line Reg[ppm/V]
[13]	ISCAS '97	0.9	42u	120	571K
[14]	JSSC '03	1	3.6u	50	38K
[15]	JSSC '97	1.2	100n	$T^{0.4}$	100K
[16]	ISCAS '04	1	100u	1.3K	100K
[17]	JSSC '03	0.9	5u	3K	NA
$\diamond$	this work	1.25	2u	1K	160K

Table 6: Sub-1V Current Reference Circuits

These variation on I_{ss} is proportionally reflected to frequency of three stage ring oscillators which will be mentioned in the next subsection 4.1.1. Due to the lack of appropriate resistor device, we cannot show the effectiveness of this method in the simulation in terms of temperature robustness. Still this current reference circuit suppresses VDD variation effect on current value I_{ss} with low power consumption.

3.3 Monte Carlo Simulation Result

Monte Carlo simulation has been done to estimate the distribution of constant current value. The result below is showing that mean value is $1.006uA$ with standard deviation of $172nA(17\%)$.If we neglecting the temperature dependence cancellation, we can enhance its yielding by trimming the resistor R_x.

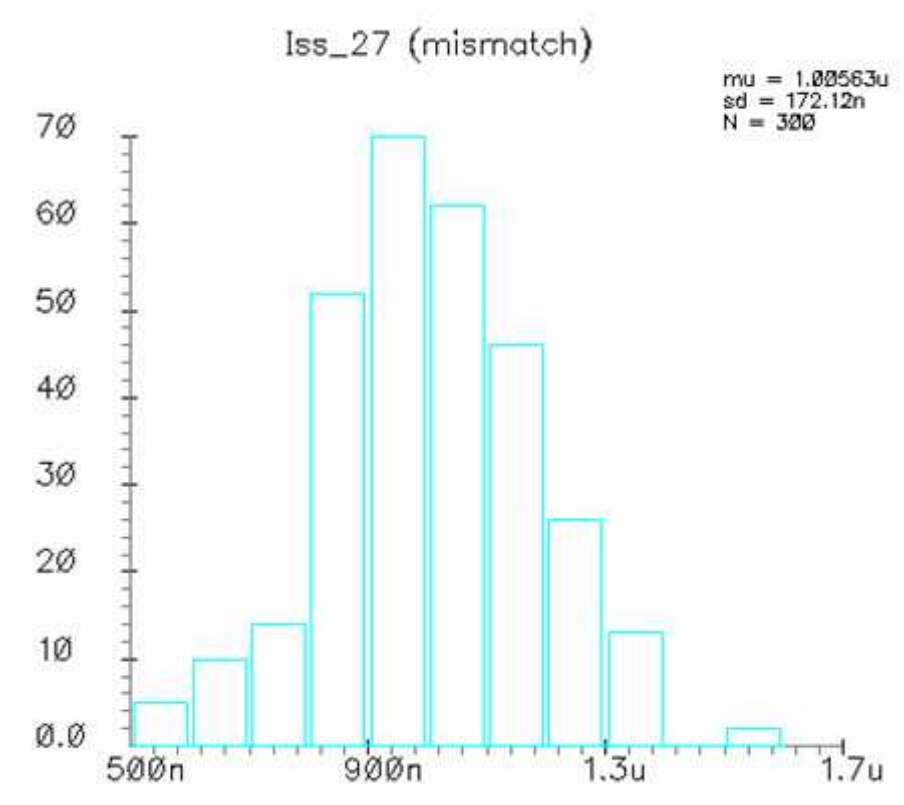
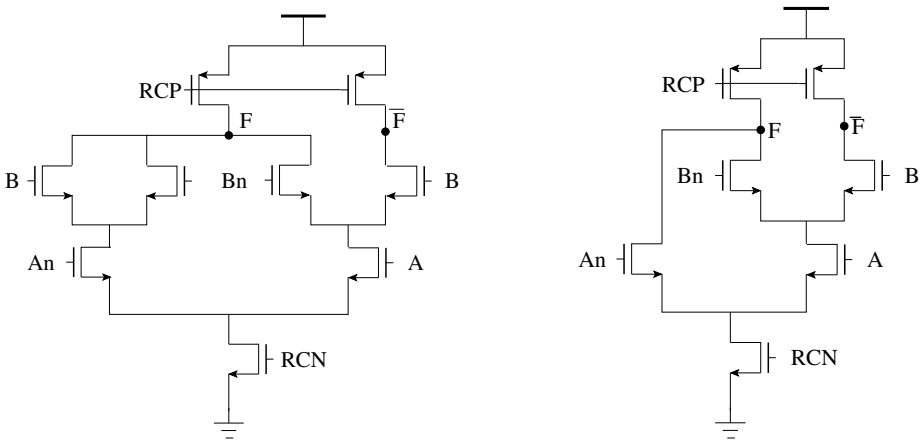


Figure 17: Mismatch Effect of Current Bias Circuit

3.4 Logic Synthesis and Robustness

In this section, tips to design sub-threshold MCML logic will be discussed. As an example, we are going to implement a AND/NAND logic. It is very straight forward to implement MCML logic; first, write Karnaugh map, then connect ”0” nodes to F(AND) and ”1” nodes to $\bar{F}$ (NAND) as in ”(a) crude AND/NAND”. Subsequently, remove ”always-on differential pair” from topology to minimize number of transistors as ”(b) minimized AND/NAND”.



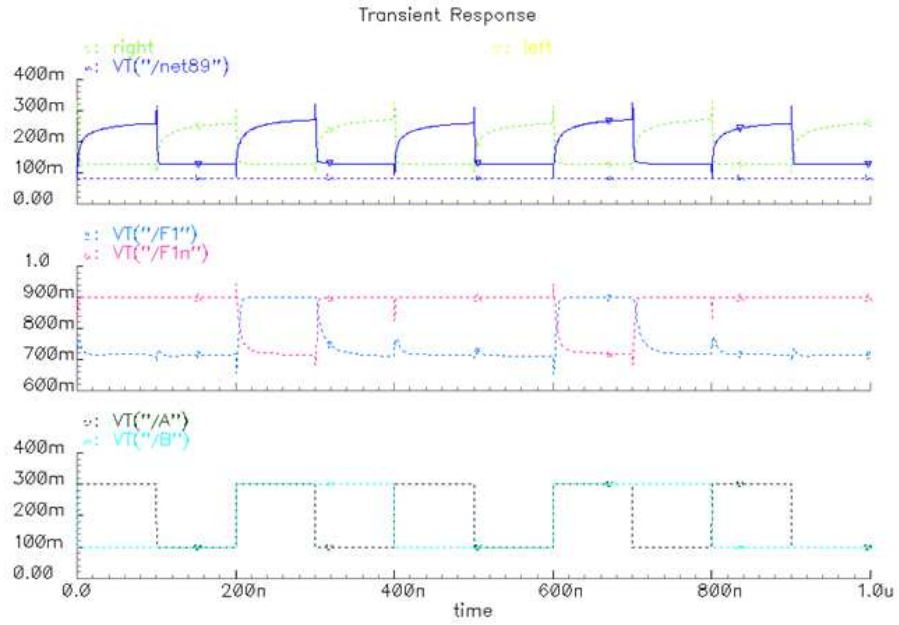
(a) Crude AND/NAND

(b) Minimized AND/NAND

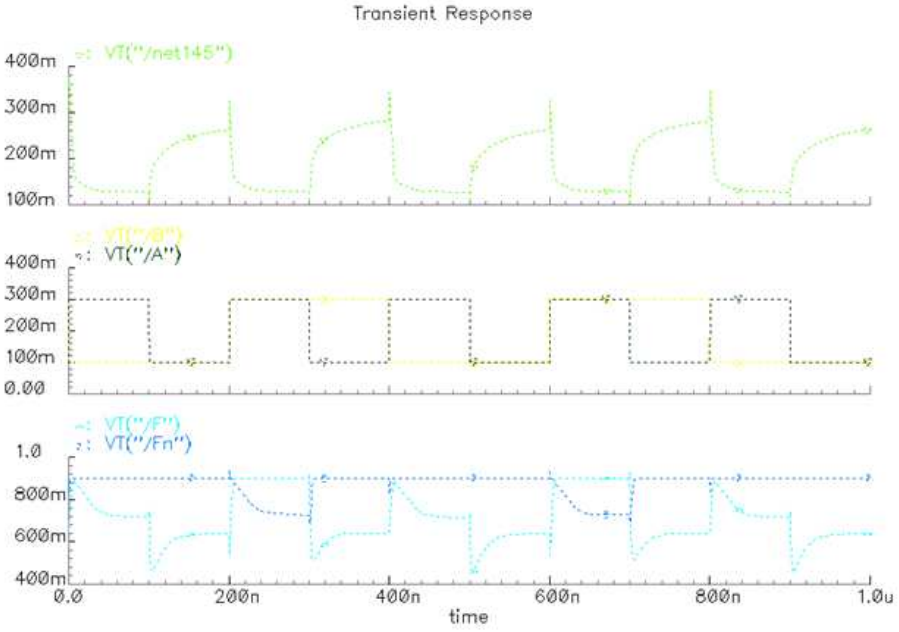
Figure 18: AND/NAND Implementation in MCML

Even though (b) is always utilized in the over-threshold MCML, removing ”always-on” diff pair is not a good idea in the case of sub-threshold MCML. In (b), just after A turns on, source node of B and Bn is still charged, and can not be fully conductive. Consequently, charge begins to be restored in the drain node to cause a hump in F despite the fact that F has to remain in low level. In (a), when right half of the circuit shut down again because source voltage of B and Bn has been charged up, left half of source voltage of B and Bn is still low enough to draw some charge. Meanwhile right half node is discharge through A, and (a) does not show a big spike as in (b).

Even though this symmetric MCML can not solve the problem thoroughly, safe operation can be guaranteed up to certain operational frequency. As [5] proposed using strong inversion MCML, these intermediate charges can be discharged using extra circuitry with the cost of extra power. (Back gate bias was expected to help discharge parasitic capacitance, however, it is observed that it cannot be a fundamental help for this problem.)



(a) Response of (a)



(b) Response of (b)

Figure 19: Transient Response of Crude vs Minimized NAND/AND

4 Clock Signal Generation with Sub-Vth MCML

As an application of sub-threshold MCML, clock generation for a UWB system proposed by [18] was chosen. In order to generate 2-GHz clock signal in ultra low power, 3-stage ring oscillator was implemented. Compared to LC-tank oscillator, its phase noise characteristic is inferior by far. However, the lenient frequency stability requirement of $\pm 10\%$ in ultra low power transceiver system proposed by [18] allows us to adopt inverter ring type of oscillator.

4.1 Ring Oscillator

In [19], differential ring oscillators with different number of stages are compared in terms of jitter. They concluded that three-stage ring oscillator has minimum jitter since the reduction of oscillation frequency to the desired value is obtained by means of the fixed capacitances C_L rather than by the voltage dependent capacitances of transistors. From this result, we adopted three-stage structure for our ring oscillator.

4.1.1 Required Gain and Phase Shift

The condition for oscillation in a three-stage oscillator is

1. Closed Loop Phase Shift = 180 degree
2. Closed Loop Gain = 1

We use the simplified model in Fig.32 for the analysis as in [20].

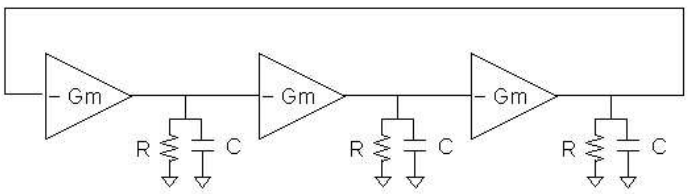


Figure 20: 3-stage Ring Oscillator

Its open loop transfer function $H(j\omega)$ is,

$$H(j\omega) = \left(\frac{-GmR}{1 + j\frac{\omega}{\omega_{RC}}} \right)^3 \tag{48}$$

where, $\omega_{RC} = 1/RC$.

In order to maintain oscillation, $H(j\omega)$ needs to satisfy magnitude and phase shift condition at the desired frequency of oscillation ω_o

$$\angle H(j\omega) = 180deg \tag{49}$$

$$|H(j\omega)| = 1 \tag{50}$$

Therefore, each stage experiences 60 degree of phase shift, and the following conditions will be derived.

$$GmR = 2 \tag{51}$$

$$f_o = \frac{\omega_o}{2\pi} = \frac{\sqrt{3}}{RC \cdot 2\pi} \tag{52}$$

More generalized solution for N-stage ring oscillator can be found in the reference [21].

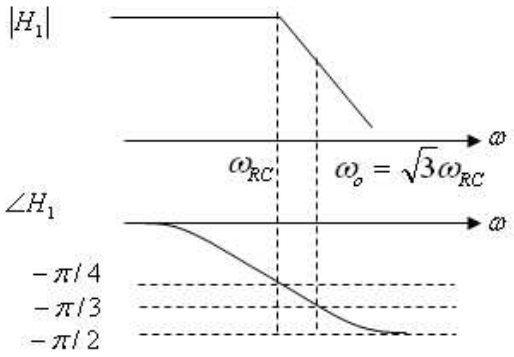


Figure 21: Body Plot of Ring Oscillator Transfer Function

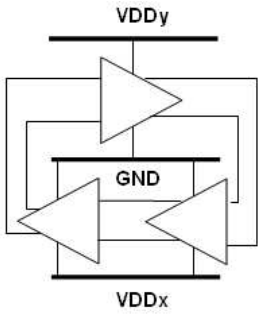
On the other hand, there is another famous formula to calculate oscillation frequency of ring oscillator. The oscillation frequency of N-stage ring oscillators is expressed with one stage delay D_{MCML} in (6).

$$f_{ring} = \frac{1}{2 \cdot N \cdot t_d} = \frac{I}{2 \cdot N \cdot C \cdot \Delta V} \tag{53}$$

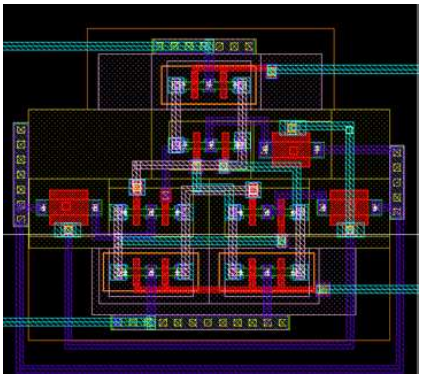
Since the pre-layout C is around 0.5fF, I=2.19uA, $\Delta V = 0.4V$, $R = \Delta V/I = 182.6KOhm$ gives us around 2.11Ghz oscillation in Spectre simulation. Hand-calculation resulted by (52) and (53) are shown below. We can say that (53) gives closer result to the simulation result.

$$f_o = 3.02GHz \tag{54}$$

$$f_{ring} = 1.82GHz \tag{55}$$



(a) Single Oscillator



(b) Layout(10um x 10um)

Figure 22: Single Oscillator

f_{ring} is based on small signal model of transistors, and it give us optimistic result since circuit is not always operating in small signal region.

The layout of each ring oscillator cell is shown below, and it occupies 10um x 10um area. Due to the high sensitivity to parasitic capacitance, ring oscillator layout needs to be symmetric. We did not put dummy buffers at each stages to achieve perfect symmetry in order to save area. Parasitic capacitance was extracted for this layout and post-layout simulation was checked. Due to the parasitic capacitances between each stages which are in the order of 0.5fF, post-layout frequency ended up with four-fold slower value, 500 MHz. Therefore, in order to achieve 2-GHz oscillation, we need to increase the bias current by 4-times, and power consumption of a single oscillator is $4 \times 6uA = 24uA$ under 1.25-V voltage supply.

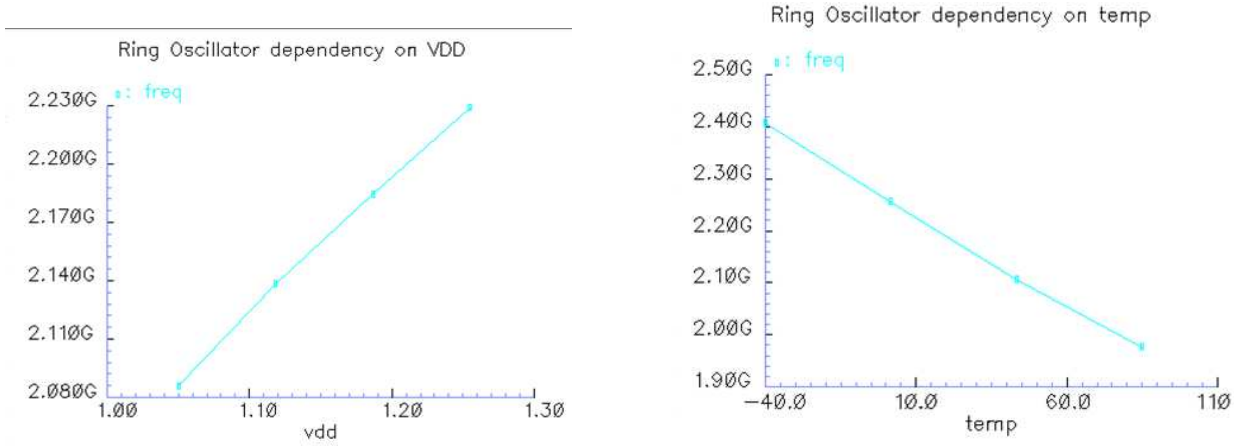
4.2 PVT Variation Effect

3-stage ring oscillator was tested with the current reference circuit (subsection 3.1.3) and Replica Bias Circuit [7] over $\pm 10\%$ VDD fluctuation, and -40 to 85 degree temperature range (Fig.23).

The variation of frequency is thus summarized as in Table 7. From Eq.(53), frequency is proportional to bias current $I = I_{ss}$, and therefore, the frequency variation is almost consistent with the current variation in Table.5

Temp	-40 85 C°	freq	$\pm 9.8\%$
VDD	$\pm 10\%$	freq	$\pm 3.3\%$

Table 7: Iss with Temp, VDD variation



(a) $Freq$ vs VDD

(b) $Freq$ vs $Temp$

Figure 23: Freqency Variation

5 Coupled Oscillator Array

In order to measure spacious variation of frequency, one hundred ring oscillators were mounted in a same die. One important characterisitic of oscillator is phase noise. Phase noise of ring oscillator is known to be inferior to that of LC oscillator. Now, our interest is directed to a simple question: ”Is phase noise going to decrease or increase if a bunch of oscillators coupled each other ?”. As a side topic of this research, we investigated coupling/injection effect on phase noise in a oscillator array.

5.1 History

Synchronized oscillation is nothing but a natural phenomena which can be seen in many situations around us. It has been studied for more than two decades especially in the field of chemistry, biology, and physics. In the field of electronics, radar systems or mm-wave communication are the emerging fields which are actively using this phenomena.

York and his group in University of California, Santa Barbara, has shown the coupling phenomena of an oscillation array by means of electric circuits [22], and they proved the decrease of phase noise as being proportional to the number of coupled oscillators. This chapter is devoted for this long research history of synchronized oscillation phenomena, followed by derivation of phase noise prediction in an oscillator array.

Even though most of us do not really notice it, synchronized oscillation phenomena is appearing

in many situations around us: [1]

- Circadian rhythms

  Many living organisms synchronize to the day-night cycle.

- Electrical generators

  All of the generators producing power on a power grid must be synchronized to one another.

- Josephson junction arrays

  Josephson junctions are fabricated, microscopic devices that behave as compact electronic oscillators, and different geometric arrangements of Josephson junctions form systems of oscillators that have been found theoretically to exhibit synchronization.

- Heart, intestinal muscles

  The muscles in your heart, for example, must all be synchronized to create a coherent beat.

- Menstrual cycles

  It has been found that the menstrual cycles of women who live together often synchronize.

- Fireflies

  Certain species of fireflies have been found to synchronize, creating swaths of light turning on and off at the same time.

- Applause

  In Eastern Europe, it is customary to clap in synchrony after a good performance.

Active research to model this natural phenomena has been conducted for over decades in diverse fields such as biology, chemistry, physics, and electronics. In the history, a Dutch scientist, Christian Huygens first time recorded his observation of coupled oscillator synchronization in 1665 [23]: while confined to bed by illness, he noticed that the pendulums of two clocks on the wall moved in unison if the clocks were hung close to each other. He postulated that the coupling of the

[1] Video of mechanical synchronization phenomena: http://physics.owu.edu/StudentResearch/2005/BryanDaniels/index.html , Bryan Daniels

mechanical vibrations through the wall drove the clocks into synchronization[1]. Since this Huygens finding, two streams of researches to understand a population of coupled oscillators appeared [24],[25]. One is on "Macro Model" and the other is on "Micro Model" of coupled oscillators.

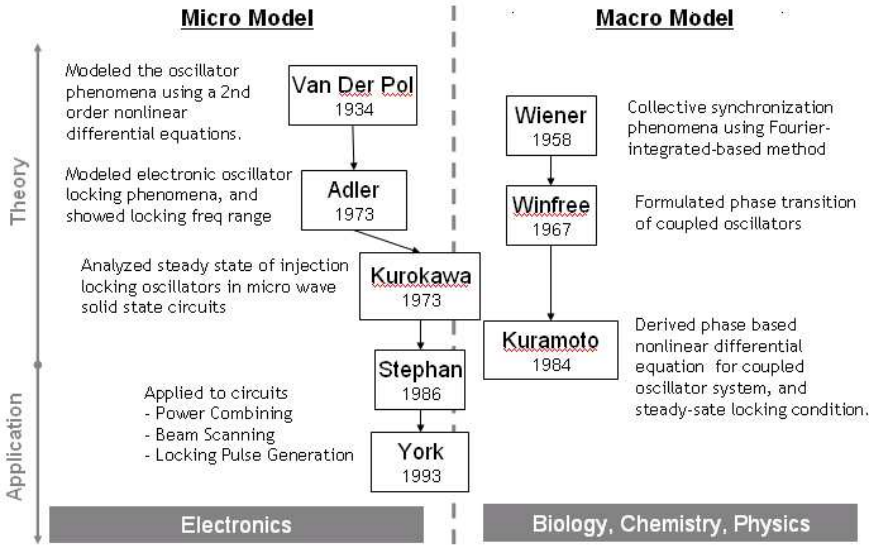


Figure 24: Research History of Coupling Oscillator Array

The research on "Macro Model" started from Wiener's research on collective synchronization phenomena using Fourier-integrated-based method in 1958. This research is thereafter continued by Winfree. He formulated an equation governing phase transition of coupled limit-cycle oscillators and presented concept of a phase sensitivity function in 1967. In 1984, Kuramoto applied Winfree's approach to systems of identical oscillators with equally weighted, purely sinusoidal couplings, and derived well-known phase based nonlinear differential equation model for coupled oscillator systems. He also developed a steady-sate locking condition which has been shown to successfully predict bifurcation of phase transitions in coupled oscillator system. This research formed the foundation of today's synchronized oscillator research in the field of chemistry, biology and physics. The model shown by Kuramoto is as follows;

$$\frac{d\theta_i}{dt} = \omega_i + \frac{K}{N}\sum_{j=1}^{N} sin(\theta_j - \theta_i) \tag{56}$$

,where θ is the phase of each oscillator, ω is the natural frequency of each oscillator, N is the number of oscillators, and K is the coupling constant.

Kuramoto showed coupling condition of oscillator: when K is larger than the threshold value K_c, coupling occurs.

Recently, Roychowdhury developed simpler algorithm to calculate Kurokawa's coupling model, and showed its application for image processing [26].

The other stream of research, "Micro Model" of coupled oscillators, opened the doors to three big

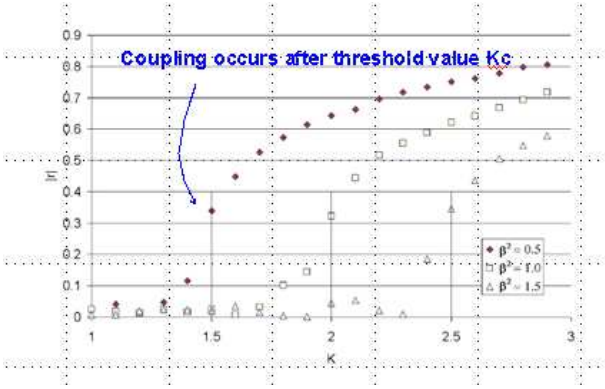


Figure 25: Locking Condition from Kuramoto Model

techniques in the field of electronics: mm-wave power combining, electronic beam scanning, and mode locking for pulse generation. After Van der Pol modeled the oscillator phenomena using 2nd order nonlinear differential equations in 1934, Adler derived a differential equation that relates the oscillator phase to the injection signal parameters, and also showed locking frequency range [27].

$$\frac{d\phi}{dt} = \omega_o - \omega_{inj} + \Delta\omega_m sin(\psi - \phi) \tag{57}$$

where the locking frequency is,

$$\Delta\omega_m = \frac{\omega_o \rho}{2QA} \tag{58}$$

Following Adler's research, Kurokawa applied work of Van der Pol to the injection of microwave oscillators in 1973 [28]. Finally, these theoretical research had started being applied to electronic circuit by two pioneers, Stephan and York. Especially, York derived a set of coupled nonlinear differential equations for coupled nonlinear oscillators based on Adler's and Kurokawa's works. York's work extended micro model of coupled oscillator to macro model. Stephan in 1986 and York in 1993 respectively proposed new method to form evenly spaced phases from 1-D coupled oscillator array by injecting frequency or phase to the two ends[29],[22]. This technique has been applied to power combining purposes in mm-wave circuits.

York also later showed that if a signal with clean phase noise profile gets injected to oscillator array [30]. This technique is called as "Injection Locking", and widely used to generate low phase noise signals [31]. Recently, quadrature signal generation was achieved in 60GHz application by applying this injection locking technique in coupling oscillator [32].

5.2 Oscillator Coupling

Oscillator coupling is categorized into "Unilateral Coupling" and "Bilateral Coupling".
"Unilateral Coupling" is the phenomena when the frequency of an oscillator changes to the frequency of the other as shown in the Fig.26 from [25]. This happens when the powers of two oscillators are not equivalent.

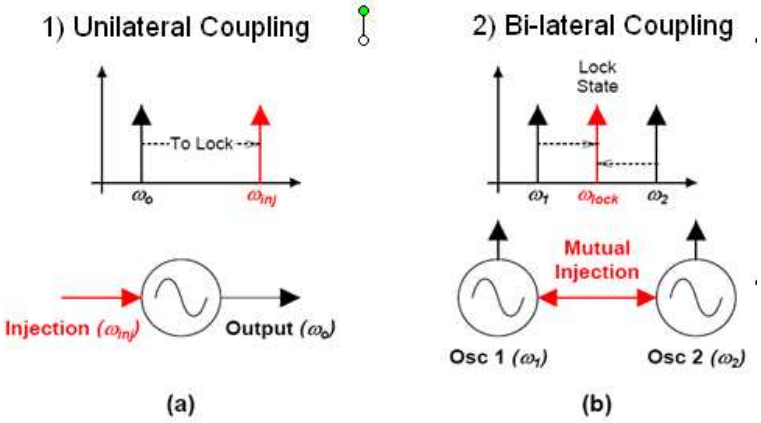


Figure 26: (a)Unilateral (b)Bilateral Injection of Nonlinear Oscillator

In our ring oscillator array, all the oscillators are same. In this case, the latter coupling type, "Bilateral Coupling" is supposed to be an appropriate model. In this case, negative feedbacks control each oscillators, and they are going to be locked in the same frequency, furthermore, in the same phase. The famous Adler's equation, Eq.(57), is showing this bilateral coupling in the steady state:

$$\frac{d\phi}{dt} = \omega_o - \omega_{inj} + \Delta\omega_m sin(\psi - \phi) \tag{59}$$

$$\rightarrow 0(SteadyState) \tag{60}$$

$$\psi - \phi = sin^{-1}(\frac{\omega_{inj} - \omega_o}{\delta\omega_m}) \tag{61}$$

This model is also called as Kurokawa model after small transformation.

$$\Delta\phi = sin^{-1}(\frac{2Q}{\omega_o}\frac{I_{osc}}{I_{inj}}\Delta\omega) \tag{62}$$

where $\Delta\phi = \phi_o - \phi_{inj}$ and $\Delta\omega = \omega_o - \omega_{inj}$. For the application of power combining, people control ω_{inj} to control the output angle ϕ in Eq.(59). In the case of our ring oscillator array, injection frequency is same as natural frequency,

$$\omega_{inj} = \omega_o \tag{63}$$

Therefore, from (59), we conclude that the phases of adjacent coupled oscillators in an array should be same.

$$\psi = \phi \tag{64}$$

5.3 Phase Noise in Oscillator Array

In this section, we discuss the effect of oscillator coupling on their phase noise, and show the hand calculation and simulation result in the end.

Effect of Coupling on Phase Noise

In the previous section, we have seen that multiple oscillator will pull each other and, in the steady state, they converge to the same frequency and the same phase. Assuming that if one of the oscillator is exposed to external noise, and experiences phase shift, then this oscillator is expected to be pulled back in to the previous phase thanks to the bilateral feedback/coupling existing in this oscillator array. Thus, phase fluctuation is suppressed, and the phase noise is expected to decrease by some amount. The unconventional solution for phase noise reduction in coupling N oscillators was proved in [30],[25]. Quantitatively, the phase noise is decreased by a factor of $1/N$.

$$|\delta\tilde{\theta_{total}}|^2 \rightarrow \frac{1}{N}|\delta\tilde{\theta}_i|^2_{uncoupled} \tag{65}$$

In [20], another way to understand this $1/N$ suppression of phase noise is given.

If the ouput voltages of N identical oscillators are added in phase, then the total carrier power is multiplied by N^2, whereas the noise power increases by N. Thus the phase noise relative to the carrier decreases by a factor N at the cost of a proportional increase in power dissipation.

Phase Noise Calculation

A formula to calculate phase noise of a ring oscillator is referenced from [20]. We used R =182.6K Ω as being used to calculate (55).

$$PhaseNoise = \boldsymbol{L}(\Delta\omega)[dBc/\sqrt{Hz}] = 8kT\frac{R}{9}\left(\frac{\omega_o}{\delta\omega}\right)^2 = -85.7dBc/\sqrt{Hz} \tag{66}$$

Now, spectre RF simulation gives a much worse phase noise result as $-60dBc/\sqrt{Hz}$ at $1MHz$ offset from carrier frequency of $2GHz$. From (65), when all the 100 oscillators in an array are coupled, and the expected phase noise is $-60 - 20 = -80dBc/\sqrt{Hz}$.

Figure of Merit on Phase Noise and Power

Phase noise and power consumption are in the trade-off relationship [33],and a FoM of oscillators can be calculated as follows;

$$FoM = \boldsymbol{L}(\Delta\omega)[dBc/\sqrt{Hz}] + 10Log(P_{dc}[mW]) - 20log(\frac{\omega_o}{\Delta\omega}) \tag{67}$$

where, $\boldsymbol{L}(\Delta\omega)$: Total single sideband phase-noise spectral density, and P_{dc}: Total VCO power consumption

However, even if the phase noise of ring oscillator will be decreased as we increase the number of coupled oscillators, FoM remains same since the power also increases along the number of oscillators. In Table 8, we compare FoM and area of LC tank oscillator from a recent technology to our sub-Vth MCML ring oscillator. Thus, FoM cannot be ameliorated by means of coupling.

	FoM@1MHz[dB]	Phase Noise[dBc/Hz]	Area[mm^2]
LC oscillator[34]	-180	-132	0.15
1 sub-vth MCML Ring Osc	-146	-60	0.0001
100 sub-Vth MCML Ring Osc	-146	-80	0.01

Table 8: FoM and Area of LC Oscillator and sub-Vth MCML Ring Oscillator

Oscillator has intrinsic FoM, and LC-tank oscillator has better inane characteristics in terms of FoM. In the recent study in [35] also pointed out this limitation of this scheme. However, the small size and portability of ring oscillator is still attractive to a system which has some endurance to variation of frequency to certain extent.

5.4 Coupling Range

So far, we have not specified the condition of coupling. In fact, the coupling condition of ring oscillator has not yet been shown in any literature. On the other hand, the coupling condition and coupling range of LC oscillator was shown by many sources:[27],[1], and graphically shown in Fig. 27.

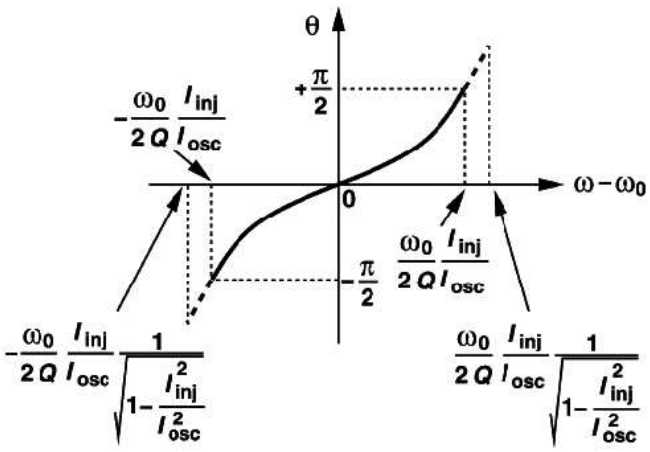


Figure 27: Phase shift in an Injection-locked LC-tank Oscillator from [1]

Empirical results reported in [1] and [21] showed really narrow locking ranges of both LC-tank and ring oscillators. In case of LC-tank oscillators, this is caused by its high Q, and they often end up with weakly coupled state as shown in [1], [2]. In [2], two nominally identical LC-tank oscillators were fabricated, and the difference of their oscillation frequencies, 1.02GHz and 1.04Ghz, was only few percent. Still, high Q of LC-tank oscillators hindered oscillators from coupling to each other, and they showed the typical frequency characteristics of weakly coupled oscillator as shown in Fig. 28.([1],[2]) When the coupling is not strong enough, frequency spectrum becomes like something that of modulated signal.

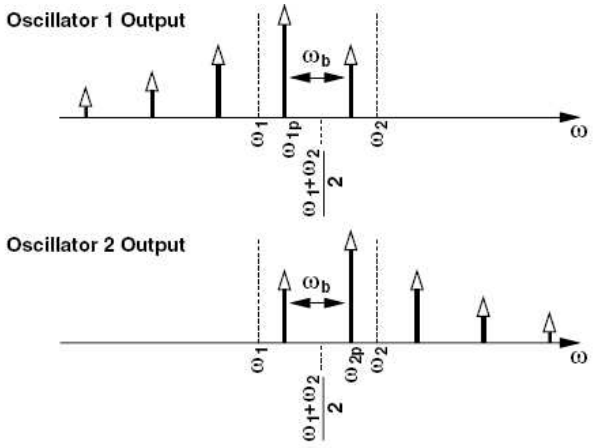


Figure 28: Output Spectra Under Mutual Pulling Condition from [2]

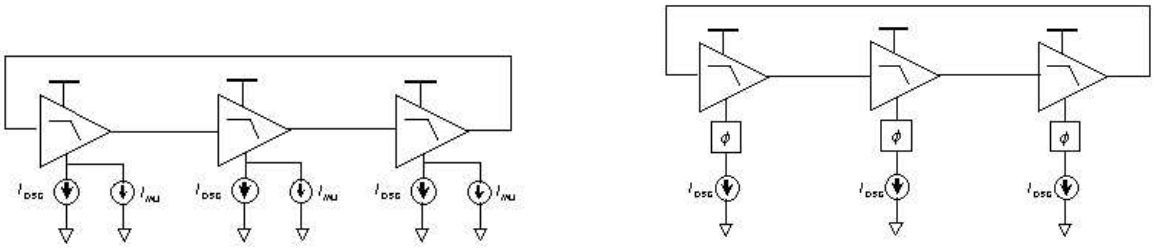
In the case of ring oscillator, quality factor Q is around 1. If we optimistically assume that the same theory can be applied to ring oscillators, it can be expected to have large locking range, and to be easier to couple. However, the reported locking range of ring oscillators in [21] is only 2% despite the hand-calculation can go as large as 30%. [2]

In status quo, people have found it quite hard to couple oscillator in their free running condition, and they rather inject clean signal and exploit the constant phase shift appears over coupled oscillator [32], [22], [30]. Since the main application of oscillator coupling is mm-wave tranceiver or power combining, even for 0.1% of locking range reported in [32], the frequency to control is few ten Mega Hz.

[2]The author concluded that injection efficiency lowers due to the parasitic capacitance at the device where the signal is injected.

In order to compare the locking range of LC-tank oscillators in Fig27 to that of ring oscillators, we apply the same concept as [1] for LC-tank oscillator.

Assuming that the same injection current I_{inj} is injected to the tail current which induces phase shift ϕ to each stage of a three stage ring oscillator.



(a) Current Injected Ring Oscillator (b) Resulted Phase Shift in Ring Oscillator

Figure 29: Injected Ring Oscillator Model

Let's define the phase shift in a single stage as α which cancel out ϕ to recover system to oscillation, then,

$$-\alpha = \phi = tan^{-1}\left(-\frac{\omega}{\omega_{RC}}\right) \tag{68}$$

which corresponds to the Eq.(5) in [1]. From Eq.(2) in [1], injection current I_{inj}, oscillator nominal current I_{osc}, and angle between I_{inj} and I_{osc} are related to ϕ.

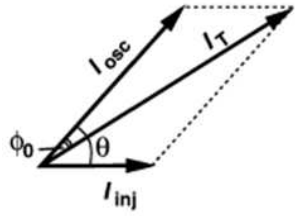


Figure 30: Geometric Relationship of Injected Current and Oscillator Current

, and the geometric calculation goes as follows.

$$sin\phi = \frac{I_{inj}sin\theta}{\sqrt{I_{osc}^2 + I_{inj}^2 + 2I_{osc}I_{inj}cos\theta}} \tag{69}$$

This equation is further reduced when we assume $I_{inj} << I_{osc}$.

$$sin\phi = sin\theta\frac{I_{inj}}{I_{osc}} \tag{70}$$

, which implies ϕ is small, and we can assume that $tan\phi \approx sin\phi$. Thus, (70) and (68) give

$$sin\theta = \frac{I_{osc}}{I_{inj}} tan\phi = \frac{I_{osc}}{I_{inj}} \frac{\omega}{\omega_{RC}} \tag{71}$$

$$\theta = sin^{-1}\left(\frac{I_{osc}}{I_{inj}} \frac{\omega}{\omega_{RC}}\right) \equiv sin^{-1}\left(\frac{\omega}{\omega_L}\right) \tag{72}$$

Here we define locking range as

$$\omega_L \equiv \frac{I_{inj}}{I_{osc}} \omega_{RC}$$

Now, we can plot (72), and mark the limit of the lock range which occurs when $sin\theta = \pm 1$.

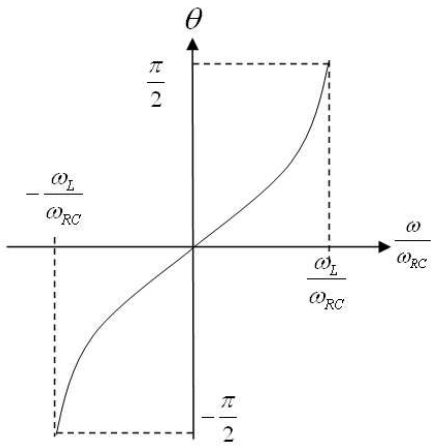


Figure 31: Phase Shift in an Injection-locked Ring Oscillator

Different from LC-tank oscillator, Injection locking occurs if $\omega_{inj} << \omega_{RC}$. Since we assumed that $I_{inj} << I_{osc}$, the upper limit is much smaller than one. This result shows that ring oscillator can lock only to quite low frequency, and ring oscillator arrays cannot be locked to each other in free-running state.

Now we notice the mechanism of coupling oscillation, and its necessary condition. Our speculation is that two characteristics of ring oscillator cause this narrow locking range of ring oscillators. The first one is gain condition: Since a ring oscillator needs to satisfy gain condition in (51), a frequency to be locked needs to be at least lower than ω_o. In contrast, LC-tank oscillator has band pass filter profile around resonant frequency, and it has high enough gain even the frequency of operation shifts to higher frequency than its resonant frequency. The second one is phase shift condition: Phase characteristics of low pass filter is not symmetric like that of bandpass filter of LC-tank oscillator, and the phase range which ring oscillator can take around oscillation frequency ω_o is quite narrow. Also, the one-pole model we used in Fig.32 which allows phi to be from 0 to $\pi/2$ whereas 2nd order system of LC-tank allows from $\pi/2$ to $-\pi/2$.

Thus, we can conclude that a oscillator which can be coupled easily around the desired frequency

ω_{des} is LC-tank oscillator of $\omega_o = \omega_{des}$ with low-Q inductor, or ring oscillator with $\omega_{des} << \omega_o$. Coupling range and phase noise are in trade-off relationship. Since the result reveals the fact that a system with band pass characteristics is ideal to cause coupling to its twin brothers, we can simply cascade high pass and low pass filters to realize band pass characteristics.

5.5 Weakly Coupling Oscillator Behavior

As shown in Fig.28, weakly coupled LC tank oscillator has higher order distortion characterized by a frequency ω_b. We are interested in the case of ring oscillator, and follow the same calculation procedure to obtain ω_b for ring oscillator.

As in Eq(16) in [1], if we add instantaneous input frequency as $d\psi/dt$, then total input frequency can be expressed as $\omega + d\psi/dt$. Therefore, (72) is going to be,

$$tan\alpha = \frac{\omega + \frac{d\psi}{dt}}{\omega_{RC}} \tag{73}$$

Now, we use the same model as in Fig.6 in [1], meaning that system has locked to the injection signal with frequency ω_{inj} but with phase shift θ at the output.

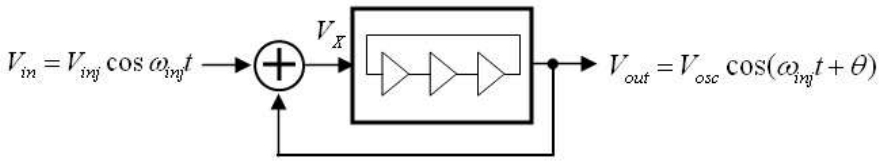


Figure 32: Weakly Coupled Ring Oscillator Bilateral Model

$$V_{in} = V_{inj}cos\omega_{inj}t \tag{74}$$

$$V_{out} = cos(\omega_{inj}t + \theta) \tag{75}$$

$$V_X = V_{in} + V_{out} \tag{76}$$

With the assumption of $V_{inj} << V_{osc}$,

$$V_X \approx V_{osc}cos(\omega_{inj}t + \psi) \qquad [1] - (21)$$

After signal goes through ring oscillator, phase shift should be added as in Eq(22) of [1].

$$V_{out} \approx V_{osc}cos\left\{\omega_{inj} + \psi + tan^{-1}\left(-\frac{\omega + \frac{d\psi}{dt}}{\omega_{RC}}\right)\right\} \tag{77}$$

Compared to the (75),

$$\psi + tan^{-1}\left(\frac{\omega + \frac{d\psi}{dt}}{\omega_{RC}}\right) = \theta \tag{78}$$

From [1],

$$\frac{d\psi}{dt} \approx \frac{d\theta}{dt} \qquad [1]-(24)$$

$$tan(\theta - \psi) \approx \frac{V_{inj}}{V_{osc}} sin\theta \qquad [1]-(26)$$

From (78),[1] - (24),[1] - (26), we can get Adler's equation for ring oscillators.

$$\frac{d\theta}{dt} = -\frac{V_{inj}}{V_{osc}}\omega_{RC} \cdot sin\theta - \omega_{inj} \tag{79}$$

5.5.1 Locked State

Under locked condition i.e. steady state,

$$\frac{d\theta}{dt} = 0$$

and (79) yields the locking range as in (72).

$$\theta = sin^{-1}\left(\frac{I_{osc}}{I_{inj}}\frac{\omega}{\omega_{RC}}\right) \tag{72}$$

5.5.2 Weakly Locked State

In under locked condition, (79) must be solved. (79) can be rewritten as

$$\frac{d\theta}{-\frac{V_{inj}}{V_{osc}}\omega_{RC}sin\theta - \omega_{inj}} = dt \tag{80}$$

The integral of (80)=$\int dt$ can be solved as a function of time t.

$$\int \frac{d\theta}{-\frac{V_{inj}}{V_{osc}}\omega_{RC}sin\theta - \omega_{inj}} = \int dt \tag{81}$$

The general solution of this equation is given in Appendix A:

$$\int \frac{d\theta}{a + b\sin\theta} = \int dt \tag{82}$$

The solution of the above equation is

$$\sqrt{1 - \frac{b^2}{a^2}}\tan\left(\frac{-\sqrt{a^2 - b^2}}{2}t\right) = \tan\frac{\theta}{2} + \frac{b}{a}$$

By using this formula, (81) becomes

$$tan\frac{\theta}{2} = \frac{\frac{V_{inj}}{V_{osc}}\omega_{RC}}{-\omega_{inj}} + \frac{\omega_b}{-\omega_{inj}} tan\frac{\omega_b t}{2} \tag{83}$$

$$\frac{\omega_L}{-\omega_{inj}} + \frac{\omega_b}{-\omega_{inj}} tan\frac{\omega_b t}{2} \tag{84}$$

$$\omega_b \equiv \sqrt{(\omega_{inj})^2 - \left(\frac{V_{inj}}{V_{osc}}\omega_R C\right)^2} = \sqrt{\omega_{inj}^2 - \omega_L^2} \tag{85}$$

By using this equation, we can evaluate behavior of output frequency $\omega_{inj}t + \theta$ for two cases of ω_{inj} out of locking range.

Quasi-Lock

"Quasi-Lock" is defined as the state where ω_{inj} is slightly faster than lower locking range. i.e.

$$\omega_{inj} > \omega_L$$

$$\omega_{inj} \approx \omega_L$$

Under this condition, transient behavior of quasi-locked system can be analyzed. From (84) and (85),

$$(85) : \omega_b = \sqrt{\omega_{inj}^2 - \omega_L^2} \approx 0$$

$$(84) : tan\frac{\theta}{2} = \frac{\omega_L}{-\omega_{inj}} + \frac{\omega_b}{-\omega_{inj}} tan\frac{\omega_b t}{2} \approx -1 + \frac{\omega_b}{-\omega_{inj}} tan\frac{\omega_b t}{2}$$

Therefore, the plot of theta has cycle of $\frac{2\pi}{\omega_b}$, and stays in $-\frac{\pi}{2}$ for most of the time which is different from the case of LC-tank oscillator stays in $\pi/2$.

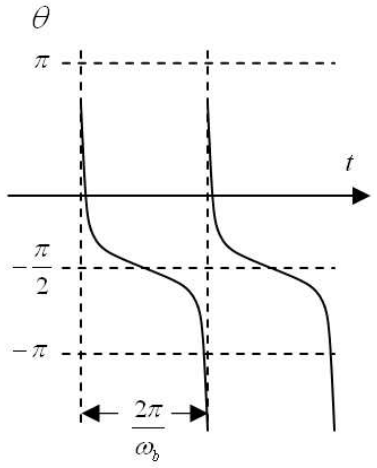


Figure 33: Output Phase Shift θ of Ring Oscillator in Quasi-Lock

Output frequency is

$$\omega_{inj} + \frac{d\theta}{dt} = \omega_{inj} - \omega_L \cdot sin\theta - \omega_{inj} \tag{86}$$

$$= -\omega_L \cdot sin\theta \tag{87}$$

$$\approx \omega_{inj} sin\theta \tag{88}$$

which is depicted in the following figure. Contrast to LC-tank oscillators output frequency range from ω_{inj} to $\omega_o + \omega_l$, output of ring oscillators spans from $-\omega_L$ to ω_L. PDF function of ring oscil-

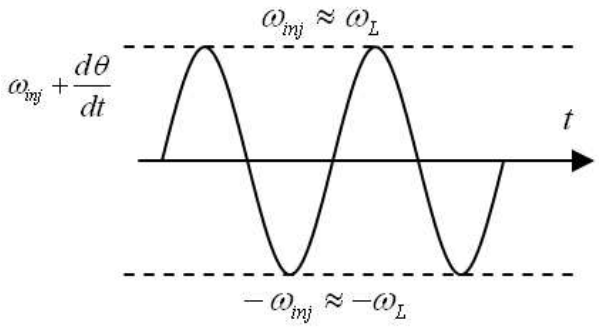
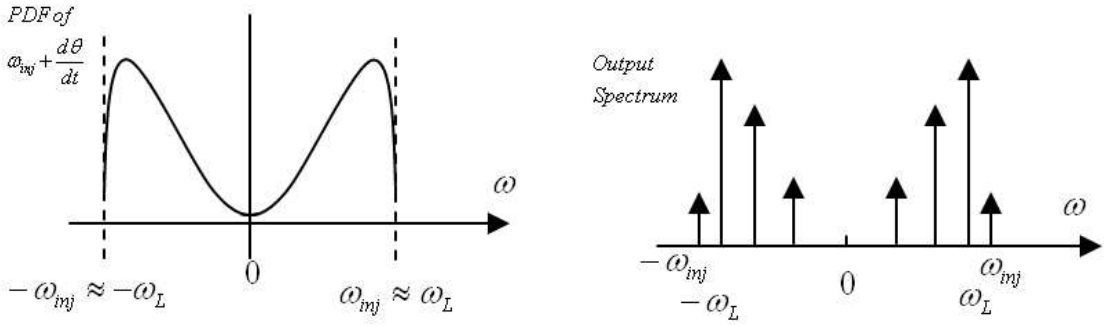


Figure 34: Output Frequency Behavior of Ring Oscillator in Quasi-Lock

lator can be estimated from the output frequency analysis shown above. The estimated distribution of PDF and output spectrum are roughly expected as below;



(a) PDF

(b) Spectrum

Figure 35: Output PDF and Spectrum of Quasi-Locked Ring Oscillator

Fast Beat

"Fast Beat" is defined as the state where

$$\omega_{inj} >> \omega_L$$

We conducted the same analysis as in "Quasi-locked", and obtained the following results. Again, (84) and (85) in this case are approximated as below;

$$(85) : \omega_b = \sqrt{\omega_{inj}^2 - \omega_L^2} \approx \omega_{inj}$$

$$(84) : tan\frac{\theta}{2} = \frac{\omega_L}{-\omega_{inj}} + \frac{\omega_b}{-\omega_{inj}} tan\frac{\omega_b t}{2} \approx 0 + \frac{\omega_b}{-\omega_{inj}} tan\frac{\omega_b t}{2}$$

$$\approx -tan\frac{\omega_b t}{2}$$

In this case, θ is almost proportional to $\omega_b \cdot t$, and linearly changes as time goes by. It does not stay in specific angle as we saw in the Quasi-Locked state. Therefore, output signal looks like slipping all the time.

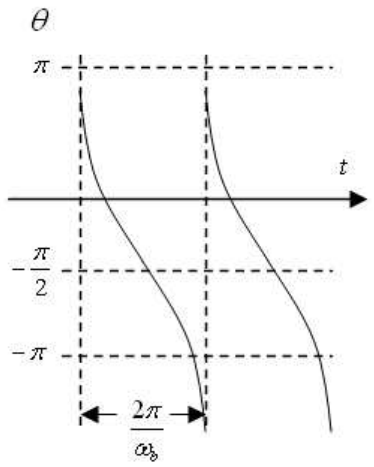


Figure 36: Output Phase Shift θ of Ring Oscillator in Fast Beat

Output frequency as a function of time t is

$$\omega_{inj} + \frac{d\theta}{dt} = \omega_L \cdot sin\theta \approx \omega_L \cdot sin\omega_b t \tag{89}$$

which gives similar result as in Quasi-locked case.

In conclusion, both in Quasi-Locked and in Fast Beat states, output spectrum of ring oscillators has symmetric distribution with respect to zero Hz, and the maximum power of spectrum is around the limit of locking range ω_L

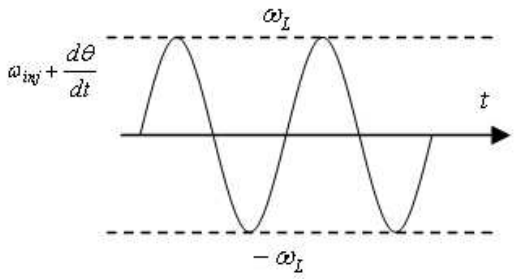


Figure 37: Output Frequency Behavior of Ring Oscillator in Fast Beat

5.6 Spectre Simulation

In order to verify the calculation done in the previous subsection, we simulated locking phenomena by Spectre. Two different injection scenarios are tested. The first scenario falls on to the setting we calculated in the previous section, however in order to apply to the simulation result in this section, it requires modification in a variable.

5.6.1 Common-mode Injection

The first scenario is when injectoin current comes as common mode noise. Ideal VCVS (Voltage Controlled Current Source) was used to inject current proportional to injection signal to the tail current source as in the calculation model in Fig.29. The values of injected current i_{inj} and oscillation current i_{osc} are $i_{inj} = \pm 0.6uApeak$ and $i_{osc} = 1.923uA(DC) \pm 0.377uApeak$, and free running oscillation frequency was $f_o = 2.56GHz$.
In the previous section, we calculated that ring oscillator locks to injected signal which has frequency within the locking range $\omega_{RC}\frac{I_{inj}}{I_{osc}}$. In the case of our ring oscillator, $\omega_{RC} = 1GHz$, and locking range is approximately around 1GHz.

Signal with 0.5GHz, 1GHz, 1.5GHz, 2GHz, 3GHz, and 4GHz were injected to result in the following spectrum in the output of ring oscillator.(Fig. 38) Output spectrum shows free-running signal modulated by injected signal, and it has harmonics at $f_o \pm f_{inj}$. The power of harmonics follows low pass characteristics of ring oscillator, and this injection system can be modeled as a combination of multiplier and low pass filter [21].

When we inject further slower frequencies, 0.1GHz, 0.25GHz, and 0.5GHz as in Fig.39. We see the second harmonic increases up to the power equivalent to free running signal f_o. Interestingly enough, the spectrum is not symmetric respect to free-running spectrum, and it resembles to the spectrum predicted for quosi-locking in Fig.35. This is because the signal which should have

been used in the calculations in the previous section was not ω_{inj}, but $\omega_o - \omega_{inj}$ since this second harmonic is the signal which goes around the loop in the case of common-mode injection.

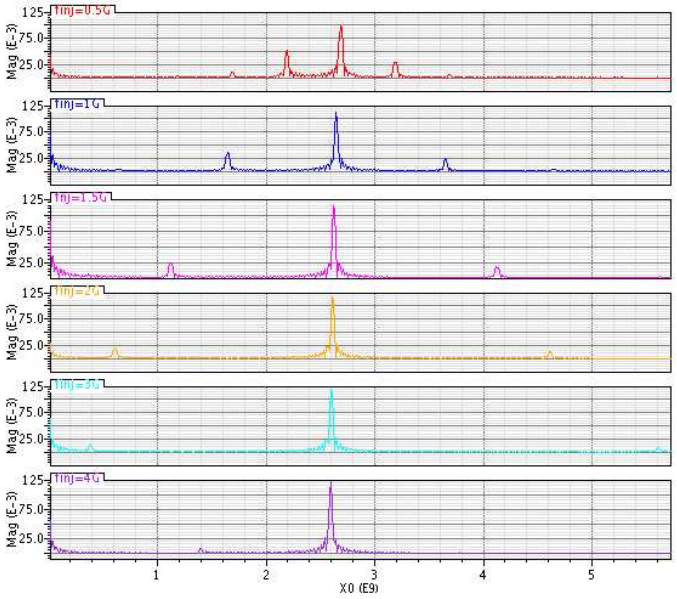


Figure 38: Output Spectrum of Signal Injecterd Ring Oscillator

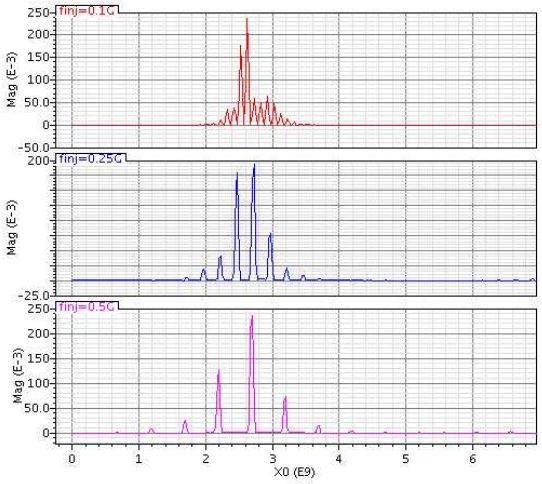


Figure 39: Output Spectrum of Slow Signal Injected Signals

We are not going to modify all the equations and graphs provided in the subsection 5.4, but will show the important figures as follows.

The revised locking range graph of common-mode injected ring oscillator is in Fig. 40

The modified locking range is $\omega'_L = (\omega_o \pm \omega_L)$, and now it has bandpass characteristics like LC-tank oscillator. This result verifies the symmetric spectrum in Fig. 38. Althogh the locking range is simular to that of LC-tank oscillator, signal going around the ring oscillator is $\omega_o - \omega_{inj}$ and much lower frequency than free running frequency ω_o. Thus, the ring oscillators still do not lock to each other in free-running oscillation .

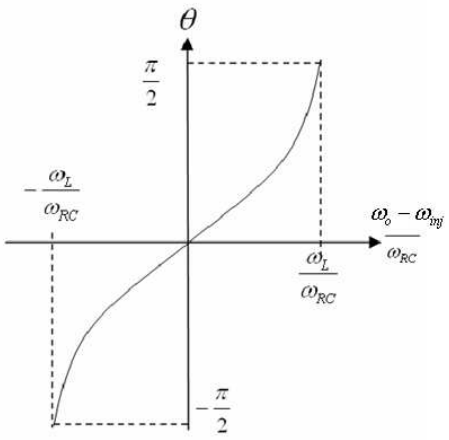
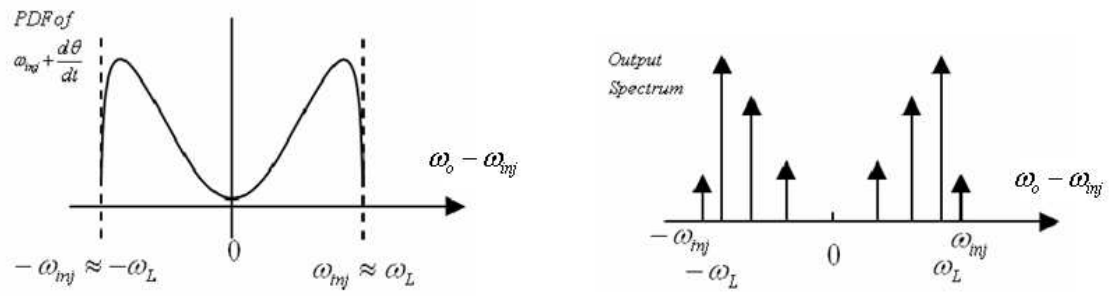


Figure 40: Phase Shift in an Common-Mode Injection-locked Ring Oscillator

After replotting the output spectrum of Common-mode injected ring oscillator in Fig. 41, we confirmed that the simulation result matches to the calculation model. Different from the Quasi-Locking state of LC-tank oscillator, ring oscillator shows low pass filter type of weakly coupled phenomena as estimated in Fig. 41.



(a) PDF

(b) Spectrum

Figure 41: Output PDF and Spectrum of Quasi-Locked Common-Mode Injected Ring Oscillator

As a conclusiont of this subsecion, we succeeded in validating the calculation in 5.4 with the mod-

ification of calculation: we need to replace ω_{inj} with $\omega_o - \omega_{inj}$ After this modification, simulation result by Spectre matches to the calculation.

The model proposed by [21] analyzed this type of injection locking in the way of commutating mixer analysis, but they have not mentioned weekly-coupled behavior. They used different approach to calculate locking range, and we have not compare theirs and ours quantatively, but two equations have similar shape.

In the oscillation array which was fabricated in the end of this research, the output spectrum of oscilltors should be similar to the result of this Spectre Simulation because the injection mechanism is indirectly via substrate without using any kind of differential coupler. This simulation concludes that we cannot expect any modification in phase noise by coupling effect.

In the model, we assumed that differential nature of the output is still kept under current injection. However, when we inject current to tail current, we modulate bias condition of differential pair and cannot sustain the small signal model in Fig.29: If the power of injection is too strong, it even collapses differential nature of output swing. In the next section, a singal is going to be injected in differential manner.

5.6.2 Differential Injection

Differential injection current was injected by VCCS (Voltage Controlled Current Source) with the same magnitude as small signal current in free-running operation (Fig. 5.6.2). When $i_{osc} = 1.923uADC \pm 0.377uApeak$, Gm of VCCS was $gm_{inj} = 1.5uS$ which gives $i_{inj} = \pm 0.3uApeak$.

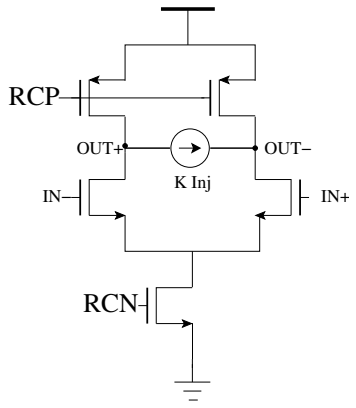


Figure 42: Differential Injection Scheme

We have obtained the following differential output spectrum with injection frequency of 0.1-GHz, 1-GHz, 2-GHz, 2.5-GHz, 3-GHz, and 4-GHz.

The result shows similar behavior as LC-tank oscillator locking phenomena with a slight effect from low pass filter characteristics.

When the injected frequency is low, free-running signal and injected signal coexist, but injected signal has small magnitude. When the injected signal comes closer to free-running frequency, there is Quasi-Locking state at $f_{inj} = 2GHz$ which has same profile as that of LC-tank oscillator. As the frequency gets higher, the oscillation of the ring oscillator tracks the injected signal until the end of locking range. At $f_{inj} = 4GHz$ which is outside of locking range, the ring oscillator is not inject-locked, and stays in the free-running state.

In [32], Hajimiri and his group used signal couplers to inject differential signals to VCOs. In order to verify this simulation result, we also need to use this kind of differential coupling technique or PLL as in Razavi's paper [1]. Differential Injection seems to be more stable injection method, however it requires extra cost of hardware.

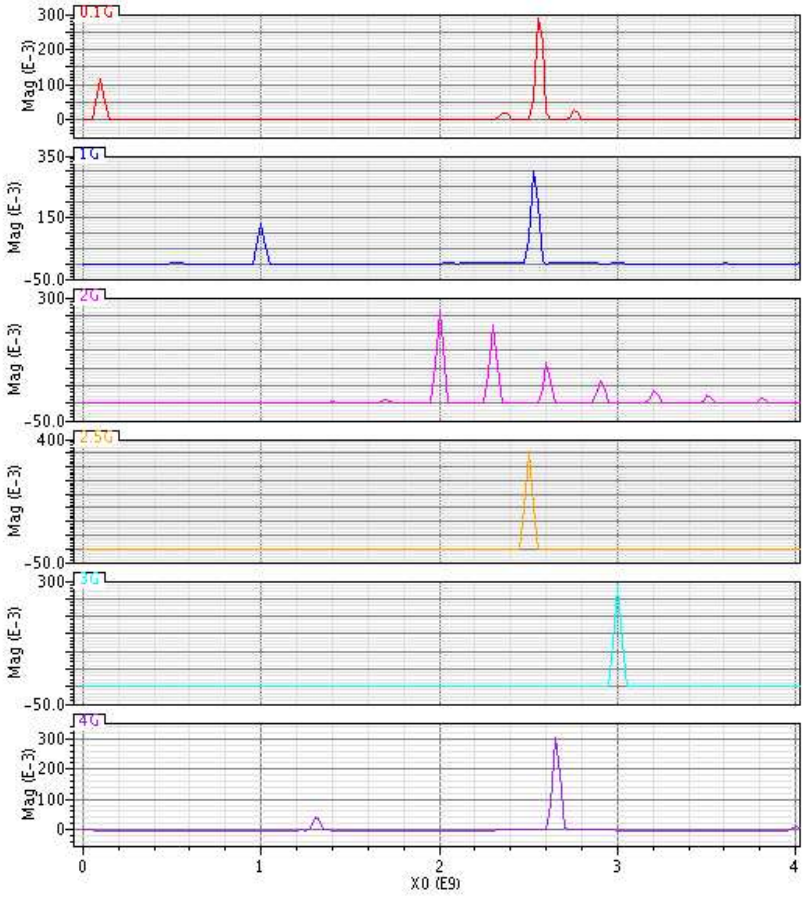
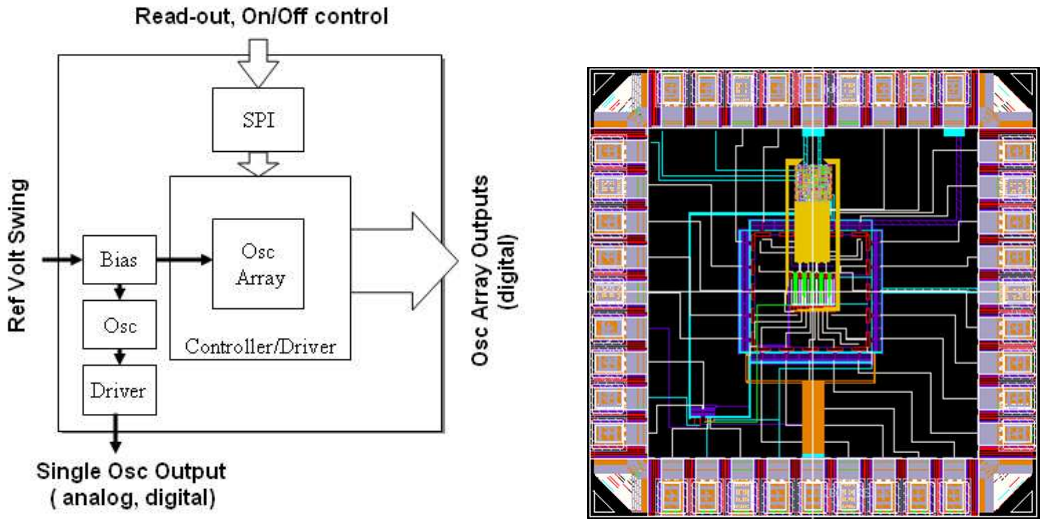


Figure 43: Output Spectrum under Differential Injection

6 Fabricated IC and its Measurement Data

An IC below was fabricated in ST Microelectronics 90nm process to validate ultra low power operation of sub-threshold MCML. The chip consists of a one-hundred oscillator array, current bias circuit, and peripherals.



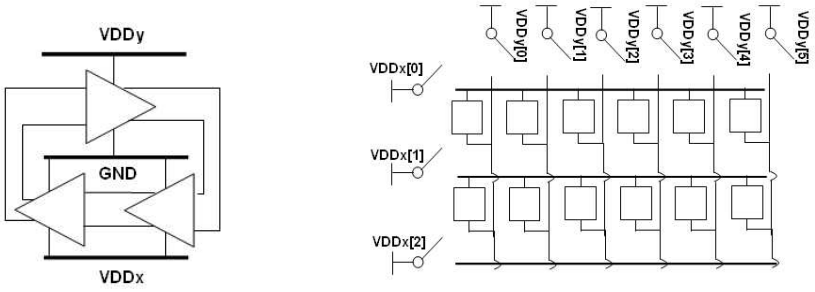
(a) Top System (b) Layout

Figure 44: Fabricated IC, 1mm x 1mm

6.1 One-hundred Oscillator Array

An oscillator consists of three sub-threshold MCML buffers. From [19], three stage ring oscillator was chosen to achieve minimum phase noise. In order to turn on/off and read out selected oscillators, we have

- Two separated VDDs in a ring to turn on/off oscillators (Fig.45)
- Read-out switches between two output buffers to selectively output oscillating signals. (Fig.46)



(a) A Single Ring Oscillator

(b) Row/Column ON/OFF Selector

Figure 45: Oscillator ON/OFF Scheme

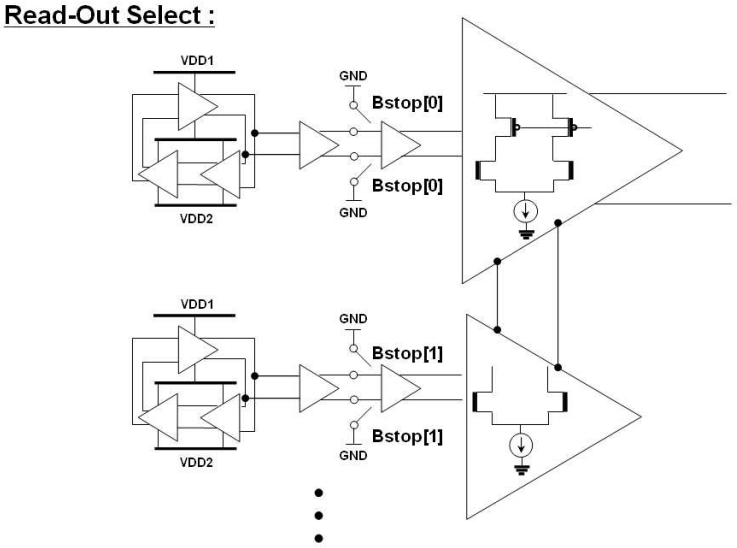
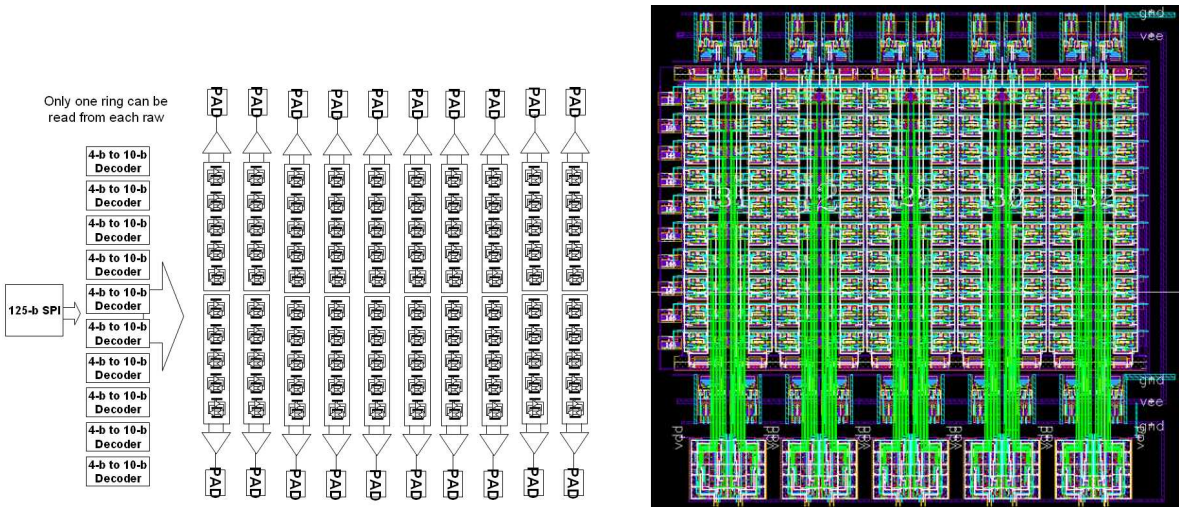


Figure 46: Oscillator Read-Out Scheme

One hundred oscillator with ON/OFF Switches and Read-out Switches was layout into 100um x 100um area. Switches are controlled by the parallel signals sent from SPI (Serial Parallel Interface).



(a) 100 Ring Oscillators with Switches

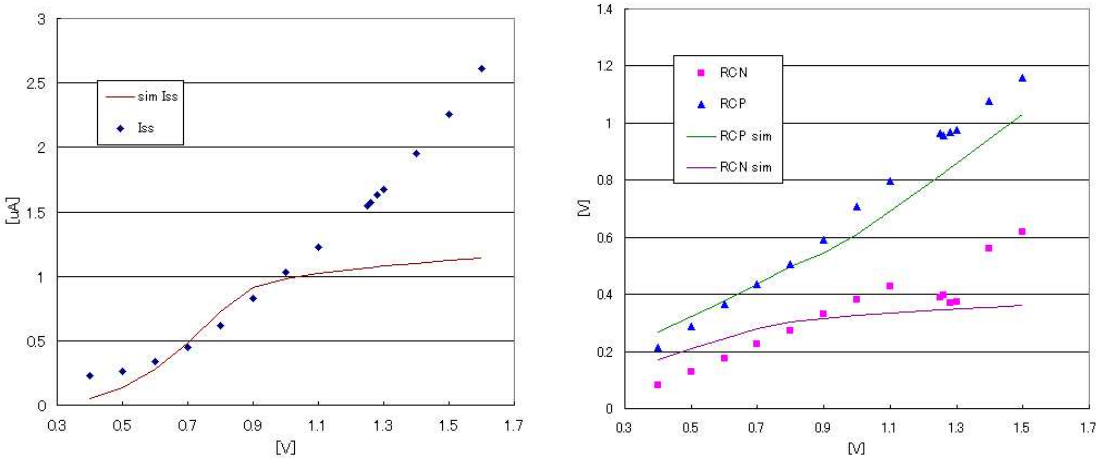
(b) 100 Ring Oscillator Layout, 100um x 100um

Figure 47: Layouts of Oscillators

6.2 Measurement Result

6.2.1 Current Bias Circuit

Bias current I_{ss} was measured for multiple values of VDD, and the data are shown below is compared to simulation results. The measurement data deviated from simulated value after 1V, whereas bias voltage RCP and RCN are mostly following the trend of simulated values.



(a) I_{ss} vs VDD (b) RCN, RCP vs VDD

Figure 48: VDD Dependence of Current Bias Circuit

6.2.2 Single Oscillator

The Output of the single isolated oscillator are taken out as analog output which can be monitored by a spectrum analyzer and as 16-time divided digital output which can be monitored by oscilloscope.

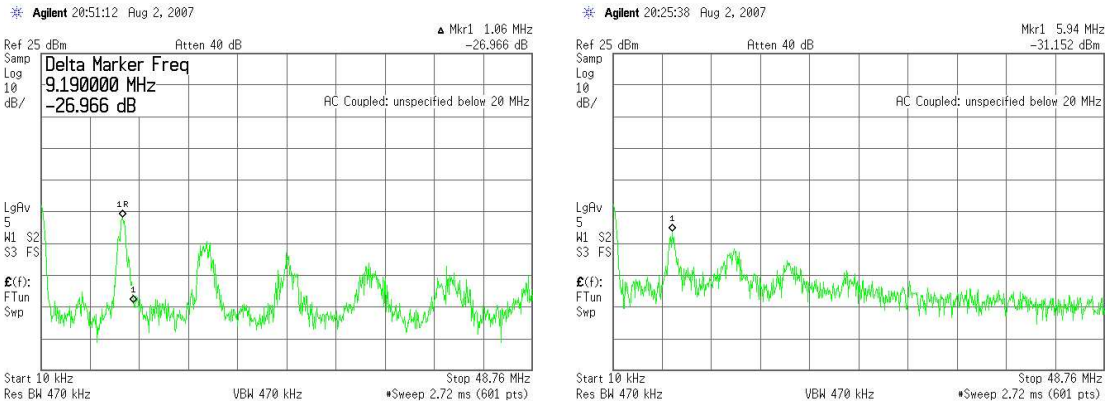
The figure below are showing the analog output spectrum in two different condition. The first one is when only the single oscillator is running and the second one is when some oscillators in the array are running at the same time.

The measured oscillation frequency and phase noise of isolated single oscillator was 9.19MHz at 1MHz offset and -26.96dBc. This result was quite inferior to the post-layout simulation result, 500MHz and -60dBc.

In the second figure, once some oscillators in the array start running, we can see that the single

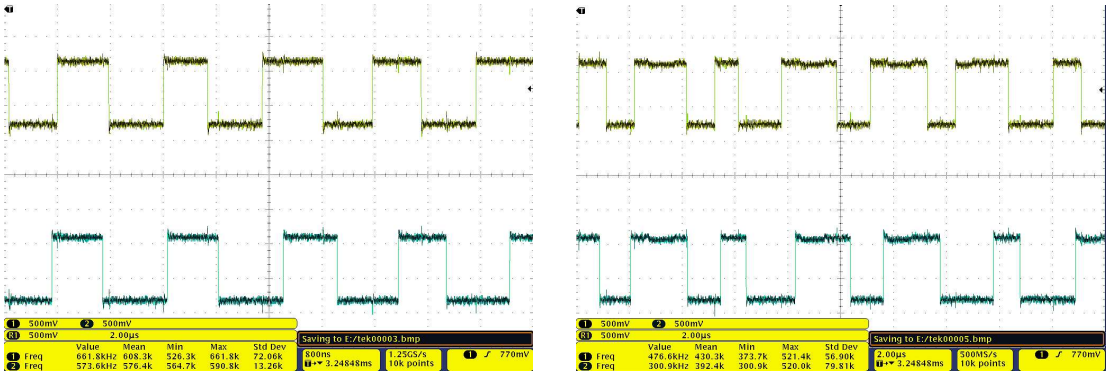
oscillator is perturbed by injected signal from the other oscillators, and its spectrum is about to change. When we turn on more number of oscillators, the spectrum peak disappeared, and the single oscillator stopped working.

From 5.4, we know that ring oscillator cannot be coupled around its free-running frequency, but lower frequency than that. We expected to see the oscillators coupled in low frequency, but we saw the oscillation eventually stopped in this one chip we measured. The measured frequency of



(a) Free Running Oscillator (b) Perturbed Free Running Oscillator

Figure 49: Free Running Oscillator Analog Output



(a) Free Running Oscillator (b) Perturbed Free Running Oscillator

Figure 50: Free Running Oscillator Digital Output

first harmonics with swept current is plotted below. From (53) or (52), we know that frequency should be proportional to bias current I_{ss}, and the result shows this tendency. However, since now our current bias circuit also has linear dependency on VDD as in Fig.48(b), we are not quite sure if this frequency is purely from I_{ss}.

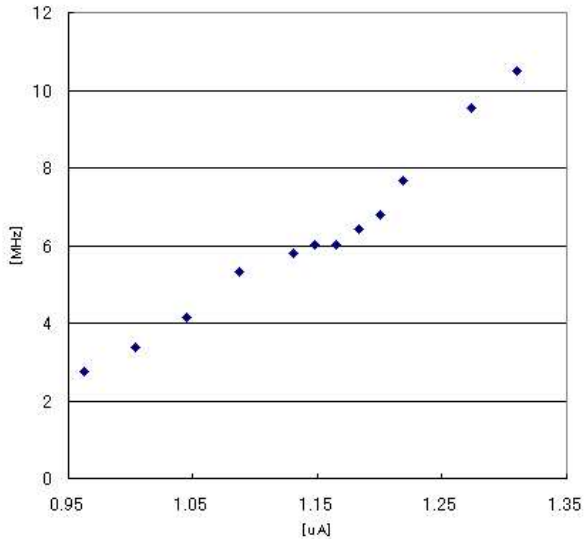


Figure 51: Oscillation Frequency vs Iss

6.2.3 100 Oscillator Array

Due to the mistake in the logic, we could not control the output of oscillator, and we cannot locate the oscillator which is outputting its oscillation signal. However, we can see the variation of frequency over the array.

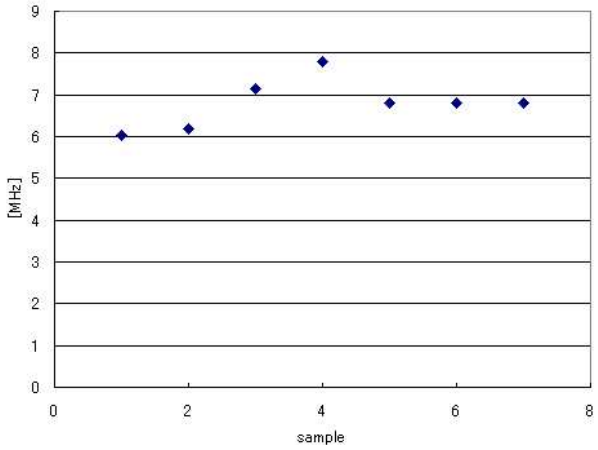


Figure 52: Oscillation Frequency Variation in the Array

7 Conclusions and Future Directions

MOS Current Mode Logic operating in Sub-threshold region was investigated in this research. When we look at Energy Delay Product, this type of logic is superior to CMOS static logic for voltage supply around V_{th}.

The main concern about sub-threshold logic is its high sensitivity to PVT variation.

Feasibility study has been performed by analyzing mismatch/variation effect with newly proposed current bias circuit. Voltage swing of $0.4 - V$ was determined to be large enough to convey logic to the next stage even under process variation/mismatch. This value was double checked by both a proposed nonlinear input-output model and Monte Carlo simulation. Current bias circuit sustains stability of bias current over voltage and temperature, 1.072K ppm/deg and 160K ppm/V, for only 1.25V and 2uA power consumption.

Clock signal generation was selected to show the validity of sub-Vth MCML, and 3-stage ring oscillator was designed and fabricated. Post-layout simulation shows 2GHz oscillation with 26uA current consumption solely in oscillator itself under 1.25-V voltage supply.

As an extended topic of this research, coupling phenomena of oscillators was studied. Phase noise of oscillators were proved to decrease proportionally to the number of oscillators coupling [30]. However, the related researches were all done for LC-tank oscillator. In this research, the locking condition and weakly coupled state were mathematically solved in the same manner as in [1], and the result was verified by Spectre simulation. Ring oscillator shows quite different coupling phenomena compared to LC-tank oscillators, and most notewowrthy fact is that a ring oscillator does not couple to each other around its free-running frequency.

By using ST Microelectronics 90nm CMOS process, current bias circuit, a single oscillator, and 100-oscillator array were fabricated. The measure oscillation frequency and phase noise were 9.19MHz at 1MHz offset and -26.96dBc which were quite inferior to the simulation result.Due to some mistakes in design, some functions of chip are not working, and in order to verify the mathematical calculations we have done, remake of the design is necessary.

In this research, we looked into ultra low power logic, and theoretically we showed its potential, and hopefully this category of research will be continued in the future.

Appendix A: General Solution [3]

We want to evaluate

$$\int \frac{d\theta}{a + b\sin\theta} \tag{90}$$

where $a = \omega_0 - \omega_{inj}$ and $b = -\omega_L$.

Remember that, by definition of $\sec\theta$

$$\frac{1}{\cos\theta} = \sec\theta \tag{91}$$

Now, first fact we require is

$$1 + \tan^2\frac{\theta}{2} = \frac{1}{\cos^2\frac{\theta}{2}} = \sec^2\frac{\theta}{2} \tag{92}$$

Second fact we require is

$$\frac{d}{d\theta}\tan\frac{\theta}{2} = -\frac{1}{2\cos^2\frac{\theta}{2}} = -\frac{1}{2}\sec^2\frac{\theta}{2} \tag{93}$$

Looking back at (90), we write it down as follows

$$\begin{aligned}
\int \frac{d\theta}{a + b\sin\theta} &= \int \frac{d\theta}{a + \frac{2b\tan\frac{\theta}{2}}{1+\tan^2\frac{\theta}{2}}} \\
&= \int \frac{d\theta(1+\tan^2\frac{\theta}{2})}{a(1+\tan^2\frac{\theta}{2}) + 2b\tan\frac{\theta}{2}} \\
&= \int \frac{d\theta\sec^2\frac{\theta}{2}}{a(1+\tan^2\frac{\theta}{2}) + 2b\tan\frac{\theta}{2}}
\end{aligned}$$

Now substituting $x = \tan\frac{\theta}{2}$,

$$dx = -\frac{1}{2}\sec^2\frac{\theta}{2}d\theta \tag{94}$$

Therefore,

$$\begin{aligned}
\int \frac{d\theta}{a + b\sin\theta} &= \int \frac{-2dx}{a(1+x^2) + 2bx} \\
&= \frac{-2}{a}\int \frac{dx}{\left(x + \frac{b}{a}\right)^2 + 1 - \frac{b^2}{a^2}}
\end{aligned}$$

Now we need another fact

$$\int \frac{dx}{x^2 + k^2} = \frac{1}{k}\tan^{-1}(x/k) \tag{95}$$

[3] This calculation is by courtesy of Pulkit Grover, pulkit@eecs.berkeley.edu

Therefore,

$$\int \frac{d\theta}{a + b\sin\theta} = \frac{-2}{a} \frac{1}{\sqrt{1 - \frac{b^2}{a^2}}} \tan^{-1} \frac{x + \frac{b}{a}}{\sqrt{1 - \frac{b^2}{a^2}}}$$

Now substitute $x = \tan\frac{\theta}{2}$.

$$t = \frac{-2}{\sqrt{a^2 - b^2}} \tan^{-1} \frac{\tan\frac{\theta}{2} + \frac{b}{a}}{\sqrt{1 - \frac{b^2}{a^2}}}$$

Therefore,

$$\sqrt{1 - \frac{b^2}{a^2}} \tan\left(\frac{-\sqrt{a^2 - b^2}}{2} t\right) = \tan\frac{\theta}{2} + \frac{b}{a}$$

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