Microwave and mm-Wave CMOS Low Noise Amplifiers

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Technical Report No. UCB/EECS-2007-160
http://www.eecs.berkeley.edu/Pubs/TechRpts/2007/EECS-2007-160.html

December 18, 2007

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Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

Figure 1.1: Deployment of wireless communication systems.

In wireless communication systems, information is transferred between two points without a direct conductive connection. While this can be done employing

sound, infrared, optical or radio frequency energy, most modern systems exploit RF, microwave or millimeter wave signals. The demand for higher data rates and spectrum crowding resulted in movement to higher frequency bands.

At present wireless systems include broadcast radio and television, cellular telephone system, direct broadcast satellite(DBS) television service, wireless local area network(WLAN), pagers, global positioning satellite(GPS) service, and radio frequency identification(RFID) systems. Each system has its particular requirements. For example in satellite receivers sensitivity is the most important factor whereas in an RFID system achieving a very low power RFID tag is the main goal.

There are different methods to categorize a wireless communication system based on the characteristic under study. According to the number and placement of users, wireless systems could be categorized as point to point, point to multipoint, or multipoint to multipoint systems. Whereas according to the directionality of communication they could be classified as simplex, half-duplex, or full-duplex systems. In simplex systems such as broadcast radio and television, communication occurs in only one direction. An Example of half-duplex system is early push-to-talk mobile radios where the same channel was used for transmitting and receiving the data but at different time intervals. Full-duplex systems provide simultaneous two-way data

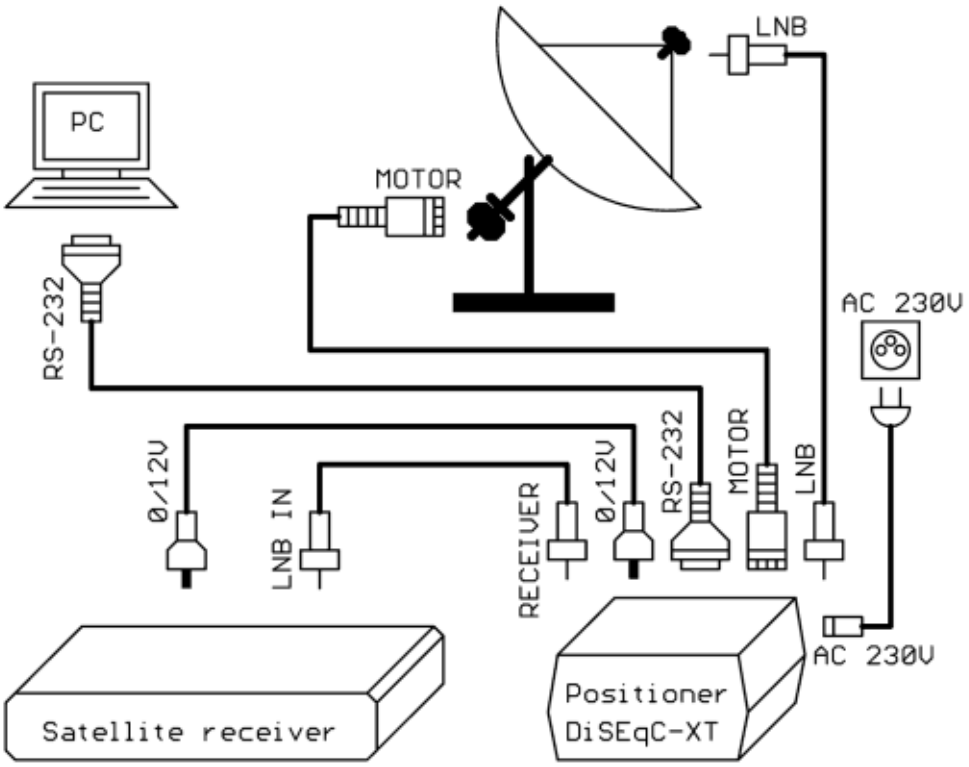


Figure 1.2: A complete satellite receiver system.

transmission and reception with the aid of duplexing techniques such as frequency division duplexing(FDD) or time division duplexing(TDD).

Most wireless systems are ground based, but there is also interest in the satellite systems for voice, video, and data communications. Satellite systems have the advantage of covering a large area and maintaining communication with a large

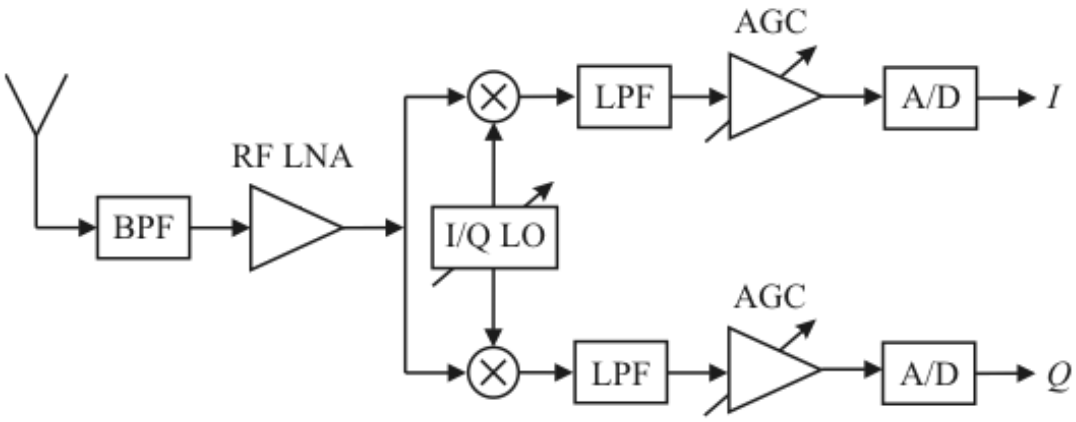


Figure 1.3: Example of a direct conversion receiver.

number of users regardless of whether they are in rural or urban areas. On the other hand, due to the large distance of satellites from Earth's surface, the received signal is very weak. Detection of this weak signal poses strict requirements on the sensitivity of the receiver and directivity of the receiving antenna.

In the satellite communication system, receiver is a very critical block and is responsible for recovering the transmitted data out of the weak received signal that is accompanied by noise and interference. The receiver should have a huge

gain(∼100dB)and a small noise figure(∼1-2dB) to restore the low power of received signal while adding minimal noise. It selects the desired signal while rejecting adjacent channels, image frequencies, and interference, and then down-converts it to an IF frequency for further detection and demodulation.

According to The Friis equation [2]:

$$P_r = \frac{G_t G_r \lambda^2}{(4\Pi R)^2} P_t \tag{1.1}$$

received power is proportional to antenna gains(G_t, G_r) and inverse-square of the distance($1/R^2$). Due to the large R, the power level is very low and therefore a high gain antenna is designed for the receiver to partially make up for that (Fig.1.2). Since all interconnections have considerable loss at high frequency, and degrade the signal quality directly a low noise block(LNB) is placed as close as possible to the antenna (Fig.1.2) to boost the signal without adding substantial noise to it and further down-converts the high frequency RF signal to a lower IF or baseband signal. This lower frequency signal could be routed to the next stage of receiver by transmission lines without any significant effect on the signal quality due to operating at frequencies where low loss transmission lines and interconnects are easily feasible.

The receive architecture could be a superheterodyne or a direct conversion

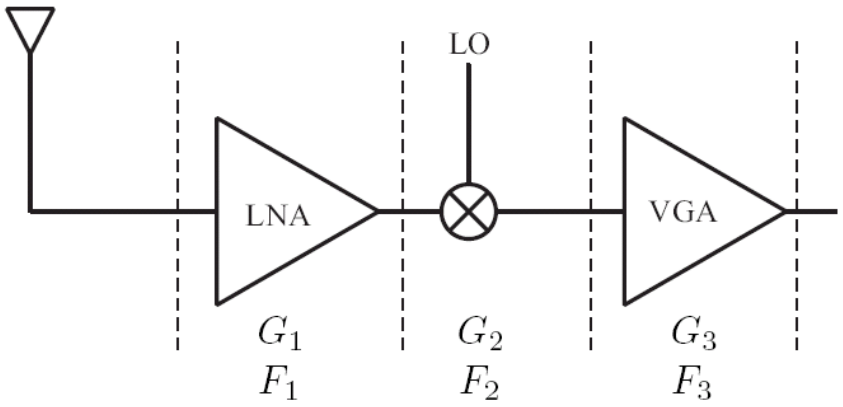


Figure 1.4: In a well designed system, total noise performance is dominated by LNA noise performance

receiver depending on the system requirements and available technology. A direct conversion receiver is depicted in Fig.1.3 and consists of a band pass filter(BPF) which is usually a high-Q, low insertion-loss off-chip filter, a low noise amplifier(LNA), I/Q mixers, baseband filtering, variable gain, and analog to digital conversion. Since a satellite receiver should be highly sensitive and able to detect signals that are almost buried in noise, total noise figure of the receiver is an important specifications and should be as low as possible. Noise factor for a cascade of three blocks in the receive

chain as shown in Fig.1.4 will be (assuming interstage matching) [3] :

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} \tag{1.2}$$

So the noise performance of the receiver will be set mainly by LNA. To make the minimum detectable signal as small as possible, LNA should have as low noise figure as possible.

To meet this requirement, traditionally microwave and mm-wave LNAs were designed in advanced and more expensive III-V technologies. Compared to CMOS These technologies offer higher performance transistors, and their nearly insulating substrate, provides high quality passive components. However since many satellite receiver applications are commercial (such as broadcasting and entertainment), having a single-chip solution in highly integrable and low-cost CMOS technology is desirable. High speed CMOS transistors that have emerged in the past decade as a result of technology scaling, enabled CMOS high frequency circuit design. In this thesis we show that even in areas such as satellite receivers where very low noise figure is an important metric, CMOS technology can be used.

In this thesis we discuss CMOS low noise amplifier(LNA) design for microwave and mm-Wave frequency bands. Two LNAs were designed, fabricated and

tested in X-band and K_a band respectively. Circuit design method of the X-band LNA is more similar to RF circuit design techniques where lumped elements are employed for matching networks whereas in K_a-band, transmission-line type of matching networks were exploited. Since noise figure(NF) is an important metric for a satellite receiver, and is dominated by NF of the LNA, it's a very important factor which will be carefully addressed along with approaches devised to lower it as much as possible. In the X-band LNA, design of a new input matching network is proposed that obviates the need of the gate inductance. The gate inductance is an important noise contributor since due to its finite quality factor, a resistance appears in series with (R_S), adding directly to the noise of the system. In the K_a-band LNA design using a new layout approach for a transistor is adopted which minimizes the noisy parasitics and increases its f_{max} considerably. Other performance characteristics such as input and output match, large signal and distortion specifications, power and area consumption will also be discussed.

Chapter 2

X-band CMOS Low Noise Amplifier with Capacitive Feedback Matching

2.1 Motivation

To date most microwave and RF CMOS amplifiers have been implemented as open-loop amplifiers due to the limited gain at radio frequencies and stability concerns due to phase shift through the transistor close to the device transit frequency(f_t). Deeply scaled CMOS transistors have tens of gigahertz of f_t and f_{max}(maximum os-

cillation frequency), enabling operation at multi-gigahertz regime using conventional analog techniques such as feedback.

In this chapter we present a capacitive shunt feedback amplifier topology which can achieve very low noise figure and offers a method to impedance match the amplifier. As a demonstration vehicle, a prototype is designed for the X-band(9GHz). Surprisingly relatively few publications have reported operation in this frequency band, although the device f_t is certainly large enough to enable operation in this frequency range. There are interesting applications for operation in these bands, including satellite communications, radio astronomy, space research, and weather radars. Most of these applications call for extremely low noise operation, beyond the capability of CMOS technology. On the other hand, CMOS offers high levels of integration and small footprint receivers. An external single device (GaAs, InP) LNA with modest gain followed by a CMOS downconverter is an attractive option. This relaxes the noise requirement on the CMOS LNA but to achieve sub-1dB overall noise figure still requires an LNA with NF below 3dB.

Despite the high operating frequency, the wavelength is still too large to allow on-chip transmission-line based designs, which means we must employ lumped passive components design. A conventional CMOS LNA is an inductively degenerated

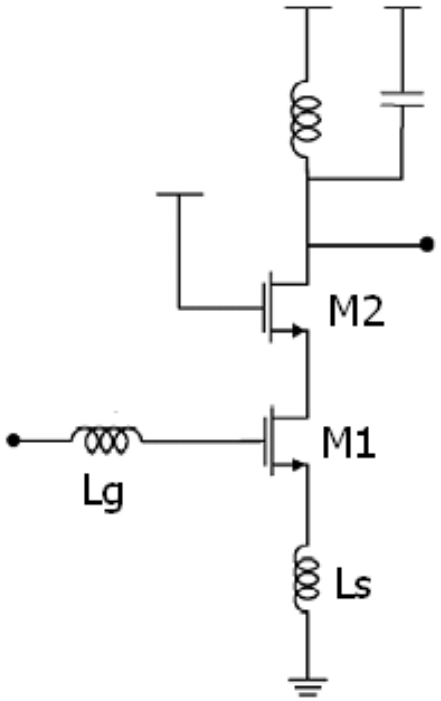


Figure 2.1: Conventional inductively degenerated cascode amplifier.

cascode amplifier that has series inductors both in its source and gate with a tuned load at its output (Fig. 2.1). The input impedance is $L_s \cdot \omega_t$ with $L_s + L_g$ resonated out by the C_{gs} of the device at the desired frequency. By moving to a better technology and scaling down the transistors, we get higher ω_t and smaller ω/ω_t which means that noise contribution from transistor will be very small. In this situation passive

components will have the main contribution in the overall noise performance of the amplifier. Since L_g is in series with the amplifier input, its series resistance due to the finite inductor quality factor will be directly added to the equivalent input noise resistance. This parasitic resistance will be the dominating factor in determining the NF of very low noise amplifiers. The noise factor of this amplifier is

$$F = 1 + \frac{R_{L_g}}{R_S} + \frac{R_g}{R_S} + \gamma g_{do} R_S \left(\frac{\omega}{\omega_t}\right)^2 \tag{2.1}$$

where R_g is the gate resistance of the FET, which is lower bounded by the channel induced gate resistance ($R_g > 1/(5g_m)$). The short-channel excess noise factor γ is bias dependent but measurements show that it ranges between 1-2. For long channel transistors $g_{d0} \approx g_m$, whereas a factor α is usually used to account for the difference for short channel devices $g_{d0} = g_m/\alpha$.

Assume that we are operating at 10 GHz while f_t=100 GHz and that we are minimizing the transistor noise contribution with g_m=40 mS and C_{gs}=64 fF. The required inductances will be L_s=80 pH and $L_g \simeq 4$ nH. This value of L_g is rather high for operating at 10 GHz. Its layout should be done carefully to have a self resonance frequency reasonably higher than 10 GHz. Even then by assuming Q =10, it will have 25Ω of series resistance, which contributes adversely to the noise factor and has

the main contribution

$$F \approx 1 + \frac{25}{50} + \frac{1}{10} + \frac{2\gamma}{100} \tag{2.2}$$

For applications such as satellite receivers that require a very low noise figure, a lot of current is consumed in the first stage to decrease the transistor noise as much as possible. In this case the resistance due to the finite Q of L_g becomes dominant and limits the minimum achievable NF. In the next section we present an input matching mechanism that obviates this inductor at the gate by providing matching through shunt capacitive feedback. Later sections discuss low noise amplifier circuit design based on the presented technique along with measurement results of the fabricated prototype.

2.2 Capacitive feedback matching network

Due to the scaling of CMOS technology, we have quite a bit of excess gain that can be traded-off for matching and linearity through feedback. There are two shunt-shunt feedback mechanisms shown in Fig. 2.2. The left structure uses a resistor to sense the output voltage, convert it to a current($I = \frac{V}{R}$), and compare it with the input current. The same thing is done in the right structure by means of a capacitor where the fed back current is ($I = -j\omega C_f V$).

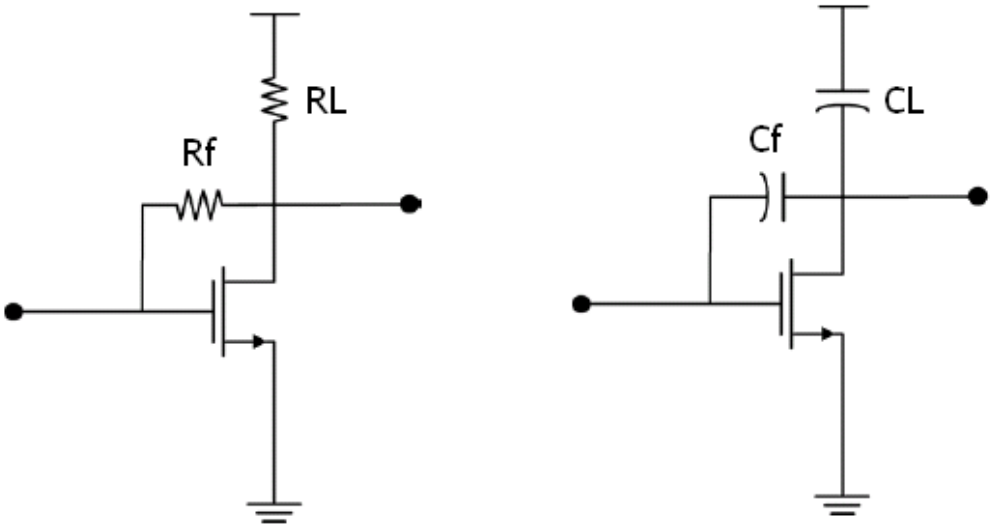


Figure 2.2: Shunt-shunt feedback structure.

Conventional resistive shunt-shunt feedback is not desirable since it adds noise to the LNA input unless the resistor is very large, which lowers the output pole and poses bandwidth limitations. But the same feedback structure with capacitive components can provide the desired input impedance without adding any extra noise. Technology scaling results in an increase in the ratio of C_{gd}/C_{gs} (in 130nm this ratio is around 0.5) so the intrinsic C_{gd} of the device can be used for the feedback network if

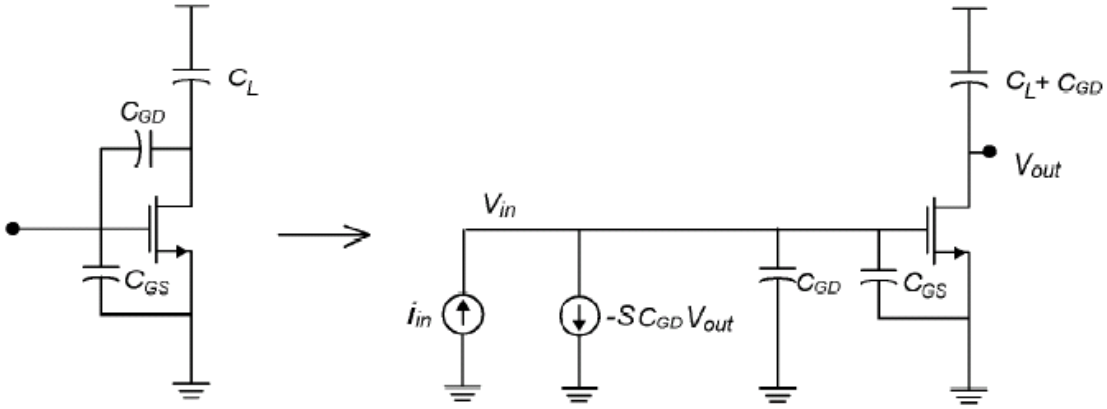


Figure 2.3: Capacitive feedback amplifier equivalent circuit.

a single transistor amplifier is incorporated instead of a cascode amplifier. Intentional feedback MIM or finger capacitors can also be added to make the circuit more robust and less prone to process variation.

The core circuit is shown in Fig. 2.3, Since there is no series L_g at the gate, the contribution of noise from series resistance of this finite-Q inductor is eliminated. Moreover the single transistor amplifier has lower noise compared to a cascode amplifier topology. This is because there is a middle node at the cascode structure (drain of M1 and source of M2 in Fig.2.1) and the pole associated with it tends to shunt

this node to ground at high frequencies. Therefore the current noise of M2 no longer completely circulates in itself and part of it finds a path to appear at the output node.

In the feedback amplifier depicted in Fig.2.3 C_{gd} senses the output voltage and subtracts the current $i_f = f \cdot v_o = -sC_{gd} \cdot v_o$ from the input current. The open loop gain is given by

$$a = \frac{v_o}{i_{in}} = \frac{-g_m}{s(C_{gs} + C_{gd})} \cdot \frac{1}{s(C_L + C_{gd})} \tag{2.3}$$

and the open loop input impedance is approximately

$$Z_i = \frac{1}{s(C_{gs} + C_{gd})} \tag{2.4}$$

The loop gain is given by

$$T = a \cdot f = \frac{g_m}{j\omega(C_{gs} + C_{gd})} \cdot \frac{C_{gd}}{C_{gd} + C_L} = \frac{\omega_t}{j\omega} \cdot \frac{C_{gd}}{C_{gd} + C_L} \tag{2.5}$$

where $\omega_t = \frac{g_m}{C_{gs}+C_{gd}}$. If $|T| \gg 1$ then we have

$$Z_{in} \approx \frac{1}{g_m} \cdot (1 + C_L/C_{gd}) \tag{2.6}$$

and under a source impedance match condition ($Z_{in} = R_s$)

$$A = \frac{v_o}{i_{in}} \approx \frac{-1}{j\omega \cdot C_{gd}} \Rightarrow A_V = \frac{v_o}{v_{in}} \approx \frac{j}{2R_s\omega C_{gd}} \tag{2.7}$$

which could be quite high in today's CMOS technology where the transit frequency is much higher then the operating frequency of many applications.

The open loop input impedance is capacitive but since there is a $-90°$ phase shift in the loop gain, the closed loop input impedance turns out to be resistive. At frequencies close to f_t where $|T|$ is not much larger than unity, the impedance should be divided by $(1+T)$ and then the capacitive term of Z_{in} will become comparable to the real part, degrading the input return loss. Although the input impedance seems to be independent of frequency, the gain varies with frequency and this structure is mostly suitable for tuned amplifiers.

It is easy to verify that the noise factor of the amplifier is the same as Eq. (2.1) with $R_{L_g} = 0$. And according to Eq. (2.1) eliminating R_{L_g} will have a substantial effect on decreasing the NF and pushing it it to its limit in a very low noise amplifier.

2.3 Amplifier Design

The proposed amplifier employs a capacitive load. One way to realize the load capacitor is to connect the drain to the supply rail through a large resistor or a choke inductor. In this case, the output impedance is effectively composed of C_{db} of the transistor and the loading capacitance of next stage. This is a simple and stable way in realizing the amplifier. The downside is that a large C_L degrades the loop gain and also needs a corresponding large g_m to drive it, or on the other hand the operating frequency should be lowered.

Alternatively, a part of this capacitance could be resonated out to achieve the desired $C_{L_{eff}}$ at the output, allowing operation at a higher frequency. In other words, an off-center tuned load should be connected to the output. By operating $\Delta\omega$ above the tank resonance frequency ω_0, the tank looks like a capacitor and the effective capacitance could be found as :

$$Z_{tank}\ (\omega = \omega_0 + \Delta\omega) \ = \ \frac{1}{j\omega C_{L_{eff}}} \tag{2.8}$$

$$j\omega C_{L_{eff}} \ = \ j\omega C + \frac{1}{j\omega L} \ \ \Rightarrow \ \ C_{L_{eff}} \ = \ C - \frac{1}{\omega^2 L} \tag{2.9}$$

$$C_{L_{eff}} \ = \ C(1 - \frac{\omega_0^2}{\omega^2}) \ \ \approx \ \ 2\frac{\Delta\omega}{\omega} \cdot C \tag{2.10}$$

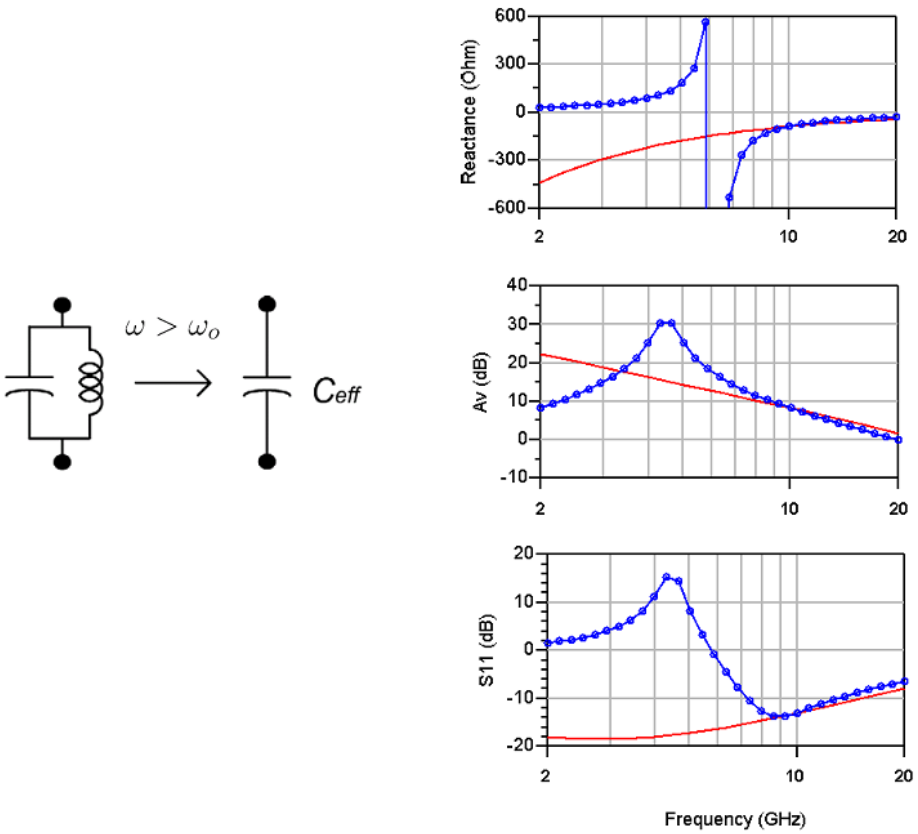


Figure 2.4: A comparison of the output reactance (top), voltage gain (middle) and input match (bottom) between the capacitive load (-) and off-tuned tank (∘). The circuits utilize the same reactance as capacitive load at 9 GHz.

This strategy requires care since below the center frequency of the load tank the impedance is inductive, there is +90° phase shift in the loop gain and this produces a negative real input impedance through feedback; which is capable of producing oscillation. The situation is depicted in Fig. 2.4 where a comparison is made between two cases. The first case assumes that the output capacitance is as small as desired

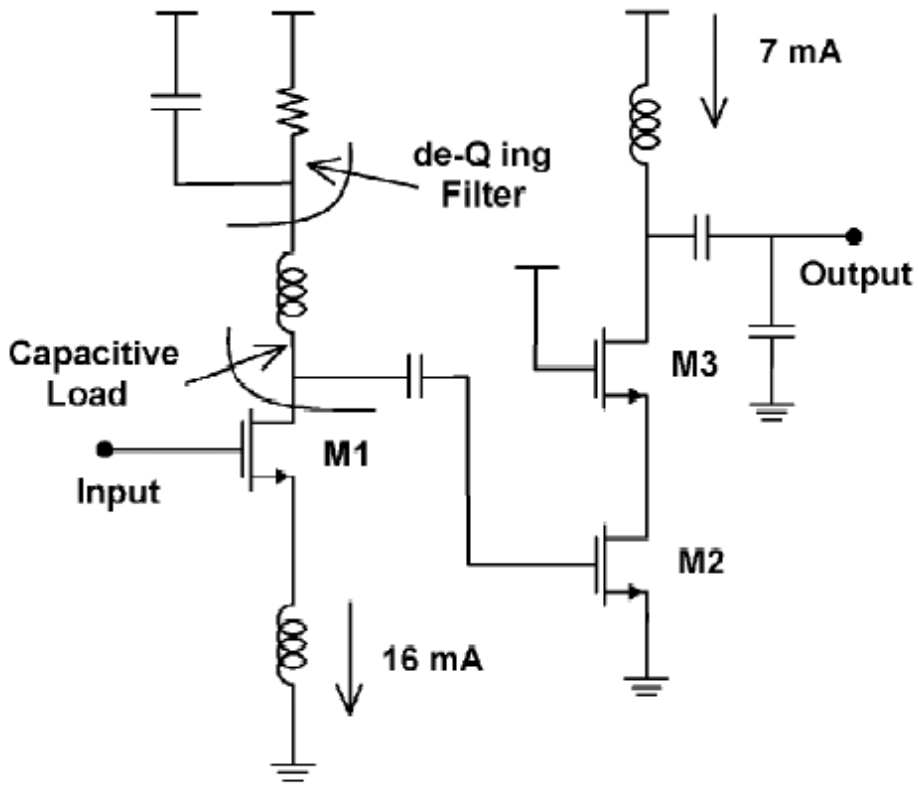


Figure 2.5: Complete schematic of the two stage prototype LNA.

and a large resistor connects the drain to V_{DD}. In the second case the output capacitance is large and some of it is resonated out, therefore a tank centered at 6.4 GHz is placed at the output to have the same reactance as that of the desired capacitance at 9 GHz. Below the center frequency of the tank, the real part of input impedance becomes negative, or equivalently S_{11} is greater than unity and peaks at 4.5GHz.

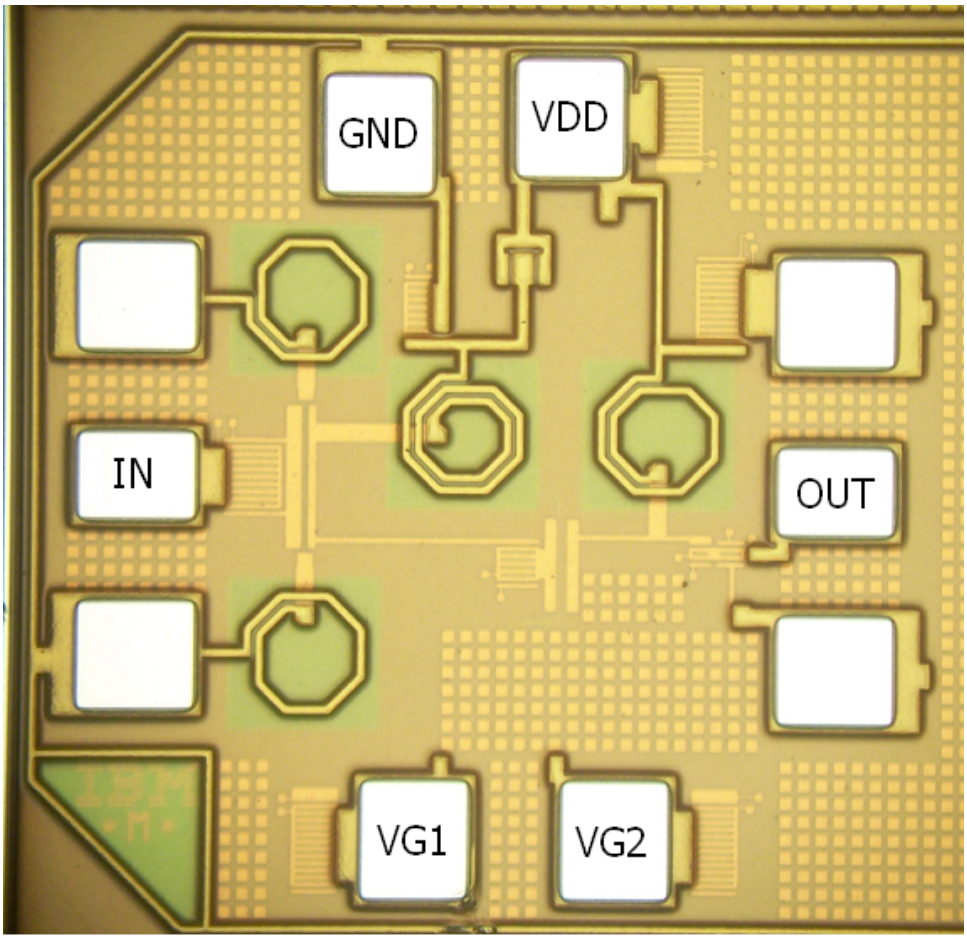


Figure 2.6: Die photo of the prototype amplifier fabricated in 130nm CMOS technology.

To solve the instability problem, the tank Q should be lowered at that frequency so that the loop gain is small enough to quench any oscillation. This is easily done with a resistor in series with the inductor at the output of the first stage (Fig. 2.5). Since this resistor is detrimental for the tank-Q at the operating frequency, it is bypassed with a capacitor in such a way that the $1/(2\pi RC)$ pole lies in the mid-

range between these two frequencies. Because these two frequencies are not far apart, a first order RC filter does not provide enough stability margin so a small inductance at the source of the transistor produces a real part $\omega_t L$ that further prohibits oscillation. Note that this inductance is small enough (its reactance $X_L = \omega L$ is negligible compared to $\frac{1}{g_m}$) not to disturb the capacitive feedback analysis done in the previous section for calculating input matching and gain .

In this design, two small inductors were placed in parallel in order to make the inductance even smaller and to also produce a symmetric ground return path for the inductor current to make the inductance value more predictable (Fig. 2.6). The measured S-parameters shown in Fig. 2.7 confirms the stability and the desired behavior of the overall circuit (S11 doesn't go beyond 0dB).

The complete schematic of the amplifier is shown in the Fig. 2.5. The first stage is composed of a single transistor incorporating C_{gd} as capacitive feedback for the input match. The load tank is off-tuned so its impedance is effectively capacitive and also a first order RC filter is incorporated to de-Q the tank and prevent parasitic oscillations below the tank center frequency. As discussed previously, a small inductance is also added to the source to increase the real part of input impedance at the problematic frequencies. The second stage is a conventional cascode amplifier that

improves the gain and reverse isolation.

2.4 Experimental Results

The chip was fabricated in IBM's CMOS $0.13\mu m$ 8RF process. The chip die photo, shown in Fig. 2.6, occupies an area of $0.64mm^2 = 800\mu m \times 800\mu m$. This amplifier draws 23mA from a 1.2V supply voltage. 16mA of this current is burned in the first stage while the second stage consumes 7mA.

Measurements were taken directly using wafer probes. The measured S-parameters are shown in Fig. 3.9. The amplifier has a peak gain of 20.5 dB at 8.8 GHz and 3-dB bandwidth of 1.4 GHz. The amplifier is well matched (S_{11} of -15 dB at the center frequency). This good S11 confirms the validity of capacitive feedback method for matching the LNA input to 50Ω .

The NF of the amplifier was measured to be below 2 dB across the band as depicted in Fig. 2.8 and it reaches its minimum of 1.7dB at the center frequency, which is a record for CMOS LNAs operating at these high frequencies. The noise was measured using the HP-8970B Noise Figure Meter. Cable losses were de-embedded from noise measurements using an on-wafer "thru" measurement. This low noise figure shows a good promise for CMOS LNA design in satellite receiver systems and

is the first step towards having a single chip solution for commercial satellite receiver applications where the cost is a significant issue.

The large signal and distortion measurements verify -2 dBm of output power at the 1-dB compression point (input $P_{-1dB} = -21$ dBm at 9GHz). Although feedback improves the linearity of an amplifier, in a two stage amplifier the linearity performance is mostly determined by the second stage (which has a larger signal at its input), using feedback at the first stage doesn't help the linearity that much. Furthermore, since the input signal level is very low($\sim$ -100dBm) in a satellite receiver, this amplifier has enough linearity to deal with such a signal.

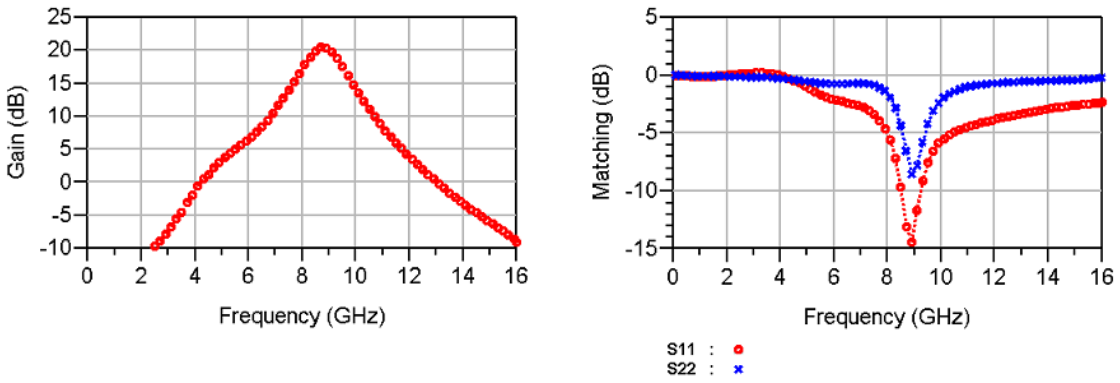


Figure 2.7: Measured S-parameters of the LNA.

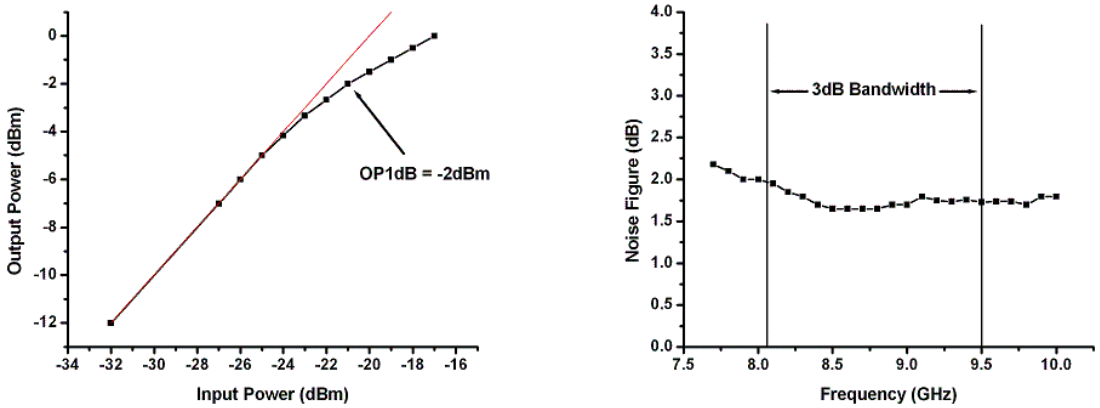


Figure 2.8: Measured linearity and noise figure.

Chapter 3

A K_a Band CMOS Low Noise Amplifier

3.1 Background

In the past, mm-wave circuits were fabricated with high performance and expensive compound semiconductor technologies because of their better electron mobility, higher breakdown voltage, and nearly insulating substrate. With today's scaled CMOS transistors having f_t and f_{max} exceeding 100 GHz, operating at tens of gigahertz frequency range with relatively inexpensive and highly integrable standard CMOS process is possible [15]-[23]. In this chapter we demonstrate an LNA operat-

ing at 30 GHz with performance comparable to or better than amplifiers designed in other more advanced technologies.

There are some major disadvantages in employing a digital CMOS process at mm-wave frequency range. Transistors have lower available gain at the desired band, so there is less room for modeling errors and mismatches. Moreover, the conductive substrate adds parasitic losses, which complicates the active and passive device modeling. Metal layers are relatively thin and in close proximity to the conductive substrate. Compared to insulating substrates, quality factors for matching elements, interconnects, and resonators are lower. Furthermore, the proximity to the substrate increases the capacitive coupling and lowers the self resonance frequency of passive devices.

Since we are operating at the frequency limits of the transistors, careful design requires incorporation of losses and parasitic effects in active and passive devices. This requires a dual approach to design which includes device and layout optimization besides circuit design. In the next section component design and methods to achieve better performance will be discussed. Later sections focus on the low noise amplifier circuit design and its measurement results along with comparisons to simulations.

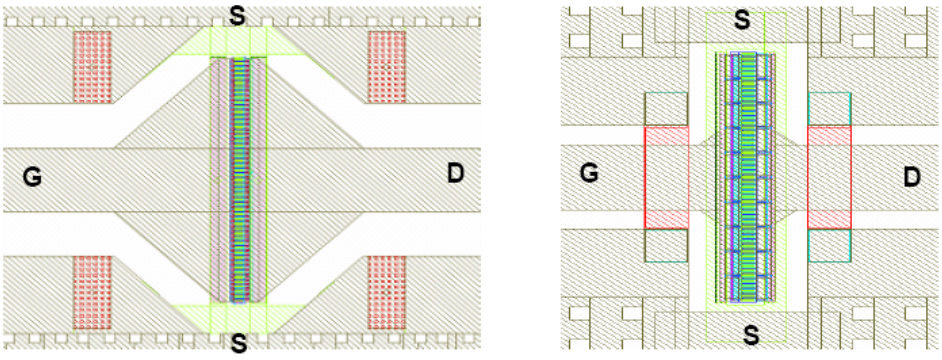


Figure 3.1: Two identical transistors with different taper structures providing connections between signal lines and transistor terminals.

3.2 mm-Wave Components

To show the importance of careful mm-wave layout and component design, layout of two identical transistors just with different tapers connected to their gate and drain terminals are shown in Fig. 3.1. At the first glance it might seem that the left one is better because it's wider and should have less resistance. But it should be noted that at 30GHz the skin depth is just a fraction of a micron, much less than the 10μm width of the line bringing in the signal, so almost all the current is flowing on

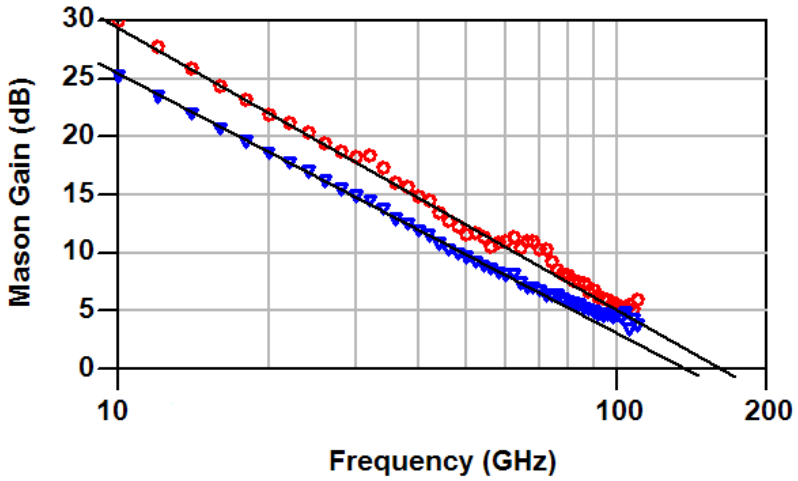


Figure 3.2: Measured Mason gain of the two transistors depicted in Fig. 3.1. The right structure in Fig. 3.1 has higher F_{max} as a result of lower series gate resistance.

the edges. Therefore for the left one the signal reaches the transistor from two sides. To go all the way down to the gate poly current chooses the path with minimum impedance $(R + j\omega L)$ which is determined by L at high frequencies. Inductance is proportional to the area enclosed by the current and return current paths. To minimize the inductance, the current path won't spread along the transistor width but instead it stays in close proximity to its return path at the two sides of the transistor. So among all those vias along the transistor width, current chooses just a few vias on the sides to go down from the top metal to gate poly. The effective series resistance will be the parallel equivalent of these few vias that pass the current

through and could be rather high since not all the vias are contributing in the current flow to the gate. Although this path has less impedance because it's less inductive but it has more loss due to its high resistance.

On the other hand for the structure on the right of Fig. 3.1, current will be distributed more evenly and uses more vias in parallel to reach down the gate poly. As a result the series taper resistance which will be in series with the overall gate resistance for the right structure is less than the left one. This added gate resistance can be harmful for f_{max} and NF_{min}. Measurement confirms this argument by showing f_{max} of 175GHz for the right structure, 30GHz more than that of the left one (Fig. 3.2).

Now that we found out that layout parasitics at 30GHz are comparable to the device parasitics and ignoring them could be detrimental to their performance, we try to come up with new ideas to improve the layout as much as possible.

By contacting the gate fingers from both sides, the distributed gate poly resistance decreases by a factor of four [4]. Being aware of this fact and also knowing that the closer the substrate guard ring is placed to the device the less substrate added noisy parasitics exist, we have reached the conclusion that we should divide the total device into pieces, each of them called a unit cell. Each unit cell has gate

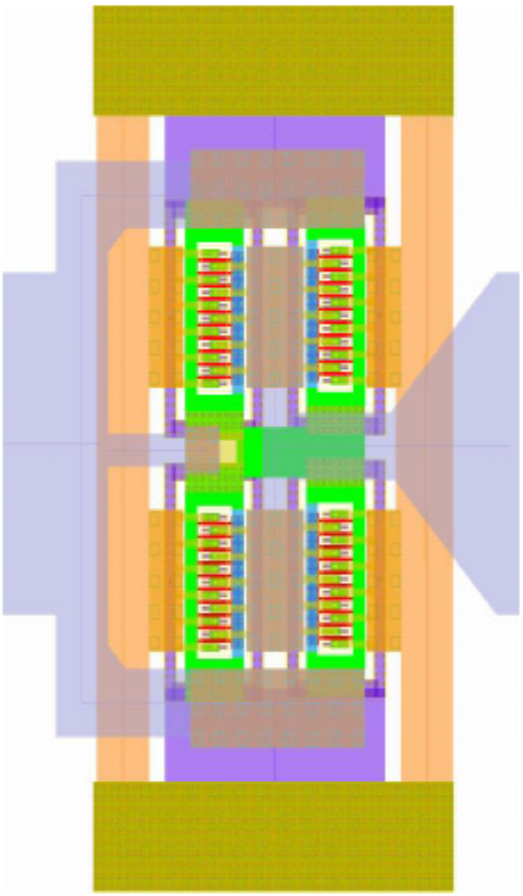


Figure 3.3: Four $10\mu m$ wide transistors placed in a 2×2 matrix structure to form a $40\mu m$ round-table transistor .

contacts on both sides and is located inside its own substrate guard ring. The next step is to connect these unit cells in such a way that they are as close as possible to each other and also we should make sure to provide multi paths for gate, source and drain lines to be able to parallelize and lower their associated parasitic resistances. Four 10μm wide (w=10μm) unit cell transistors placed in a matrix to comprise a

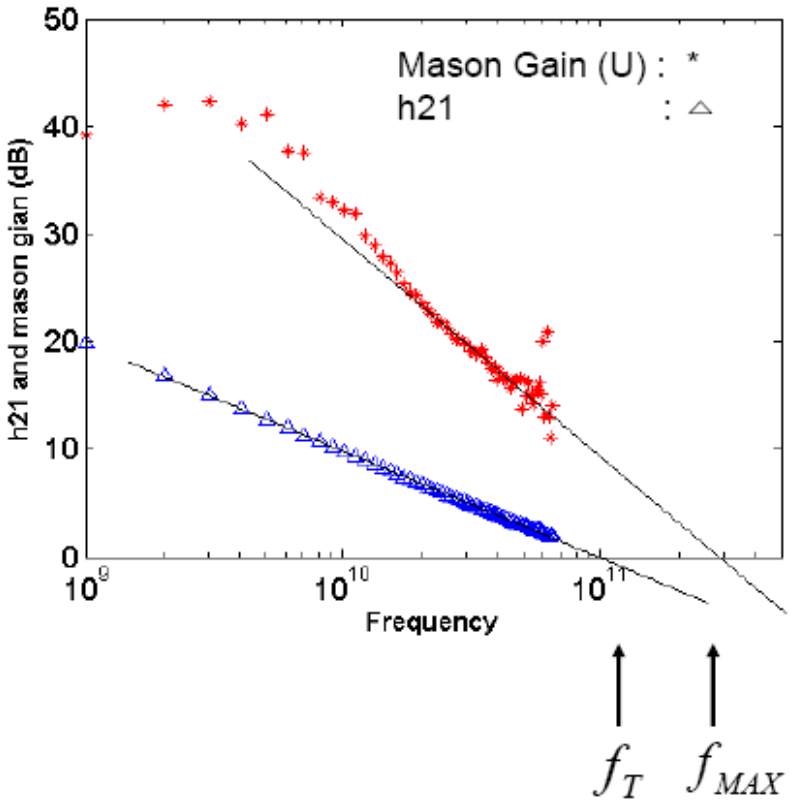
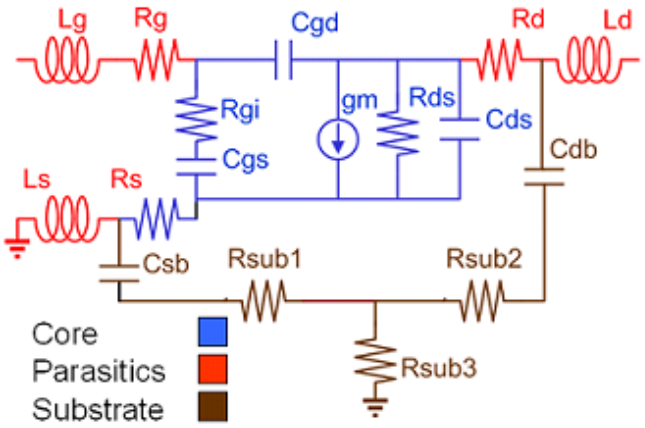


Figure 3.4: By careful layout and device optimization, maximum oscillation frequency of a $40\mu m$ round table transistor is three times its f_t.

40μm wide round table transistor is shown in the Fig. 3.4. As expected and proved by measurement, transistor performance improved to a great extent and as illustrated in the Fig. 3.4 extrapolated f_{max} got almost doubled and reached to the record value of 300GHz.

Fig. 3.5 depicts the small signal model of mm-wave transistors which includes substrate network and terminal parasitics. Comparison of parasitic resistances and



	Regular	Round Table
Rg (Ω)	4.46	2.23
Rd (Ω)	3.54	2.42
Rs (Ω)	672m	438m
Cgs (fF)	35.7	57.1
Cgd (fF)	21.3	19.2

Figure 3.5: Small signal transistor model for mm-wave circuit design(top) and comparison of parasitic capacitances/resistances between regular and round-table 40 μm wide transistors both biased at 0.2mA/μm

capacitances between a regular and a round table transistor both biased at 0.2mA/μm is also demonstrated in Fig. 3.5. This figure shows that all the parasitic resistances are reduced due to multi-paths provided for current flow. Because of all those metal routings C_{gs} is higher for a round table transistor but since it will be resonated out in the amplifier design it will not degrade the amplifier performance.

Because of minimization of gate and source resistance, the Round Table structure also has a better noise performance. We used this high performance device in the first stage of the 30GHz amplifier which is the most critical one in terms of noise and linearity and has to provide enough gain to reject the noise of next stages.

For the matching networks we preferred transmission lines to loop inductors because the simulation of an inductor requires a detailed knowledge of the substrate as well as structures in close proximity to the inductor that contribute to return current paths. Additionally, due to the small dimensions of inductors at mm-wave frequencies, the size and effect of the interconnects will be crucial for their performance, which necessitates simulation of the entire layout. In contrast, the return current in a transmission line can be made to flow through a well defined path. The characteristic impedance of the line is thus highly predictable via EM simulations and there is close agreement between the measured and simulated data.

For transmission lines, coplanar waveguide structure was used rather than microstrip lines due to the higher achievable Z_o. In order to lower the conductive loss, two top metal layers were strapped together to form the signal and ground lines. A $Z_o = 51\Omega$ was obtained by setting the signal line width to 10μm and gap spacing to 7μm.

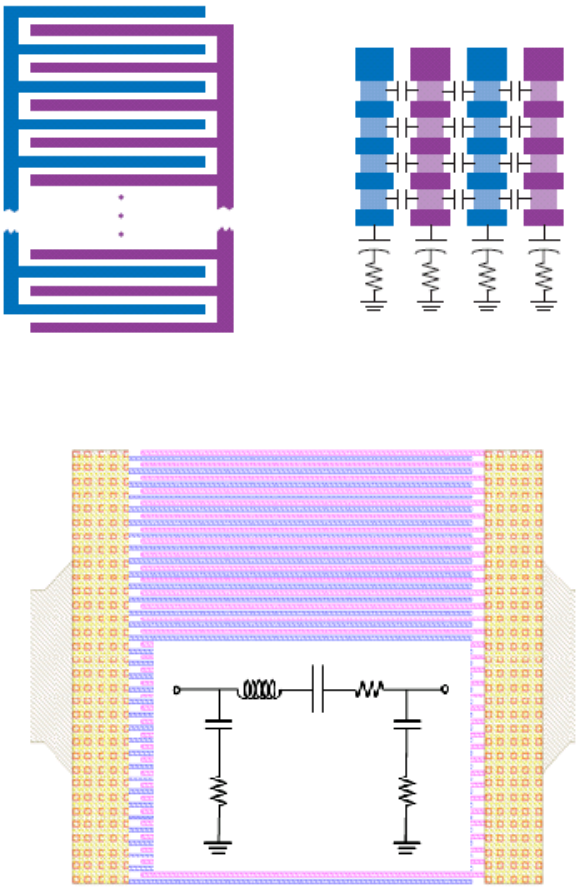


Figure 3.6: Top and side view of a MOM finger capacitor(top) and its model(bottom) that fits the measurement data from 5GHz up to 65GHz

While MIM capacitors are optional in this process, they were avoided to keep costs low. Custom "finger" capacitors were designed for coupling and bypass. In these capacitors we took the advantage of the high density capacitance between different metal layers and between vias. A capacitance density of about 1.5fF/μm^2 is achievable in this process. A typical capacitor employed in the design has an area

of 25μm $\times$ 25μm and 914fF of capacitance, with a measured resonance frequency of 41 GHz. Its reactance at 30GHz is +3jΩ which is low enough to be assumed as a short circuit for coupling and bypassing. Top and side views of a MOM capacitor along with its model that was fitted to measurement data from 5GHz up to 65GHz is illustrated in Fig. 3.6.

3.3 Circuit Design

Fig. 3.7 shows maximum stable gain plots for 40μm wide round table common source transistor and also a 40μm wide cascode device both biased at 0.2mA/μm. This is a good compromise bias point for both high MSG and low NF_{min}. As depicted in the figure, at 30GHz the CS has a MSG=10.7 dB whereas the cascode has an MSG of 16.2dB.

As illustrated in Fig. 3.7, up to 35 GHz the second pole does not have that much of effect on the cascode gain. On the other hand, the cascode device has noticeably poorer noise performance which makes it unsuitable for the first stage of an amplifier. One approach to overcome this problem is to resonate out the junction capacitance [20],[24] but an alternative approach is to employ a single transistor amplifier as a first stage and remove the noise generated by the cascode device com-

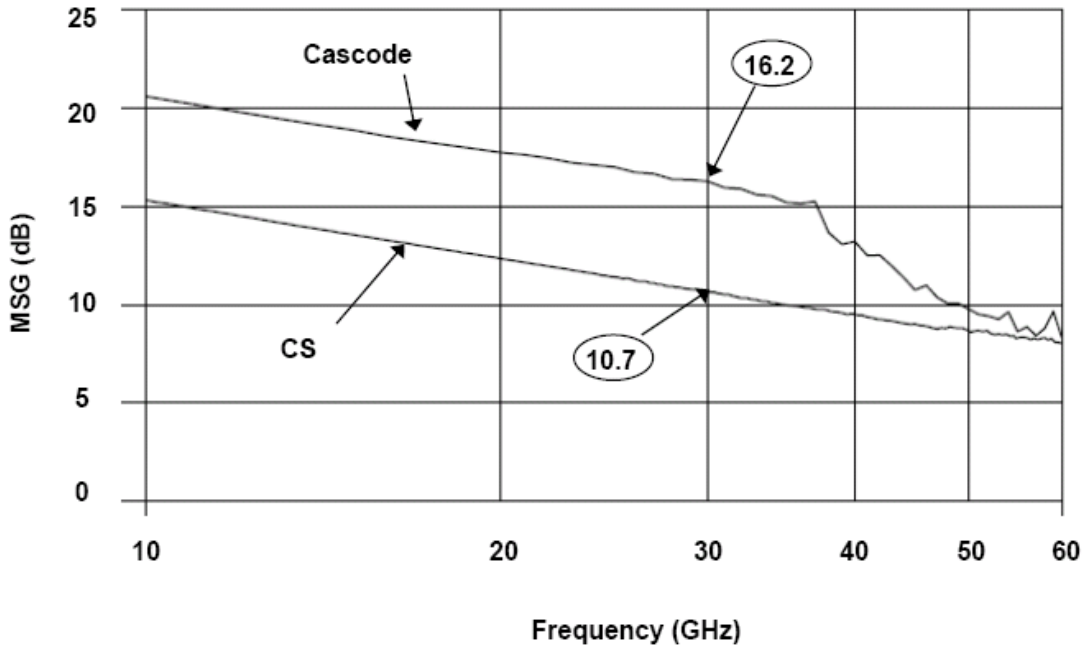


Figure 3.7: Maximum stable gain for 40μm wide cascode and round-table common source transistors biased at 0.2mA/μm .

pletely. Since gate resistance R_g has a great effect on the noise, we incorporate a round table structure in order to minimize this contribution as much as possible. A single transistor amplifier exploiting the round table structure and biased at 0.2mA/μm is used for the first stage. This round table device has NF_{min} of 1.25dB at 30GHz.

Active devices are unconditionally stable at very low frequencies where capacitors are open and at very high frequency where the substrate and parasitic losses dominate. Due to the poor reverse isolation of a common source transistor at mm-

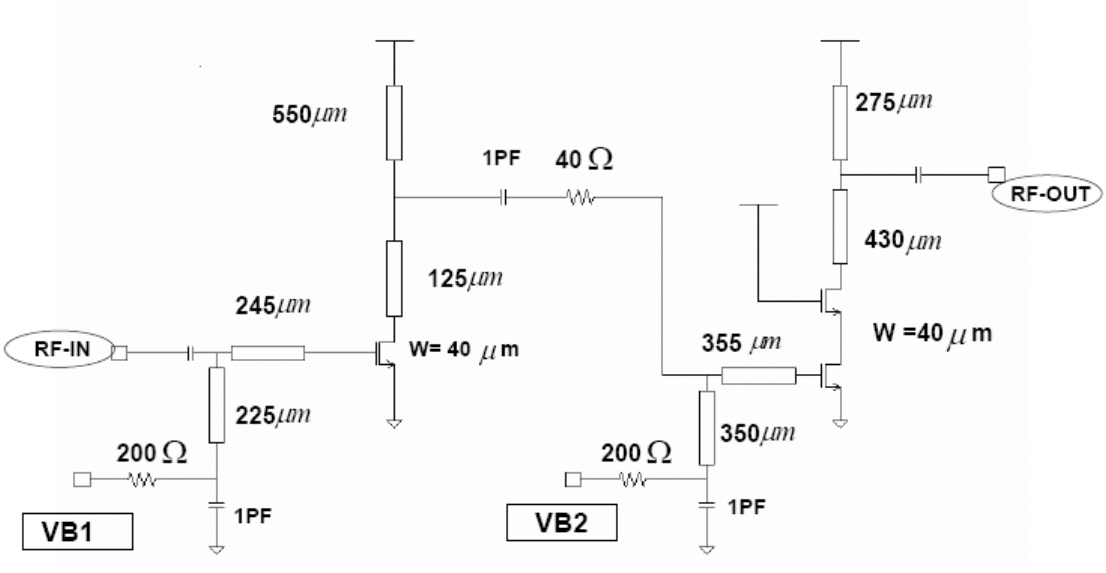


Figure 3.8: Schematic of the mm-Wave LNA.

wave frequencies, the first stage has stability issue and to resolve this problem a 40Ω stabilizing resistor is used between the two stages. The first stage has 12 dB of voltage gain and its output impedance is 130Ωwhich will be matched to the series impedance of the stabilizing resistor and input impedance of the next stage. Adding this stabilizing resistor decreases the voltage level by 3dB so its effects on the overall noise performance is almost negligible and it increases the total NF by 0.5 dB while mak-

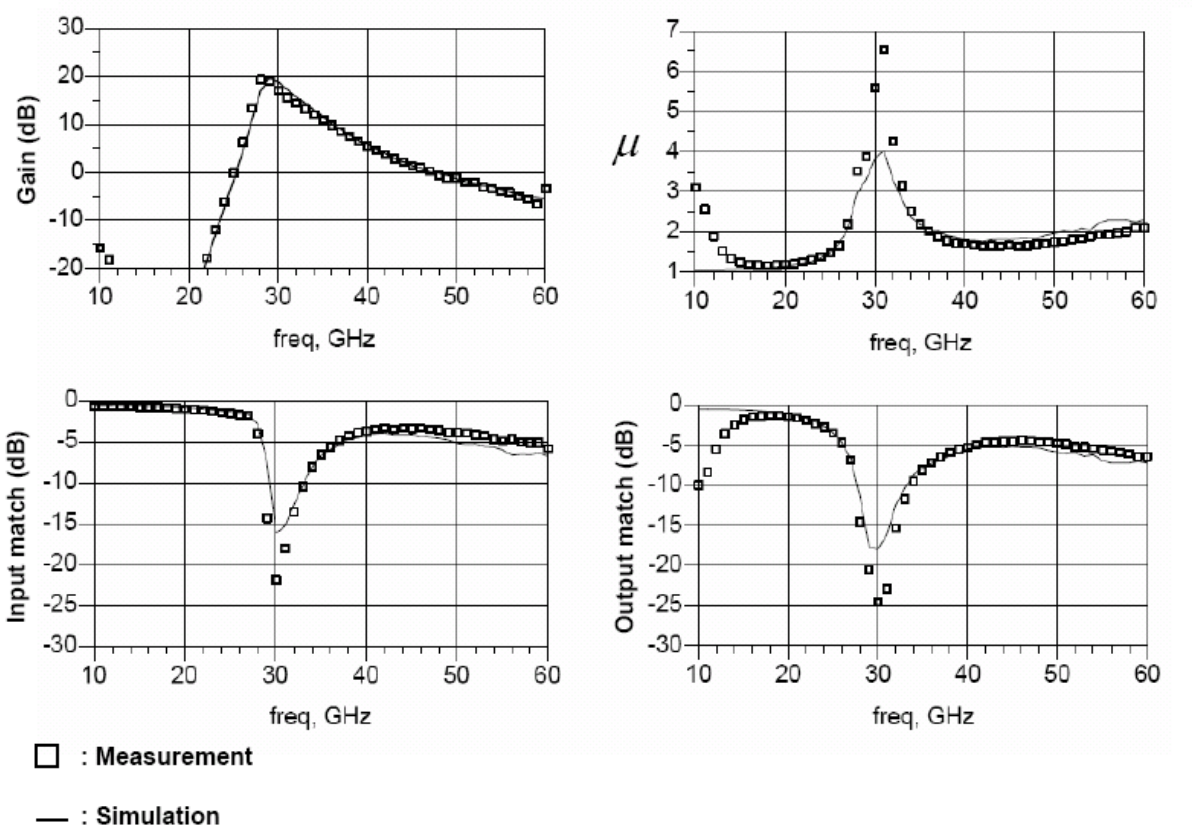


Figure 3.9: Measured vs. simulated S-parameters and μ-stability factor.

ing the amplifier unconditionally stable for any load/source impedance value. Having used a stable cascode amplifier for the first stage we would get a noise figure which was about 1.5dB larger than a single transistor amplifier. Hence this method of using a stabilizing resistor improved the overall noise figure by 1dB.

To get enough gain and isolation, a cascode transistor was used for the second

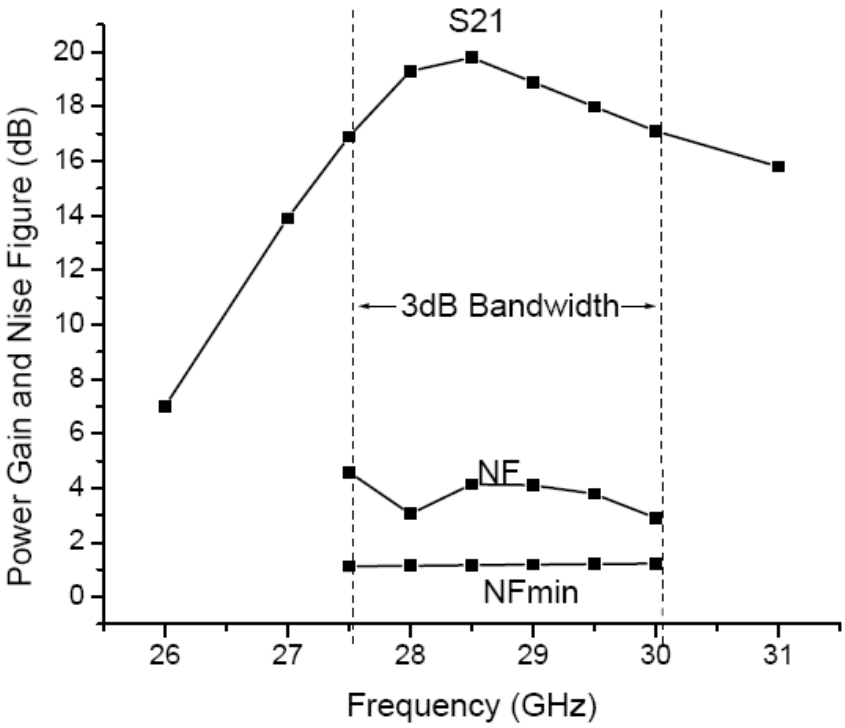


Figure 3.10: Measured gain and noise figure along with the simulated NF_{min}=1.25dB for a 40μm wide round table transistor.

stage amplifier which is not a crucial stage for the overall noise figure. Input and output pads are also part of the design and were absorbed in the matching networks.

Coplanar waveguide(CPW) transmission-line structures were used extensively to realize the input, output and interstage matching networks as shown in the layout (Fig. 3.13). At mm-wave frequencies, the lengths are not prohibitively

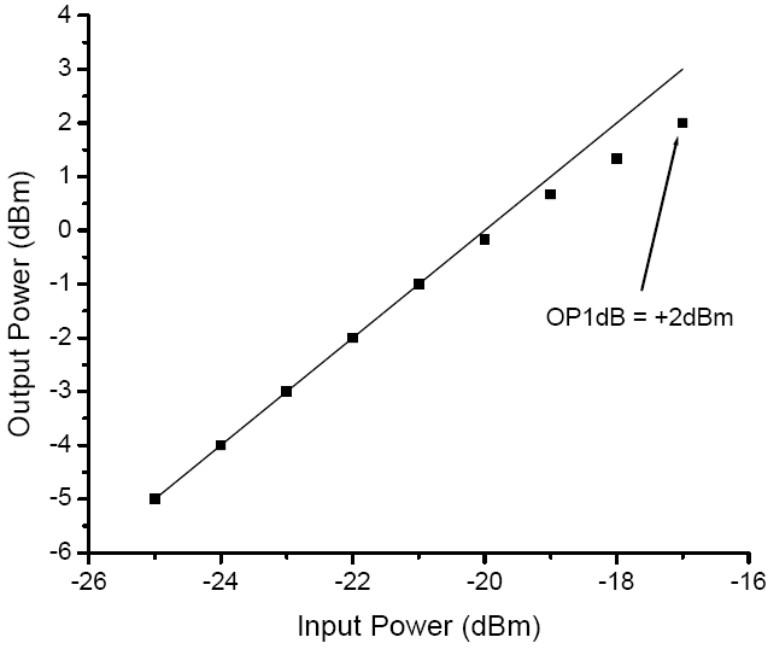


Figure 3.11: Measured compression characteristics.

long and bending them saves even more area.

Transmission lines can provide same reactances at multiple frequencies. They also act as small inductors at very low frequencies. So care should be taken for transmission-line type of matching networks outside their band of interest. Because they might provide enough match at undesired bands and under these conditions the amplifier will have gain which is not expected. Due to non-negligible gain at an

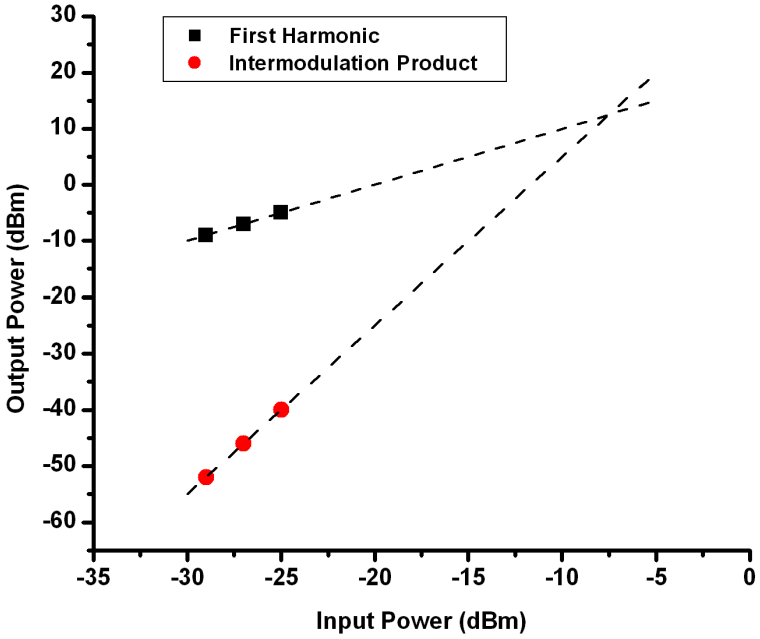


Figure 3.12: IIP3 measurement of the amplifier. The two tones were at 28.6GHz and 28.4GHz; the intermodulation product was measured at 28.8GHz.

unwanted band around 5 GHz in simulations, 200Ω resistors were added to the gate bias lines to de-Q the matching network and dampen the gain at 5 GHz completely. A 1PF custom designed finger capacitors bypasses these de-Q ing resistors at the desired frequency band.

3.4 Experimental Results

The mm-wave amplifier was fabricated in a standard digital 90nm CMOS process provided by STMicroelectronics. The fabricated prototype, shown in Fig. 3.13,

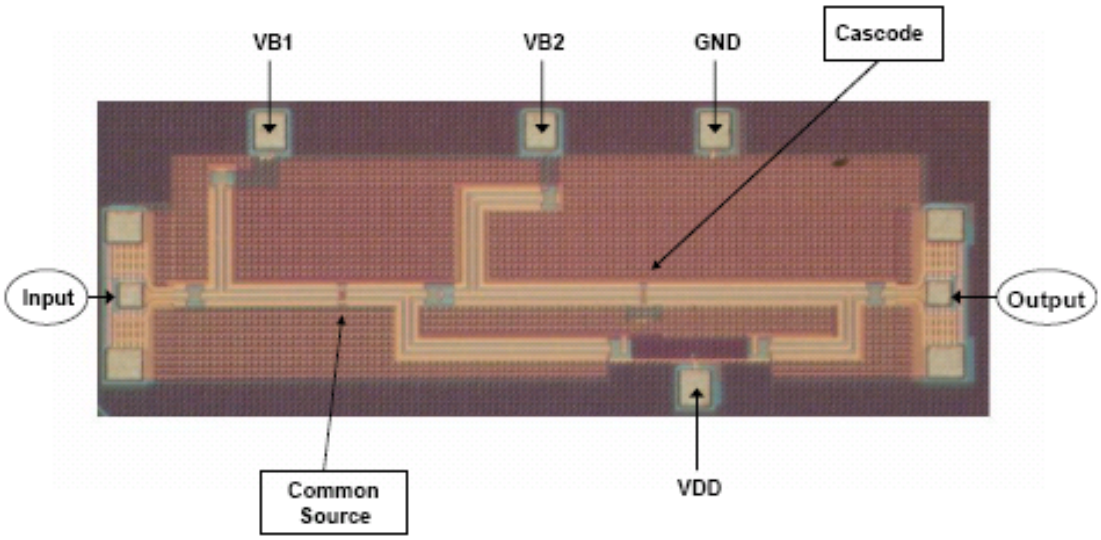


Figure 3.13: mm-Wave Amplifier prototype die photo.

has been characterized. Measurements were taken directly using wafer probes.

The measured S-parameters are shown in Fig. 3.9, displaying good match between measurements and simulation. The amplifier has a peak gain of 20 dB at 28.5 GHz and 3-dB bandwidth from 27.6 GHz to 30.2 GHz. The amplifier is well matched, with input and output return losses better than 12dB and 17dB respectively over the 3dB bandwidth.

The large signal and distortion measurements verify +2 dBm of output power

at the 1-dB compression point (input P1dB=-17dBm) and two tone measurement shows -7.5 dBm of IIP3 which is 9.5dB above the input P1dB and in good agreement with the theoretical 9.6dB value (Fig. 3.12).

Noise measurements were performed using the gain method. The input of the amplifier is matched and the output noise power is measured on a spectrum analyzer. The spectrum analyzer noise floor was too high (-140 dBm/Hz) for a direct measurement, so a second amplifier module with 28 dB of gain at 30 GHz was used to raise the output noise higher than the spectrum analyzer noise floor (around -127.5 dBm). The noise figure is calculated at a few points across the band and we found the minimum noise figure of 2.9 dB at 28 GHZ (where the gain is close to its peak) and the NF is lower than 4.2 dB over the bandwidth of the amplifier (Fig. 3.10). The amplifier consumes 16.25 mW of power from a 1 V supply voltage. The current is nearly evenly divided between the stages.

Table 3.1 summarizes the performance of recently reported mm-wave amplifiers. The amplifier presented in this work has good gain, matching and noise performance while dissipating only 16.25mW of power. The linearity is satisfactory for most wireless applications, which is achieved with a low supply voltage of 1 V (Fig. 3.11).

Table 3.1: Comparison to recently published mm-wave amplifiers.

Ref.	This Work	[15]	[16]	[17] (amp1)	[20]	[21]
Process	90nm CMOS	90nm SOI	130nm CMOS	90nm CMOS	90nm CMOS	130nm CMOS
Gain (dB)	20 @ 28.5GHz	11.9 @ 35GHz	20 @ 43GHz	5.8 @ 20GHz	18.6 @ 33GHz	8.4 @ 26.2GHz
S11 (dB)	-12	-6	-14	-10	-8	-10
S22 (dB)	-17	-18	-17	-18	-8	-10
NF (dB)	2.9 @ 28GHz	3.6 @ 35GHz	6.3 @ 41GHz	6.4 @ 20GHz	3 @ 33GHz	4.8 @ 26.2GHz
OP1dB(dBm)	2	4	4	1	N/A	N/A
IIP3 (dBm)	-7.5	N/A	-5.5	-2.8	N/A	-13
P_{dis}(mW)	16.25	40.8	36	10	10	0.8
Area(mm^2)	0.67	0.18	0.525	0.56	0.856	N/A

Chapter 4

Conclusion

In this work we demonstrated using lower cost and highly integrable CMOS technology in designing low noise amplifiers to be used in front-ends of satellite receiver systems was accomplished. Two LNAs at X and K_a bands were designed, fabricated and tested.

For the X-band (9GHz) LNA, a capacitive shunt matching technique has been proposed where a capacitor in shunt-shunt feedback configuration provides the matching condition at the input without adding noise. Compared to inductive degeneration, this technique eliminates the series gate inductor along with its associated noise. To realize sufficient gain at high frequency, an off-center tuned load has been utilized. The prototype amplifier is designed and fabricated in a 130nm RF-CMOS

process.

The measured amplifier has 20.5dB of gain at 8.8GHz with input and output match of -15dB and -8dB respectively. It has 1.4 GHz of 3dB-bandwidth around 9 GHz with the noise figure of 1.7dB at the center frequency and below 2dB across the band. Large signal measurements reveal that the amplifier can deliver -2dBm of power to the 50Ω output load at its 1dB compression point. It draws 23mA of current from a 1.2V supply. The chip occupies an area of 0.64mm^2.

The K_a-band (30GHz) low noise amplifier was implemented in a standard digital 90nm CMOS process. Good performance was achieved through careful device and layout optimizations without utilizing RF/analog process options. A round table transistor structure was used to realize higher f_{max} and lower NF_{min}. Low loss CPW lines with two top metal layers strapped together and custom finger capacitors were used for the matching and bypassing networks.

The mm-wave amplifier has a peak gain of 20 dB at 28.5 GHz and a 3dB bandwidth of 2.6 GHz with the input and output matching better than 12 dB and 17 dB over the entire band respectively. The NF is 2.9 dB at 28 GHz and less than 4.2 dB across the band, and the amplifier can deliver 2 dBm of power to a matched load at its 1 dB compression point. The amplifier has a measured linearity of IIP3=-

7.5 dBm. It consumes 16.25 mW of power using a low supply voltage of 1 V and occupies an area (excluding the pads) of 1600μm $\times$ 420μm

Demonstrating CMOS LNA design is the first step toward accomplishing a CMOS single-chip solution for satellite receivers. This low cost single-chip solution would be very beneficial for applications such as entertainment and broadcasting where cost is an important parameter in commercializing the application.

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