

Solution Processing Techniques for Low-Cost Circuit Fabrication

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Solution Processing Techniques for Low-Cost Circuit Fabrication

by

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Fall 2006

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Chair

Date

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Fall 2006

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Abstract

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Professor Vivek Subramanian, Chair

With the high performance and cost associated with today's silicon integrated circuits there is a market for lower-performing, yet extremely inexpensive circuits. This work focuses on the materials, processes, and techniques of ultra-low-cost fabrication. In particular the fabrication of devices using inkjet printing and aqueous deposition is addressed in detail.

Low-cost RFID tags would enable automated inventory and checkout in retail stores by replacing the ubiquitous UPC barcode. In this work the fabrication of the passive components for RFID tags is achieved primarily by inkjet printing, using a gold nanoparticle ink to generate conductive lines on plastic substrates. After considering the performance requirements of 13.56 MHz RFID passive devices, the all-printed devices are improved by using a combination of inkjet patterning with an electroless copper deposition. The results of this hybrid approach are shown to be far superior to printing alone, generating inductors with quality factors above 20.

The concept of solution-processing is then expanded to cover semiconductor and insulator materials, with a focus on transparent TFTs for active-matrix OLED dis-

plays. Zinc oxide TFTs are fabricated using chemical bath deposition followed by an anneal in oxygen ambient. Electron mobility as high as $3.5 \text{ cm}^2/\text{Vs}$ is achieved, and mobility of $1.5 \text{ cm}^2/\text{Vs}$ is achieved at low anneal temperatures (450°C), enabling the use of cheap glass substrates. These results present a significant improvement over amorphous silicon, and will allow the development of low-power high-resolution OLED displays.

Professor Vivek Subramanian
Dissertation Committee Chair

To my beloved grandmother Hannah Stannard, who passed away at the age of 92 March 2, 2006. She missed my sister's wedding and my graduation by a few months.

To my parents Sarah Stannard and Howard Redinger, for their unwavering support and faith in their son. To them I owe a debt I can never repay.

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Chapter 1

Introduction

For over 40 years silicon has been the material of choice for circuit fabrication. Moore's law has been fulfilled time and time again, and today microprocessors are functioning at frequencies orders of magnitude faster than perhaps the first researchers ever imagined. Silicon circuit fabrication is one of the most reliable and well controlled processes known to man. However, silicon is quite expensive to process and package. The capital investment necessary for a new fabrication facility runs into the billions of dollars, and then it costs thousands of dollars to process each wafer.

The development of low-cost circuits, even with degraded performance, would enable the use of electronics and automated systems where they previously would be cost-prohibitive. The main premise of low-cost fabrication is the use of inexpensive materials which can be processed without the use of a cleanroom environment or special lithographic techniques. The avoidance of vacuum systems (e.g. sputtering and evaporation) is also preferred. These sacrifices come at the cost of performance, but there are many applications where the high performance of silicon is not required.

For example, amorphous silicon has become the dominant technology for active matrix display backplanes.

The low-cost fabrication of circuits must be approached from several directions. Material development, especially soluble materials, is obviously a major focus of current research, but there are also challenges in deposition and patterning methods. Much of the work in this thesis focuses on the use of inkjet printing as a patterning tool because of its flexibility, capacity for large area throughput, and compatibility with a large number of soluble materials. However, significant challenges remain in the development of printable metals and semiconductors. Alternatives to inkjetting alone are proposed and examined in detail. A major focus of this work is the development of a hybrid approach where inkjet printing is used to define an area rather than deposit electrically active materials. This approach is shown to give far superior results compared to inkjet printing alone. The use of aqueous deposition methods in combination with inkjet patterning has been investigated for both metal and semiconductor materials.

The poster child of the low-cost fabrication field has been Radio Frequency Identification (RFID), with the intention of replacing the ubiquitous Universal Product Code (UPC) barcodes. However, low-cost fabrication techniques could also be applied to supply developing nations with electronics for display or other applications. It is this market segment, where the ultra-high performance of silicon is not required, where low-cost techniques become economically advantageous. In the following sections the specific motivation for considering application of printed electronics to RFID and displays will be considered in more detail.

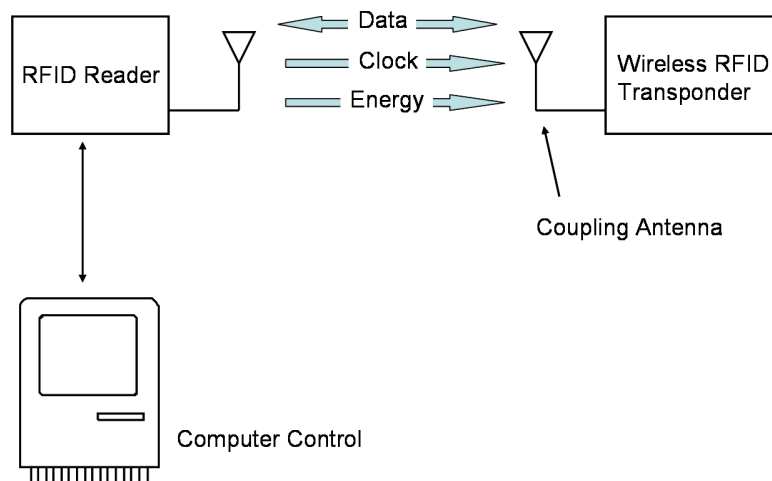


Figure 1.1. Diagram of an RFID system.

1.1 Radio Frequency Identification

Low-Cost RFID tags would allow the replacement of UPC barcodes with a wireless system, which would allow faster checkout and inventory. The system, depicted in Figure 1.1, consists of a computer-controlled reader antenna, and the RFID tag itself. At lower communication frequencies (such as 13.56 MHz) data and power are transferred via a coupling magnetic field. At higher frequencies (above 900 MHz) communication occurs via an electromagnetic field. Since the reader is plugged into a power outlet its functionality is not limited by power consumption, circuit speed, or cost since each implementation typically has only a few readers. In contrast, the tags are limited by power and cost.

In order to be economically viable as a replacement for UPC barcodes these tags have to be manufactured cheaply, typically for less than one cent per tag (124). A fabrication method that does not involve expensive processes or the use of silicon substrates is highly desirable. The development of a solution-based process on a flexible substrate would allow reel-to-reel fabrication, which is an extremely inexpensive

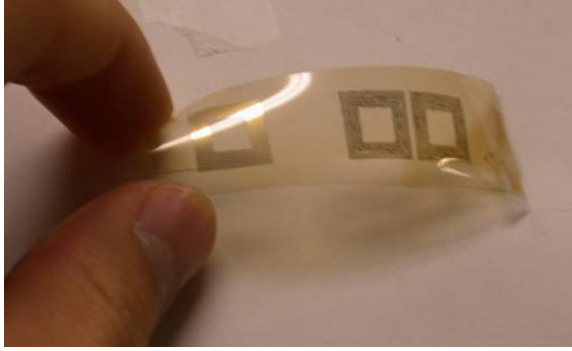


Figure 1.2. Spiral inductor printed onto a flexible plastic substrate.

way to mass-produce circuits since it eliminates vacuum processing, lithography, and subtractive processing steps.

Passive components such as inductors and capacitors are required on the RFID tag because they are used in circuits such as filters, oscillators, and memory, and also for power transfer. Inductive coupling is used to transfer power from a reader to a RFID tag. The tag inductor is placed in the near field of a reader coil, causing a voltage to be induced on the tag inductor. Typically a capacitor is put in parallel with the tag inductor to create a resonant circuit, in order to boost the tag voltage at the tuned frequency. This voltage is then rectified and used as the DC source for any analog or digital processing necessary for communication. High quality components are needed to allow adequate communication range. The main challenge in building high quality inductors is reducing the sheet resistance of the metal layer, because resistance is the dominant loss mechanism at low frequencies.

The development of passive devices suitable for use in a RFID system operating in the 100 kHz to 15 MHz range is the subject of the first half of this thesis. Inductors, capacitors, and interconnect are fabricated on flexible plastic substrates. After an analysis of the performance requirements of the coupling inductor an improved inductor process that combines inkjet printing and electroless copper plating is described.

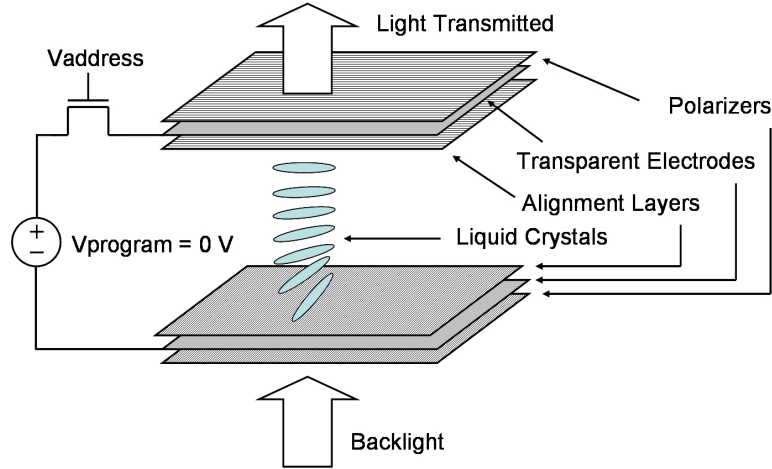


Figure 1.3. A liquid-crystal pixel in the transparent state.

1.2 Transparent TFTs for Display Applications

Thin-film transistors (TFTs) have been used in active-matrix liquid crystal display (LCD) backplanes for decades. Each pixel of LCD (shown in Figure 1.3) contains at least one TFT that acts as a switch to program the liquid-crystal (LC) material. The pixel itself consists of a linear polarizer, transparent electrode, alignment layer, liquid-crystal material, then another alignment layer, transparent electrode, and polarizer oriented 90 degrees relative to the first. As light from a backlight passes through the display it is either allowed to pass, or is blocked by the opposed polarizers. The LC material is chiral, and will rotate the polarization of the incident light if no bias is applied, thus aligning the light polarization with the second polarizer and allowing it to pass. If a bias is applied, the LC molecules will align with the applied field and not rotate the light. This results in a dark pixel (Figure 1.4).

Transistors fabricated from amorphous silicon (α -Si) have found wide application in LCDs, and processing cost has been reduced to a point where a high-resolution LCD display can be fabricated for a few hundred dollars. A typical active-matrix pixel circuit diagram is shown in Figure 1.5. When the gate bus line is activated the

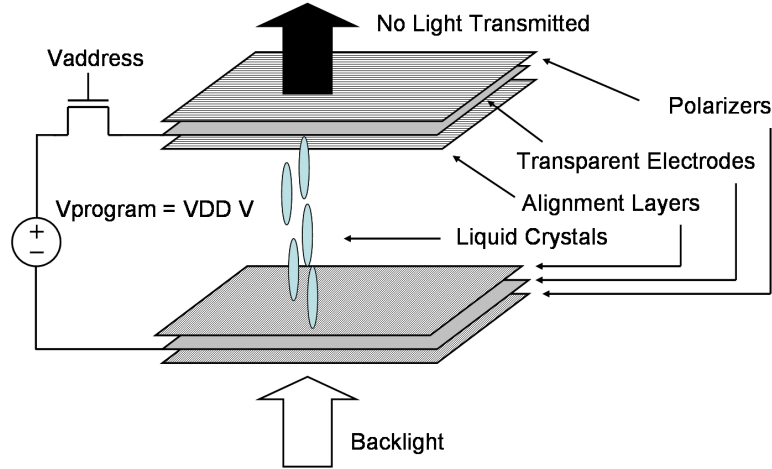


Figure 1.4. A liquid-crystal pixel in the blocking state.

TFT samples the voltage on the data bus line and programs the liquid crystal cell with voltage V_A . Amorphous silicon is well suited to this task because the power consumption of the display is dominated by the dynamic power associated with charging the cell. There is no static power consumption, and thus, the high drive voltages required are tolerable.

However, α -Si is not well suited for other types of displays such as those fabricated from organic light-emitting diodes (OLEDs). The cross-section of an OLED pixel is much simpler because the OLED is an emissive device, and no polarizers or backlight is needed. A simple circuit diagram is shown in Figure 1.6. An OLED is a current-driven device, and requires a static current for emission. α -Si simply cannot provide enough current without the use of high supply voltages. This results in displays with unacceptably high power consumption. Increasing the size of the TFT is not a viable solution because it would consume too much of the pixel area, requiring higher OLED brightness and resulting in decreased device lifetime.

A solution to this problem that many people have pursued is the fabrication of transparent transistors that consume the entire pixel area without significantly impacting display brightness. By taking advantage of the larger area available for

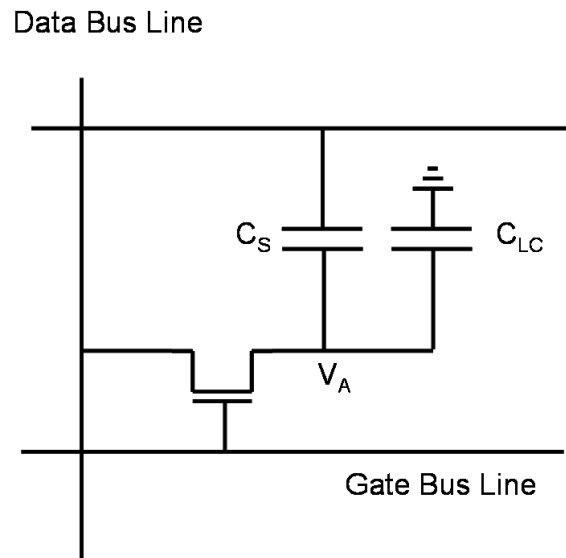


Figure 1.5. Circuit diagram of an active-matrix LCD pixel.

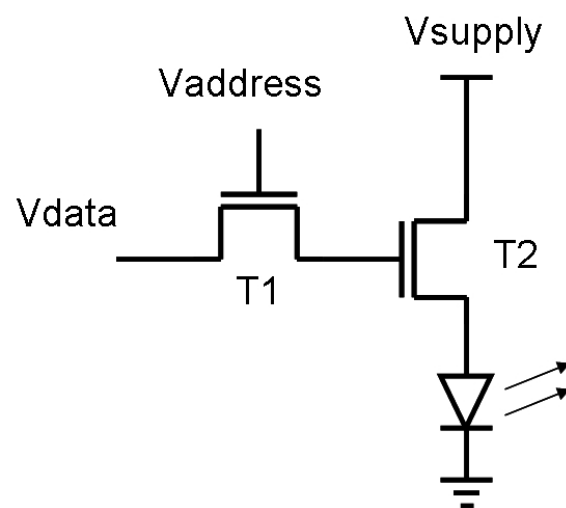


Figure 1.6. Circuit diagram for an active-matrix OLED pixel.

device layout the operating voltage, and hence display power, can be reduced to acceptable levels.

1.3 Organization

In Chapter 2 the deposition of electronic materials using printing techniques is discussed, with a focus on specific materials used for inkjet printing. A background of RFID operation is given in Chapter 3, with a detailed analysis of the performance requirements for the coupling inductor of an RFID tag. The results of an all-inkjetted passive component process for RFID fabricated at low temperature on plastic substrates are shown. Simulation results show that even in the best-case scenario printing alone cannot generate inductors suitable for RFID, so Chapter 3 concludes with an improvement to the process that uses an aqueous deposition combined with inkjet printing to fabricate high quality components. The aqueous deposition of semiconductor and insulator materials is the subject of Chapter 4, with a focus on zinc oxide. Chapter 5 provides a background of the use of TFTs in active-matrix displays, and gives an analysis of the performance requirements of a transparent TFT for use in active-matrix organic light-emitting diode (AM-OLED) displays. After motivating the use of transparent zinc oxide, Chapter 5 presents the first demonstration of zinc oxide thin-film transistors fabricated using an aqueous deposition of the semiconductor layer. Finally, Chapter 6 provides conclusions and insight into the future directions of this work.

Chapter 2

Printing Technology

2.1 Introduction

In recent years there has been a great deal of interest in alternative patterning methods. Cost models show that the highest throughput fabrication systems will be reel-to-reel, necessitating the use of flexible substrates and all-additive processing steps. Several printing techniques have been developed or adapted to suit device manufacture. Of these the most promising appear to be inkjet printing, gravure printing, and microcontact printing. In this chapter the different printing techniques are discussed, followed by a brief overview of the inkjet printer and techniques used in this work.

2.2 Reel-to-Reel Fabrication

Reel-to-reel fabrication is the ultimate low-cost fabrication scheme. Throughput is extremely high in part because it is compatible with large-area substrates. Ide-

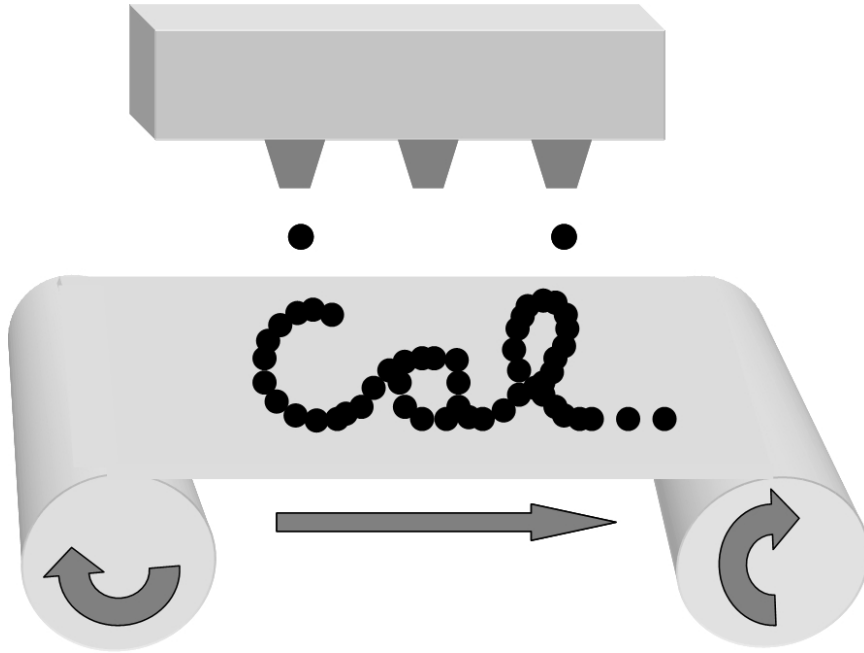


Figure 2.1. Low-cost reel-to-reel fabrication system.

ally flexible substrates such as plastic are used so they can be stored in rolls. As depicted in Figure 2.1, processing is done by sequential additive processing steps. However, there are practical limitations regarding what types of processing can be achieved. Plastic is a convenient low-cost substrate material that is highly available, non-conductive, and flexible. However it has several drawbacks. Plastic is generally limited to temperatures below 200 °C, and those that are stable at high temperatures are significantly more expensive than conventional plastics. Plastic also tends to shrink under elevated temperatures, which can make alignment difficult. Also, processing is limited to steps that do not require vacuum. While in theory a reel-to-reel system could be placed in a vacuum environment, in practice it would be difficult to integrate the vacuum steps with non-vacuum steps and still maintain the cost benefits of a reel-to-reel process. Therefore printing techniques such as inkjet, gravure, and microcontact are promising.

2.3 All-Additive Processes

Traditional lithography and patterning techniques require several steps: spinning photoresist, pre-bake, exposure, development, post bake, etch, and finally a photoresist strip. Each step adds to the cost of the process by increasing the time required and by decreasing yield. There is also substantial material wasted when entire wafers are coated with photoresist or other material (for instance, polysilicon or aluminum) and then a majority of the material is removed after patterning. Not only does this consume more material than necessary, but the excess material must be disposed of properly, adding additional cost. An all-additive process is defined as one where no material is removed after deposition. This dramatically cuts down on cost because material is only deposited where it is needed.

2.4 Printing Methods

In order to realize an all-additive process a method of selectively depositing the material is needed. Printing techniques have been used for centuries for the selective deposition of inks, and are seen as a logical choice for the selective deposition of “electronic ink.” The main techniques are inkjet, gravure, and microcontact printing. The advantages and disadvantages of each is discussed below, with regard to resolution, material compatibility, and flexibility of design.

2.4.1 Inkjet Printing

Inkjet printing has been used in manufacturing processes such as food packaging (potato chip bags), and of course has found wide application in the computer industry. A typical configuration is shown in Figure 2.2. The throughput is determined

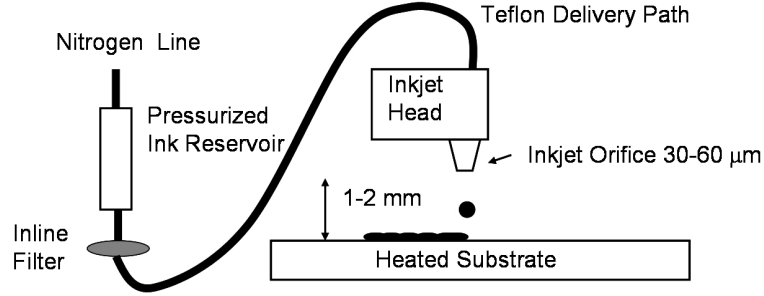


Figure 2.2. Typical inkjet printer configuration.

mainly by the number of print heads and the volume of material required. Epson inkjet printers for desktop use have around 80 individual orifices, and a commercial configuration may have thousands. Inkjet heads specifically developed for electronics by Dimatix Inc. have 128-256 individually controlled orifices with resolution up to 900 dpi. That translates to a drop size of approximately $30\text{ }\mu\text{m}$. The minimum feature size is determined by the accuracy with which the drops can be placed rather than the drop size. Dimatix has achieved drop accuracy of $2\text{ }\mu\text{m}$, which would allow fabrication of a TFT with a channel length of a few microns.

Material compatibility is excellent with inkjet. Both aqueous and organic materials can be used depending on the ink delivery path. The heads themselves are piezoelectric and fabricated out of glass or silicon micromachined. As Table 2.1 shows, inkjet is compatible with a wide range of ink viscosity, ranging from less than 1 to over 40 cP, again increasing the range of material compatibility. This is a clear advantage for inkjet printing over other methods such as gravure, which require higher viscosities of approximately 30-100 cP. Typically polymer binders are used to increase ink viscosity, but these materials are typically highly resistive, and the resulting deposited layer is a mixture of desired material and binder. Thus, the overall resistance of the material is increased. Since inkjet is not as dependent on viscosity as other methods, the use of binders is not required (130).

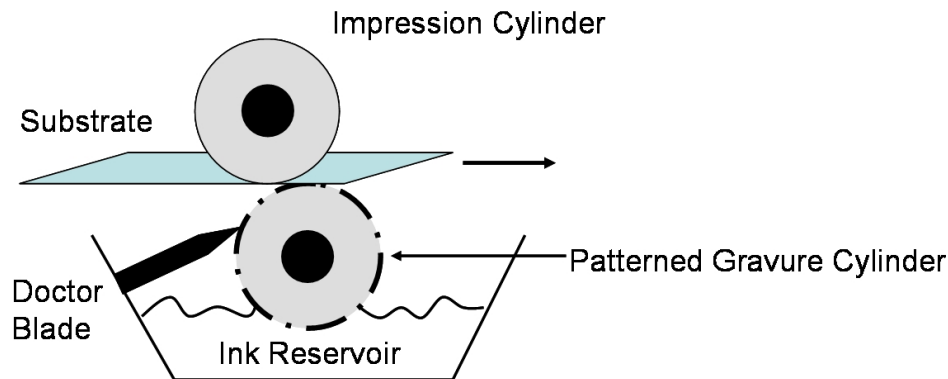


Figure 2.3. A typical gravure system consisting of an ink reservoir, patterned roll, doctor blade, and impression roll.

From a development standpoint inkjet printing is extremely flexible. Designs can be modified simply by changing computer code, rather than having to modify a master pattern such as a photolithographic mask or gravure roll.

2.4.2 Gravure

Gravure is a high-throughput printing technique that has been used for food labels, magazines, and wallpaper. Inherently compatible with a reel-to-reel process, gravure is currently being investigated for the deposition of electronic materials. The apparatus is shown in Figure 2.3. The patterned roll is typically made from copper and patterned with small hexagonal wells. As the roll is drawn through the reservoir it is covered in ink. A doctor blade then removes excess ink, leaving ink only in the wells. The patterned roll then comes into contact with the substrate under pressure from a second roll and the ink is transferred to the substrate.

To date, the smallest wells fabricated on a copper roll are approximately $50\text{ }\mu\text{m}$ in diameter. During the impression the ink spreads slightly resulting in a feature of $60\text{--}80\text{ }\mu\text{m}$. Thus the minimum feature size is on the order of $50\text{ }\mu\text{m}$, much greater than the resolution of inkjet. Both organic and aqueous inks are compatible with gravure, but

high-viscosity materials are not easily transferred from the cylinder to the substrate. The result is an incomplete pattern with possible voids in lines that were intended to be continuous. Inks that are not viscous enough will not be completely removed by the doctor blade and will result in excess ink deposited on the substrate. Therefore gravure is considered more sensitive to ink viscosity than inkjet.

While the throughput of gravure is higher than inkjet the initial cost is significantly higher. The equipment itself is expensive, and each copper roll must be fabricated at a cost of several thousand dollars. In a production environment this is not a large concern, but it makes for expensive experimentation.

2.4.3 Microcontact Printing

Microcontact printing is analogous to stamping, but with a very high resolution stamp. Traditional silicon lithographic techniques are used to create a master pattern on a silicon wafer with features approximately 500 nm to 1 μm in height, which is then used to create a stamp, typically out of the polymer polydimethylsiloxane (PDMS). The stamp is then coated with an “ink” that it transfers to the substrate during patterning. The process is quick, requiring only about ten seconds to transfer the material to the substrate (133). Alkanethiols are typically used as the “ink” because they transfer very well and adhere well to gold (and other metal) substrates (70). Microcontact printing has been used to pattern source and drain contacts for organic thin-film transistors with channel lengths of approximately 100 nm (69), demonstrating that high-resolution printing is possible so long as the substrate is very smooth. The tradeoff, however, is compatibility with large-area substrates. Uniformity of transfer over large area is difficult when using flexible substrates, due to the need to apply uniform pressure without flexing the substrate. In addition, the stamp size is

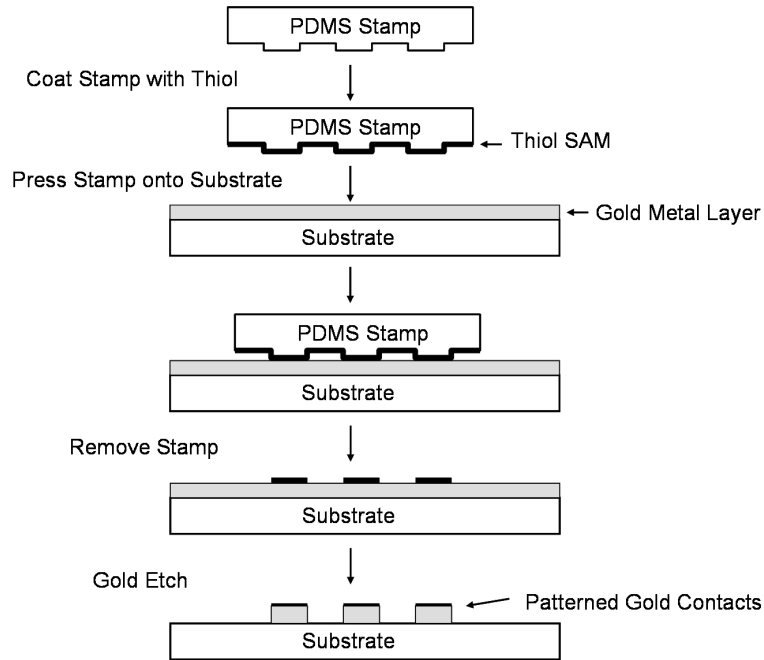


Figure 2.4. High-resolution patterning of gold using a PDMS stamp.

limited to approximately the diameter of a silicon wafer. Contamination can also be a concern, as with any technique requiring contact to the substrate.

The stamp fabrication process is not complex and although it requires silicon processing to create a master pattern, this pattern only needs to be made once. Several PDMS stamps can be patterned from the master. The process starts by coating a silicon substrate with a monolayer of vinyltrichlorosilane, then defining a pattern using e-beam lithography using polymethylmethacrylate (PMMA) as a mold for the precursor to PDMS. The PMMA is coated with dodecyltrichlorosilane before deposition of the PDMS precursor to ensure release of the stamp after curing. Curing is done at room temperature to prevent shrinkage (which results in distortion of the pattern) at approximately 8 bar pressure for 5 hours (69). The resulting PDMS layer should be $2\text{ }\mu\text{m}$ thick, or approximately twice the height of the master-defined pattern.

There are several variations on this theme. Offset liquid embossing (OLE) is sim-

ilar to microcontact printing, but the stamp is used to create a pattern in a blanket-deposited film rather than transfer material. After the pattern has been created another substrate is pressed onto the original, and the film transfers. This technique has been used to pattern nanoparticle films and spin-on-glasses (142), however, the resolution is somewhat less than microcontact printing with a minimum feature size of approximately $2\text{ }\mu\text{m}$. A second variation uses thermal imaging to transfer the organic conductor DNNSA-PANI/SWNT for use as organic transistor source and drain electrodes (8). Not surprisingly, this technique has degraded resolution of approximately $20\text{ }\mu\text{m}$.

2.5 Description of Custom Inkjet System

The printer used to deposit materials in this work is a custom drop-on-demand design with a temperature-controlled vacuum chuck so drops may be deposited onto a heated substrate (Figure 2.5). The ability to jet onto heated substrates is important since it enables greater flexibility in the control of surface fluid viscosity and evaporation rate. Elevated substrate temperatures reduce the amount printed materials spread after contacting the substrate, and also effects adhesion of some materials such as polyimide.

The delivery path consists of a pressurized Teflon reservoir, Teflon tubing, an in-line filter, and finally the glass inkjet head (See Figure 2.2). Teflon is an excellent choice because it is very resistive to organic solvents (unlike most plastic tubing) and it is transparent, allowing the user to easily see air bubbles or other problems with the line. Stainless steel is also another good choice in terms of material compatibility, but it is then difficult to diagnose problems. The in-line filter is extremely important to avoid clogged heads from dust or other small particles. The pore size was $5\text{ }\mu\text{m}$,

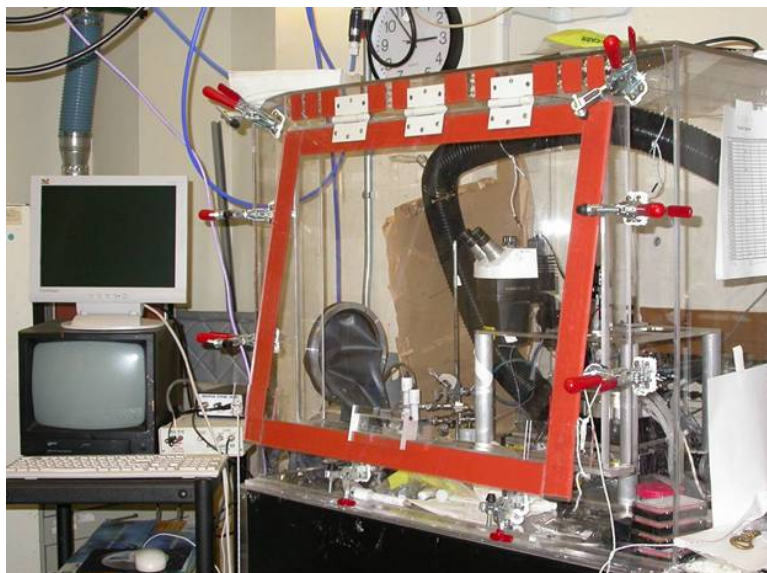


Figure 2.5. The printer used to fabricate devices in this work.

which allowed nanoparticle solutions to flow through without too much pressure, and effectively eliminated clogs in the head from dust particles. Head clogging resulting from nanoparticles drying inside or at the tip of the head was still a problem, but manageable again by the choice of solvent and substrate temperature.

The printer is enclosed in a nitrogen box so that inert atmospheres can be used. Since the printed materials used in this work were not oxygen sensitive all printing was done in air. Now that the different printing techniques have been discussed and a detailed description of the inkjet system used here has been given, it is appropriate to discuss the specific inks used to deposit metal layers. Gold nanoparticles that are soluble in organic solvents can be printed to form conductive gold, and this technique is used extensively in this work. These nanoparticles are discussed in detail in the next section, followed by a discussion of the various solvent choices, and finally a survey of the available flexible plastic substrates used for the fabrication of ultra-low-cost devices.

2.6 Gold Nanoparticles

The deposition of metals is typically done via sputtering or thermal evaporation. However, these processes are blanket depositions, require vacuum, and in the case of thermal evaporation, require very high temperatures. None of which is compatible with an all-additive low-cost process. Therefore a metallic “ink” is necessary to selectively deposit metals. This is achieved by printing layers of metallic nanoparticles.

Gold nanoparticles were used for the majority of this work, although processes for many other metals including silver and copper exist. Gold nanoparticles are made using a wet chemical process, where gold is encapsulated with an alkane thiol, depicted in Figure 2.6(a).

A TEM image of the nanocrystals is shown in Figure 2.6(b). The encapsulant keeps the gold particles separate from each other, and also makes them soluble in organic solvents, allowing the particles to be printed. Once deposited, the nanocrystals are heated, the thiol burns off, and the gold particles anneal together. Due to the extremely large surface area to volume ratio of these particles the melting temperature is approximately 130 °C, which is significantly lower than the 1000 °C bulk melting temperature of gold. This low processing temperature enables the use of flexible plastic substrates. When combined with an inkjet printer, nanocrystals are used to create gold patterns on plastic substrates.

The concentration of alkane thiol determines the nanocrystal size, and the length of the alkane chain determines the temperature at which the thiol burns off. Optimal results were found using hexane thiol, resulting in nanocrystals approximately 2 nm in diameter (50; 51). The process for making gold nanocrystals is given in Appendix B.

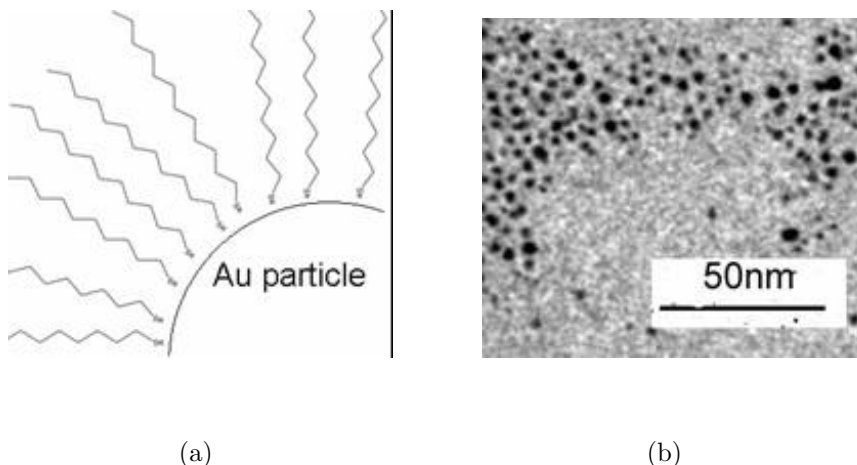


Figure 2.6. (a) Gold nanocrystal showing alkane-thiol encapsulant. (b) TEM image of nanoparticles.

2.7 Solvent Choice

Additional process margin is obtained through careful choice of the solvent used, with particular attention paid to solvent viscosity (to produce stable droplets) and evaporation rate (to minimize in-head clogging). The solvent used for a majority of this work, α -terpineol, printed cleanly due to its high viscosity, and also worked well over a heated substrate because of its high boiling point (94). If a material with low boiling point is used the solvent will evaporate while it is still in the head, leading to a buildup of material and eventually a clogged head. All devices presented in this work were fabricated using a 60 μm head manufactured by MicroFab Technologies, Inc. (3). This head has an all-glass delivery path, making it compatible with a wide range of solvents, and uses a piezo-based actuation mechanism that is compatible with the inks and temperatures used herein.

The alkane chains that encapsulate the gold particle are non-polar, and therefore make the particles soluble in non-polar solvents such as toluene and butylbenzene. However, the solvent needs to be fairly viscous to print cleanly, and also needs to

Table 2.1. Properties of nanoparticle solvents

Solvent	Boiling Point(°C)	Vapor Pressure (Torr)	Viscosity (cP)
Toluene	110	28.5	0.59
Butylbenzene	183	1.06	0.95
α -terpineol	217	0.1	39.23
Dihydroterpineol	199	N/A	N/A

have a high boiling point to print over a heated substrate. If a material with low boiling point is used the solvent will evaporate while it is still in the head, leading to a buildup of material and eventually a clogged head. Two solvents, α -terpineol shown in Figure 2.7(a), and dihydroterpineol shown in Figure 2.7(b), were found to have excellent printing properties.

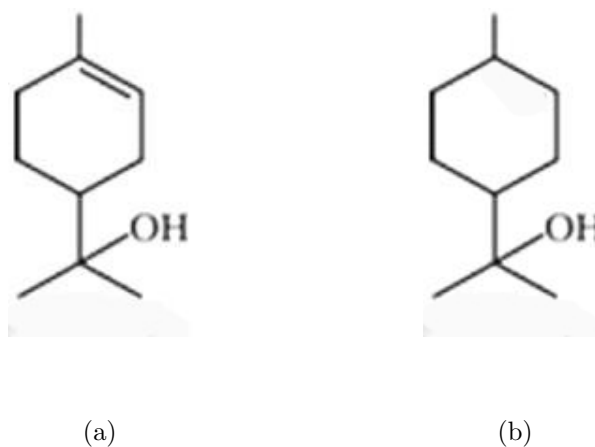


Figure 2.7. (a) α -terpineol and (b) dihydroterpineol structures.

Note that α -terpineol is not a toluene derivative and that it is actually an alcohol, but has sufficient non-polar character to solubilize the nanocrystals. A summary of solvent properties is shown in Table 2.1. Dihydroterpineol has very similar properties to α -terpineol (and can be produced via hydrogenation of α -terpineol with a platinum catalyst) but exact numbers for vapor pressure and viscosity were not available.

Now that gold nanoparticles and the solvents used to print them have been discussed, the available plastic substrates are presented. There are several types of plastic, each with different thermal and chemical properties, with more desirable properties generally costing more.

2.8 Plastic Substrates

The plastics commonly used as substrates are Polyethylene Terephthalate (PET) and Polyethylene Naphthalate (PEN). PET is used to make soft drink bottles, but is permeable to oxygen, which drove the development of PEN. PEN is a superior oxygen barrier, making it suitable for packaging perishable foods such as beer. In general PEN has a higher temperature stability, and has a glass transition temperature of 120 °C, compared to 80 °C for PET (95). Plastics are available with temperature compatibility up to 350 °C, for instance, DuPont’s Kapton polyimide films. However, these films are extremely expensive compared to the lower-temperature plastics, so processing temperature should be kept as low as possible.

The best performing substrate with respect to melting temperature and gold adhesion for our purposes was found to be Melinex (35), a polyester made by DuPont Teijin Films. The glass transition temperature was in excess of 220 °C, and gold adhered well.

2.9 Conclusion

Inkjet printing, gravure, and microcontact printing are all capable of patterning electronic materials. To date, microcontact printing has shown the highest resolution, but inkjet printing is compatible with a wider range of materials. It is also easier to

prototype systems than with gravure because the design can be easily changed in computer code rather than having to create a new gravure roll. Thus, inkjet was the method of choice for this work. Having provided an introduction to printing technology, it is now possible to investigate applications of printing to specific problems in low-cost electronics. In the next chapter, the use of printing in the fabrication of passive components for low-cost RFID is investigated.

Chapter 3

Printed Passive Components for RFID

3.1 Introduction

An RFID tag consists of three main components: the passive front-end that contains an inductor and capacitor, a rectification and voltage regulation system, and finally the back-end circuitry which is responsible for doing calculations, encryption, data storage, barcode comparison, or anti-collision, depending on the application (Figure 3.1). In this work the focus is on the fabrication of the passive front-end using patterning technology, materials, and temperatures that are compatible with a low-cost plastic substrate.

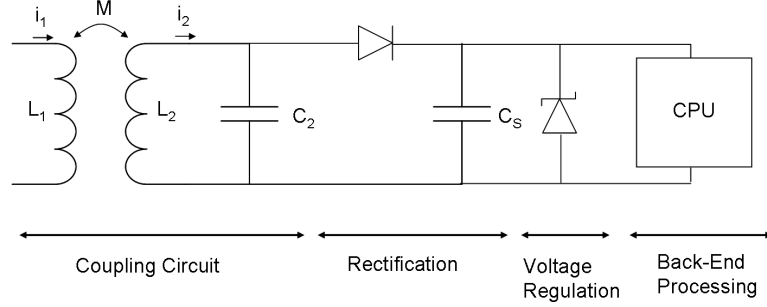


Figure 3.1. Diagram of full RFID tag including rectification and voltage regulation components.

3.2 Theory of RFID Coupling

RFID tags in the 13.56 MHz band use inductive coupling for power and information transfer between the reader and tag. The 13.56 MHz band is ideal for low-cost RFID systems because reader output power is maximized based on FCC specifications, and better range is achieved in metal contaminated environments (36). The tag must be in the near field of the reader antenna, typically $\lambda/2\pi$, or 3.5 meters at 13.56 MHz. In this scheme the reader and tag inductors are intimately connected by a magnetic field. The tag inductor receives information and power from the reader, and via load modulation can affect the current in the primary, thus transferring information back. The principles of this scheme are covered in the next sections.

3.2.1 Power Constraints

The useful range of the tag is governed by the ability of the tag to generate a supply voltage for its back-end circuitry. If the supply drops below a defined minimum logic circuits will fail to operate properly. The Federal Communications Commission (FCC) (33) limits the electric field strength that may be emitted by the reader. At frequencies between 13.553 MHz and 13.567 MHz the maximum electric field (E_{max})

Table 3.1. Field strength limitations imposed at 13.56 MHz.

Location	Field Measured	Field Limit	At Distance
United States	E_{max}	10,000 $\mu\text{V}/\text{m}$	30 m
Europe	B_{max}	42 dB $\mu\text{A}/\text{m}$	10 m
Japan	E_{max}	47,544 $\mu\text{V}/\text{m}$	10 m

measured at a distance of 30 meters is 10,000 $\mu\text{V}/\text{m}$ (1). This can be converted to maximum magnetic field (B_{max}) using the relationship:

$$\frac{E_{max}}{B_{max}} = v \quad (3.1)$$

where v is the velocity of propagation given by:

$$v = \frac{c}{\sqrt{\mu_r \epsilon_r}} \quad (3.2)$$

where c is the speed of light, μ_r is the relative permeability, and ϵ_r is the relative permittivity. The value of B_{max} is more useful than E_{max} because the tag and reader transfer power and information via the magnetic field.

While the FCC regulates emissions in the United States, there are separate rules governing emissions in Europe (32) and Japan. Table 3.1 describes the major differences between the regulations (31; 84). They are, however, all equivalent.

3.2.2 Mutual Inductance

It is useful to think of the reader and tag inductors as a transformer with a very low coupling coefficient (typically 0.01 to 0.05). Current in the primary will create a magnetic field, which will induce a current (and hence a voltage) on the secondary. This scheme is depicted in Figure 3.2.

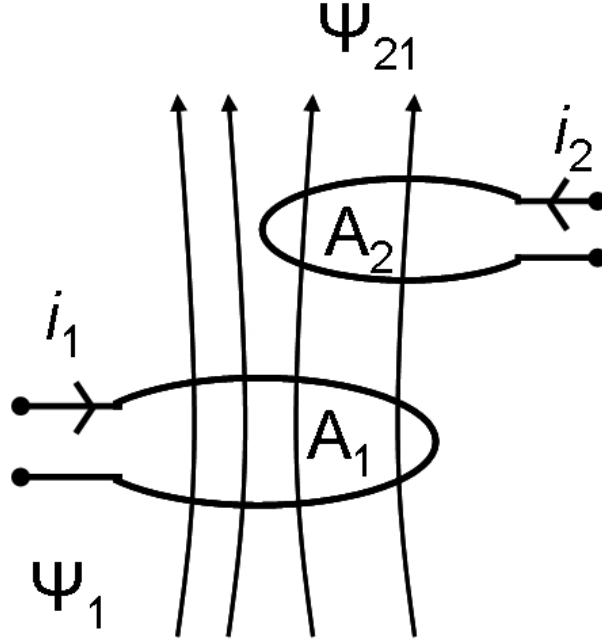


Figure 3.2. Magnetic flux shared by two inductors in close proximity.

The magnetic flux Φ is related to the magnetic field by:

$$\Phi = BA \quad (3.3)$$

where B is the magnetic field, and A is the area of the inductor. If the inductor has n turns then it is more useful to refer to the total flux Ψ :

$$\Psi = n\Phi \quad (3.4)$$

Inductance L relates the total flux to the current in the inductor:

$$L = \frac{\Psi}{I} \quad (3.5)$$

The coupling between two inductors can be represented by the mutual inductance, which is a measure of the flux shared by the two inductors.

$$M_{21} = \frac{\Psi_{21}(I_1)}{I_1} = \oint_{A_2} \frac{B_2(I_1)}{I_1} dA_2 \quad (3.6)$$

If there are only two inductors in the system then a single mutual inductance is sufficient to describe the system:

$$M_{21} = M_{12} = M \quad (3.7)$$

While the mutual inductance is significant, it does not give a feel for how intimately the inductors are coupled because several factors, including the layout and physical size of the inductor influence the shared flux. The coupling coefficient k gives a number between 0 and 1 that describes the extent of the coupling.

$$k = \frac{M}{\sqrt{L_1 L_2}} \quad (3.8)$$

Inductors that are not coupled will have a coupling coefficient of 0, and inductors that are perfectly coupled (and share all magnetic flux) have a coupling coefficient of 1.

3.2.3 Induced Voltage

Faraday's Law states that the induced voltage on an inductor is equal to the negative time rate of change of the flux. This can be used to calculate the voltage

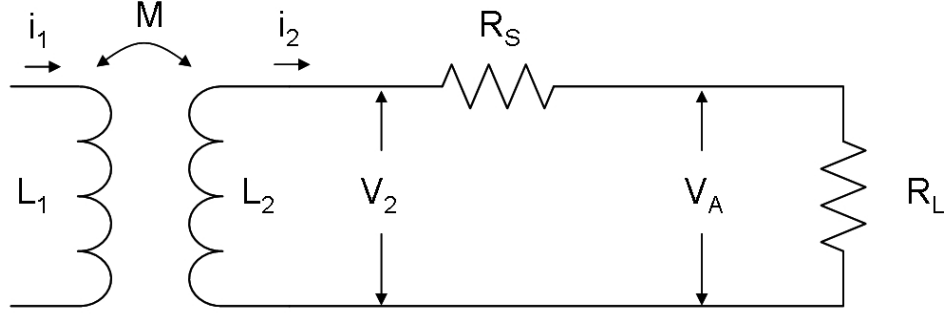


Figure 3.3. Circuit diagram used to evaluate the coupled voltage. R_L represents the load of the tag internals.

induced on the tag inductor, which is the value that determines the available supply voltage (and hence the range) of the tag.

$$V_i = \oint_C E_i dl = \frac{-d\Psi}{dt} = -N \frac{d\Phi}{dt} \quad (3.9)$$

Of course no inductor is ideal and has an associated series resistance. Although this resistance is distributed throughout the entire structure it is usually modeled as a discrete resistor in series with the inductor. This resistor affects the available supply voltage, and is depicted in Figure 3.3. Reducing the effect of this resistance is the subject of Section 3.6.

The voltage V_2 across inductor L_2 consists of two parts. The first is due to the incident flux and is given by Faraday's Law:

$$V_{2a} = -N \frac{d\Phi}{dt} = M \frac{di_1}{dt} \quad (3.10)$$

Since the tag inductor is part of a closed circuit, a current i_2 will flow and generate

a magnetic flux which opposes the incident flux. This resulting flux also creates a voltage:

$$V_{2b} = -L_2 \frac{di_2}{dt} \quad (3.11)$$

The total voltage across the inductor is then a superposition of the two induced voltages:

$$V_2 = M \frac{di_1}{dt} - L_2 \frac{di_2}{dt} \quad (3.12)$$

From here it is simple to derive the supply voltage available to the internals of the tag, denoted V_A .

$$V_A = M \frac{di_1}{dt} - L_2 \frac{di_2}{dt} - i_2 R_s \quad (3.13)$$

Typically when analyzing these types of linear time-invariant circuits it is useful to take advantage of the Laplace Transform to convert from the time domain to the frequency domain. The task of solving differential equations is reduced to algebraic equations, greatly simplifying the math. In the frequency domain:

$$V_A = j\omega M i_1 - j\omega L_2 i_2 - i_2 R_s \quad (3.14)$$

Using the equation $V_A = i_2 R_L$, the above equation can be simplified to a form which relates V_A to the current in the primary, the mutual inductance, and component parameters.

$$V_A = j\omega M i_1 - j\omega L_2 \frac{V_A}{R_L} - R_s \frac{V_A}{R_L} \quad (3.15)$$

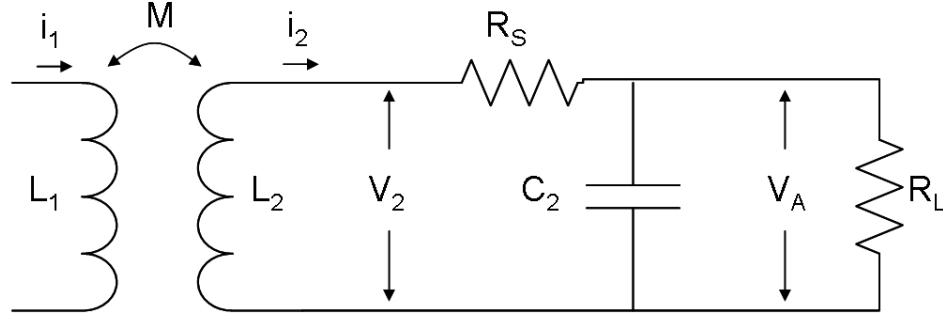


Figure 3.4. Circuit diagram used to evaluate the coupled voltage, with resonant capacitor.

$$V_A = \frac{j\omega M i_1}{1 + \frac{j\omega L_2 + R_s}{R_L}} \quad (3.16)$$

For RFID systems operating at 13.56 MHz, R_L is typically a few kilohms, R_s is a few ohms to tens of ohms, the inductor is a few microhenries, and the coupling factor κ is 0.01-0.05. These values are useful to keep in mind when simplifying equations derived in the next section.

3.2.4 Using Resonance to Boost the Supply Voltage

Since the range of the tag depends on the ability to couple a minimum supply voltage it is important to make the available voltage V_A as high as possible. A simple way employs resonance by adding a capacitor in parallel with the tag inductor, shown in Figure 3.4. The resulting RLC resonant tank will boost the available voltage by a factor equal to the quality factor (Q) of the tank. The tank quality is proportional to the energy stored over the energy dissipated per cycle, and is discussed in detail in Section 3.3.

The value of the capacitor is chosen to resonate with the inductor.

$$\omega = \frac{1}{\sqrt{L_2 C_2}} \quad (3.17)$$

$$C_2 = \frac{1}{L_2 \omega^2} \quad (3.18)$$

To calculate the effect on V_A the load resistor in Equation 3.16 is replaced by a resistor in parallel with a capacitor.

$$R_L // \frac{1}{j\omega C_2} = \frac{R_L}{1 + j\omega C_2 R_L} \quad (3.19)$$

Plugging in to Equation 3.16 we get:

$$V_A = \frac{j\omega M i_1}{1 + \frac{j\omega L_2 + R_s}{\frac{R_L}{1 + j\omega C_2 R_L}}} \quad (3.20)$$

$$V_A = \frac{j\omega M i_1}{1 + \frac{(j\omega L_2 + R_s)(1 + j\omega C_2 R_L)}{R_L}} \quad (3.21)$$

$$V_A = \frac{j\omega M i_1}{1 + \frac{j\omega L_2 + R_s - \omega^2 L_2 C_2 R_L + j\omega C_2 R_s R_L}{R_L}} \quad (3.22)$$

$$V_A = \frac{j\omega M i_1}{(1 + \frac{R_s}{R_L} - \omega^2 L_2 C_2 R_L) + j(\frac{\omega L_2}{R_L} + \omega C_2 R_s)} \quad (3.23)$$

The magnitude of V_A can now be easily calculated:

$$|V_A| = \frac{\omega M i_1}{\sqrt{(1 + \frac{R_s}{R_L} - \omega^2 L_2 C_2 R_L)^2 + (\frac{\omega L_2}{R_L} + \omega C_2 R_s)^2}} \quad (3.24)$$

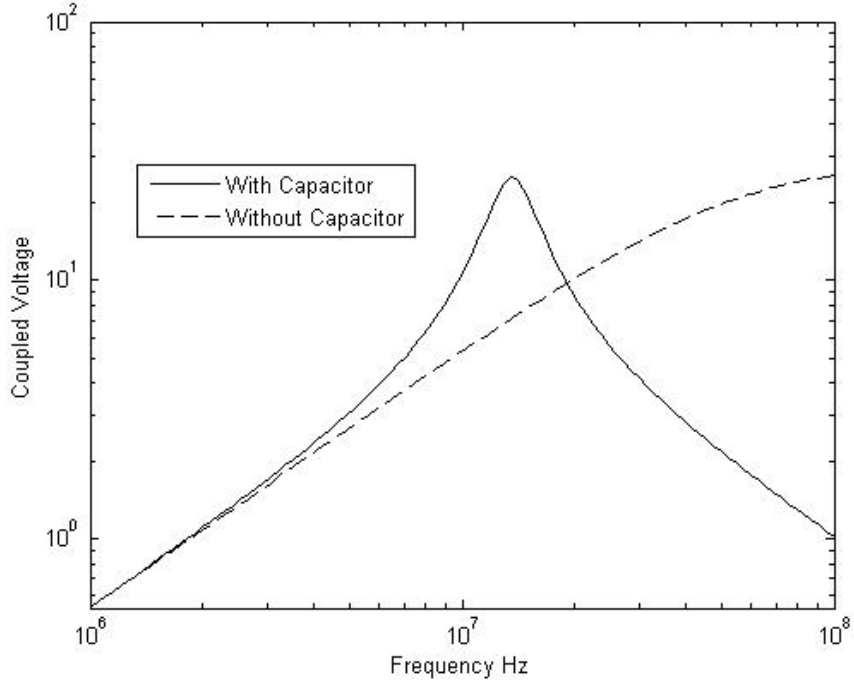


Figure 3.5. Increase in coupled voltage due to resonant capacitor.

$$|V_A| = \frac{\omega k \sqrt{L_1 L_2} i_1}{\sqrt{\left(1 + \frac{R_s}{R_L} - \omega^2 L_2 C_2 R_L\right)^2 + \left(\frac{\omega L_2}{R_L} + \omega C_2 R_s\right)^2}} \quad (3.25)$$

Plotting Equations 3.25 and 3.16 on the same graph illustrates the advantage of including the resonant capacitor, which boosts the coupled voltage by a factor of Q . Figure 3.5 was created with the following values: $f_0 = 13.56$ MHz, $k = 0.05$, $L_1 = 3 \mu\text{H}$, $L_2 = 3 \mu\text{H}$, $R_s = 10 \Omega$, $R_L = 1 \text{ k}\Omega$, $C_2 = 46 \text{ pF}$, and $i_1 = 1 \text{ A}$.

To calculate the RLC tank quality factor, the magnitude of Equation 3.25 is compared to the magnitude of Equation 3.16 at resonance. The ratio will be the quality factor Q . Starting with Equations 3.16 and 3.22:

$$Q = \left| \frac{\frac{1 + j\omega L_2 + R_s}{R_L}}{1 + \frac{j\omega L_2 + R_s - \omega^2 L_2 C_2 R_L + j\omega C_2 R_s R_L}{R_L}} \right| \quad (3.26)$$

Using $\omega^2 = 1/L_2C_2$ to simplify:

$$Q = \left| \frac{R_L + R_s + j\omega L_2}{R_s + j\omega L_2 + j\omega C_2 R_s R_L} \right| \quad (3.27)$$

Substituting for ω :

$$Q = \left| \frac{R_L + R_s + j\sqrt{\frac{L_2}{C_2}}}{R_s + j\sqrt{\frac{L_2}{C_2}} + jR_s R_L \sqrt{\frac{C_2}{L_2}}} \right| \quad (3.28)$$

$$Q = \left| \frac{1 + R_s/R_L + j\frac{1}{R_L}\sqrt{\frac{L_2}{C_2}}}{\frac{R_s}{R_L} + j\frac{1}{R_L}\sqrt{\frac{L_2}{C_2}} + jR_s\sqrt{\frac{C_2}{L_2}}} \right| \quad (3.29)$$

After clearing the denominator, simplifying using $(R_s/R_L)^2 \ll 1$, and eliminating the insignificant terms:

$$Q = \left| \frac{-j\left(\frac{1}{R_L}\sqrt{\frac{L_2}{C_2}} + R_s\sqrt{\frac{C_2}{L_2}}\right) + \frac{1}{R_L}\sqrt{\frac{L_2}{C_2}}\left(\frac{1}{R_L}\sqrt{\frac{L_2}{C_2}} + R_s\sqrt{\frac{C_2}{L_2}}\right)}{\left(\frac{1}{R_L}\sqrt{\frac{L_2}{C_2}} + R_s\sqrt{\frac{C_2}{L_2}}\right)^2} \right| \quad (3.30)$$

$$Q = \left| \frac{\frac{1}{R_L}\sqrt{\frac{L_2}{C_2}} - j}{\frac{1}{R_L}\sqrt{\frac{L_2}{C_2}} + R_s\sqrt{\frac{C_2}{L_2}}} \right| \quad (3.31)$$

Before taking the absolute value, note that $1/R_L\sqrt{L_2/C_2} = \omega L_2/R_L$. If the tank has a high quality factor, this term must be very small. In fact, if the inductor were ideal, this value would equal $1/Q$ of the tank. Therefore, Equation 3.31 can be simplified to give an approximate value of the tank quality factor:

$$Q = \frac{1}{\frac{1}{R_L}\sqrt{\frac{L_2}{C_2}} + R_s\sqrt{\frac{C_2}{L_2}}} \quad (3.32)$$

Note that this is precisely the equation (3.39) derived in Section 3.3.1, where the quality factor is calculated from an energy perspective.

The net consequence of these equations is clear, use of high-Q inductors is desirable to boost voltage available to the tag circuitry; this is achieved through a minimization of series resistance of the inductor, necessitating the development of the associated materials and printing processes.

3.2.5 Summary of Components Necessary

In order to create an RFID front-end it is necessary to fabricate inductors, capacitors, and interconnect layers, preferably on a low-cost plastic substrate. This challenge is met using inkjet printing as a patterning tool, along with careful choice of “inks” to deposit conductive metal and insulating dielectric layers.

3.3 Impact of Inductor Quality Factor on Coupled Voltage

Maximizing the coupled voltage of Equation 3.24 requires fabrication of a high quality factor inductor. Quality factor is defined as the energy stored over the energy lost per cycle, and for an inductor is equal to:

$$Q_L = \frac{\omega L}{R_s} \quad (3.33)$$

where ω is the frequency (rad/s), L is the inductance, and R_s is the series resistance. Recall that the coupled voltage is boosted by a factor Q, but it is the Q of the resonant RLC tank, not simply the inductor that is important. The energy consumed by the tag back-end circuitry, which will be optimized for low-power consumption, will also reduce the Q of the resonant circuit. Ideally the back-end should dominate the Q of

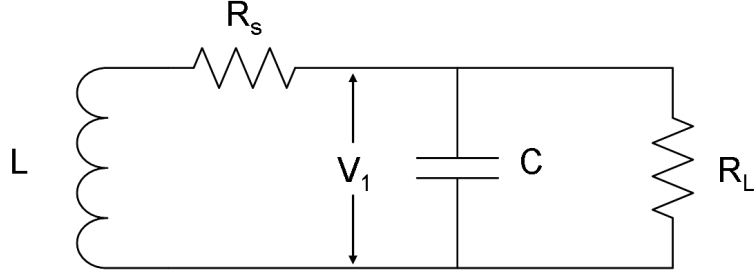


Figure 3.6. Circuit used to calculate the RLC tank quality factor.

the tank. This means that as much coupled energy as possible is transferred to the back-end and not dissipated in the coupling inductor.

3.3.1 Quality Factor of Tag Front End

In order to determine the quality requirements for the tag inductor it is necessary to derive an equation for the tank quality factor that incorporates the inductor quality factor. This is done using the circuit in Figure 3.6.

Quality factor is mathematically defined as:

$$Q = \frac{\omega(\text{time average energy stored in system})}{\text{energy loss per second}} \quad (3.34)$$

For the circuit in Figure 3.6 this is expressed as:

$$Q = \frac{\omega \frac{1}{2} C |V_1|^2}{\frac{1}{2} \frac{|V_1|^2}{R_L} + \frac{1}{2} R_s |I_L|^2} \quad (3.35)$$

Where I_L is the current through the inductor:

$$I_L = \frac{V_1}{R_s + j\omega L} \quad (3.36)$$

Solving for $|I_L|^2$ gives:

$$|I_L|^2 = \frac{|V_1|^2}{R_s^2 + \omega^2 L^2} \quad (3.37)$$

Equation 3.37 can now be substituted into Equation 3.35 and simplified:

$$Q = \frac{\omega C}{\frac{1}{R_L} + \frac{R_s}{R_s^2 + \omega^2 L^2}} \quad (3.38)$$

In order to further simplify this equation it is assumed that the inductor has a quality factor greater than 1, and $\omega^2 L^2 \gg R_s^2$. This is a reasonable assumption, given that the goal is to maximize inductor quality factor.

$$Q = \frac{\sqrt{\frac{C}{L}}}{\frac{1}{R_L} + \frac{R_s}{\omega^2 L^2}} = \frac{1}{\frac{1}{R_L} \sqrt{\frac{L}{C}} + R_s \sqrt{\frac{C}{L}}} \quad (3.39)$$

It is now possible to rearrange the equation in terms of Q_L , the inductor quality factor:

$$Q = \frac{1}{\frac{R_s}{\omega L} + \frac{\omega L}{R_L}} = \frac{1}{\frac{1}{Q_L} + \frac{\omega L}{R_L}} \quad (3.40)$$

3.3.2 Quality Factor Degradation Due to Finite Inductor Quality

In order to determine the required tag inductor quality factor, the effect of Q_L on the overall quality factor must be considered with respect to the power consumed by the tag. Obviously from Equation 3.40 there is a strong dependence on R_L , which represents the power consumption of the back-end circuitry. Currently it is expected that with the application of high- κ dielectrics and improved mobility, transistors on

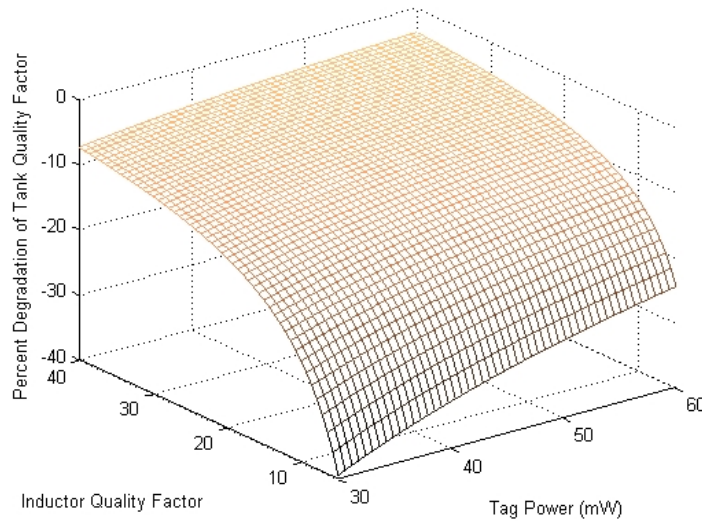


Figure 3.7. Decrease in RLC tank quality factor as a function of tag power and inductor quality factor.

plastic will be able to operate at a supply voltage of 5-10 V with currents of approximately $10 \mu\text{A}$ per transistor. While an exact design will depend on the complexity of the tag, the number of transistors should be in the range of 600-1200. Using these numbers as a guide it is possible to compute the impact of finite Q_L on RLC tank Q . Figure 3.7 shows the results of this simulation, which varied the tag power and Q_L from 5-40.

Significant loss starts to occur in the inductor when Q_L drops below 20, for a wide range of tag power consumption.

3.3.3 Optimizing Inductor Geometry

At low frequencies (such as 13.56 MHz) series resistance is the major cause of energy loss in inductors (76). Planar inductors can be designed in square, spiral, or segmented configurations. There are several techniques to calculate the inductance of a planar structure. Simple equations suitable for hand calculations are given in (68).

For more accurate calculations the Greenhouse method (41) is extremely good, but is not closed-form and requires the assistance of a computer to solve. An improvement to the Greenhouse method that provides closed-form equations is given in (63). The effect of substrate loss on silicon substrates is accounted for in (146).

Simple yet accurate equations for the calculation of planar spiral inductances are given in (85). The inductance of a planar spiral can be estimated using the following method:

$$L = \frac{\mu n^2 d_{avg} C_1}{2} \left(\ln \frac{C_2}{\rho} + C_4 \rho^2 \right) \quad (3.41)$$

where $\mu = 4\pi \times 10^{-7}$, d_{avg} is the average diameter of the structure, ρ is the fill factor defined below, and C_1 , C_2 , and C_4 are geometric constants. For a spiral inductor $C_1 = 1.00$, $C_2 = 2.46$, and $C_4 = 0.20$. The fill factor represents the fraction of the inductor area that contains the turns.

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \quad (3.42)$$

where d_{out} and d_{in} are the outer and inner inductor diameters respectively.

The series resistance of spiral inductors can be calculated using the relationship:

$$R_s = R_{\square} \frac{2\pi r_{avg} n}{w} \quad (3.43)$$

where R_{\square} is the sheet resistance of the metal lines in Ω/\square , r_{avg} is the arithmetic mean of the radii of the inductor coils, w is the line width, and n is the number of coils.

Typically spiral structures will have a higher Q than their square counterparts, for a given inductance (118). In addition, coupling coefficients have been shown to be slightly higher for spiral (or segmented) structures compared to square structures

(12). For these reasons spiral inductors were studied and fabricated exclusively in this work.

3.3.4 Summary of Inductor Quality Requirements

In this chapter inductively coupled RFID systems have been examined in detail, with particular attention paid to the requirements of passive components present in the front-end. The critical component with regard to tag range is the coupling inductor. For low-cost printed RFID tags operating at 13.56 MHz the inductor quality should be greater than 20. Capacitors are also required for resonance, but generally do not have significant loss at low frequency. The following sections deal with the fabrication of capacitors, interconnect, and inductors that are shown to meet the requirements presented.

3.4 Fabrication of All-Printed Passive Components on Plastic

A method of fabricating passive components for RFID that does not involve expensive processes or the use of silicon substrates is highly desirable. The development of a solution-based process on a flexible substrate would allow reel-to-reel fabrication, since it eliminates conventional lithography, and complex substrate processing including chemical vapor deposition (CVD), physical vapor deposition (PVD), and etching. While various groups have printed transistors (22; 119), little work has been performed on the associated passives required for RFID. Some work has been done using substrate transfer (19), and evaporated devices (5), but the scalability and manufacturability at low cost is problematic. For the first time an all inkjet-deposited passive

component process is demonstrated on plastic, including inductors, capacitors, and multilevel interconnects. These passive devices are suitable for use in a RFID system operating in the 100 kHz to 15 MHz range.

3.4.1 Printing Nanoparticle Solutions

Structures such as inductors and capacitors are constructed by printing a set of lines. There are many ways to create lines from discrete drops, and two methods were investigated. The first, which turns out to be problematic, places drops only on top of dried nanocrystals (or plastic) and not onto a drop that is still wet. This was an attempt to minimize running of the material by limiting the amount of solvent in a given area. The drops were printed with drop spacings approximately equal to the drop diameter, so that the drops were next to each other, but not touching. Additional layers were then printed on top of the first layer at a small offset, to create thicker lines. Unfortunately the difference in surface tension between the plastic and previous layers of nanocrystals led to an accumulation of material in particular areas, resulting in a very rough line. Figure 3.8(a) shows an atomic force microscopy (AFM) image of a line printed using this method. The sheet resistance of this line is dominated by the thin areas, and is significantly worse than that of the purely linear printing method, which is discussed next. This method also printed five times slower because the printer head had to cover a much farther distance, as it was continually backtracking.

The best way to create lines from drops is to overlay them in a linear fashion. Drops are deposited using 5 to 15 μm spacing, resulting in 8 to 24 layers of drops at any given point on the line. Figure 3.9(a) shows an AFM image of drops overlaid with linear placement. This method gives lines with uniform distribution of nanocrystals in the printed direction. The cross section, however, is not uniform due to the fact

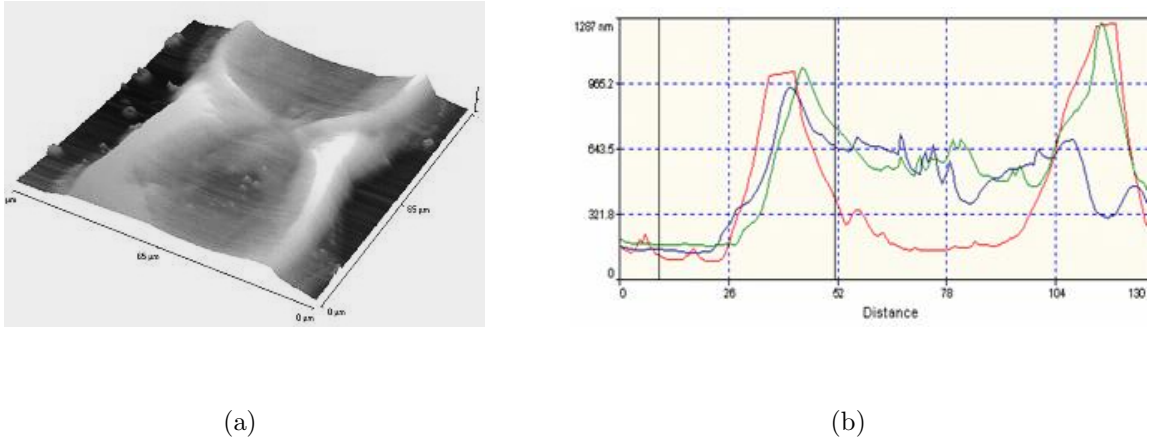


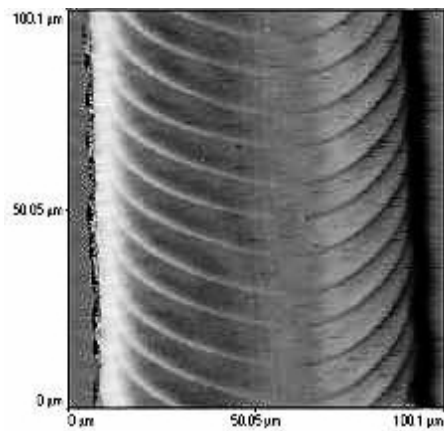
Figure 3.8. (a) AFM of line printed with non-linear method showing extremely rough surface. (b) Cross section.

that printed drops tend to have a “donut” shape with more material around the edges than in the center. This effect was minimized through the use of solvents such as α -terpineol and by heating the substrate (86).

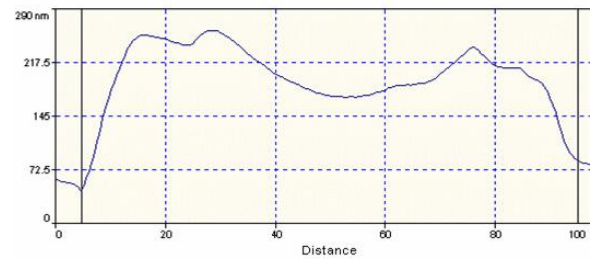
3.4.2 Low Resistance Gold Lines

In order to create thicker lines and reduce sheet resistance, multiple passes are made with the print head and lines are placed directly on top of each other. As the number of layers is increased there is a linear increase in the average line height shown by Figure 3.10. There is a slight increase in line width up to about 3 layers due to different surface tensions between the gold and plastic surfaces. However, after about 3 layers the line width stabilizes at $160\ \mu\text{m}$, which allows the optimization of structures such as inductors, where the lines need to be placed as close as possible.

Printing at elevated temperature helps reduce the “donut” effect on the drops so lines are typically printed at 160 to $190\ ^\circ\text{C}$. The substrate temperature has a significant influence on the quality of the printed gold, which is measured as a percentage of bulk conductivity. Three different substrate temperatures were tested: 160 , 190 and



(a)



(b)

Figure 3.9. (a) AFM of line printed with linear overlay method showing smoother surface. (b) Cross-section of smoother line.

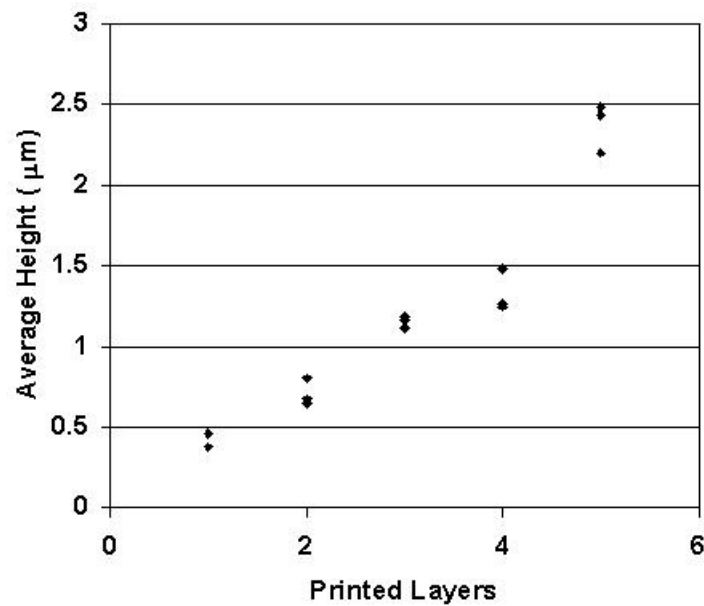


Figure 3.10. Average line height plotted versus number of printed layers.

220 °C, and the resulting conductivity of the gold was measured versus the number of printed layers. Results as high as 40 percent of the bulk conductivity were achieved.

As Figure 3.11 shows, there is a decrease in the quality of the gold as the number of printed layers is increased at temperatures of 160 and 220 °C. For those temperatures printing extra layers of gold does not improve the sheet resistance as much as expected. At 190 °C there was no decrease, so this temperature was chosen for printing. At 160 °C the additional layers may have been put down too quickly, not allowing thiol encapsulant from previous layers to burn off completely. The thiol cannot diffuse through the upper layers and becomes trapped. This is supported by another experiment using toluene as the solvent. In that case the amount of gold printed was significantly less, and the lines were much thinner, therefore allowing more thiol to escape. Conductivities as high as 70 percent of bulk gold were achieved in that case, but the sheet resistance was unacceptable due to the thinness of the lines. An explanation has not been found for the decreased gold quality at 220 °C.

The sheet resistance was measured versus number of printed layers at 190 °C. Figure 3.12 shows the inverse relationship between number of layers and sheet resistance, with values as low as 23 m Ω /□. Now that the deposition of a low-resistance metal layer has been described, an insulating layer is needed to allow two lines to intersect without electrical contact. The development of a printed insulating layer is discussed next, which enables the fabrication of multi-level interconnect.

3.4.3 Crossovers and Interconnect

Pinhole-free films are necessary for the creation of capacitors, center taps for inductors, and interconnect. PI2555 polyimide from HD Microsystems, Inc. was used as the dielectric (2). The polyimide was diluted 2:1 with Pyralin thinner from the same manufacturer.

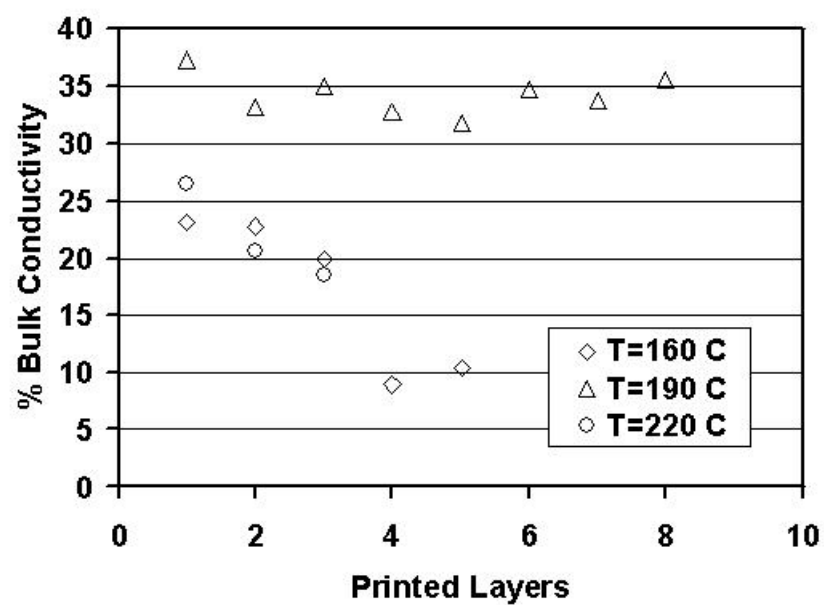


Figure 3.11. Quality of printed gold as a function of bulk conductivity showing no degradation at 190 °C as the number of layers increases.

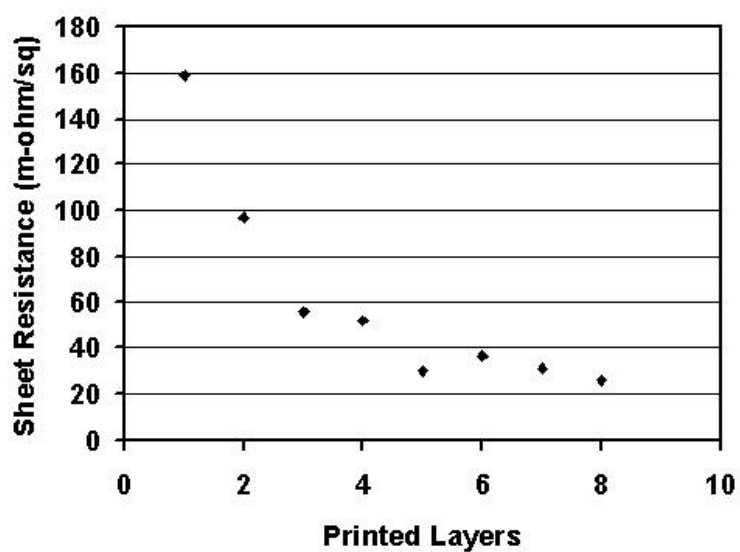


Figure 3.12. Inverse relationship between sheet resistance and number of printed layers at 190 °C.

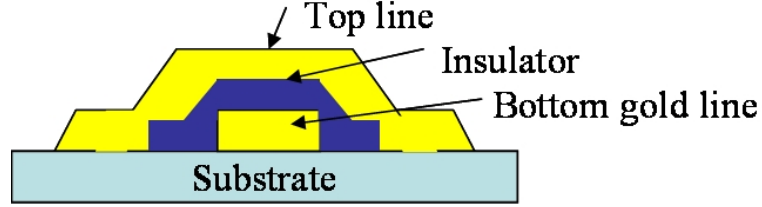


Figure 3.13. Cross section of printed crossover structure enabling multi-layer interconnect.

Polyimide is extremely sensitive to substrate temperature. Pinhole-free films require the correct substrate temperature and the correct drop spacing. If too much material is deposited the polyimide agglomerates and does not form a film. Temperature was varied from 50 to 110 °C and drop spacing was varied from 50-90 μm in the x- and y-directions. Drops were printed every 175 milliseconds (ms). Rectangular pads of polyimide were created using a linear array of lines, adjusting the line spacing to equal the drop spacing. The best conditions were found using a substrate temperature of 90 °C with drop and line spacing of 60 μm . The surface of this film is quite rough; with an average thickness of 1 μm .

These films are used as an insulating layer allowing the creation of multi-layer interconnect (Figure 3.13). The crossing line resistance, shown in Figure 3.14, tests the step coverage of the top gold line. The layers in the figure represent the number of printed layers of gold in the bottom conductor. Good step coverage is achieved for gold lines up to 2.5 μm thick. Figure 3.15 shows the insulating properties of the dielectric versus number of printed layers. Three layers of dielectric are needed to ensure isolation, which results in an average film thickness of 3 μm .

3.4.4 Inductors

Spiral inductors of 350 nH were fabricated using three layers of printed gold. Since the inkjet printer is not limited to Manhattan designs, spiral inductors were fabri-

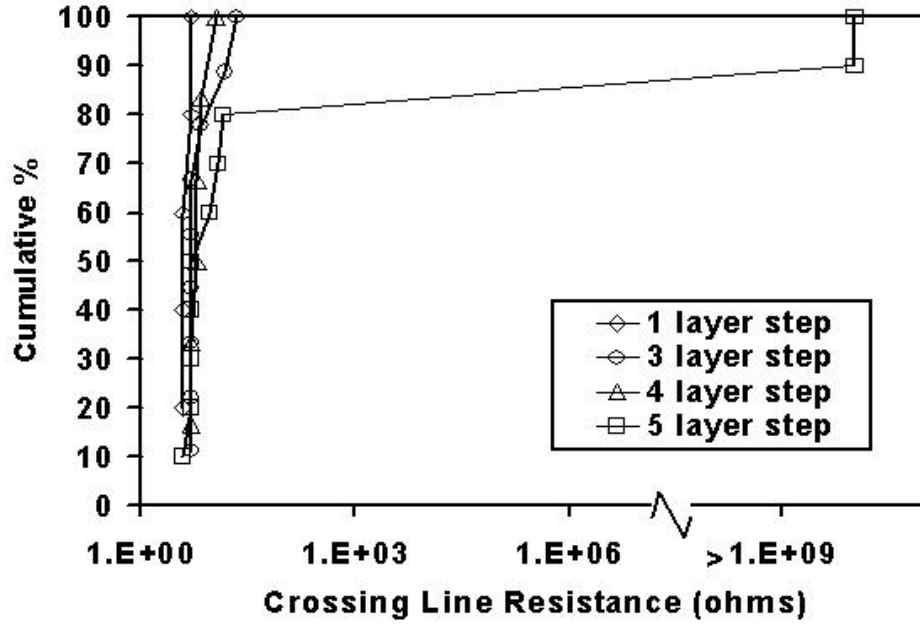


Figure 3.14. Good step coverage is achieved for gold lines up to $2.5 \mu\text{m}$ thick. Crossing line resistance represents the resistance of a line passing over another insulated line. High crossing line resistance indicates an open.

cated rather than square inductors. Spiral inductors are superior to square inductors because they give higher quality factors for a given inductance. These structures were created in a piecewise-linear manner with 32 segments. The measured inductance agreed extremely well with simulation using ASITIC (100). The inductors had radii of $5000 \mu\text{m}$, line widths of $160 \mu\text{m}$, line spacing of $100 \mu\text{m}$, and five turns. Center taps were achieved using three layers of printed polyimide as an insulator, and then printing a line from the innermost turn across the device to the outside where connections to other devices can be made.

Figure 3.16 is a picture showing one of these devices. Resistance is the major loss mechanism for these inductors. The series resistance was approximately 58Ω , giving a quality factor (Q) of 0.5 at 13.5 MHz. This value is too low for use in RFID circuits, but additional layers of gold would improve the quality factor of this device to approximately unity. This inductor geometry is also not optimal for the given

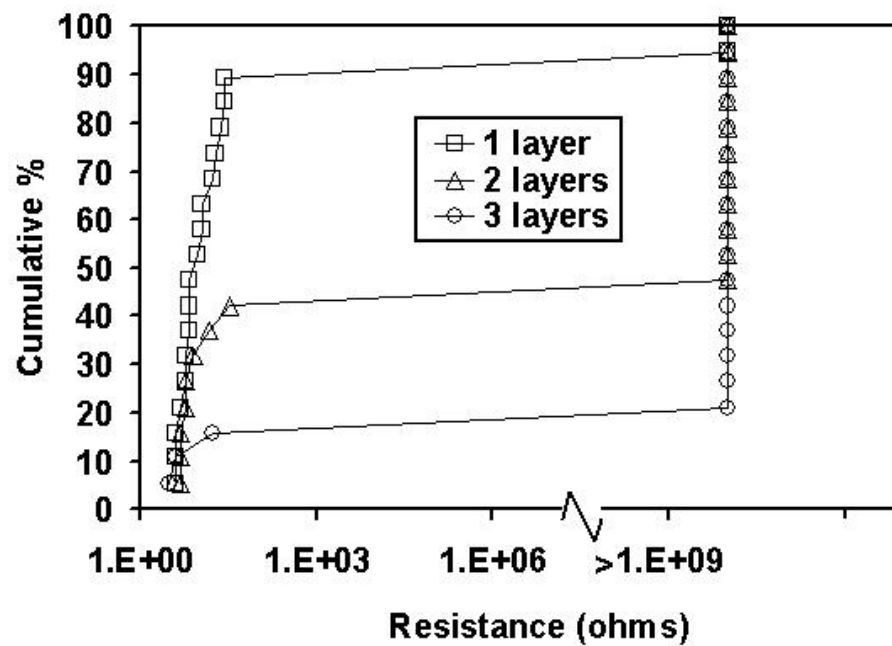


Figure 3.15. Three layers of polyimide provides adequate isolation. The resistance measured is between the top and bottom conductors. High resistance indicates an open circuit and therefore good isolation.

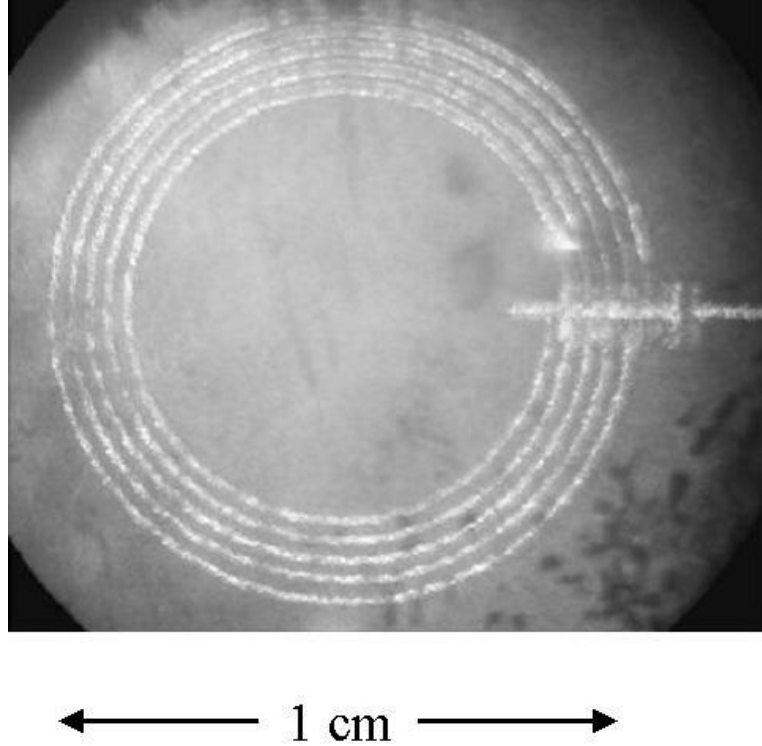


Figure 3.16. 350 nH inductor complete with contact to center coil achieved using the crossover process.

inductance value. An optimized structure would use additional turns to fill more area in the center of the inductor. Using a sheet resistance of $23 \text{ m}\Omega/\square$, simulations were run using ASITIC to determine the highest achievable Q for a $1 \mu\text{H}$ spiral inductor using this process. Inductor radius was varied and the number of turns was adjusted to give the correct inductance, and then Q was calculated at 13.5 MHz. Line widths were kept at a constant $160 \mu\text{m}$, and line spacing was fixed at $50 \mu\text{m}$. Quality factors of 2.5 are obtainable for $1 \mu\text{H}$ inductors. As Figure 3.17(a) shows, the radius of the inductor does not have a large effect on the inductor quality. Hence inductors should be made as large as possible to maximize the coupling factor between reader and tag inductors. Further simulations indicated that a larger line width would increase the Q to 5, for inductors of the same value. It is possible to print wider lines by essentially printing two inductors at the same origin, one with a slightly larger radius.

Variation of the line spacing was also investigated. Using smaller line spacing increases the inductance per length of printed lines. However, the gain in Q as line spacing is reduced from 100 to 20 μm is fairly small at 10 percent. Figure 3.17(b) shows the variation of Q versus line spacing for 1 μH devices with fixed radius of 5000 μm . Larger inductors generally give higher quality factors. The highest simulated Q (at 13.5 MHz) was 9.5 for a large inductor with 15000 μm radius, 300 μm line width, 20 μm line spacing, and 20 turns. The inductance was 12.7 μH , which is slightly large for this application.

These attempts to optimize the inductor structure show that printing inductors using gold nanoparticles results in inductors with fairly low quality factors. Yield is also low due to the extremely long time necessary to print 5-8 layers of gold. Using a system where drops are printed one at a time (such as our system) it takes 7-8 hours to print a single inductor, which is far too long for a manufacturable process. Fabrication time would be even longer if multiple coils were used to generate wider lines. For these reasons an alternate solution to fabricating high-quality inductors is presented in Section 3.6, which is based on using an inkjet printer to pattern the inductor and a subsequent electroless plating of copper to grow a highly conducting layer.

3.4.5 Capacitors

Parallel plate capacitors were fabricated by first printing a bottom plate, then printing three layers of polyimide, and then printing a top contact. The structure is shown in Figure 3.18. The dielectric must be as thin as possible to create capacitors large enough for use at 13.5 MHz. In order to get thin dielectric films that provided good isolation the gold bottom plates had to be smooth. Rough bottom plates with a thin insulating layer results in shorted capacitors. Gold was deposited at 45 °C

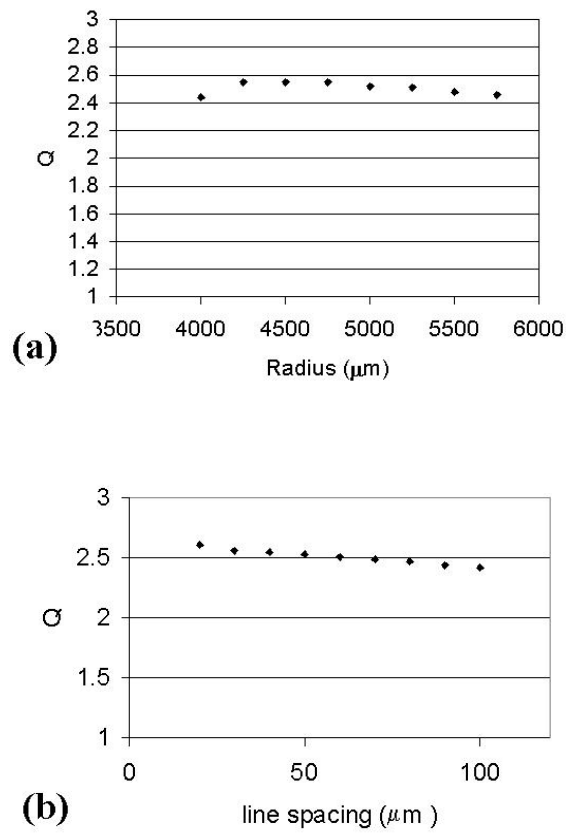


Figure 3.17. (a) Simulated results showing variation of Q with inductor radius at 13.5 MHz. Realizable quality factor is fairly independent of inductor radius. (b) Quality factor decreases slightly as line spacing is increased.

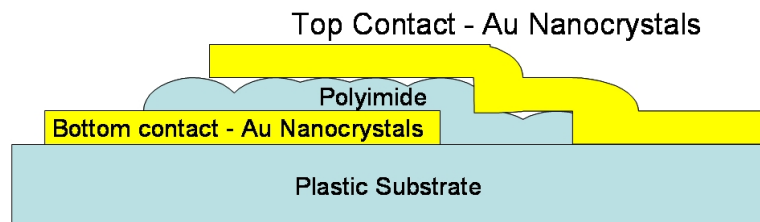


Figure 3.18. Cross-section of a printed capacitor.

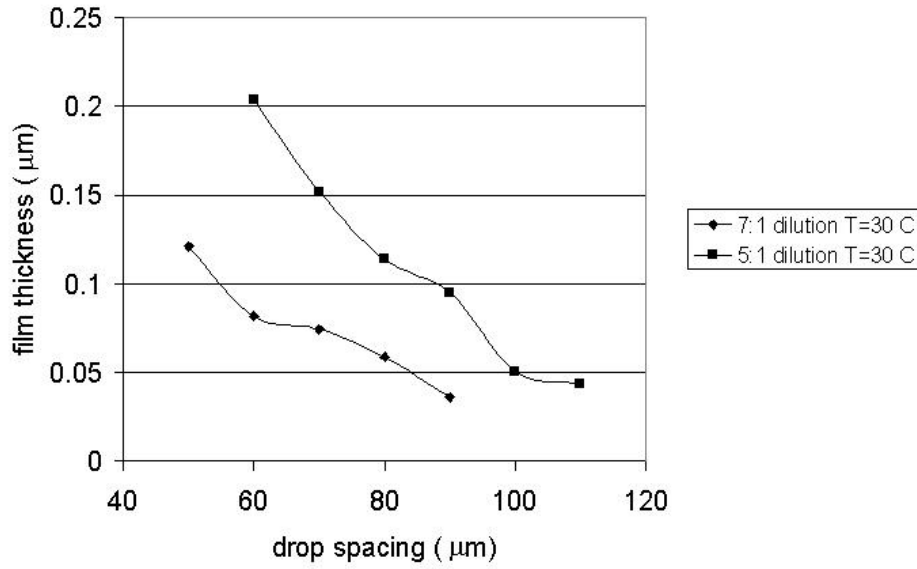
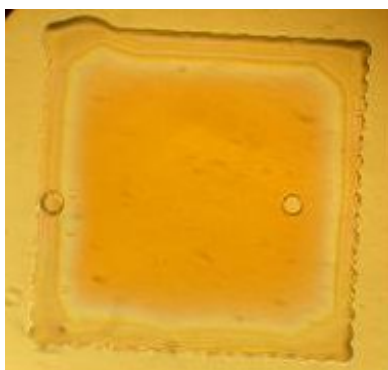


Figure 3.19. Effect of drop spacing on polyimide film thickness at 30 °C.

so that the material is allowed to flow on the surface without drying too quickly. Once a smooth gold layer was deposited and annealed a thin layer of polyimide was printed. The polyimide was diluted using the same thinner as before to 3:1, 5:1, and 7:1, and a drop spacing and temperature matrix was run to determine optimal printing conditions. Temperatures of 30-110 °C were tested with drop spacings of 50-120 μm in the x- and y-directions. Film thickness was as low as 35 nm. Substrate temperatures of 60 °C and higher resulted in films that were extremely rough because the lines dried before the next line was printed. The surface roughness disappeared at temperatures below 60 °C, allowing the material to remain liquid as the adjacent row of drops was printed. Temperatures of 30 and 45 °C gave smooth films. Figure 3.19 shows the effect of dilution and drop spacing on film thickness. Photos of films printed at 30, 60, and 110 °C are shown in Figures 3.20(a)-3.20(c). At elevated temperatures the polyimide will dry in lines, and then eventually individual drops can be seen. The delay between printing each drop was approximately 25 ms.

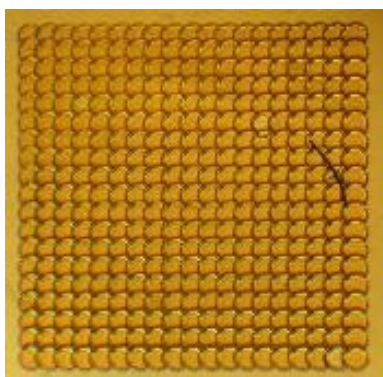
Capacitors were fabricated using the smooth gold pads and thin dielectric. Poly-



(a) 30 °C

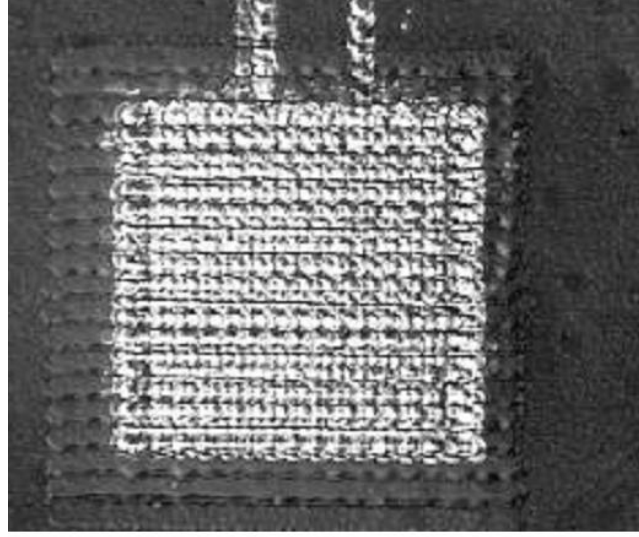


(b) 60 °C



(c) 110 °C

Figure 3.20. Effect of substrate temperature on polyimide surface using 80 μm drop spacing.



←1500 μ m →

Figure 3.21. All-printed capacitor fabricated on plastic.

imide diluted to 7:1 was deposited at 45 °C using drop spacings of 70 μ m. In order to ensure isolation between capacitor plates three layers of polyimide were used, even though this decreased the capacitance. Capacitors fabricated with three layers of polyimide proved to be the most reliable, with high yield. The resulting 600x600 μ m capacitors had an average capacitance of 42 pF. Figure 3.21 shows an all-printed capacitor fabricated using this process. The film thickness is approximately 340 nm, allowing the fabrication of capacitors suitable for use in RFID applications. All devices tested had a breakdown voltage greater than 70 V. The dispersion characteristics of the capacitors were measured to see if there was a degradation of the dielectric at higher frequencies. Capacitance was measured as the frequency was swept from 1 to 13 MHz. Figure 3.22 shows that polyimide is a viable dielectric material for low-frequency RFID applications. The relative permittivity was calculated to be 4.5, which is slightly higher than the manufacturer's value of 3.3 (2). This is due to surface roughness of the capacitor plates, and thickness variation inherent in printing.

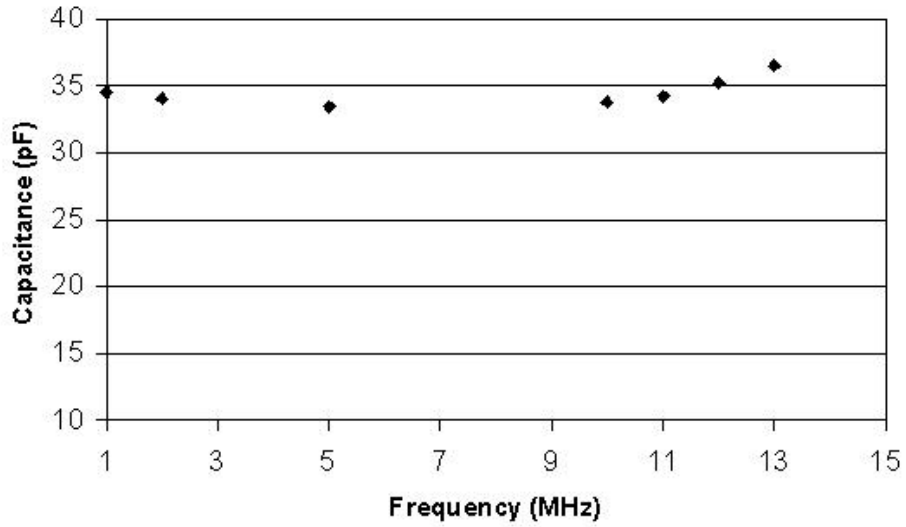


Figure 3.22. Dispersion characteristics of printed capacitors. The upturn at high frequency is within the error bars of the measurement.

3.5 Discussion

This all-inkjet deposited process is capable of producing interconnect and capacitors suitable for use at the lower frequencies used for RFID (i.e. 125 kHz and 13.56 MHz). Optimization of the inductor structure has shown that quality factors suitable for data and power transfer are not achievable with printing alone. However, the structural optimizations will benefit inductor Q regardless of the sheet resistance of the metal layer. Large inductors with wider line widths achieved the highest quality factors. For a given inductance radius and line spacing did not have a major effect on quality factor, so there is not a large penalty for using large radii to increase coupling from reader to tag or using a large line spacing to increase inductor yield.

It is worth discussing the potential drawbacks of using gold nanoparticles, in terms of cost and performance. Processes have been developed for silver and copper nanocrystals as a potential alternative. Although gold is a fairly expensive material, cost models indicate that throughput will dominate over other costs in the manu-

facture of RFID tags. Moving to a different metal would decrease cost slightly, but the main advantage would be that silver and copper both have bulk conductivities that are approximately 50 percent higher than gold. It remains to be seen, however, if that translates into improved sheet resistance when the nanoparticles are printed. The conductivity is most likely limited by the ability of the encapsulant to leave the film during the anneal, and therefore copper and silver nanoparticles may not show as much benefit as their bulk conductivities may indicate. In addition, copper must be annealed under an inert atmosphere (such as nitrogen) to prevent oxidation. This adds to the cost and potentially lowers the throughput of a reel-to-reel process.

Other potential applications exist for this technology. Small high-Q inductors (3 nH) can be fabricated for use in high frequency filters, where loss is due primarily to eddy currents in the substrate, rather than series resistance. Polyimide may not be suitable for use as a dielectric at gigahertz frequencies, however, there are materials known to function at these frequencies such as benzocyclobutene (BCB), which could be printed. This would allow the fabrication of discrete and distributed filters useable at gigahertz frequencies.

3.6 High-Quality Inductors Fabricated Using Inkjet Printing and Electroless Plating

At the lower frequencies, power for RFID tags is coupled inductively, necessitating the use of inductors with high quality factor (Q) to maximize range. There is great interest in using printing to realize these inductors since it lowers the cost of the tag; unfortunately, to date, printed technologies have not provided the requisite low resistance conductors required for high-Q inductors. Therefore, most low-frequency tags

today are realized using conventional etch or cut-based techniques, which are expensive (36). The components demonstrated previously were adequate for the internals of RFID circuits, but the Q of the inductors was inadequate for power coupling. Here a novel high-quality inductor technology based on a combination of inkjet printing and aqueous deposition is demonstrated on plastic. The resulting metal layers have extremely low resistance. This leads to a significant improvement (10-20X) in inductor quality factor over printed nanoparticles alone. Finally, therefore, performance levels required for inductively-coupled RFID are realized via a low-cost method.

3.6.1 Electroplating Problems

Plating technologies are commonly used to realize metal lines in microelectronics. A simple improvement to printed conductors would be to electroplate copper on top of the printed gold lines. Copper has extremely high conductivity and electroplating processes are well understood. For low-cost RFID on reel-to-reel plastic substrates, conventional electroplating is not an option since electrical contact to the structures to be plated is not conveniently available and DC path problems can occur. For instance a series capacitor will isolate areas of the circuit by blocking current.

The biggest problem, however, is due to the spiral geometry of inductors. Electroplating uses an externally supplied current as a source of electrons, and the current must flow through the structure. As the electroplating current flows through the structure a potential is generated that opposes the applied potential (Figure 3.23). Unfortunately over a large spiral structure such as an inductor this causes a nonuniform potential and therefore an uneven plating rate. The electroplating current can be expressed as:

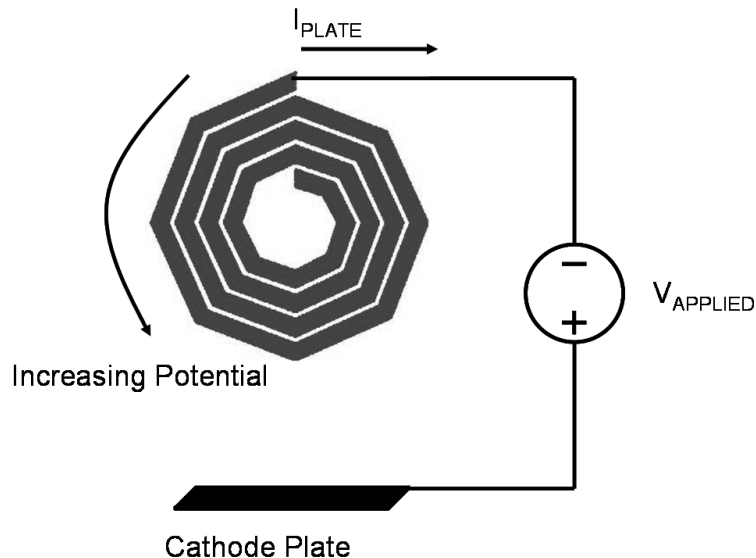


Figure 3.23. Electroplating current causes a potential that opposes the applied potential.

$$\ln i = \ln i_0 - \frac{\alpha n F \eta}{RT} \quad (3.44)$$

where η is the overpotential ($E - E_0$), i is the current density, i_0 is the exchange current density, α is the cathodic electron transfer coefficient, n is the number of electrons, F is Faraday's constant, R is the universal gas constant, and T is temperature.

Rearranging to solve for η :

$$\eta = \frac{2.3RT}{\alpha n F} \log i_0 - \frac{2.3RT}{\alpha n F} \log i \quad (3.45)$$

This expression was empirically stated by Tafel circa 1905, and is known as the Tafel equation (132):

$$\eta = a + b \log i \quad (3.46)$$

Figure 3.24 shows the relationship between potential and plating rate. At low po-

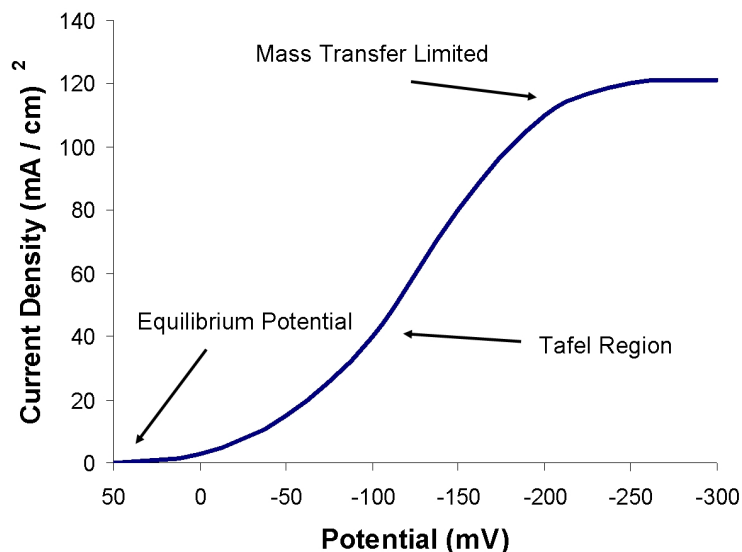


Figure 3.24. Electroplating current density versus potential curve.

tentials the curve obeys the Tafel Equation, which shows an exponential dependence of rate on potential. At high bias the reaction becomes mass transfer limited and the rate becomes independent of potential. While this would seem to eliminate the problem posed by the uneven potential across this structure, this regime is usually avoided because the deposition has very poor quality and high porosity.

When plating a spiral inductor, the potential drop is so significant that even with gold lines printed using the lowest achievable printed sheet resistance ($23 \text{ m}\Omega/\square$) only the outer few coils of an inductor are plated. The inner coils are not plated at all.

Electroless plating presents an intriguing solution to these problems, since it may be used to plate metal over printed metallic catalytic layers without requiring electrical contact. Plating occurs evenly over the entire circuit, and the seed layer does not need to conduct.

3.7 Electroless Deposition - A Brief Introduction

The term “electroless deposition” is used to describe a system where metals are deposited from solution without the need for an electrical current. Often, though, it is used synonymously with similar processes such as chemical bath deposition (CBD), successive ionic-layer absorption and reaction (SILAR), and liquid-phase deposition (LPD), to describe deposition from an aqueous solution. To avoid confusion, “electroless deposition” will refer to only the deposition of metals in this work. The other aqueous deposition methods will be covered in Chapter 4.

Electroless plating takes place in a bath of metal ions, similar to electroplating, but in this case it is a reduction-oxidation (redox) reaction that converts the ions to metal rather than an electrical current. In a redox reaction, as the name suggests, one species is oxidized and the other is reduced. The reaction is completed by the transfer of electrons from the oxidized to the reduced species.

Copper electroless processes have been known for roughly 60 years, with the first report in 1947 (92). The most common application has been the through-hole plating of printed-circuit boards (PCBs) (10). The advantages of electroless plating over electroplating have made it an attractive process for MEMS (145; 144), improving the conductivity of interconnect layers on silicon substrates (60) (121), and for the fabrication of on-chip transmission lines (64). The use of electroless plating to improve the quality of on-chip inductors was studied by Jiang *et al.* (56).

The remainder of this chapter covers the basic concepts of electroless plating, followed by a demonstration of electroless plating applied to printed electronics. High-quality inductors are fabricated by printing a gold nanoparticle solution, which is shown to act as a seed layer for electroless plating, followed by an electroless copper deposition to grow a highly conductive metal layer.

3.7.1 Immersion Plating

Immersion plating is the simplest form of electroless plating and involves only a metal film and a solution of metal ions. A surface layer of metal with high electrochemical potential is replaced by atoms of lower electrochemical potential. Conceptually this is a very simple case of atoms which are more electronegative taking electrons away from atoms which are more electropositive. Unfortunately once the surface of the original metal is covered the reaction ceases, which limits the thickness of deposited films. Film thicknesses of approximately $1\text{ }\mu\text{m}$ are achievable.

An example of immersion plating is shown in the following reaction, where a zinc is immersed into a solution of cupric ions. The zinc is displaced at the surface and copper is deposited.



When dealing with redox reactions it is useful to split 3.47 into reduction and oxidation half reactions:



In order to determine whether a reaction will proceed spontaneously it is necessary to examine the standard electrode potentials (E^0) for the two half reactions. The standard electrode potentials are values which represent the measured potential differences between an electrode and a standard reference electrode under standard conditions. Standard conditions are defined as follows: solids must be the pure compound, gases are at a pressure of 100 kPa (1 atm), and solutions must be 1 molar

Table 3.2. Standard reduction potentials for selected half reactions.

Reaction	E^0 (V)
$\text{Zn}^{2+} + 2\text{e}^- \rightleftharpoons \text{Zn}$	-0.76
$\text{Cu}^{2+} + \text{e}^- \rightleftharpoons \text{Cu}^+$	1.58
$\text{Cu}^{2+} + 2\text{e}^- \rightleftharpoons \text{Cu}$	0.340
$\text{Ag}^+ + \text{e}^- \rightleftharpoons \text{Ag}$	0.799
$\text{Ni}^{2+} + 2\text{e}^- \rightleftharpoons \text{Ni}$	0.230
$\text{Fe}^{2+} + 2\text{e}^- \rightleftharpoons \text{Fe}$	-0.44
$\text{Li}^+ + \text{e}^- \rightleftharpoons \text{Li}$	-3.040
$\text{K}^+ + \text{e}^- \rightleftharpoons \text{K}$	-2.936
$\text{Al}^{3+} + 3\text{e}^- \rightleftharpoons \text{Al}$	-1.662
$\text{Au}^+ + \text{e}^- \rightleftharpoons \text{Au}$	1.692
$\text{Pt}^{2+} + 2\text{e}^- \rightleftharpoons \text{Pt}$	1.18

(mol/L) concentration. The standard reference electrode is arbitrarily chosen as the hydrogen electrode, commonly referred to as the Standard Hydrogen Electrode (SHE). The SHE half reaction is shown below:



A table of standard electrode potentials for various metals is given in Table 3.2 (71).

The overall standard electrode potential is the sum of the potentials for the half reactions. For instance, the value $E^0 = 1.1 \text{ V}$ in 3.47 is the sum of the E^0 values for the half reactions 3.48 and 3.49. Of course, a very small percentage of reactions are ever run under standard conditions. To account for this the Nernst equation 3.51 takes into consideration different temperatures and concentrations (52).

$$E = E^0 - \frac{RT}{nF} \ln Q \quad (3.51)$$

where R is the universal gas constant, T is the temperature, n is the number of moles, F is Faraday's constant, and Q is the reaction quotient. For the general reaction:



the reaction quotient is defined as:

$$Q = \frac{[\text{C}]^c [\text{D}]^d}{[\text{A}]^a [\text{B}]^b} \quad (3.53)$$

Thus, it is possible to calculate the overall electrode potential for a given reaction. In order to determine if the reaction is spontaneous it is necessary to consider the change in Gibbs free energy ΔG . The relationship between electrode potential and Gibbs free energy is given in Equation 3.54:

$$\Delta G = -nFE \quad (3.54)$$

Spontaneous reactions always have $E^0 > 0$ and $\Delta G < 0$. This means that the products of a reaction are always at an energy less than the reagents, and there is a net release of energy in the system.

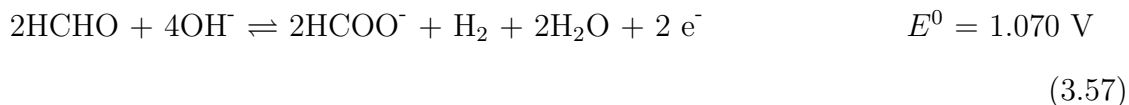
3.7.2 Continuous Electroless Deposition of Copper

While immersion plating is conceptually simple, it is not very useful for depositing thick conducting layers. Not only must the seed layer be thick and more electropositive than copper, but once the surface is covered the reaction stops. A reaction that is continuous is necessary for the fabrication of thick metal layers.

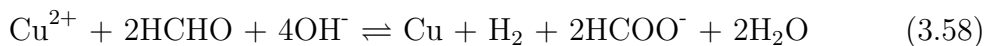
Since deposition of copper is still the ultimate goal, the reduction half reaction is still the same as in the immersion process:



In order to make the reaction continuous the reducing agent must be in solution rather than on the substrate. Formaldehyde is commonly used as a reducing agent in electroless systems. Allowing the reaction to take place on the surface of the substrate places no limitations on the thickness of grown film. The oxidation of formaldehyde can take place in either acidic (Equation 3.56) or basic (Equation 3.57) conditions, shown below:

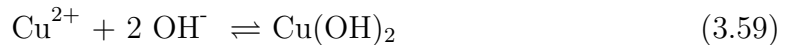


Because the standard electrode potential is higher under basic conditions, the overall reaction:



is more thermodynamically favorable under basic conditions. Therefore electroless copper reactions that use formaldehyde as a reducing agent are always run basic.

However, copper in a basic solution will tend to spontaneously precipitate and form copper hydroxide:



In order to avoid this undesirable reaction a complexing agent is used to stabilize copper. Common complexing agents are sodium potassium tartrate (Rochelle salts), ethylenediaminetetraacetic acid (EDTA), glycolic acid, and triethanol amine. Typically Rochelle salts are used for low-temperature and low plating-rate applications (77), and EDTA is used for higher temperatures and plating rates (15). For this work EDTA was used exclusively.

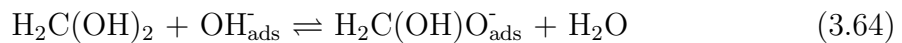
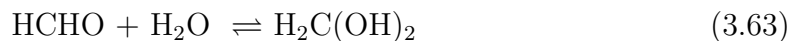
The complexing reaction is:

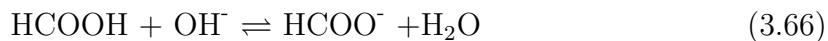
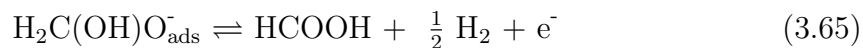


And the reduction reaction now proceeds in two steps:

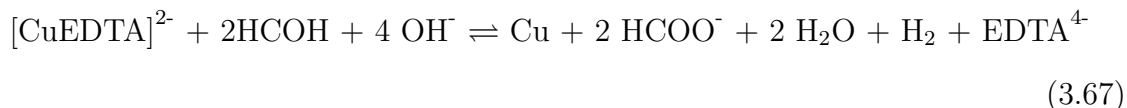


The oxidation reaction also occurs in several steps, as shown below:





Combining the oxidation and reduction half reactions the overall balanced reaction is written:



3.7.3 Rate of the Electroless Reaction

Now that the mechanism of the electroless deposition has been considered, it is worthwhile to examine the factors that determine the rate of the reaction. In general, the rate of a reaction is proportional to the concentrations of reagents and products. A reaction proceeds until equilibrium is achieved, where the rate of the forward and reverse reactions are equal. In the case where one of the products is a gas that leaves solution the reaction is driven until one of the reagents is completely consumed, or another side reaction becomes dominant. For the electroless process described above, the rate equation can be generally written as:

$$r = \kappa [\text{Cu}^{2+}]^a [\text{OH}^-]^b [\text{HCHO}]^c [\text{EDTA}]^d \quad (3.68)$$

where κ is the temperature-dependent rate constant and a-d are constants that determine the effect of concentration on the rate. Typically the constants a-d are dependent on the stoichiometry of the balanced reaction, but in the electroless process several

factors make determining the rate constants more complicated. First, as the reaction proceeds the rate tends to decrease with time (27; 26). Also the surface concentration of reagents varies differently than in solution (24). The presence of complexing agents often slows the reaction down, so accelerants such as pyridine (102) or cyanide are added to increase the reaction rate. Also stabilizers are added to prevent dust from acting as a nucleation site and causing precipitation of copper in solution (125; 53). A summary of the effects of different additives is available in (111).

The temperature dependence of the reaction follows the Arrhenius equation:

$$\kappa = Ce^{-\frac{E_a}{kT}} \quad (3.69)$$

where κ is the rate constant, C is a temperature-independent constant, E_a is the activation energy, k is Boltzmann's constant, and T is the temperature.

There have been several studies which attempt to determine the constants stated above and are summarized in (25). Combining Equations 3.68 and 3.69 the authors empirically determined the following rate law:

$$r = 2.81 \frac{[\text{Cu}^{2+}]^{0.43} [\text{HCHO}]^{0.16}}{[\text{OH}^-]^{0.70} [\text{EDTA}]^{0.04}} e^{11.5 \frac{T-313}{T}} \quad (3.70)$$

From Equation 3.70, the rate is only slightly dependent on the concentration of complexing agent EDTA. This is not unexpected, since the rate-determining step is generally accepted to be the cleavage of the carbon-hydrogen bond of methylene glycolate (Equation 3.65). However, should the concentration of EDTA become excessive, release of copper from the complexing agent would become the rate determining step, so care must be used when choosing the ratio of Cu^{2+} to EDTA.

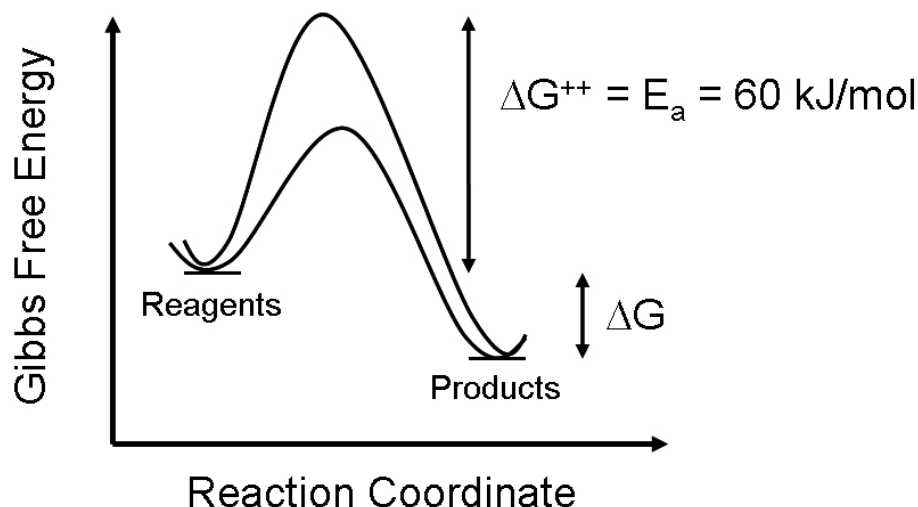


Figure 3.25. Gibbs free energy diagram showing reduced activation energy in presence of metal catalyst.

3.7.4 Metal Catalysis

Having a reaction that is thermodynamically favorable does not mean that the reaction will proceed at an observable rate. Figure 3.25 shows a Gibbs Free Energy diagram for the electroless process. As the reaction proceeds in the forward direction it must go through a high-energy transition state. From the Arrhenius equation 3.69 the rate is exponentially dependent on the activation energy E_a . For the electroless copper reaction the activation energy E_a is approximately 60.9 kJ/mol (126), which results in a negligible rate at temperatures of interest. Thus, no deposition will occur without the presence of a catalyst.

The presence of a metal catalyst results in the lower curve of Figure 3.25, where the activation energy is significantly reduced. It is this relationship that is exploited to give selective copper deposition. Several metals including gold (30), silver, nickel, copper, platinum, and palladium (6) can be used to catalyze the electroless copper reaction. Activation energies for the various catalysts are shown in Table 3.3.

The activation energy for the catalyst is only important until the catalyst is cov-

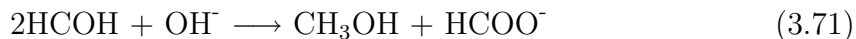
Table 3.3. Activation energies for the electroless copper process with various catalysts.

Metal	E_a (kJ/mol)	Reference
Cu	49-50	(127) (103)
Au	29	(103)
Ag	29	(103)
Pt	38	(103)
Pd	24	(103)
Ni	46	(103)

ered, which happens fairly quickly. After the seed layer has been covered the reaction becomes autocatalytic, which means the deposited copper acts as a catalyst for further plating. In theory there is no limit to the thickness of grown films. In practice, however, side reactions will eventually become dominant, and bath lifetime is finite.

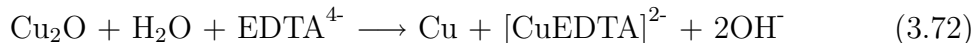
3.7.5 Competing Side Reactions

In addition to the plating reaction there are several side reactions that occur in solution. These undesirable reactions affect bath lifetime and maximum plating temperature. The Cannizzaro reaction, shown in Equation 3.71 limits the lifetime of the bath by consuming the formaldehyde reducing agent. There is no way to prevent this reaction from occurring, but it's rate can be limited by keeping the bath temperature below 70 °C. The reaction bath will stop plating after only a few minutes if the temperature is too high. At lower temperatures the rate of the plating reaction is faster than the Cannizzaro reaction, and bath lifetime is not limited by this side reaction.



Another potential problem occurs because the cuprous (Cu^+) ion is not complexed

by EDTA, and any in solution will tend to form Cu_2O . Cu_2O then reacts further under the reaction conditions to form copper, shown by the reaction below:



Free copper in solution is a major concern, because it will catalyze further reduction of copper. This causes a chain reaction to occur where the plating bath will crash out with uncontrolled precipitation of copper. This problem can also occur as a result of another side reaction, where the evolved hydrogen gas can act as a secondary reducing agent and cause copper precipitation. Aeration of the bath is a known solution to this problem, and most commercial baths are aerated. Bath lifetime was increased by four times when aerated with just a simple bubbler. Using a diffuser to increase the surface area of the bubbles would increase lifetime further, but was not found to be necessary in this work. Under sufficient aeration bath lifetime can be extended up to 20X (45).

3.7.6 Printed Nanoparticles as a Seed Layer

Gold (50) and silver nanoparticles were found to catalyze the electroless plating reaction. The nanoparticles were printed using a very dilute solution to avoid significant deposition of metal. Using thick conducting lines as a seed layer is problematic because the lattice mismatch between copper and gold (which is about 11 percent) causes stress which results in delamination of the inductor. Inductors fabricated with very dilute nanoparticle solutions passed the industry-standard “scotch tape test” of adhesion.

A schematic of the process is shown in Figure 3.26. After the nanoparticles are

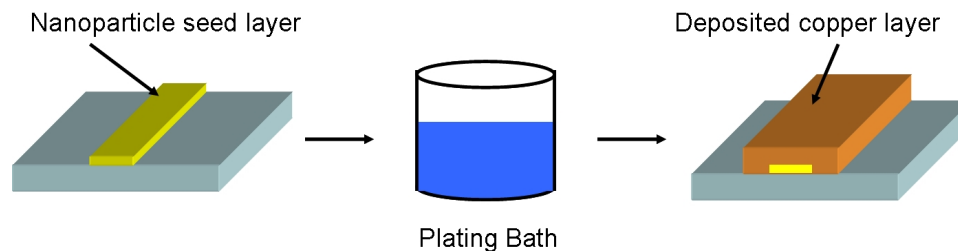


Figure 3.26. Process flow for electroless plating on nanoparticle seed layer.

printed and annealed the entire substrate is immersed into the plating solution. After a prescribed amount of time the substrates are removed and rinsed in water.

3.7.7 Seed layer preparation

The seed layer was printed using a solution of 0.2 weight-percent oleic acid-encapsulated silver nanoparticles in dihydroterpineol (DHT) solvent. Dihydroterpineol is very similar in structure to α -terpineol, and has similar properties. The change was made because the α -terpineol sourced from Aldrich was only 90% pure and tended to strip the encapsulant from the silver nanoparticles. This was not a problem with gold nanoparticles because the thiol-to-gold bond is more stable than the thiol-to-silver bond. Silver is much more reactive than gold and will oxidize more readily, making the Ag-S-C bond less stable (78). Dihydroterpineol was available in much higher purity from International Flavors and Fragrances Inc. (DHT and α -terpineol are most commonly used for pine or lavender perfumes). 2 atomic-percent of palladium organometallic was added to improve adhesion to the plastic substrate. DuPont Melinex was again used as the substrate, and was heated to 160 °C. In addition to having good thermal stability, the DuPont Melinex also showed excellent resistance to the corrosive plating bath. The substrates could be left in the plating

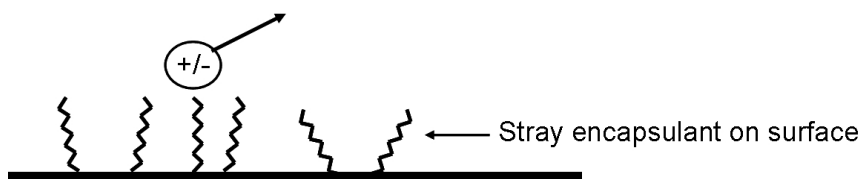


Figure 3.27. Polar reagents are repelled by the non-polar encapsulant.

solution for hours without showing any visible sign of deterioration, such as softening or losing transparency.

After printing the substrates were annealed at 190 °C to drive off the nanoparticle encapsulant. Before plating, the substrates were rinsed in methanol to remove any remaining encapsulant from the surface. This step proved to be critical since any remaining non-polar encapsulate on the surface will interfere with the polar reagents in the plating solution, and the reaction will not initiate. It was found that both the 190 °C anneal and rinse in methanol were necessary to get reliable initiation of the electroless reaction.

3.7.8 Plating Solution

The plating solution consisted of 4.75 g of copper sulfate pentahydrate ($\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$), 8.5 g of ethylenediaminetetraacetic acid (EDTA) complexing agent, 0.5 mL of RE-610 surfactant, 18 μL pyridine accelerant, 2 g paraformaldehyde reducing agent, and 250 mL DI water. The RE-610 surfactant is commonly used in electroless processes because it prevents hydrogen from forming bubbles on the surface of the substrate. As hydrogen is evolved during the reaction large bubbles will cover areas of the metal and prevent the reaction from proceeding in those locations. This is obviously unacceptable, but easily solved with a very small amount of surfactant.

First the copper sulfate is mixed into the DI water to form a royal blue solution.

Then the EDTA is added which causes the solution to turn light blue. Not all of the EDTA will be soluble until the base is added. Potassium hydroxide (KOH) pellets are added until the pH is 13.2. At this point the EDTA will be completely soluble (and complexing the copper), and the solution will return to the royal blue color. At this point the solution is allowed to heat up to 60 °C. RE-610 and pyridine are added after the solution is heated, but they could be added earlier without issue. The paraformaldehyde is the final reagent added. After paraformaldehyde addition the solution is allowed to mix for three minutes to ensure equilibrium. Then the substrates are added and left horizontal in the bath. Plating should occur in less than two minutes. The bath was kept at 60 °C and stirred at 180 rpm using a Teflon stir bar. A simple bubbler made from a glass pipette was used to aerate the bath during the deposition to increase bath lifetime (7).

3.7.9 Plated Copper Results

A 60 μm diameter print head was used to deposit the seed layer, resulting in lines approximately 80 μm wide. The lines here were somewhat thinner than in the previous chapter because the drop spacing was increased from 5 to 15 μm , and the dynamics of the solvent evaporation changed because the solutions were now much more dilute.

Plated line width increases linearly with plating time and although we expect isotropic growth there is a preference for horizontal rather than vertical growth as shown in Figure 3.28. This is advantageous, since it allows the shrinking of the space between adjacent turns in the inductor beyond that achievable by printing, resulting in a boost in inductance, or equivalently, a boost in Q for a given final inductance. Line height increases linearly with plating time until a point where the plating solution becomes unstable, which happens after approximately two hours (Figure 3.29). Bath

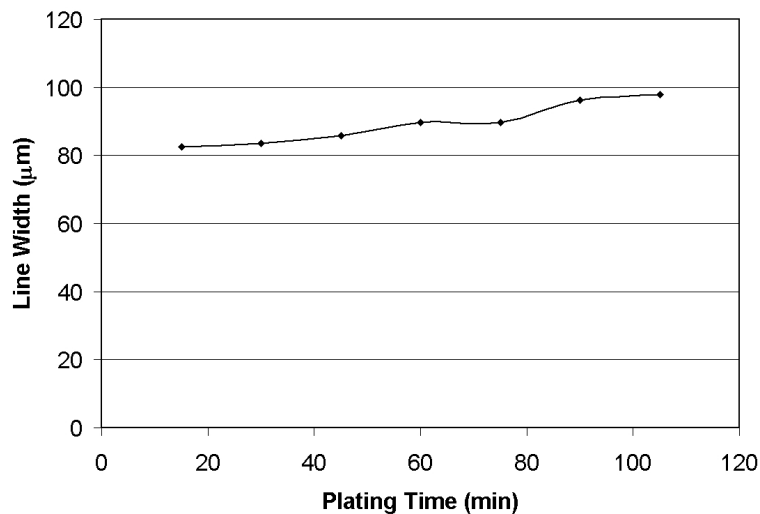


Figure 3.28. Variation in line width versus plating time.

stability is always a concern in electroless systems, but generally most commercial applications have found ways of adequately stabilizing the baths. Proper aeration can extend bath lifetime to 8-12 hours (129), thus allowing the bath to be reused for multiple runs.

Substantially faster plating is possible with appropriately altered plating solutions (138); however, control becomes substantially more complicated, and therefore, this was not pursued herein. As Figure 3.29 shows, copper lines $3.5\ \mu\text{m}$ thick are reliably deposited. At low frequencies the series resistance determines inductor quality, and therefore sheet resistance of the metal layer is an important metric. Sheet resistances as low as $7.5\ \text{m}\Omega/\square$ were obtained (Figure 3.30).

Conductivity of the deposited copper was found to be as high as 73 percent of bulk copper (Figure 3.31). Due to the “coffee ring” pattern commonly seen in inkjetted nanoparticles, more material is deposited at the edges of the lines (86). The higher concentration of nanoparticles causes the reaction to initiate near the edges of the lines first. Therefore the lines are slightly thicker near the edges (Figure 3.32). In-

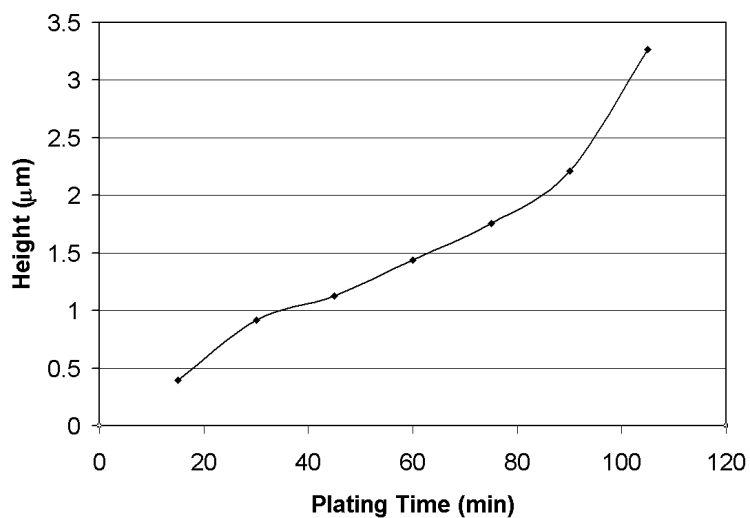


Figure 3.29. Line height versus plating time. There is a linear increase in line height until approximately two hour when the bath becomes unstable. Better aeration can prolong bath life..

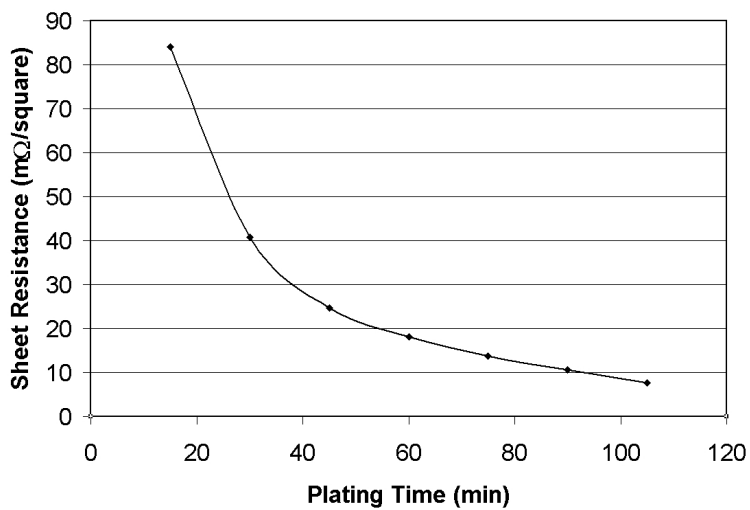


Figure 3.30. Sheet resistance falls off as expected with plating time. 7.5 mΩ/□ is achievable.

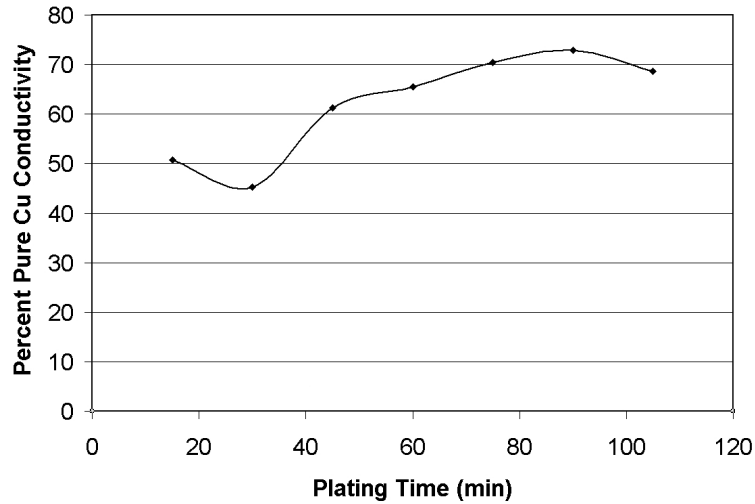


Figure 3.31. Copper quality is excellent until the bath becomes unstable. 73 percent of bulk conductivity is achievable.

terestingly, this process gives cross-sections that are very similar to lines fabricated from printed nanoparticles alone.

3.7.10 High-Quality Inductors

A $3.2 \mu\text{H}$ inductor was fabricated (Figure 3.33) that had a series resistance of 12.4Ω , with a quality factor of 21.3 at 13.56 MHz. For this inductor a line width of $260 \mu\text{m}$ was achieved by printing each trace with three parallel passes. The algorithm for generating this inductor is included in Appendix A. Inductors with arbitrary line width (obviously greater than a drop diameter) are achievable using this method.

Thus, the Q realized using this process is suitable for use in inductively-coupled RFID applications based on the arguments presented in Section 3.3.4. Better aeration would prolong bath life and allow the copper lines to grow thicker. The skin depth of copper is approximately $17 \mu\text{m}$ at 13.56 MHz, so additional copper thickness would benefit the inductor quality. There are also various other plating solutions that give

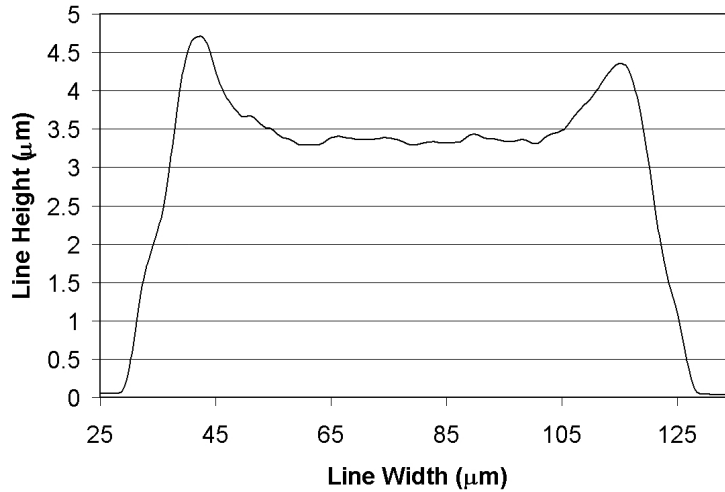


Figure 3.32. Cross section of a line plated for 105 minutes. Peaks at the edges are a result of the plating reaction starting sooner, due to a higher concentration of nanoparticles on the substrate.

higher rates, but without automatic process controls they are hard to stabilize, and were not explored here. Most production electroless baths are all microprocessor controlled, giving extremely good control over reagent concentrations, pH, byproduct concentrations, and temperature.

3.8 Conclusion

Passive components are necessary for power coupling (and data communication) between an RFID reader and tag. An analysis of the coupling inductor quality requirements has been given, and inductors with quality factors above 20 were found to be sufficient for a wide range of tag power consumption.

A low-cost method of fabricating passive devices on plastic substrates has been developed. Inkjet printing has been shown to be a useful and inexpensive tool to fabricate devices on flexible plastic substrates. The gold nanocrystal process has been extensively characterized, and gives consistent results. Polyimide has been shown to

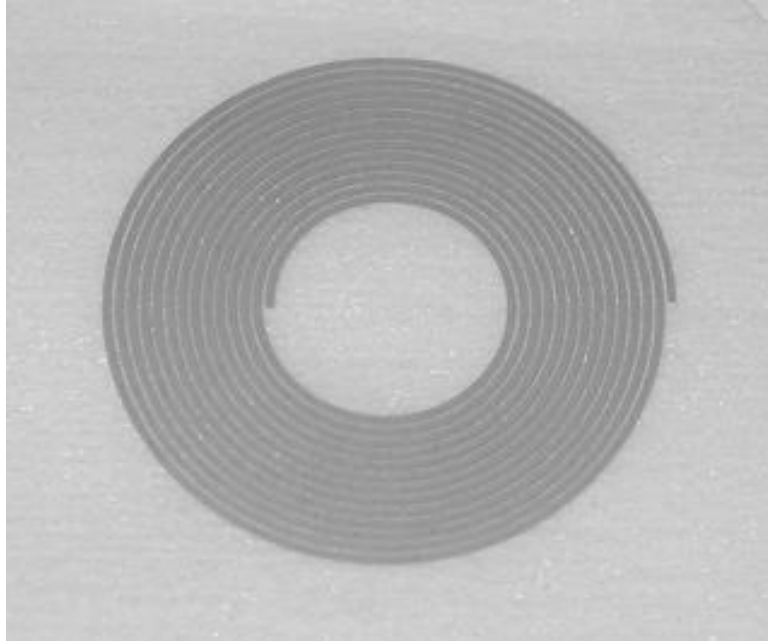


Figure 3.33. $3.2\ \mu\text{H}$ inductor fabricated on plastic with a Q of 21.3 at 13.56 MHz.

be an effective dielectric for isolation, and its dielectric constant does not change significantly at the frequencies of interest, making it suitable as a capacitor dielectric.

Due to the relatively low quality factor of inductors fabricated with printing alone, a novel high- Q printed inductor technology based on nanoparticle-initiated electroless copper plating has been developed, which is suitable for the fabrication of inductors on plastic substrates. Quality factors above 20 are achieved, making this process suitable for use in an RFID front-end without significant loss of tag range.

This is also the first demonstration of the advantages of solution processing techniques. One of the major disadvantages of inkjet printing is that the printed material must have both good electrical and printing properties. Unfortunately not very many materials (especially semiconductors) have this characteristic. In fact, some of the best performing organic semiconductors, such as pentacene, are completely insoluble and must be deposited in a precursor form. As a result the mobility of printed

pentacene is an order of magnitude worse than evaporated systems (88). What this process has demonstrated is the ability to decouple the two requirements, and print a material which does not have good electrical characteristics, but acts as a seed layer for a material that does. The ability to grow materials selectively allows for an all-additive process, greatly reducing the cost of materials, processing, and waste disposal. This represents a paradigm shift in the printed electronics field, and the possibilities are vast.

Chapter 4

Solution-Processing – An Introduction

4.1 Introduction

The deposition of materials from aqueous solutions has been the subject of intense research over the past two decades. While vapor deposition techniques (such as CVD) have become the standard in most production-level processes, the interest in aqueous deposition persists because of the potential for extremely low-cost fabrication. While the earliest reports of solution-deposited PbS date back to at least 1884 (28), a majority of the work was begun in the 1980's with the goal of creating ultra-low-cost solar cells.

The cost advantages to aqueous deposition arise not necessarily from decreased cost of materials, but from simplified processing. Unlike vapor deposition techniques, vacuum is not necessary, nor is an inert atmosphere. Depositions can be carried out

in air, at low temperature, and with increased throughput. The equipment necessary to carry out the deposition is therefore also less expensive. Cost, however, is not the only advantage to using an aqueous deposition. The deposition process is not line-of-sight, like many physical deposition methods (sputtering or evaporation). There are no sensitive organometallic precursors and no toxic or pyrophoric gases, therefore easing the task of waste disposal. Another potentially significant advantage is the compatibility of aqueous deposition with plastic substrates. Plastics are able to withstand the acidic and basic conditions of aqueous deposition quite well, but would not be able to handle exposure to plasma, for instance.

There are some disadvantages to using aqueous deposition methods. First, the substrate temperature is fixed to the bath temperature, which is always less than 100 °C. While this may not seem like a major disadvantage, substrate temperature during growth is often adjusted to control the properties of deposited films. Temperature affects the nucleation and growth rate of films, and as a general rule crystallinity is increased with higher temperatures and slower growth rates (104). With an aqueous deposition not only is the range of temperatures fairly small (30-100 °C) but there are other constraints on the temperature, such as solubility of reagents. Therefore, designing an optimal process is often difficult. Most solution deposited films are either amorphous or polycrystalline with grain sizes in the tens of nanometers.

The remaining sections of this chapter discuss the major concepts of aqueous deposition. Section 4.2 explores the wide range of materials available via aqueous deposition routes. Sections 4.3-4.5 describe the three main deposition techniques, namely chemical bath deposition (CBD), successive ion layer adsorption and reaction (SILAR), and liquid phase deposition (LPD). One of the potential advantages of aqueous deposition is the ability to selectively deposit material, and these techniques are described in Section 4.6. Section 4.7 covers the details of CBD zinc oxide depo-

sition. Finally, the chapter will conclude with a description of the ZnO deposition technique developed and used exclusively in this work in Section 4.8.

4.2 Materials Available

Due to the focus on solar applications much of the literature is related to the deposition of metal chalcogenides, specifically sulfides, selenides, and tellurides. While it is not the goal of this thesis to describe each synthesis in detail, there are several review articles that provide the necessary background (74; 42; 90; 123). Cadmium is used frequently because of the favorable properties of its associated semiconductor compounds, however, cadmium is an extremely toxic material (as are selenium and tellurium) and efforts have been made to create synthesis for non-toxic alternatives such as Ag_2S (21; 43), Cu_2O (34), Cu_2S (109; 20), and CuInS_2 (106; 110), among others.

Solar absorbers have not been the only proposed application. Transparent semiconducting oxides have been developed for use as anti-reflective coatings in solar cells and as electrodes in display applications. Among the most widely studied are ZnO and (ZnS) (13), and there has been some work on ternary compounds such as $\text{Zn}_x(\text{O,S})_y$ (75). The synthesis of ZnO is discussed in detail later in the chapter. Synthesis for insulators have also been published, including not only the ubiquitous SiO_2 (49), but also high- κ dielectrics such as TiO_2 (16; 67), SrTiO_3 (39), and ZrO_2 (143).

Thus, there are wide variety of materials available via aqueous deposition, spanning the entire insulator to semiconductor to conductor continuum. An intriguing possibility, then, is the fabrication of a device using purely aqueous deposition methods. Such a process would represent the “holy grail” of low-cost fabrication. However, in order to create such a device two remaining issues need to be addressed. The first

is selectivity of the deposition, discussed later, and the second is the ability to add dopant to the material for ohmic contacts to a semiconductor, or simply to create a conducting layer. A major advantage of aqueous methods is the simplicity of doping. It has been shown that adding the desired dopant to the deposition solution can result in predictable quantities of dopant in the deposited film. This was shown in the case of zinc oxide doped with aluminum (117), and for zinc oxide doped with nickel, copper, or cadmium (57). Hence, all the pieces necessary to create an all solution-processed transistor exist, but the engineering challenge of integrating them remains.

4.3 Chemical Bath Deposition

CBD is the simplest of the aqueous deposition methods. Reagents are mixed together and heated to the desired deposition temperature. Often reagents are heated to the desired temperature before mixing, because the reaction will start before the mixture is fully heated and consume reagents. This causes some amount of uncertainty in the concentration of reagents unless the heating is at a constant rate and the substrates are immersed at some fixed time. Hence, in a production environment where throughput is a concern reagents should be heated before mixing. After the bath has been prepared the substrates are immersed into solution and deposition occurs via a controlled precipitation reaction.

4.3.1 Deposition Setup

The deposition setup has not changed much since the original description of a CdS CBD process by Pavaskar *et al.* nearly 20 years ago (115). The setup, shown in Figure 4.1, consists of an oil bath, thermometer, stirring apparatus, heater, and reac-

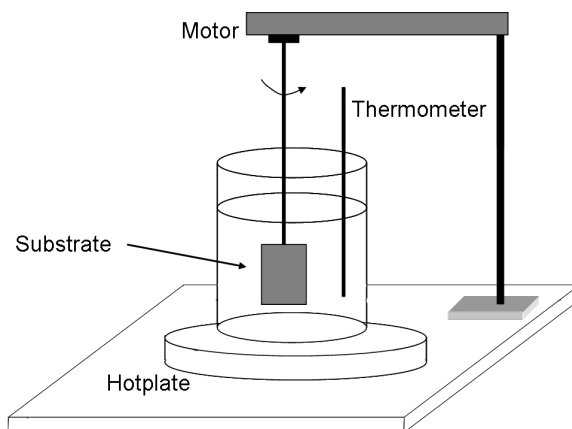


Figure 4.1. CBD deposition apparatus described by Pavaskar *et al.*

tion vessel. The only difference today is the level of automation. The thermometer, heater, and stirring apparatus have been integrated into an automatic temperature controlled stirrer-hotplate, allowing computer control of the process.

4.3.2 Growth Mechanisms

Typically there are two competing growth mechanisms present in the bath. The first occurs at the solid-solution interface and is called the heterogeneous mechanism. Film growth progresses via an ion-by-ion method where a complexed metal is first adsorbed onto the surface and then reacts to form the desired product. In contrast, the homogeneous mechanism involves precipitation in solution followed by adsorption of the colloidal particles. Heterogeneous deposition produces dense, adherent, and mirror-like films, while homogeneous deposition produces thick, rough, and extremely porous films. Homogeneous deposition also consumes reagents much more quickly, and hence, reaction conditions are not constant during the deposition. Although a purely heterogeneous mechanism is desirable, it is difficult to achieve and there will

usually be some degree of homogeneous precipitation. Generally the homogeneous precipitation becomes more pronounced as the bath ages.

4.3.3 Common Bath Components

Bath chemistry consists of a metal ion source typically chosen for high solubility in water (for instance, nitrates, sulfates, acetates, and halides), a complexing agent, and a source for the chalcogenide. Oxygen is typically provided by the hydroxide ion in basic solution. Thiourea ($\text{S}=\text{C}(\text{NH}_2)_2$) is a very common sulfur source because it easily hydrolyzed via one of the following two reactions:



In addition to thiourea, other sulfur sources are thiosulfate ($\text{S}_2\text{O}_3^{2-}$) and thioacetamide (CH_3CSNH_2).

Complexing agents are used to control the release of metal to solution, and prevent the formation of insoluble metal hydroxides. Common complexing agents are ammonia (NH_3), ethylenediamine ($\text{H}_2\text{N}(\text{CH}_2)_2\text{NH}_2$), and ethylenediaminetetraacetic acid (EDTA) (Figure 4.2). Ammonia is commonly used because ammonium hydroxide (aqueous ammonia) can be used to adjust the bath pH in addition to complexing the metal. EDTA will form a complex with most metals, especially with the transition metals. It is so good, in fact, that it is used to treat cases of lead poisoning. EDTA is fairly unique among complexing agents because of its ability to complex in a one-to-one ratio with metal ions. From the structure shown in Figure 4.2, EDTA has four acidic protons in addition to two sets of unpaired electrons on the nitrogen

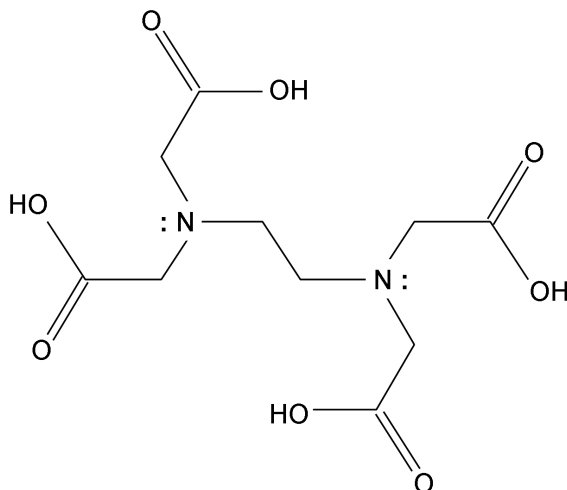
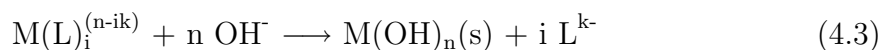
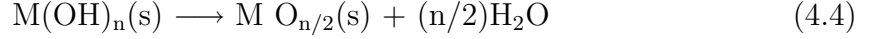


Figure 4.2. Structure of the complexing agent EDTA.

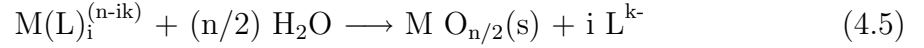
atoms. EDTA is used in basic solutions where all four carboxylic groups have been deprotonated leaving EDTA^{4-} . Typically all six electron pairs are used to bind to the metal ion, although sometimes only five with one of the carboxylic groups still protonated.

The reaction proceeds in several steps. First, the metal-ligand complex is formed. In the case of EDTA this must take place under basic conditions in order to deprotonate its carboxylic acid groups, and with ammonia the solution will already be basic due to the addition of NH_4OH . The second step is the adsorption of the metal-ligand complex on the substrate. After adsorption the ligand dissociates and hydrolysis of the chalcogenide source results in film growth. These very general steps are present in all forms of CBD, and can be described for oxide systems by the following reactions (97). For a metal cation M^{n+} complexed by i ligands L^{k-} :





for the overall reaction:

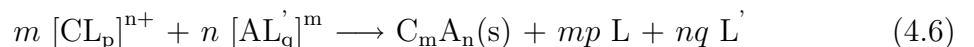


The conversion of metal hydroxide to metal oxide sometimes occurs during the deposition, but often requires a post-deposition anneal above 150 °C.

4.4 Successive Ion Layer Adsorption and Reaction

The development of SILAR was motivated by the desire to eliminate the problem of homogeneous precipitation in solution. As mentioned previously, the homogeneous precipitation decreases bath lifetime by consuming reagents and tends to produce rough porous films. SILAR addresses this problem by keeping the solutions of complexed metal ions and chalcogenide separate. Thus, in theory, there will be no opportunity for the homogeneous reaction to occur. The process, depicted in Figure 4.3, involves alternately dipping the substrate into a solution of metal ions and then the chalcogenide source. Metal ions are adsorbed onto the surface in the first solution, then a water rinse is used to remove excess solution, and the reaction proceeds only on the substrate when it's placed in the second bath. The sequence is repeated until the desired thickness is achieved.

The reaction of adsorbed cations, $[CL_p]^{n+}$, and anions, $[AL_q]^{m-}$, can be described by the following reaction (96):



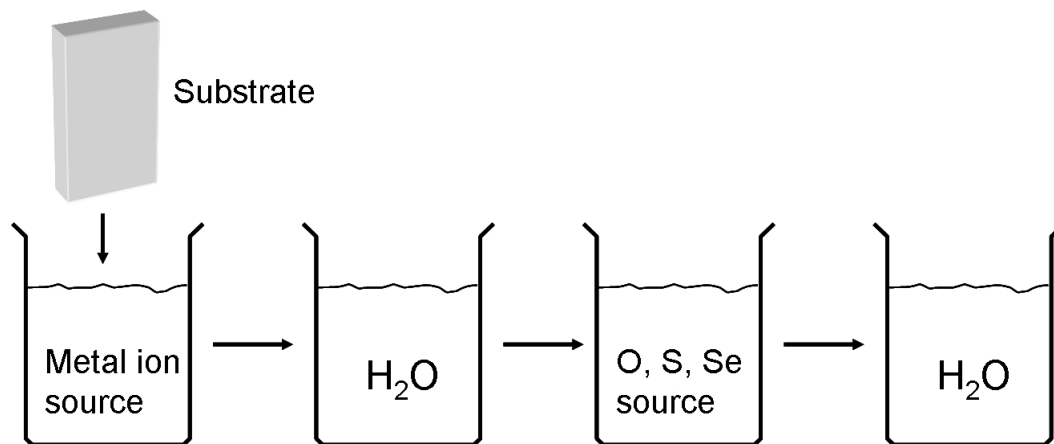


Figure 4.3. Description of the SILAR process flow.

The metal ligands are chosen, again, for their solubility in water. Complexing agents are not needed in SILAR because the metal ions in solution are not exposed to basic conditions and therefore will not precipitate. There are a few exceptions, however, where CN^- (120) or ammonia are used (58). For sulfide systems the sulfur source is either Na_2S , or a solution of H_2S and NaOH . The oxygen for oxide systems is again provided either by hydroxide ions.

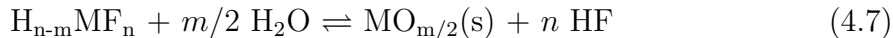
Unlike CBD, SILAR is not well suited for large-area applications. Repeatedly moving large substrates is a mechanical challenge, and can result in breakage even when care is taken. Uniformity is a concern with SILAR because different areas on the substrate are exposed to the solutions for differing amounts of time, due to the finite time required to immerse and withdraw the substrate. The repeated exposure to air between immersions also increases the risk of contamination. Perhaps the largest drawback to SILAR processes is that in practice, even though solutions are kept separate and substrates rinsed between immersions, there is a finite amount of homogeneous precipitation in the chalcogenide bath due to desorption of the metal ions. Thus, SILAR is not seen as a replacement for CBD, since the homogeneous precipitation cannot be fully prevented.

Throughput can be a concern because of the many repetitions required to deposit substantial thickness. The thickness per cycle varies based on the specific process and can vary from less than one angstrom (on average) to a few nanometers. In order to speed up the process Nicolau designed and built a computer-controlled deposition apparatus (shown in Figure 4.4) that used a circular arrangement of beakers and a rotating spindle that would hold several substrates at a time (96). However, the process was still extremely slow, and they reported that a deposition of 2500 Å required six days. More recent reactions deposit roughly 0.5-1 nm per cycle, which would still require 250-500 cycles to deposit 2500 Å, but at least it could be done in less than one day.

4.5 Liquid Phase Deposition

Liquid Phase Deposition is really a subset of CBD, but the chemistry is sufficiently different that it is generally considered a separate technique. LPD was originally developed for the deposition of SiO₂ by Nagayama *et al.* (89), but has since been expanded to other oxide dielectrics as well. Processes exist for Ni₂O₃ (116), TiO₂ (16), Fe₂O₃ (18), Vn₂O₃ (17), SnO₂ (135), and the high- κ dielectric ZrO₂ (143).

LPD is characterized by the controlled hydrolysis of a metal-fluoro complex by addition of water, boric acid (H₃BO₃), or aluminum metal. The following reaction describes the overall process (97):



Addition of water will drive the reaction towards the products by Le Châtlier's principle. The addition of boric acid (89) or aluminum (46) scavenges fluorine, effec-

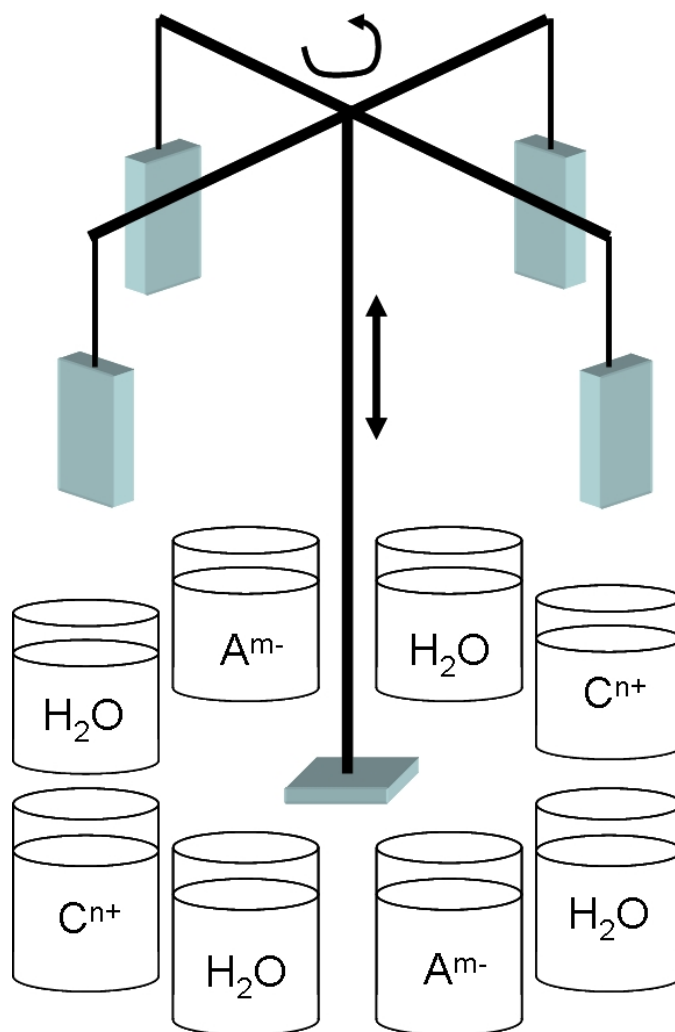
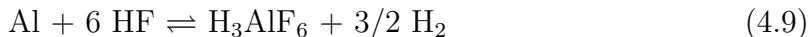


Figure 4.4. Nicolau's apparatus designed to automate SILAR.

tively decreasing the concentration of products and again drives the reaction towards the products by Le Châtlier's principle. The relevant reactions are shown below:



LPD deposition is preferential to surfaces with high -OH content. This includes native SiO_2 , alumina, stainless steel, copper oxide, quartz, and glass, among others. The deposition does not easily occur on hydrophobic surfaces such as photoresist, although some plastics will work after exposure to oxygen plasma (49).

While fluorine chemistry is common in microfabrication processes, the associated hazards involved may not make this technique applicable to low-cost fabrication processes. It may be useful, however, if an oxide needs to be deposited onto another layer which will not survive the basic conditions of CBD or SILAR.

4.6 Selective Deposition

There are two methods to make aqueous depositions selective. The first is simple and involves changing the surface properties of the substrate to make areas of hydrophilic and hydrophobic areas. The second involves depositing self-assembled monolayers (SAMs) to define regions for deposition to occur.

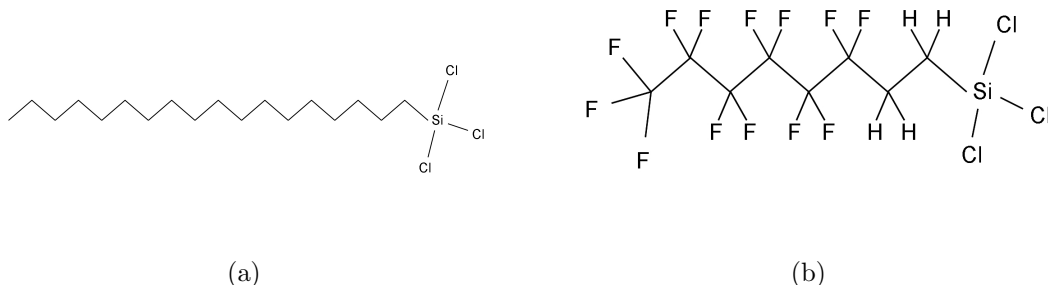


Figure 4.5. (a) OTS molecule used for hydrophobic surface modification. (b) FOTS.

4.6.1 Exploiting Hydrophilic/Hydrophobic Surfaces

Selectivity can be achieved by creating areas where adsorption of the metal-ligand complex is unfavorable, achieved by creating hydrophobic areas on the substrate. This can be done by either spinning and patterning photoresist (48) or by depositing a monolayer of material which results in a high contact angle.

Organosilane molecules are used when working with silicon or silicon-dioxide because of their good adhesion and ordering on the surface. In this work it was found that octadecyltrichlorosilane (OTS), shown in Figure 4.5(a), and tridecafluoro-1,1,2,2-tetrahydrooctyltrichlorosilane (FOTS), shown in Figure 4.5(b), were capable of producing a sufficiently hydrophobic surface on SiO_2 surfaces, enabling selective deposition of ZnO. Organosilane molecules are not removed in acidic or basic conditions, making them ideal for application with aqueous deposition techniques. They can be patterned by exposure to ultra-violet light (a technique used later) or removed entirely by oxygen plasma.

This method was employed by Hwang *et al.*, for the selective deposition of CdS onto silicon wafers (54). The OTS was patterned by microcontact printing, demonstrating the compatibility of this method with printing and CBD processes.

4.6.2 Selectivity via Self-Assembled Monolayers

The techniques of Section 4.6.1 can be expanded to not only inhibit growth, but to change the surface properties to promote film growth. This is done by the deposition of a self-assembled monolayer (SAM). Instead of depositing a molecule like OTS (Figure 4.5(a)) which terminates in an alkane chain, other terminating groups can be chosen to promote film growth. The SAM can be designed in such a way that one end will bond to the substrate, and the molecule will orient vertically to expose the other end, therefore creating a new surface with different properties than the original substrate. Table 4.1 shows the functional groups that have been used to grow oxide and sulfide films from aqueous solutions.

Using a combination of directing and inhibiting monolayers selective deposition using CBD is achievable. This is a very exciting possibility. The ideal low-cost manufacturing process would be to start with a glass substrate patterned using microcontact or inkjet printing and then use a combination of CBD and SAM layers to create a multi-level electronic structure, such as a thin-film transistor or diode. All the cost saving arguments presented earlier apply, but now the structure is not limited by the ability to print active material. As with the electroless copper plating process, we have decoupled the deposition of electronic materials from the lithographic steps. While a fully integrated CBD/SAM TFT process is still the subject of future work, it is the hope that performance will be substantially higher than that achievable with organic semiconducting materials.

4.7 Chemical Bath Deposition of ZnO

Zinc oxide is a transparent semiconductor that has many applications in displays, discussed in Chapter 5. While much of the CBD literature has been devoted to the

Table 4.1. SAMs used for aqueous deposition of oxides and sulfides

Material	Functional Group	Substrate	Reference
ZrO ₂	-SO ₃ H	SiO ₂ /Si	(98)
ZrO ₂	-SO ₃ H	SiO ₂ /Si	(4)
SnO ₂	-SO ₃ H	SiO ₂ /Si	(131)
TiO ₂	phenyl	SiO ₂ /Si	(61)
ZnO	-SO ₃ H	SiO ₂ /Si	(14)
ZnO	-NH ₂	SiO ₂ /Si	(62)
ZnS	-COOH	Au	(37)
PbS	-COOH	Au	(82)

deposition of sulfides, there have been several techniques developed for the deposition of zinc oxide. It is the goal of this section to describe the various bath chemistries, and the factors governing the deposition of ZnO.

4.7.1 Background

Zinc oxide CBD processes do not always produce ZnO directly. The insoluble species of zinc in aqueous medium is Zn(OH)₂, which is insoluble in the pH range of $7.5 < \text{pH} < 13.7$ for a Zn²⁺ concentration of approximately 10⁻² M (23). As mentioned previously, these reactions are typically run in basic solutions so complexing agents are necessary to prevent homogeneous precipitation. It is common for CBD processes to produce a mixture of ZnO and Zn(OH)₂. A post-deposition anneal will then convert the Zn(OH)₂ to ZnO by the following mechanism:

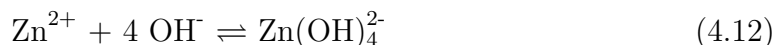
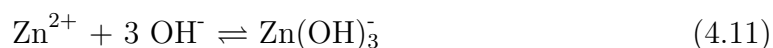


This conversion is known to occur at 200 °C (99), but has been reported at temperatures as low as 120 °C (29). However, one of the reasons a mixture is produced is that this conversion can also occur in aqueous solutions above 50 °C (112). Therefore,

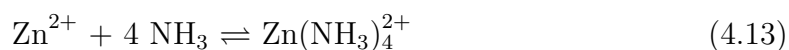
this conversion can occur during the deposition, even when Zn(OH)_2 is the deposited species.

4.7.2 Soluble Zinc Species in Basic Solutions

Zn(OH)_2 is not very soluble in basic solutions, with a solubility product of approximately 10^{-16} . However, zinc may appear to be more soluble than its solubility constant would imply because of the existence of two soluble zinc-hydroxide complexes:



The situation is made more complex by the addition of the complexing agent itself, such as ammonia, which adds another species to the bath:



This last complex is, of course, the one that was intended and is present in the highest concentration. At pH above approximately 11.4 another species, ZnO_2^{2-} , can be present in solution as well. Figure 4.6 shows the relationship between ammonia concentration, pH, and which species of zinc will be present in solution. The shaded box indicates the region where most CBD processes are run.

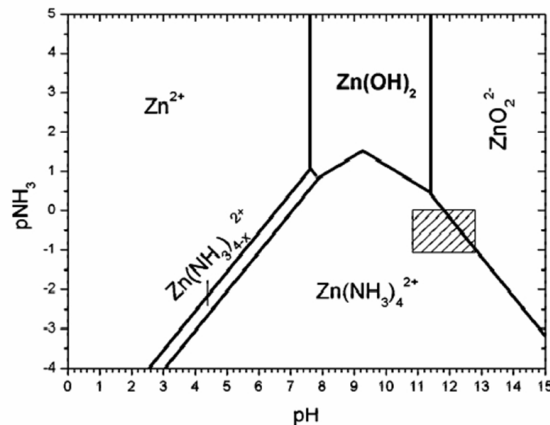
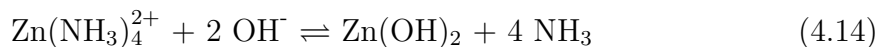


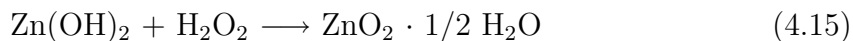
Figure 4.6. Zinc species in solution based on pH and ammonia concentration, from (11).

4.7.3 Precipitation of Zinc Species

The precipitation of Zn(OH)_2 follows the straightforward hydrolysis of the tetraamino complex:



Several studies have investigated the influence of hydrogen peroxide on the deposition of ZnO. Usually hydrogen peroxide is used as the oxygen source in electrochemical depositions, where it is reduced to give the products ZnO and H_2O (114; 113). However, it has also been used in SILAR (73) and CBD (105) reactions. Addition of hydrogen peroxide to the reaction causes conversion of Zn(OH)_2 to ZnO_2 by the reaction (79):



Conversion of ZnO_2 to ZnO occurs at temperatures of approximately 180 °C when annealed at atmospheric pressure, but can be reduced to 150 °C under reduced

pressure (1 kPa) (80). ZnO₂ is the primary material deposited from baths containing zinc, ammonia, and hydrogen peroxide (105).

4.8 Deposition of ZnO for use as a Transparent Semiconductor

The deposition in this work uses ammonia as the complexing agent and includes hydrogen peroxide. All chemicals were obtained from Sigma Aldrich, and no purification was needed. The zinc source was 99.995% anhydrous ZnCl₂, mixed into a 0.08 M solution using ultra-filtered deionized water (DIUF). The anhydrous powder was used simply because it was the highest purity available. The choice of counter ion is not critical. The reaction was found to work with zinc nitrate, acetate, and bromide. Stock solutions of approximately 1.9 M NH₄OH were mixed from 28% aqueous ammonia and DIUF. Ammonia is a weak base, and always obeys the following equilibrium:



Since ammonia is a gas, it tends to leave solution over time, and the equilibrium is constantly being shifted to the left. A consequence of this is a gradual decrease in pH as stock solutions age. Therefore when reagents are mixed together the pH is set manually by the addition of concentrated (28%) aqueous ammonia.

The deposition bath is mixed in a glass beaker using 15 mL of 0.08 M ZnCl₂ and 62 mL of 1.9 M NH₄OH, and is stirred at 60 rpm using a Teflon magnetic stir bar. At this point the pH is set to the appropriate value, which ranged from 11.0-11.6 in this study. The baths are covered and allowed to warm to the deposition temperature

(50-70 °C) for 90 minutes. At this point the baths are still clear and visibly free of precipitation. 2 mL of H_2O_2 are then added, followed by the SiO_2 substrates two minutes later.

The deposition itself is a two-step process. Under the deposition conditions described above no deposition will occur onto the SiO_2 substrate. Therefore a seeding step is used to force a seed layer to precipitate onto the surface. This is achieved by pulling the substrates out of solution for 5-10 seconds and then reimmersing the substrates. While the substrates are out of solution they cool just enough to cause nucleation on the surface. Once seeded the reaction proceeds normally. Since this particular bath chemistry does not deposit without seeding, the bath is also fairly immune to the problem of homogeneous precipitation, and in fact the bath lifetime is several hours before any homogeneous precipitation is noticeable.

Growth time is temperature dependent, but films approximately 12nm thick are grown in 6, 30, and 150 seconds at 70, 60, and 50 °C respectively. The process is very well controlled, and the deposition times are precisely what you would predict from the Arrhenius Equation. The electrical properties of the deposited thin films is the subject of Section 5.6.

4.9 Commercial Applications of CBD

Of the three methods, only CBD has found commercial application thus far. Siemens Solar (now Shell Solar) used CBD to create the CdS layer for their *Apollo* (CdTe/CdS) solar cells (136), and their ST-Module CuInSe_2 (CIS) cells (59). These modules are formed on 1x4 foot soda-lime glass substrates, demonstrating that CBD is well suited for large-area low-cost applications in a production environment. Through optimizations of the manufacturing process Shell Solar is able to

produce modules with yearly capacity exceeding 1 MWp, with a goal of eventually 10 MWp (140; 141). Recently, Shell has reported that their new pilot process for Cu(In,Ga)(S,Se)_2 (CIGSSe) cells on $60 \times 90 \text{ cm}^2$ glass substrates also includes the CBD CdS deposition step (107; 108).

4.10 Conclusion

The three main aqueous deposition techniques have been discussed, along with a discussion of their major advantages and disadvantages. While CBD generally excels in large-area applications, selectivity is achievable by modifying the substrate surface, so it should not be considered only a blanket deposition process. Finally, CBD processes have found application in commercial solar cell fabrication, showing that controlled, reliable depositions are possible. In this work zinc oxide has been used exclusively for the fabrication of thin film transistors and the deposition has been described in detail.

Chapter 5

Zinc Oxide Transparent TFTs for AM-OLED Displays

5.1 Introduction

The computer display market has undergone a dramatic shift in the past few years from traditional CRT monitors to newer liquid-crystal displays (LCDs). In the year 2006 revenue generated by LCD displays is expected to surpass CRTs for the first time. Although LCDs have been around for more than twenty years, it was not until recently that performance on par with CRTs was achievable at an affordable price point. This was achieved mainly through the advancement of amorphous silicon processing.

Traditional LCD computer monitors fall into a general category called flat-panel displays (FPDs). This includes not only color, active-matrix, high-resolution, high-power, and high brightness displays for computing, but also low-power, low-resolution,

passive addressed, reflective, monochrome displays for hand-held devices or other simple applications. Obviously there is a continuum of specifications that falls between these two extremes.

A fairly new type of display based on organic light-emitting diodes (OLEDs) has become the subject of intense research because of its potential advantages over LCDs. It is the goal of this chapter to explain why OLED displays are so compelling, and then show how the application of transparent zinc oxide transistors, rather than amorphous of polysilicon TFTs, can lower both the cost and power consumption of these displays.

5.2 OLED Displays

In contrast to organic TFTs, organic light-emitting diodes have found commercial application in small displays such as Pioneer's in-dash CD player, cell phones, and digital cameras. The manufacturing process is now mature enough that pixel-to-pixel brightness variation has been reduced to acceptable levels, and device lifetime has been increased to 25,000+ hours. Thus, there has been great interest in expanding the use of OLEDs from simple displays to high-resolution desktop monitors.

5.2.1 OLED Device Structure

The structure of a typical bottom-emitting OLED is shown in Figure 5.1. The stacked structure consists of a glass substrate, transparent ITO anode, hole injection layer, hole transport layer, emissive layer, electron transport layer, and finally a low work function metallic cathode. An important feature is the presence of a desiccant in the pixel. Moisture is detrimental to the cathode metal within the OLED

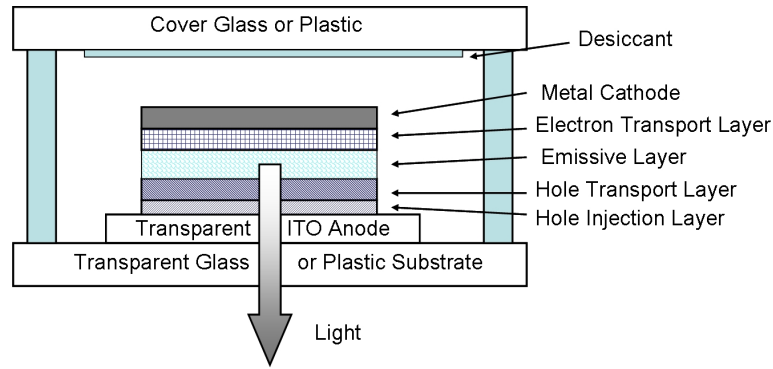


Figure 5.1. Structure of the bottom emitting OLED.

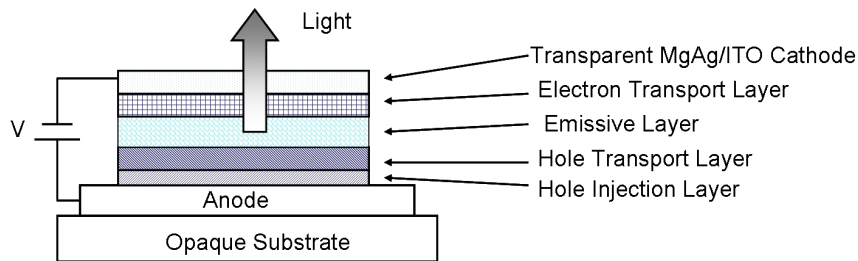


Figure 5.2. Structure of the top emitting OLED.

and will cause dark spots to form. Water is introduced to the system either during encapsulation, or by diffusing in during the device lifetime. Desiccants must be integrated into an automated manufacturing process to enable mass production of OLED displays (40).

An alternate structure called the top emitter architecture is shown in Figure 5.2. In this structure light is emitted through the cathode instead of anode, allowing the use of an opaque substrate. The advantage is that drive TFTs can be placed under the pixel and not degrade the aperture ratio. However, this structure requires a transparent or semi-transparent cathode, and a transparent desiccant. A semi-transparent MgAg/ITO cathode has been demonstrated, but to date a transparent desiccant has not been developed. Due to the obvious benefits of this top emitter structure it remains the focus of intense research.

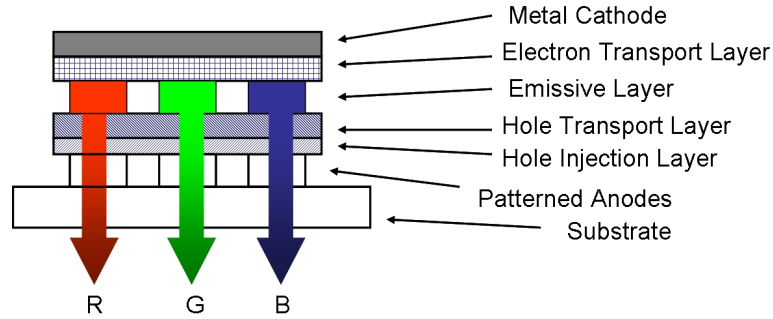


Figure 5.3. Color generated by doping OLED emitting layer.

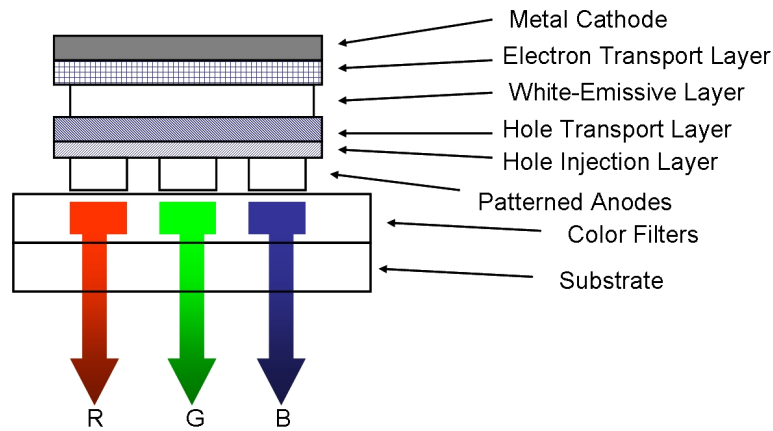


Figure 5.4. Color generated with a white OLED and color filters.

5.2.2 OLED Colors

Color is achieved by dividing the pixel into three subpixels, one for red, green, and blue. The two major methods of generating color are shown in Figures 5.3 and 5.4. In the first method the emitting layer is doped to emit light at the appropriate wavelength. This method gives high efficiency, but the subpixels tend to age differently, resulting in inaccurate color rendering over time. The second method is similar to an LCD, where color filters are used to generate color from a white emitting OLED. This method does not require patterning of the emitting material, but suffers from decreased efficiency due to the absorption of the color filter.

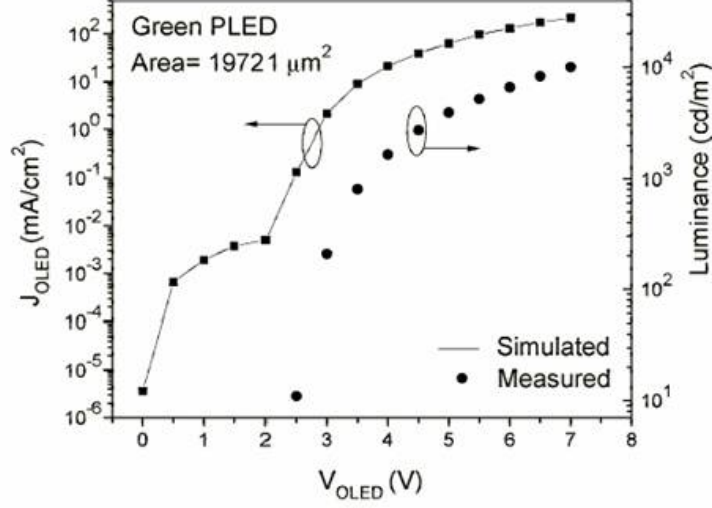


Figure 5.5. Typical OLED current-voltage characteristic, from (72).

5.2.3 OLED Current-Voltage Characteristics

Like many organic devices, OLED IV behavior is dominated by space charge limited conduction (SCLC). In this regime the current density can be modeled by Mott-Gurney law:

$$J = \frac{9}{8} \mu \epsilon \epsilon_0 \frac{V^2}{L^3} \quad (5.1)$$

where J is the current density, ϵ is the relative dielectric constant, ϵ_0 is the permittivity of free space, V is the applied bias, and L is the thickness of the material. For polymer materials used in OLEDs common values are: $J = 10 \text{ mA/cm}^2$, $\epsilon = 3.0$, and $L = 100 \text{ nm}$. Figure 5.5 shows typical OLED behavior with respect to current density, luminance, and drive voltage. For display applications a luminance of 100 cd/m^2 is considered the minimum, and OLEDs therefore require a drive voltage of approximately 3 V. State-of-the-art OLEDs are not much better than average, requiring 2.55 V (9).

Now that the basic principles of OLEDs have been discussed, the next section

describes the major differences between OLED displays and the dominant liquid-crystal display (LCD) technologies.

5.3 OLED Versus LCD - A Technology Comparison

OLED displays are emissive in nature, rather than passive in the case of LCD. LCD displays are only about 10% efficient, meaning 90% of the power consumed by the backlight is lost in the two polarizers and the LC material itself. In addition, the backlight must be on full brightness 100% of the time, even when the screen is black. In an OLED display the brightness is proportional to the current supplied to the OLED, and when the display is dark no power is consumed except for the power required for the pixel switching circuitry, which is similar for OLED and LCD displays. So the potential for lower-power displays exists in theory, but as will be shown, it is entirely dependent on the properties of the drive TFTs.

The existence of polarizers in LCDs causes a few other problems, the most important of which is the limited viewing angle. Since OLED displays do not require polarizers, and the light is emitted from the front surface of the display, OLED-based displays have far better viewing characteristics. The viewing angle is increased to almost a perfect 180 degrees. In addition, they are potentially brighter, and have enhanced contrast.

Finally, elimination of the backlight reduces the bulk of the display, allowing thinner modules, and it also reduces the cost significantly. Since the switching speed of OLED displays is based only on the organic diode's turn off transient, and not the relaxation time of an LC cell, OLED displays are expected to be faster and handle full-

motion video better than LCD. Increased switching speed comes at a price, though. Passive addressing schemes (that require no pixel TFTs) are not practical for displays with more than a few hundred pixels. The eye integrates brightness in time, so if an OLED only emits for $1/\text{resolution}$ of the refresh rate, then it must be *resolution* times brighter, requiring approximately *resolution* times the current density. For even a small display this would require significantly more current, which decreases device lifetime (91; 44; 137; 134).

The only real advantage LCD has over OLED is the ability to make an ultra low-power reflective LCD with no backlight. These displays require ambient light to function, but require less power than any OLED or backlit LCD display. Therefore, it is not these ultra low power applications that OLEDs are most suited for, but rather high performance displays for computing or small low-cost displays with superior viewing properties than LCD.

5.4 OLED Pixel Drive Techniques

OLEDs are current-driven devices, whereas LCDs are voltage-driven. Therefore the pixel driving scheme is significantly different. While LCD pixels can be made with a simple one transistor design, much like a DRAM cell, OLEDs require at least a two transistor design, shown in Figure 5.6. The circuit in Figure 5.6 is not practical, however, because most TFTs suffer from device degradation including threshold shift and decreased drive current as the devices age. This causes brightness non-uniformity across the display, and decreased performance (i.e. brightness) over time.

The solution lies with the fact that OLED brightness is proportional to device current. If the diodes could be programmed with a current, rather than voltage, then brightness would be uniform and constant with time. This is achieved with the four

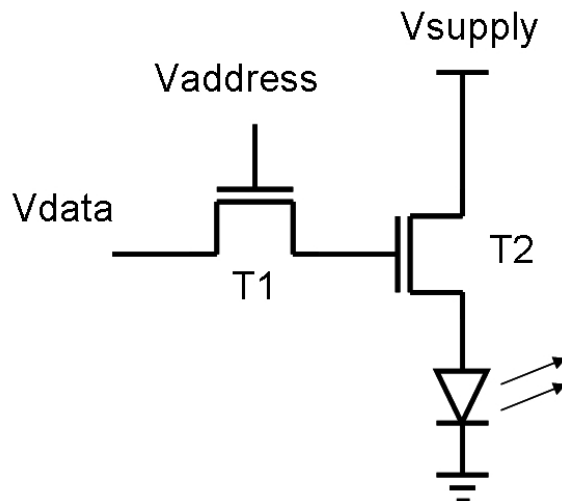


Figure 5.6. Two transistor pixel design.

transistor circuit shown in Figure 5.7. The pixel is addressed by enabling the column line and sending the programming current over the row line. Initially, assuming the pixel is off, the programming current will flow onto the gate of T3 until T3 turns on. Then the programming current will be split between the gate of T3 and the drain of T3, until a steady-state is reached where no further current flows onto the gate of T3, and all the programming current is flowing through the drain of T3. Thus, no matter what the mobility or threshold voltage of T3, the gate bias will be set to the correct value. Then a current mirror is utilized via T3 and T4 to drive the OLED with a current proportional to the programming current. In this manner only T4 needs to be large. All other transistors can be small. The programming current is merely a fraction of the OLED drive current, therefore reducing power consumption (although the gain is small) and pixel programming time.

While the four transistor design has been shown to give superior uniformity across the display, long-term reliability is still unknown. Since transistors T3 and T4 are fabricated near each other it is expected that they will be fairly well matched. However, as with α -Si, it is anticipated that threshold voltages will drift over time. Both

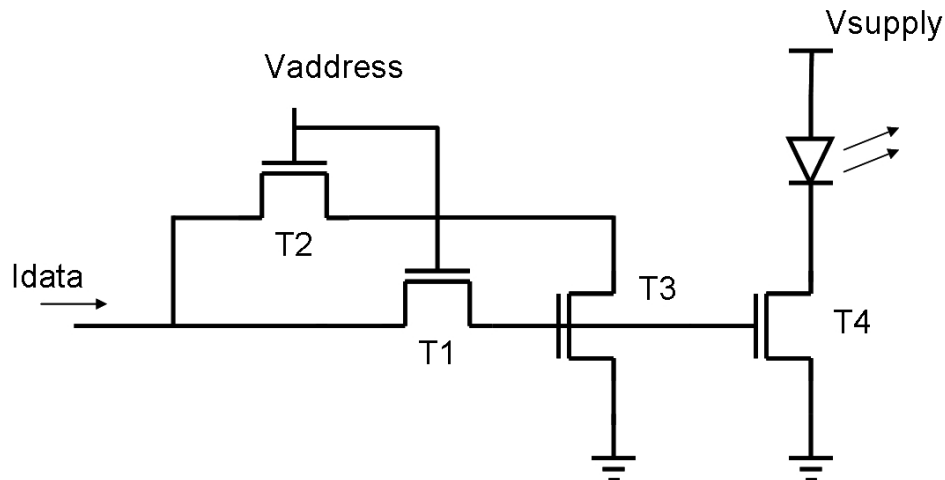


Figure 5.7. Four transistor pixel design.

transistors will be biased with the same gate voltage, but in this configuration the drain bias will be different, potentially causing different aging behavior. To date the long-term performance of this pixel has not been studied in detail.

5.4.1 Pixel TFT Considerations

Currently both amorphous silicon (α -Si) and polysilicon transistors are being pursued for use in pixel drivers. α -Si is appealing because of the maturity of the LCD market. The processing is well understood and inexpensive. Therefore, there have been several attempts to use α -Si TFTs in OLED displays. However, for several reasons described below, α -Si is not suitable for high resolution or low power applications. Polysilicon, with mobilities approximately 100 times higher than α -Si, is more than capable of driving pixel TFTs. It is also capable of driving the display control circuitry, therefore reducing the cost of bonding external components to the display. However, polysilicon processing is quite expensive, requiring either a long high temperature solid-phase recrystallization (increasing substrate costs) or laser re-

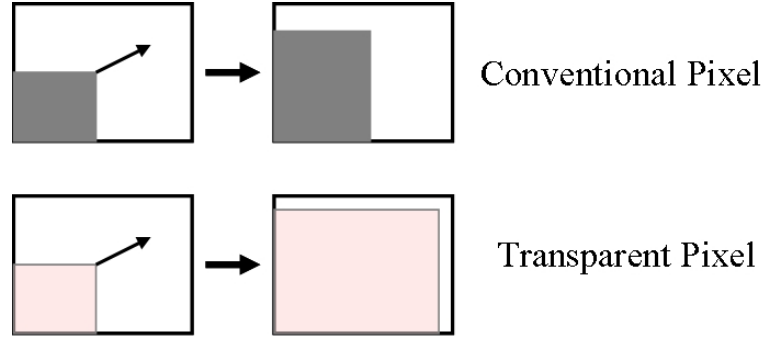


Figure 5.8. As pixel size decreases the area required for pixel TFTs does not scale.

crystallization over extremely large areas which suffers from poor uniformity. Laser recrystallization is currently the method of choice.

5.4.2 Pixel Scaling

As display resolutions increase the pixel aperture ratio, defined as the ratio between total pixel area and emissive area (Figure 5.8), decreases. This occurs because the pixel TFT area does not scale at the same rate as the pixel area. Transistor T4 does scale with pixel area because the OLED drive current scales with area, but transistor area is defined by not only the width-to-length ratio but also the area of the contacts and interconnect, so it is not a linear relationship. Transistors T1-T3 do not scale at all. As a consequence of reduced aperture ratio the OLED brightness must be increased to compensate. This decreases device lifetime and is generally not a viable option.

An alternative solution is to use TFTs based on transparent semiconductors such as zinc oxide. As depicted in Figure 5.8, transparent electronics allow the pixel drive TFTs to occupy the entire pixel area. This reduces the brightness requirements of the OLED, increasing lifetime, and also reduces the performance requirements of the drive TFTs since larger with-to-length ratios are possible.

Another proposed alternative to the pixel scaling problem is to put the pixel drive TFTs behind the OLED. As simple as this solution sounds, it has been difficult to achieve. In this process the OLEDs would first be fabricated on the glass substrate, followed by processing of the TFTs, which would have to be processed on top of the OLEDs. Since OLEDs are fabricated from organic molecules they tend to be sensitive to temperature, vacuum, oxygen, and are attacked by most liquids (organic and otherwise). Thus, fabricating TFTs on top of OLEDs tends to degrade the performance of the OLED significantly.

5.4.3 Power

In order for OLED displays to compete with LCDs, they must not only possess superior viewing qualities, but they must do it while consuming equal or lesser power. Typical LCD panels consume 300 W/m², most of which is consumed by the backlight. For comparison a traditional cathode ray tube (CRT) monitor consumes approximately 500 W/m².

Using α -Si to drive OLEDs requires a supply voltage of 25-30 V depending on the W/L of the drive transistor (122; 65). This translates into a maximum display power density of 2750-3300 W/m², ten times that of an LCD! However, the display will not always be operating at full brightness so the average power will be slightly reduced. The need for high voltage comes in part because of the low mobility of α -Si transistors, and in part because the aperture ratios for even modest resolution displays can be as low as 40%. The situation can be improved by moving from a 25 μ m to a state-of-the-art 5 μ m gate length, which would reduce the supply voltage to 15 V, and the maximum power to 1650 W/m². Needless to say these numbers are far too high for portable laptop applications, and would result in excessive heat generation even if implemented for the desktop market. Many researchers choose to

ignore this fact when arguing that α -Si is suitable for high-resolution OLED displays (66; 93).

Of course, power consumption is the first thing mentioned by researchers working on polysilicon TFT pixels (83). The higher mobility of polysilicon allows for a reduced supply voltage, to a point where the minimum required supply voltage is dominated by the OLED instead of the TFT. Polysilicon transistors typically do not suffer from threshold variation to the extent of α -Si, so the four transistor pixel of Figure 5.7 is not strictly necessary. A simpler two transistor pixel is sufficient. Since a current mirror is not necessary, the drive transistor can be run in the linear operating regime. This fact, combined with the higher mobility of polysilicon, reduces the required V_{ds} to a minimal 0.1 V (128). Thus, the minimum supply voltage is limited to the OLED drive voltage of approximately 3 V, and the maximum display power is approximately the same as LCD. On average though, the OLED display power will be lower than the LCD because it is not always operating at the maximum brightness.

Therefore, polysilicon is an accepted technological solution that meets all the required specifications for an active matrix OLED display. However, the additional cost of polysilicon is currently prohibitive, and thus no high-resolution OLED displays have come to market.

5.5 Transparent TFTs

Transparent electronics provide an alternative that would meet the technological requirements of OLED displays while potentially reducing the cost of processing. Since the drive transistor can occupy almost the entire pixel area the performance requirements are significantly reduced. A simple increase in transistor size, coupled with a mobility that falls between α -Si and polycrystalline silicon, can reduce the

supply voltage to levels such that the display power is on par with an LCD. In this section the performance requirements for transparent TFTs is considered, with respect to the patterning limitations of high-resolution inkjet printing.

5.5.1 Analysis of ZnO CBD TFT Requirements

Consider a pixel of an OLED display of $200 \times 200 \mu\text{m}^2$. The maximum required OLED drive current is $5 \mu\text{A}$, assuming the standard 110 A/m^2 current density. Using state-of-the-art printing heads a gate pattern of $10 \mu\text{m}$ is achievable. If the drive transistor is interdigitated a W/L ratio of 100 could fit within the pixel area. For the sake of argument let us assume this transistor is driven by a 20 V supply, similar to what α -Si requires. Also assuming a threshold voltage of 5 V and an oxide thickness of 50 nm, we can calculate the required mobility of the semiconductor material. The result is only $0.006 \text{ cm}^2/\text{Vs}$. A surprisingly low value! Since the aperture ratio is 100% with transparent TFTs, both the required maximum current and the available W/L ratio scale at approximately the same rate (with area). Thus, the supply voltage should not depend on pixel size the same way it does with α -Si. Therefore, the choice of a $200 \times 200 \mu\text{m}^2$ pixel was arbitrary and the mobility requirements are quite general.

Based on the analysis above, it would seem that almost any semiconductor would fulfill these criteria, so long as it were transparent. However, recall that power is the major concern with OLED displays. Power can be reduced by improving OLED efficiency or by reducing the supply voltage. The primary goal of this work is to enable the reduction in supply voltage through optimization of mobility. Recall again Figure 5.7 where the minimum supply voltage is given by the equation:

$$V_{DD} = V_{OLED,max} + V_{dsat,T4} \quad (5.2)$$

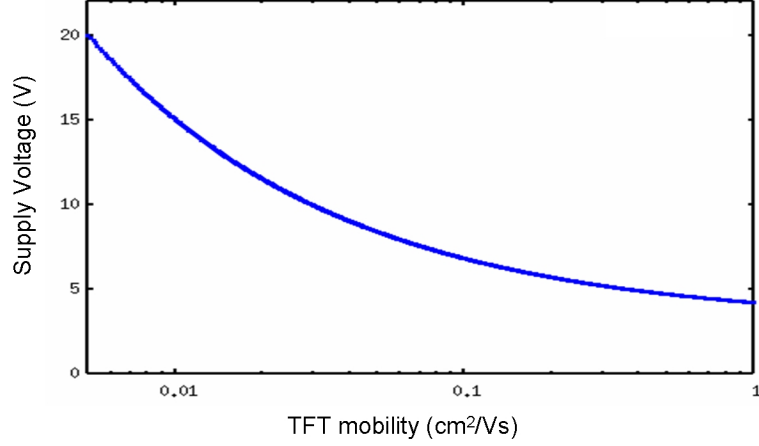


Figure 5.9. Simulated TFT mobility requirements for a given supply voltage.

At the edge of saturation the transistor behavior becomes independent of threshold voltage, giving:

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_{ds}^2 \quad (5.3)$$

Now the required minimum supply voltage can be calculated using the same 50 nm gate oxide, W/L of 100, and a required OLED voltage of 3 V. The results are shown in Figure 5.9. As the plot shows, the supply voltage can be reduced to 4 V if the transistor mobility is 1 cm²/Vs, of which 3 V is due to the OLED. In fact, as the mobility increases from 0.1 to 1 cm²/Vs the supply becomes increasingly dominated by the OLED. Therefore, if the mobility of the transparent semiconductor can be improved to approximately 1 cm²/Vs, then the total display power will be approximately 400 W/m² maximum, and on average should be similar to LCD.

Another requirement of pixel TFTs is the off-current. The pixel must be able to maintain charge for the duration of the frame (approximately a time equal to the reciprocal of the refresh rate). If charge leakage occurs then the pixel will dim and it will appear as flicker to the eye. On/off ratios of 10^6 are generally considered sufficient.

5.5.2 Summary of Transparent TFT Requirements

Transparent TFTs provide an alternative to amorphous and polycrystalline silicon for AM-OLED displays. Since OLEDs, unlike LCDs, are current driven, high current densities are required. In conventional amorphous-silicon-based backplanes, this necessitates the use of high drive voltages, since the opaque α -Si TFTs must be kept small to avoid blocking light. The resulting displays thus have power densities much higher than LCDs. Using a transparent backplane significantly reduces the area restriction of the pixel driver TFTs, allowing a lower supply voltage, since a wide drive transistor may cover a large portion of the pixel without degrading aperture ratio. Simulations show that transistors patterned using inkjet printing (to achieve a gate length of $10\text{ }\mu\text{m}$) would be capable of low-voltage operation as the mobility approaches $1\text{ cm}^2/\text{Vs}$.

In this work we wish to explore the possibility of using CBD zinc oxide TFTs for use in OLED active matrix backplanes. The ultimate goal would be a low-cost display where both the OLED and pixel TFTs were fabricated using a combination of ink-jet patterning and solution deposition techniques.

5.6 Zinc Oxide TFTs Fabricated by Chemical Bath Deposition

Zinc oxide (ZnO) has received attention recently because of its transparency and high mobility, making it attractive for use in transparent thin film transistors (TFTs). The high mobility coupled with the optical transparency of ZnO will enable high-brightness displays fabricated using low-cost solution processing.

5.6.1 Background

In recent years, there have been several reports on ZnO TFTs. Using vacuum-based techniques such as pulsed-laser deposition, ZnO TFTs have been demonstrated on glass. Mobilities of sputtered systems span quite a large range, with many reported between 1-3 cm²/Vs (81; 47). However, more recently careful control of the sputtering process has shown the ability to fabricate transistors with mobilities of 70 cm²/Vs (38). In order to obtain high mobility the substrates must undergo a post-deposition anneal, typically between 600-800 °C.

Analogous to the printing of gold nanoparticles for conductive metallic layers, fabrication of TFTs by printing zinc oxide nanoparticles would be an extremely inexpensive method. The development of encapsulated zinc oxide nanoparticles was pursued by Volkman *et al.* (139). In that report zinc oxide nanoparticles were spun onto a Si/SiO₂ gate stack and annealed in forming gas (5% H₂ in N₂) for several hours at 300-400 °C. The resulting device mobility was 0.3 cm²/Vs, which is on par with the mobility of printed organic TFTs at 0.1 cm²/Vs (87). If material interactions can be eliminated the potential exists for a complementary MOS logic system using printed n-channel zinc oxide and p-channel pentacene TFTs. To date, nobody has attempted this task.

Solution-processed zinc oxide TFTs have been fabricated by spinning a zinc salt solution onto a wafer and then annealing at high temperature in an oxygen ambient (101). This is not a selective deposition, and the resulting mobility was quite low at only 0.2 cm²/Vs. In addition, the counter-ion from the zinc source will end up in the film with unknown consequences.

Here, novel ZnO TFTs are fabricated using a low-cost chemical bath deposition (CBD) process that delivers a dramatic (>10X) boost in performance over nanoparticle systems. The process is compatible with numerous low-cost glass substrates, and

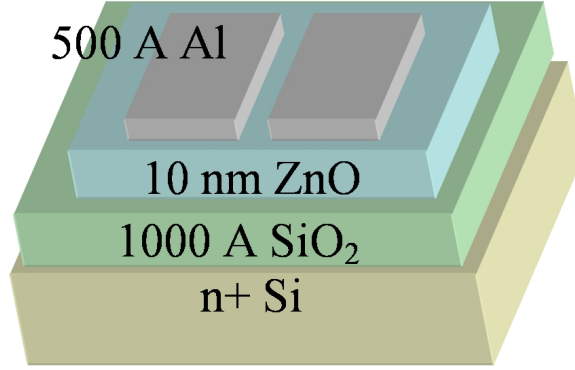


Figure 5.10. Structure of a substrate-gated top-contact ZnO TFT test device.

is also compatible with printing-based fabrication to achieve ultra-low cost. Mobilities as high as $3.5 \text{ cm}^2/\text{Vs}$ are reported. Given the transparent nature of the ZnO, it is possible to use wide transistors covering a substantial fraction of the pixel, and therefore, this mobility is likely sufficient for realization of high-brightness OLED displays with transparent ZnO TFT drivers.

5.6.2 TFT Fabrication

The TFTs fabricated herein used back-gated SiO_2 substrates for convenience. A heavily-doped n+ silicon wafer with 100 nm thermally grown SiO_2 dielectric was used as a substrate for testing purposes, and the device (Figure 5.10) is a typical substrate-gated top-contact TFT. ZnO TFTs typically operate in accumulation mode. Therefore, it is necessary to use thin channel films to avoid excessive leakage currents; CBD is easily able to deliver controllable channel thicknesses in the range of 10 nm.

One of the advantages of CBD processes is that the deposition can be made selective by changing the surface properties of the substrate to exploit hydrophilic / hydrophobic interactions. This may be achieved by patterning hydrophobic regions us-

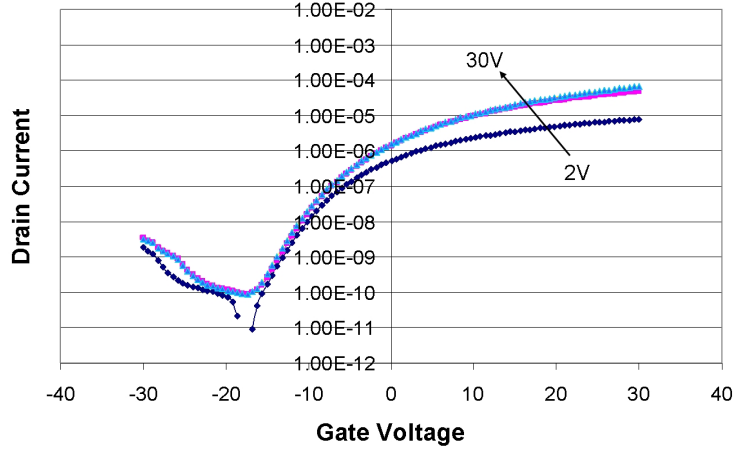


Figure 5.11. ID-VG curve for device annealed at 700 °C.

ing a wide-range of techniques including printing of hydrophobic polymers, patterned deposition of hydrophobic monolayers, etc. Here, a monolayer of fluorooctyltrichlorosilane (FOTS) was deposited by vapor exposure and subsequently patterned with UV ozone to create the active areas on the substrate. During subsequent CBD processing, deposition of ZnO only occurs in areas where the FOTS has been removed. The process results in islands of ZnO on top of the SiO₂ gate dielectric that are approximately 1.5 mm square. If the ZnO layer is not patterned defects through the oxide will allow excessive gate leakage current. Even with patterning of the ZnO this structure is limited to an on/off ratio of approximately 10⁵, for the mobilities achieved here. Some of the best devices (Figure 5.11, for example) have on/off ratios limited by gate leakage, but this was not the case for a majority of the devices presented here.

The CBD zinc oxide deposition step is described in detail in Section 4.8. Deposition bath temperatures ranged from 50-70 °C and had a significant effect on the resulting device mobility. The ZnO layer was grown to approximately 10-12 nm regardless of deposition temperature. After deposition the substrates are annealed in oxygen at 425-700 °C for two hours. Longer anneals were not found to improve mobility or on/off ratio.

50 nm of aluminum is evaporated to form source and drain contacts, followed by a 15 second contact anneal at 300 °C in nitrogen. The length of the contact anneal is critical because aluminum from the contacts can diffuse into the channel. This causes the effective channel length to decrease below the expected value, which will artificially increase the extracted mobility. More importantly, it will significantly degrade the on/off ratio. Aluminum is chosen as the contact metal because of its workfunction match to zinc oxide, but also because it is an n-type dopant. The zinc oxide beneath the evaporated contact is doped n+, creating an excellent contact. As a consequence, if aluminum is allowed to diffuse into the channel it will dope the channel and make it harder to turn the device off. The effect of a longer contact anneal is shown in Figure 5.12. The upper curve was annealed for 15 seconds and the lower for 75 seconds (first 15 seconds, then 1 minute).

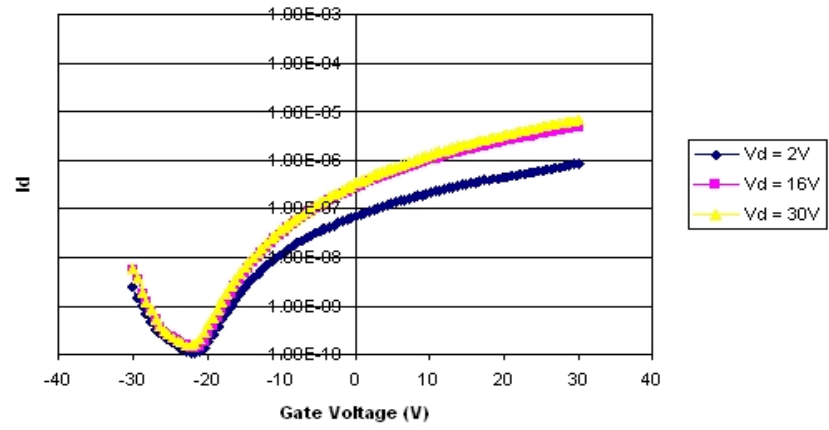
5.6.3 Extraction of Field-Effect Mobility

TFTs typically do not follow exact square-law behavior due to a vertical field mobility dependence, and slower turn-on. For amorphous silicon TFTs mobility is reduced because of multiple carrier trapping in the band tail states. This is dependent on the width of the band tail states and given by the equation:

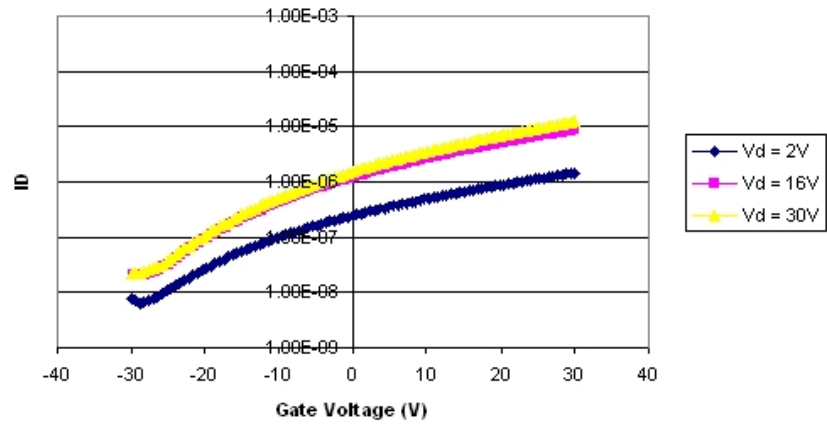
$$\mu_{FE} = \mu_0 e^{-\frac{E_c - E_A}{kT}} \quad (5.4)$$

where $E_c - E_A$ is the width of the conduction band tails.

The mobility of polycrystalline TFTs is limited by the grain boundary barrier height. Most of the lateral voltage is dropped across the grain boundaries because they have high resistance. However, as the gate bias increases the number of carriers at the surface increases, which fills traps at higher energies, and the effective barrier



(a)



(b)

Figure 5.12. (a) IDVG curve for device with 15 second contact anneal. (b) After an additional 1 minute contact anneal.

height at the grain boundaries decreases. At sufficiently high gate bias most carriers are delocalized and move freely through the conduction band. Then typically the mobility is limited by scattering at the interface. The result is a higher mobility for higher gate bias, with a maximum extracted value occurring at the highest tested bias. The gate voltage dependence can be modeled as (55):

$$\frac{1}{\mu_{FE}} = \frac{1}{\mu_1 \left| \frac{2V_{gte}}{\eta V_{th}} \right|^{m_\mu}} + \frac{1}{\mu_0} \quad (5.5)$$

where m_μ , μ_0 , and μ_1 are extracted from measured data, and the value V_{gte} is given by:

$$V_{gte} = \eta V_{th} \left(1 + \frac{V_{gs} - V_{th}}{2\eta V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{gs} - V_{th}}{2\eta V_{th}} - 1 \right)^2} \right) \quad (5.6)$$

where δ is a constant of approximately 2, and η is the subthreshold ideality factor. Below threshold V_{gte} is approximately ηV_{th} and above threshold it is $V_{gs} - V_{th}$.

The overall saturation current equation is then quite complicated. However, for simplicity square-law behavior is typically assumed when extracting mobility. The standard expression of saturation current for single-crystal MOSFETs is used:

$$I_D = \frac{1}{2} \mu_{FE} C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \quad (5.7)$$

However, due to the voltage-dependent mobility and slow turn on it is difficult to extract V_{th} . Figure 5.13 shows a plot of the square root of drain current versus gate bias. At high bias the device shows typical square law behavior and a line can be extrapolated back to the x-axis. This intercept would normally be considered the value for V_{th} , but as the figure shows there can be a large error. Therefore, another method is needed to extract mobility.

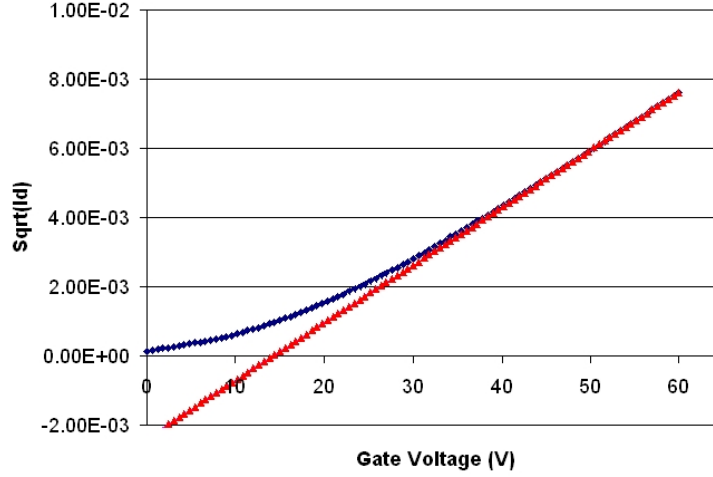


Figure 5.13. Square root of drain current with extrapolated V_{th} .

Transconductance is defined as the derivative of the IDVG curve:

$$gm = \frac{dI_D}{dV_{gs}} \quad (5.8)$$

$$gm = \mu_{FE} C_{ox} \frac{W}{L} (V_{gs} - V_{th}) \quad (5.9)$$

Calculation of gm can be done numerically by taking the slope of the measured data. Then the V_{th} term can be eliminated by taking gm^2 and dividing by I_D :

$$\frac{gm^2}{I_D} = 2\mu_{FE} C_{ox} \frac{W}{L} \quad (5.10)$$

Equation 5.10 can then be used to calculate an effective mobility from measured data without the need for estimating the threshold voltage. One consequence of this method is that the mobility can be calculated for each bias point, and the mobility can be modeled via Equation 5.5.

While this is the most convenient method to calculate mobility, there are several

sources of error. The most significant is probably the presence of finite contact resistance. The method is dependent on the calculation of the slope of the IDVG curve, and assumes square law behavior. If contact resistance is significant, the measured device is effectively two resistors in series with a transistor, and the overall IDVG curve will be linearized. As a result the calculated value of gm will be artificially low, and the extracted mobility will be lower than the actual mobility.

Having understood the methods of extracting mobility and the limitations therewith, it is now possible to study the impact of various CBD deposition parameters on mobility. These may then be used in turn to optimize mobility, thus allowing the realization of a high-performance transparent transistor technology suitable for use in high-resolution, high-brightness OLED-based displays.

5.6.4 Dependence of Field-Effect Mobility on Bath pH

The CBD process shows strong dependency on the pH of the solution, and therefore substantial optimization may be achieved through control of solution pH. In order to measure the effect of bath pH eight baths were prepared using the normal reagent concentrations, with only the pH varied by addition of ammonium hydroxide. Depositions were done at 60 °C for 30 seconds and annealed at 550 °C for two hours. Figure 5.14 clearly shows a strong dependence on pH with a peak at 11.3. This stresses the importance of careful control of reaction conditions and reagents. For instance, the pH of stock ammonium hydroxide solutions will drop over time. If an old stock solution is used then the pH will be lower than 11.3, and the device mobility will be degraded. All depositions were therefore carried out at a pH of 11.3.

The increased volume of ammonium hydroxide will not only increase the pH but also the concentration of ammonia complexing agent (Equation 4.16). This will decrease the rate of the reaction by inhibiting the release of zinc ion from the ammonia

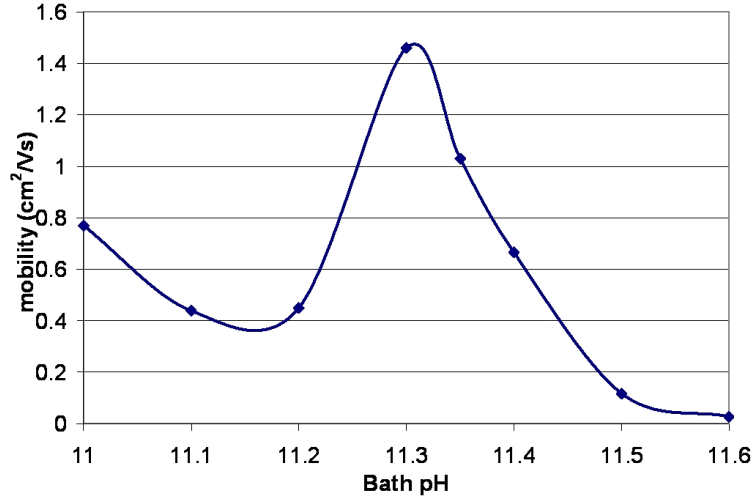


Figure 5.14. Dependence of mobility on bath pH.

complex. This is evident in Figure 5.15 which shows the thickness variation for samples grown for 30 seconds. At higher pH the final thickness (and hence the rate) decreases with pH.

5.6.5 The Effects of Bath and Anneal Temperatures

The temperature of the CBD bath also affects film quality and the resultant device mobility and on/off ratio. In general, increased bath temperature results in higher performance for reduced anneal temperatures. The effect is most pronounced when increasing from 50 to 60 °C, which results in nearly an order of magnitude increase in mobility. This may be due to the tendency of $\text{Zn}(\text{OH})_2$ to convert to ZnO during the deposition at temperatures above 50 °C (see Section 4.7.1).

As expected, anneal temperature strongly impacts mobility (Figure 5.16). Annealing at 700 °C resulted in mobilities of approximately 2.5 cm²/Vs regardless of deposition temperature, but the dependence on bath temperature is clearly seen for samples annealed at 450 °C (Figure 5.17). Inexpensive soda lime glass is compatible

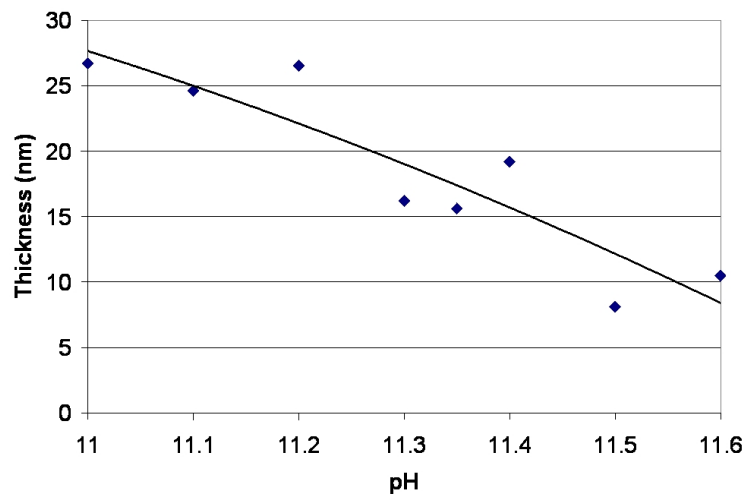


Figure 5.15. Variation in deposited film thickness with bath pH for fixed deposition time, showing change in deposition rate.

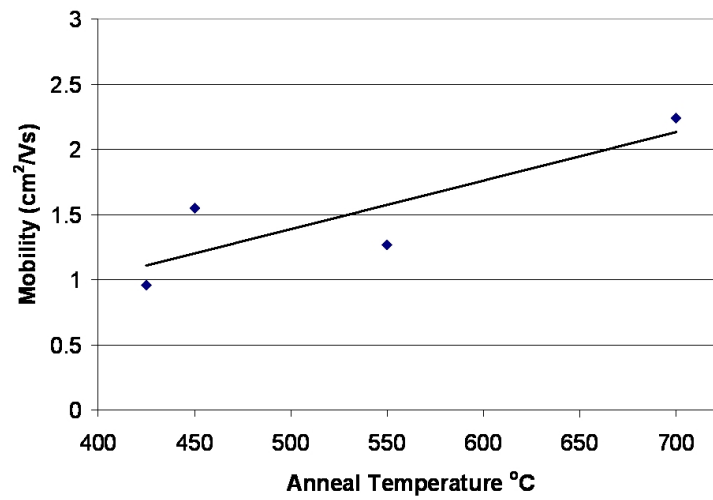


Figure 5.16. Variation in TFT mobility with anneal temperature, for bath temperature of 60 °C.

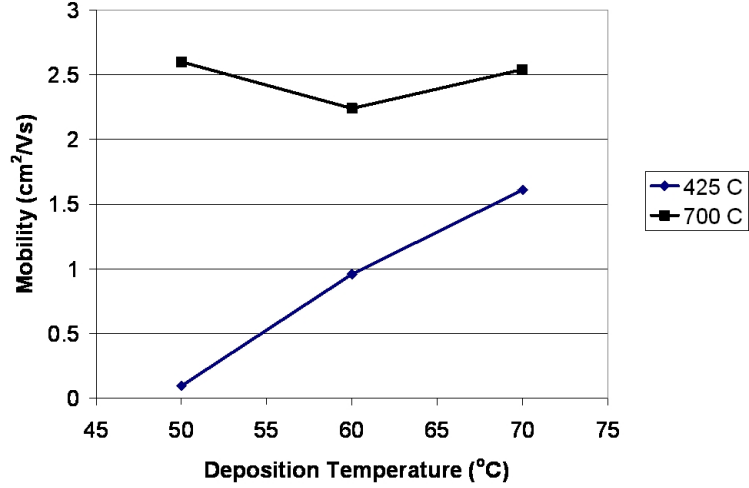
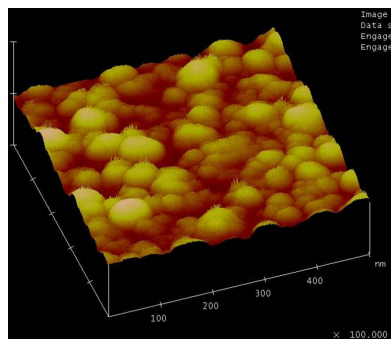


Figure 5.17. Variation in TFT mobility with bath temperature for different anneal temperatures.

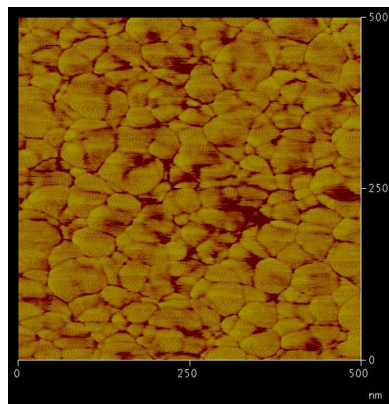
with temperatures below 450 °C, and mobilities above 1.5 cm²/Vs are realized in that temperature range.

The higher mobility is explained by change in the grain size (Figure 5.18). AFM was used to examine grain size rather than XRD due to the thin semiconductor films. As anneal temperature increases average grain size also increases, which is consistent with the higher mobility seen at elevated temperatures. Surface roughness also increases, but this is not surprising given that the grain size is similar to the film thickness.

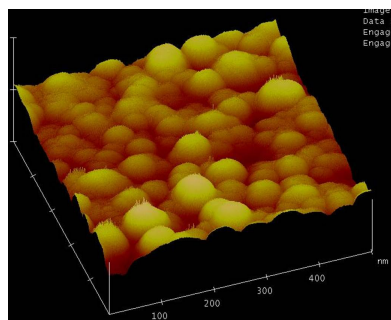
By combining a high bath temperature and a glass-compatible (<600 °C) anneal, it is possible to achieve substantial performance improvement over the state of art; thus, mobilities substantially greater than that achieved in α -Si are realized while delivering solution-processed fabrication and optical transparency.



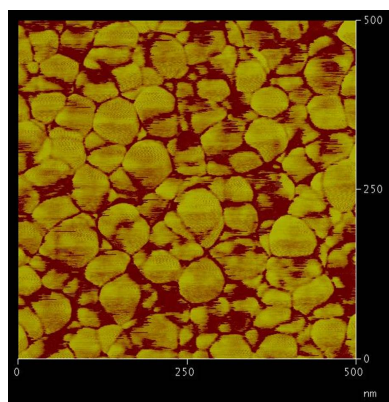
(a) 425 °C Height



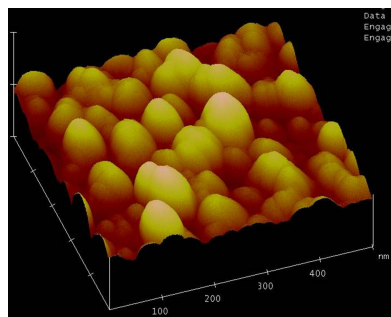
(b) 425 °C Phase



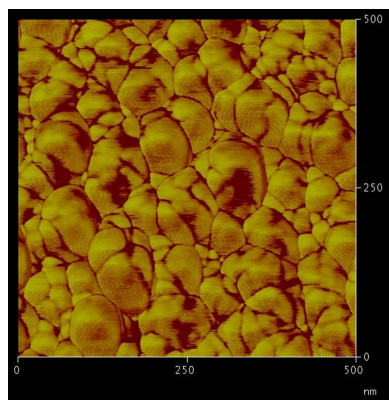
(c) 550 °C Height



(d) 550 °C Phase



(e) 700 °C Height



(f) 700 °C Phase

Figure 5.18. AFM images of CBD ZnO films after anneal.

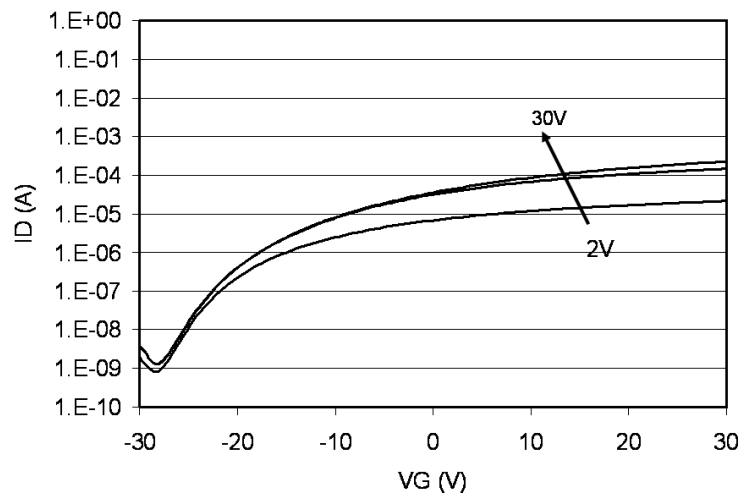


Figure 5.19. Transfer characteristics for a typical CBD ZnO TFT ($W/L = 400/100 \mu\text{m}$).

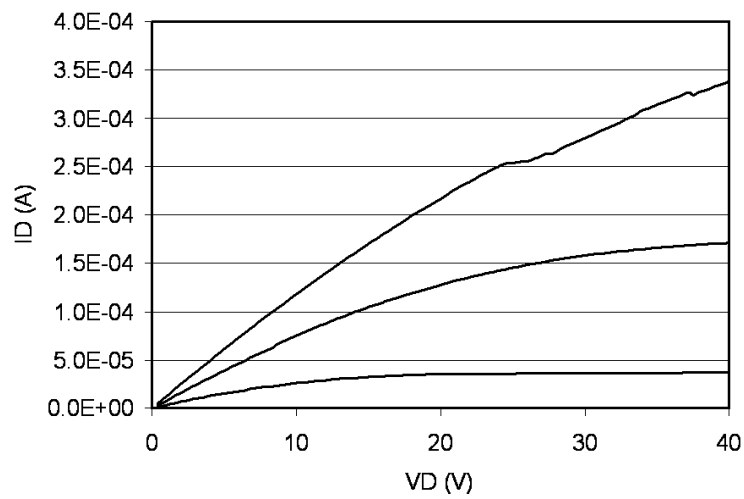


Figure 5.20. Output characteristics for the above transistor.

5.6.6 Current-Voltage Characteristics

Typical device I-V characteristics are shown in Figures 5.19 and 5.20. Mobilities as high as $3.5 \text{ cm}^2/\text{Vs}$ are obtained, with average mobility for a $<600^\circ\text{C}$ process being $2 \text{ cm}^2/\text{Vs}$. This is a substantial improvement over other reported solution-processed devices. Indeed, devices with this mobility range are obtained at temperatures as low as 450°C , though on/off ratio is typically degraded (Figure 5.21). This dramatic improvement in performance has been achieved through optimization of the CBD process.

It is apparent from the ID-VG curve that these devices are fairly conductive in the off-state, meaning either the carrier concentration in the films is high, or interface states pin the Fermi level near the conduction band creating an accumulation layer. The carrier concentration and Hall mobility are measured in Section 5.7, where this issue is addressed further. The devices with the best on/off ratio (measured from $-30 < V_G < 30 \text{ V}$) typically had at best a zero-to-max current ratio of 10^3 . While this is not ideal, it is not uncommon to require a negative gate bias to fully turn off polycrystalline TFTs. The magnitude can be reduced by reducing the oxide thickness (which will reduce the operating voltages altogether) and by thinning the semiconductor layer. The choice of 100 nm thick oxide is higher than is needed, but was used because it was a standard process in our group. A 50 nm oxide would have been more appropriate.

5.6.7 Dependence of Film Thickness

In an effort to reduce the voltage required to fully turn off these TFTs the film growth time was varied, and the effects on film thickness, mobility, on/off ratio, and turn-off voltage were studied. The deposition process was run in the same manner,

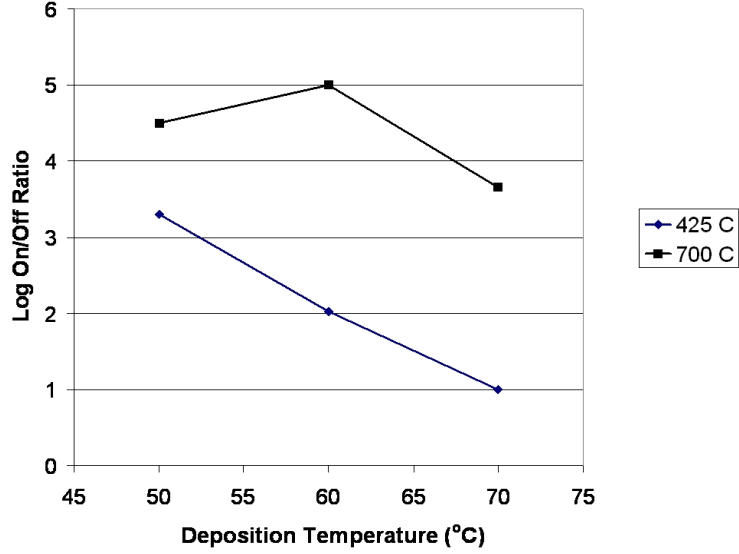


Figure 5.21. Variation in TFT on/off ratio with anneal.

but growth time varied from 15-30 seconds, instead of the standard 30 seconds. The resulting on/off ratio versus thickness is shown in Figure 5.22. Substantial improvement in on/off ratio can be achieved by thinning the film, but at the cost of reduced mobility (Figure 5.23). The lower mobility is a result of the grain size being limited by the extremely thin films. A sample ID-VG curve is shown in Figure 5.24.

In order to determine whether the poor on/off ratio is the result of high carrier concentration or from interface states, Hall Effect measurements were taken to measure the carrier concentration and mobility. Since carrier concentration is controlled primarily by oxygen deficiency it is possible that the higher temperature oxygen anneals simply reduced the free carriers. Alternatively, the interface states could be caused by unreacted zinc ions at the gate oxide interface, which are then reacted under oxygen atmosphere only at elevated temperature.

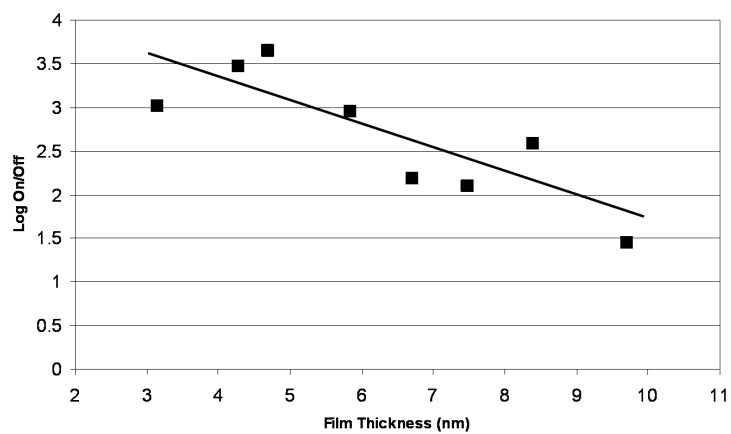


Figure 5.22. Variation in TFT on/off ratio with film thickness.

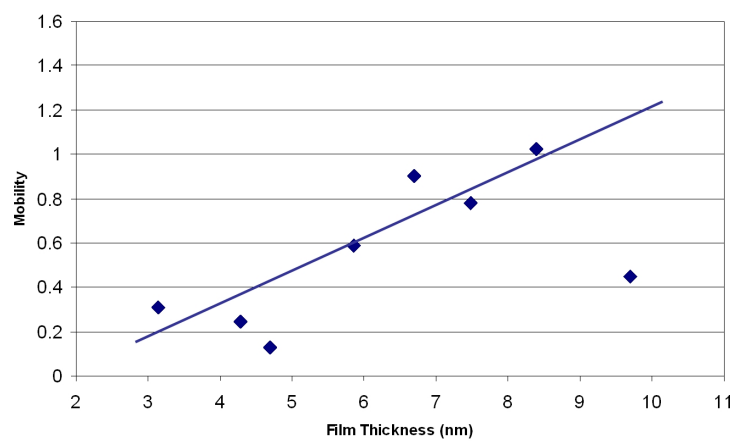


Figure 5.23. Variation in TFT mobility with film thickness.

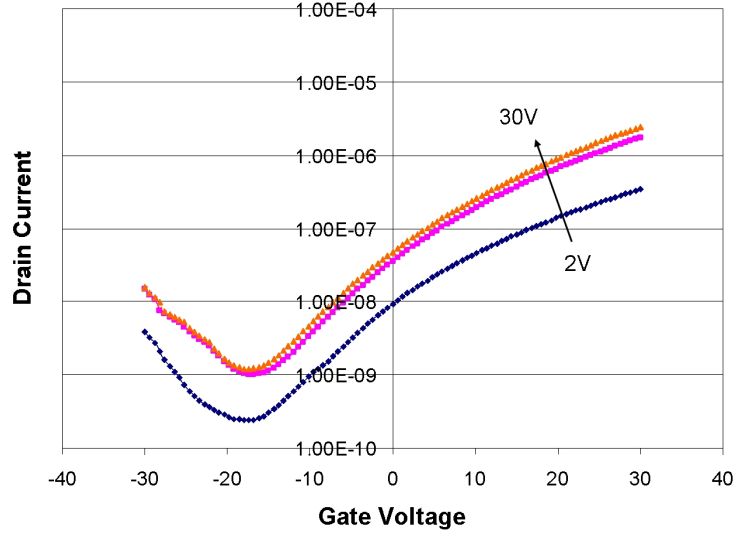


Figure 5.24. ID-VG curves for a TFT with a 4.3 nm ZnO film annealed at 450 °C .

5.7 Hall Effect Measurements of CBD ZnO Films

Hall Effect measurements were performed on the CBD zinc oxide films after anneals at 450-700 °C. Fabrication of the samples was done on insulating quartz substrates. Since ZnO is not visible on top of quartz a multi-layer structure was created by depositing 200 nm of Si_3N_4 , followed by 200 nm of SiO_2 by PECVD (Figure 5.25). Inserting the nitride layer, which has an index of refraction of approximately 2, caused thin-film interference that colored the substrate. The zinc oxide deposited on top of the SiO_2 then caused an obvious color shift, allowing the zinc oxide pattern to be seen. For example, the substrates were normally colored orange, but the ZnO areas appeared blue. After a blanket 150 nm zinc oxide deposition, photoresist was pipetted onto the surface to make a circular drop approximately 8 mm in diameter, and then the zinc oxide was etched in 1% H_2SO_4 . The photoresist was then removed by rinsing in acetone.

The Hall Effect results make it clear that the TFT on/off ratio is determined not by the film conductivity, but rather by a significant number of interface states. This



Figure 5.25. Structure of the Hall Effect samples.

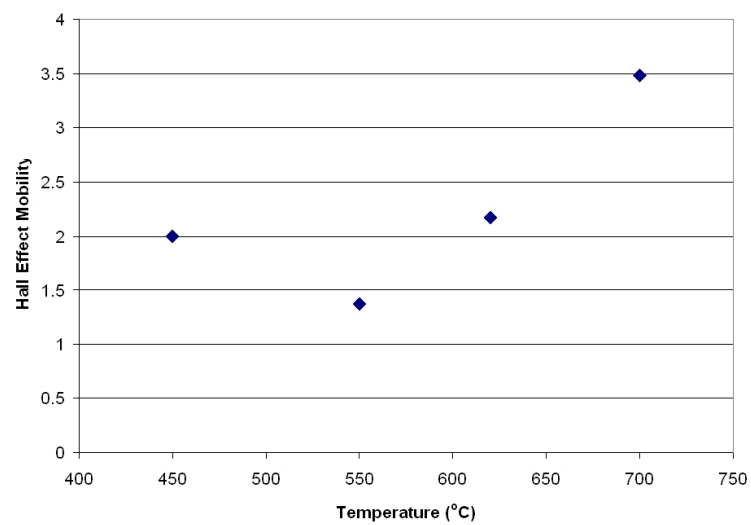


Figure 5.26. Measured Hall Effect mobility versus anneal temperature.

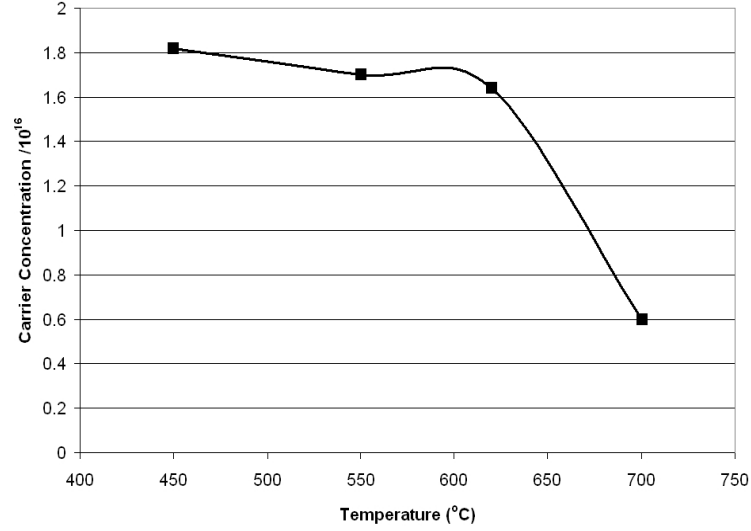


Figure 5.27. Hall Effect carrier concentration versus anneal temperature.

is a very promising result because the properties of the film (in terms of mobility and carrier concentration) are satisfactory when annealed at low glass-compatible temperatures (450 °C). Reduction of interface states can be achieved through device engineering, for instance, by moving to a top-gate structure where the zinc oxide seed layer would not be at the gate oxide interface.

5.8 Conclusion

TFTs formed using solution-processed ZnO deposited using chemical bath deposition have been demonstrated. Mobilities as high as 3.5 cm²/Vs have been achieved. By optimizing bath conditions and anneal conditions, we have demonstrated transparent TFTs in a glass-compatible process flow with mobility greater than 2 cm²/Vs; coupled with the viability of full-pixel coverage allowed by the optical transparency of ZnO, this will enable the realization of high-brightness, high-efficiency active-matrix OLED displays on glass using low-cost fabrication processes.

One remaining concern with zinc oxide is long-term reliability, which is an issue not only with the deposition method presented in this work, but also in sputtered systems. In silicon systems there are several methods of passivation used to improve device stability, but these techniques are not readily adaptable to zinc oxide. Hydrogen passivation cannot be used because hydrogen treatment is known to increase the carrier concentration by creating oxygen vacancies. This leads to an unacceptable degradation of the on/off ratio. Halogens have also received attention for silicon passivation, but if a halogen substitutes for an oxygen atom it can act as a donor and increase carrier concentration. Other elements are also ruled out, such as transition metals with oxidation states above +2. Therefore new passivation techniques must be developed, and this is an active area of research.

Chapter 6

Conclusions and Future Work

6.1 Low-Cost Fabrication Techniques

This thesis covers a wide array of subjects, from electromagnetic coupling to inorganic chemistry, with a focus on making electronic devices as cheaply as possible while still meeting minimum performance requirements. The challenge is met through careful analysis of each particular application, be it RFID or OLED displays, and then by applying processing techniques known to be less expensive than the current state-of-the-art. While very simple in principle the challenge lies in making it work, which is the art of engineering.

Through a careful study of the chemistry of solution-based material deposition, the optimization of material properties, and the impact of the same on device parameters, it is possible to realize remarkable improvement in performance and to realize high-quality devices formed entirely through solution-processing. Indeed, in this work, we have reported on the first all-printed passive component process demonstrated on plastic, the first use of printed gold nanoparticles to seed an electroless copper

deposition, and finally, the first demonstration of a zinc oxide TFT fabricated using chemical bath deposition.

The strength of inkjet printing really lies in the wide range of material compatibility and accuracy of drop placement, making it an ideal patterning device. Ideally a low-cost process would be fully reel-to-reel and all-printed, but in reality printing has limitations. Materials with excellent printing properties do not always have the desired electrical properties, and vice versa. For certain applications, such as deposition of highly conductive metal on plastic, the combination of inkjet printing and solution processing has been shown to give superior results compared to printing alone. The application of this technique to other devices, such as transistors, is discussed below.

6.2 Future Work

Zinc oxide TFTs fabricated using chemical bath deposition are promising because they would dramatically lower the cost of AM-OLED displays. The mobility of these devices annealed at temperatures compatible with cheap glass ($<450^{\circ}\text{C}$) is more than adequate, however, the operating voltages are still comparable with α -Si and need to be reduced. This can be attempted from several directions. Moving to a thinner oxide has been mentioned previously, but the devices fabricated here are all back-gated test structures which are not useful, other than as test structures. The real challenge (and potential improvement) comes with the integration of a CBD zinc oxide layer with a CBD high- κ dielectric, such as zirconia. The use of a thinner high- κ dielectric would significantly reduce the operating voltages, and bring the device one step closer to a fully solution-processed TFT.

Integration of a CBD dielectric is only one step in moving from a test structure to a usable device. Patterning of the active areas would ideally not be done through

a mask, but rather via inkjet printing of the materials used to control selectivity. This assumption was made when calculating the mobility requirements of transparent TFTs for displays, but it has not been done.

While these particular CBD conditions have shown excellent results, there may also be room for optimization of the chemistry. Most data in this thesis is taken from devices deposited at 60 °C, because the reaction proceeds very quickly at higher temperatures at it is not easy to control. If the reaction could be slowed either through change in reagent concentration or pH (perhaps having to find a new optimum pH), then it could be run at higher temperatures. This would possibly result in even higher mobility.

Finally, if the ZnO process temperature could be lowered to below 200 °C, then it would be compatible with plastic substrates. In theory, the conversion of Zn(OH)_2 to ZnO occurs at these low temperatures, but the reaction used here did not produce high mobility TFTs until the substrates were annealed at a minimum temperature of 300 °C. Mobility on the order of $10^{-2} \text{ cm}^2/\text{Vs}$ was achieved at 200 °C, so there is certainly room for improvement.

In summary, the improvements to the CBD ZnO TFT process fall into the categories of inkjet patterning, integration with other CBD materials, optimization of the bath chemistry, and reduction of the process temperature to plastic-compatible levels.

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Appendix A

Algorithms and Methods for Inkjet Printing of Electronic Structures

The printer accepts input files with move and drop commands, which means each drop must be specified individually. Needless to say this becomes impossible to do by hand for any structure requiring more than a few dozen drops. Typical print jobs run in the neighborhood of 100,000 to 500,000 drops. A structure library was written in C++ to automate this process. This library is included in a program that will define the structures, which is then compiled and run to generate the printer input file. This technique is an extremely powerful method of generating files, and it is very easy to align layers of metal and dielectric.

The library has functions to create the following structures: lines, squares, rectangles, four-point resistivity test structures, square inductors, spiral inductors, baluns, GSG probing structures, and transformers. There are also functions provided to assist in the creation of custom structures, such as movement, triggering the print head, and accessing the current position.

All structures are created using a set of lines. Squares and rectangles are made from rows of lines spaced approximately $60\text{ }\mu\text{m}$ apart so that they overlap. The code is flexible enough that the direction that both the lines and drops are printed can be specified for rectangular structures. This allows any of the four corners of a rectangle to be used as the origin. Because of the discrete nature of the drops, it is not always possible to end lines with exactly the correct length, and depending on the drop spacing there could be an error of about 10 microns. It is also not possible to place

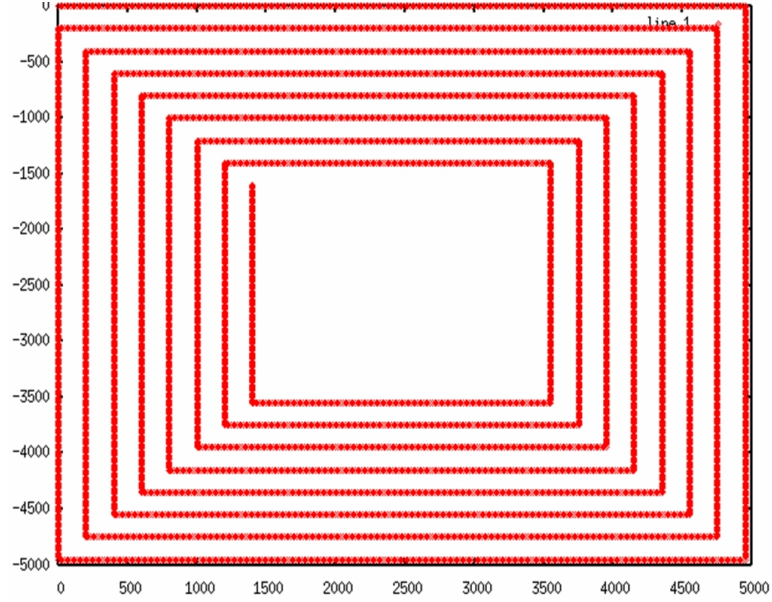


Figure A.1. Output of printer file simulator showing square inductor.

the last row of a rectangle so that the last edge makes the overall size exactly what is specified. In general, all other structures are composed of single-width lines, and it is necessary to specify the line and drop spacing only. Algorithms for inductors and transformers are very general, and can accommodate any size, line width, spacing, and number of turns.

Because of the time and cost involved in printing each structure a simulator was written in order to test printer input files. The simulator reads in printer input files directly, generates a matrix of drop locations, and then plots the resulting matrix. A point is placed at each drop location, which means the resulting plot is not to scale, but it is sufficient to verify the drop locations. Coincidentally structures such as inductors end up drawn almost to scale (Figure A.1). The simulator is a simple MATLAB script that reads in the printer input file line by line, tracks the head movement, and stores drop locations in a matrix.

Up to this point all structures discussed have been made with lines that were restricted to Manhattan layout. Spiral inductors, which generally obtain higher quality factors than their square counterparts, require lines printed at angles. Spiral inductors are created in a piecewise-linear manner; so again, the structure is simply broken down into a set of lines.

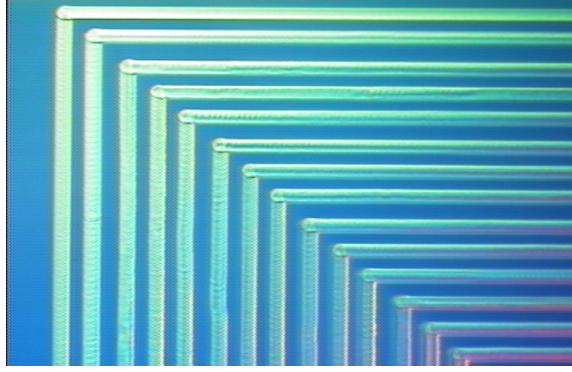


Figure A.2. Close-up of actual printed square spiral structure.

The need to make non-Manhattan lines presents an interesting rounding problem. The printer only accepts movements in increments of $1\text{ }\mu\text{m}$, and an attempt should be made to place drops using the given drop spacing, regardless of the direction the line is printed. A simple (and incorrect) way to implement this function is as follows:

```

Angled_Line(int Xstart , int Ystart , int Xstop , int Ystop ,
            int Drop_Spacing)
{
    int y = Ystop-Ystart;
    int x = Xstop-Xstart;
    double theta = atan(double(y)/double(x));

    int signx = x&0x80000000?-1:1; // left as an exercise
                                // for the reader

    int dx = round( Drop_Spacing * cos(theta) ) * signx;
    int dy = round( tan(theta) * dx );
    int Xtemp = xstart;

    while(! ( abs( Xstop - Xtemp ) < abs(dx) ) ) {
        print_drop();
        Xtemp += dx;
        move_head(dx, dy, 0);
    }
}

```

The function calculates, based on the angle of the line, a static dx and dy to be moved each drop. The error in dy is at most $0.5\text{ }\mu\text{m}$, but it occurs for every drop, and when there are several hundred drops in a line that error becomes very significant.

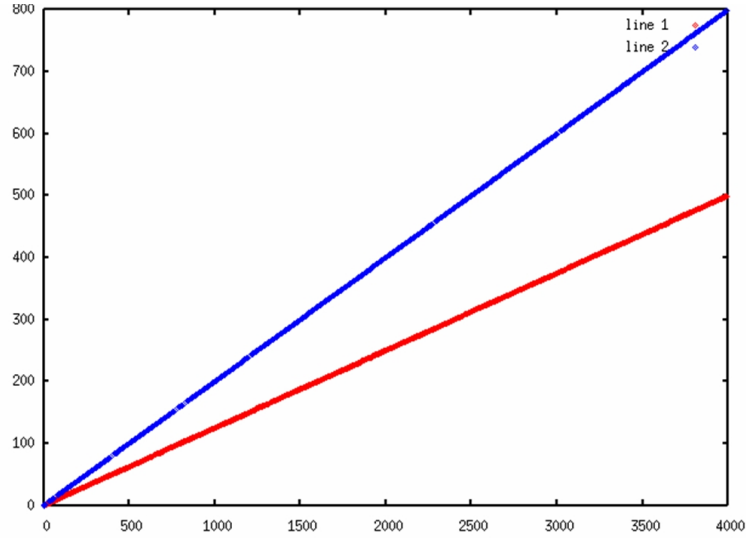


Figure A.3. The error created by rounding can be significant. The lower line was the intended one, but instead the upper line would have been printed.

Figure A.3 shows the gross errors that this algorithm creates. The line was supposed to go from the origin to the point (4000, 500) shown by the lower line, but instead the line ended up closer to (4000, 800).

This problem was fixed by recalculating dy for each drop location. Rather than calculate dy based on the x increment, the correct y -position is calculated based on θ and the current x -position, then rounded to the nearest integer, and the previous y -position is subtracted to give dy . Note that the dx value is kept static, so there is still a small error in the drop spacing, but in practice this has not been an issue.

However, the algorithm still has a subtle error. When a line is almost vertical, $\cos(\theta)$ is close to zero, and hence dx is zero. There are several creative ways to work around this problem; a simple one involves breaking these lines into three vertical segments and shifting each one by a few microns in the appropriate direction. Figure A.4 shows a corrected spiral inductor.

As discussed in Section 3.4.4, inductor quality factor increases with increased line width. Therefore an algorithm was developed to print inductors with line widths greater than a single drop diameter. Analogous to the rectangle printing method, two lines can be overlapped slightly to create a wider line. Spiral structures with wide

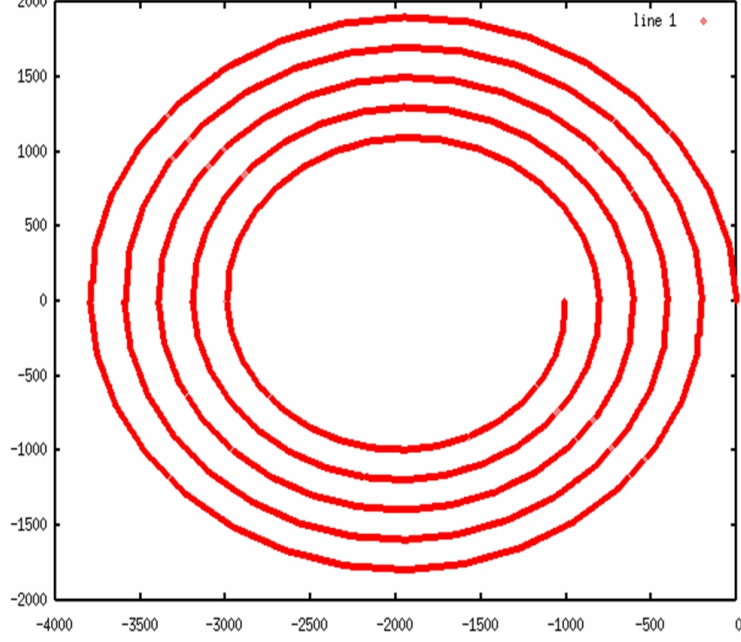


Figure A.4. Spiral inductor generated using segment and shift method for almost vertical lines.

lines can be printed by overlaying several spirals of normal (single drop) line width. However, the parameters of each spiral must be adjusted. For a final structure with radius R , line spacing S , line overlap O , and number of spirals n , the parameters of the i_{th} individual spiral are:

$$linespacing = S + n * O \quad (A.1)$$

$$origin(x, y)_i = (x_{i=0} - i * O, y_{i=0}) \quad (A.2)$$

$$radius_i = R - i * O \quad (A.3)$$

with the spiral algorithm accounting for the width of each printed line. Figure A.5 shows the drop pattern generated using this algorithm.

This algorithm is capable of generating spiral structures of arbitrary line width, number of turns, turn spacing, and radius. Thus, inductor geometry can be fully optimized for a given application.

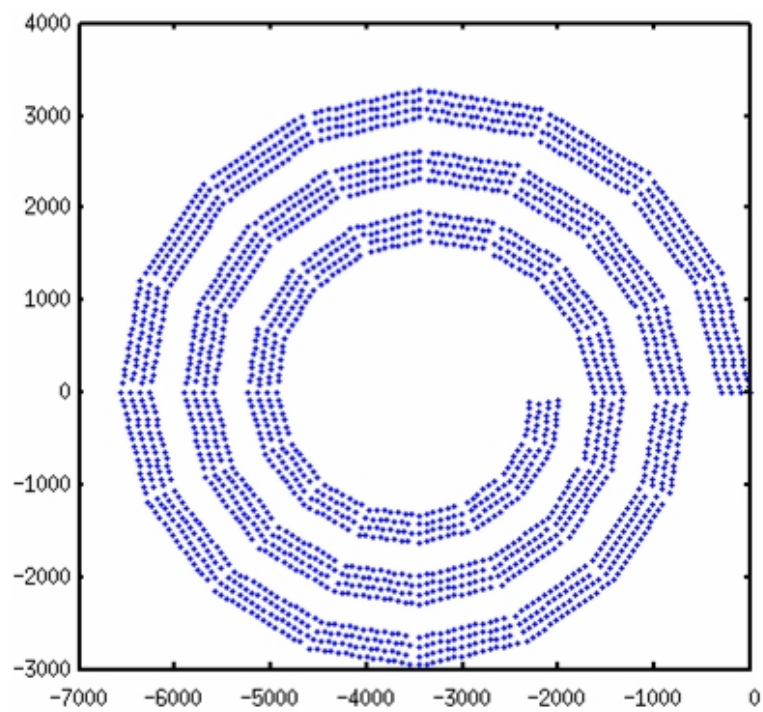


Figure A.5. Drop pattern for inductors of arbitrary line width.

Appendix B

Gold Nanocrystal Synthesis

Gold nanocrystals are created using a two-phase chemical reaction. The length of the thiol encapsulant will determine the temperature that the encapsulant burns off, and the amount of thiol added will determine the size of the nanocrystals. Higher concentrations of thiol will result in smaller nanocrystals because they are encapsulated earlier in the growth process. A detailed examination of thiol length and concentration was done by Daniel Huang as an undergraduate researcher in our group, and much of the printed work since that time has been enabled by his efforts (50).

The most common nanocrystal system used in our group is hexanethiol encapsulated gold. Using a 4:1 molar ratio of hexanethiol to gold results in nanocrystals approximately 1.5 nm in diameter. The synthesis of these nanocrystals is presented here in detail. The materials needed are:

Hydrogen tetrachloroaurate(III) hydrate	$\text{HAuCl}_4 \cdot x\text{H}_2\text{O}$
1-Hexanethiol	$\text{C}_6\text{H}_{13}\text{SH}$
Sodium Borohydride	NaBH_4
Tetraoctylammonium Bromide	$\text{C}_{32}\text{H}_{68}\text{BrN}$
Toluene	C_7H_8
Deionized water	H_2O
Ethanol	$\text{C}_2\text{H}_5\text{OH}$
Acetone	$(\text{CH}_3)_2\text{CO}$

The reaction is two-phase for several reasons. The thiol encapsulant is very non-polar and not soluble in water. This is desired because then the nanocrystals are also soluble in nonpolar solvents. Therefore the thiol is added to the organic toluene phase

of the reaction. Sodium borohydride (the reducing agent) is soluble only in water, as is the gold ion. Tetraoctylammonium bromide is called a transfer agent, and is used to “transfer” the gold ion to the organic phase. It basically forms a complex with gold ion that is large enough to be soluble in the organic phase. The sodium borohydride aqueous phase is added and the solution vigorously stirred. The analogy of a mixture of oil and water is applicable; unless the solution is stirred the two phases will separate. The reduction reaction actually occurs at the organic/aqueous interface as the solution is stirred. A purification process then follows.

Since the gold is light and air sensitive it should be dissolved in water as soon as it is opened. Since it is ordered in 5 g vials the entire vial is dissolved into 400 mL DI water and then split in half. Two reactions are then run in parallel.

The detailed steps are:

- Add 12.10 g of tetraoctylammonium bromide to a vigorously stirred solution of 645 mL toluene. (Organic phase)
- Add 2.5 g of $\text{HAuCl}_4 \cdot x\text{H}_2\text{O}$ to 200mL of deionized water. This should be a yellow solution. (Aqueous phase)
- Mix solution the aqueous phase in the vigorously stirred organic phase. The aqueous phase should now be clear and the organic phase should be orange-brown.
- Isolate the organic phase and add 4.152 mL of hexanethiol (4 moles of thiol to 1 mole of gold). The solution must be stirred for at least 15 minutes at room temperature. The solution should become pale yellow or colorless.
- Mix 3.065 g of NaBH_4 in 200mL of deionized water. (Reduction solution)
- Vigorously stir the organic phase as the reduction solution is added in. Pour the reduction solution into the organic phase in about 20 seconds. The solution should now become very dark.
- Stir the solution for 3.5 hours at room temperature.
- The reaction is now complete, and the nanocrystals can be left in solution overnight (if necessary) before purification.

- Isolate the organic phase and remove all the solvent in a rotary evaporator. Do not allow the temperature to exceed 35 °C to prevent partial decomposition of large gold cluster and removal of surfactant.
- Suspend the particles in 240 mL of ethanol and sonicate the suspension briefly for complete dissolution of byproducts.
- Collect particles on a glass filtration frit (Fine). Wash with 650 mL of ethanol and 1200 mL of acetone.
- Air dry particles and collect them from the frit.
- There should be approximately 1 gram of nanocrystals from each batch.