A 98% peak efficiency 1.5A 12V-to-1.5V Switched Capacitor dc-dc converter in 0.18um CMOS technology

Vincent Wai-Shan Ng
Seth R. Sanders

Electrical Engineering and Computer Sciences
University of California at Berkeley

January 13, 2008

A 98% peak efficiency 1.5A 12V-to-1.5V Switched Capacitor dc-dc converter in 0.18μm CMOS technology

by Vincent W Ng

Masters Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

Approval for the Report and Comprehensive Examination:

Committee:

Professor Seth Sanders
Research Advisor

(Date)

* * * * * * *

Professor Elad Alon
Second Reader

(Date)

Table of Content

List of figures and tables

Abstract

This thesis presents a 12V-to-1.5V Switched-Capacitor dc-dc converter. The overall circuit is a Dickson-type 8-to-1 step down converter in a 0.18μm CMOS technology. The power transistors are implemented with native 0.18μm 1.8V NMOS and 0.5μm 5V NMOS, whereas the power-train capacitors are implemented with off-chip ceramic capacitors. The die is divided into various voltage domains isolated with triple-well nwell structures to ensure that no terminal of any transistor has overstress voltage levels, even though, each terminal itself may be as high as 15V above the substrate voltage level. This circuit shows a peak efficiency of 98% at 50mA load and a maximum load of about 1.5A. Significantly, the efficiency remains at 90% or higher for the load range from 6 mA to 400 mA without need for any mode or switching frequency adjustments. The efficiency at low load condition can be further increased by reducing the switching frequency of the circuit. The active die area is 3 mm^2 out of a total area of 9mm^2. All power switches are located at the periphery of the die to minimize on-chip metal resistances, leaving the middle portion of the die empty. The experimental efficiency data matches very well with the theoretical curve. If solder bump pads are used to eliminate bondwires and other interconnect pathways to the printed circuit board, the output referred resistance can be potentially reduced by 50% while reducing the die area by 66%.

1. Introduction and Motivation

This work explores the design and development of CMOS-based switched-capacitor (SC) dc-dc conversion circuitry aimed at applications traditionally addressed with the ubiquitous buck converter. The traditional buck converter requires at least one substantial inductor and transistors with voltage rating matched to the input source voltage, which may be costly to integrate in a submicron CMOS technology. The traditional buck converter also suffers from low efficiency or poor power device utilization when used in a high-conversion-ratio application. Figure 1 [1, 2] shows the relative conduction loss of an SC converter when compared to a boost converter and transformer-bridge converter for a given G-V^2 product for power switches, where G is the conductance and V is the blocking voltage of power switches. The G-V^2 product roughly corresponds to silicon area for MOSFET transistors and thus represents device cost in this analysis. Besides suffering from low efficiency in a high-conversion-ratio application, the buck converter efficiency also degrades rapidly in low-power modes unless additional special modes (like PFM) are enabled. Switched-capacitor dc-dc converters, on the other hand, can sustain high efficiency with a high conversion ratio, and also over a very wide load range. Moreover, SC dc-dc converters do not require any magnetics or high voltage transistors. As discussed in this thesis, each power transistor needs to only block a fraction of the input voltage, thus allowing a high voltage dc-dc converter to be built in a submicron technology with native transistors.

This thesis first summarizes the background theory and work in designing an SC dc-dc converter in submicron CMOS technology. This includes the mathematical calculations
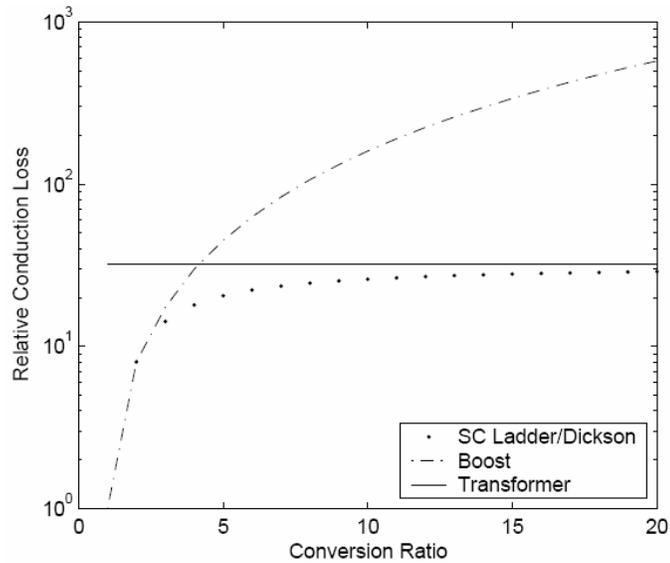
Figure 1: Conduction Loss Comparison

and optimization procedures of designing an SC dc-dc converter [1, 2], and an analysis of the latch-up issues and voltage stress concerns of triple well devices. Afterwards, the thesis will focus on the design issue of the switched capacitor dc-dc converter and the test results of the first prototype. This prototype is a 12V-to-1.5V SC dc-dc converter in a 0.18μm CMOS technology with a peak output current of 1.5A and a peak efficiency of 98%. The result not only shows that 12V conversion is indeed possible in a submicron technology, but that this converter has very attractive performance and efficiency over a wide load range, in spite of the high conversion ratio. This converter is ideal for the point-of-load application in which a dc-dc converter is placed close to an associated load.

2 Background Theories and Previous Work

2.1 Analysis and optimization procedures for SC dc-dc converters

2.1.1 Performance analysis of SC dc-dc converters

The losses in SC dc-dc converters can be separated into load dependent losses and load independent losses. Load independent losses refer to the power consumed by the converter at zero load condition. In the case of an SC dc-dc converter, this loss mostly arises from charging and discharging parasitic capacitances, for example, the gates of power switches. These losses can be easily calculated by using conventional circuit analysis. For example power switch gate losses can be calculated by CV^2f, where C is the value of the parasitic capacitor, V is the voltage swing of the capacitor and f is the switching frequency of the converter. Load dependent losses, on the other hand, are less intuitive to calculate. They are modeled by an output referred resistance, and will be the focus of this section.

Makowski and Maksimovic [6] use the fundamental loop matrices and the fundamental cut-set matrices to derive an SC dc-dc converter's output impedance. The analysis is fundamental but requires a fair amount of calculations. Seeman and Sanders [1, 2] derives a simpler methodology based on Tellegen's theory [7] and Kirchhoff's law. This methodology is easier to use and is summarized below.

Seeman and Sanders [1, 2] divide the load dependent losses into slow switching limit regime and fast switching limit regime. The slow switching limit corresponds to operation at sufficiently low frequency that capacitor voltages fully equalize after each

switch event. Losses in this regime are due to voltage swings in the power-train capacitors during each cycle. The losses are only dependent on the sizes of the power-train capacitors and the switching frequency. On the other hand, the fast switching limit is characterized by nearly constant current flows between power-train capacitors. The switch on-state resistance and other parasitic resistances are sufficiently large such that during each phase, the capacitors do not approach equilibrium. In this asymptotic limit, the currents between power-train capacitors are constant and capacitor voltages are modeled as constant. Losses in the fast switching limit are due to conduction losses in the resistances within the converters. These resistances include the power switch triode region resistance and parasitic resistances. The losses in these two regimes are dependent on two separate lists of parameters, and thus allow the designer to consider the operation in these two regimes separately. The total output referred resistance can be approximated [1, 2] as:

$$R_{OUT} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{1}$$

where R_{SSL} and R_{FSL} are the slow switching limit asymptotic resistance and fast switching limit asymptotic resistance respectively. The method to calculate these terms will be discussed in the following sections.

2.1.1.1 Slow Switching Limit output referred resistance:

In the slow switching limit, the output referred resistance is given by:

$$R_{SSL} = \sum_i \frac{(a_{c,i})^2}{C_i f_{sw}} \tag{2}$$

where f_{sw} is the switching frequency, C_i is the capacitance of capacitor i and $a_{c,i}$ is the

charge multiplier coefficient of capacitor i. Coefficient $a_{c,i}$ can be considered simply as
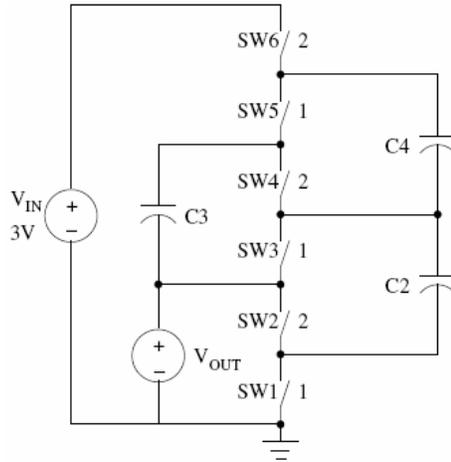
Figure 2: Ladder-type SC converter

a) phase 1

b) phase 2
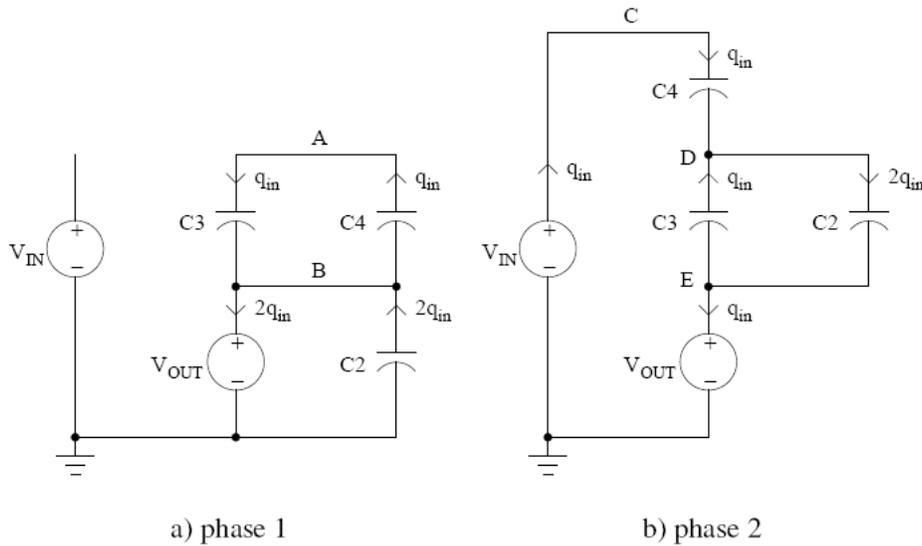
Figure 3: Capacitor charge flows

the ratio between the charge flow in C_i and the output charge flow in steady state. The

way to obtain this number is illustrated with an example below [1, 2].

Figure 2 [2] shows a step down Ladder-type SC converter and Figure 3 [2] shows the

charge flow in the two clock phases during steady state. First the charge supplied by V_{IN}

is denoted as q_{in}. Since V_{IN} is only connected to the converter in phase 2, the charge flow

to C_4 in phase 2 ($q_{c4,2}$) is q_{in}. By conservation of charge, C_4 has to supply an equal amount of charge in phase 1, that is $q_{c4,1} = -q_{c4,2}$. Thus the charge flowing into C_3 ($q_{c3,1}$) during phase 1 is equal to q_{in}. Using Kirchhoff's Current Law (KCL) on node D in phase 2, the charge flowing into C_2 ($q_{c2,2}$) is equal to $2q_{in}$. Similarly, the amount of charges flowing into and out of each capacitor and terminals in each phase can be determined. Using this analysis, one can show that the total amount of charge flowing into the output terminal is $3q_{in}$. The charge multiplier coefficient $a_{c,i}$ can then be determined by dividing the charge flow of each capacitor by the charge delivered to the output terminal.

$$a_{c,i} = \left| \frac{q_{ci,1}}{q_{out}} \right| = \left| \frac{q_{ci,2}}{q_{out}} \right| \tag{3}$$

For example, for C_2,

$$a_{c,2} = \left| \frac{q_{c2,2}}{q_{out}} \right| = \frac{2q_{in}}{3q_{in}} = \frac{2}{3} \tag{4}$$

Similarly, the charge multiplier coefficients can be obtained for all the power-train capacitors.

2.1.1.2 Fast Switching Limit output referred resistance:

In the fast switching limit (FSL), the output referred resistance is given by:

$$R_{FSL} = 2\sum_i R_i (a_{r,i})^2 \tag{5}$$

where R_i is the on-state resistance of resistor i. This resistor can be the on-state resistance of a switch or any parasitic resistances. Parameter $a_{r,i}$ is the charge multiplier coefficient of resistor i and has a similar definition to that of $a_{c,i}$; it can be considered simply as the

a) phase 1   b) phase 2
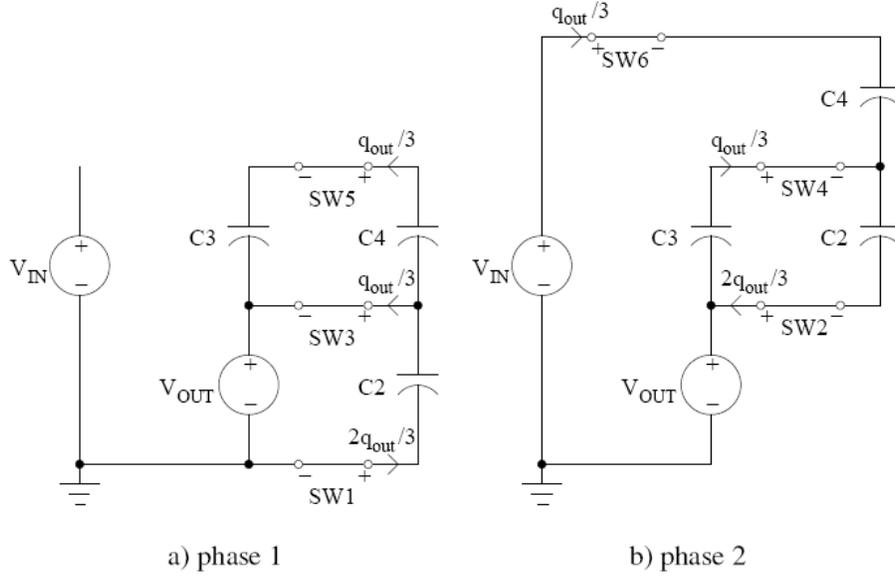
Figure 4: Switch charge flows

ratio between current flow in that resistor and the output current in steady state. Using the same example above, Figure 4 [2] shows the charge flow in each of the switches in the two clock phases. These charge flow quantities are already calculated when the charge multiplier coefficients $a_{c,i}$ are obtained for the capacitors. Using a similar approach as equation (4), the switch 5 (SW_5) charge multiplier coefficient is given by:

$$a_{r,5} = \left| \frac{a_{r5,2}}{q_{out}} \right| = \frac{q_{out}/3}{q_{out}} = \frac{1}{3} \tag{6}$$

Similarly, the charge multiplier coefficient, $a_{r,i}$, can be obtained for all resistances in the circuit.
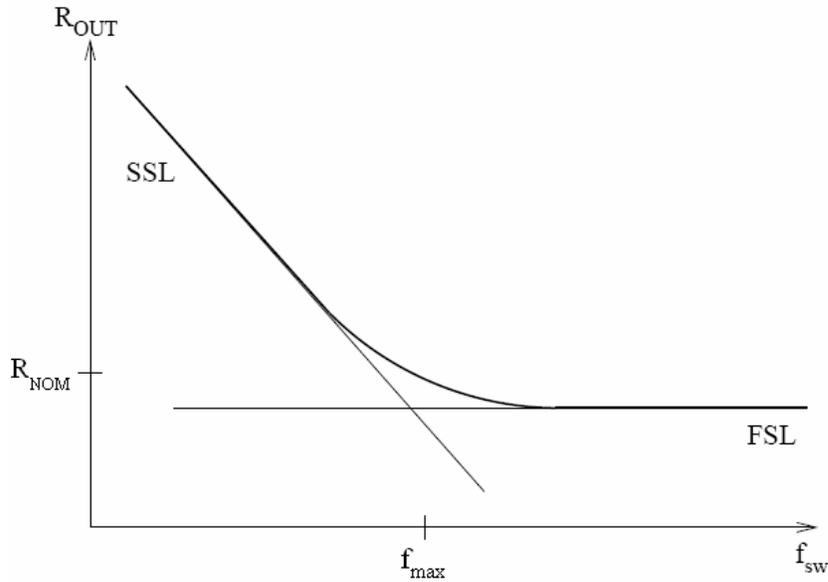
Figure 5: Output impedance vs. switching frequency

2.1.2 Optimization of SC dc-dc converters

Besides deriving the formula for the output referred resistance for SC dc-dc converters, Seeman and Sanders [1, 2] also derived the formula for optimizing the power-train capacitors and power switches. Figure 5 shows the approximated output resistance versus switching frequency given by equation (1). The design process begins with first determining the nominal output impedance R_{NOM} at a maximum load current I_{LOAD}. Factors affecting the choice of R_{NOM} may include a load regulation requirement and an efficiency requirement. One will also need to choose the maximum operating frequency f_{max} of the converter. A higher switching frequency will either reduce R_{SSL} or allow the designer to use smaller capacitors to attain the same R_{SSL}. However, a higher switching frequency will increase the losses due to charging and discharging parasitic capacitances. The designer will also need to consider device speed constraints and circuit speed constraints while choosing the operating frequency.

After determining the target R_{NOM} and f_{max}, R_{SSL} and R_{FSL} are chosen to be

$$R_{SSL} = R_{FSL} = R_{NOM} / \sqrt{2} \qquad (7)$$

at f_{max}. Since R_{SSL} and R_{FSL} depend on two separate set of parameters, the designer can then optimize the power-train capacitors and power switches separately.

2.1.2.1 Power-train Capacitor Optimization

The power-train capacitors only affect R_{SSL} but not R_{FSL}, and thus power-train capacitor sizes can be optimized using the slow switching limit equations alone. In this optimization process, the power-train capacitors are sized such that the total energy storage capability is minimized while the required R_{SSL} is satisfied at the chosen f_{max}. Seeman and Sanders [1, 2] chose to minimize energy storage capability since it is roughly proportional to physical size and device cost of capacitors. The R_{SSL} equation given by equation (2) can be rewritten as:

$$R_{SSL} = \frac{1}{2E_{tot}f_{sw}} \left(\sum |a_{c,i}v_{c,i(rated)}| \right)^2 \qquad (8)$$

where f_{sw} is the switching frequency, E_{tot} is the total energy storage capacity of all power train capacitors, $a_{c,i}$ is the charge multiplier coefficient of capacitor i, and $v_{c,i(rated)}$ is the rated voltage of capacitor i. Note that $v_{c,i(rated)}$ is defined to be the rated voltage of capacitor i but not the working voltage of capacitor i. The working voltage of a power-train capacitor is the maximum voltage on the capacitor during steady-state operation. Ideally, capacitors are chosen such that the rated voltage matches the working voltage. However, when a match is impossible, the rated voltage has to be greater than the

working voltage, and the rated voltage will be used in the calculations. Parameter f_{sw} in this calculation is the f_{max} chosen for the design, and $a_{c,i}$ can be determined using the method outlined in section 2.1.1.1.

The optimization procedure begins with using equation (8) to solve for E_{tot} with the chosen R_{SSL} and f_{sw}. Afterwards, the optimized capacitance for each power train capacitor i can be obtained by:

$$C_i = \left| \frac{a_{c,i}}{v_{c,i(rated)}} \right| \frac{2E_{tot}}{\sum_k \left| a_{c,k} v_{c,k(rated)} \right|} \tag{9}$$

2.1.2.2 Power Switch Optimization

Power switches in SC dc-dc converters only affect R_{FSL} but not R_{SSL}, and thus they can be optimized independently from the power-train capacitors. The optimization procedure [1, 2] minimizes the V-A product, or equivalently G-V^2 product, over all switches while attaining the chosen R_{FSL} value. The V-A product stands for the product of the rated voltage and current flow of MOSFET transistors; it roughly corresponds to silicon area and thus represents device cost. Ignoring all parasitic resistances in the converter, the R_{FSL} equation given by equation (5) can be written as:

$$R_{FSL} = \frac{2}{A_{tot}} \left(\sum_i \left| a_{r,i} v_{r,i(rated)} \right| \right)^2 \tag{10}$$

where A_{tot} is a parameter roughly proportional to the total silicon area usage, $a_{r,i}$ is the charge multiplier coefficient of switch i, and $v_{r,i(rated)}$ is the rated voltage of the switches. Parameter $v_{r,i(rated)}$ is defined to be the voltages in which these power transistors are

designed to operate at. Ideally, the rated voltage of transistors are equal to the maximum

voltages these transistors block in steady state; but if they are different due to process

availability, the designer should choose transistors with a rated voltage larger than the

voltage the transistors are expected to block in steady state. The optimization procedure

uses the rated voltage of the transistors instead of its blocking voltage because rated

voltage better represents the device cost. Parameter $a_{r,i}$ can be obtained in the same way

as illustrated in section 2.1.1.2.

The optimization procedure begins with using equation (10) to obtain A_{tot} for the chosen

R_{FSL}. The optimal conductance G_i of each power transistor can be obtained by:

$$G_i = \left| \frac{a_{r,i}}{v_{r,i(rated)}} \right| \frac{A_{tot}}{\sum_k \left| a_{r,k} v_{r,k(rated)} \right|} \tag{11}$$

The above optimization procedure ignores parasitic resistances in the converter. Parasitic

resistances can be incorporated into the model by first evaluating their contribution to

R_{FSL} using equation (5). The result ($R_{FSL(parasitic)}$) can then be subtracted from the R_{FSL}

obtained from equation (7). This remaining portion of R_{FSL} ($R_{FSL(switch)}$) is the quota of

R_{FSL} left for power switches. This $R_{FSL(switch)}$, together with equations (10) and (11), can

be used to calculate the optimal conductance of each power switch.

2.2 Analysis of Triple well devices

One of the main advantages of using SC converters over the buck converter is that each power switch in a SC converter needs to only block a fraction of the input voltage, thus allowing a high voltage dc-dc converter to be built in a submicron technology with native transistors. Triple well structures allow isolation of transistors into different voltage domains, so that no terminal of any transistor (except the n-well to p-subtrate junction) has overstress voltage levels, even though, each terminal is at a very high voltage relative to the substrate. The circuit described in this thesis has 5V transistors biased up to 15V, but the only junction that needs to sustain voltages higher than 3V is the n-well to p-substrate pn junction. This section investigates latch-up and voltage stress concerns with biasing triple well structures in this manner.
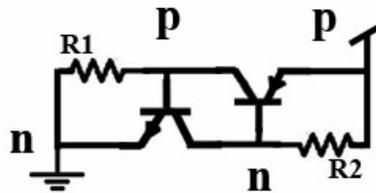
Figure 6: Thyristor structure

2.2.1 Latch-up Concerns

Figure 6 shows the thyristor structure that leads to latch-up in single n-well CMOS process. The structure is a parasitic npnp structure in which the first np pair is connected to one voltage level whereas the second np pair is connected to another voltage level. In a conventional CMOS connection, this structure exists with the 4 layers corresponding to source of NMOS (n) – substrate (p) – well of PMOS (n) – source of PMOS (p), and the two voltage levels corresponding to ground and power supply. This structure forms a positive feedback loop of gain greater than 1 if

$$\beta_{npn} * R_1 * \beta_{pnp} * R_2 > 1 \tag{12}$$

where β_{npn} and β_{pnp} are the current gain of the parasitic npn and pnp bipolar transistors respectively. If equation (12) is satisfied, the thyristor will turn on, causing huge current to flow from the power supply to ground. This is called latch-up. When latch-up occurs, the only way to stop it is to disconnect the power supply. Designers are advised to reduce the magnitude of the four terms in equation (12) such that equation (12) is never satisfied.

Triple well devices have an extra n-layer making the structure more complicated. Muth [3] considered all paths in a triple-well device, and concluded that the thyristor structure shown in figure 6 does not exist. Without the thyristor structure, triple-well devices cannot latch-up. Intuitively, one can consider the n-well as an isolating layer separating the NMOS from the PMOS, thus breaking the thyristor structure. However, if the designer merges the triple-well n-well of the NMOS with the n-well of the PMOS, then a thyristor structure will exist in a similar way as in a single well CMOS technology. This does not necessarily lead to a higher latch-up probability when compared to a single well CMOS technology, but the designer will no longer benefit from the latch-up robustness of triple-well structures.

The circuit presented in this thesis involves biasing the n-well of the NMOS and the n-well of the PMOS to a voltage much higher than the p-substrate. One can show that this biasing scheme is very similar to the conventional triple-well biasing scheme, and no thyristor structure exists. As a quick check, the p-substrate is not at the same voltage potential as any adjacent n layers. Since both of the two p layers in the thyristor structure

has an adjacent n layer at the same voltage potential, the p-substrate cannot be part of the thyristor structure. Thus the p-substrate continues to isolate the NMOS from the PMOS in this biasing scheme, making latch-up highly unlikely to occur.

2.2.2 Voltage Stress Concerns

The topology outlined in this thesis involves biasing low voltage transistors at high voltages; as a result, some junctions have to be stressed more than their design values. The gate oxide cannot be overstressed because this can easily lead to oxide breakdown. Reverse biasing the NMOS source and body pn junction is undesirable since this reduces transistor conductance due to body effect. The only junctions left are the NMOS p-body to n-well junction and the n-well to p-substrate junction. Figure 7 shows the net dopant profile of a typical triple-well NMOS device, whereas Figure 8 shows the voltage potential of the device with n-well and drain biased to 1.5V whereas all other terminals are biased at ground. One can see that the voltage potential of the portion of the p-body between the n-well and drain is raised. This indicates that the depletion region surrounding the drain has touched the depletion region surrounding the n-well; there is punch-through from the drain to the n-well through the p-body. This shows that punch-through may occur if the n-well to p-body junction is biased above its design value. On the other hand, due to the low dopant concentration in the p-substrate, only a small proportion of the depletion region occurs in the n-well; thus a punch-through in the n-well is usually not a big concern. So it is generally safe to strongly reverse bias the n-well to p-substrate pn junction; the n-well to p-body pn junction should be reverse bias, but it should not exceed its design value.
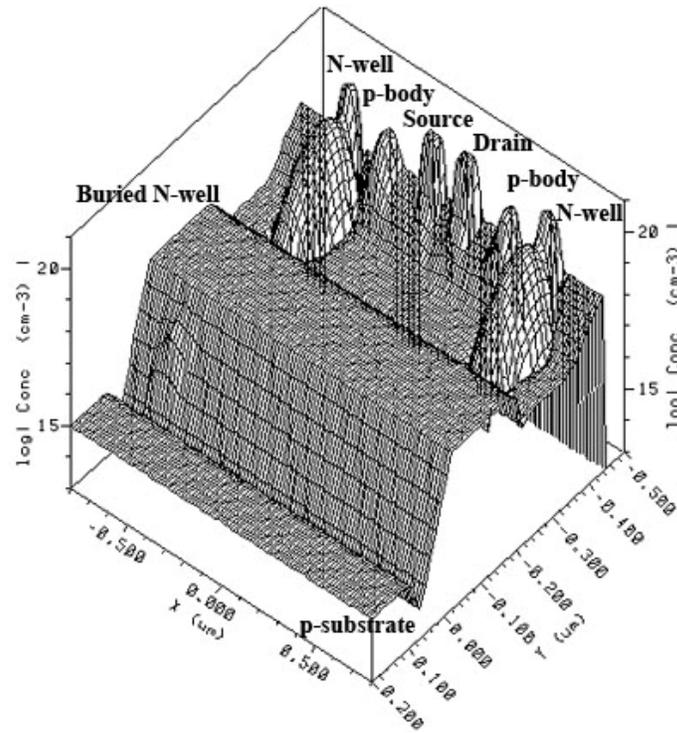
Figure 7: Net dopant concentration of a
typical Triple well NMOS
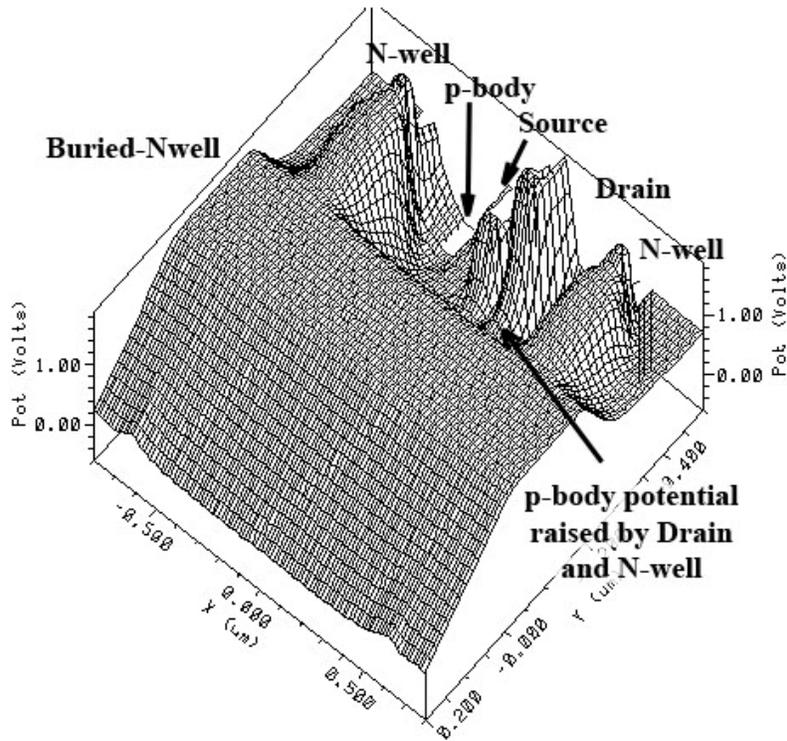
Figure 8: Voltage potential profile with N-well and Drain at
1.2V while p-body, Source and substrate at 0V

3. Architecture

3.1 Overall Architecture

Figure 9 shows the schematic of the 12V-to-1.5V Dickson converter [4]. In contrast to the original design, the circuit of Figure 9 uses MOS switches in each position, and can thus support bilateral current and power flow. Our initial interest is in its use as a step-down converter. The switches are gated in a two-phase pattern, as indicated by number in bracket next to the switch names in the figure. These two-phase clocks are non-overlapping to avoid direct current consumption. The clock generator, together with all control circuits, is powered by the output voltage of 1.5V. The clocks are level-shifted upwards by the driver blocks shown in figure 9.

Besides the seven main power-train capacitors, C_1-C_7, there are three bypass capacitors, C_8-C_{10}, shown in Figure 9. Capacitors C_8 (12V cap) and C_9 (13.5V cap) are needed to provide gate-drive charge to the top NMOS power switches. Capacitor C_{10} (1.5V right-hand-branch cap) is needed to provide 1.5V gate drive to power switch S_4 on the bottom right-hand side. All power-train capacitors and bypass capacitors are implemented with off-chip ceramic capacitors. Power-train capacitors have to be implemented off-chip due to their high value; bypass capacitors have smaller values but are nonetheless implemented off-chip to save die area. NMOS transistors are used throughout the power-train to minimize transistor area and gate charge. There may be strategic opportunities for swapping in PMOS devices in a few locations, and in turn obviating the need for some of the bypass capacitors, though this has not been done here.
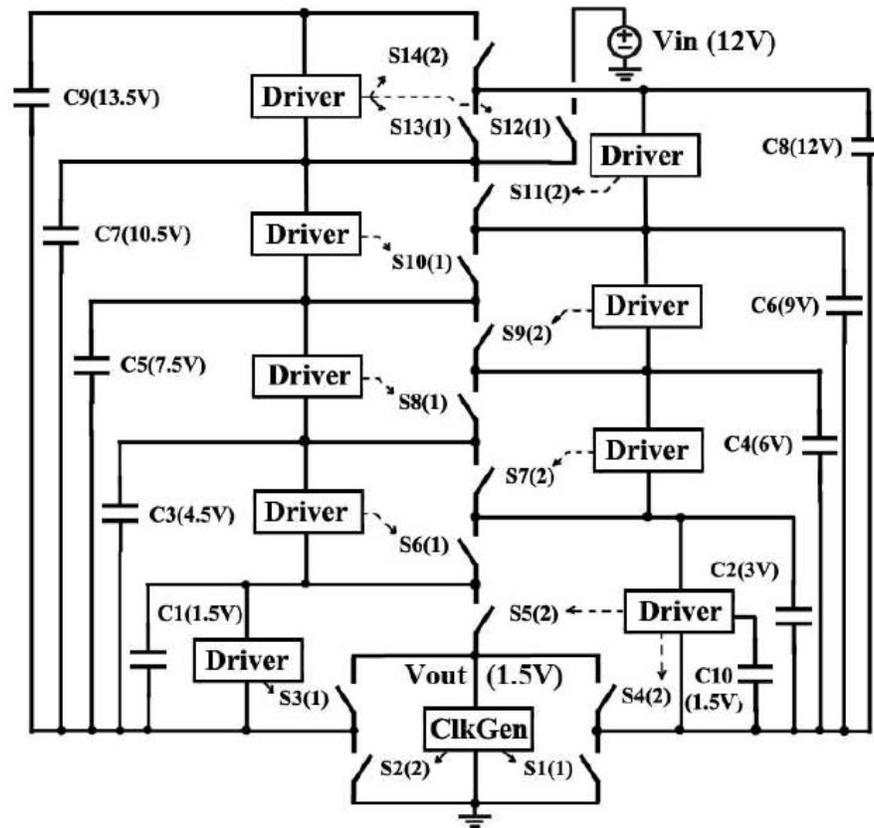
Figure 9. Overall Circuit of the 12V-to-1.5V step down Dickson converter. The numbers in bracket of the switches indicate their respective clock phases. The dotted arrows show the respective driver block that drives each powertrain switch

A switching frequency of 1 MHz is selected based upon practical capacitor choices. Although the silicon can easily support a higher frequency, load-independent gating and parasitic dynamic losses scale up with increasing frequency, while the effective discrete capacitor impedance ceases to decrease in the range of 1-10 MHz due to the equivalent series resistance (ESR) of standard ceramic capacitors. Thus, there is no substantial value in operating at higher frequency unless the capacitors could be integrated on chip, or radically reduced in physical size. However, the discrete parts selected here are already in tiny 0603 packages, and by simple scaling from 1 MHz to 100 MHz, the multiple capacitors in the range of 1 uF would scale to the range of 10 nF, still impractical for on-

chip integration. Thus, 1 MHz provides an "easy" operating frequency at which gate drive losses are relatively low, and are about 1 mW.

3.2 Device Choice and Biasing

The power switches in the Dickson converter block two different voltages. Referring to Figure 9, the bottom 4 switches (S_1-S_4) only need to block a voltage of 1.5V whereas the other switches (S_5-S_{12}) need to block 3V. S_{13} and S_{14} block 3V as well but they are not part of the power-train. With the availability of 5V transistors in our 0.18μm process, the 1.5V switches are implemented with native 0.18μm 1.8V NMOS transistors and the 3V switches are implemented with 0.6μm 5V transistors. Cascoding two 1.8V switches to block 3V was not implemented due to complexity of implementation, even though, using 5V transistors to block 3V is a slightly inefficient usage of these higher voltage transistors. All power switches are implemented with NMOS devices for highest mobility, with each p-body isolated in a triple-well nwell. Each power device has its p-body shorted to its source to eliminate body effect.

Each power switch is driven by its respective driver block, as indicated by the dotted arrows in Figure 9. Each driver block is referenced to the source of the power switch that it drives. As such, each driver block is locally powered from two of the power-train capacitors, as indicated in the figure. Isolation of NMOS devices is again achieved with utilization of the triple-well structure as needed. This isolation ensures that no terminal of any transistor within each voltage domain has overstress voltage level, even though each terminal itself may be as high as 15V above the substrate voltage level. The triple-well

nwells of the isolated NMOS in each voltage domain are tied together and connected to the respective p-body with rare exceptions. The nwell is connected this way because intermediate fixed voltage levels are not readily available. This connection scheme reduces the p-body to deep Nwell voltage stress and also makes the layout simpler than an arrangement in which the deep Nwell is biased at a higher fixed potential. The only junctions that need to sustain voltages higher than 3V are the isolated NMOS deep Nwell to p-substrate pn junctions and the PMOS nwell to p-substrate pn junctions. These blocking voltage requirements are easily achieved with the low substrate dopant levels and reasonable substrate thickness in most bulk CMOS technologies.

As previously discussed in section 2.2, one major concern of this biasing scheme is latchup possibility. There are numerous pn junctions in this design and they are all biased at different voltage levels. To make things worse, these voltage levels are time-varying with respect to each other due to the switching activity of the converter. This will inject carriers by capacitive coupling into the substrate and wells, which have low dopant levels and high resistivity. Fortunately, this latchup concern is greatly mitigated by the mere fact that triple well structures are extremely robust to latchup [3]. To further improve latchup immunity, PMOS nwells are never merged with isolated NMOS nwells, and substrate contact rings are placed to separate each voltage domain.

3.3 Topology Choices

Figure 10 [2] shows the five popular topologies compared and contrasted in [2]. Among these five choices, the Dickson and Ladder circuits are best suited to CMOS integration

a) Ladder

b) Dickson Charge Pump

c) Fibonacci

d) Series-Parallel

e) Doubler
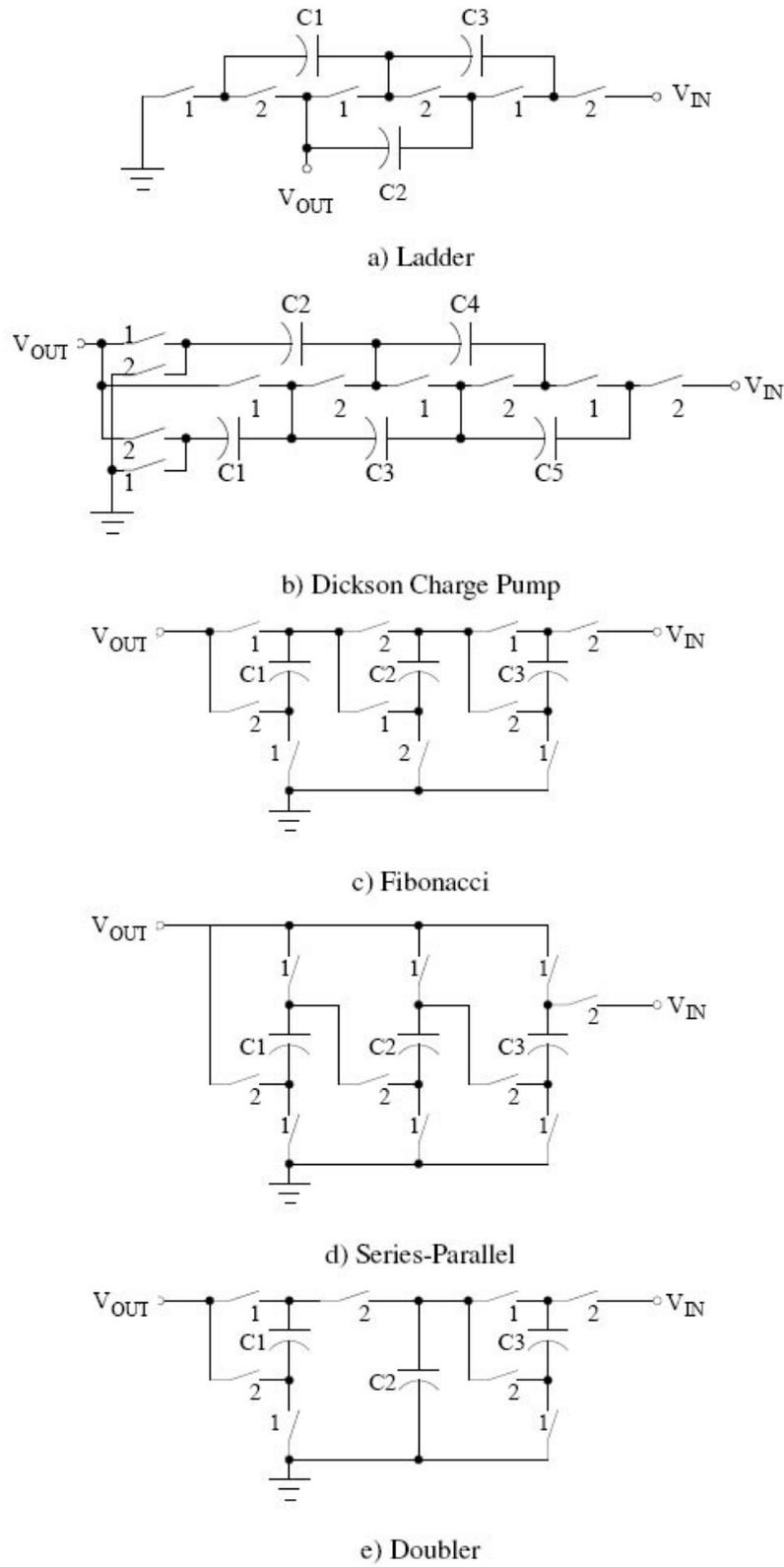
Figure 10: Five common switched-capacitor converter topologies

since the switches in these circuits each block a fraction of the input source voltage. Further, the required voltage ratings are uniform at one or two levels for these candidate topologies. Additionally, the regular structure of these circuits facilitates a relatively simple gate-drive level shifting scheme. Significantly, the Ladder and Dickson circuits also make optimal use of the available silicon in terms of power output per total silicon area, as discussed in [2]. The Dickson circuit has been selected over the Ladder circuit since it requires roughly one-half the number of capacitors for a given application. In the case of a multi-watt application, it is not feasible to realize the capacitors on-chip, and thus, the pin and external component count is minimized with this choice.

The power-train capacitors in a Dickson topology can be implemented in two different fashions as shown in figure 11. Both topologies give the same power switch constraints, but one requires high voltage capacitors while the other only requires low voltage capacitors. Since all power-train capacitors are implemented with discrete off-chip ceramic capacitors, both topologies are practical. The optimization method outlined in section 2.1.2 gives different capacitor values for these two topologies, but the resulting capacitor energy storage capability is the same. Since the optimization method assumes that capacitor cost is directly proportional to energy storage capability, these two topologies should be equivalent to one another. However, ceramic capacitors have a much higher energy density at high voltage ratings, thus the assumption no longer holds and a high voltage capacitor version should be used.
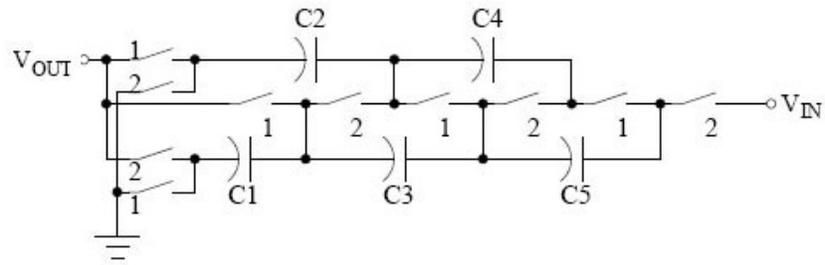
a) low voltage capacitor version
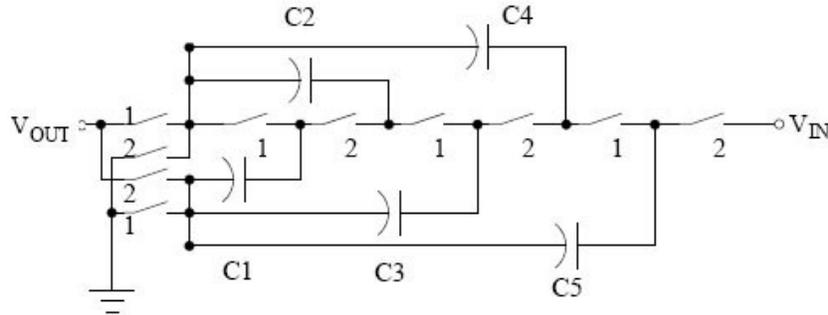
b) high voltage capacitor version

Figure 11: Equivalent Circuits of Dickson SC converter
for different capacitor voltages

3.4 Transistor and Capacitor sizing

After the system architecture is determined, the next step is to optimally size the switches

and capacitors to achieve the target efficiency and power ratings. Based on the theory

outlined in section 2.1, the optimization steps are shown in the following subsections.

The optimization procedure below aims to produce a converter that can achieve 90%

efficiency at 1A output load conditions and at 1MHz switching frequency. The resulting

target output resistance at 1MHz is 150mΩ.

3.4.1 Capacitor Optimization

Using the methods outlined in section 2.1.1.1 and section 2.1.2.1, the capacitor charge multiplier coefficient, $a_{c,i}$, and the capacitor working voltage, $v_{c,i(working)}$, are respectively given by:

$$\begin{bmatrix} a_{c,1} & a_{c,2} \ldots a_{c,6} & a_{c,7} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{8} & \dfrac{1}{8} \ldots \dfrac{1}{8} & \dfrac{1}{8} \end{bmatrix} \tag{13}$$

$$\begin{bmatrix} v_{c,1(working)} \ldots v_{c,7(working)} \end{bmatrix} = \begin{bmatrix} 1.5 & 3 & 4.5 & 6 & 7.5 & 9 & 10.5 \end{bmatrix} \tag{14}$$

Setting f_{sw} = 1MHz and R_{SSL} = 150mΩ $/ \sqrt{2}$ = 106mΩ, the optimized capacitor values are given by:

$$\begin{bmatrix} c_1 \ldots c_7 \end{bmatrix} = \begin{bmatrix} 4.1\mu F & 2.1\mu F & 1.3\mu F & 1.0\mu F & 0.82\mu F & 0.69\mu F & 0.59\mu F \end{bmatrix} \tag{15}$$

However, the optimization procedure outlined in section 2.1.2.1 uses capacitor rated voltage, $v_{c,i(rated)}$, instead of capacitor working voltages. Using the rated voltages of available ceramic capacitors, $v_{c,i(rated)}$ are given by:

$$\begin{bmatrix} v_{c,1(rated)} \ldots v_{c,7(rated)} \end{bmatrix} = \begin{bmatrix} 4 & 4 & 6.3 & 6.3 & 10 & 10 & 16 \end{bmatrix} \tag{16}$$

and the optimized capacitor values are given by:

$$\begin{bmatrix} c_1 \ldots c_7 \end{bmatrix} = \begin{bmatrix} 2.1\mu F & 2.1\mu F & 1.3\mu F & 1.3\mu F & 0.83\mu F & 0.83\mu F & 0.52\mu F \end{bmatrix} \tag{17}$$

Since discrete capacitors cannot be of arbitrary value, the actual capacitor sizes used in this design are given by:

$$\begin{bmatrix} c_1 \ldots c_7 \end{bmatrix} = \begin{bmatrix} 2.2\mu F & 2.2\mu F & 1\mu F & 1\mu F & 0.68\mu F & 0.68\mu F & 0.47\mu F \end{bmatrix} \tag{18}$$

This result is summarized in Table I. The first column of Table I shows the ideal capacitor values given by equation (15), whereas the second column of Table I shows the actual capacitor values used given by equation (18). Table I also shows the value of the

helper capacitors, C_8 - C_{10}, used in this design. Capacitor values for C_8 - C_{10} are chosen arbitrarily based on the smallest available ceramic capacitor sizes.

3.4.2 Switch Optimization

Using the methods outlined in section 2.1.1.2 and section 2.1.2.2, the switch charge multiplier coefficient, $a_{r,i}$, and the switch blocking voltage, $v_{r,i(blocking)}$, are respectively given by:

$$\left[a_{r,1}...a_{r,4} \quad a_{r,5}...a_{r,12}\right] = \left[\frac{1}{2}...\frac{1}{2} \quad \frac{1}{8}...\frac{1}{8}\right] \tag{19}$$

$$\left[v_{r,1(blocking)}...v_{r,4(blocking)} \quad v_{r,5(blocking)}...v_{r,12(blocking)}\right] = \left[1.5\cdots1.5 \quad 3\cdots3\right] \tag{20}$$

However, the optimization procedure outlined in section 2.1.2.2 uses switch rated voltages, $v_{r,i(rated)}$, instead of switch blocking voltages. Since only 0.18μm 1.8V transistor and 0.6μm 5V transistor are available in this technology, the switch rated voltages, $v_{r,i(rated)}$, are given by:

$$\left[v_{r,1(rated)}...v_{r,4(rated)} \quad v_{r,5(rated)}...v_{r,12(rated)}\right] = \left[1.8\cdots1.8 \quad 5\cdots5\right] \tag{21}$$

Setting $R_{FSL} = 150\text{m}\Omega / \sqrt{2} = 106\text{m}\Omega$, the optimized switch resistances are given by:

$$\left[r_{s1}...r_{s4} \quad r_{s5}...r_{s12}\right] = \left[14m\Omega\cdots14m\Omega \quad 240m\Omega\cdots240m\Omega\right] \tag{22}$$

This corresponds to the following transistor widths:

$$\left[S_1...S_4 \quad S_5...S_{12}\right] = \left[25.4mm\cdots25.4mm \quad 9.4mm\cdots9.4mm\right] \tag{23}$$

The above analysis ignores parasitic resistances, which are actually the dominating resistances in this design. With each bondwire having a resistance of about 250mΩ, the contribution of bondwire resistances to R_{FSL} is 160mΩ, even though there are multiple bondwires per transistor terminal as described in section 5. Bondwire resistance alone has

exceeded the required R_{FSL}, making it impossible to satisfy the required R_{FSL} even if the power-switches have zero resistance. The final design uses transistors far wider than the value given in equation (22). The limitations of bondwire resistances can be overcome by using solder bump interconnect in future works.

Table I summarizes the optimization results and the design values outlined in this section. Column 1 of Table I shows the ideal transistor value as given by equations (22) and (23), whereas column 2 of Table I shows the actual transistor values used in this design. Column 2 of Table I also shows the estimated effects on R_{FSL} of bondwire resistances, on-chip metal resistances, test socket resistance, capacitor R_{ESR}, and switch resistances. The second last row of Table I shows the estimated R_{OUT} in both the ideal calculation and the actual design. The last row of Table I also shows the estimated frequency-dependent switch loss due to the power consumed by driving the power switches.

TABLE I
SIZES OF CAPACITORS AND POWER SWITCHES

	ideal value	design value
1.5V cap	$4.1\mu F$	$2.2\mu F$
3V cap	$2.1\mu F$	$2.2\mu F$
4.5V cap	$1.3\mu F$	$1\mu F$
6V cap	$1.0\mu F$	$1\mu F$
7.5V cap	$0.82\mu F$	$0.68\mu F$
9V cap	$0.69\mu F$	$0.68\mu F$
10.5V cap	$0.59\mu F$	$0.47\mu F$
1.5V helper cap		$2.2\mu F$
12V helper cap		$0.47\mu F$
13.5V helper cap		$0.47\mu F$
12V input cap		$0.47\mu F$
1.5V output cap		$24\mu F$
R_{SSL}@1MHz	$106m\Omega$	$125m\Omega$
3V switch width	$9.4mm$	$16mm$
3V switch resistance	$238m\Omega$	$140m\Omega$
1.5V switch width	$25mm$	$75mm$
1.5V switch resistance	$14m\Omega$	$5m\Omega$
Contribution to R_{FSL}		
all switches	$106m\Omega$	$51m\Omega$
onchip metal resistance		$39m\Omega$
capacitor R_{ESR}		$15m\Omega$
bondwire resistance		$160m\Omega$
test socket resistance		$65m\Omega$
R_{FSL}	$106m\Omega$	$330m\Omega$
R_{out}@1MHz	$150m\Omega$	$353m\Omega$
Freq-dep switch loss	0	1mW

4. Circuit Design

4.1 Driver block circuit

Figure 12 shows the details of the driver blocks shown in Figure 9. The main functions of these driver blocks are to serve as gate drivers, and to shift the clock signal upward across adjacent voltage domains. The buffer and level-shifter [5] fulfill these two respective functions. The Schmitt Trigger and delay line is used to speed up the clock edge and approximately line up the clock edges for multiple power switches. Regeneration of the clock edge is necessary because the level-shifter is a slow circuit and has a slow output signal edge. A slow clock edge could cause significant power loss due to short circuit current in the large buffer. The delay line offsets the skew of the clock signal due to the delay of the level-shifters, so that the clock is re-aligned at its respective power switch gate. Clock skew at the gates of the power switches would increase the required dead-time between the two non-overlapping phase clocks, which would in turn reduce the duty cycle and also limit the maximum clock frequency. A 50% duty cycle is desirable for switched-capacitor circuit operation to allow maximum time for all voltages to settle in each phase.

4.2 Clock Generation Circuit

Figure 13 shows the detail of the clock generator block. This clock generator takes in an off chip clock signal and generates a non-overlapping clock with dead-time controlled by an off-chip tunable resistor. By tuning the off-chip resistor from 1kΩ to 1MΩ, a dead-time from 1ns to 1μs can be attained. A tunable dead-time is necessary because the delay of the level-shifter circuit shown in figure 12 is strongly dependent on voltage variations,
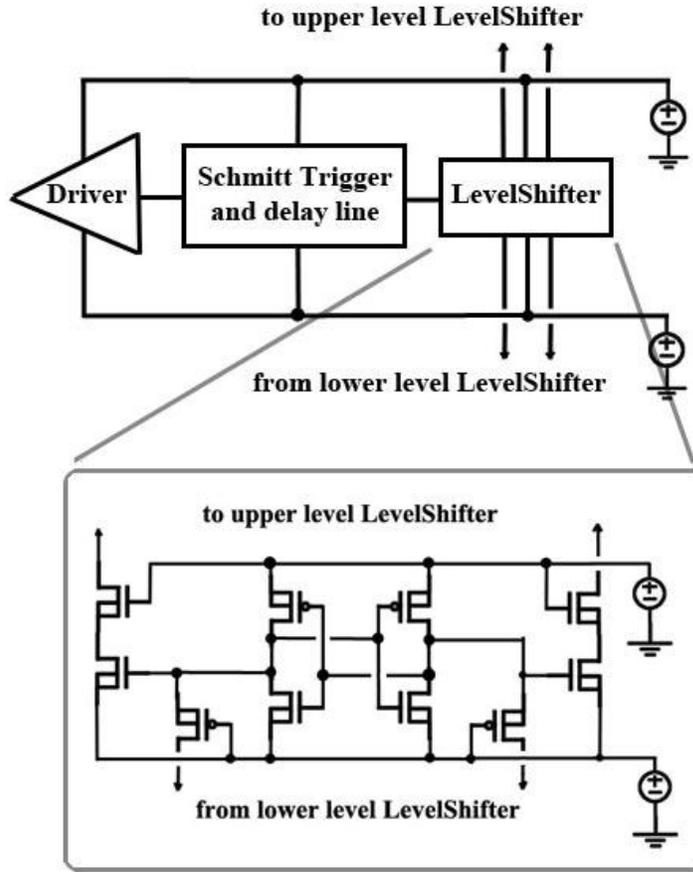
Figure 12: Details of the driver block in figure 9

process variations and temperature, and it is very challenging to set a dead-time at design time that will guarantee a non-overlapping gate drive in all conditions. A non-overlapping gate drive is very important not only because short circuit current through the power transistor reduces efficiency, but because this can significantly distort the steady state power-train capacitor voltages and lead to malfunctioning of level-shifters.

4.3 Helper Rail Implementation

As mentioned in section 3.1, bypass capacitors C_8 to C_{10} are included to provide gate drive to power switches. Capacitors C_8 and C_9 are implemented similar to the power-train capacitors, $C_1 - C_7$, as shown in figure 9. Implementation of C_{10} is shown in figure 14.
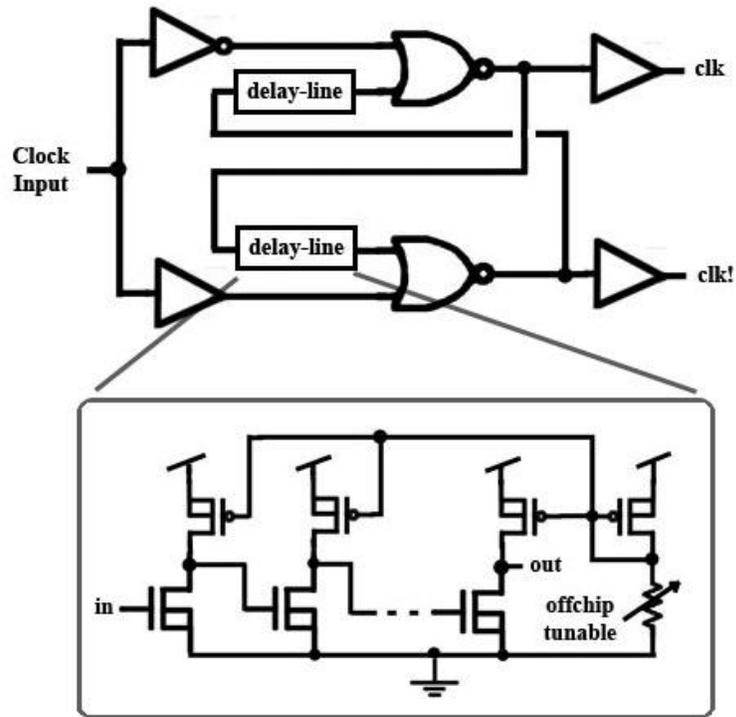
Figure 13: Details of the clock generator

During phase 1 of the clock, C_{10} is charged to 1.5V by the output terminal; while during phase 2 of the clock, C_{10} provides gate drive charge to transistor S_4. This process is achieved by having 3 additional transistors and using the control signal from the driver block as shown.
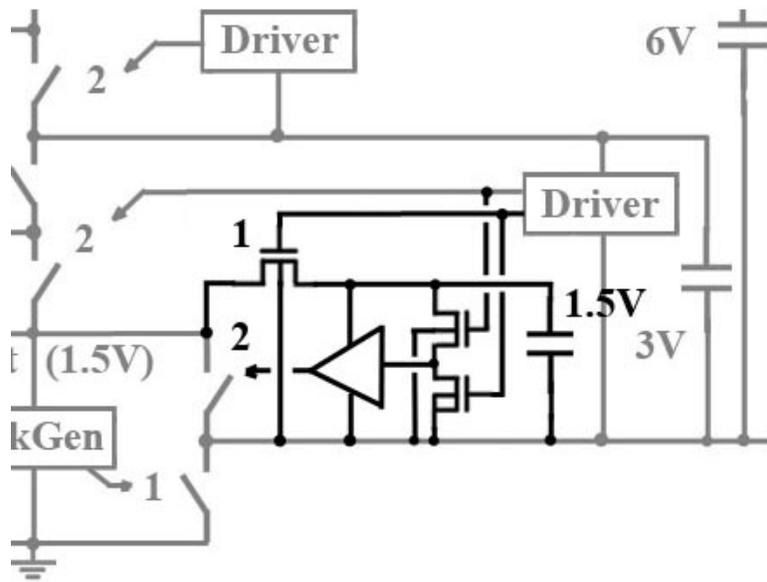
Figure 14: Implementation of C10 helper rail. The bottom right part of figure 9 is included as a background

5. Layout

Figure 15 shows the die photo of the circuit. As evident from the photo, all power switches are located at the periphery of the die to minimize the on-chip metal resistances. The buffers driving these power switches are placed next to the power switches, but are not easily distinguishable in the case of the 1.5V switches. All the other circuits are placed in the small block in the middle of the die. Bond pads are designed to allow double bonding of 1mil gold wire on each pad to reduce bond-wire resistances and inductances.

Due to the large current multipler coefficient $a_{r,i}$ of the 1.5V switches, series parasitic resistances at the 1.5V switches terminals have a substantial impact on the overall R_{FSL}. In order to further reduce the series parasitic resistance of the 1.5V switches, 5 bond pads are placed in parallel for each 1.5V switch terminal. This results in the slender aspect ratio of the 1.5V switches as shown in Figure 15. All of these factors make the active circuitry concentrate at the periphery of the die and leave the middle portion empty. Decoupling capacitors are added in this empty space to reduce the effect of parasitic inductances of the bond-wires, which can cause serious ringing as shown in figure 16 in section 6. There are about 200pF of decoupling capacitors across each of the 3V power domains, and about 1nF of decoupling capacitors across each of the 1.5V power domains. However, even including the decoupling capacitors, 55% of the die is still empty. Table II shows the layout area of the various components of the circuit.
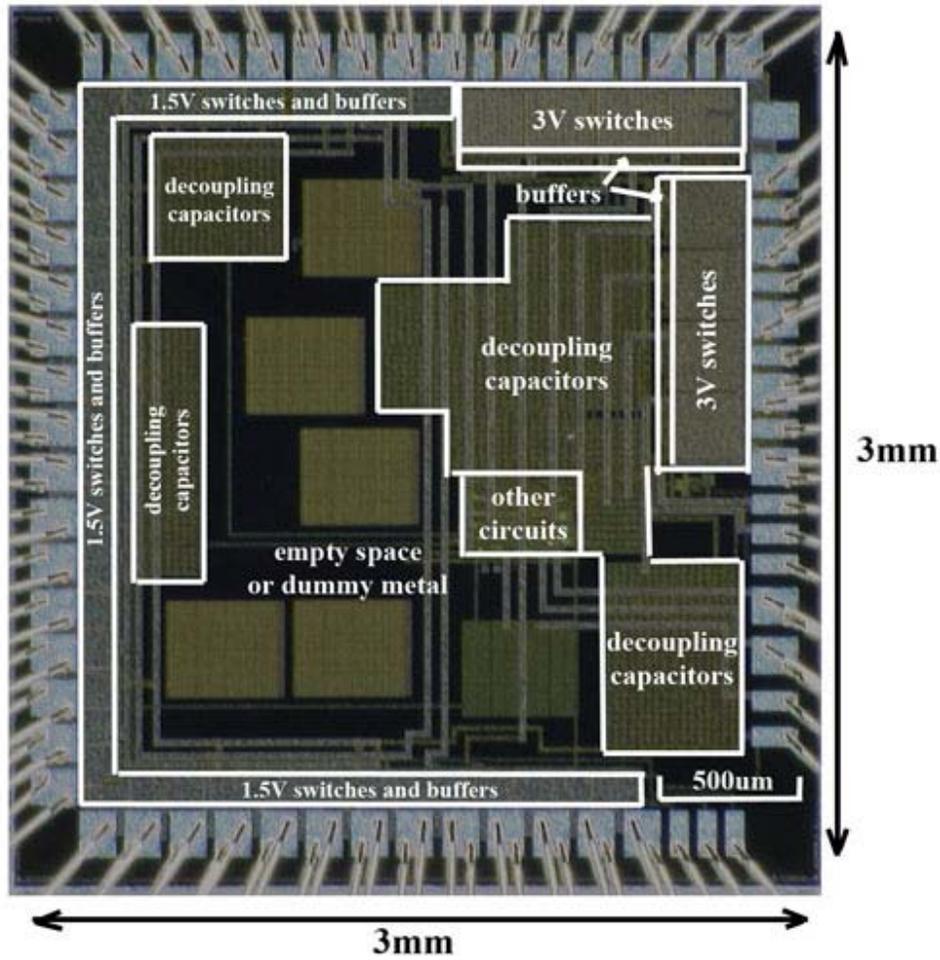
Figure 15: The die photo of the layout of the fabricated circuit

TABLE II
AREA OF DIFFERENT COMPONENTS IN DIE LAYOUT

	area in layout
3V switches	$0.57mm^2$
3V switch buffers	$0.1mm^2$
1.5V switches	$0.5mm^2$
1.5V switch buffers	$0.06mm^2$
Other circuits	$0.13mm^2$
decoupling capacitors	$1.56mm^2$
Total active area	**3mm^2**
Total area excluding pads	$6.7mm^2$
Total area including pads	**9mm^2**

6. Experimental Results

Figure 16 shows the waveform of the output voltage rail at 1A load current at the nominal switching frequency of 1MHz. This waveform shows a 100mV peak to peak ripple voltage due to the relatively low output capacitance of 24µF. The bottom two waveforms shown in figure 16 are gate drive waveforms at the bottom two (ground referenced) power switches, illustrating the non-overlapping clock signals. The ringing on these two gate drive signals is due to parasitic inductances of bondwires.

Figure 17 shows measured and theoretical output resistance R_{OUT} of the converter at a range of switching frequencies. The solid curve shows the theoretical value expected by using the calculations and values reported in sections 3.4, whereas the dots are the experimental results obtained at a range of load current levels for each frequency. One can see that the circuit behaves very similarly to the theoretical calculation results.

Figure 18 shows the efficiency of this converter versus load current at 1MHz switching frequency. Again, the solid curve shows the theoretical value whereas the dots show the experimental results. The theoretical efficiency curve includes two loss components: load-independent switching loss (about 1 mW) and a load-dependent loss reflecting the finite output resistance. The experimental data matches very well with the theoretical curve. It shows a peak efficiency of 98% at 50mA load and a maximum possible load of about 1.5A. Significantly, the efficiency remains at 90% or higher for the load range from 6 mA to 400 mA without need for any mode or switching frequency adjustments. The efficiency at low load condition can be further increased by reducing the switching

frequency of the circuit since most fixed loss arises from the switching action of the converter.
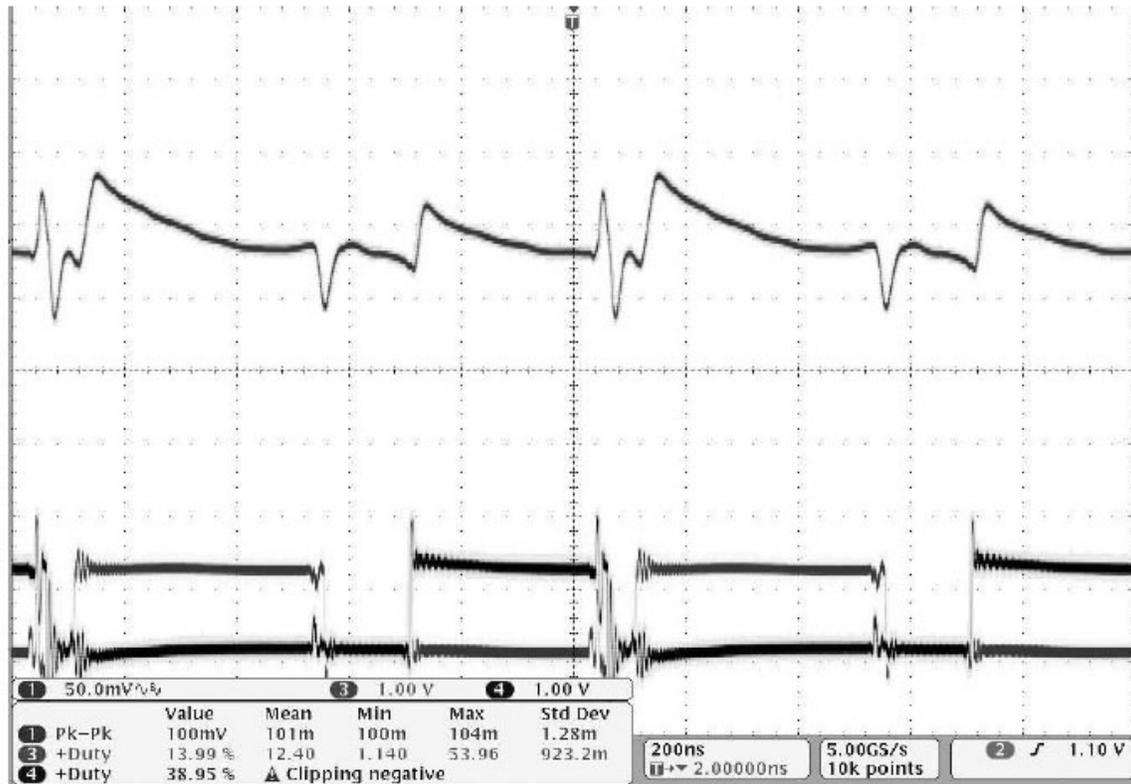

Figure 16. The output waveforms at 1A load current and 1MHz switching frequency. The top curve shows the output voltage and the two bottom curves shows the two phase non-overlapping clock. The vertical scale is 50mV per interval and the horizontal scale is 200ns per interval
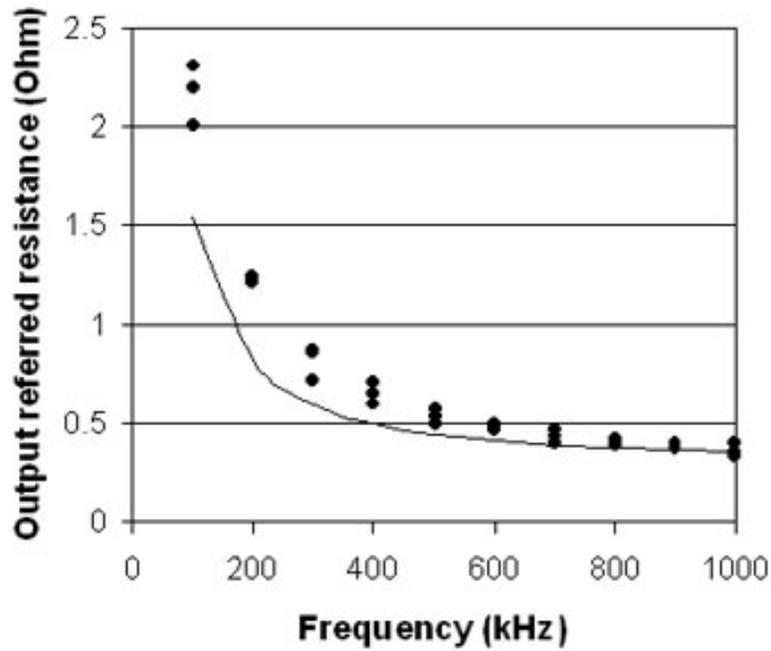
Figure 17: The measured and theoretical output referred resistance *Rout* at different switching frequencies
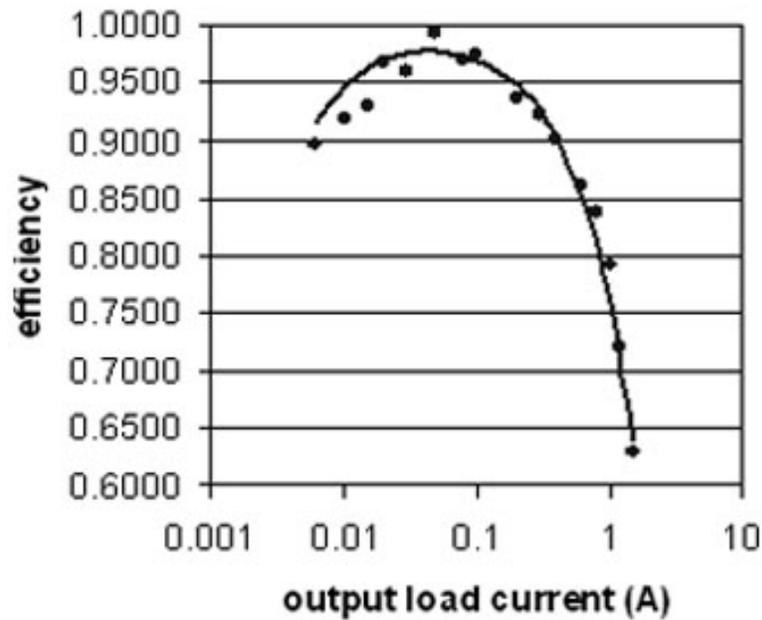
Figure 18: The theoretical and experimental efficiency of the circuit vesus load current at the nominal switching frequency of 1MHz

7. Discussion

This thesis has proved the feasibility of realizing a moderate-voltage switched-capacitor dc-dc converter in a 0.18μm technology. However, the data suggests that the circuit has yet to fully reveal the full potential of this circuit strategy. As evident from Table I, the dominating factors of R_{FSL} is bondwire resistance followed by socket resistance, instead of the MOSFET triode region resistance. These dominant loss contributors can be reduced by using solder bump pads to eliminate bondwires and other interconnect pathways to the printed circuit board. Future use of this option not only allows the designer to potentially reduce R_{FSL} by 66%, but also to get rid of all the bondpads and place some of the power transistors in the center of the die. This would reduce the die area from 9mm^2 to 3mm^2, or would allow for a design with larger transistors supporting a much higher output current. Further, solder bump interconnect offers the promise of reduced parasitic inductance, enabling more effective off-chip bypassing. The latter consideration could potentially allow for further die area reduction by elimination of on-chip bypass capacitance.

8. Conclusion

This thesis presents the design and measured performance of a 12V-to-1.5V switched capacitor dc-dc converter realized in a 0.18μm technology. This circuit shows a peak efficiency of 98% at 50mA load and a maximum load of about 1.5A. Significantly, the efficiency remains at 90% or higher for the load range from 6 mA to 400 mA without need for any mode or switching frequency adjustments. The active die area is 3mm^2 in a 0.18μm technology.

This thesis shows that highly efficient moderate voltage level conversion is realizable in low voltage technology by using triple-well isolation to separate the circuits into various voltage domains, each of which supports voltages that are only a fraction of the total voltage incident on the die. The circuit strategy allows potential integration of the dc-dc conversion function with the main function circuit core, and further allows use of silicon area more efficiently when compared to the traditional buck converter.

Acknowledgment

References

[1] Michael D. Seeman and Seth R. Sanders, "Analysis and Optimization of Switched-Capacitor dc-dc converter", *IEEE COMPEL workshop*, pp 216-224, July 2006

[2] Michael D. Seeman, "Analytical and Practical Analysis of Switched-Capacitor DC-DC Converters", *master thesis*, University of California, Berkeley, May 19, 2006

[3] Werner Muth, "Matrix Method for Latch-up Free Demonstration in a Triple-Well Bulk-Silicon Technology", *IEEE transaction on Nuclear Science*, vol 9, issue 3, part 1-2, pp 296-400, June 1992

[4] J.F. Dickson, "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol 11, pp 376-378, June 1976

[5] S Rajapandian, K shepard, P Hazucha, et al., "High-tesion power delivery: operating 0.18um CMOS digital logic at 5.4V", *Solid State circuit conference*, vol 1, pp 298-299, Feb 2005.

[6] M.S. Makowski and D. Maksimovic. *Performance Limits of Switched-Capacitor DC-DC Converters*. Power Electronics Specialists Conference, June 18-22 1995, pp 1215-1221

[7] L. Chua, C. Desoer, and E. Kuh. Linear and Nonlinear Circuits. McGraw Hill, New York, 1987