Digitally Calibrated Analog-to-Digital Converters in Deep Sub-micron CMOS

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by

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Chair Date

Date

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University of California, Berkeley

Spring 2008

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Abstract

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Professor Borivoje Nikolić , Chair

We present and implement an adaptive digital technique to calibrate pipelined analog-to-digital converters (ADCs). Rather than achieving linearity by adjustment of analog component values, the new approach infers component errors from conversion results and applies digital postprocessing to correct those results. The scheme proposed here draws close analogy to the channel equalization problem commonly encountered in digital communications. We show that, with the help of a slow but accurate ADC, the proposed code-domain adaptive digital filter is sufficient to remove the effects of component errors including capacitor mismatch, signal-dependent finite op-amp gain, op-amp offset, and sampling-switch-induced offset. The algorithm is all digital, fully adaptive, data-driven, and operates in the background. Strong tradeoffs between accuracy and speed of pipelined ADCs are greatly relaxed in this approach with the aid of digital correction techniques. Analog precision problems are translated into the complexity of digital signal-processing circuits, allowing this approach to

benefit from CMOS device scaling in contrast to most conventional correction techniques.

To demonstrate the idea, a prototype has been designed and fabricated in 0.13μm with 1.35V power supply. The system mainly consists of a pipelined ADC, a reference ADC, and an adaptive digital filter in FPGA. The measured results show that the SNR improves from 28.1dB before calibration to 59.4dB after calibration at 100MS/s with a 411kHz. The SFDR improves from 29.8dB to 67.8dB. The total power consumption of the chip is 448mW and the estimated power consumption of the adaptive digital filter is 7mW at 100MHz.

Professor Borivoje Nikolić
Dissertation Committee Chair

To my parents

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Chapter 1

Introduction

1.1 Motivation

With the advent of high performance digital signal processing systems, there is a constant increase in demand for high-resolution, high-speed analog-to-digital converters (ADCs). Besides resolution and speed, power consumption is another key metric in ADC design, especially in mobile applications. Pipelined analog-to-digital converter architecture provides a mean to achieve high-speed and high-precision simultaneously; however, high throughput and high resolution must be realized simultaneously [1]. The 1.5-b/stage architecture [2, 3] is widely used due to its low per stage complexity, large feedback factor for its residue amplifier and tolerance to comparator offset. Prominent analog impairments for ADCs include sampling capacitor mismatch, finite op-amp gain and switch charge injection errors [1–5]. As we are moving towards system-on-a-chip solution, ADCs have to be integrated on a single chip with digital circuits in deep sub-micron CMOS technology. Deep sub-micron CMOS technology poses immense challenge in ADCs design. First, the supply

voltage is reduced. This results in reduction in signal swing and thus SNR. Low supply voltage also causes problem in designing high-gain amplifiers because there are small voltage headroom to cascode transistors. In addition, the intrinsic gain of transistor is reduced with scaling. Furthermore, there are no good matched capacitors in scaled digital CMOS as compared to dedicated analog process. A promising ADC architecture in scaled CMOS should be able to utilize faster transistors and abundant digital gates available in CMOS technology to mitigate errors from analog components and to improve ADC performance. In the past, numerous background calibration techniques [6–12] have been proposed to correct errors in pipelined ADCs.

1.2 State-of-the-Art Calibrated ADCs

Calibration in ADCs is to measure errors introduced by analog circuit impairments and errors are compensated in either analog or digital domain. Background calibration performs the measurement and compensation without interrupting the normal operation of ADCs. Some existing background calibration algorithms are skip-and-fill [6, 7], using an extra pipeline stage [8], reference ADC to correct residue error [9], digital calibration with a slow-but-accurate ADC [10], adjusting reference voltages [11], and pseudo random number dithering method [12]. The algorithm used in [6, 7] is based on the concept of skipping conversion cycles randomly but filling in the data later by nonlinear interpolation. In [8], the calibration is done by employing an extra stage that is calibrated outside of the main converter's operation and periodically substituted for a stage within the main converter. [9] uses a slow-but-accurate ADC to correct the pipelined stage residue voltage

error. [10] utilizes a slow calibrated algorithmic ADC to calibrate the linear gain error in the multiplying-DAC in the pipelined ADC. In [11], non-linearity caused by inter-stage gain error is compensated by adjusting the reference voltages of calibrated stages during the normal operation of the ADC. [12] relies on applying pseudo random number in the DAC to measure the gain error in the residue amplifier and then compensate the error in digital domain.

We propose a complete digital background calibration technique to achieve high conversion rate and high speed simultaneously without the need of both high-throughput and high-precision analog components. The proposed technique utilizes digital post-processing without tempering with the analog path. It is widely known that accuracy and speed of pipelined ADCs are limited by residue amplifiers. Since the calibration can correct for analog impairments such as analog component mismatch, signal-dependent amplifier finite-gain error, and switch charge injection, the residue amplifiers can be optimized for speed and power only by relaxing the gain requirement. Therefore, the proposed correction technique can be utilized to improve the effective conversion accuracy and conversion speed, and/or to reduce power consumption. Furthermore, the calibration runs in the background so that after the initial acquisition, the calibration algorithm can track temperature drift, supply variation, and device aging. Finally, the calibration is fully digital post-processing; it does not involve any altering of the analog path. Analog precision problems are translated into the complexity of digital signal-processing circuits, allowing this approach to benefit from CMOS device scaling in contrast to most conventional correction techniques.

1.3 Thesis Organization

The proposed background calibration algorithm is discussed in detail in Chapter 2. Then, high-resolution ADC techniques are reviewed in Chapter 3. Chapter 4 focuses on the design of sigma-delta ($\Sigma\Delta$) ADC as a reference ADC for the proposed ADC architecture; Chapter 5 presents the circuit design of the sigma-delta ADC. Chapter 6 gives an overview of the dedicated sample-and-hold amplifier (SHA) for $\Sigma\Delta$ ADC, while Chapter 7 presents the pipelined ADC design. Clock generation circuit is shown in Chapter 8. Layout, floor planning, and full-chip integration issues, are discussed in Chapter 9. Chapter 10 discusses the design and optimization of the least-mean-square (LMS) adaptive digital filter (ADF). Finally, measured results are presented in Chapter 11, and the conclusion is presented at the end.

Chapter 2

Fully Digital Background Calibration of Pipelined ADCs

2.1 Introduction

Resolution of pipelined ADCs is limited by the accuracy of the DACs they employ. Traditionally, uncalibrated and untrimmed pipelined ADCs can achieve 10-b accuracy with careful design and layout techniques [4]. In order to achieve accuracy higher than 10-b, trimming or calibration is usually required. This chapter is intended to review some published ADC calibration techniques and to present a new background calibration technique for pipelined A/D converters.

2.2 Overview of Pipelined ADCs

Pipelined ADCs convert analog signals to digital codes stage by stage; each pipeline stage makes a coarse decision and then passes the residue voltage to the subsequence stages for fine conversions. The residue voltage is usually gained to maintain good dynamic range for the subsequent stages. For a given resolution, the number of stages and the gain of the residue signal depend on the number of bits each stage is resolving. Although a complete conversion involves multiple steps, the throughput, with pipelining, is only determined by one stage delay but not the total delay of all stages because pipelining only introduces latency. Figure 2.1 shows a block diagram of a 1-b per stage pipelined ADC. Ideally, the final output code is given by

$$D_o = d_1 \cdot 2^{N-1} + d_2 \cdot 2^{N-2} + d_3 \cdot 2^{N-3} + \cdots + d_{N-1} \cdot 2^1 + d_N \cdot 2^0 \tag{2.1}$$

where d_N is the decision from N-th stage. The figure also illustrates the ideal residue voltage transfer function of a 1-b pipeline stage. However, analog circuit impairments cause the transfer function to differ from the ideal one shown in Figure 2.2 [13]. Figure 2.2(b) plots the residue amplifier transfer function with switch charge injection, while Figure 2.2(c) and (d) plot the transfer functions with comparator offset and capacitor mismatch respectively. Beside resolving one bit per stage, each stage can resolve more than one bit; the 1.5-b/stage architecture [2, 3] is widely used due to its low per stage complexity, large feedback factor for its residue amplifier, and tolerance to comparator offset.

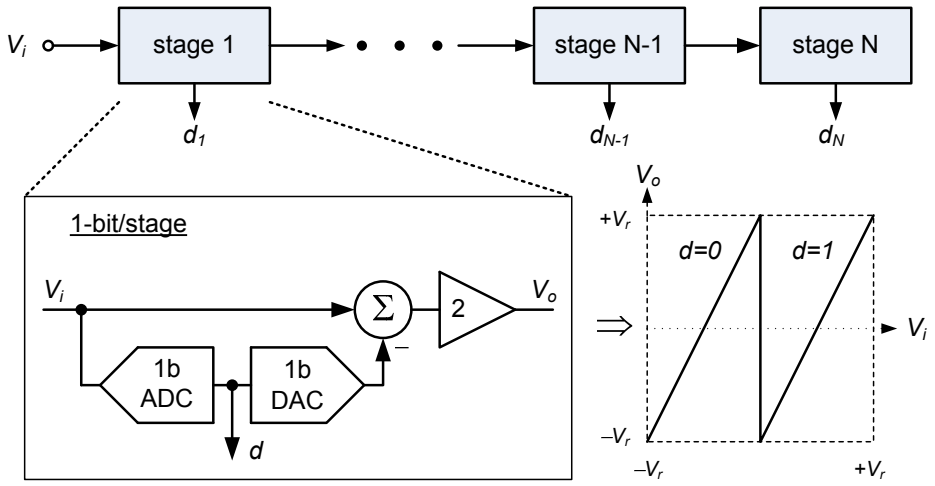


Figure 2.1: Ideal 1-b/stage pipelined ADC.

2.3 Review of ADC Calibration Techniques

In addition to the front-end track-and-hold (T/H) bandwidth limitation given by a technology, prominent analog impairments for ADCs include sampling capacitor mismatch, finite op-amp gain, and switch charge injection errors [1–5]. Analog circuit techniques [8, 14–19] have been used to correct these imperfections. However, complicated circuits are typically used to alter the analog path, which in turn lowers the conversion speed. In addition, analog techniques do not benefit from the CMOS device scaling that has improved the performance of digital circuits tremendously in the past three decades and will continue to improve in the coming decade. Digital calibration techniques [6, 7, 9–13, 20–30] have been used to correct ADC errors. Digital calibration can be further grouped into two categories, foreground [13, 20–22, 27] and background [6, 7, 9–12, 23–26, 28–30].

Digital foreground calibration usually involves measuring and storing the code error at major code transitions at system start-up and compensating afterward in digital domain during normal operation. One early example is [13]. In [13], the nominal gain

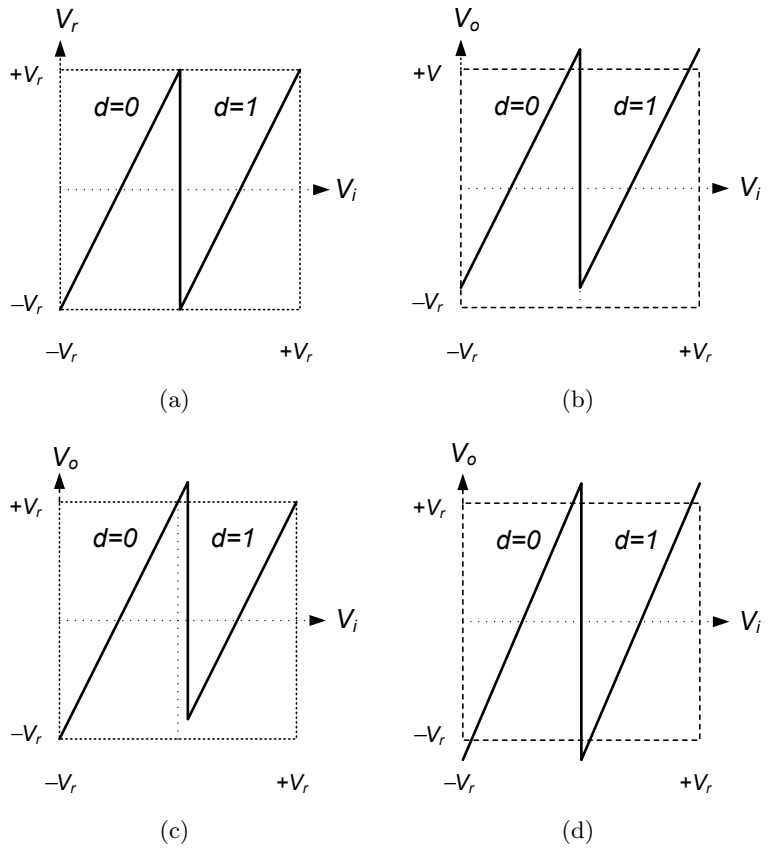


Figure 2.2: Residue amplifier transfer function: (a) ideal, (b) charge injection, (c) comparator offset, (d) capacitor mismatch.

of the residue amplifier is set to 1.93 (Figure 2.3) to ensure that the stage output does not over-range the subsequent stage because over-ranging problem cannot be corrected by digital post processing [13]. Assuming that the most significant bit (MSB) stage transfer function resembles that in the left of Figure 2.3, the overall transfer function of the ADC before calibration is the solid curve in the right side of Figure 2.3 provided that later stages are accurate. The missing codes cause the big jump in the ADC transfer function. In order to correct for the transition error, D_Δ which is S_1 - S_2 in digital form is first measured. If the current stage decision (D) is 0, the final ADC output (D_{out}) is the code from rest of

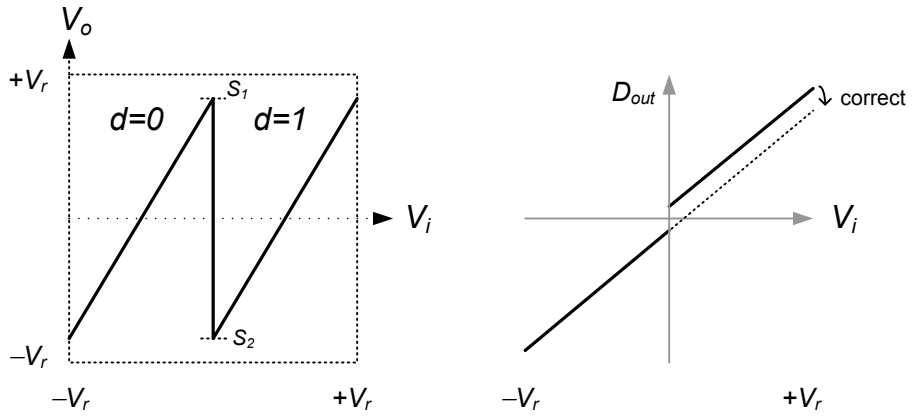


Figure 2.3: Residue amplifier transfer function with reduced radix and correction idea.

the pipelined stages, $D_{backend}$. When D is 1, $D_{out} = D_{backend} + D_{\Delta}$. This is equivalent to moving the right section of the original ADC transfer function down as illustrated in dotted line in Figure 2.3. Thus, this method eliminates the big jump in the overall transfer curve. The same measurement technique can be applied to any stage from the least significant bit (LSB) stages to the most significant bit (MSB) stages if necessary. The measured codes are stored in memory and used to compensate for the errors during normal ADC operation. However, foreground calibration lacks tracking capability; therefore, it is sensitive to drift in temperature, voltage supply, and device aging. Background calibration, no matter digital or analog, calibrates ADCs continuously in the background during normal operation [6–12, 23–26, 28–30]; thus, it has the advantages of tracking temperature change, voltage supply variations, and device aging. [6, 7] use skip-and-fill algorithm with nonlinear interpolation to allow the possibility of calibrating ADCs in the background synchronously with their normal operation. A conversion cycle is randomly chosen and skipped to free up a time slot for calibration. Then, the skipped conversion is filled in with nonlinear interpolation.

The calibration is done by forcing a known reference signal at the ADC input and then the error in the gain stage is measured. The error codes are stored in a memory to be addressed during normal operation. The calibration is done stage by stage, from the LSB stage to the MSB stage. Due to the nature of skipping a conversion, the input signal is limited to below $f_s/2$ where f_s is the sampling frequency of the ADC.

Instead of the skip-and-fill technique, [23] demonstrates a background calibration technique using a sample-and-hold queue to obtain time slots for calibration. A sample-and-hold (S/H) queue is placed in front of the ADC. Since the S/H queue is sampling at a slower rate than the ADC, the queue is empty after certain samples. When the queue is empty, the ADC following the queue is available for calibration. After one calibration cycle is completed, the ADC is switched back to convert the actual signal in the S/H. The same procedure repeats when the queue becomes empty again. The digital calibration is done by forcing the major transitions in the ADC transfer function to 1 LSB by an adaptive filter.

Another background calibration method utilizes an accurate-but-slow ADC [9,10] to correct for the errors in the ADC under calibration. [9] proposes using an accurate-but-slow ADC to correct the pipelined ADC residue amplifier voltage using LMS adaptive algorithm. The calibration is done stage by stage, from the LSB stages to the MSB stages. [10] employs a LMS adaptive filter to find the weight of each 1.5-b stage simultaneously pipelined stage with the help of a calibrated algorithmic ADC. However, the signal-dependent gain error in the residue amplifier is not calibrated in these techniques.

Dithering based techniques are utilized in [12,24–26,28–31] to calibrate the residue amplifier gain error. The idea is based on injecting a pseudo random signal (PRS) [12, 25,

26, 28–30] which is uncorrelated to the input signal to the MDAC. The gain of the pseudo random signal through the residue amplifier can be obtained by examining output of the whole ADC with correlation technique. Since the regular signal experiences the same gain as the pseudo random signal, the gain error of the residue amplifier can be found and corrected in digital domain. In [24], the first stage residue amplifier has two transfer voltage functions; either one will allow the correct operation of the ADC. The two transfer functions of the residue amplifier is dithered to find the nonlinear gain error caused by the low gain op-amp.

All these calibration techniques have been proven to be insufficient because analog signal paths are always disturbed during calibration, independent of whether the calibration is performed in the foreground or background. Traditional calibration is performed stage by stage from the LSB stage to the MSB stage. Calibrated less significant stages are used to calibrate the more significant stages until the MSB stage is calibrated. The sequential calibration is very cumbersome to implement, because it often requires switching precision circuits between different stages during calibration. The penalty of such technique is either consumption of higher power or reduction of the conversion speed [6–8, 13, 20–23]. Dithering based algorithm reduces the usable signal range and the tolerance range of comparator offset error. In addition, it often requires additional technique to correct the capacitor mismatch [12]. Finally, most techniques do not correct for nonlinear op-amp gain error except for those in [24, 27, 31].

2.4 Least-Mean-Square (LMS) Equalization Method

In contrast to traditional calibration techniques, a new calibration technique that treats analog impairments in analogy to distortion in communication channels can be employed to remove errors from all pipeline stages simultaneously using an adaptive digital filter. With this approach, the analog signal path is not disturbed during calibration and thus can maintain maximum conversion speed allowed by a certain technology. This approach is able to correct errors caused by capacitor mismatch, signal-dependent finite op-amp gain, and switch induced offset error. By relaxing requirements on precision matching and high open-loop op-amp gain, the new least-mean-square (LMS) calibration method can improve conversion accuracy and speed and can reduce power consumption.

2.5 Code-Domain Filtering Approach

A description of the calibration technique is discussed in this section. First, we formulate the input-output relationship of a 1.5-b/stage residue amplifier in code-domain filtering form. Second, we show that the same analysis can be applied to a 2.5-b/stage. Third, the effect of signal-dependent op-amp gain in the 1.5-b/stage is also investigated. In the end, we demonstrate that an LMS filter can be used to correct the errors by using an accurate reference signal. This is an extension to the work report in [32].

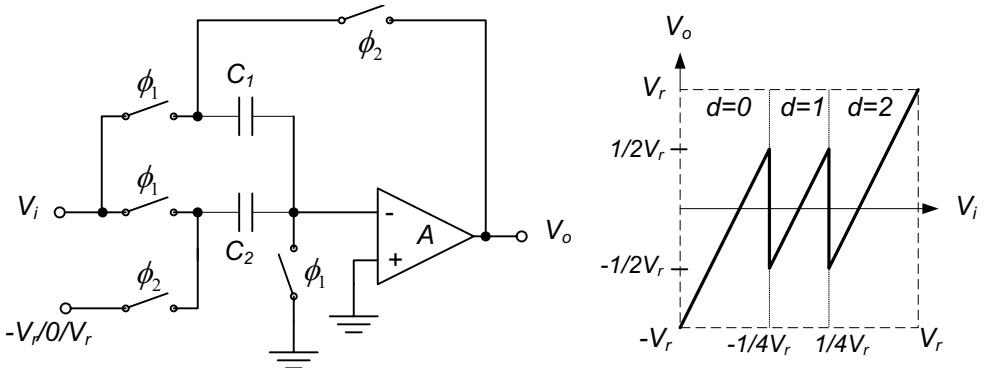


Figure 2.4: Residue amplifier of a 1.5-b/stage pipelined ADC and its voltage transfer function.

2.5.1 Code-Domain Formulation of 1.5-b/Stage Pipelined ADC Architecture

Figure 2.5.1 shows the residue amplifier of a typical switched-capacitor 1.5-b pipeline ADC stage and its voltage transfer function curve. The residue voltage can be derived as [32]

$$V_o = \frac{V_i(C_1 + C_2) - (d-1)V_r C_2 + V_{os}(C_1 + C_2 + C_x)}{C_1(1 + \frac{C_1 + C_2 + C_x}{AC_1})}. \tag{2.2}$$

where V_r is the reference voltage, C_x is the virtual ground parasitic capacitance, V_{os} is the offset voltage, A is the op-amp DC gain (constant), and d is the digital decision of the current stage. Specifically, d can either be 0, 1, or 2. The term $\frac{C_1+C_2+C_x}{AC_1}$ is the error from the finite op-amp DC gain. After some manipulations and dividing the equation by the reference voltage V_r (given that $D_i = \frac{V_i}{V_r}$, $D_o = \frac{V_o}{V_r}$, and $D_{os} = \frac{V_{os}}{V_r}$), a purely digital

representation of (2.2) is obtained,

$$D_i(\frac{C_1+C_2}{C_1}) = D_o(1+\frac{C_1+C_2+C_x}{C_1}\frac{1}{A}) + (d-1)(\frac{C_2}{C_1}) - D_{os}(\frac{C_1+C_2+C_x}{C_1}) \quad (2.3)$$

Equivalently, (2.3) can be rewritten as

$$D_i = D_o\alpha + (d-1)\beta - D_{os}\gamma \quad (2.4)$$

where

$$\alpha = (\frac{C_1}{C_1+C_2})(1+\frac{C_1+C_2+C_x}{C_1}\frac{1}{A}),$$

$$\beta = (\frac{C_2}{C_1+C_2}),$$

and

$$\gamma = (\frac{C_1+C_2+C_x}{C_1+C_2}).$$

(2.4) represents a filter with taps α, β, and γ. For an ideal pipeline stage, the values of α and β are 1/2, and the value of γ is 1. In reality, these coefficients are unknown due to capacitor mismatch, finite op-amp gain, and offset error.

2.5.2 Code-Domain Formulation of 2.5-b/Stage Pipelined ADC Architecture

The above code-domain analysis can be further extended to a 2.5-b pipeline stage. Figure 2.5 illustrates the residue amplifier of a 2.5-b pipeline stage and its voltage transfer function. The decision of the stage is listed in Table 2.1. The residue voltage of the 2.5-

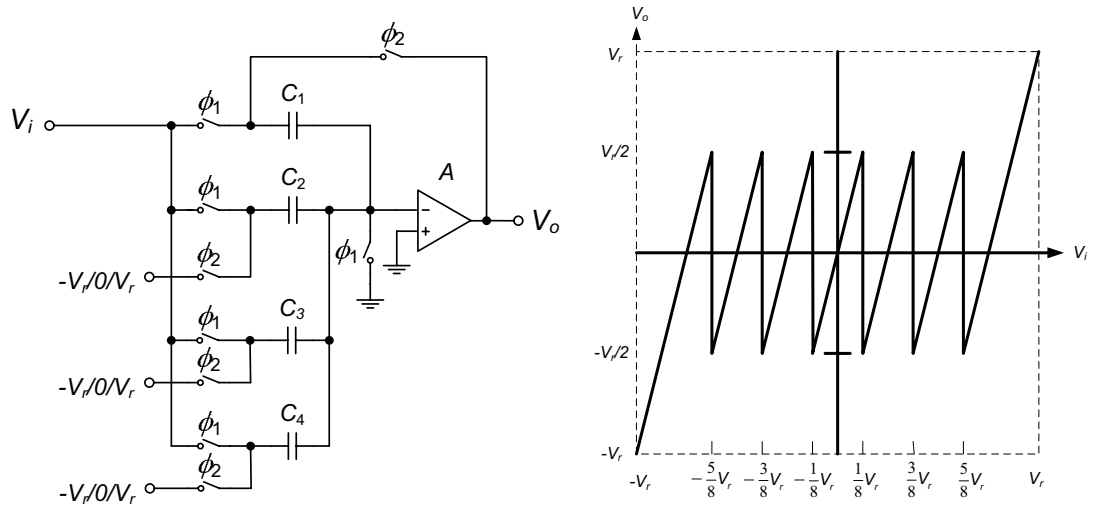


Figure 2.5: (a) Residue amplifier of a 2.5-b/stage pipelined architecture and (b) its voltage transfer function.

b/stage architecture can be derived as

$$V_o = \frac{1}{C_1(1+\frac{C_1+C_2+C_3+C_4+C_x}{AC_1})}\{V_i(C_1+C_2+C_3+C_4) - V_r[C_2a_1+C_3a_2+C_4a_3]+V_{os}(C_1+C_2+C_3+C_4+C_x)\} \tag{2.5}$$

Table 2.1: Decision of 2.5-b pipelined ADC stage

Analog input	Stage decision		
	a_1	a_2	a_3
$-V_r \leq V_i < -5/8V_r$	-1	-1	-1
$-5/8V_r \leq V_i < -3/8V_r$	-1	-1	0
$-3/8V_r \leq V_i < -1/8V_r$	-1	0	0
$-1/8V_r \leq V_i < 1/8V_r$	0	0	0
$1/8V_r \leq V_i < 3/8V_r$	1	0	0
$3/8V_r \leq V_i < 5/8V_r$	1	1	0
$5/8V_r \leq V_i < V_r$	1	1	1

where V_r is the reference voltage, C_x is the virtual ground parasitic capacitance, V_{os} is the offset voltage, A is the op-amp DC gain (constant), and a_1, a_2, a_3 are the digital decision of the current stage. Decisions a_1, a_2 and a_3 determine whether C_2, C_3 and C_4 should be connected to $-V_r$, 0 or V_r when ϕ_2 is high (amplifying phase). The term $\frac{C_1+C_2+C_3+C_4+C_x}{AC_1}$ is the error from the finite op-amp DC gain. Similar to the 1.5-b case, after some manipulations and dividing the equation by V_r (given that $D_i = \frac{V_i}{V_r}$, $D_o = \frac{V_o}{V_r}$, and $D_{os} = \frac{V_{os}}{V_r}$), a purely digital representation of (2.5) is obtained,

$$\begin{aligned} D_i(\frac{C_1+C_2+C_3+C_4}{C_1}) =& D_o(1+\frac{C_1+C_2+C_3+C_4+C_x}{C_1}\frac{1}{A}) \\ &+ a_1(\frac{C_2}{C_1}) + a_2(\frac{C_3}{C_1}) + a_3(\frac{C_4}{C_1}) \\ &- D_{os}(\frac{C_1+C_2+C_3+C_4+C_x}{C_1}) \end{aligned} \tag{2.6}$$

Equivalently, (2.6) can be written as

$$D_i = D_o\alpha + [a_1\ a_2\ a_3]\cdot\vec{\beta} - D_{os}\gamma \tag{2.7}$$

where

$$\alpha = (\frac{C_1}{C_1+C_2+C_3+C_4})(1+\frac{C_1+C_2+C_3+C_4+C_x}{C_1}\frac{1}{A}),$$

$$\vec{\beta} = [\beta_1\ \beta_2\ \beta_3] = [\frac{C_2}{C_1+C_2+C_3+C_4}\ \frac{C_3}{C_1+C_2+C_3+C_4}\ \frac{C_4}{C_1+C_2+C_3+C_4}],$$

and

$$\gamma = (\frac{C_1+C_2+C_3+C_4+C_x}{C_1+C_2+C_3+C_4}).$$

For an ideal 2.5-b pipeline stage, the values of α and each entry of $\vec{\beta}$ are 1/4, and the value of γ is 1. In reality, these coefficients are unknown due to capacitor mismatch, finite op-amp gain, and offset error.

2.5.3 Code-Domain Formulation of Residue Amplifier with Nonlinear Amplifier Gain

We have shown the input(D_i)-output(D_o) relationship of a residue amplifier with a linear amplifier DC voltage gain (A). However, the amplifier actual DC gain is nonlinear, i.e., signal dependent. We will show that we can also obtain an D_i-D_o relationship in code-domain filtering form [33]. For simplicity, a 1.5-b/stage residue amplifier is used to illustrate the idea. Figure 2.6 shows the block diagram of a 1.5-b/stage residue amplifier and its voltage transfer function with nonlinear amplifier gain. Similar to the case with a linear amplifier gain in Section 2.5.1, the residue voltage of a 1.5-b/stage can be expressed as

$$V_o = \frac{V_i(C_1+C_2) - (d-1)V_rC_2 + V_{os}(C_1+C_2+C_x)}{C_1(1+\frac{C_1+C_2+C_x}{A(V_o)C_1})} \tag{2.8}$$

where V_r is the reference voltage, C_x is the virtual ground parasitic capacitance, V_{os} is the offset voltage, $A(V_o)$ is the signal-dependent op-amp DC gain, and d is the digital decision of the current stage. The term $\frac{C_1+C_2+C_x}{A(V_o)C_1}$ is the error from the finite and nonlinear op-amp DC gain. Compare to (2.2), the only difference is that A is a function of V_o. After some manipulations and dividing the equation by V_r (given that $D_i = \frac{V_i}{V_r}$,and $D_{os} = \frac{V_{os}}{V_r}$), a

purely digital representation of (2.8) is obtained,

$$D_i(\frac{C_1+C_2}{C_1}) = D_o(1+\frac{C_1+C_2+C_x}{C_1}\frac{1}{A(D_o)}) + (d-1)(\frac{C_2}{C_1}) - D_{os}(\frac{C_1+C_2+C_x}{C_1}). \quad (2.9)$$

Equivalently, (2.9) can be rewritten as

$$\begin{aligned} D_i =& D_o\alpha_1 + {D_o}^2\alpha_2 + {D_o}^3\alpha_3 + {D_o}^4\alpha_4 + {D_o}^5\alpha_5 + ... \\ &+ (d-1)\beta - D_{os}\gamma \end{aligned} \quad (2.10)$$

where

$$\alpha_k = f_k(C_1, C_2, C_x, A(D_o)),$$

$$\beta = (\frac{C_2}{C_1+C_2}),$$

and

$$\gamma = (\frac{C_1+C_2+C_x}{C_1+C_2}).$$

The same analysis can be applied to 2.5-b/stage residue amplifier to derive the digital representation of the analog input voltage.

2.5.4 Code-Domain Formulation of a Complete Pipelined ADC

After deriving the input(D_i)-output(D_o) relationship of a single residue amplifier, we are now going to show the input-output relationship of a complete pipelined ADC. A 1.5-b/stage pipelined ADC is shown in Figure 2.7. Using (2.4), we obtain D_i of each

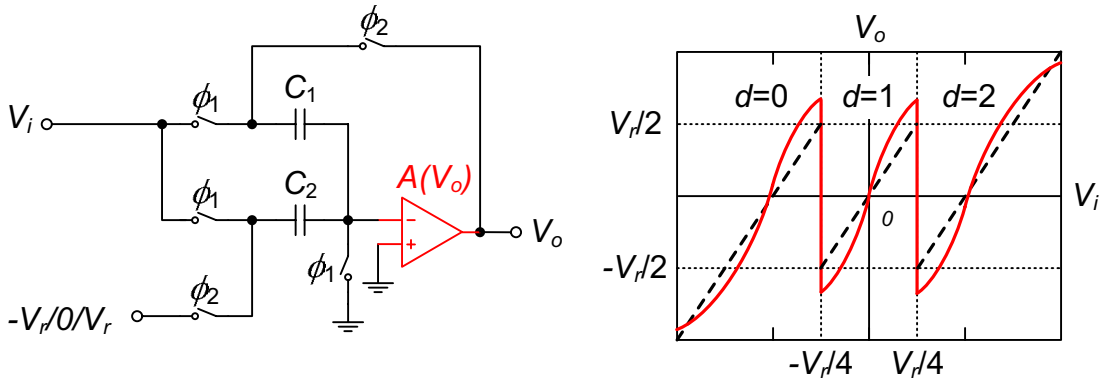


Figure 2.6: Residue amplifier of a 1.5-b/stage pipelined ADC with nonlinear-amplifier gain and its voltage transfer function (solid line).

stage [32],

$$D_{i,1} = D_{o,1}\alpha_1 + (d_1 - 1)\beta_1 - D_{os,1}\gamma_1 \tag{2.11}$$

$$D_{i,2} = D_{o,2}\alpha_2 + (d_2 - 1)\beta_2 - D_{os,2}\gamma_2 \tag{2.12}$$

$$D_{i,3} = D_{o,3}\alpha_3 + (d_3 - 1)\beta_3 - D_{os,3}\gamma_3 \tag{2.13}$$

$$\vdots$$

$$D_{i,N} = D_{o,N}\alpha_N + (d_N - 1)\beta_N - D_{os,N}\gamma_N. \tag{2.14}$$

Since $D_{o,N} = D_{i,N+1}$, the digital representation of the input signal can be derived recursively as

$$D_{in} = D_{i,1} = [[(..)\alpha_3 + (d_3 - 1)\beta_3 - D_{os,3}\gamma_3)]\alpha_2 + (d_2 - 1)\beta_2 - D_{os,2}\gamma_2]\alpha_1 + (d_1 - 1)\beta_1 - D_{os,1}\gamma_1. \tag{2.15}$$

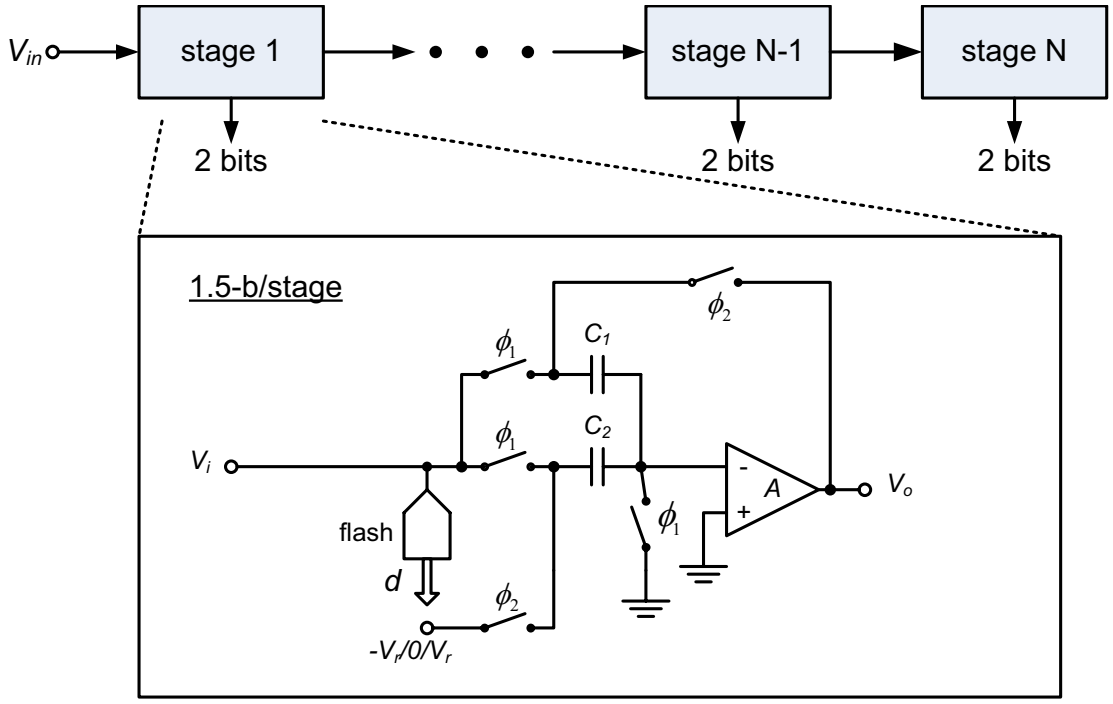


Figure 2.7: Block diagram of a multi-stage 1.5-b/stage pipelined ADC.

Equivalently, (2.15) can be written as

$$D_{in} = A + B + \Gamma \tag{2.16}$$

where

$$\begin{aligned} A &= ((d_1 - 1)\beta_1 + (d_2 - 1)\beta_2\alpha_1 + (d_3 - 1)\beta_3\alpha_2\alpha_1 + ... + (d_N - 1)\beta_N\alpha_{N-1}\alpha_{N-2}...\alpha_1 \\ &= \sum_{k=1}^{N}(d_k - 1)f_k \end{aligned}$$

$$B = D_{o,N}\alpha_N\alpha_{N-1}...\alpha_2\alpha_1 = D_{o,N}\prod_{k=1}^{N}\alpha_k,$$

$$\Gamma = -D_{os,1}\gamma_1 - D_{os,2}\gamma_2\alpha_1 - D_{os,3}\gamma_3\alpha_2\alpha_1 - ... - D_{os,N}\gamma_N\alpha_{N-1}\alpha_{N-2}...\alpha_1.$$

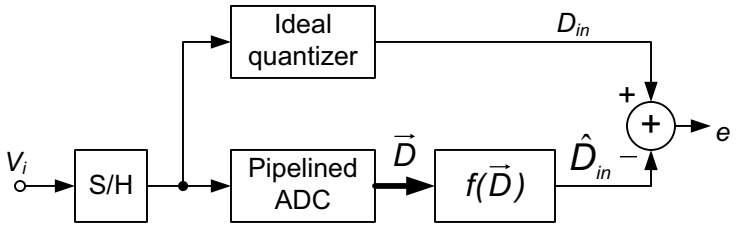


Figure 2.8: Error correction of pipelined ADC: code-domain nonlinear channel equalizer.

(2.16) formulates a filter in code-domain. A, B, and Γ are the weighed sum of digital output of each pipelined stage, quantization error, and the total input-referred offset respectively. D_{in} with signal-dependent op-amp gain can be derived in the same fashion using (2.10) and the method presented in this subsection. The same method can also be extended to 2.5-b per stage using (2.7).

2.5.5 Code-Domain Filtering Technique System Architecture

Although, the tap values in (2.16) are, in reality, unknown due to capacitor mismatch, finite op-amp gain, and offset error, an adaptive technique can be applied to obtain the tap values. This problem can be treated similar to a channel equalization problem as illustrated in 2.8. An ideal qualifier is used to train the filter taps in this case. This leads to an adaptive background calibration scheme using the steepest decent gradient method as shown in Figure 2.9. The output vector $\vec{D}$ of a high-speed, inaccurate pipelined ADC is decimated and applied to the adaptive digital filter, while a slow-but-accurate A/D converter is used to obtain the ideal value of D_{in}. Least-mean-square (LMS) algorithm is used to update the filter taps at the speed of the slow-but-accurate A/D converter.

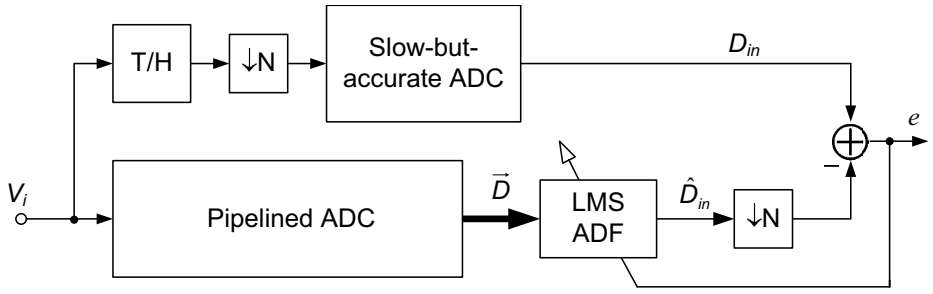


Figure 2.9: Error correction of pipelined ADC: code-domain LMS adaptive equalizer.

2.6 Behavioral Simulations

To demonstrate the effectiveness of the scheme, a behavioral model (Figure 2.9) is developed to simulate the LMS calibration scheme. Using this technique, the gain requirement of amplifiers can be greatly reduced; thus, simple and inherently fast amplifiers can be used to increase ADC conversion speed. The pipelined ADC, the reference ADC, and the LMS adaptive filter are modeled using Simulink® blocks [34]. To reduce the simulation time, no decimation is performed, i.e., LMS adaption is running at the sampling rate of the pipelined ADC. Since the target accuracy of the calibrated ADC is 12-b, an ideal 14-b ADC is used as the slow-but-accurate reference ADC. The pipelined ADC has $(12+2)$ raw output bits; the extra two bits is used for calibration and ensures that the final quantization error(2.15) is below one LSB (12 bits). The pipelined ADC model includes analog circuit non-idealities such as capacitor mismatch, small and nonlinear amplifier gain, comparator offset, and amplifier offset.

2.6.1 Simulation Results

As an example, the first stage of the pipelined ADC employs 1.5-b/stage architecture, while stage 2 to stage 7 employ 2.5-bit/stage architecture. In the LMS filter, additional taps are used to correct signal-dependent op-amp gain up to fifth-order as explained in Section 2.5.3. Despite of the described pipelined ADC architecture is used, the LMS calibration algorithm is valid in any pipelined ADC architecture with inter-stage redundancy. The initial parameter settings are listed in Table 2.2. The op-amp gain for the simulation is also in illustrated in Figure 2.10. The capacitor mismatch errors are first examined. The input signal of the simulation is a sine wave with an amplitude equal to the pipelined ADC reference voltage, V_r. The sampling capacitors are set as listed in Table 2.2, but all other parameters are ideal. The smallest step size is 2^{-29}. The learning curve is shown in Figure 2.11(a). The mean-square-error (MSE) converges to below -70dB after 500,000 iterations. The amplifier gain effect is the next impairment examined. The nonlinear amplifier gain is modeled as a power series up to fifth order. A typical amplifier gain transfer function shown in Figure 2.10 is used in the behavioral simulations. Again, other parameters are set to ideal values. The learning curve is shown in Figure 2.11(b). Finally, all the static error sources are included in the simulation (Table 2.2 and Figure 2.10). The learning curve and the convergence of filter taps are shown in Figure 2.11(c) and Figure 2.11(d), respectively. Figure 2.12 shows the INL and DNL of the ADC before and after calibration. Although a sine wave input is used in the above simulations, we found in simulation that input signal statistics have little effect on the convergence rate of the adaptive LMS filter. The learning curve with saw-tooth and random inputs are shown in Figure 2.13. Compared to the one

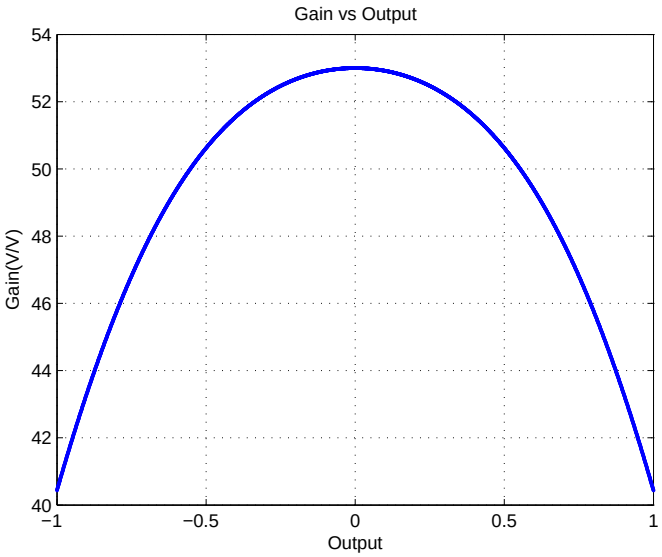


Figure 2.10: Gain transfer function of a typical amplifier.

Table 2.2: Circuit parameters of the pipelined ADC used in behavioral simulations.

Pipelined stage	Sampling Cap mismatch	Op-amp input-referred offset	Comparator offset	Comparator noise	C_x/C_1
1(1.5-b)	5%	10% $V_r(3\sigma)$	10% $V_r(3\sigma)$	1% $V_r(3\sigma)$	30%
2-7(2.5-b)	5%	10% $V_r(3\sigma)$	10% $V_r(3\sigma)$	1% $V_r(3\sigma)$	30%

with sine wave input (Figure 2.11), the difference is very negligible. Figure 2.14 shows the FFT plot of a sine wave input before and after calibration. The SNR improves from 32 dB to 72 dB and the SFDR improves from 35 dB to 93 dB. Although an ideal 14-b reference ADC is used here, simulation shows that random noise at the 14-b reference ADC output has small effect on the effectiveness of the calibration because the random noise is averaged in the LMS filter. Figure 2.15 shows the PSD of the ADC before and after calibration when the reference ADC only has an SNR of 9 bits but more than 16-bit SFDR. We can achieve close to 12-b SNR after calibration; thus, achieving high-linearity of the reference ADC is

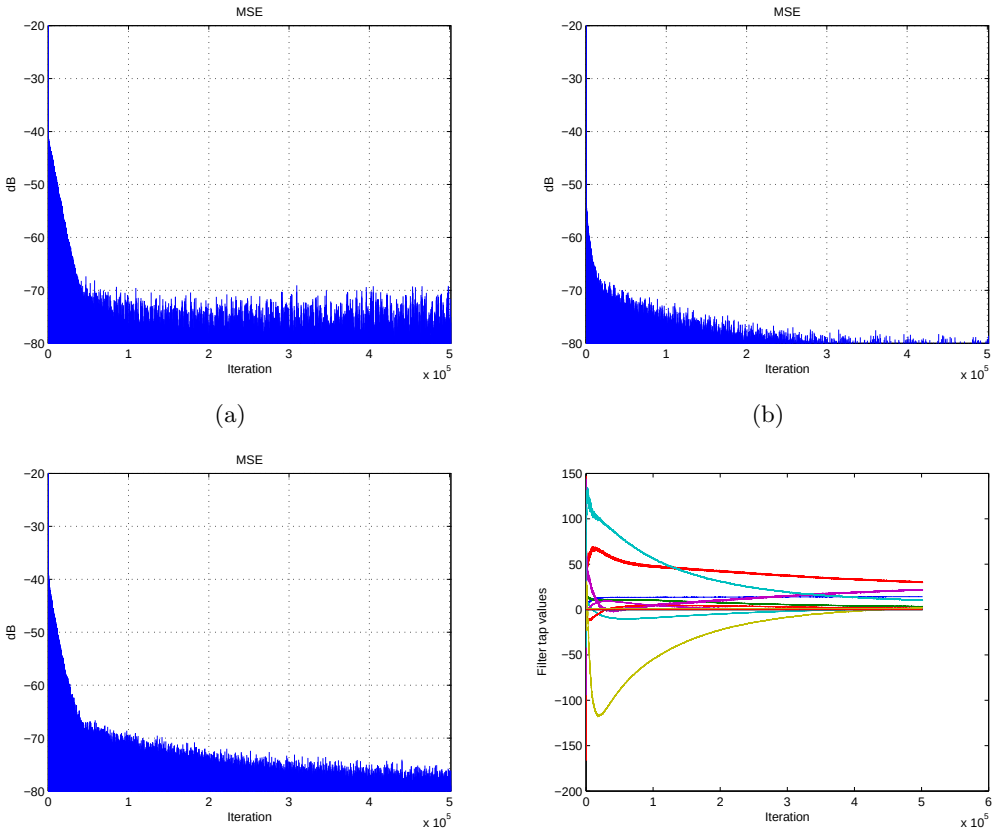


Figure 2.11: Learning curve for (a) capacitor mismatch, (b) nonlinear amplifier gain, (c) all combined errors, (d) filter tap values.

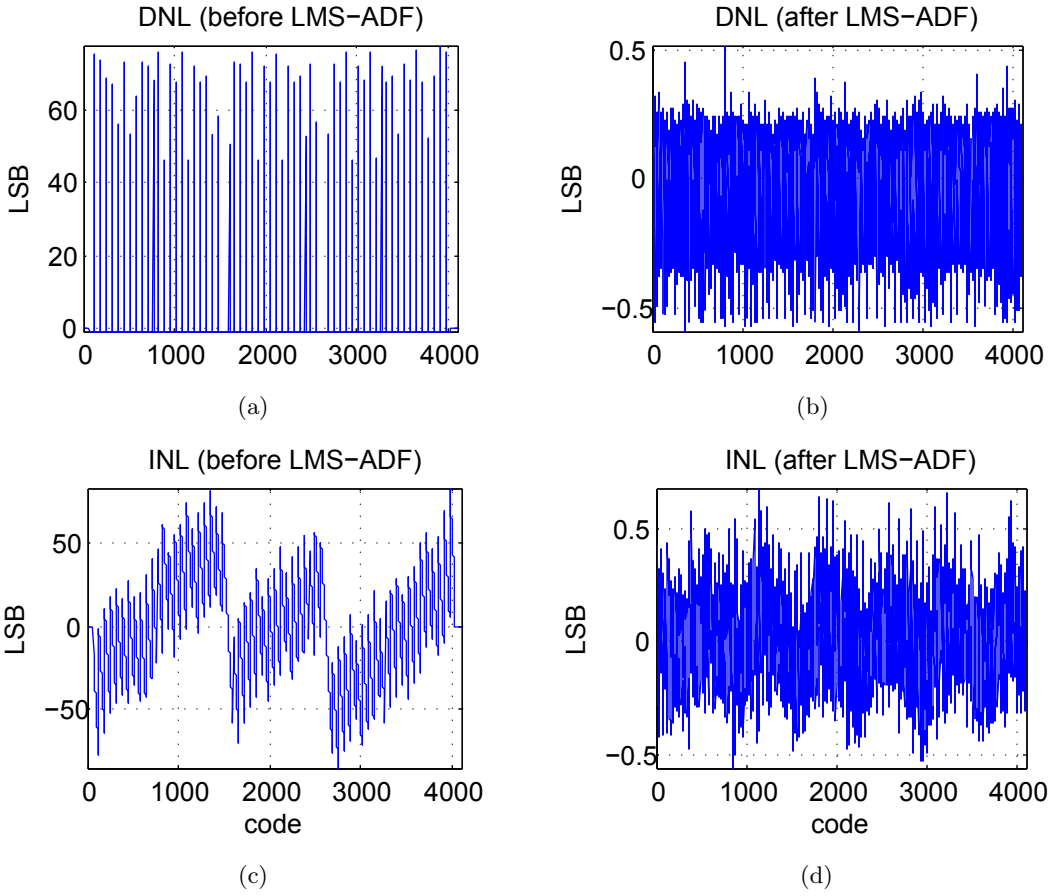
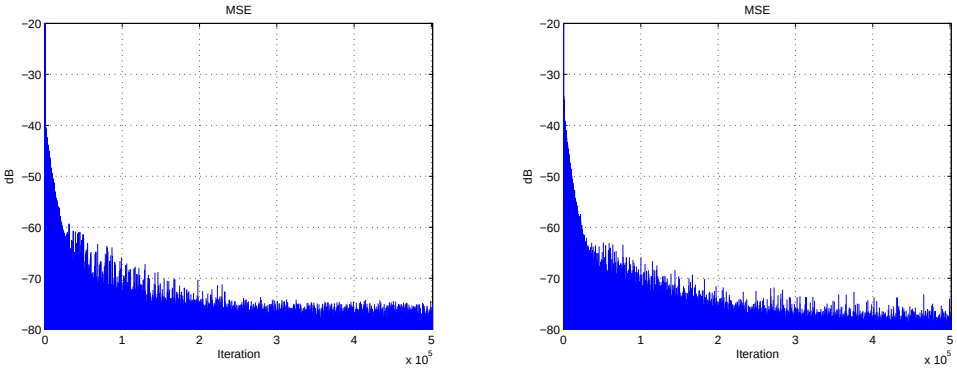
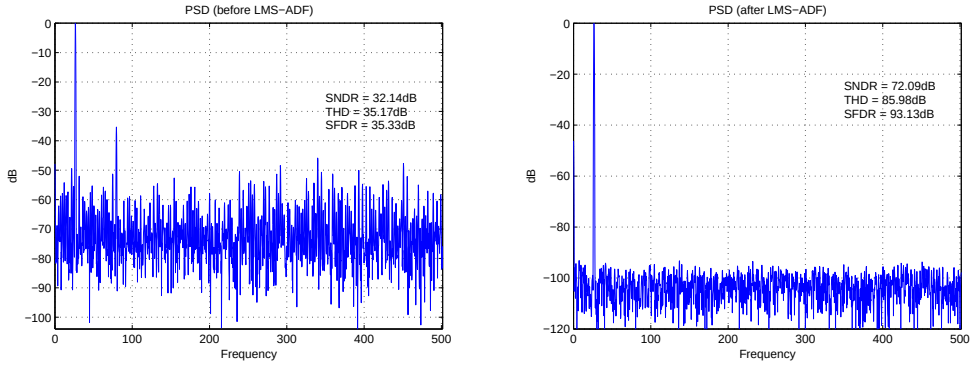


Figure 2.12: (a) DNL before calibration, (b) INL after calibration, (c) INL before calibration, (d) DNL after calibration.



(a) (b)

Figure 2.13: Learning curve of (a) saw-tooth, (b) random signal



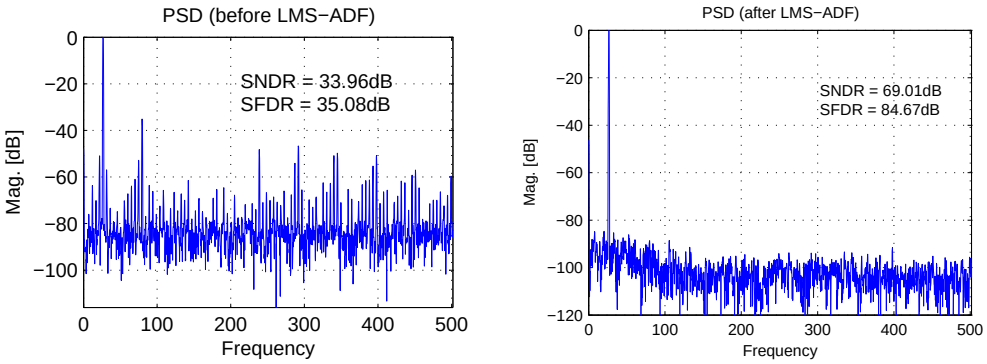
(a) (b)

Figure 2.14: (a) FFT plot before calibration, (b) FFT plot after calibration.

most important.

2.6.2 Performance Analysis

In Section 2.5, we formulated a code-domain adaptive filter that compensates linear and nonlinear errors of pipelined ADCs. This code-domain is unique to pipelined ADCs due to the built-in redundancy of the decisions levels. Instead of giving a thorough treatment of performance analysis, a few observations are summarized below [32]:



(a) (b)

Figure 2.15: Calibration with a noisy reference ADC: (a) FFT plot before calibration, (b) FFT plot after calibration.

Steady-State MSE

When op-amp nonlinearity is excluded, the filtering formulation derived in (2.16) is exact. This indicates that memoryless errors can be fully removed when quantization noise is negligible(noise enhancement will be covered in the next part). This argument is justified by behavioral simulations: steady state MSE close to 12 bits is constantly achieved in spite of the presence of various other errors in the ADC. The MSE is also a function of the step size μ; a gear-shifting algorithm can be used to further reduce MSE in the steady state.

Noise Enhancement

It is widely known in communication theory that linear equalization (LE) suffers from a noise enhancement problem when the power spectrum of the input signal is not flat [35]. It is difficult to quantify the noise enhancement effect of the proposed calibration algorithm as the concept "frequency" in code-domain is not well understood. However, we

point out the following case where quantization noise is enhanced due to equalization: if many output codes are missing, i.e., all α_k in (2.16) are substantially larger than 1/2 , the second term in (2.16) which is normally the quantization noise will be greatly magnified. This happens when capacitor mismatch or finite op-amp gain effect is severe. A code density test reveals nulls in the statistics (DNL in Figure 2.12). This may serve as an intuition for the non-flatness of the "spectrum". The remedy to this problem is to increase the word length of the raw code, i.e., to add more stages. This occurs with low overhead of power consumption since an optimum pipelined design often employs stage scaling where power consumption is dominated by the MSB stages.

Singularity

The filtering problem can be approached using a least-squares formulation [35] as well. As before, define a code-domain vector $\overrightarrow{D(n)} = [D_1(n)\ D_2(n) \cdots D_N(n)]^T$ for ADC decisions on the n-th sample. Augment $\overrightarrow{D(n)}$ by a dc component, $D_0(n)$, $\overrightarrow{D(n)} = [D_0(n)\ D_1(n)\ D_2(n) \cdots D_N(n)]^T$. We want to solve the linear equations (2.17),

$$\begin{bmatrix} D_{in}(n) \\ D_{in}(n+1) \\ \vdots \\ D_{in}(n+N) \end{bmatrix} \approx \begin{bmatrix} D_0(n) & D_1(n) & \cdots & D_N(n) \\ D_0(n+1) & D_1 n+1 & \cdots & D_N(n+1) \\ \vdots & \vdots & \vdots & \vdots \\ D_0(n+N) & D_1(n+N) & \cdots & D_N(n+N) \end{bmatrix} \begin{bmatrix} f_0 \\ f_1 \\ \vdots \\ f_N \end{bmatrix}$$

or

$$\vec{Y} \approx \mathbf{X}\vec{F} \tag{2.17}$$

for $\vec{F}$ subject to least-squares criteria, where $\vec{Y}$ is a vector of $(N+1)$ input samples, $\vec{F}$ contains $(N+1)$ unknown tap values of the filter, and $\mathbf{X}$ is a matrix of $(N+1)\times(N+1)$ decision codes of the ADC made across time (rows) and stages (columns).

Note that we have formulated $\mathbf{X}$ as a square matrix for illustration purpose. In general, it can be rectangular, and numerical techniques such as singular value decomposition (SVD) can be applied to the problem. In case when $\mathbf{X}$ is nonsingular, the solution to (2.17) is trivial, shown here as

$$\vec{F} = \mathbf{X}^{-1}\vec{Y}. \tag{2.18}$$

In theory, this means that a set of $(N+1)$ noiseless observations of D_{in} and $\vec{D}$ should yield enough information to determine $(N+1)$ unknown tap values. This statement has a profound implication: it means that the input signal V_{in} does not have to exercise the whole input range to make the digital correction work; a limited set of $(N+1)$ noiseless samples is enough. But singularity can occur if V_{in} is confined to a small region which is a subset of $[-V_r, V_r]$, where $D_1(n)$ does not toggle for all $(N+1)$ samples as an example. This means that the second column of $\mathbf{X}$ is constant, making it linearly dependent on the first column that is also a constant (the dc tap). Thus, rank($\mathbf{X}$) is at most N , i.e., the matrix is singular. Fortunately, when $\mathbf{X}$ is singular, a solution to (2.17) still exists, but it is not unique. Adaptive filtering theory says that an LMS or a recursive-least-squares (RLS) algorithm will still work [35]. The difference is that the error surface $|\epsilon(f_0, f_1, \cdots, f_N)|^2$ as a function of the filter tap values will not be a bowl shape with a global minimum, but instead will be a valley where $|\epsilon|^2$ is minimum everywhere inside; instead of converging, f_0 and f_1 wander around subject to a linear constraint. As (2.16) says the global optimum

filter is unique, this indicates that a subset of the solution (f_2 to f_N) has been found and this solution is still optimal inside the limited region of observation. As V_{in} excursion reaches outside of this region, the degeneration is lifted and more tap values can be determined. On the other hand, when more degeneration occurs, i.e., the second stage of the ADC also outputs a constant, f_2 will also fail to converge, and an even smaller subset of the solution yields. The above phenomena have been observed through simulation.

Another way of interpreting this is that ADF adaptation follows the input signal: it will adapt to the right local solution wherever the input signal resides. This occurs when the system of (2.17) becomes underdetermined. The local solution will converge to the unique global optimum when enough information is obtained from samples, and $\mathbf{X}$ goes out of singularity. In other words, this indicates that calibration will yield better performance where the ADC is more frequently used.

2.7 Conclusion

In this chapter, we have reviewed different calibration techniques used to correct gain stages in ADCs. We have also shown the effectiveness of the nonlinear filtering technique with LMS algorithm in correcting pipelined ADC analog circuit impairments. We will next present the design of the reference ADC.

Chapter 3

High-Accuracy Reference ADC

3.1 Background Calibrated Analog-to-Digital Converter (ADC) System Overview

The block diagram of the ADC system is shown in Figure 3.1. The analog/mixed-signal portions are implemented on a chip while the digital portion is implemented on an FPGA. The system consists of a S/H followed by a slow-and-accurate ADC, a pipelined ADC, and a clock generator producing all clock phases for different building blocks. Note that the S/H could either be a dedicated block or a part of the slow-and-accurate ADC depends on the reference ADC architecture. The target performance of the calibrated ADC is 12 bits.

The rest of this chapter explores options for high-resolution ADCs to be used as the reference ADC previously discussed in Section 2.6. The performance requirement of the ADC is first discussed. Then, a few potential architecture such as integrating ADC,

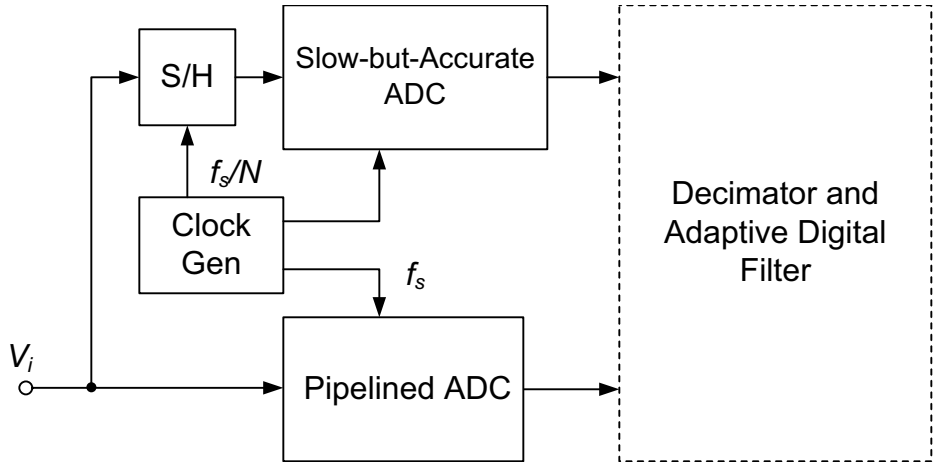


Figure 3.1: ADC system block diagram.

successive approximation ADC, algorithmic ADC, and oversampling ADC are presented.

3.2 Slow-but-Accurate A/D Converters

Chapter 2 details the LMS calibration algorithm, which allows us to combine the high speed of pipelined A/D converters and the accuracy of a slower ADC to implement a high-speed and accurate converter. Although the speed of the reference ADC is not our main concern, its data rate must be fast enough for the adaptive digital filter to track drifts in temperature and power supply variations. In addition, the reference A/D converter has to be more accurate than the target overall A/D converter to provide a good reference signal to the LMS adaptive digital filter. As simulations in Section 2.6 show that the calibration performance tends to be limited by the linearity of the reference path instead of noise, extra attention is required in the reference ADC design to ensure an almost 14-bit accuracy. Candidates for this kind of application are integrating, successive approximation, algorithmic/cyclic, and $\Sigma\Delta$ A/D converters.

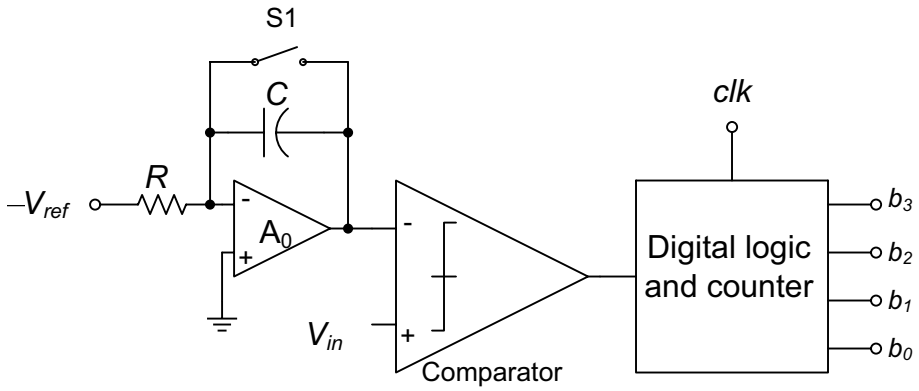


Figure 3.2: Block diagram of a single-slope integrating A/D converter.

3.3 Integrating A/D Converters

Integrating A/D conversion [36] [37] is a very efficient approach in realizing high accuracy data converters. Integrating ADCs can be implemented with a small amount of simple analog components and digital logic. Figure 3.2 shows the block diagram of a single-slope integrating A/D converter. The integrator produces an input ramp signal, which is compared with the input signal (V_{in}). The digital counter begins counting when the ramp starts and stops incrementing after the ramp signal reaches the input signal level. Let the time taken for the counter to stop be t_1. t_1 is given by

$$t_1 = RC\frac{V_{in}}{V_{ref}}. \tag{3.1}$$

The digital code (D) of the input analog signal is

$$D = t_1 \times f_{clk}. \tag{3.2}$$

This type of data converter is linear and inherently monotonic. The accuracy of the system is determined by the clock generator, the RC time constant of the integrator, and the reference voltage V_{ref}. The amplifier offset can be measured with a zero input and canceled out using digital logic. However, this kind of converter is quite slow and the worst-case speed occurs when V_{in} equals V_{ref}. In this case, one conversion requires 2^N clock cycles. For example, a 14-b single-slope integrating converter with a 64MHz clock rate, the conversion rate is only 3.9kHz. Besides the simple single-slope topology, there is also a dual-slope counterpart [36] [37]. Dual-slope converters solve some of the accuracy problems of single-slope converters, but the conversion time is doubled.

3.4 Successive Approximation A/D Converters

The block diagram of a successive approximation A/D converter is illustrated in Figure 3.3. A successive approximation converter applies a binary search to find a digital code closest to the analog input signal. The most significant bit (MSB) is first resolved, then the second most significant bit is determined, and so on until the least significant bit (LSB) is found. For example, initially, the A/D converter decides if an analog input is greater than or smaller than 1/2. If it is smaller than 1/2, the converter then determines whether the input is greater than or smaller than 1/4. If it is smaller than 1/4, the successive approximation A/D converter again determines if the input is greater or smaller than 1/8 and so on until the LSB is resolved. Thus, an N-b successive approximation A/D converter requires N clock cycles. In Figure 3.3, the sample-and-hold (S/H) is required to keep the input constant during the conversion process. The DAC is the main design challenge

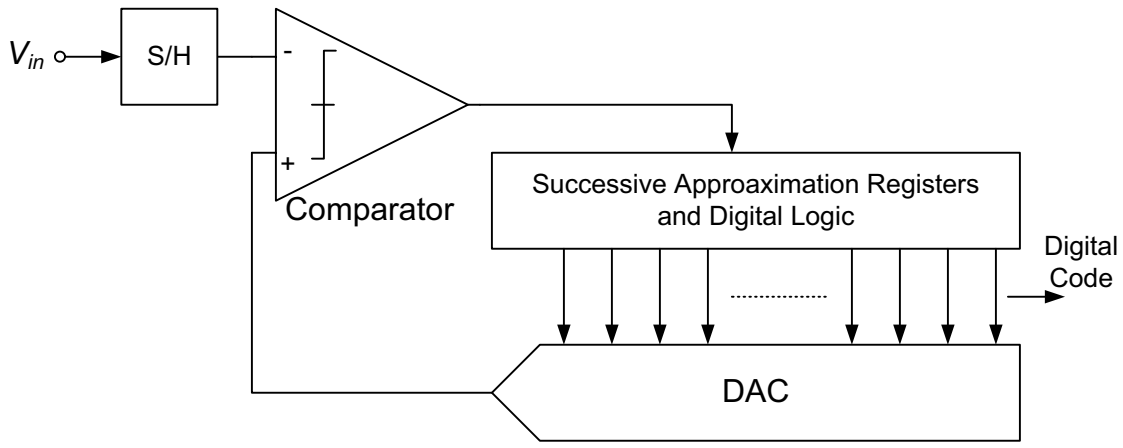


Figure 3.3: Block diagram of a successive approximation ADC.

because it determines the A/D converter's accuracy and speed. It usually requires trimming or calibration achieve more than 10 bits. The conversion rate for successive approximation ADCs is moderate. For example, a 14-b converter, with a 64MHz clock, the conversion rate is 4.5Msample/sec. This topology is very power efficient.

3.5 Algorithmic/Cyclic A/D Converters

An algorithmic A/D converter [14] [15] [38] is very similar to a successive approximation ADC. Instead of changing the comparator threshold voltage in each clock cycle, algorithmic ADC doubles the error (residue) voltage in every cycle. The block diagram of an algorithmic converter is shown in Figure 3.4. During each clock cycle, one bit is resolved, from MSB to LSB. Limitation of an algorithmic ADC is the building of an accurate multiply-by-two gain stage due to analog component mismatch and amplifier gain error. The conversion rate of an algorithmic ADC is the same as a successive approximation ADC. N clock cycles are required for an N-b converter.

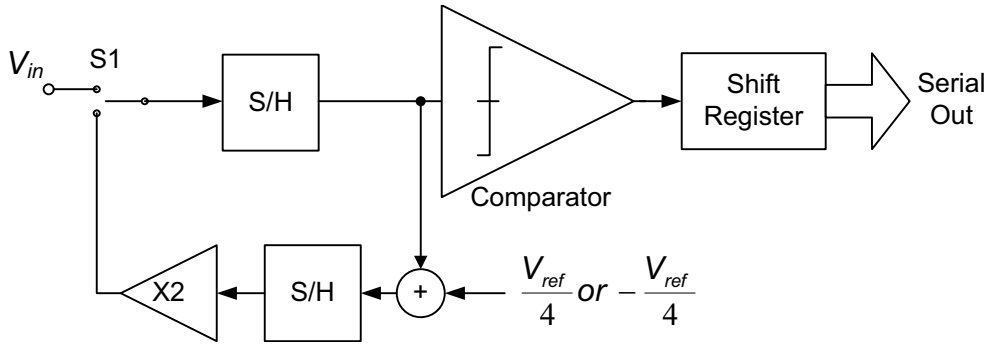


Figure 3.4: Block diagram of an algorithmic/cyclic ADC (full-scale input = $\pm 1/2V_{ref}$).

3.6 Oversampling A/D Converters

Oversampling A/D converters are commonly used in digital audio applications to achieve very high accuracy (16-b or more) [39] [40] [41] [42]. Extra dynamic range is obtained by spreading the quantization noise over a large frequency range. A digital low-pass filter is then used to filter out the quantization noise at high frequencies. Noise-shaped oversampling (sigma-delta) ADC further enhances the dynamic range by pushing most of the quantization noise into the high frequency range, which is attenuated by a low-pass digital filter. It has been proven that $\Sigma\Delta$ A/D converters are very insensitive to analog impairments such op-amp gain error and capacitor mismatch. The conversion rate of a $\Sigma\Delta$ ADC is equal to the sampling rate divided by the oversampling ratio (M). $\Sigma\Delta$ ADCs can be separated to two categories, which are single-loop [43] and multi-loop cascaded sigma-delta ADCs [44]. Besides, some ADCs [43] employ a single-bit quantizer due to its inherent linearity. Other published recently published ADCs [45] [46] use a multi-bit DAC with dynamic element matching (DEM) to achieve increased high dynamic range without raising the oversampling ratio (M). A more detailed analysis of sigma-delta ADCs is presented

next.

3.7 First-Order Sigma-Delta ($\Sigma\Delta$) A/D Converters

Sigma-delta A/D converters are the most popular and widely used oversampling A/D converters. The block diagram of a first-order single-bit design is shown in Figure 3.5. The digital integrator in the figure is given by

$$H_{int}(z) = \frac{z^{-1}}{(1 - z^{-1})}. \tag{3.3}$$

The feedback loop forces the output digital signal Y to match the input signal X so that the average DAC output is approximately equal to the average of the input signal. Since the transfer function of the comparator quantization noise has a high-pass characteristic, quantization noise (error) from the single-bit quantizer is shaped by the loop filter such that it is pushed out to high frequencies. The following low-pass decimation filter attenuates the high frequency components of quantization noise. The quantization noise transfer function is given by

$$H_Q(z) = (1 - z^{-1}). \tag{3.4}$$

The dynamic range (DR) of the first-order sigma-delta is given by [47]

$$DR = 10 \cdot log(\frac{9M^3}{2\pi^2}) \tag{3.5}$$

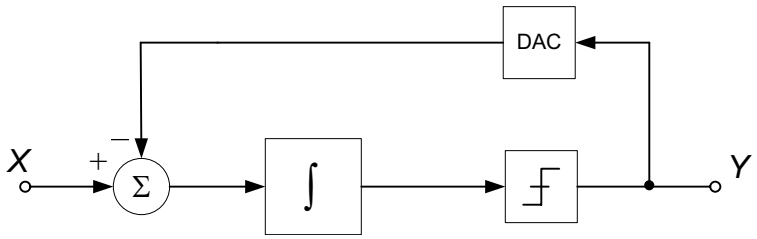


Figure 3.5: First-order ΣΔ A/D converter.

in dB where M is the oversampling ratio. The dynamic range increases by 9dB with doubling the oversampling ratio M. A first-order sigma-delta ADC is unconditionally stable because the pole is always inside the unit circle in the pole-zero plot. However, it suffers from DC idle tones [48].

3.8 Second-Order ΣΔ A/D Converters

Second-order ΣΔ ADCs [49] further reduce inband quantization noise by adding an extra integrator in the loop as illustrated in Figure 3.6. The quantization noise transfer function is given by

$$H_Q = (1 - z^{-1})^2 \tag{3.6}$$

The dynamic range of a second-order sigma-delta A/D converter is given by [47]

$$DR = 10 \cdot log(\frac{15M^5}{2\pi^4}) \tag{3.7}$$

in dB. Thus, the dynamic range increases by 15dB with doubling the oversampling ratio M. This is a significant improvement over the first-order sigma-delta A/D converter. The stability of the second-order sigma-delta is also unconditionally guaranteed.

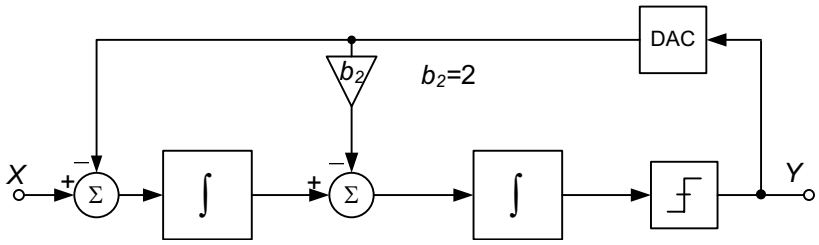


Figure 3.6: Second-order ΣΔ A/D converter.

3.9 Multi-Stage Noise Shaping (MASH) ΣΔ A/D Converters

Second-order noise-shaping with low oversampling ratio may not be adequate to achieve high resolution. To achieve a 14-b dynamic range, the oversampling ratio needs to be at least 80. Adding additional integrators inside the loop further boosts the order of noise-shaping [50]. However, stability is not guaranteed with a third or higher-order ΣΔ A/D converter. Due to nonlinear nature of the comparator, it is difficult to model the comparator and to use linear feedback theory to ensure the stability of higher-order ΣΔ ADC. Thus, most designs are based on cascading multiple first and second-order ΣΔ A/D converters as an alternative scheme to realize high-order noise-shaping. Such architecture is called MASH [36] or cascaded ΣΔ A/D converter.

3.9.1 2-1 MASH ΣΔ A/D Converters

The simplest MASH ΣΔ A/D converter is 2-1 MASH, in which a second-order converter is cascaded by a first-order sigma-delta. In Figure 3.7, results from both the first stage and the second stage are post-processed by the digital error correction logic. An intuitive way to understand MASH sigma-delta ADC operation is by noting that quantization noise from the first stage is additively shaped by the second stage. Thus, the addition of the

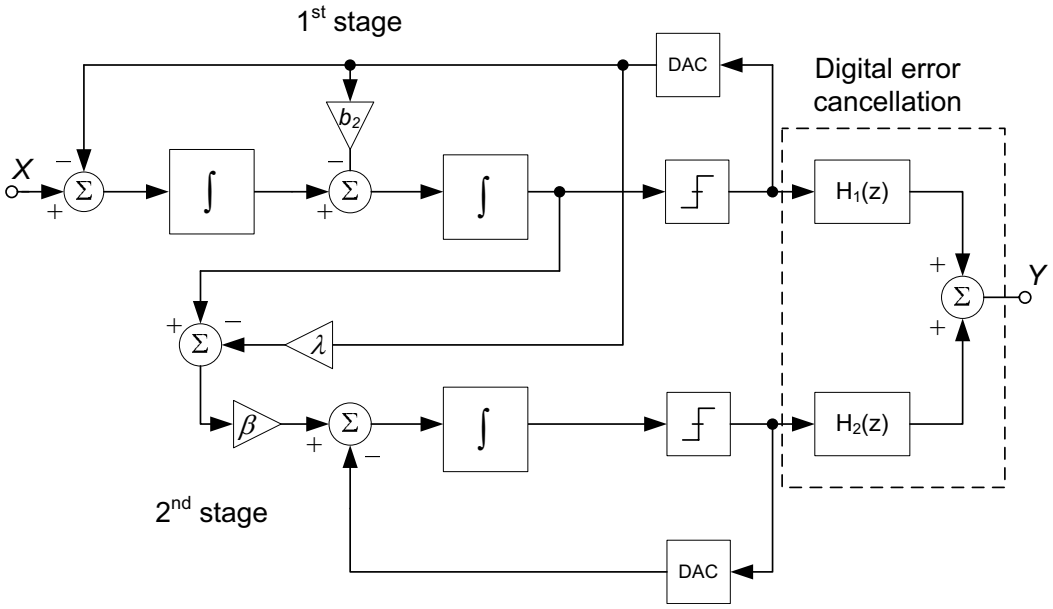


Figure 3.7: 2-1 MASH ΣΔ A/D converter.

second stage provides extra resolution, but the additional resolution achievable is subject to integrator coefficient matching [47]. The digital error cancellation logic is given by [47]

$$H_1(z) = z^{-1} - (1 - \hat{\lambda})(1 - z^{-1})^2 z^{-1} \tag{3.8}$$

and

$$H_2(z) = \frac{1}{\hat{\beta}}(1 - z^{-1})^2 \tag{3.9}$$

For perfect noise cancellation, the $\hat{\lambda}$ and $\hat{\beta}$ in digital domain must match the λ and β in analog domain. Digital calibration [51] can be employed to achieve better matching if needed. The dynamic range of the 2-1 MASH ADC is

$$DR = 10 \cdot log(\frac{21\beta^2 M^7}{2\pi^6}) \tag{3.10}$$

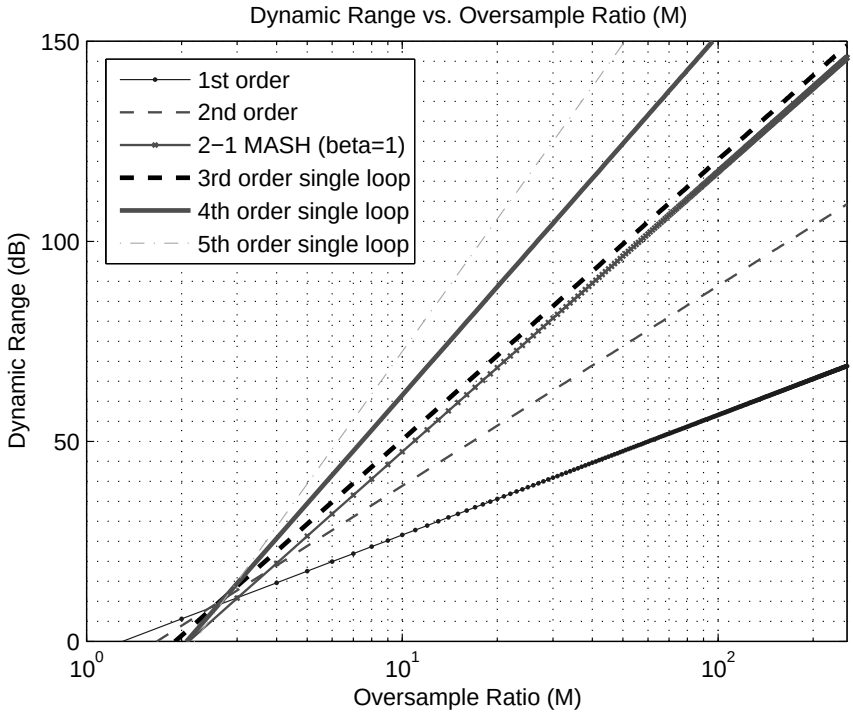


Figure 3.8: Dynamic range vs. oversampling ratio (M).

in dB. The dynamic range increases by 21dB with doubling the oversampling ratio M. The stability of the 2-1 MASH $\Sigma\Delta$ is guaranteed because there is no feedback signal from the second stage to the first stage and second-order and first-order loops are inherently stable.

As discussed above, there are many different types of sigma-delta A/D converters, ranging from first-order and higher-order single-loop topologies to cascaded architecture. The complexity increases as the order of noise-shaping increases. Figure 3.8 plots the dynamic range versus the oversampling ratio (M) of different types of $\Sigma\Delta$ converters.

3.10 Conclusion

Properties of different kinds of high-precision converters, namely integrating, algorithmic, successive approximation and oversampling converters have been analyzed. Integrating ADCs suffer from very slow conversion rate. Successive approximation converters usually need a high-precision DAC that requires either calibration or trimming, which is costly. A very high-gain op-amp is typically required to implement the DAC for a very high-resolution successive approximation ADC. An algorithmic ADC demands a very precise gain-of-two stage that requires a high-gain op-amp and good analog component matching. An algorithmic ADC has been used in [10] as a reference ADC to calibrate a pipelined ADC, but the algorithmic ADC requires calibration itself. In contrast, a $\Sigma\Delta$ ADC does not require very precise analog components and is very insensitive to matching. In addition, a 1-b $\Sigma\Delta$ ADC is inherently linear, which is highly desired as a reference ADC. In conclusion, $\Sigma\Delta$ ADC architecture is the most suitable converter for our application.

Chapter 4

Design of ΣΔ A/D Converter

4.1 Introduction

The primary target is to design a highly linear 14-b sigma-delta (ΣΔ) ADC operating at 1.2V supply voltage. From the previous chapter, considering the complexity and resolution, the second-order and the 2-1 MASH ΣΔ ADCs are the most viable candidates. This chapter investigates the performance of second-order and 2-1 MASH ΣΔ A/D converters. Simulink® models are constructed to evaluate the performance of both topologies. Then, a final ADC topology is chosen based on the comparisons of the second-order and the 2-1 MASH architecture. In the second half, circuit design issues such as integrator gain coefficient scaling, capacitor mismatch, integrator settling, and circuit noise are considered.

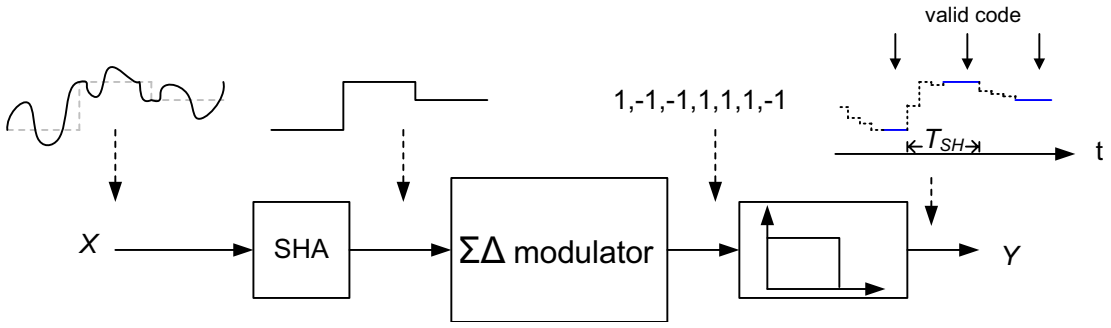


Figure 4.1: Operation of a ΣΔ ADC as a DC voltage.

4.2 ΣΔ ADC as a DC Voltmeter

As a reference path for the proposed ADC calibration, the usage of ΣΔ ADCs is different from the one used in a typical communication system receiver [52] where converters are interested in signals in the signal bandwidth; the ΣΔ ADC acts as a DC voltmeter instead, i.e., it is only interested in DC signals. Therefore, a dedicated front-end sample-and-hold amplifier (SHA) is required to hold the sampled signal for ΣΔ ADC conversion. Figure 4.1 shows the detailed operation of the ΣΔ ADC. Signals at different building blocks are also annotated in the figure. During the hold phase of the SHA, the ΣΔ ADC converts the DC signal to digital code. The converter does not care the signal before and after the current sample. As a result, aliasing is not a problem in this application, although the SHA is sub-sampling the analog signal. The transient response of the decimator is also shown in the figure. In order to get one valid sample, we need to wait until the transient response of the decimator dies down.

4.3 Reference ADC Architecture

In the proposed LMS calibration scheme, since the pipelined A/D converter consumes most of the total chip power, the power consumption of the ΣΔ A/D converter is not the most important factor in deciding the architecture. In addition, in order to facilitate the design of finite impulse response (FIR) decimation filter, an oversampling ratio in multiples of two is desirable. Considering the design complexity and the dynamic range with a reasonable oversampling ratio (<256) limited by the technology, second-order single-loop and 2-1 MASH ΣΔ A/D converters are the most promising candidates. We can show that the oversampling ratio (M) has to be at least 64 and 128 for a second-order converter and a 2-1 MASH ΣΔ A/D converter respectively. The following sections compare the performance of a second-order and a 2-1 MASH converters.

4.3.1 Second-Order ΣΔ Architecture

A conventional second-order ΣΔ with $b_2 = 2$ has been shown Figure 3.6 in Chapter 3. It has been shown in [53] that $b_2 = 2.5$ gives better DC tone performance, but $b_2 = 2$ is used in the behavioral model for the second-order ΣΔ ADC. Due to the scaling of power supply in CMOS process to lower the power in digital circuits, the voltage swing of an integrator is very limited. Based on Figure 3.6 with $b_2 = 2$, we apply voltage scaling to lower the voltage swing at outputs of both integrators as illustrated in Figure 4.2 [43]. This voltage scaling does not modify the characteristics of the modulator because the gain of the comparator will be adjusted accordingly. With this voltage scaling, we can prevent the saturation of the integrators, which would result in large non-linearity. However, one

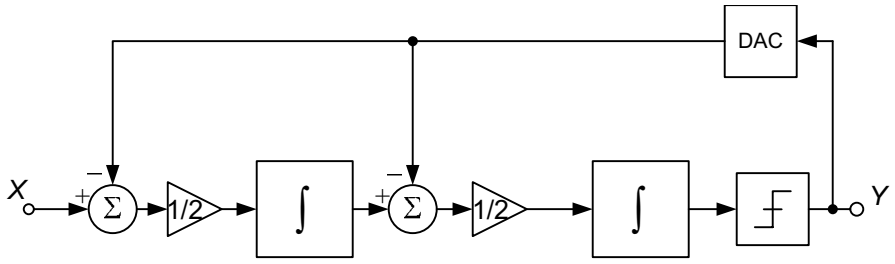


Figure 4.2: Second-order ΣΔ with scaled gain coefficients.

main drawback of the gain coefficient scaling is that the modulator's input-referred noise is increased by the scaling factors.

4.3.2 2-1 MASH ΣΔ Architecture

Basic architecture of a 2-1 MASH ΣΔ is shown in Figure 4.3. It is derived directly from cascading a second-order ΣΔ and a first-order ΣΔ. $\lambda = 1$, $\beta = 0.5$, and $b_2 = 2.5$ are used for behavioral simulation. In the next section, comparisons of the second-order and the 2-1 MASH ΣΔ ADCs are made through behavioral simulations.

4.4 Simulink Models of ΣΔ ADCs

In the Simulink model, gain, discrete filter and relay blocks model the gain coefficients, integrators and comparators respectively. Distortion analysis is not performed due to difficulty in modeling the circuit non-linearity in Simulink. Therefore, we will rely on transistor level simulations to obtain distortion information. Sampling noise and integrator input-referred noise are modeled by an equivalent noise source at the input of the ΣΔ modulator. Flicker noise is not included in the Simulink model. In the following sections, we

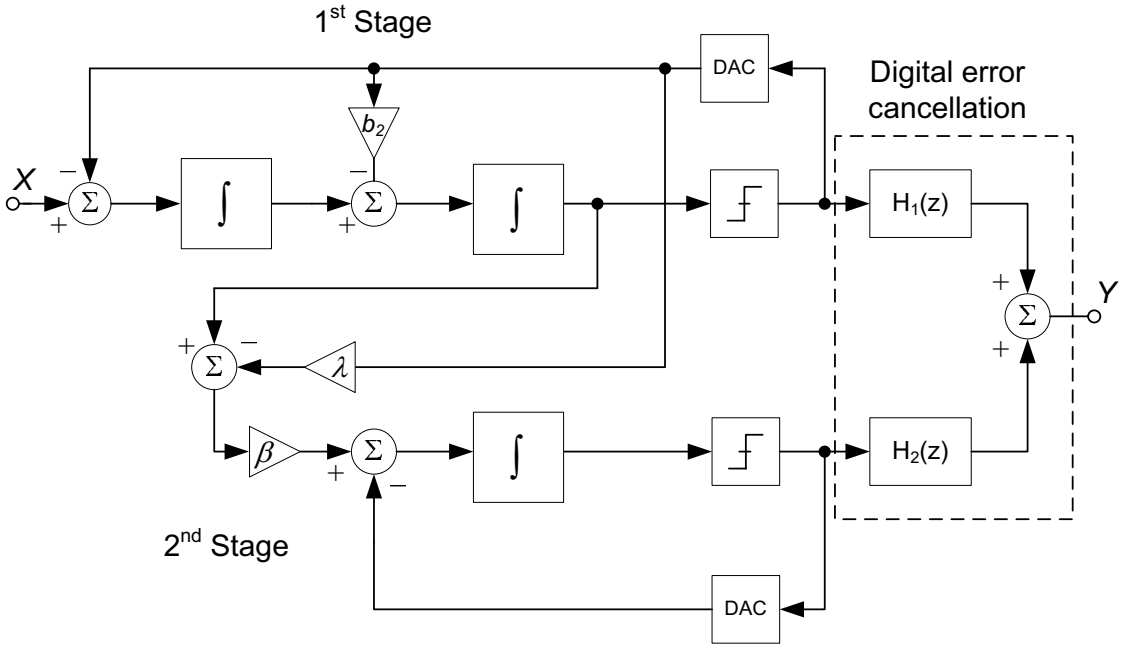


Figure 4.3: Block diagram of 2-1 MASH ΣΔ architecture.

will compare the second-order and the 2-1 MASH design with respect to the dynamic range, DC tones, power consumption, and finally the requirement of the finite impulse response (FIR) decimation filter.

4.4.1 Dynamic Range

This section presents simulation results from Simulink models. In simulations, white noise with variance of $(1/2\text{LSB})^2$ is injected at the input to model input-referred electronic noise. The output spectrum of a 750kHz input is plotted in Figure 4.4, where fast Fourier transform (FFT) analysis is done with windowing (Nuttall window). The sampling rate is 64MHz in the simulation. Figure 4.4(a) plots the spectrum of the second-order design, and Figure 4.4(b) shows the spectrum from the 2-1 MASH ΣΔ ADC. We observe

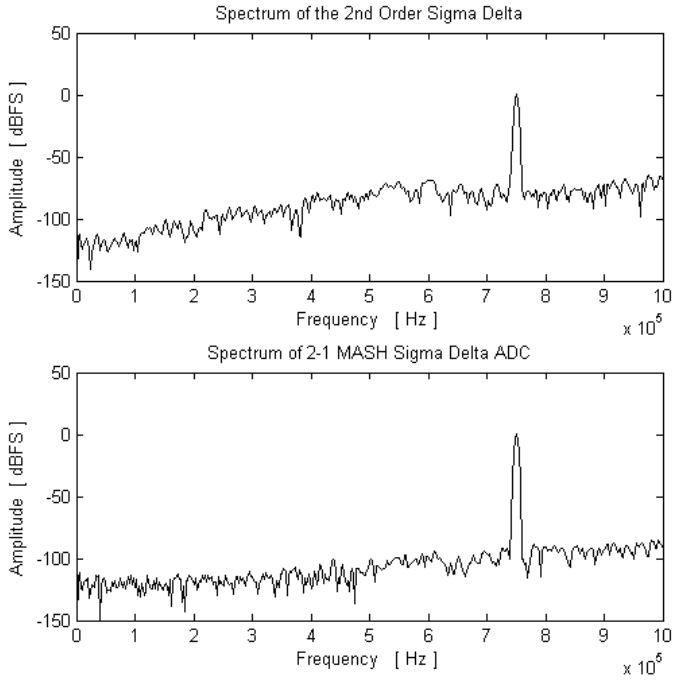


Figure 4.4: Output spectra of a 0dBFS 750 kHz sine wave: (a) second-order ΣΔ ADC, (b) 2-1 MASH ΣΔ ADC.

that noise floor of the 2-1 MASH modulator is lower than that of the second-order ΣΔ converter. Figure 4.5 shows the integrated noise from the second-order and the 2-1 MASH architecture. To achieve 14-bit accuracy, oversampling ratios (M) of the second-order and the 2-1 MASH architecture have to be at least 128 and 64 respectively. For the second-order architecture, the graph shows that the dynamic range is 85dB with $M = 128$. For the 2-1 MASH architecture, the dynamic range is 90dB with $M = 64$.

4.4.2 DC Tones and Dithering

DC tones are caused by the periodicity of the digital outputs from the 1-bit comparator with a DC input [53]. To understand the origin of these DC tones, one considers a

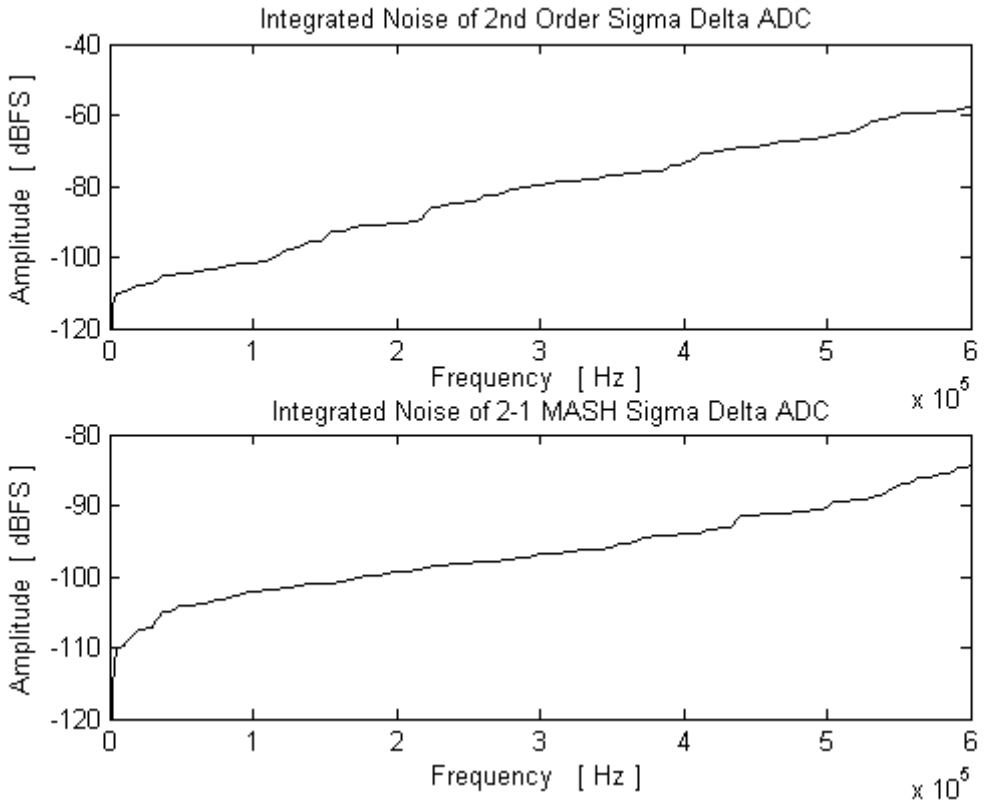


Figure 4.5: Integrated noise the second-order $\Sigma\Delta$ and the 2-1 MASH $\Sigma\Delta$ ADCs.

single-stage $\Sigma\Delta$ modulator with a 1-bit comparator output equal to ± 1. The feedback loop forces the average of the output to equal to the average of the input. For example, with a DC input of 0.001, the quantizer output will be a sequence of $+1$ and -1's, such that the running average is 0.001. Figure 4.6(a) shows the output pattern of the comparator with zero DC input. There are equal numbers of $+1$'s and -1's. In Figure 4.6(b), with a DC input of 0.001, there is an additional $+1$ in every 1000 cycles (T). This repetition of pattern produces a tone at a frequency of

$$f_{DC} = \frac{1}{1000T} = \frac{1}{1000} f_s. \tag{4.1}$$

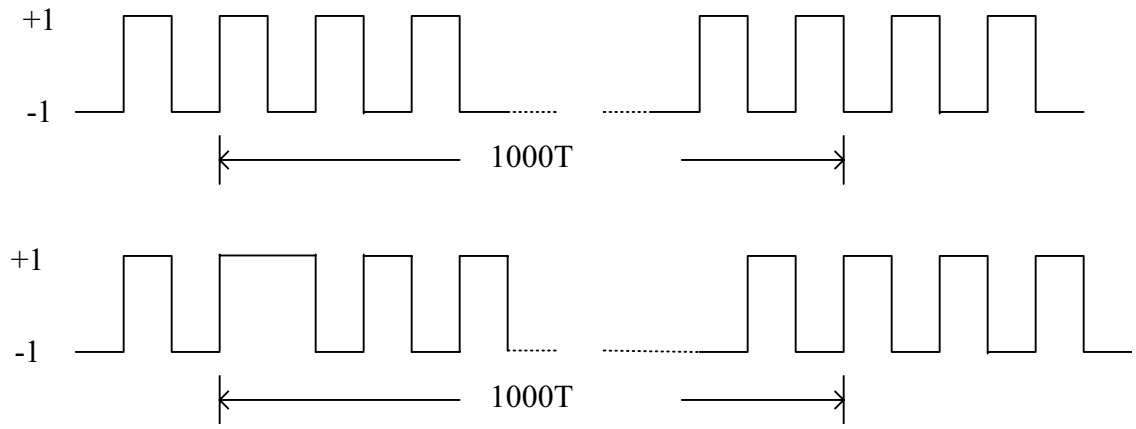


Figure 4.6: Output pattern of the comparator: (a) 0 DC input, (b) 0.001 DC input.

Additional noise can be added at the comparator input to randomize the output digital code from the comparator. Such process is called dithering, and thermal noise from the devices can be used in dithering. Thermal noise from electronic devices is modeled as a white noise at the modulator input in the Simulink model. The spectra of the second-order and the 2-1 MASH $\Sigma\Delta$ with a DC input with and without white noise are shown in Figure 4.7 and Figure 4.8, respectively. In Figure 4.7, DC tones are clearly visible. With a $30\mu {V_{rms}}^2$ $(1/2\text{LSB})^2$ input-referred random noise, although the DC tones are greatly reduced in both the second-order and the 2-1 MASH designs, the later exhibits better tone performance over the second-order design. DC tone performance is very important in our application because the converter is only interested in DC inputs. Thus, the 2-1 MASH architecture is superior to the second-order one.

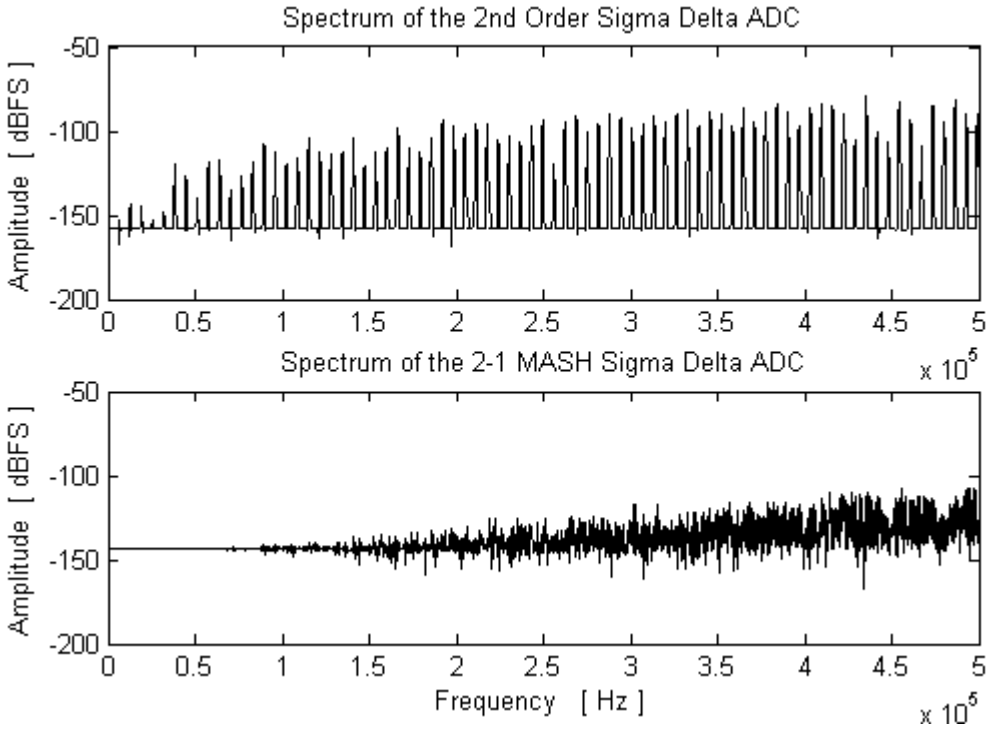


Figure 4.7: DC tones without circuit noise (8000-point FFT).

4.4.3 Power Consumption

For power estimation, it is assumed that electronic noise limits the converter resolution. The power of the modulator is given by

$$Power \propto \frac{1}{C_{total} \cdot M}. \tag{4.2}$$

The oversampling ratio does not affect the power dissipation because when the oversampling ratio is increased, the capacitor sizes can be decreased proportionally to maintain a constant noise level. The above analysis assumes parasitic capacitances are negligible. A 2-1 MASH $\Sigma\Delta$ architecture has an extra stage; however, the power consumption is minimal in this

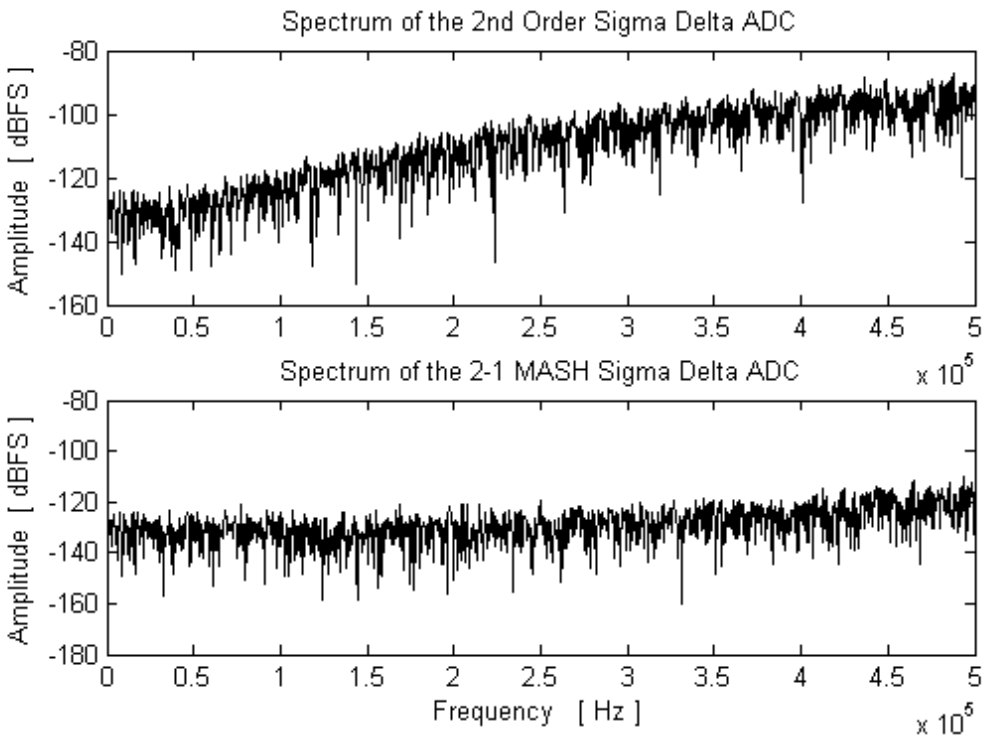


Figure 4.8: 0.001 DC input (8000-point FFT).

stage. This is because the input-inferred noise of the third integrator undergoing second-order noise-shaping, thus the capacitors of the third integrator can be very small. Therefore, power consumption in the 2-1 MASH ($M = 128$) and the second-order ($M = 64$) topologies is comparable.

4.4.4 Settling of Finite Impulse Response (FIR) Decimation Filter

The input signal of a conventional discrete-time $\Sigma\Delta$ A/D has to be band-limited in order to avoid aliasing. Thus, there is usually a low-pass filter preceding the A/D converter. However in our application, the $\Sigma\Delta$ is preceded by a sample-and-hold (S/H), so that the input signal is not band-limited, rather it is a step waveform as shown in Figure

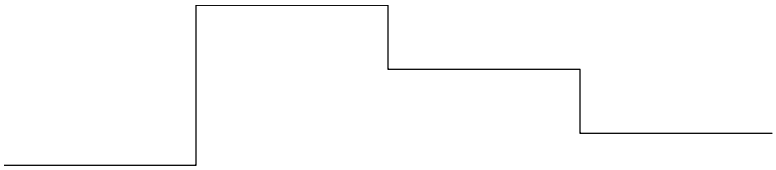


Figure 4.9: Sigma-delta A/D converter input waveform.

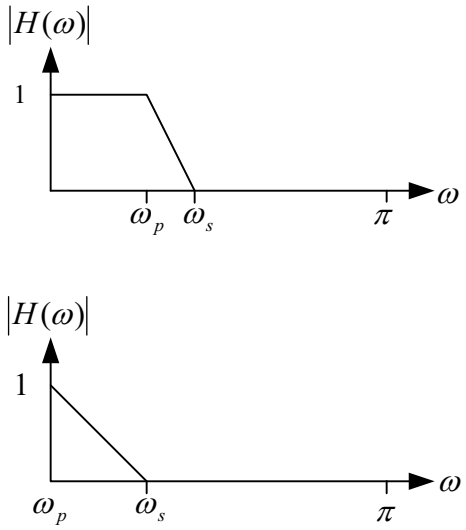


Figure 4.10: (a) Traditional decimation filter, (b) proposed decimation filter.

4.9. Since the input is a DC signal in a specific time period, the FIR decimation filter length should be kept as short as possible so as to reduce its transient response, resulting in a higher conversion rate. A conventional low-pass decimation filter is shown in Figure 4.10(a). Nevertheless, since the signal of our interest is DC, the pass-band can be put at much lower frequency as shown in Figure 4.10(b). The filter of a FIR filter (L) is given by [54]

$$L \propto \frac{1}{\omega_p - \omega_s} \tag{4.3}$$

where ω_p is the cutoff frequency and ω_s is the stop-band frequency. With the same sam-

pling rate for the second-order and the 2-1 MASH architecture, doubling the oversampling ratio doubles the filter length and the settling time for a direct implementation of digital filters. The transient response time determines the number of valid DC outputs per second achievable by the $\Sigma\Delta$ ADC. In calibrating the pipelined A/D converter, a faster conversion rate of the $\Sigma\Delta$ ADC decreases the convergence time of the LMS ADF. Thus, a low oversampling ratio is favorable. Simulink models are used to simulate the transient responses of FIR decimation filters for both converters. Decimation filters are constructed using the Simulink filter generation tool. Both decimation filters are implemented using two stages of low-pass decimation filters. For the second-order $\Sigma\Delta$, the digital code is first decimated by 64 and then by 2. For the 2-1 MASH $\Sigma\Delta$, the digital code is decimated by 8 in both stages. Figure 4.11 shows the transient response of the decimation filters. With a $0.5V_{FS}$ DC input, the error signal is plotted for both cases. The decimation filter for the second-order $\Sigma\Delta$ ADC requires 10μs to settle, but the decimation filter for the 2-1 MASH $\Sigma\Delta$ only requires 6μs to settle with a 64MHz clock. By no means we want to show optimized filters here. Both filters can be further optimized to reduce transient response by using different number of stages. The purpose of plotting the transient response is to verify that higher oversampling ratios requires a longer filter.

We have compared the dynamic range, DC tones issue, power consumption and FIR filter response of the second-order and the 2-1 MASH sigma-delta ADCs. The results are summarized in Table 4.1. The 2-1 MASH ADC achieves higher dynamic and better DC tone performance. In addition, its decimator also requires shorter time to settle to the desired value. The power consumption of both topologies is comparable. Therefore, the 2-1

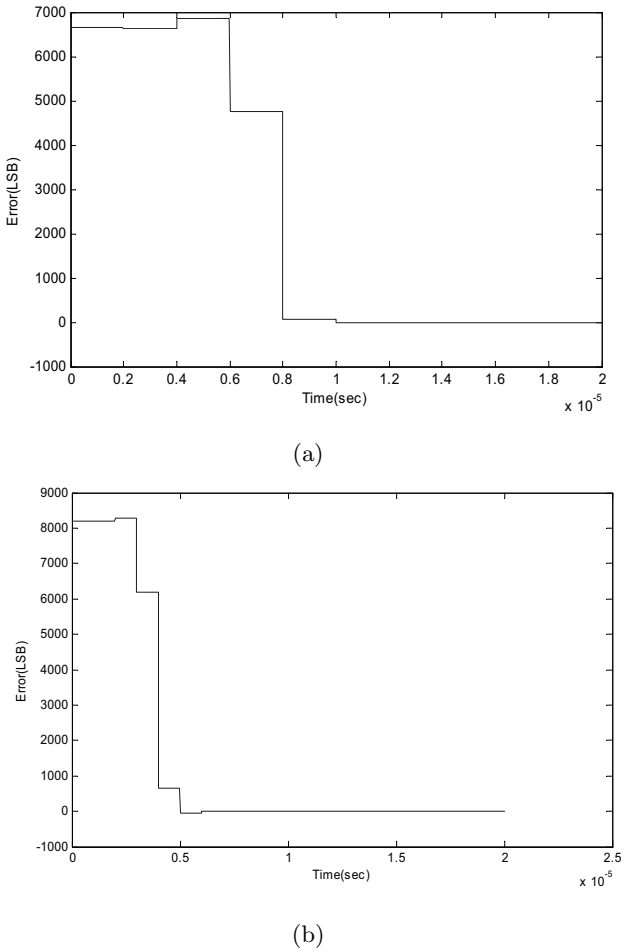


Figure 4.11: Transient response of decimation filters: (a) second-order ΣΔ ADC (14-b), (b) 2-1 MASH ΣΔ ADC (14-b).

MASH topology is better than the second-order topology. Following sections will discuss some design issues in 2-1 MASH ΣΔ ADCs.

4.5 Integrator Signal Scaling

To avoid overloading integrators, it is necessary to reduce gain coefficients of integrators in ΣΔ ADCs. To perform the scaling process, the block diagram in Figure 4.3 must

Table 4.1: Comparison of the second-order ΣΔ and the 2-1 MASH ΣΔ ADCs

	Second-Order	**2-1 MASH**
Dynamic Range	85dB	90dB
DC Tones	poor	good
FIR Decimation Filter req.	longer filter	shorter filter
Power	comparable	comparable

be mapped into an equivalent structure that can be implemented with switched-capacitor circuits as shown in Figure 4.12. To maintain equivalence, the gain coefficients must satisfy [53]:

$$b_2 = \frac{f_2}{f_1 a_2}, \tag{4.4}$$

$$\beta = \frac{f_1 a_2 a_3}{f_3}, \tag{4.5}$$

and

$$\lambda = \frac{a_4}{f_1 a_2 a_3}. \tag{4.6}$$

The next step is to tune the coefficients subject to the above constraints to limit the output swings of the integrators. This is accomplished by Simulink simulations. Since the output swings of the integrators are the largest with a large input, a step jumping from maximum positive input signal level to maximum negative signal is applied to the ADC. Gain coefficients are adjusted until all the integrator output swings are limited to 1.4 times of the full scaled input voltage. The final gain coefficients are shown in Table 4.2. Figure 4.13 shows the output swings of the integrators with the determined gain coefficients. Output swings of all integrators are below 1.4× the full-scale input voltage.

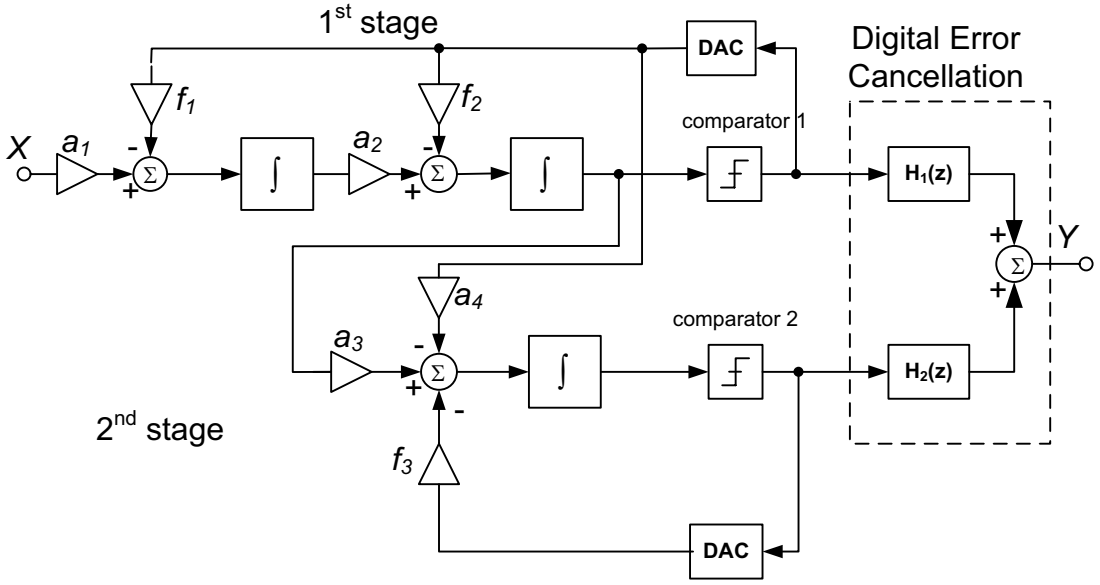


Figure 4.12: Block diagram of a 2-1 MASH $\Sigma\Delta$ with scaled gain coefficients.

Table 4.2: Gain coefficients of integrators

Gain Coefficients	**Value**
a_1	0.25
f_1	0.25
a_2	0.4
f_2	0.25
a_3	1
a_4	0.1
f_3	0.2

4.6 Thermal Noise

Thermal noise places the fundamental limit on power dissipation and dynamic range of a $\Sigma\Delta$ modulator. Dynamic range, including quantization noise, thermal noise, and flicker noise is given by

$$DR = \frac{V_{pk}^2}{2(S_{N,th} + S_{N,Q} + S_{N,1/f})} \tag{4.7}$$

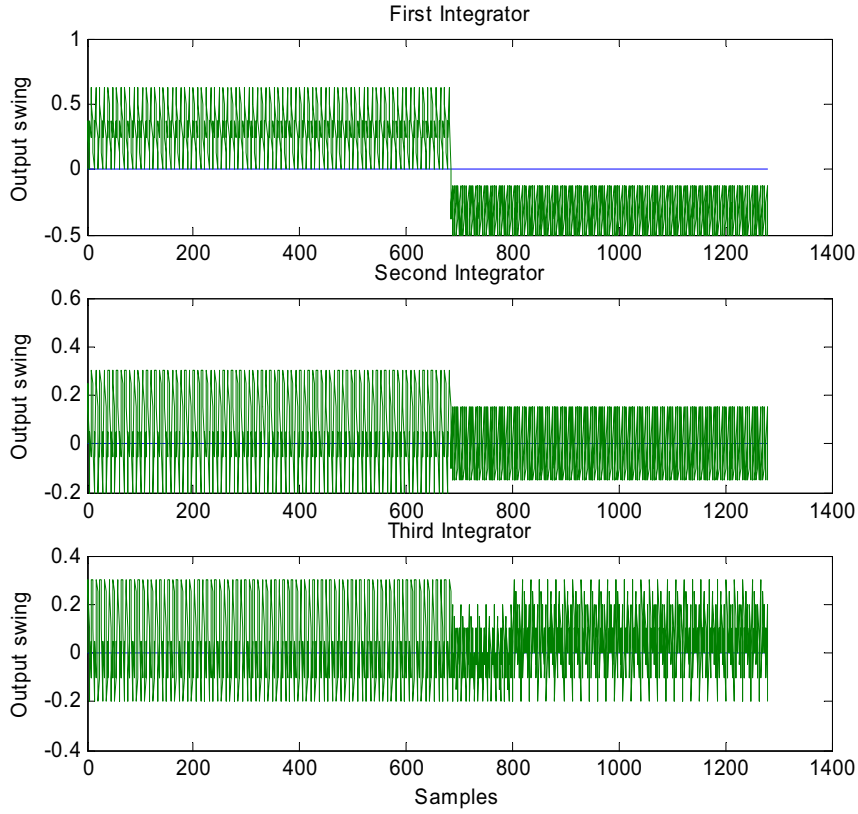


Figure 4.13: Output swings of integrators.

where $S_{N,th}$, $S_{N,Q}$, and $S_{N,1/f}$ denote thermal noise, quantization noise and flicker noise respectively. Thermal noise of a transistor can be represented by a voltage noise source at the gate by

$$\overline{V_{thermal}^2} = \frac{4kT\gamma}{g_m} \tag{4.8}$$

where k is Boltzmann's constant and γ is a technology dependent constant. γ is 2/3 for long channel devices. At room temperature, $4kT = 1.66 \times 10^{-20}$ V-C. Since a switched-capacitor $\Sigma\Delta$ A/D converter is a sampled-data system, there is also sampling noise from the sampling network in addition to the circuit noise from the amplifier. A differential switched-capacitor

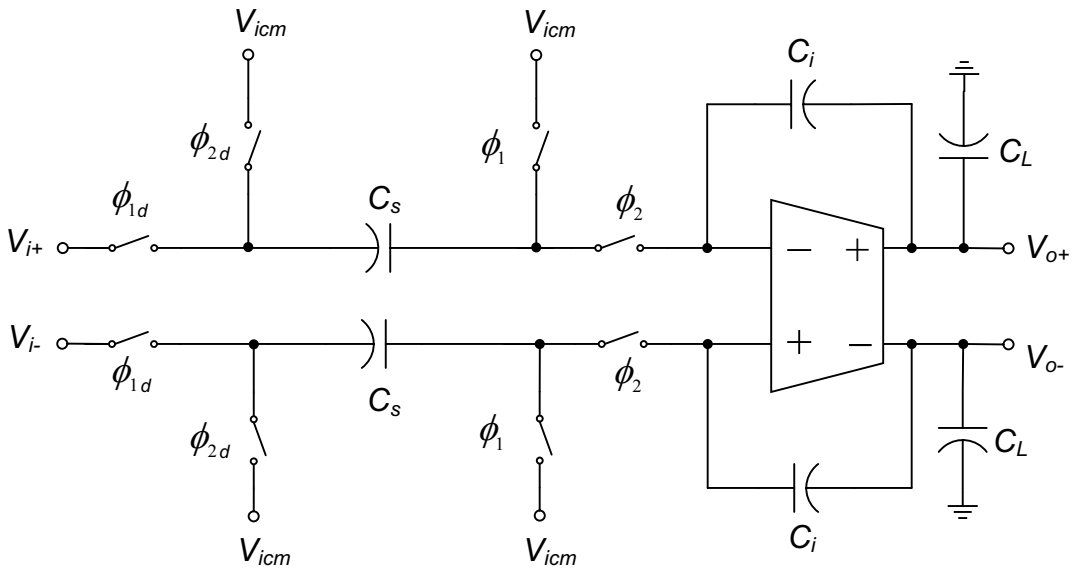


Figure 4.14: Switched-capacitor integrator.

integrator is shown in Figure 4.14. The sampling noise power is given by [51]

$$\overline{V_{N,sample}^2} = \frac{4kT}{C_s} \tag{4.9}$$

where C_s is the sampling capacitor. The input-referred noise spectrum of the amplifier is given by [55]

$$\overline{V_{N,amp}^2} = \frac{4kT\gamma}{g_m}(1 + n_f) \tag{4.10}$$

where n_f is a noise factor that depends on a specific amplifier topology.

4.7 Flicker Noise

Flicker noise is caused by the trapping and releasing of carriers at the gate oxide and channel interface. It is concentrated at low frequency and has a $1/f$ frequency depen-

dence. Flicker noise of a single transistor can be represented by a voltage source in series with the gate with value

$$\overline{V_{1/f}^2} = \frac{K_f}{WLC_{ox}f} \tag{4.11}$$

where K_f is a process dependent constant. Since PMOS transistors have smaller flicker noise than NMOS transistors, PMOS-input amplifier is preferred for low noise application. Circuit techniques such as chopper stabilization [56] and correlated double sampling [52] can attenuate flicker noise. From (4.11), flicker noise is inversely proportional to the transistor area. Thus, we rely on large transistors areas to reduce flicker noise without increasing circuit complexity.

4.8 Effects of Circuit Noise

After examining at the electronic noise sources, the effects of circuit noise to $\Sigma\Delta$ ADC is investigated. For simplicity, a schematic of a single ended switched-capacitor integrator is shown in Figure 4.15. V_n is the input-referred noise voltage of the amplifier. We can use charge conservation analysis to find input-referred noise of the switched-capacitor integrator due to amplifier noise [57]. Assuming the input to be zero, at time $(n-1)T$ the total charge is

$$Q_a = V_{out}(n-1)C_i - V_n(n-1)C_i. \tag{4.12}$$

At time $(n-1/2)T$:

$$Q_b = V_{out}(n-1/2)C_i - V_n(n-1/2)C_i - V_n(n-1/2)C_s \tag{4.13}$$

Combining (4.12) and (4.13),

$$Q_a = Q_b \Longleftrightarrow V_{out}(n-1)C_i - V_n(n-1)C_i = V_{out}(n-1/2)C_i - V_n(n-1/2)C_i - V_n(n-1/2)C_s \tag{4.14}$$

From time $(n-1/2)T$ to time nT, the charge on C_i is conserved, thus

$$V_{out}(n-1/2)C_i - V_n(n-1/2)C_i = V_{out}(n)C_i - V_n(n)C_i \tag{4.15}$$

Substituting (4.15) into (4.14), we have

$$V_{out}(n-1)C_i - V_n(n-1)C_i = V_{out}(n)C_i - V_n(n)C_i - V_n(n-1/2)C_s \tag{4.16}$$

The z-domain transfer function becomes

$$V_{out}(z) = V_{n,\phi 1}(z) + V_{n,\phi 2}(z)\frac{\frac{C_s}{C_i}z^{-1/2}}{1-z^{-1}} \tag{4.17}$$

where $V_{n,\phi 1}(z)$ is noise contribution in ϕ_1 and $V_{n,\phi 2}(z)$ is noise contribution in ϕ_2. When the noise is referred to the integrator input,

$$V_{n,in}(z) = V_{n,\phi 1}(z)\frac{1-z^{-1}}{\frac{C_s}{C_i}z^{-1}} + V_{n,\phi 2}(z)z^{+1/2} \tag{4.18}$$

The first term in (4.18) is negligible with a high oversampling ratio because it is under first-order noise-shaping. For a differential switched-capacitor integrator, the total input-referred

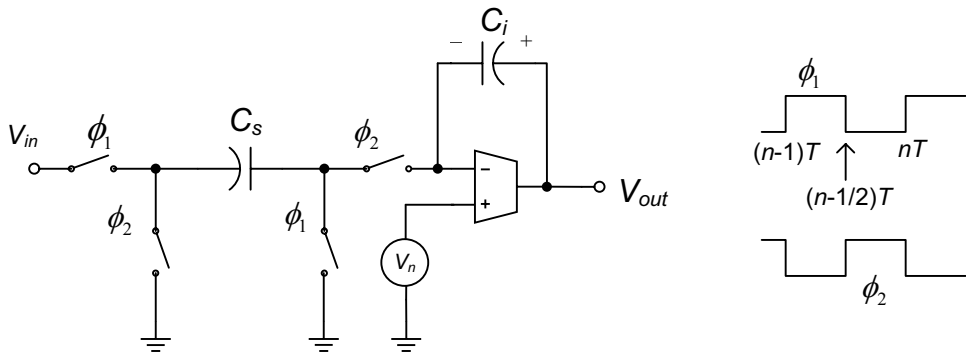


Figure 4.15: Single-ended switched-capacitor integrator with OTA noise.

noise power including sampling noise is approximated by

$$\overline{V^2_{n,in,int,total}} = \overline{V^2_{n,in,total}} + \frac{4kT}{C_s} \tag{4.19}$$

After finding the input-inferred noise of an integrator, we can calculate the $\Sigma\Delta$ modulator input-referred noise power, which is given by,

$$S_{N,electronic} = \frac{S_{N1}}{M} + \frac{\pi^2}{3a_1^2M^3}S_{N2} + \frac{\pi^4}{5a_1^2a_2^2M^5}S_{N3} \tag{4.20}$$

where S_{Nn} is the input-referred noise of the n-th integrator including sampling noise. We observe from (4.20) that noise from the second and third integrator undergoes first-order and second order noise-shaping respectively. (4.20) will be used to determine the size of capacitors.

4.9 Matching of λ, β in 2-1 MASH $\Sigma\Delta$ ADCs

Apart from electronic noise, another important issue in designing MASH $\Sigma\Delta$ ADCs is gain coefficient matching, which does not exist in single-loop $\Sigma\Delta$ ADCs. The block diagram of the 2-1 MASH $\Sigma\Delta$ has been shown in Figure 4.3. Variations in the CMOS processing cause mismatch between λ, β and $\hat{\lambda}$, $\hat{\beta}$ and result in imperfect cancellation of quantization noise from the first stage. Let

$$\beta = \hat{\beta}(1 + \Delta_\beta) \tag{4.21}$$

and

$$\lambda = \hat{\lambda}(1 + \Delta_\lambda) \tag{4.22}$$

The transfer function of the ADC is approximately given by

$$Y(z) = X(z)z^{-3} - \Delta_\beta(1 - z^{-1})^2 z^{-1} E_{Q1}(z) + \frac{1}{\hat{\beta}}(1 - z^{-1})^3 E_{Q2}(z) \tag{4.23}$$

where E_{Q1} and E_{Q2} are quantization noise from the first and the second comparators in Figure 4.3 respectively. Since λ and Δ_λ would only show up in higher-order terms in (4.23), it is not critical to the design. The second term of (4.23) indicates that the quantization noise of the first comparator is leaked to the output. However, the leaked noise is under first-order noise-shaping. The resulting noise power is given by

$$S_{mismatch} = \Delta_\beta^2 \frac{\pi^4}{5M^5}\sigma_{Q1}^2 + \frac{1}{\hat{\beta}^2}\frac{\pi^6}{7M^7}\sigma_{Q2}^2. \tag{4.24}$$

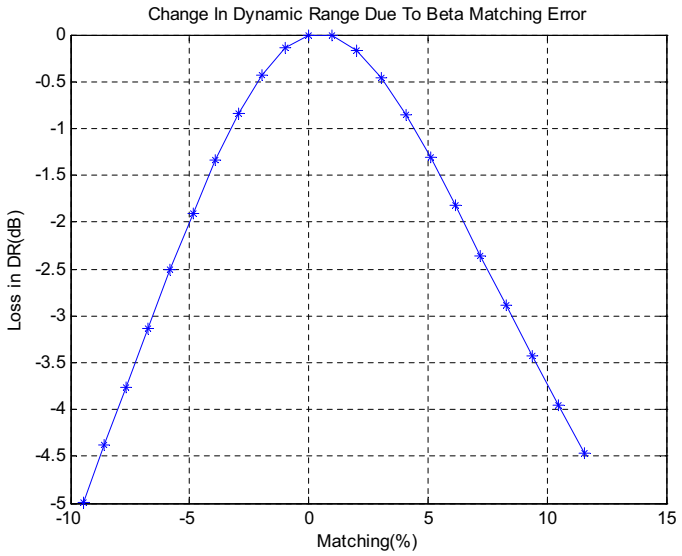


Figure 4.16: Dynamic range degradation due to β mismatch.

For 1dB degradation in dynamic range:

$$\Delta_\beta < \sqrt{\frac{5(10^{0.1}-1)}{7}}\frac{\pi}{\hat{\beta}M} \tag{4.25}$$

Considering only quantization noise, Figure 4.16 shows the effect of mismatch to dynamic range degradation. It shows that a 2% mismatch results in less than 1dB dynamic range degradation . From (4.5), β depends on four gain coefficients that in turn depend on capacitor matching. On the other hand, since our dynamic range is limited by the electronic noise, the actual degradation in dynamic range will be mush less.

4.10 Amplifier DC Gain

The transfer function of a switched capacitor integrator is never ideal. Integrators suffer from leakage due to finite amplifier DC gain. The transfer function of a leaky switched-capacitor integrator with finite DC gain (ADC) can be modeled as

$$H_{int}(z) = \frac{\frac{C_s}{C_i} z^{-1}}{1-(1-\epsilon)z^{-1}} \tag{4.26}$$

where ϵ equals $1/A_{DC}$ for an unity gain integrator and A_{DC} is the amplifier DC gain. With the integrator model in (4.26), after some manipulations, the transfer function of the 2-1 MASH $\Sigma\Delta$ A/D converters is given by [47]

$$Y(z) = z^{-3}X(z) + z^{-2}[(1-z^{-1})(\epsilon_1+\epsilon_2) + z^{-1}\epsilon_1\epsilon_2]E_{Q1}(z) + \frac{1}{\hat{\beta}}[(1-z^{-1})^3 + (1-z^{-1})^2\epsilon_3]E_{Q2} \tag{4.27}$$

where ϵ_1 , ϵ_2, and ϵ_3 are leakage of integrators. From (4.27), we can calculate the leakage power, which is given by

$$S_{leakage} = [\frac{\epsilon_1\epsilon_2}{M} + (\epsilon_1+\epsilon_2)^2\frac{\pi^2}{3M^3}]\sigma_{Q1}^2 + \frac{1}{\hat{\beta}}[\epsilon_3^2\frac{\pi^4}{5M^5} + \frac{\pi^6}{7M^7}]\sigma_{Q2}^2 \tag{4.28}$$

where M is the oversampling ratio, σ_{Q1}^2 and σ_{Q2}^2 together are the quantization noise power from the first and the second comparator in Figure 4.3. With a dynamic range degradation of 1dB,

$$(\epsilon_1+\epsilon_2)^2 \leq \frac{3(10^{0.1}-1)}{7}\frac{\pi^4}{\hat{\beta}^2 M^4} \tag{4.29}$$

$$\Longrightarrow (\epsilon_1 + \epsilon_2) \leq \sqrt{\frac{3(10^{0.1}-1)}{7}}\frac{\pi^2}{\hat{\beta}M^2} < 0.0016 < \frac{1}{622} \tag{4.30}$$

$$\epsilon_3 \leq \sqrt{\frac{5(10^{0.1}-1)}{7}}\frac{\pi}{M} = 0.0211 \approx \frac{1}{47} \tag{4.31}$$

Therefore, the total gain of the first and second amplifier must be at least 622, and the minimum gain of the third amplifier is 47.

4.11 Amplifier Settling

With the size of capacitors fixed by the thermal noise requirement, the settling requirement of the amplifiers will determine the power consumption. An integrator operating in integrating phase is illustrated in Figure 4.17. Assuming a single dominant pole, the unity gain frequency (f_u) has value [55]

$$f_u = \frac{G_m}{C_L + (1-F)C_s} \tag{4.32}$$

where

$$F = \frac{C_i}{C_s + C_i}. \tag{4.33}$$

In time domain, the output voltage is given by

$$V_o(t) = V_{o,ideal}(1 - e^{-2\pi F f_u t}) \tag{4.34}$$

Incomplete linear settling translates in linear gain error of the integrator, which is tolerable by $\Sigma\Delta$ A/D converters [22]. Nevertheless, linear settling is never guaranteed due to the

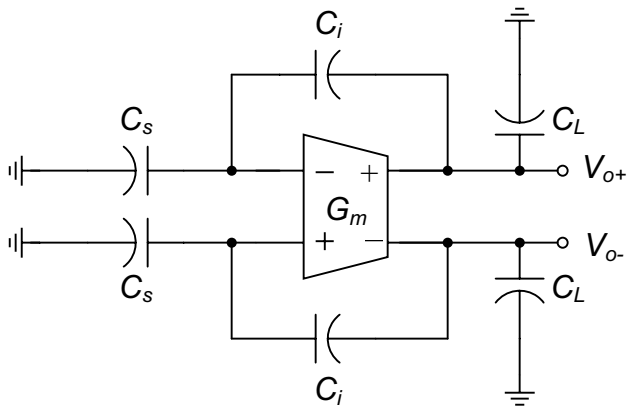


Figure 4.17: Integrator configuration during integrating phase.

presence of parasitic capacitances. Therefore, amplifiers are designed complete settling.

4.12 Conclusion

Comparisons of a second-order and a 2-1 MASH ΣΔ A/D converter have been presented. The 2-1 MASH architecture has lower quantization noise, better DC tone performance, and higher conversion rate. The 2-1 MASH ΣΔ A/D converter is chosen for our application for its superior performance. In addition, analog circuit design issues are presented in the second half of this chapter. These issues are finite op-amp output swings, electronic noise, finite op-amp DC gain, and integrator coefficient matching. Through analysis and simulations, the oversampling ratio (M) has been determined to be 64. The gain coefficients of the integrators have been finalized. The minimum op-amp DC gains with an additional margin should be at least 1000. In the next chapter, we will present the circuit design of the 2-1 MASH ΣΔ ADC.

Chapter 5

Circuit Implementation of ΣΔ A/D Converter Prototype

5.1 Introduction

This chapter describes circuit building blocks used in the 2-1 MASH ΣΔ ADC. The ΣΔ ADC is intended to run at 64 MHz with $M = 64$. Switched-capacitor circuits, which are very robust and tolerant to clock jitter compared with continuous time circuits, are commonly used in implementing high-resolution ΣΔ ADCs [58]. Thus, integrators are implemented with switched-capacitor circuits. The ΣΔ ADC will be fabricated in 0.13μm CMOS process with inter-digitated finger capacitors (CMOM) [59] and with a supply voltage of 1.2V. All building blocks are fully-differential circuits. Fully-differential architecture provides high rejection ratios from power supply, signal coupling, substrate

noise, and switch charge injection error. [1]

5.2 Switched-Capacitor Integrators

The main challenge in designing a $\Sigma\Delta$ ADC is building high speed and moderately accurate integrators. To ensure adequate performance amid process variations and device modeling inaccuracy, a margin has been added in addition to the minimum requirements.

The schematic of the modulator is shown in Figure 5.1. It contains three integrators, two comparators, and two 1-bit DACs. During phase 1 (ϕ_1), all the integrators either sample the preceding integrator output signal or the ADC input. During phase 2 (ϕ_2), the integrators sample the signals from 1-bit DACs. The integrators are designed to run at 64MHz so that the amplifiers have to settle completely within less than 8ns.

5.2.1 First Integrator

Requirements for the first integrator are the most stringent; signals after the first integrator are noise-shaped, thus, relaxing the design requirements for the following circuitry. In contrast, the input-referred noise (error) of the first integrator does not undergo any noise-shaping and adds directly to the input signal. Figure 5.2(a) and Figure 5.2(b) show the schematic of the first integrator and the clock waveforms respectively. A non-overlapping clocking scheme is used to reduce switch charge injection. During phase 1 (sampling phase), the top plates of the sampling capacitors (C_{s1}) are first connected to the amplifier input common-mode voltage (V_{icm}), which is at 0.5V. After a short delay,

[1] In all the schematics, bodies of NMOS and PMOS transistors that are without explicit connections are tied to *VDD* and *GND* respectively. The positive terminal is denoted with $'p'$ or $'+'$ and the negative terminal is denoted as $'n'$ or $'-'$. The delayed version of a clock signal ϕ_1 is denoted as ϕ_{1d}.

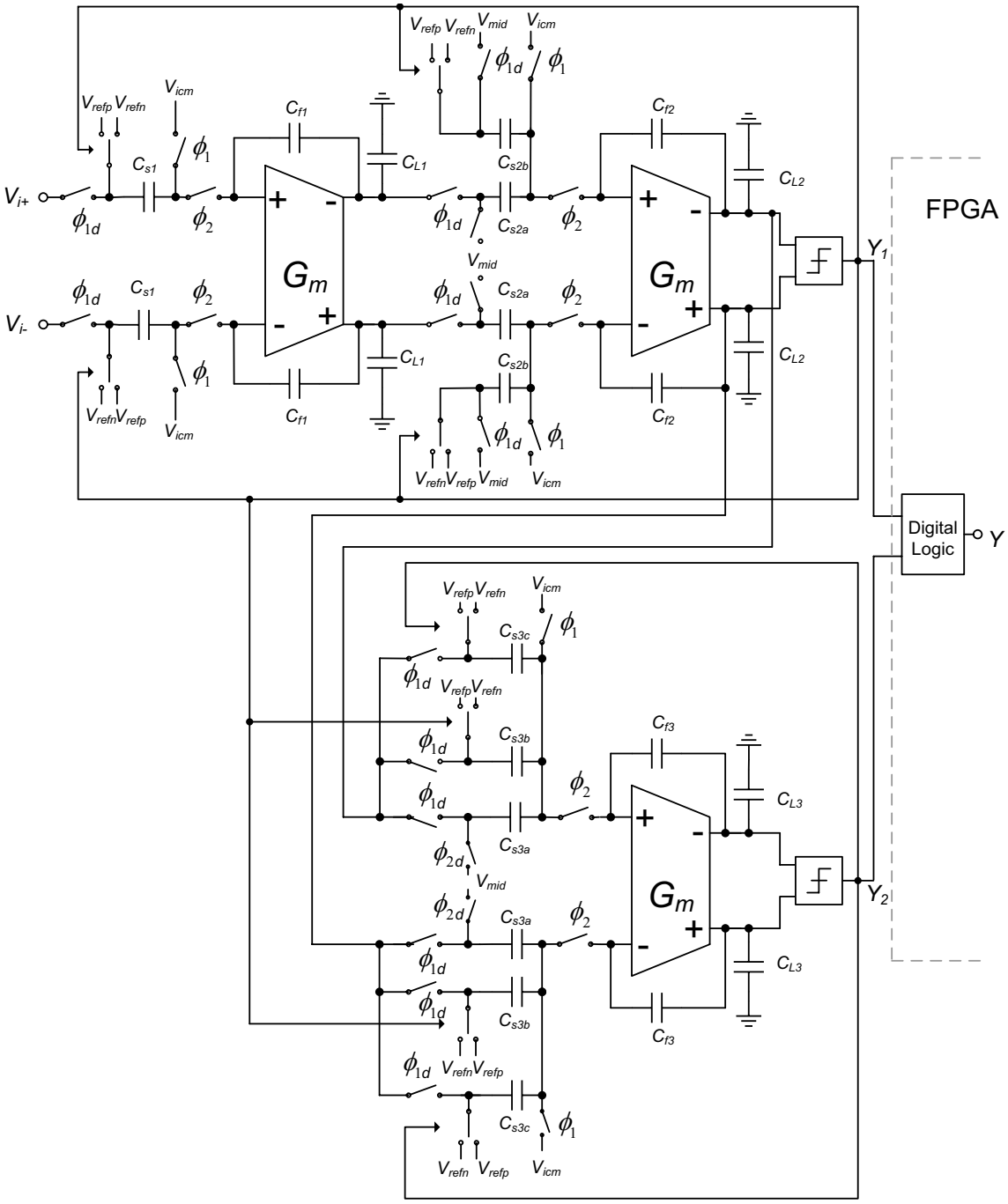


Figure 5.1: Schematic of the 2-1 MASH ΣΔ ADC.

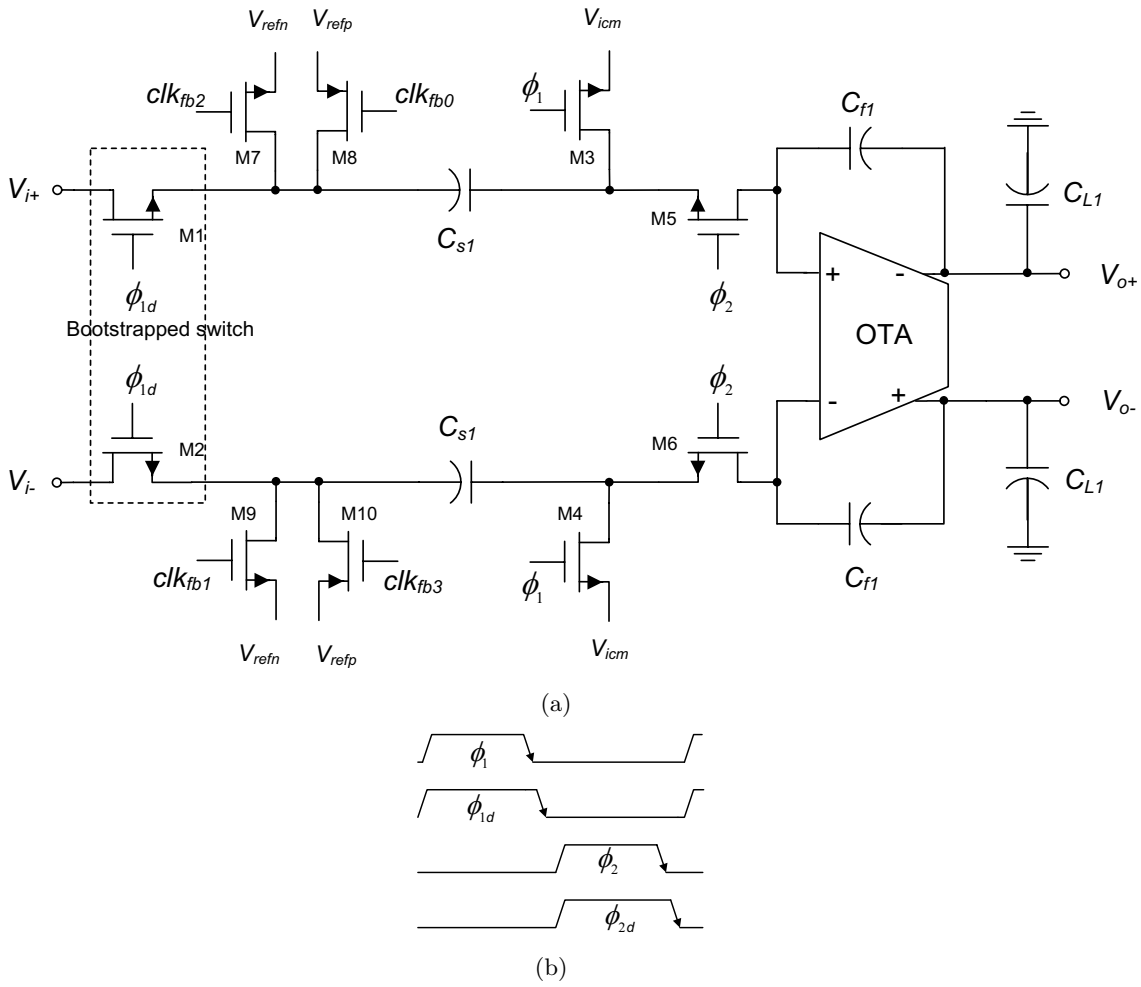


Figure 5.2: (a)Schematic of first integrator, (b)its clock waveform.

sampling switches M1 and M2 are switched on to track the input signal. At the end of phase 1 (sampling phase), M3 and M4 are turned off before opening switches M1 and M2 in order to prevent channel charge injection from M1 and M2. Although we avoid the charge injection from M1 and M2, we still experience the switch charge injection from M3 and M4 when turning off. Charge injection from transistors M3 and M4 depends upon the impedance they see at their source and drain terminals. However, BSIM3 device modeling

models 50%-50% split of channel charge in the source and drain terminals.

During phase 2 (integrating phase), M5 and M6 are turned on first. Depending on the comparator output, either V_{refp} or V_{refn} is fed to the sampling capacitors. At the end of phase 2, transistors M5 and M6 are turned off before opening transistors M7-M10 if they are not originally open. The sizes of transistors M3-M6 are small because amplifier virtual ground nodes are positioned at a voltage very close to the OTA common-mode input voltage (V_{icm}) at both phases. Small transistors keep the charge injection from transistors M3-M6 at minimal. With 1.2V supply voltage, bootstrapping the sampling switches is necessary in order to keep the on-resistance low with a reasonable switch size. Thus, switches M1 and M2 are bootstrapped switches to reduce non-linearity and to increase sampling speed [60]. Furthermore, by bootstrapping the sampling switches, we can avoid using any large PMOS sampling switch, whose parasitic capacitance loads the input significantly. Table 5.1 and Table 5.2 list the sizes of the switches and the sizes of the capacitors respectively. Since 0.13μm is at the limit of the lithography process in 0.13μm CMOS process, any physical dimension of 0.l3μm is not very well controlled. Thus, channel length (L) of 0.14μm is used in our design for better matching. The capacitor sizes are determined using (4.20) because electronic noise level sets capacitor sizes. The sampling noise and input-referred noise of the first integrator add directly to the signal so the capacitors are the largest. In our design, 90% of the noise budget is allocated to first integrator; 9% and 1% of the noise budget are allocated to the second and third integrators respectively.

Table 5.1: First integrator transistor sizes.

Transistors	Type	W (μm)	L (μm)
M1,M2	NMOS	89.60	0.14
M3,M4	NMOS	20.00	0.14
M5,M6	NMOS	20.00	0.14
M7,M9	NMOS	26.00	0.14
M8,M10	PMOS	88.92	0.14

Table 5.2: First integrator capacitor values.

Capacitors	Size (pF)
C_{s1}	1
C_{f1}	4
C_{L1}	3.5

5.2.2 Second Integrator

The schematic of the second switched-capacitor integrator is shown in Figure 5.3. The operation of the second integrator is very similar to the first one. Same non-overlapping clocking scheme as in the first integrator is used, and the switching sequence is also the same. The main difference is that the DAC feedback signal gain is not equivalent to the gain of the input. Thus, we have to use two separate capacitors for the input and the DAC feedback signal. CMOS sampling switches are used instead of the bootstrapped switches in the first integrator because any error at the input of the second integrator is attenuated by first-order noise-shaping $(1 - z^{-1})$. In addition, since noise contribution from the second integrator is smaller the capacitors are also smaller. Thus, we are able to save power in the second integrator with smaller capacitors. However, matching becomes worse for small capacitors. Therefore, larger capacitors are used. The common-mode input voltage of the OTA is maintained at 0.5V. Table 5.3 and 5.4 list the capacitor sizes and the switch sizes.

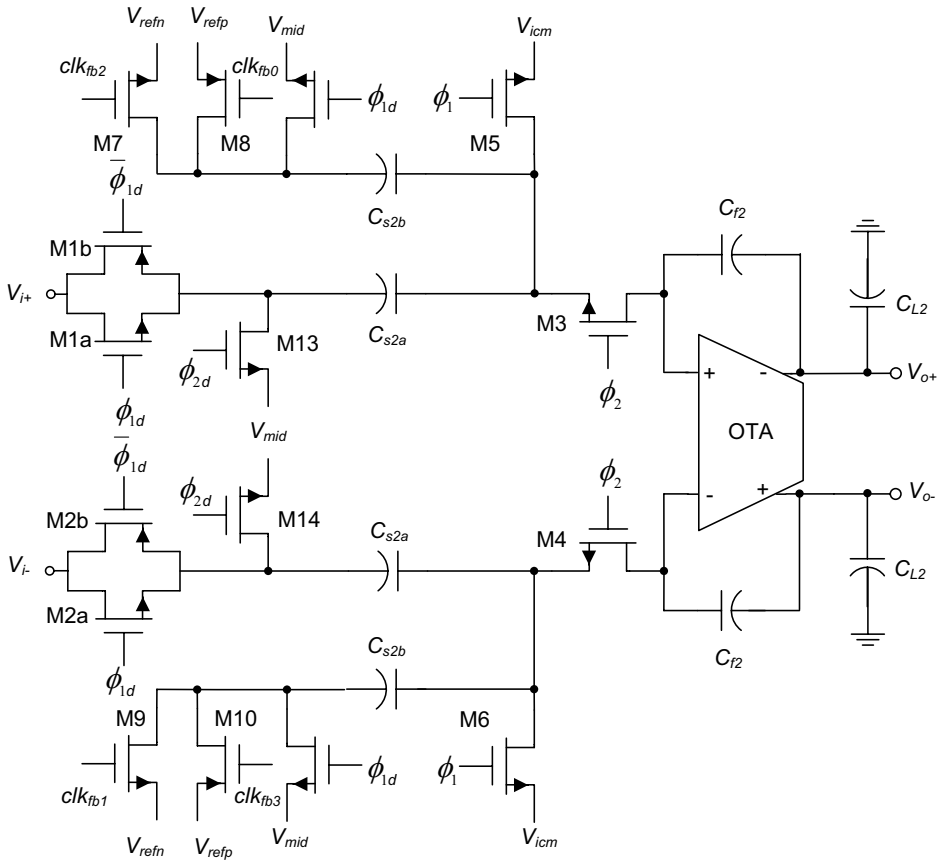


Figure 5.3: Schematic of second integrator.

5.2.3 Third Integrator

The third integrator has three inputs, which are the output of the second integrator and the outputs from both the first and the second DACs shown in Figure 5.4. The main input shares the sampling capacitors with the DACs instead of using three separate capacitors for three different inputs. This reduces loading from the sampling network to the OTA during integrating phase. Again, CMOS switches are used for the input. Common-mode input voltage and common-mode output voltage of the amplifier are kept at 0.5V and 0.6V respectively. The transistor sizes and the capacitor sizes are listed in Tables 5.5 and

Table 5.3: Second integrator transistor sizes.

Transistors	Type	W (μm)	L (μm)
M1a,M2a	NMOS	4.00	0.14
M1b,M2b	PMOS	13.68	0.14
M3,M4	NMOS	12.00	0.14
M5,M6	NMOS	3.00	0.14
M7,M9	NMOS	10.00	0.14
M8,M10	PMOS	34.20	0.14
M11,M12	NMOS	15.00	0.14
M13,M14	NMOS	2.00	0.14

Table 5.4: Second integrator capacitor values.

Capacitors	Size (fF)
C_{s2a}	160
C_{s2b}	100
C_{f2}	400
C_{L2}	900

5.6 respectively.

5.3 Operational Trans-conductance Amplifiers (OTAs)

This section describes the design of three operational trans-conductance amplifiers (OTAs). DC gain requirement of the OTAs has been discussed in Chapter 4. However, higher DC gain is desirable to suppress harmonic distortions. As a result of CMOS scaling, the voltage gain of a single transistor has dropped from generation to generation due to reduced output resistance, which is caused by changes to CMOS processing steps. In a general-purpose foundry 0.13μm process, the gain of a single transistor common source amplifier ($g_m r_o$) is in the order of 15-20dB. In order to achieve a DC gain of about 70dB, a gain on the order of $(g_m r_o)^4$ is required. Therefore, a folded-cascode amplifier with gain-boosting meets the requirement. The gain-boosting technique allows us to achieve high gain

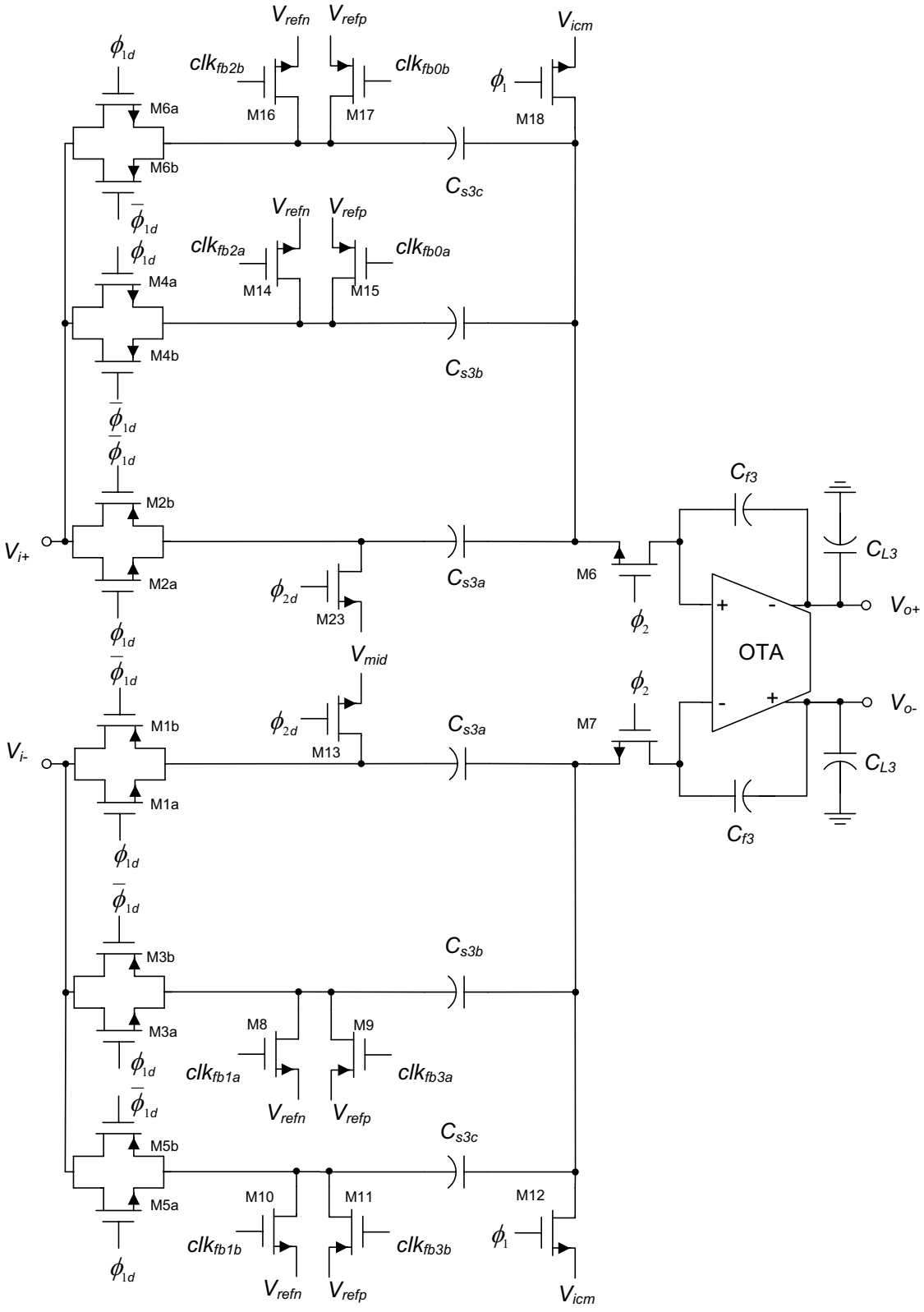


Figure 5.4: Schematic of third integrator.

Table 5.5: Third integrator transistor values.

Transistors	Type	W (μm)	L (μm)
M1a,M2a	NMOS	4.00	0.14
M1b,M2b	PMOS	13.68	0.14
M3a,M4a	NMOS	1.00	0.14
M3b,M4b	PMOS	3.42	0.14
M5a,M6a	NMOS	2.00	0.14
M5b,M6b	PMOS	6.84	0.14
M7,M8	NMOS	5.00	0.14
M9,M15	NMOS	6.00	0.14
M10,M16	PMOS	20.52	0.14
M11,M17	NMOS	8.00	0.14
M12,M18	PMOS	27.36	0.14
M19,M20	NMOS	2.00	0.14

Table 5.6: Third integrator capacitor values.

Capacitors	Size (fF)
C_{s3a}	350
C_{s3b}	50
C_{s3c}	100
C_{f3}	500
C_{L3}	100

as in a two-stage amplifier while maintaining high bandwidth as of a simple single-stage folded-cascode amplifier [61]. Compared with the power consumption of the main OTA, the additional power consumption from the boosters is small with a careful design [62].

5.3.1 Main OTAs

The circuit topology of all three OTAs is equivalent except for the device widths and lengths. Longer channel length devices are used in first OTA to obtain a higher gain. The schematic of the OTA is shown in Figure 5.5. The OTA consists of a folded-cascode main OTA and two folded-cascode boosters resulting in DC gain of the OTA in the order of $(g_m r_o)^4$. However, when output swings close to *VDD* or *GND*, hot electrons may be injected

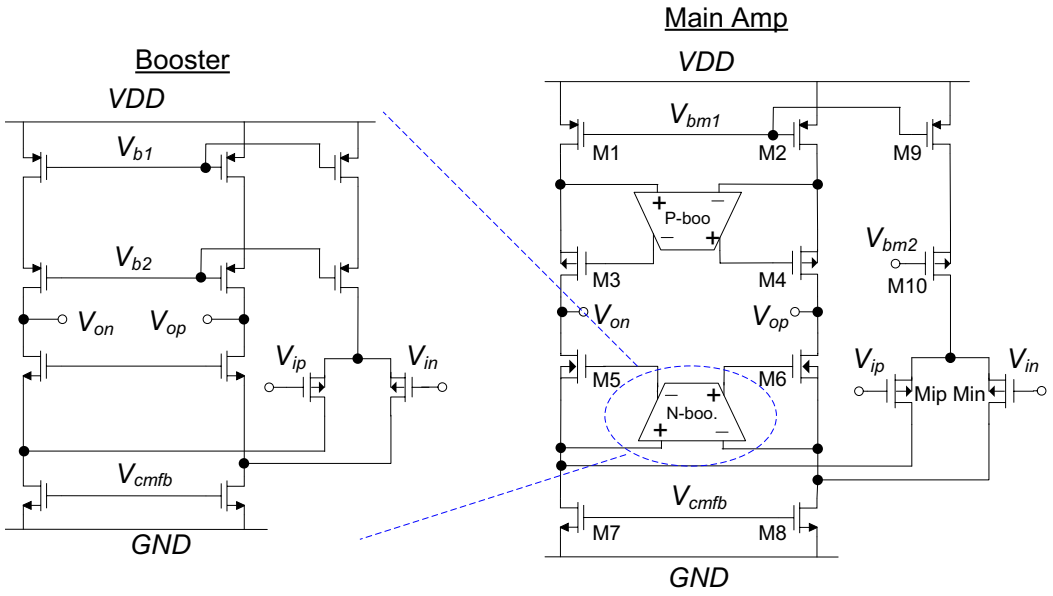


Figure 5.5: Folded-cascode OTA with gain-boosting.

into the substrate and supplies reducing the output impedance in effect. To remedy this problem, the bodies of the cascode transistors (M3-M6) are connected to the sources in order to collect hot electrons. However, extra well-capacitance at the sources of the cascode transistors lowers the frequency of the second pole and thus degrade the phase margin. Large PMOS instead of NMOS input transistors are used to keep the flicker noise low. The common-mode input voltage and the common-mode output voltage are maintained at 0.5V and 0.6V respectively. A switched-capacitor common-mode feedback circuit sets the common-mode output voltage. Table 5.7 shows the sizes of the transistors used in three OTAs. Figure 5.6 plots the DC gain of the first OTA against the output voltage swing. The peak DC gain is 94dB, and the gain drops to 89dB at ±0.7V output swing. The target unity gain frequency(f_u) of the amplifier is 300MHz. This allows 15 time constants for the OTA to settle.

Table 5.7: Transistor sizes in OTAs.

Transistors	Type	1st OTA ($W(\mu\text{m})/L(\mu\text{m})$)	2nd OTA ($W(\mu\text{m})/L(\mu\text{m})$)	3rd OTA ($W(\mu\text{m})/L(\mu\text{m})$)
M1,M2	PMOS	360.0/0.21	120/0.14	60/0.14
M3,M4	PMOS	294.4/0.21	120/0.14	60/0.14
M5,M6	NMOS	112.0/0.21	36.0/0.14	18/0.14
M7,M8	NMOS	384.0/0.21	57.6/0.14	36/0.14
M9	PMOS	720/0.21	240/0.14	120/0.14
M10	PMOS	588.8/0.21	240/0.14	120/0.14
Mip,Min	PMOS	256/0.14	96.0/0.14	48.0/0.14

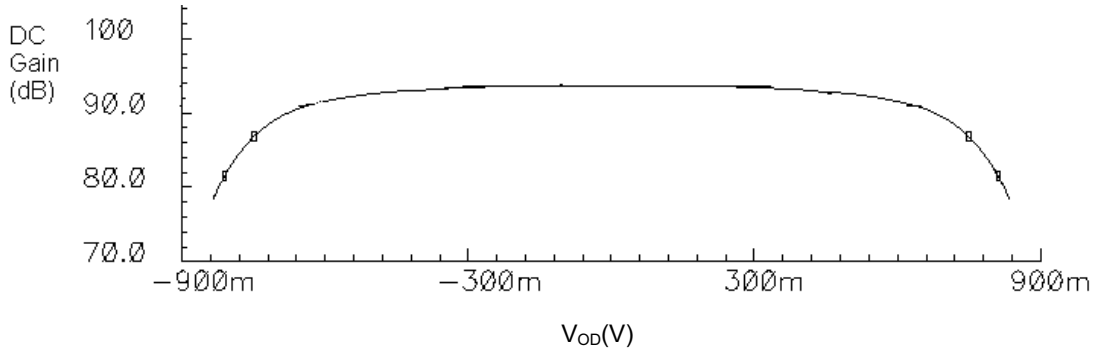


Figure 5.6: DC gain of the first amplifier.

5.3.2 N-side Boosters

Figure 5.7 illustrates the schematic of the N-side booster, which is a PMOS-input folded-cascode amplifier. PMOS-input folded-cascode is used for its low input common-mode voltage because inputs of the N-side booster are connected to the drains of the NMOS current sources (M7 and M8 in Figure 5.5) in the main folded-cascode amplifier. The N-side booster employs a continuous-time common-mode feedback by controlling the current in transistor M11. Since they are used to bias the main amplifier, the outputs of boosters do not need to swing. Therefore, more voltage headroom are allocated to the PMOS (M1 and M2) and NMOS (M7 and M8) current sources, which in turn increases the output

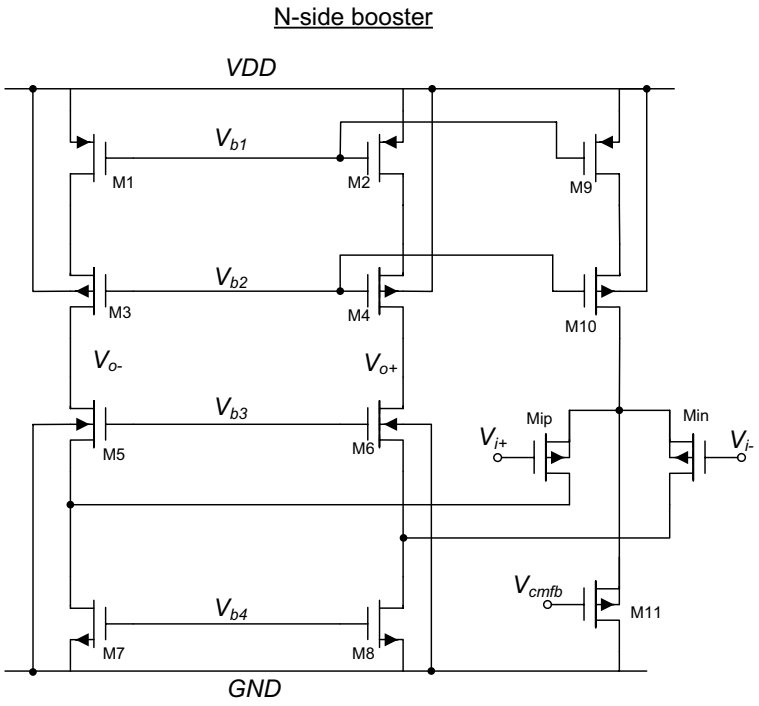


Figure 5.7: Schematic of N-side booster.

impedance (r_o) of the current sources and thus increases the voltage gain. Transistor sizes of the N-side booster are summarized in Table 5.8.

5.3.3 P-side Boosters

Figure 5.8 shows the schematic of the P-side booster, which is an NMOS-input folded-cascode. NMOS-input folded-cascode is used for its high input common-mode voltage because inputs of the P-side booster are connected to the drains of the PMOS current sources (M1 and M2 in Figure 5.5) in the main folded-cascode amplifier. The P-side booster employs a continuous-time common-mode feedback by controlling the current in transistor M11 as shown in Figure 5.8. Transistor sizes are summarized in Table 5.9.

Table 5.8: Transistor sizes in N-side boosters.

Transistors	Type	1st OTA ($W(\mu m)/L(\mu m)$)	2nd OTA ($W(\mu m)/L(\mu m)$)	3rd OTA ($W(\mu m)/L(\mu m)$)
M1,M2	PMOS	45.0/0.4	48.0/0.4	24/0.4
M3,M4	PMOS	45.0/0.4	64.0/0.4	32/0.4
M5,M6	NMOS	30.0/0.4	30.0/0.4	12/0.4
M7,M8	NMOS	40.0/0.6	24.0/0.4	16/0.4
M9	PMOS	135/0.4	144.0/0.4	72.0/0.4
M10	PMOS	135/0.4	192.0/0.4	96.0/0.4
Mip,Min	PMOS	35/0.14	25.6/0.14	12.8/0.14

Table 5.9: Transistor sizes in P-side boosters.

Transistors	Type	1st OTA ($W(\mu m)/L(\mu m)$)	2nd OTA ($W(\mu m)/L(\mu m)$)	3rd OTA ($W(\mu m)/L(\mu m)$)
M1,M2	PMOS	96.0/0.4	96.0/0.4	48/0.4
M3,M4	PMOS	120.0/0.4	96.0/0.4	48/0.4
M5,M6	NMOS	32.0/0.4	48.0/0.4	24/0.4
M7,M8	NMOS	24.0/0.6	24.0/0.4	12/0.4
M9	NMOS	96.0/0.4	144.0/0.4	72.0/0.4
M10	NMOS	72.0/0.4	72.0/0.4	36.0/0.4
Mip,Min	PMOS	16.0/0.14	16.8/0.14	8.4/0.14

5.3.4 Switched-Capacitor Common-Mode Feedback (CMFB) Circuits

Switched-capacitor common-mode feedback circuit [63] is used to set the OTA common-mode output voltage at 0.6V. In order to cascade multiple integrators, the output common-mode voltage of the OTA must be set identical to the input common-mode voltage of the following integrator. The schematic of the common-mode feedback circuit is shown in Figure 5.9. During phase 2 (integrating) when ϕ_{2d} is high, capacitors C_2 sample the common-mode bias voltage and the desired output common mode voltage (V_{ocm}). Since C_2 are disconnected from the OTA output during phase 2, they do not load the OTA settling. During phase 1, transistors M1-M3 are turned on, and charge is redistributed over all the capacitors. Redistribution of charge sets the OTA output to the desired level, but does

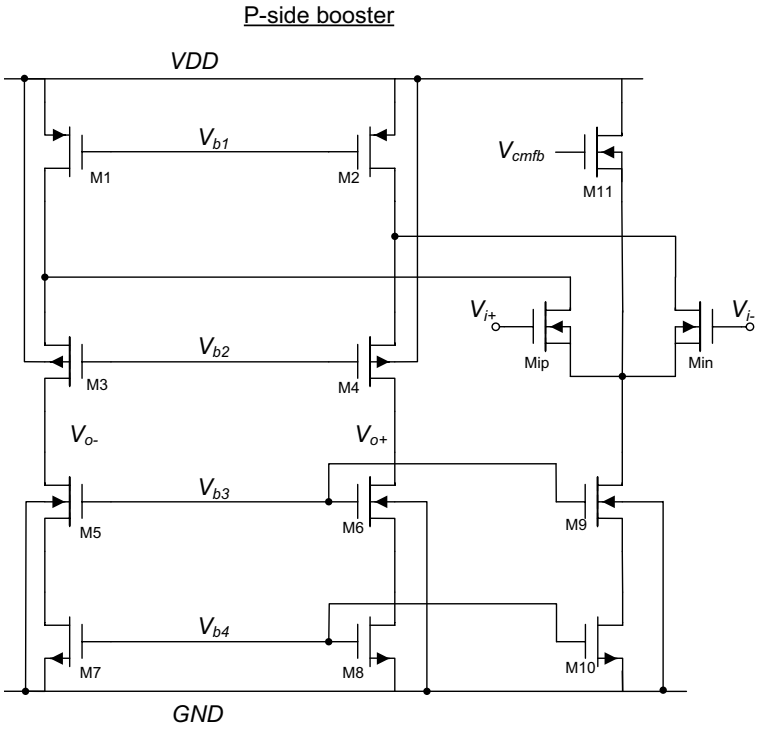


Figure 5.8: Schematic of P-side booster.

not alter the differential voltage. To avoid differential to common-mode conversion at the output of the OTA, the common-mode loop is designed to be as fast as the differential loop. In addition, extra attention is needed when sizing M1-M3 because they inject channel charge into C_1 when being turned off.

5.4 Comparators

Comparators are the second most important analog components in $\Sigma\Delta$ ADCs. In the 2-1 MASH architecture, there are two comparators, and each samples the second integrator or the third integrator. Many different kinds of comparators such as regenerative comparators with [64] [65] or without an input buffer [3] or comparators with offset cancel-

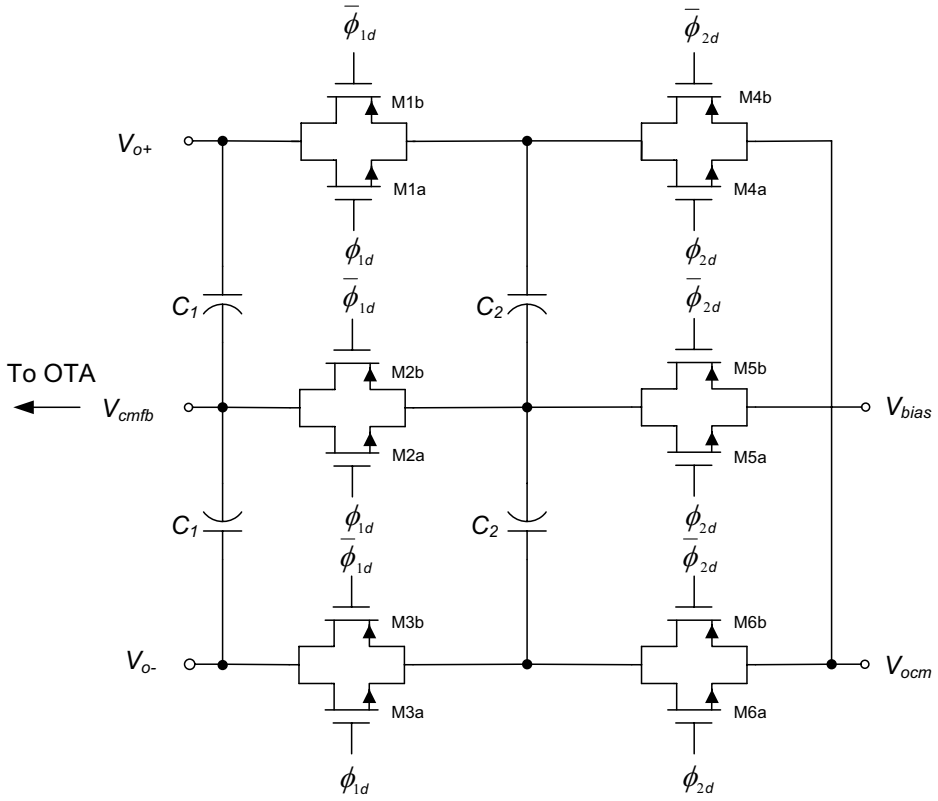


Figure 5.9: Switched-capacitor common-mode feedback.

lation [66] have been reported. $\Sigma\Delta$ A/D converters are insensitive to comparator offset and hysteresis [43]. Thus, a regenerative comparator without input buffer as shown in Figure 5.10 is sufficient for our design [47]. When ϕ_{1E} is low, the comparator is in pre-charge phase. As ϕ_{1E} goes high to turn on M5 and M6, transistors M3, M4, M7 and M8 form a back-to-back inverter pair. The back-to-back inverter pair flips to an appropriate state depending on the polarity of the differential input. There is a temporary transient disturbance when the integrator changes from integrating phase to sampling phase due to the change in feedback factor. Therefore, comparators are strobed before integrators transition from integrating phase to sampling phase. One possible solution is to have an early phase 1 clock (ϕ_{1E}) so

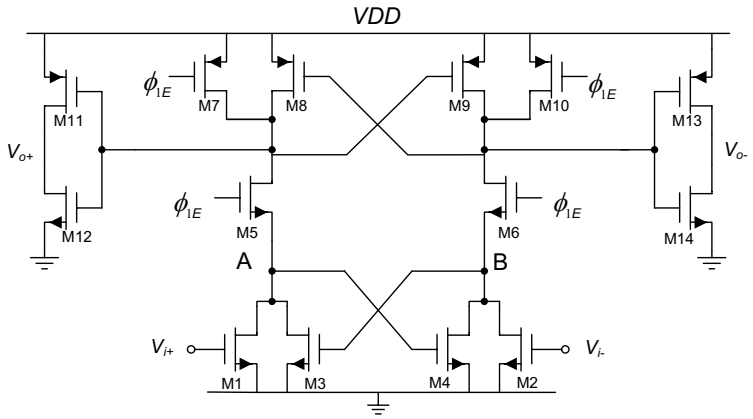


Figure 5.10: Regenerative comparator.

that the comparator is strobed shortly before ϕ_{2d} goes low. Another potential problem is the kickback noise from the comparator the integrator output. When ϕ_{1E} is high, nodes A and B flip depending on the comparator input. This causes a disturbance at the comparator input due to coupling through C_{gd} of M1 and M2. Comparators are carefully verified that the kickback noise does not degrade the performance of the converter.

5.5 Latches and DACs

When ϕ_{1E} goes low, the comparator enters the pre-charge state by turning on transistor M7 and M10; and the previous state is lost. At the same time, however, the integrator enters the integrating phase, and the DAC feedback signal must be kept constant. Thus, we need a storage element after the comparator to keep the state before the comparator returns to pre-charge. A simple back-to-back NAND SR-latch can serve this purpose. Figure 5.11 shows the schematic of the SR-latch and the DAC. Gates G1-G3 prevent false triggering of the SR-latch when the comparator is still resolving its output state

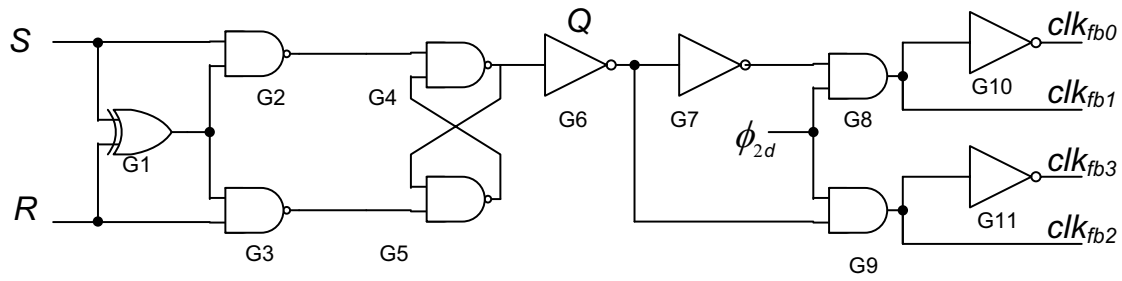


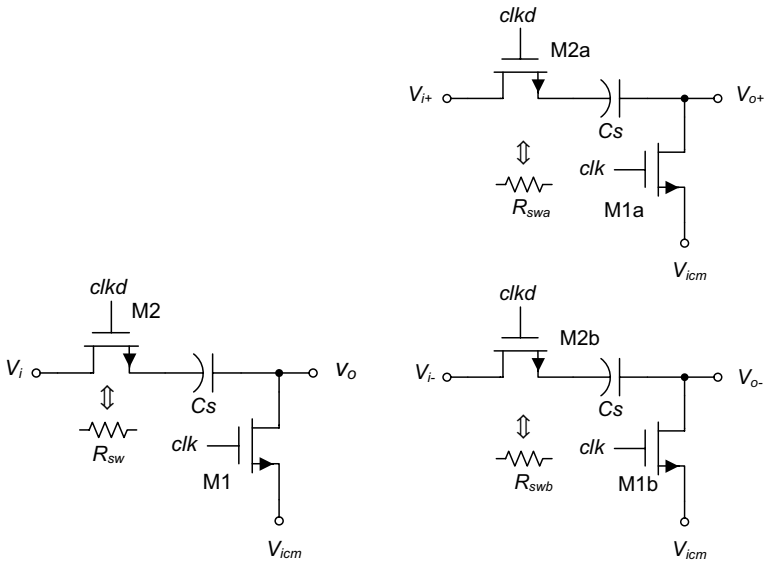
Figure 5.11: SR-latch and DAC.

or in metastability. Signals clk_{fb0}, clk_{fb1}, clk_{fb2} and clk_{fb3} control whether to feed V_{refn} or V_{refp} to the integrators during integrating phase.

5.6 Sampling Switches

Figure 5.12(a) shows a single-ended sampling circuit, where clock *clkd* is a delayed version of the clock *clk*. When transistors M1 and M2 are on, the capacitor tracks the input voltage. At the end of the tracking period, M1 is turned off before M2. At the instance of turning off M1, the channel charge is injected into both the drain and source terminals. The amount of charge injection to the source or drain nodes depends on the impedance looking outward from the source and drain terminals. However, there is no channel charge injection from M2 because the sampling capacitor is floating while turning off M2. The sampled voltage including switch charge injection is given by

$$V_{S/H,SE} = \frac{Q_{inj}(R_{sw})}{C_s} + V_i \tag{5.1}$$



(a) (b)

Figure 5.12: (a) Single-ended sampling network, (b) fully-differential sampling network.

where $Q_{inj}(R_{sw})$ is the charge injection into the drain of transistor M1, and it is dependent on the sampling switch's (M2) equivalent resistance (R_{sw}).

A fully differential sampling network is shown Figure 5.12(b). To have equal charge injection in both positive and negative paths, it is necessary to keep the on-resistance of the sampling switches constant across all input range. Then, charge injection only leads to common mode drift leaving differential signal undisturbed. The differential sampled voltage is given by

$$V_{S/H,diff} = V_{o+} + V_{o-} = \frac{Q_{inj}(R_{swa})}{C_s} + V_{i+} - \frac{Q_{inj}(R_{swb})}{C_s} + V_{i-} \tag{5.2}$$

where R_{swa} and R_{swb} are the equivalent resistance of transistor M2a and M2b. If R_{swa}

equals R_{swb}, (5.2) reduces to

$$V_{S/H,diff} = V_{i+} + V_{i-}. \tag{5.3}$$

Two kinds of sampling switches are used in our design. Bootstrapped switches are used in the first integrator to achieve high linearity. For simplicity, CMOS switches are used in the second and third integrators. A bootstrapped switch similar to [60] is shown in Figure 5.13. Transistor M1 is the sampling switch. Transistors M9, M10, C_1 and C_2 form a voltage doubler, which is able to raise the gate voltage of M8 to approximately $2\,VDD$ when clock $\bar{\phi}$ is high. This allows transistor M8 to charge the capacitor C_3 to VDD. When clock ϕ goes high, M3 is turned on by M6. C_3, which acts as a battery, is placed across the sampling switch M1, and it maintains a constant V_{gs} at M1. Ideally, the V_{gs} should be at VDD; however, the charge on C_3 is subject to the charge sharing at the gate of the sampling switch. This V_{gs} is

$$V_{gs,M1} = \frac{-C_p V_i + C_3 VDD}{C_p + C_3} \tag{5.4}$$

where C_p is the total parasitic capacitance at the gate of the sampling switch with M3 on. Therefore, equivalent resistance of the sampling switch is kept relatively constant subject to the effect of the parasitic capacitance, C_p. C_3 should be large in comparison to C_p in order to keep the V_{gs} constant. However, the sampling switch still exhibits non-linearity due to its body effect. Functionalities of other transistors are as follows. Transistor M5 turns off the sampling switch when clock ϕ goes low. M4 is added for reliability issue because the voltage at the gate of the sampling switch can reach $2\,VDD$ at maximum.

A CMOS sampling switch is shown in Figure 5.14. Since the integrator common-

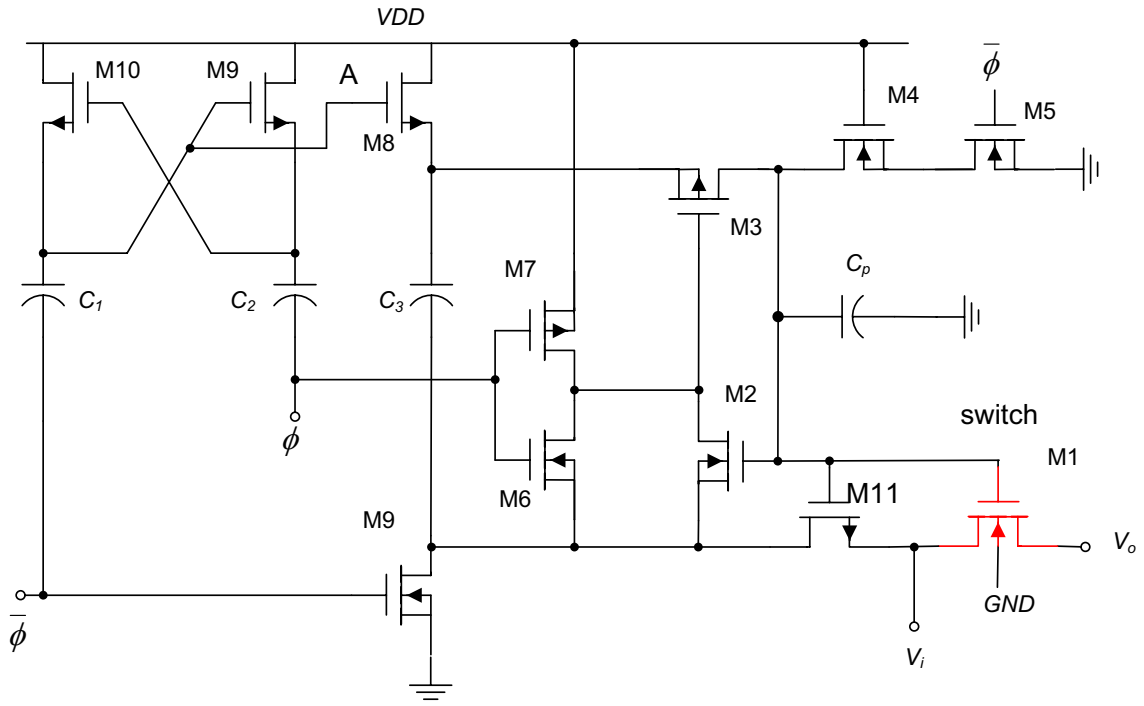


Figure 5.13: Bootstrapped switch.

mode input voltage is 0.6V, the equivalent resistance of the switch are designed to be symmetric about 0.6V such that the resistance is equal for swings above or below the common-mode voltage. Ideally, this only introduces a common-mode charge injection in a fully differential circuit. In addition, there is a cancellation of channel electrons from the NMOS transistor and channel holes from the PMOS transistor. Equivalent resistance of the CMOS switch versus input voltage is plotted in Figure 5.15.

5.7 Clock Generation

Switched-capacitor circuits require generation of two-phase non-overlapping clocks and with delayed versions to reduce signal-dependent charge injection. Figure 5.16 shows

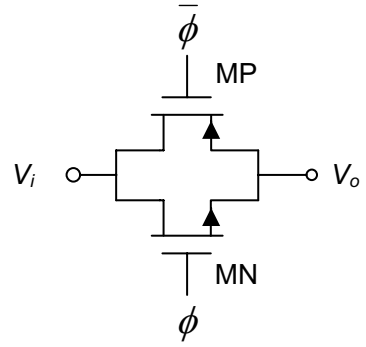


Figure 5.14: CMOS sampling switch.

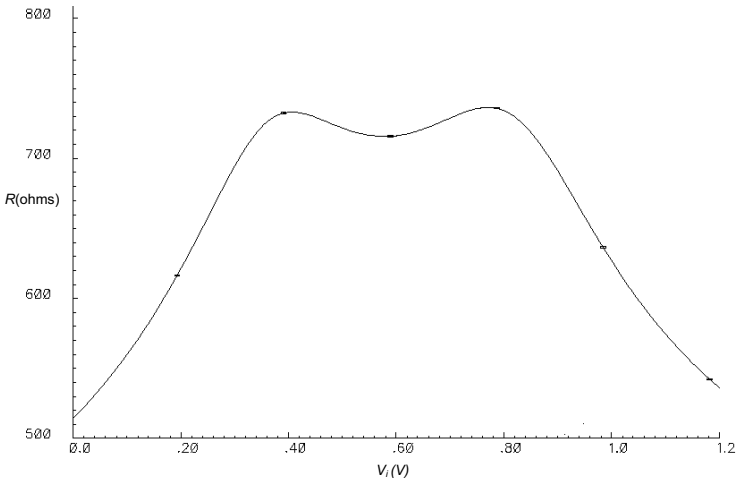


Figure 5.15: Equivalent resistance of a CMOS sampling switch with NMOS, PMOS sizes of 3.42μm/0.14μm and $1\mu/0.14\mu$m, respectively.

the clock generation circuit, and Figure 5.17 shows the waveform of some of the clock signals. The delay between phase 1 and phase 2 is controlled by delays of the inverter chains. The pass gates are added to introduce delay without signal inversion. The early phase clock ϕ_{1E} is used to strobe the comparators.

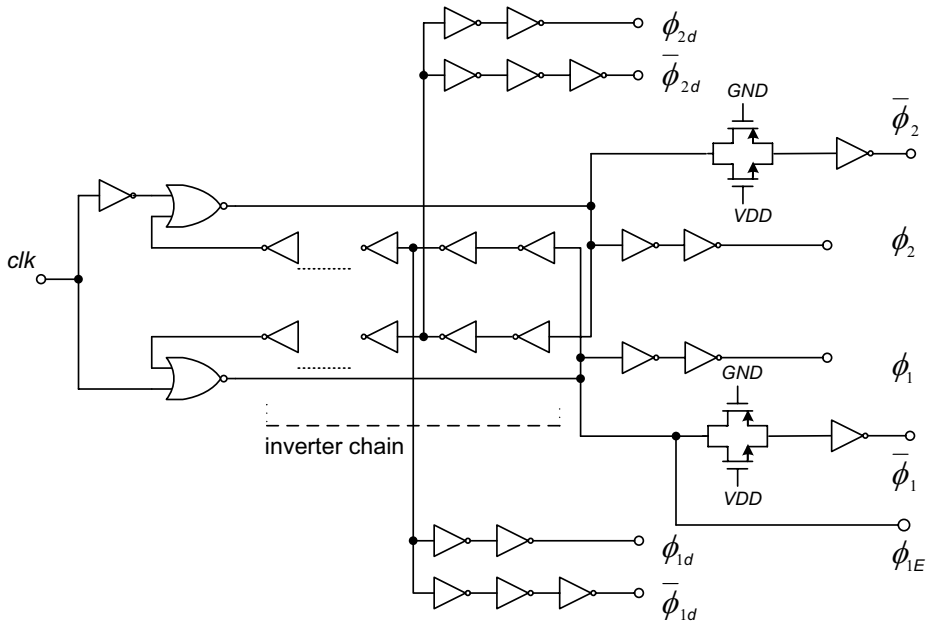


Figure 5.16: Non-overlapping clock generation circuit.

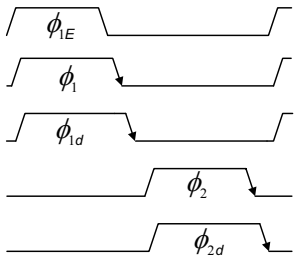


Figure 5.17: Non-overlapping clocks.

5.8 Conclusion

This chapter presents the designs of different analog circuits for the $\Sigma\Delta$ A/D converter. These building blocks are integrators, amplifiers, switches, comparators, DAC, and the non-overlapping clock generator. Furthermore, the operation and design considerations of each building block are also discussed.

Chapter 6

Sample-and-Hold Amplifier for ΣΔ A/D Converter (ΣΔ-SHA)

6.1 Introduction

[1] In this application, the ΣΔ ADC acts like a DC voltage meter. ΣΔ ADC requires a front-end sample-and-hold amplifier (SHA) to be used as a slow-but-accurate reference ADC for the proposed calibration (Figure 6.1(a)). The timing diagram of the sampling clocks of the SHA, the pipelined ADC and the ΣΔ ADC is shown in Figure 6.1(b). Since the conversion speed of the ΣΔ ADC is much slower than that of the pipelined ADC, the SHA first samples the input and then holds the acquired signal for multiple cycles of pipelined ADC clock for the ΣΔ ADC to convert the acquired signal. The parameters M and N are programmable. Not only does the SHA need to accurately sample the signal but it is also necessary to sample the signal at the same moment as the pipelined ADC

[1]The SHA is designed by Yun Chiu.

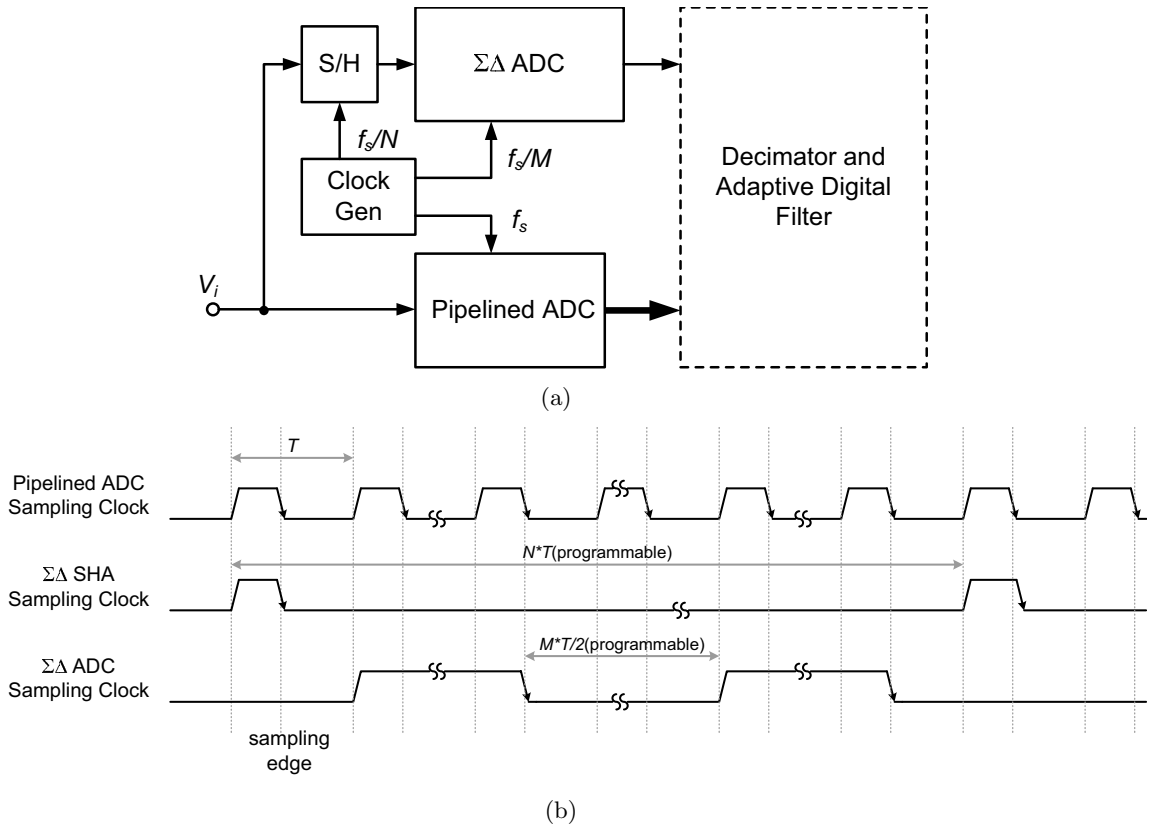


Figure 6.1: (a) ADC system block diagram, (b) timing diagram.

as indicated in Figure 6.1(b). Any sampling skew between the SHA and the pipelined ADC results in degradation in effectiveness of the calibration algorithm. Besides timing mismatch, input bandwidth mismatch between the SHA and pipelined ADC will also have a similar effect. On the other hand, electronic noise is not critical in the SHA because noise is averaged in the LMS ADF (Section 2.6.1); thus, obtaining high-linearity is most important in the SHA.

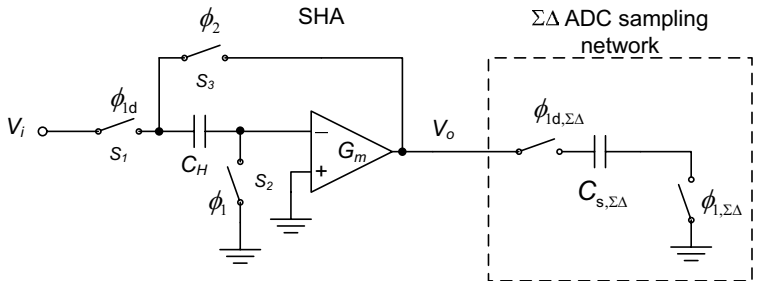


Figure 6.2: Flip-over type switched-capacitor SHA.

6.2 S/H Architecture

The settling speed of the SHA is not very critical in this prototype because long hold time (Figure 6.1) allows extra time for settling, i.e., settling timing can be longer than $T/2$ where T is period of the pipelined ADC clock. A flip-over switched-capacitor SHA architecture (Figure 6.2) [16] is employed here because it is simple and compact. The flip-over architecture also has the advantage of high feedback factor which can in turn save power consumption in the amplifier. During tracking phase, the capacitor C_H is charged to the input voltage by switches S_1 and S_2. In hold mode, switches S_1 and S_2 are open and switch S_3 is closed. The sampled signal of the capacitor is put over the output and the input of the amplifier. As a result, the same sampled input signal appears at the output terminal. The bandwidth of this system during hold phase is determined by

$$f_{-3dB} = \frac{g_m}{2\pi C_H + C_{s,\Sigma\Delta}} \tag{6.1}$$

where $C_{s,\Sigma\Delta}$ is the sampling capacitor of the ΣΔ ADC following the SHA. The bandwidth determines the settling time constant of the SHA. Since the ΣΔ decimated SHA and the pipelined ADC sample the same signal, the bandwidth of the sampling networks of the

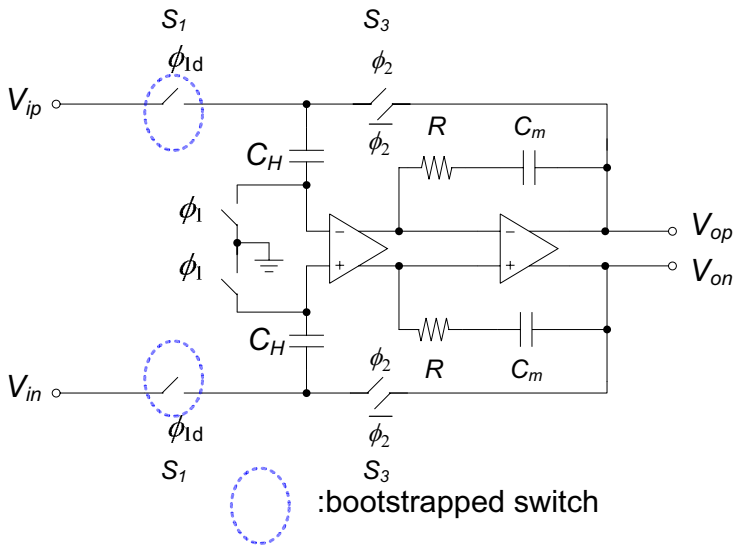


Figure 6.3: Two-stage high-gain amplifier in S/H.

SHA and the pipelined ADC are matched. C_H is 0.5pF is our design. The capacitors and switches sizes of the SHA are 1/4 of that of the first pipelined ADC stage so that the RC time constants of both circuits are equal.

Traditional non-overlapping clocking scheme is used to reduce switch charge injection. In additional to switch charge injection error, another prominent error in SHA is amplifier gain error; thus a two-stage Miller-compensated high-gain amplifier is used (Figure 6.3). A two-stage amplifier is preferable over a single-stage one because the off-resistance of the switches (S_1) hurts the overall amplifier gain in a single-stage amplifier. However, in a two-stage amplifier, the total gain is distributed into two different stages. The first stage by design provides most of the gain, and a small gain is added by the second stage; thus, the off-resistance of S_1 does not degrade the overall gain.

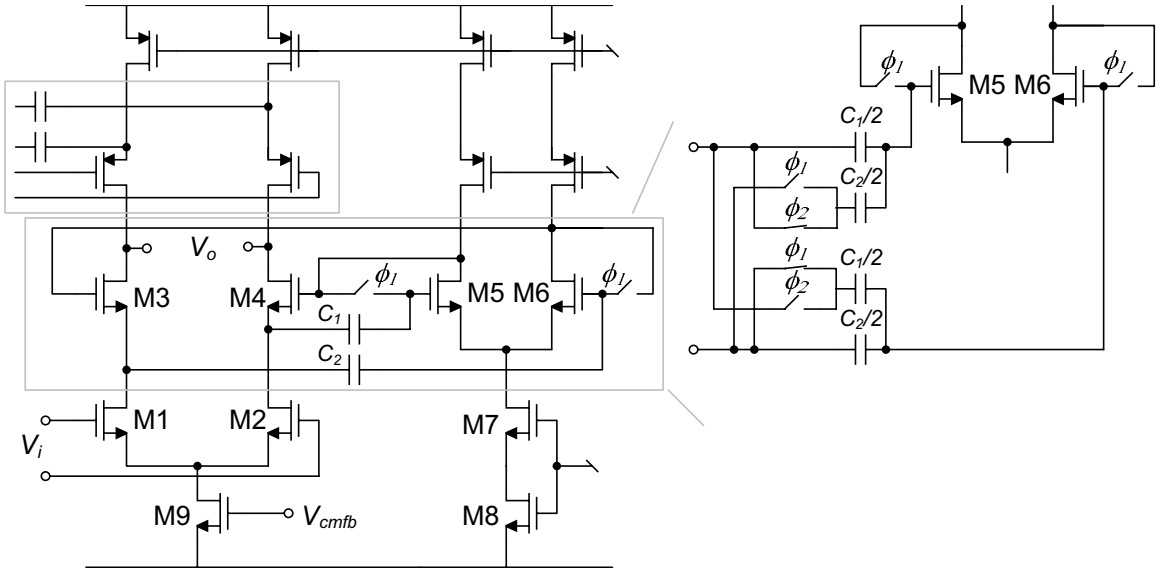


Figure 6.4: S/H amplifier: stage 1.

6.2.1 High-gain Amplifier

A fully differential, two-stage high-gain amplifier with >100dB gain is used to minimize gain error because nonlinear gain causes distortion. The first stage is a telescopic amplifier with gain-boosting shown in Figure 6.4 [67]. The N-side gain-boosters are NMOS common-source amplifiers, M5 and M6, with capacitors, C_1 and C_2, as level shifters. Capacitors, C_1 and C_2 are cross-coupled at two clock phases to reduce memory effect. P-side gain-boosters are constructed similarly with PMOS common-source amplifiers. The second stage is a differential pair with PMOS input and cascode NMOS load (Figure 6.5). Since the duty cycle of the SHA clocks are much smaller than 50%, non-overlapping clocks from the $\Sigma\Delta$ ADC are utilized to drive the switches of the gain-boosting circuits in Figure 6.4.

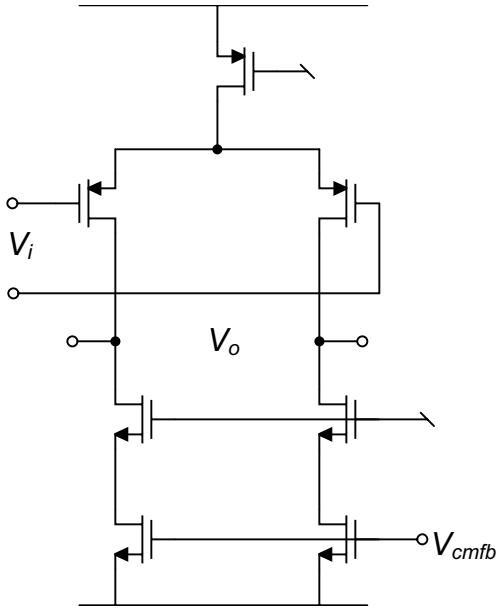


Figure 6.5: S/H amplifier: stage 2.

6.3 Simulations

Figure 6.6 shows the simulated performance of the SHA including packaging bond wire at different sampling frequencies and input frequencies. The THD drops with increasing input frequency. The SHA maintains THD above 60dB for up to 500MS/s, i.e, T=1/500MHz.

6.4 Summary

We have presented the design of the SHA in this chapter. The key design issues are input bandwidth difference between the SHA and the pipelined ADC and linearity of the SHA. Input bandwidth mismatch is mitigated with replica sampling network; high linearity was achieve using a high-gain two-stage amplifier (>100dB).

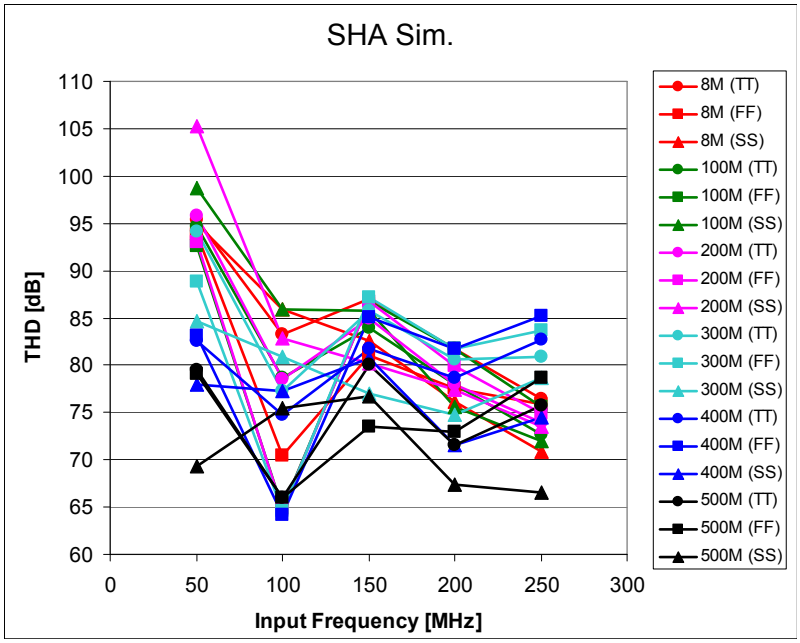


Figure 6.6: SHA simulated results.

Chapter 7

Design of High-speed Pipelined A/D Converter

7.1 Introduction

[1] [2] This chapter discusses the design of the high-speed-but-inaccurate pipelined ADC which is calibrated by the digital calibration framework presented in Chapter 2. This framework alleviates the analog circuit accuracy requirement such as switch charge injection, capacitor matching, and amplifier gain. Since the speed bottleneck in pipelined ADC lies in the amplifier settling speed, without craving for high-gain amplifiers required by conventional pipelined ADCs [68], we can fully take advantage of short channel transistors available in deep sub-micron CMOS technology to maximize ADCs' conversion rate.

[1] The pipelined ADC is designed in collaboration with Johan Vanderhaegen and with help from Dusan Stepanovic.

[2] Although all circuits are fully differential, some circuits are drawn in single-ended manner for clarity.

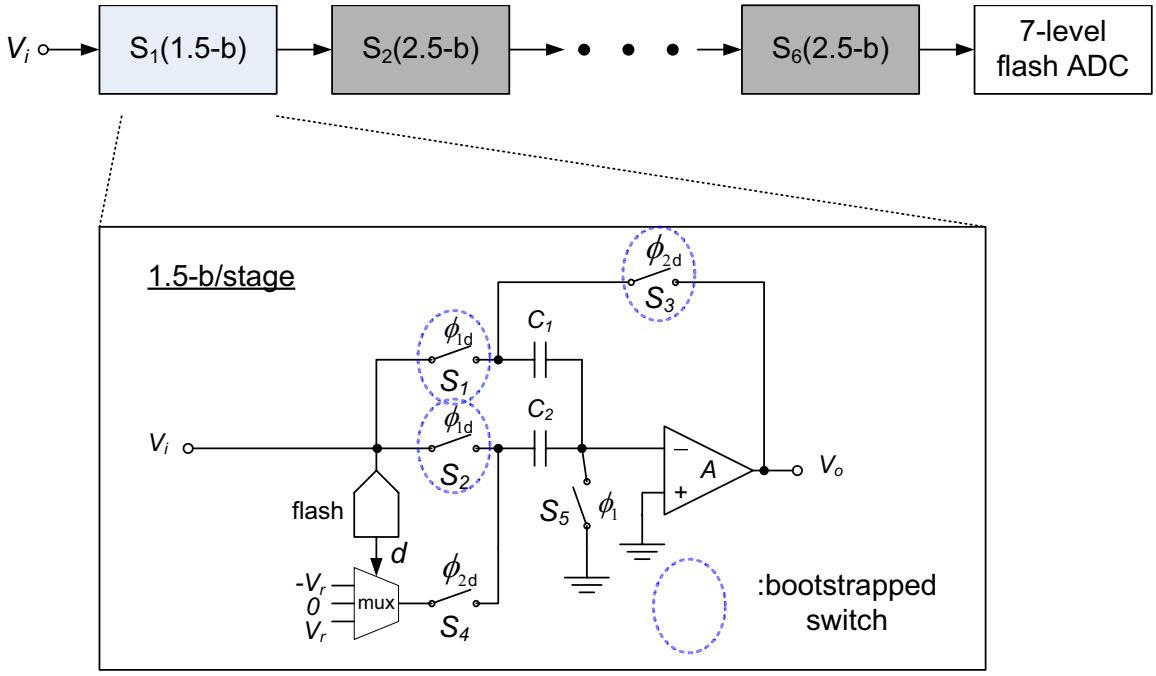


Figure 7.1: Block diagram of a pipelined ADC.

7.2 Power Optimization of Pipelined ADC

A key design step to minimize power consumption in a pipelined ADC is to determine the appropriate number-of-bit/stage for the pipelined stages. The optimization is performed using the global optimization algorithm developed in by Johan Vanderhaegen at Berkeley Wireless Research Center [69]. For a 14-bit (raw bits) pipelined ADC at 400MS/s, the power consumption is optimized with 1.5-b/stage in stage 1 and 2.5-b/stage in stages 2-6, followed by a 3-b (7-level) flash ADC at the end. It is well-known that 1.5-b/stage is equivalent to 2-b/stage with 1-bit overlap and 2.5-b/stage is equivalent to 3-b/stage with 1-bit overlap. Thus, total number of bits is $(2 + 3 + 3 + 3 + 3 + 3 + 3 - 6) = 14$. The architecture of the pipelined ADC as well as the schematic of the first stage are shown in Figure 7.1.

7.3 Stage 1: 1.5-b/stage

The first stage of a pipelined ADC is the most critical in terms of speed, power, and noise. Since 1.5-b architecture is more tolerant to comparator offset and timing skew between residue amplifier and comparator, 1.5-b architecture is used in the first stage. The schematic of the first stage is illustrated in the lower portion of Figure 7.1. SNR limit determines capacitor sizes which in turn decide the power consumption in the amplifier with a given settling speed. To achieve 10.5-b SNR with $1V_{pk-pk}$ full-scale input voltage, capacitors C_1 and C_2 are both 1pF and are implemented with MOM capacitors. The reference voltage V_r is equal to 0.5V and the common-mode voltage is 0.6V. Switches S_1, S_2, and S_3 are bootstrapped switches similar to Figure 5.13 , while S_4 and S_5 are single transistor switches. Since this is a 1.5-b/stage architecture, the flash ADC is a 3-level switched-capacitor flash implementation. Switched-capacitor flash ADC are used to minimize the timing skew between the flash ADC and the residue amplifier because the input signal are both sampled onto capacitors in flash ADC and sampling capacitors of the residue amplifier. The sampling actions are controlled by the same clock signal.

7.3.1 Fast-settling, Low-gain Amplifier

Since the calibration algorithm is capable of correcting nonlinear amplifier gain error (Chapter 2), the amplifier gain is not very critical. To save power and maximize settling speed, a very simple, single-stage pseudo-differential amplifier is sufficient. Device sizes are determined using optimization methodology described in [69]. The simplified schematic of the amplifier is shown in Figure 7.2. In stage 1, there is no common-mode feedback circuit,

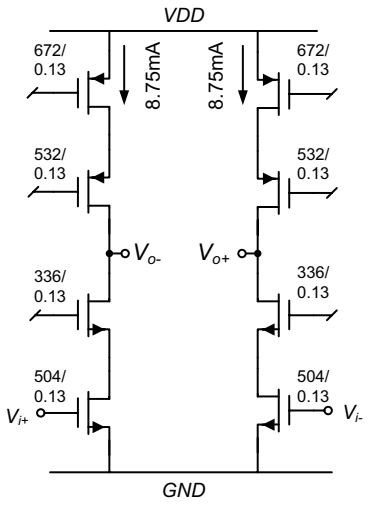


Figure 7.2: Amplifier in stage 1.

so the output common-mode level is determined by the input common-mode level of the switched-capacitor residue amplifier. Figure 7.3 plots the simulated settling of the first stage residue amplifier. The curve in the middle shows that the amplifier settles to its DC gain during amplifying phase with a 400MHz clock.

7.3.2 1.5-b Flash ADC

The schematic of a single-ended switched-capacitor 1.5-b flash ADC is shown in Figure 7.4. In the figure, ϕ_1 and ϕ_2 are non-overlapping clock phases, and ϕ_{1d} is a delayed version of ϕ_1. Comparator 1 decides if V_i is smaller $1/4V_r$, while comparator 2 decides if V_i is smaller than $-1/4V_r$. Table 7.1 shows the outputs of the comparators with different input levels. The flash ADC requires a high-speed comparator because time available for comparators to resolve is the short time window after the falling edge of the sampling phase (ϕ_1) and before the rising of the amplifying phase clock (ϕ_2). On the contrary, comparator

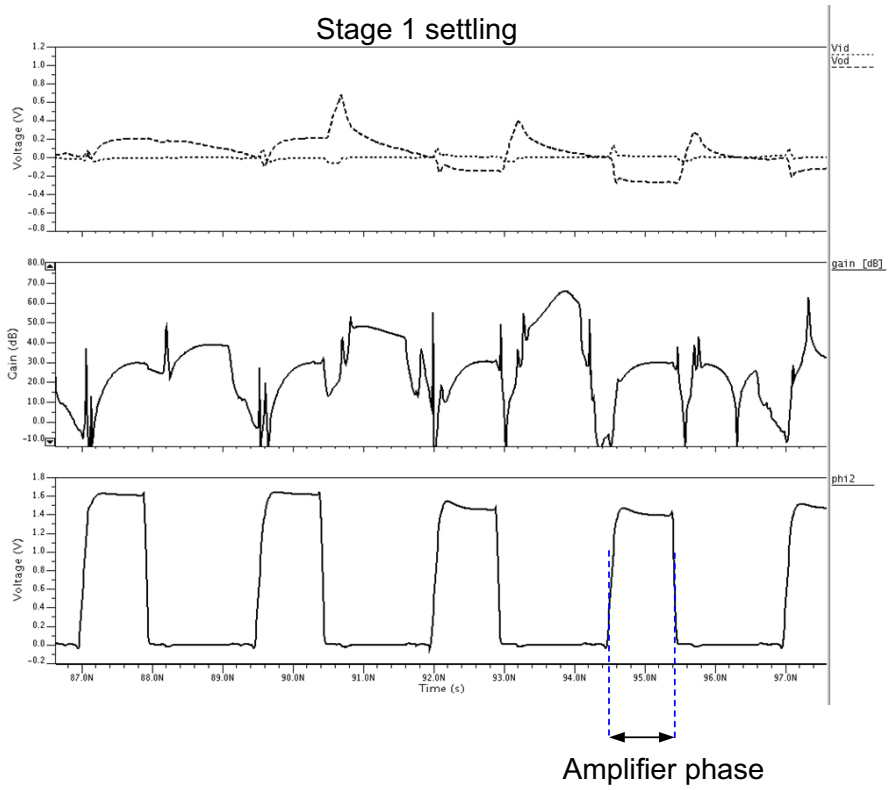


Figure 7.3: Simulated settling of the first stage residue amplifier (post-layout, 400MS/s).

input offset is not an issue here because 1.5-b architecture can tolerate a comparator offset of up $1/4V_r$. Therefore, a simple dynamic high-speed comparator without pre-amp is sufficient (Figure 7.5). When clock ϕ is high, the comparator is under reset, and Q and $\overline{Q}$ are equalized to mid-rail. Pre-charging Q and $\overline{Q}$ to mid-rail decreases the regeneration time when clock ϕ goes low. The complementary outputs are followed by an S-R latch (Figure 5.11).

Table 7.1: Decision of the 1.5-b flash ADC.

Input level	B_1	B_0
$V_i > 1/4V_r$	0	0
$1/4V_r \geq V_i > -1/4V_r$	1	0
$V_i < -1/4V_r$	1	1

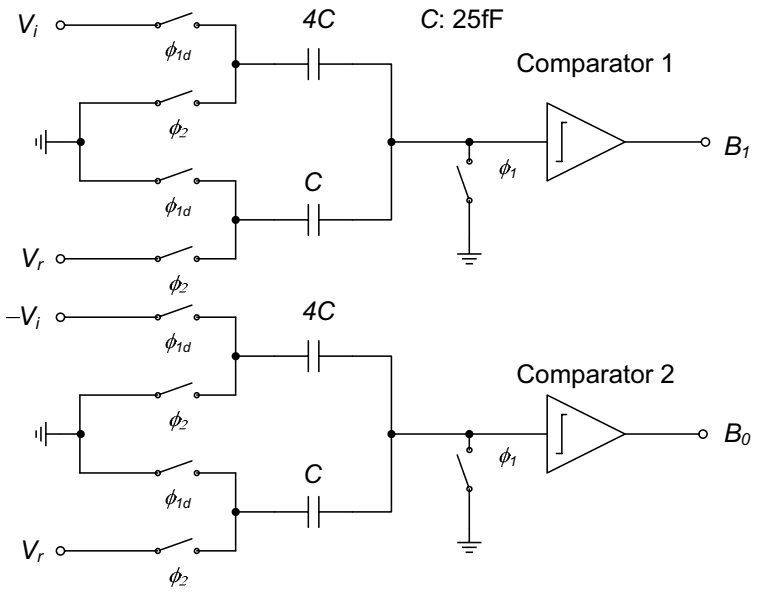


Figure 7.4: Switched-capacitor flash ADC schematic.

7.4 Stages 2-6: 2.5-b/stage

The 1.5-b stage 1 is followed by five 2.5-b stages. The schematic of the 2.5-b/stage is shown in Figure 7.6. Switches S_1 to S_5 are bootstrapped switches similar to the one in Figure 5.13, while the others are single/complementary transistor switches. Main amplifiers in stages 2-6 are the same as the one in stage 1 except the size is scaled down to reduce power consumption. Table 7.2 summarizes the amplifier size and the input capacitance of each stage. A main drawback of pseudo-differential amplifiers is the propagation of common-mode variation along the pipeline stages. Therefore, a $\Sigma\Delta$ common-mode feedback/feedforward circuit described in [62] is devised to control common-mode voltages.

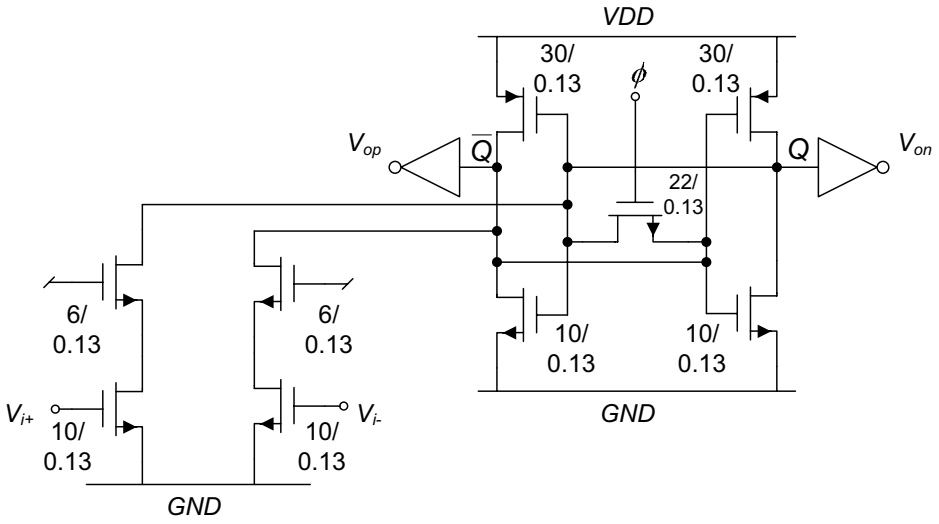


Figure 7.5: Dynamic comparator in stage 1.

Table 7.2: Scaling of the pipelines stages.

Parameters	Stage 1	Stage 2	Stage 3-6
Stage Input Capacitance (pF)	2	1	0.250
Amplifier Size (normalized)	7	4	1
Amplifier DC gain (dB)	∼30	∼30	∼30

7.4.1 7-level Flash ADC

Since the residue signal is held steady after the first stage, the timing skew problem between the flash ADC and the sampling capacitor of the residue amplifier is not an issue. Therefore, the 2.5-b stage employs a 7-level flash ADC constructed with six comparators and a resistive divider instead of a switched-capacitor flash ADC shown in Figure 7.7. Since this is a 2.5-b/stage, the pipeline stage can only tolerate $1/8V_r$ comparator offset. With V_r=0.5V, only 62.5mV of comparator offset can be tolerated; thus, the comparator in stage 1 with reasonable transistor sizes is not adequate due to its large input offset. A comparator consists of a pre-amp and a regenerative latch [70] in Figure 7.8 is fast and has lower offset.

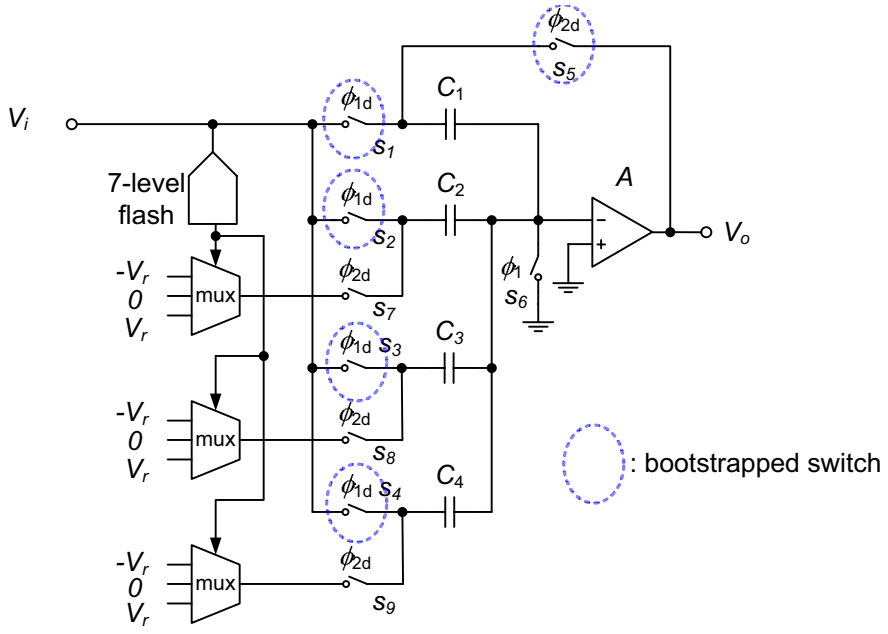


Figure 7.6: Schematic of stages 2-6.

The offset of this comparator is dominated by the pre-amp because any offset caused by the regenerative latch is divided by the gain of the pre-amp stage. Thus, transistors in the latch are small. The NMOS load transistors in the pre-amp are turned off during regeneration to boost the gain of the pre-amp. The offset of this comparator is dominated by the input NMOS transistors and the two pull-down NMOS transistors after the output of the pre-amp stage. With the sizing indicated in Figure 7.8, the standard deviation (σ) of offset is 12.1mV. The distribution of offset with 50 Monte Carlo simulations is plotted in Figure 7.9.

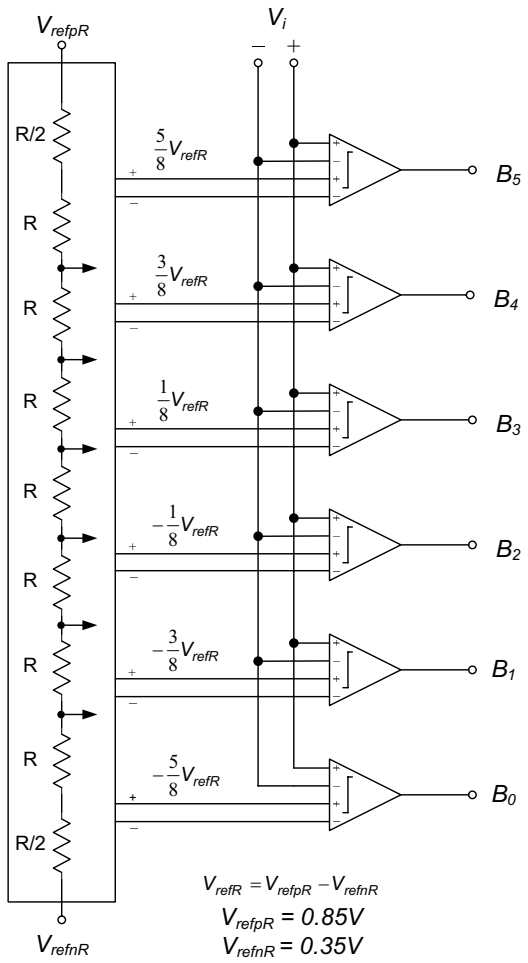


Figure 7.7: 7-level flash ADC in stages 2-7.

7.5 Summary

We have presented the design of the high-speed pipelined ADC under calibration. A very simple pseudo-differential amplifier with minimum-channel length devices is used in the stage residue amplification to maximize speed.

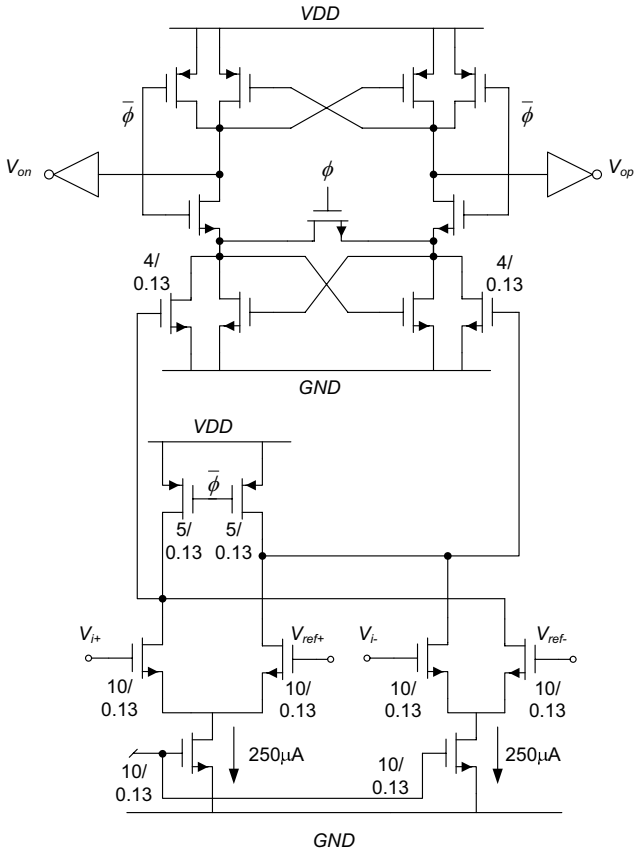


Figure 7.8: Comparator schematic stage 2-7.

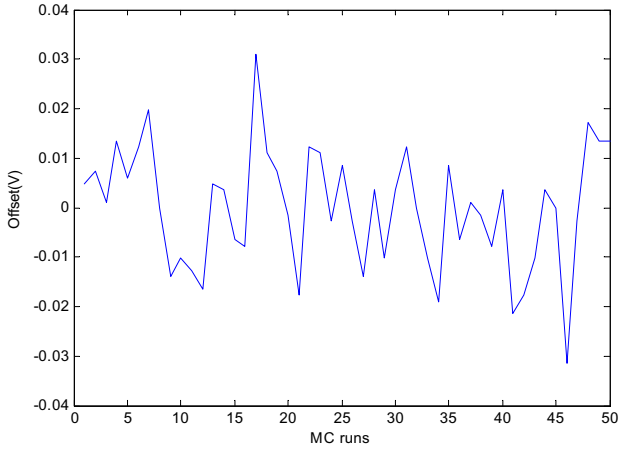


Figure 7.9: Comparator offset (50 Monte Carlo simulations).

Chapter 8

Clock Generation Circuit

8.1 Introduction

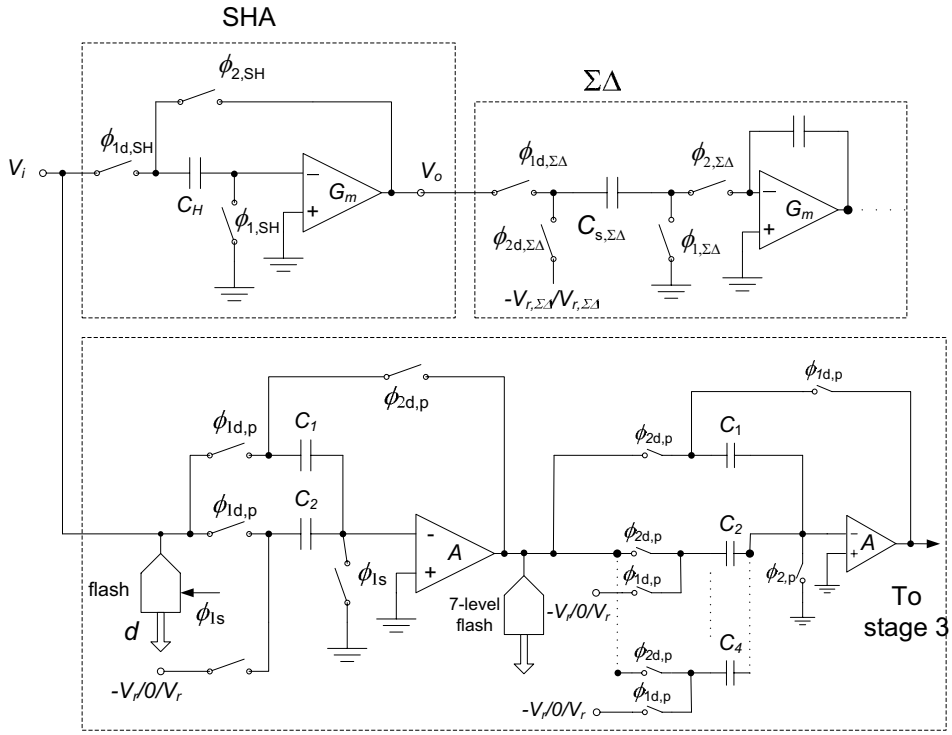
[1] The proposed ADC requires a clock generator, which generates three groups of synchronized clock signals for the pipelined ADC, ΣΔ-SHA, and ΣΔ. The clock generator has to operate over a wide frequency range because ADC needs to be tested at different frequencies. In addition, the sampling edge of the ΣΔ SHA clock and the pipelined ADC clock need to be aligned accurately with minimum jitter. A delay-locked-loop (DLL)-based architecture [71, 72] is used to generate clock signals for ADC system. A DLL generates multi-phase non-overlapping clock phases by combining different phases from the delay line at wide-range frequencies.

[1] The clock generation circuit is designed together with Sebastian Hoyos

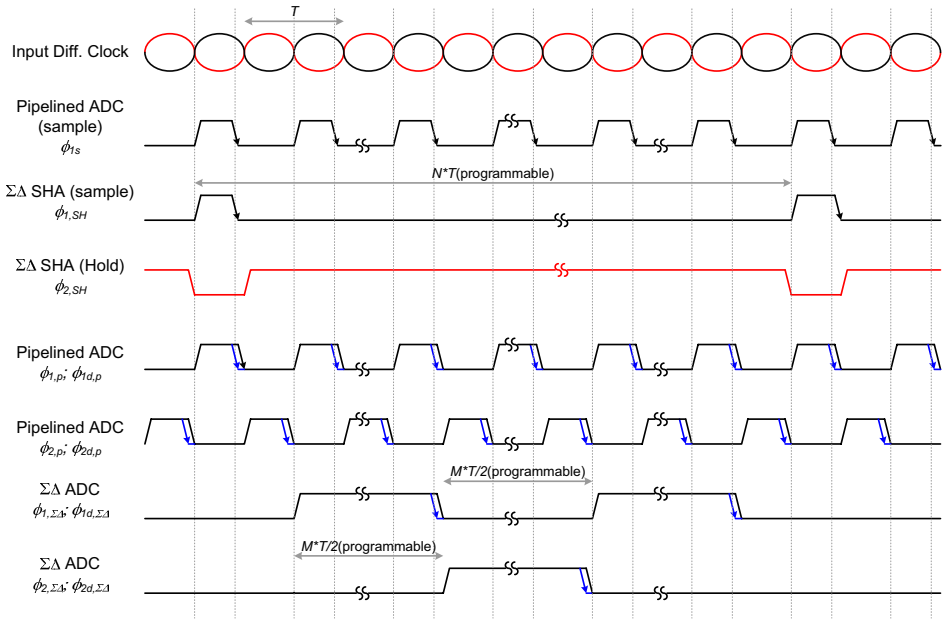
8.2 Main Clocks for the Proposed ADC

Since the system requires a very low-jitter clock source, an input differential sine wave from an instrument is fed from off-chip. From this input sine wave, all other clocks are derived. Pipelined ADC, ΣΔ SHA, and ΣΔ operate at different frequencies as illustrated previously in Figure 6.1. The detailed operation of each building block is illustrated in Figure 8.1. Figure 8.1(a) and (b) show the schematic of the front-end with annotated clocks and the corresponding clock waveforms respectively. Pipelined ADC sampling clock, ϕ_{1s}, which is at the same frequency of the input differential clock, defines the sampling instance of the pipelined ADC; thus, minimum jitter of the pipelined ADC sampling clock is required. Figure 8.1(b) also shows the ΣΔ SHA clocks. The falling edges of the sampling clock, $\phi_{1,SH}$, and pipelined ADC sampling clock, ϕ_{1s}, have to be aligned precisely. The ΣΔ SHA clock is N times slower than the pipelined ADC sampling clock. This N determines the filter update rate of the LMS ADF. For flexibility, N is programmable to either 2^{14} or 2^{16} from off-chip during testing.

Besides sampling clocks, other clock phases for the pipelined ADC are also shown in the timing diagram. Odd and even stages of the pipelined ADC operate in alternate phases. It is important that the early phase of pipelined ADC clock, $\phi_{1,p}$, is aligned with the pipelined ADC sampling clock, ϕ_{1s}, because ϕ_{1s} drives the sampling switch of the first stage of the pipelined ADC, while $\phi_{1,p}$ drives the sampling switches of all odd stages and $\phi_{2,p}$ drives the sampling switches of even stages. ΣΔ clocks, which are M times slower than the pipelined ADC clocks, are shown at bottom of the figure. Note that this clock generation circuit only produces a single-phase clock $\phi_{1,\Sigma\Delta}$, and the circuit in Section 5.7



(a)



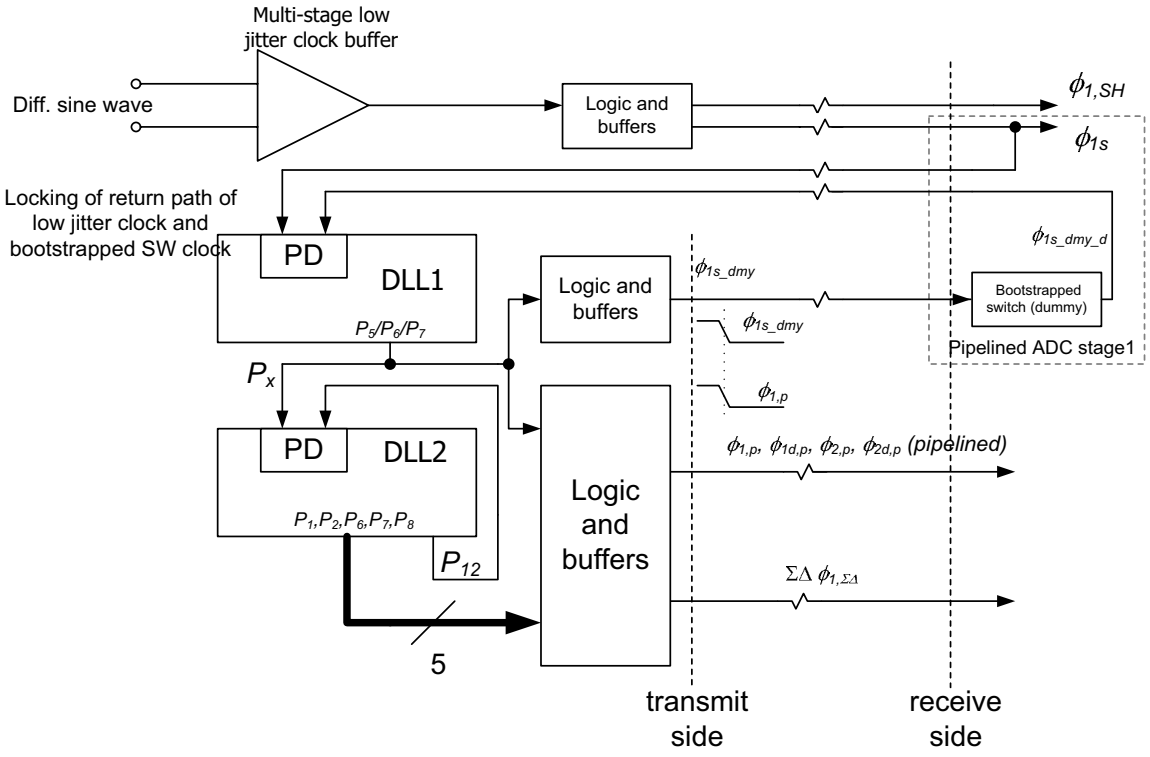
(b)

Figure 8.1: (a) ADC front-end with annotated clock signals, (b) timing diagram.

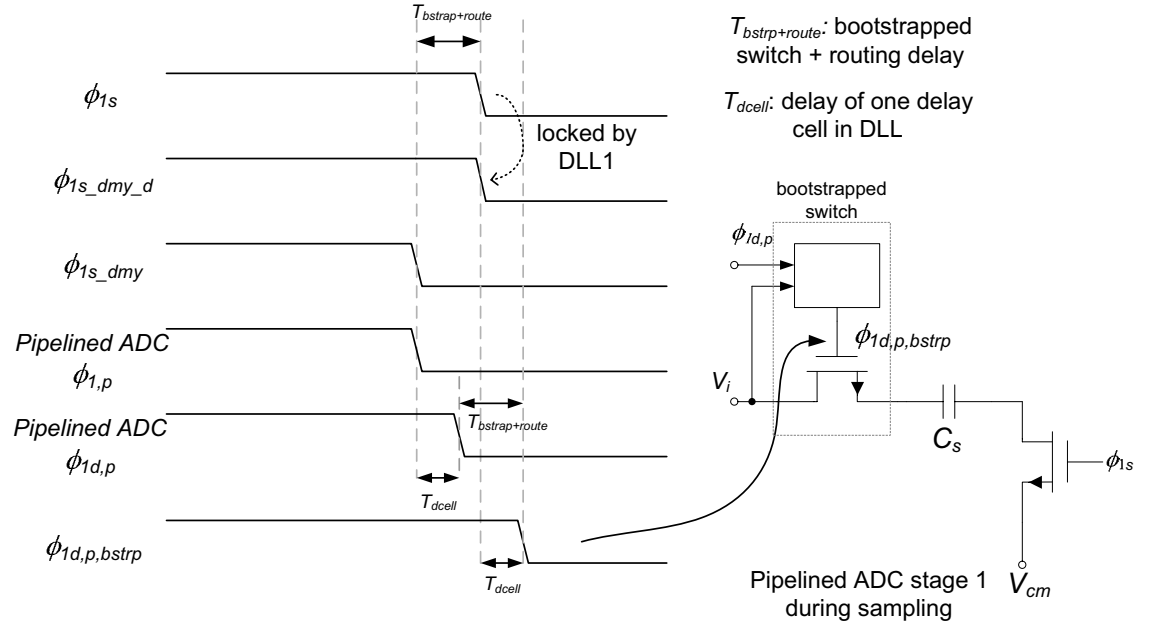
derives non-overlapping clock phases from it. Again, for testing purpose, the clock frequency is programmable. We can set M to either 2^4 or 2^6 from off-chip.

8.3 DLL-Based Clock Generator

A DLL-based clock generator is constructed to generate all the clocks described in the previous section. There are a few advantages for a DLL based clock generator. First, it can operate across a wide frequency range [73, 74]. Second, it can easily generate different multi-phase clocks needed by switched-capacitor circuits [71]. Figure 8.2(a) shows the interconnection of a low-jitter clock buffer and two DLLs for the clock generation for the proposed ADC. DLL1 is designed to absorb the bootstrapped switch delay at the bottom plate of the pipelined ADC stage 1 shown in Figure 8.2(b). As illustrated in Figure 8.2(b), when DLL1 is locked, the falling edges of pipelined ADC sampling clock ϕ_{1s} and the dummy clock $\phi_{1s\_dmy\_d}$ are locked by DLL1. Clock $\phi_{1s\_dmy\_d}$ is ϕ_{1s_dmy} after routing relay and bootstrapped switch delay, $T_{bstrap+route}$. The falling edges of clock ϕ_{1s_dmy} and pipelined ADC clock $\phi_{1,p}$ are aligned because they are derived from the same signal, P_x from DLL1. $\phi_{1d,p}$ is a delayed version of $\phi_{1,p}$ and the delay (T_{dcell}) is equal to the delay of a delay cell in the DLL delay line. Given that (a) $\phi_{1d,p}$ and ϕ_{1s_dmy} both pass through bootstrapped switches and (b) the falling edge of ϕ_{1s_dmy} and the falling edge of $\phi_{1,p}$ are aligned at the driver side, the clock signal $\phi_{1d,p,bstrp}$ is a delay T_{dcell} later than ϕ_{1s} as illustrated in 8.2(b). With this scheme, routing and bootstrapped switch delay is compensated, therefore the delay between an early phase clock (eg. ϕ_{1s}) and a delayed clock (eg. $\phi_{1d,p,bstrp}$) is controlled a delay line delay, T_{dcell}.



(a)



(b)

Figure 8.2: (a) Simplified block diagram of the clock generator, (b) locking of different clock phases.

Pipelined ADC clocks $\phi_{1,p}$, $\phi_{1d,p}$, $\phi_{2,p}$, and $\phi_{2d,p}$ are derived by combining different phases, namely phase P_x from DLL1 and phases P_1, P_2, P_6, P_7 and P_8 from the delay line in DLL2. Phase P_x can be selected to be phase P_5, P_6, or P_7 from DLL1 depending on the clock frequency. In Figure 8.2(a), pipelined ADC clocks $\phi_{1d,p}$ and $\phi_{2d,p}$ are delayed versions of pipelined ADC clocks $\phi_{1,p}$ and $\phi_{2,p}$ respectively. $\phi_{1,\Sigma\Delta}$ is fed to non-overlapping clock generator in Figure 5.16 to create all non-overlapping clock phases for the $\Sigma\Delta$ ADC.

8.4 Low Jitter Clock Buffer (LJCB)

Given that the maximum frequency operation of the DLL is 600MHz, it is very difficult to directly drive a square wave from off-chip. Therefore, a differential input sine wave is driven onto the chip, which is then clipped to become a square waveform by a chain of three *RC* loaded differential-pair amplifiers whose gains and *RC* values are set to minimize jitter induced by thermal noise.

8.5 All Digital DLL Architecture

Many all digital DLLs [74–77] have been published recently in literature. Figure 8.3 shows the basic digital DLL architecture used. The DLL contains two control loops: a fast, coarse acquisition loop (4 bits) and a fine, linear control loop (6 bits). The fast, coarse acquisition loop is based on a binary search algorithm that uses 12 clock cycles to quickly determine the range of input frequencies. Once this loop converges and stops, the control releases the linear loop that finely adjusts the total delay of the delay line until DLL is locked. The fine, linear control is always on after the coarse control loop has stopped. DLL

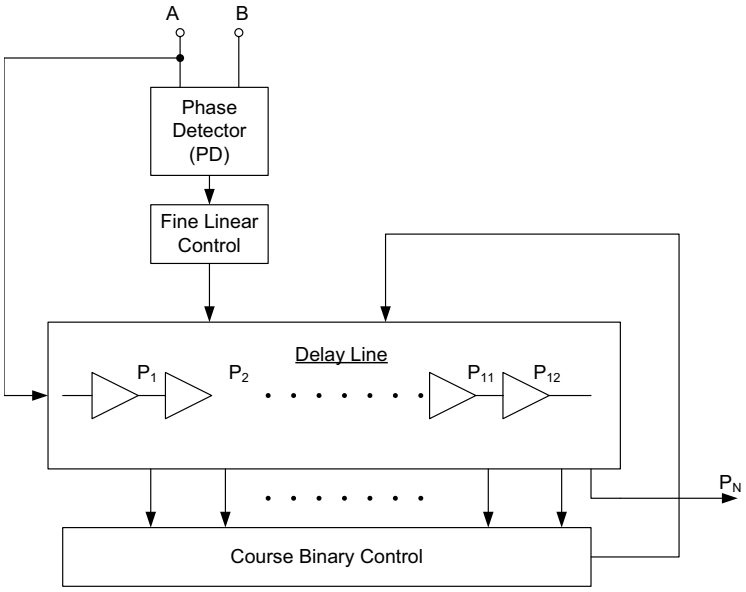


Figure 8.3: Block diagram of digital DLL architecture.

Table 8.1: Jitter at different frequencies.

Frequency	Peak-to-Peak Jitter
600MHz	$<$ 5ps
400MHz	$<$ 11ps
300MHz	$<$ 20ps
200MHz	$<$ 45ps
100MHz	$<$ 180ps

jitter is determined by the number of bits in the digital control. The linear loop uses a 6-b digital control, so a total of 10 bits are used in the representation of delay which allows a better jitter than 5ps peak-to-peak at 600MHz. The jitter increases quadratically with the inverse of clock frequency, resulting in increase in jitter as the clock frequency decreases. However, the jitter is not very critical as long as the non-overlapping between two phases is maintained. Table 8.1 lists the jitter at different frequencies.

8.5.1 Delay Line

A chain of 24 basic current starved inverters composes the delay line providing 12 uniformly distributed phases. The current starvation of the inverters is realized by digital to analog converters (DAC) whose input bits are determined by the control words provided by the coarse and fine control loops. The DAC used in the coarse loop is a 4-b binary weighted DAC whereas the DAC architecture used in the linear loop is a 6-b unit element DAC in order to guarantee a monotonically increasing transfer function, which is important for minimizing timing jitter.

8.6 Simulations

Simulations are performed to ensure that DLLs lock at different frequencies. To obtain more accurate simulation results, distributed RC model is used in extracting parasitics for long wires in the DLL loops while CC model is used for the rest. Figure 8.4 shows the locking of the two DLLs at 200MHz. The top graph plots the locking of ϕ_{1s} and $\phi_{1s\_dmy\_d}$ at the phase detector input in DLL1, while the bottom graph plots the locking of P_x and P_{12} at the phase detector input in DLL2.

8.7 Summary

We have presented a DLL-based clock generation circuit. It derives synchronized clocks for pipelined ADC, ΣΔ-SHA, and ΣΔ ADC from an external source.

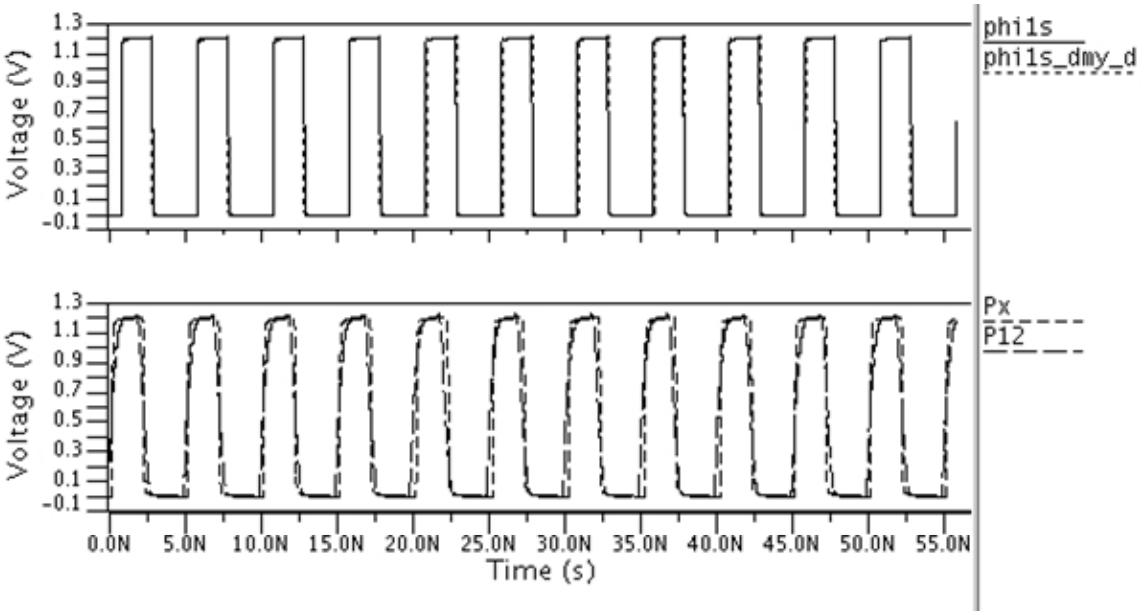


Figure 8.4: Locking of DLL1 and DLL2.

Chapter 9

Full-Chip Integration

9.1 Full-Chip Floor Planning and Signal Routings

The floor plan of the ADC prototype is shown in Figure 9.1. The ΣΔ-SHA and the pipelined ADC stage 1 are placed side-by-side, and the input differential signal is fed from the bottom to both blocks for sampling. The ΣΔ ADC is placed at the left of the SHA.

The differential input clock is fed from the top left side of the chip to the clock generator. Sampling clocks of the ΣΔ ADC and the pipelined ADC are routed carefully to ensure that they both experience the same wire delay. The delay is verified through extensive RC extracted simulations. Reference voltages for the pipelined ADC are routed from the top center of the chip to different pipelined ADC stages. All references are bypassed with MOS capacitors on the chip. To reduce wire resistance, very wide, multiple layers of metal lines are used to route reference signals and power supplies. The outputs from ΣΔ ADC and pipelined ADC are brought off-chip through LVDS pads on the right side of the

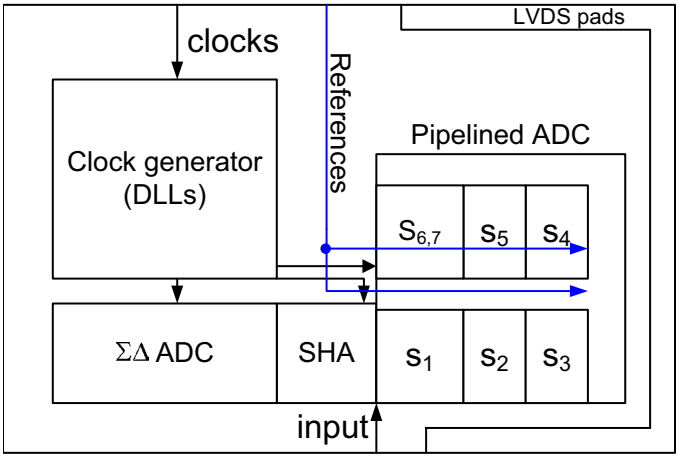


Figure 9.1: Full-chip floor plan.

chip.

9.2 Front-end Sampling Networks

To ensure good matching between the reference and the main signal paths, a replica switched-capacitor S/H structure is used by the SHA to mimic that of the pipeline. This also minimizes the systematic sampling clock skew existed in between the paths. SHA and pipelined ADC further share the same analog supply. In addition, both paths are drawn carefully to minimize clock skew as shown in Figure 9.2. Note that a sampling clock skew may exist at the front-end between the ΣΔ-SHA and the pipelined ADC. As long as the resulting sampling error exhibits a symmetrical probability distribution in the long term, the effect is removed by accumulators of the LMS loop. Sampling capacitors of the pipelined ADC and the SHA are 2pF and 0.5pF respectively.

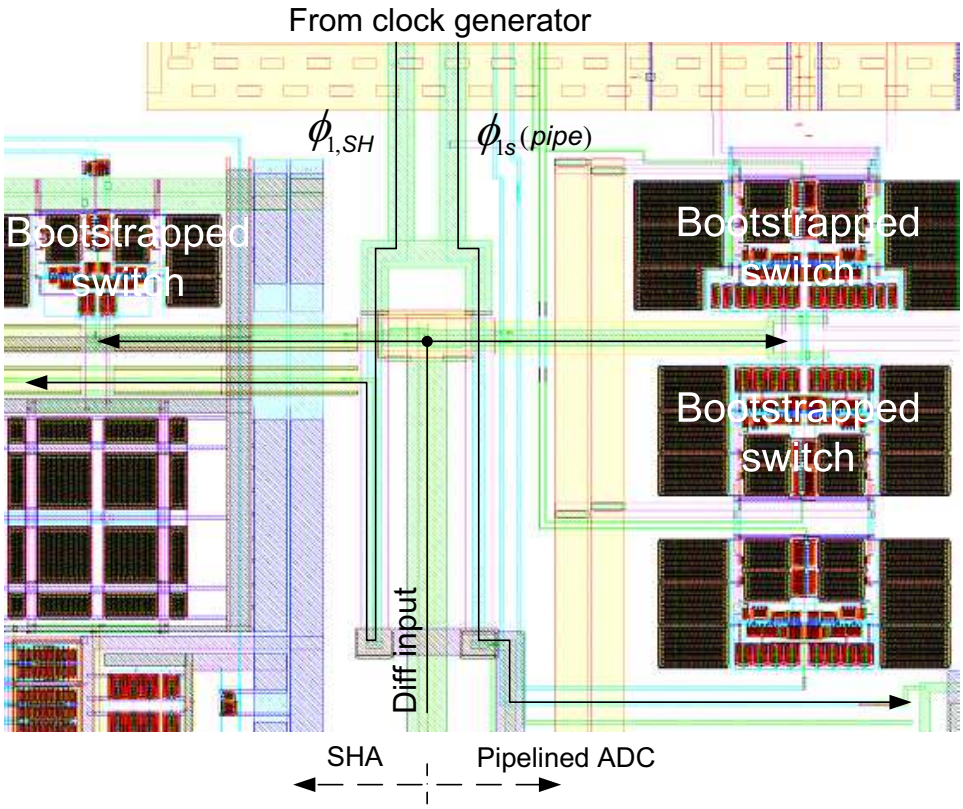


Figure 9.2: Layout of the input path and sampling clocks.

9.3 Simulations

After placing and routing all building blocks, post-layout simulations are performed to verify all clocks in the reference ADC, and the pipelined ADC are working correctly across different frequencies. Figure 9.3 shows the falling edges of the sampling clocks of the SHA and the pipelined ADC. We run post-layout simulation to ensure their falling edges aligned with no skew at least in simulations. Some clocks swing above *VDD* because these clocks are bootstrapped. Figure 9.4 shows different clock phases for the ΣΔ ADC. $\phi_{1,\Sigma\Delta}$ rises from 0V to *VDD* after $\phi_{1,SH}$ has transition from *VDD* to 0 completely. This guarantees that ΣΔ ADC does not disturb the SHA until sampling switches of the

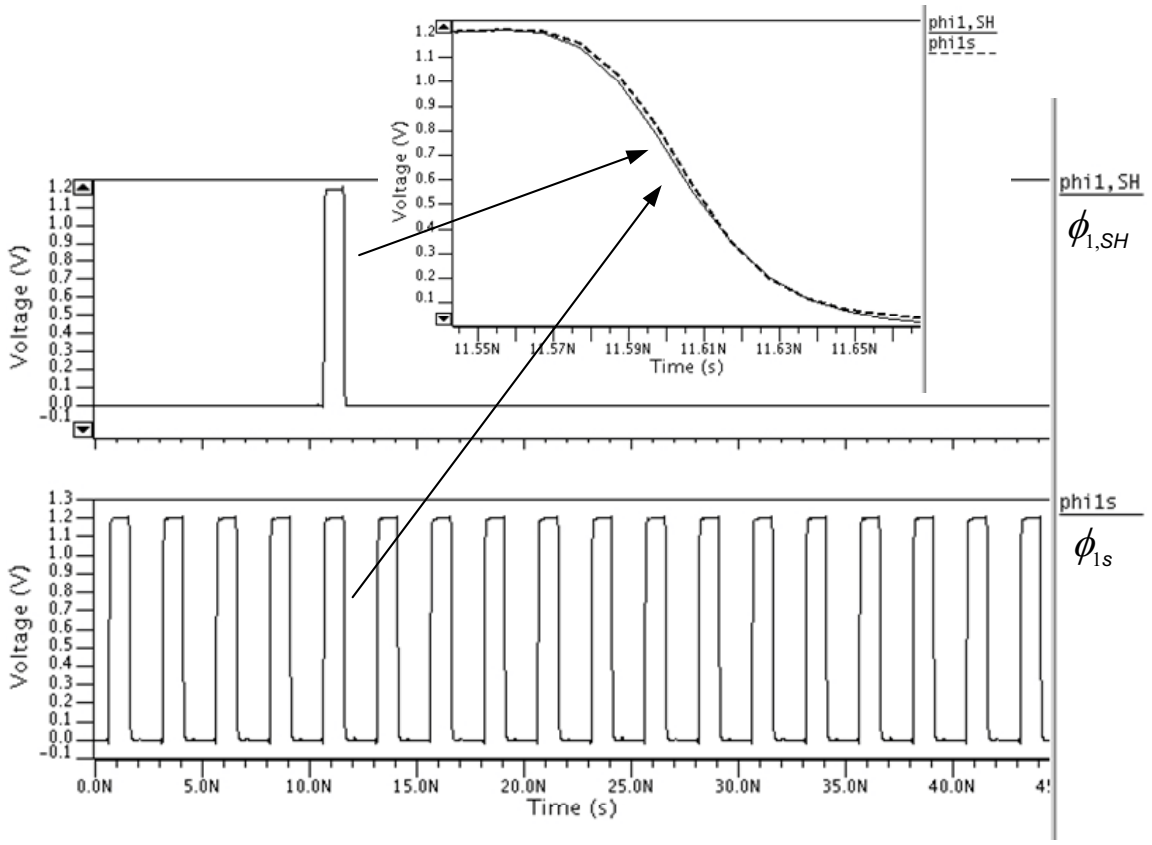


Figure 9.3: Post-layout simulation of SHA and pipeline ADC sampling clocks (f_s=400MHz).

SHA are completely off. Figure 9.5 shows simulated different clock phases for stage 1 of the pipelined ADC.

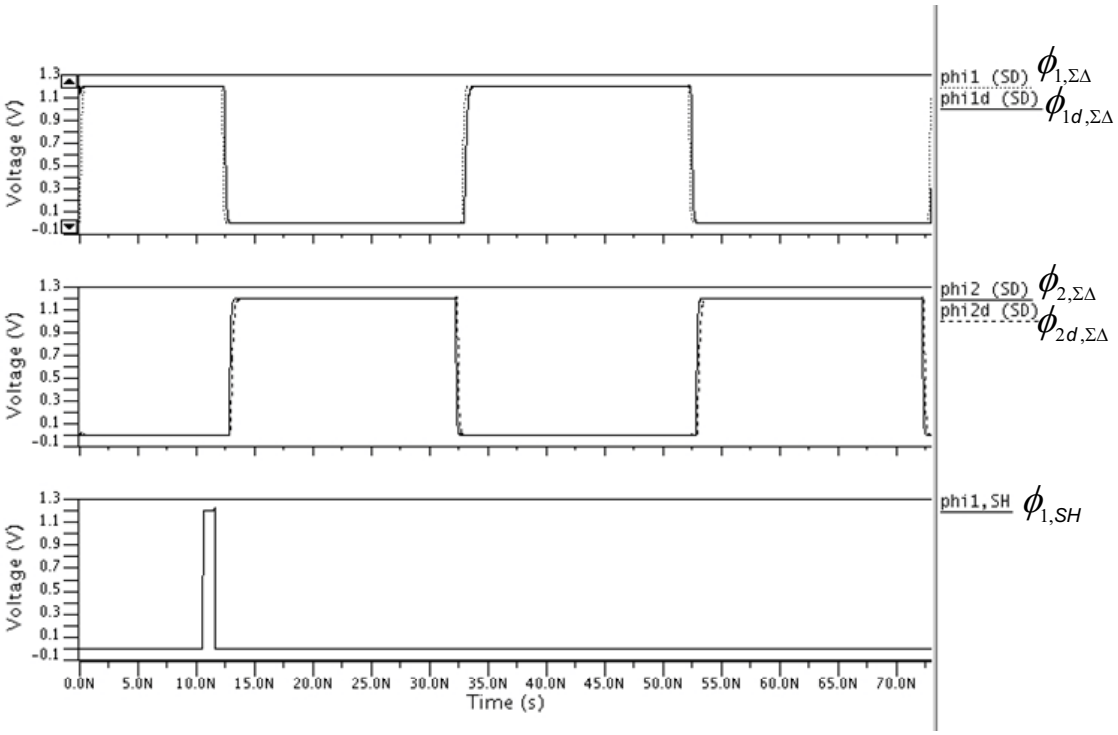


Figure 9.4: Post-layout simulation of non-overlapping clock phases for $\Sigma\Delta$ (f_s=400MHz).

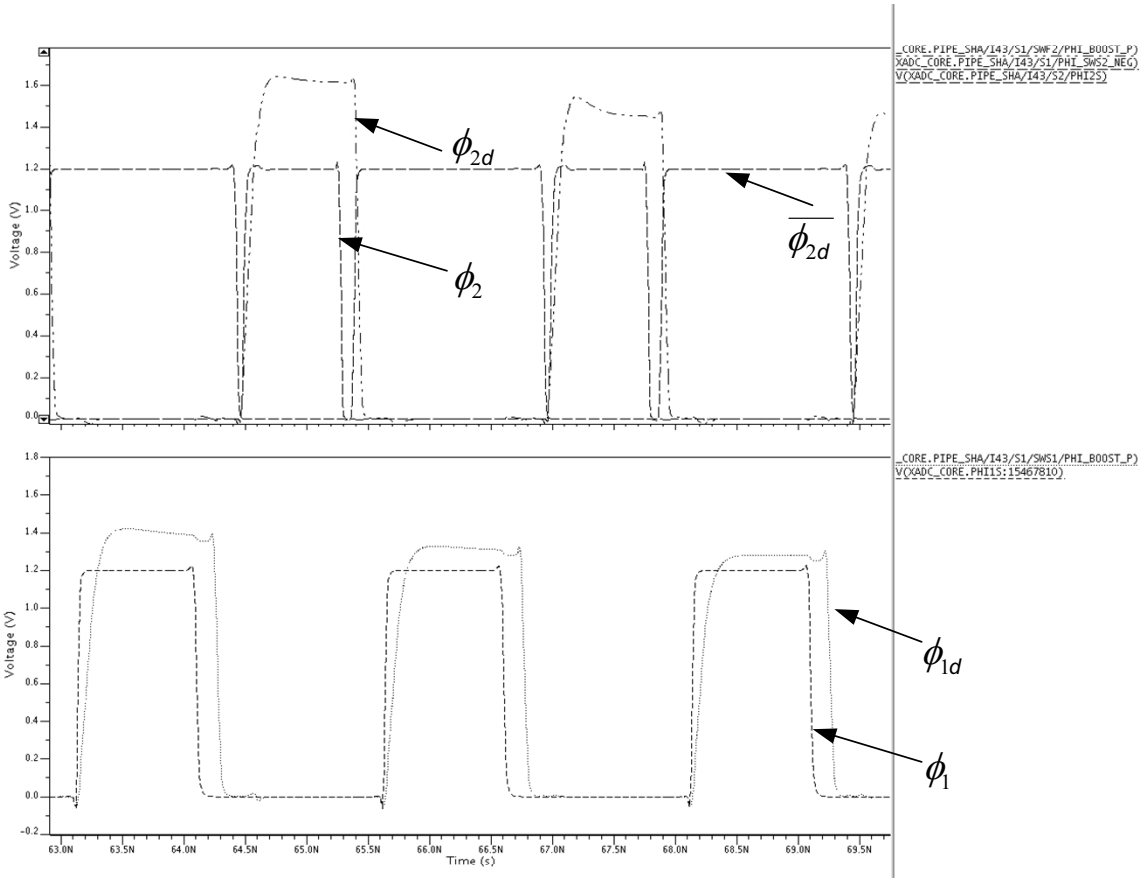


Figure 9.5: Post-layout simulation of non-overlapping clock phases for pipelined ADC stage 1 (f_s=400MHz).

Chapter 10

Digital Filters

10.1 Introduction

This chapter discusses the design of the ΣΔ ADC decimation filter and the least-mean-square (LMS) adaptive digital filter (ADF). Both filters are implemented using Xilinx FPGA blocks under Simulink®. Using Xilinx FPGA blocks not only enables bit-true and cycle-true computer simulation, but also facilitates our chip testing process. During chip testing, LMS ADF and decimation filter are programmed on a Xilinx FPGA; outputs from the ΣΔ ADC and the pipelined ADC are fed to the FPGA board for processing in real time. FPGA also gives us flexibility to modify the filters easily.

10.2 Digital Filter Implementation

Figure 10.1 shows the code-domain calibration scheme of pipelined ADCs in more detail. The digital filter consists of a decimation filter and an LMS ADF. The decimation

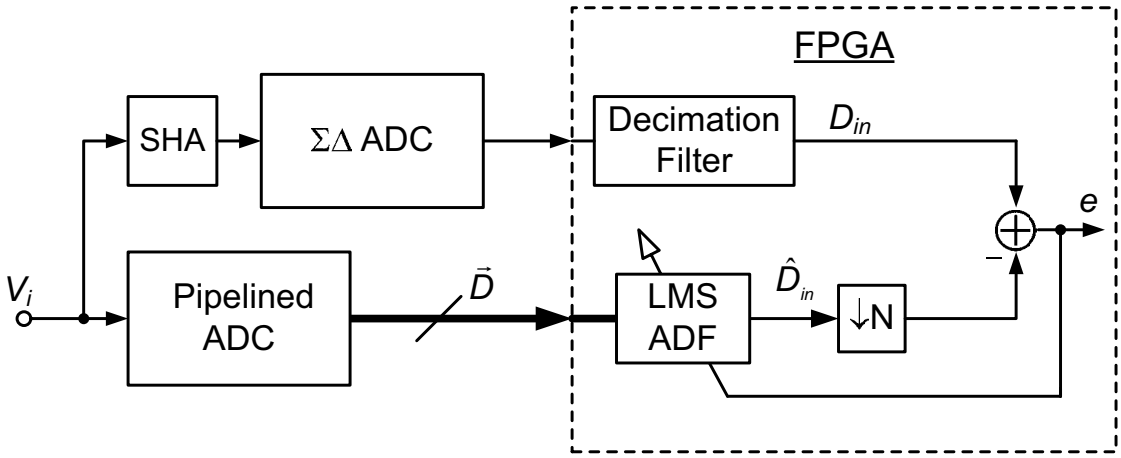


Figure 10.1: Nonlinear adaptive digital calibration of pipelined ADCs.

filter attenuates out-of-band quantization noise in ΣΔ modulator and decimates the signal. The LMS ADF uses the error signal which is the difference of the desired output (D_{in}) and the estimate from ADF ($\widehat{D}_{in}$) to drive coefficient update of the LMS ADF.

10.2.1 Decimation Filter

Coefficients of the decimation filter are synthesized using Matlab® filter toolbox. Then, the filter is implemented by Xilinx FPGA blocks under Simulink. The output of the ΣΔ modulator is decimated by 64×.

10.2.2 LMS ADF

The goal is to design an LMS ADF which is sufficient for calibration need with minimum power consumption and chip area. Although we can implement the filter directly in an expanded form according to (2.16), i.e., the recursion is unrolled, it is simpler and more manageable to implement the filter recursively according to (2.15). The block diagram

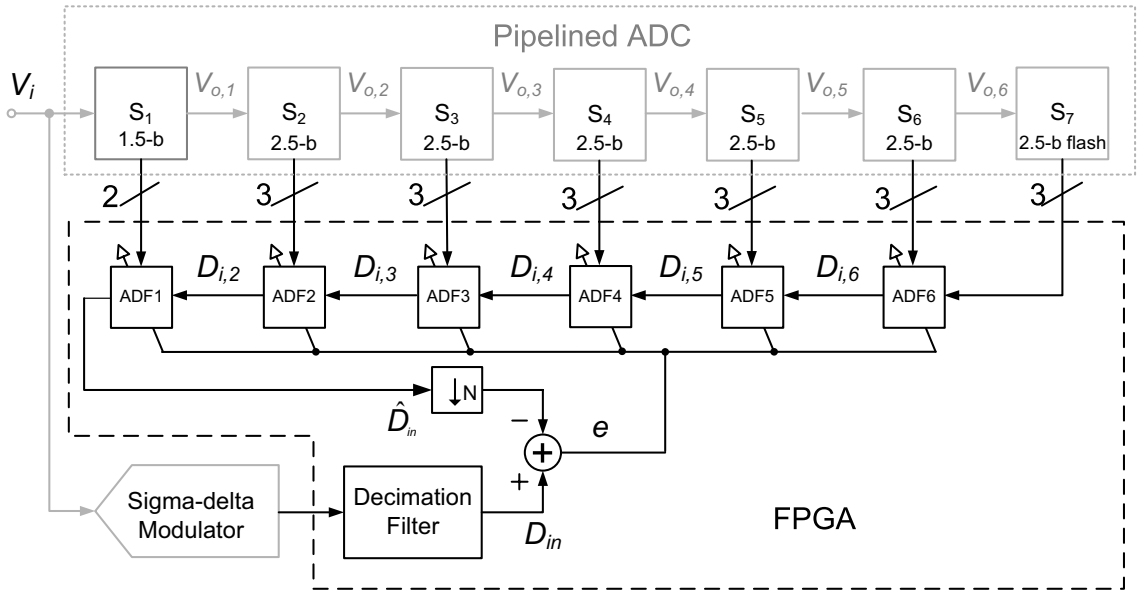


Figure 10.2: Reverse pipelining of multi-stage adaptive digital filter.

of the recursive filter is illustrated in Figure 10.2. The pipelining of the ADF is the reverse of the pipelined ADC; filter output from ADF for the LSB stage is fed to the input of ADF for the next MSB stage. Recursive calibration makes word-length optimization of the filter easier because digital word truncation accuracy for each stage is easily determined because the expected accuracy from each pipelined stage is known. In a pipelined ADC, requirements of analog components such as amplifier gain and capacitor matching are most stringent in MSB stages. Thus, we tailor the ADF with the need of each stage. Nonlinear op-amp gain error is calibrated in the first two stages, while only linear op-amp gain error is calibrated in the rest stages. Capacitor mismatch is not calibrated from stage 3 and on.

The nonlinear ADF for the 1.5-b first stage (ADF1) is illustrated in Figure 10.3. d_1 is the decision of stage 1. $D_{os,1}$ is a constant used to find the offset filter tap adaptively. $D_{i,2}$

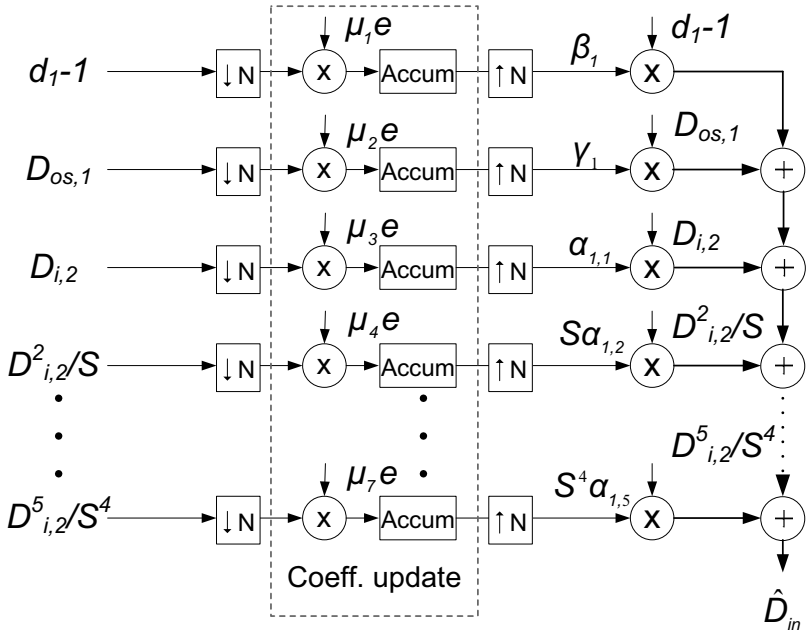


Figure 10.3: Simplified coefficient update diagram for the first pipeline stage (1.5-b). Parameter S is a constant scaling factor.

is the output from the ADF for stage 2 (ADF2). Since the LMS ADF coefficient update is N times slower than the pipelined ADC sampling rate, the power consumption is negligible. The implementation of the filter in Simulink is shown in Figure 10.4. The top portion is the LMS ADF coefficient update, and the lower portion is the filtering of pipelined ADC codes. The later is running at the sampling rate of the pipelined ADC under calibration although filter coefficients are only updated every N samples.

The nonlinear ADF for the 2.5-b second stage is illustrated in Figure 10.5, and its Simulink implementation is in Figure 10.6. Since this is a 2.5-b/stage architecture, three capacitor ratios, β_1 β_2, and β_3 require calibration. This portion involves decision from current stage, a_1, a_2, and a_3. The digital filter adaptively derives the coefficients corresponding to capacitor ratios and op-amp gain but not the offset coefficient (γ) because

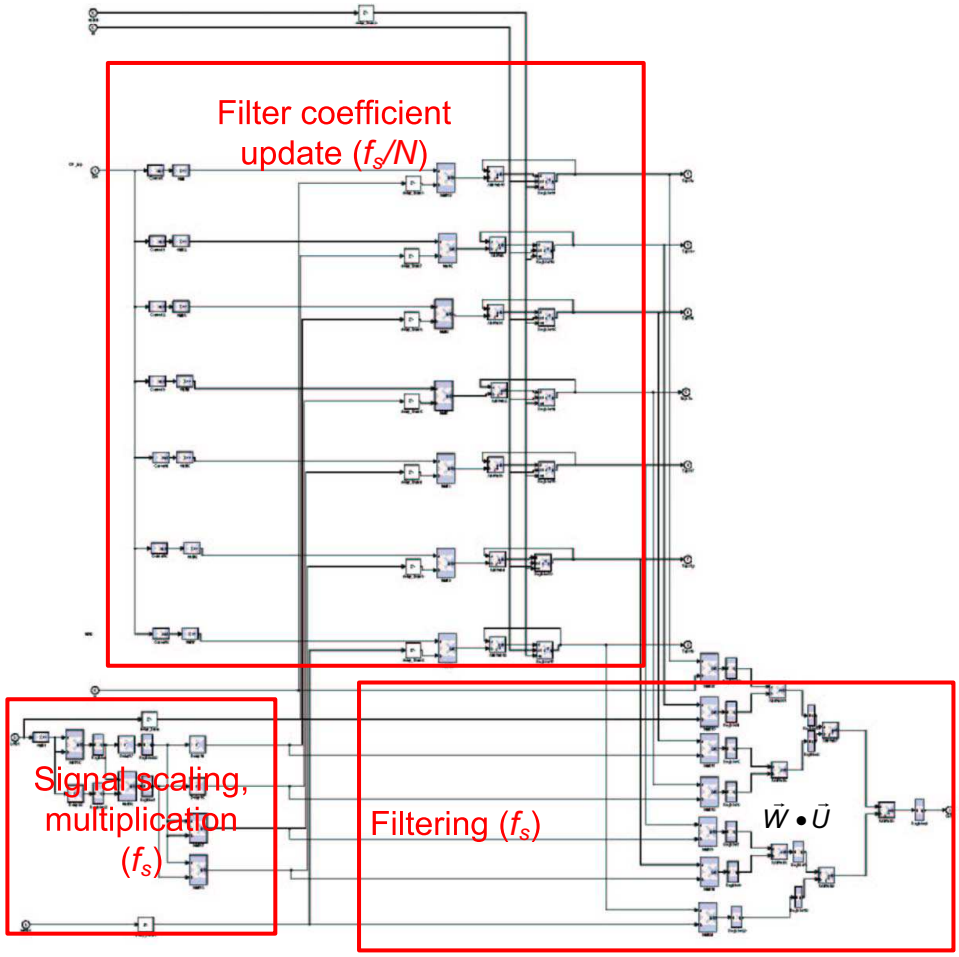


Figure 10.4: Simulink design for nonlinear ADF for 1.5-b/stage architecture.

offsets from all stages are lumped together as a single term in ADF1. As amplifier gain requirement and capacitor matching are more relaxed in later stages, a linear version, which does not have the second-order and higher-order terms, is employed. The formulation of the linear version of the calibration filter is given by (2.7).

This recursive filter searches for the coefficients adaptively by LMS algorithm.

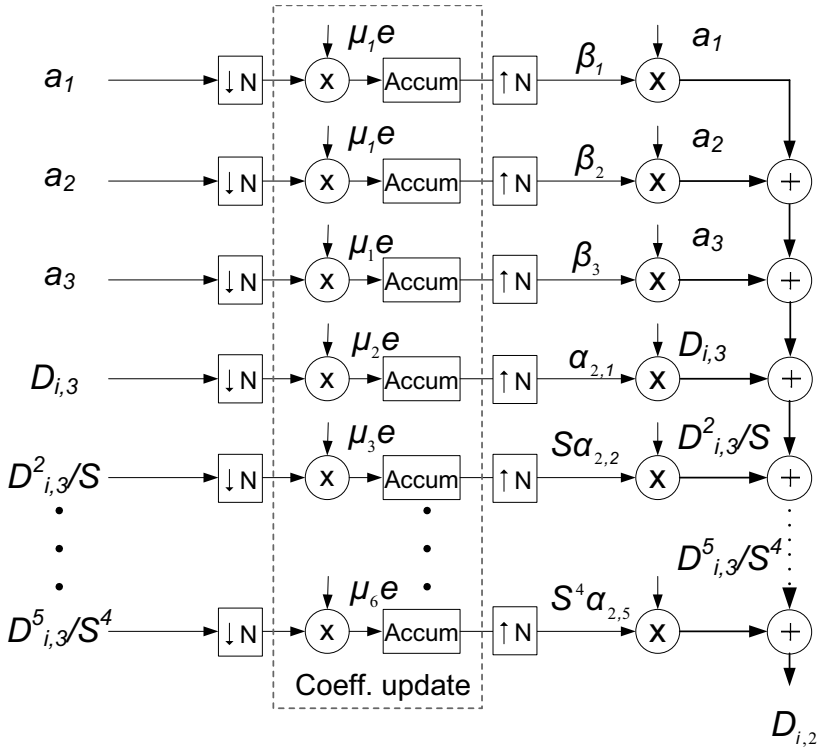


Figure 10.5: Simplified coefficient update diagram for the second pipeline stage (2.5-b). Parameter S is a constant scaling factor.

Generally, LMS filter coefficient update is given by [35]

$$\vec{W}(n) = \vec{W}(n-1) + e(n) \cdot \vec{\mu} \cdot \vec{U}(n) \tag{10.1}$$

where $\vec{W}$ is the filter weights, e is the error, $\vec{\mu}$ is the step size, and $\vec{U}$ is the input signal vector. In ADF1 shown in Figure 10.2 , $\vec{W}$ are the coefficients, α, β etc, in (2.10); $\vec{U}$ are decision d_1 from S_1, $D_{os,1}$, $D_{i,2}$ from ADF2 and its scaled powers as shown in Figure 10.3; e is the difference between the decimator output and the LMS ADF output. In actual implementation, decisions from all stages, d_1 from S_1, $a_1{}'s$, $a_2{}'s$, and $a_3{}'s$ from S_{2-6} are scaled by their equivalent weights of the pipeline stage such that $\beta' s$ and op-amp linear gain

Table 10.1: Word-length of calibration filter for different stages.

Filter for calibrating stage	Max. WL in coeff. update	Max. WL in filtering
1	36	23
2	36	22
3	36	20
4	36	18
5	36	14
6	36	12

taps $\alpha_{k,1}$ are equal to one for an ideal pipelined ADC.

Filter Digital Word-Length (WL) Optimization

Word-length of LMS ADF needs to be optimized to minimize power consumption and chip area. As mentioned earlier in Section 10.2.2, recursive calibration facilitate digital word-length optimization in the LMS ADF because precision of each stage is known, i.e., MSB stages require the longest word-length, while LSB stages require the shortest word-length. This is from the fact that SNR of MSB stages is higher than that of the LSB stages; the word-length truncation error needs to be smaller than the error from the ADC itself. Extensive simulations are carried out to shorten the word-length but the filter still maintains the required accuracy. Optimization process is carried out as follows. First, we estimate the word-length requirement for each stage. Then, we compare the simulation result with that of the floating-point Simulink model to ensure that there is no SNR degradation in the calibrated ADC. Next, we start shortening the word-length of the filter building blocks until a significant degradation is observed.

Table 10.2: Error correction of each stage.

Stages	Nonlinear op-amp gain error	Linear op-amp gain error	Capacitor mismatch	# of taps
1	Yes	Yes	Yes	7 (with offset tap)
2	Yes	Yes	Yes	8
3-6	No	Yes	No	5 (total)

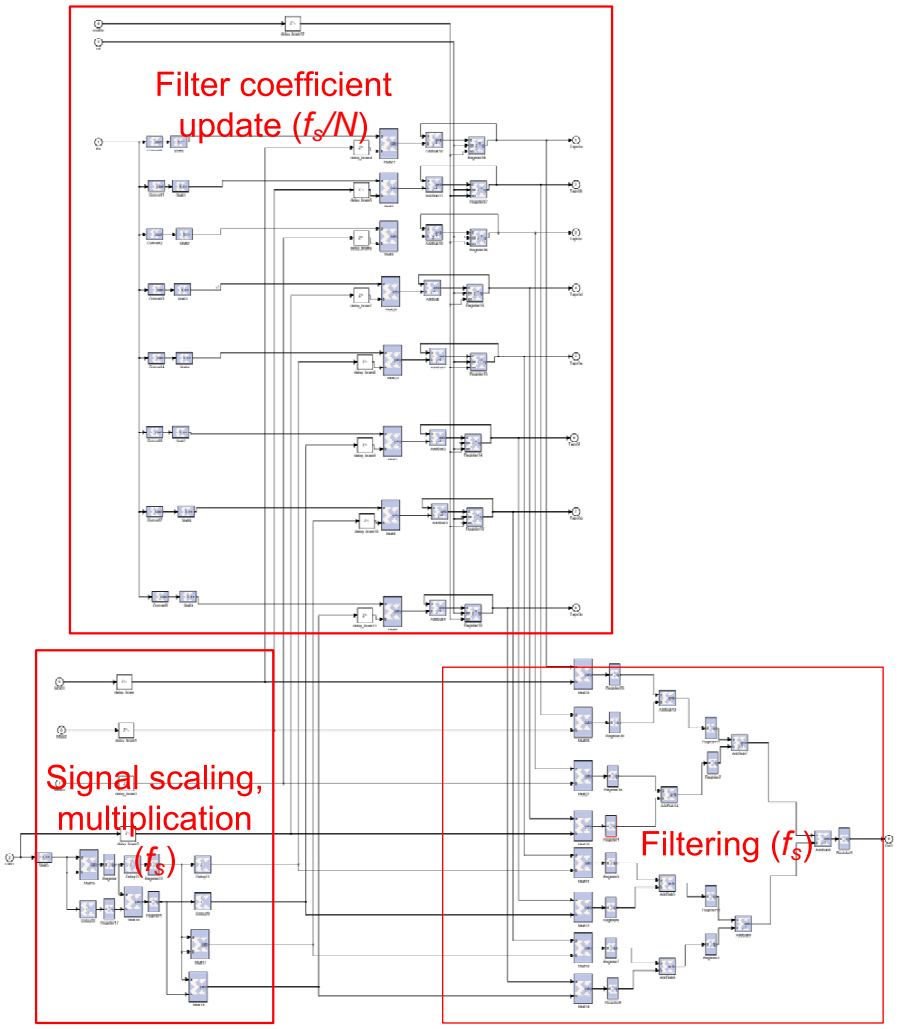


Figure 10.6: Simulink design for nonlinear ADF for 2.5-b/stage architecture.

Table 10.3: Estimated power and area(downsampling ratios N=2^{14}, M=2^4).

Speed	100MHz (f_s)
Power supply	1.1V
Process	ST90nm CMOS
Estimated Power	7mW
Estimated Area	1.4mm×1.4mm

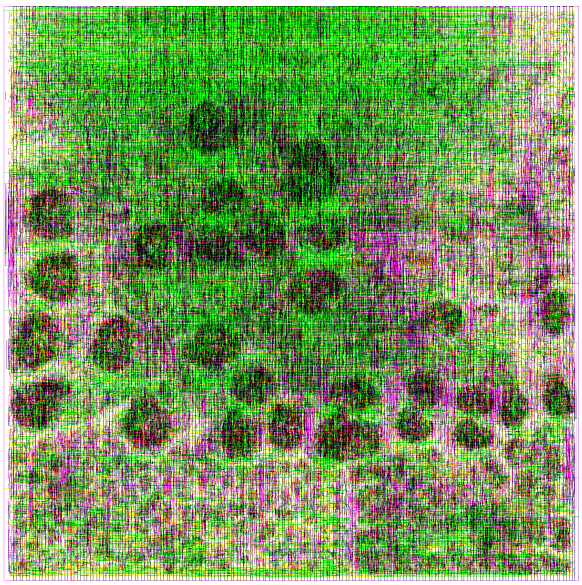


Figure 10.7: Synthesized layout of the LMS ADF and the decimation filter in 90nm CMOS process (1.4mm×1.4mm).

Speed, Power, Silicon Area

As discussed earlier in the section, part (a) the signal scaling and filtering portion operates at the speed of the pipelined ADC, f_s, while part (b) the coefficient update portion operates at f_s/N. All multiplications involve adaptive update of taps $\beta's$ can be implemented with negations and shifts because the pipelined stage decisions d_1, a_1, a_2, and a_3 are either -1, 0, 1, or 2. If the filter is implemented in silicon, the part (b) consumes most of the power, while part (a) consumes a small portion of the total power. Although, this digital filter is not fabricated in silicon, the power and area are estimated in 90nm CMOS digital process. With analog circuit impairments listed in Table 10.2 being calibrated, the estimated power and area are shown in Table 10.3. Since capacitor mismatch in stages 3-6 does not require calibration, the recursion of these stages are unrolled to make the filter implementation simpler. The last five stages only require five filter taps. The total number of taps is 20. The synthesized layout of the digital filter in 0.90nm CMOS process is shown in Figure 10.7. Since we only want to get a fast estimate of the power and the area, these estimates are far from optimal design.

10.3 Conclusion

In this chapter, the design of the LMS ADF and the decimation filter is presented. Power and area of the filters are estimated in 90nm CMOS process. The power of consumption for the filter coefficient is only a small fraction of the total power because the update of the coefficients runs at a slower rate than the ADC speed.

Chapter 11

Measured Results

11.1 Introduction

Experimental results are presented in this chapter. First, measured results of the stand-alone ΣΔ ADC test chip, which was fabricated independently, are presented. Then, measured results of the complete background calibrated ADC system are followed.

11.2 ΣΔ ADC

The stand-alone 2-1 MASH ΣΔ ADC was fabricated in 0.13μm CMOS triple-well process technology with 1.2V supply. The prototype core area is 1.51mm^2 (Figure 11.1), and the die including the pads occupies 2.52mm^2. As a part of the reference ADC for the proposed calibration framework, the key performance metric of the ΣΔ ADC is the linearity when converting DC signals held by the preceding dedicated SHA. Although the SHA is not present in the test chip, the linearity of the ΣΔ ADC can be characterized by

examining harmonic distortion (HD) of the converter using conventional dynamic testing for ΣΔ ADCs.

11.2.1 Packaging and Test Setup

The chip is assembled in a 44-pin TQFP package. The bonding diagram is shown in Figure 11.2 The die is aligned close to upper left corner to minimize the length of bond wires for critical signals such as references and input.

The test setup for the stand-alone ΣΔ ADC is shown in Figure 11.3. The packaged chip is mounted on a custom-designed printed circuit board (PCB). All the power supplies to the chip are regulated on the PCB. To attenuate harmonic distortion from signal source, the single-ended input signal is filtered by a bandpass filter before being converted to a differential signal by a balun on the board. The chip receives the differential signal from the balun, and the clock is generated from a pulse generator. Digital outputs from the chip are captured by a logic analyzer and then exported to a personal computer for analysis.

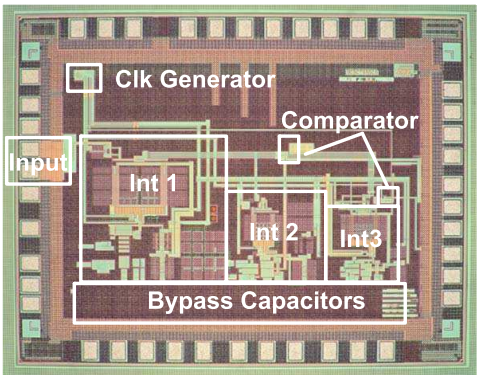


Figure 11.1: Stand-alone ΣΔ ADC die micrograph.

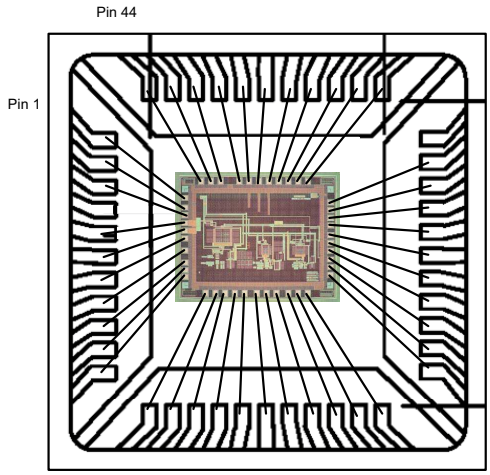


Figure 11.2: Stand-alone ΣΔ ADC bonding diagram.

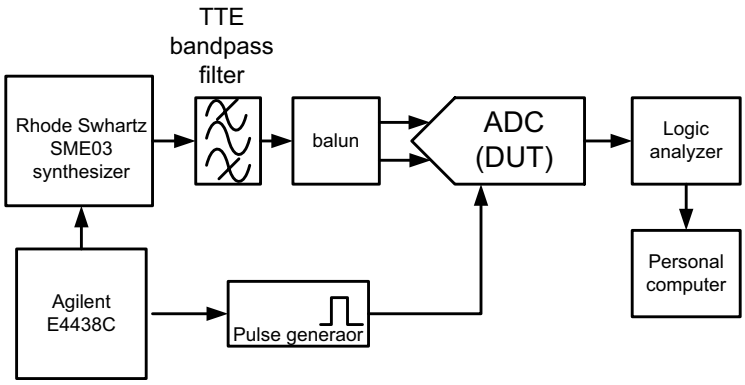
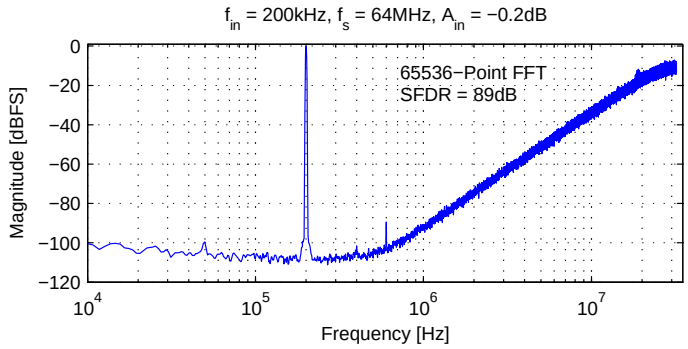


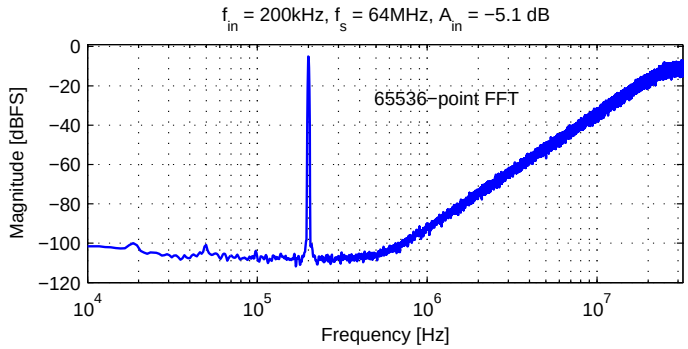
Figure 11.3: Stand-alone ΣΔ ADC test setup.

11.2.2 Experimental Performance: Stand-alone ΣΔ ADC

The full-scale input voltage of this modulator is $1V_{pk-pk}$, and the references are 1.2V and 0V. Figure 11.4 plots the measured PSD of a 200kHz input signal with 64MHz sampling frequency at -0.2dBFS and -5dBFS input levels. Figure 11.5 plots the measured SNDR versus the input level at 200kHz. At an oversampling ratio of 64, the peak SNDR is 84dB with a full-scale input. The DR is also 84dB. The peak SFDR is 96dB. For 300kHz and 400kHz input frequencies, the peak SNDR is still 84dB. Table 11.1 summarizes the



(a)



(b)

Figure 11.4: Measured PSD at 64MS/s and 200kHz input: (a) -0.2dBFS input level, (b) -5.1dBFS input level.

performance of the experimental chip. The FOM ($FOM = \frac{Power}{2 \times BW \times 2^{ENOB}}$) of this converter is 0.83pJ/conversion-step.

Table 11.1: Measured performance summary of the stand-alone 2-1 MASH $\Sigma\Delta$ ADC.

Full-Scale Voltage (pk-pk)	$\pm$0.5V
Sampling Frequency	64MHz
Oversampling ratio (M)	64
VDD	1.2V
Process	0.13μm CMOS
Linearity	96dB peak SFDR
Power	10mW

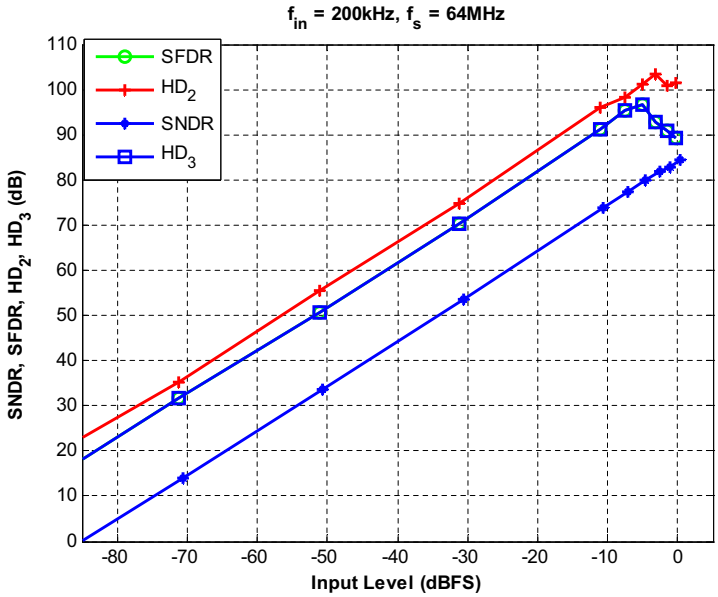


Figure 11.5: Measured performance vs. input level.

11.3 Background Calibrated ADC

11.3.1 Chip Layout and Wire Bonding

The analog portion of the prototype background calibrated ADC including the clock generation circuit, SHA + $\Sigma\Delta$ ADC, and the pipelined ADC was fabricated in a triple-well 0.13μm digital CMOS process without analog options. Capacitors of the switched-capacitor circuits are implemented using fingered-metal capacitor (MOM). A micrograph of the 3.7mm$\times$4.7mm chip is shown in Figure 11.6. Different components of the prototype are labeled in the figure. The chip is directly attached to a custom-designed PCB and is bonded using chip-on-board (COB) technology. The bonding diagram of the prototype is shown in Figure 11.7.

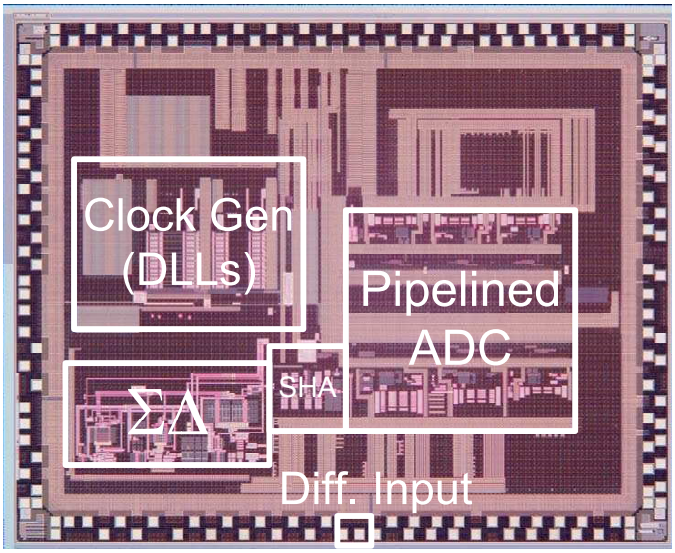


Figure 11.6: Background calibrated ADC die micrograph (3.7mm×4.7mm).

11.3.2 Test Setup

The test setup for experimental testing is shown in Figure 11.8. The chip is attached and bonded directly on the PCB using Chip-on-Board(COB) technology to minimize the bond wire length.

The master clock and the ADC input signal are generated using high-performance RF generators. The clock and the ADC input signal are converted from single-ended sinusoids to differential signals using baluns on the PCB. For the input signal, spurious components in the signal source are rejected using bandpass filter from TTE [78].

Raw outputs from the ΣΔ ADC and the pipelined ADC are exported continuously from the chip using LVDS pads through a high-speed z-dok [79] connector to an FPGA board called IBOB. The LMS ADF implemented in the FPGA calibrates the pipelined ADC using codes from the reference ADC in real time. A personal computer is used to control the FPGA and to analyze the results.

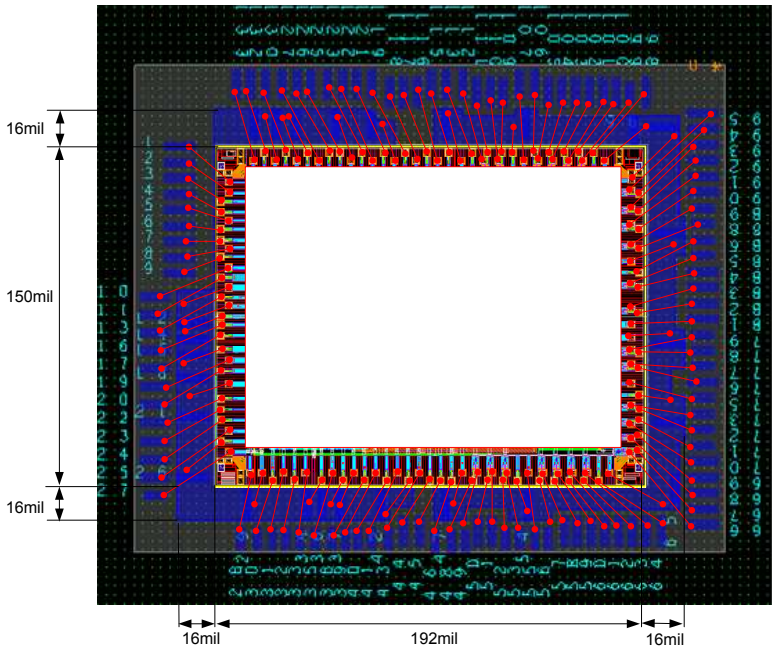


Figure 11.7: Background calibrated ADC bonding diagram.

11.3.3 Measured Performance

LMS ADF Convergence

In experiments, nonlinear residue gain errors up to the 5th-order in stage 1 and 2 are calibrated, while only linear gain errors require calibration for the remaining stages. Capacitor mismatch in only stages 1 and 2 requires calibration. Figure 11.9 shows the convergence of linear filter coefficients for OTA gain for all pipelined ADC stages. With a full-scaling input sinusoid, the LMS ADF converges after approximately 50k adaptations. The filter adaptation rate is the conversion rate of the reference ADC, i.e., the sampling rate of the dedicated SHA, which is at $f_s/2^{14}$. The convergence time is equivalent to approximately eight seconds running at 100MS/s in this prototype. In experiments, the $\Sigma\Delta$ ADC is running at $f_s/2^4$. The reference ADC is designed to be able to operate at

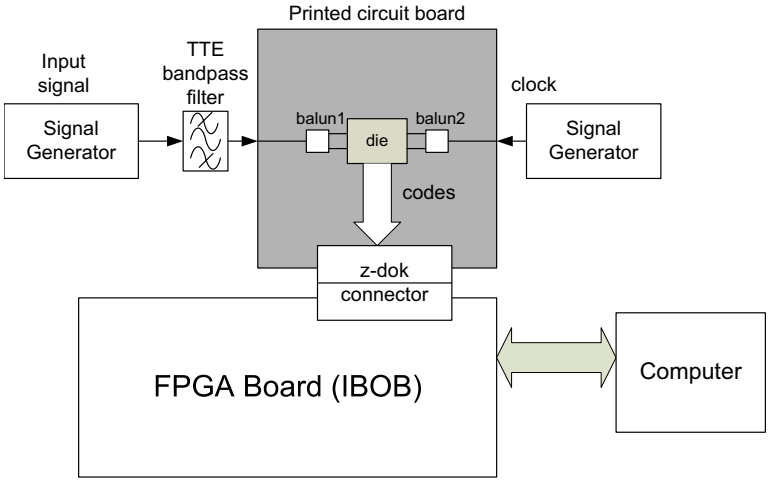


Figure 11.8: Background Calibrated ADC test setup.

$f_s/10^{10}$. However, the downsampling factor N could only be selected to either 2^{14} and 2^{16} in our prototype. Otherwise, the convergence time should be 16 times shorter.

Static Performance

Figure 11.10 plots the DNL and INL of the prototype ADC before calibration. There are many missing codes (DNL=-1) in the ADC transfer function due the low-gain amplifiers in the pipelined ADC. Big jumps in INL before calibration are also caused by low DC gains of the amplifiers. Figure 11.11 plots the DNL and INL of the prototype after calibration. The calibration removes all missing codes and improves the DNL to within 1LSB at 10-b level. The worst INL improves from -34.6LSB to -1.1LSB.

Dynamic Performance

Figure 11.12 shows the power spectral density (PSD) of (a) the reference ADC, the pipelined ADC (b) before and (c) after calibration with 1.35V analog supply. The

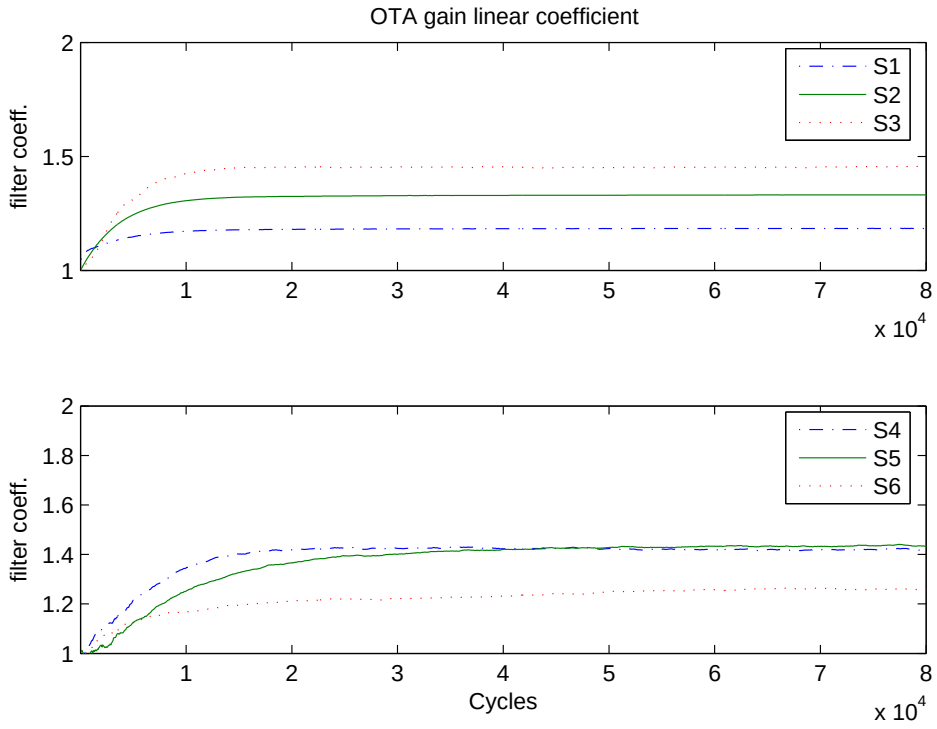


Figure 11.9: Measured convergence of OTA linear gain filter coefficients (one cycle = $\frac{1}{f_s/2^{14}}$).

input frequency is 411kHz and the sample rate of the pipelined ADC is 100.12MS/s. Before calibration, the SFDR is limited by HD_3 at -29.8dB; after calibration, the HD_3 drops to -72.2dB, and the SFDR is limited to 67.8dB by a spur at $f_s/2$. Without this $f_s/2$ spur, the new SFDR is 72.2dB. The SNDR improves from 28.1dB to 59.4dB after calibration. Results of a similar experiment performed on a 49MHz input are plotted in Figure 11.13, wherein the SNDR improves from 29.4dB to 54.8dB and the SFDR improves from 31.7dB to 63.4dB.

Figure 11.14 shows the measured (a) SNDR and (b) SFDR vs. the input frequency (f_{in}) before and after calibration at 100MS/s. The measured SNDR and SFDR of the reference ADC are also shown in the figure. Since the SNDR and SFDR before calibration are all below 35dB, any performance degradation from higher f_{in} is masked. Therefore, the

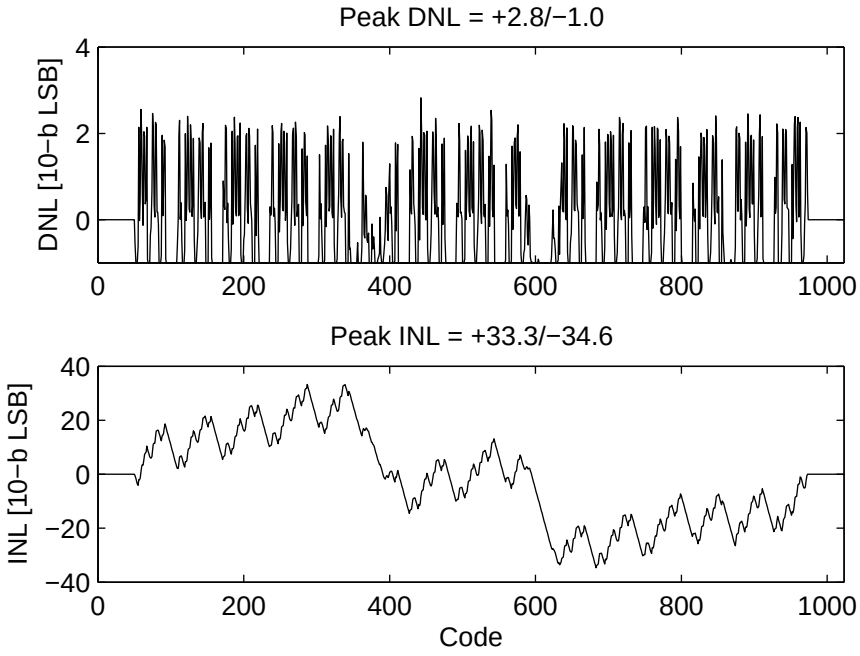


Figure 11.10: Measured DNL and INL before calibration.

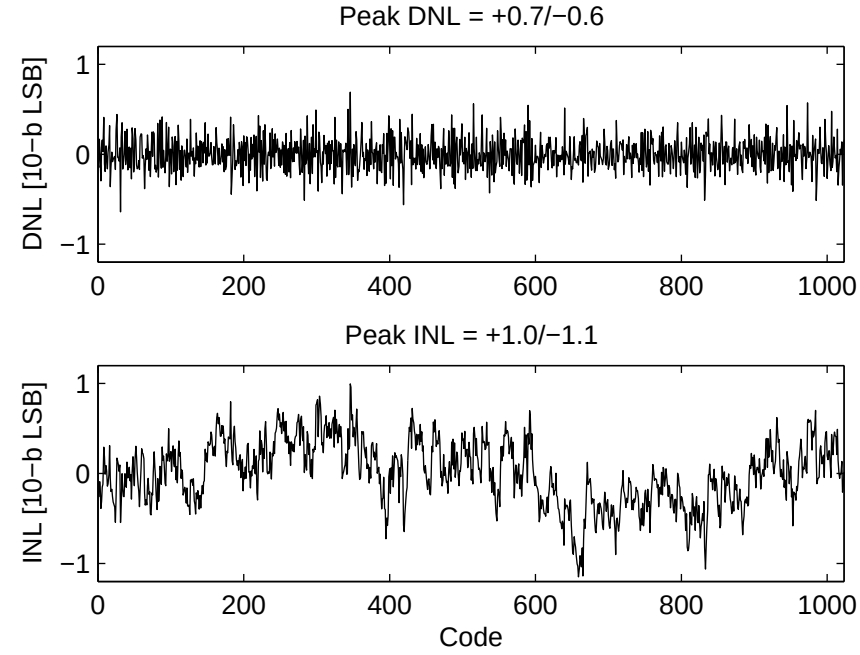
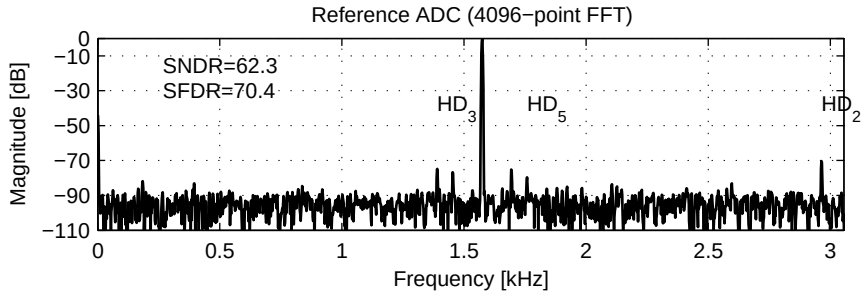
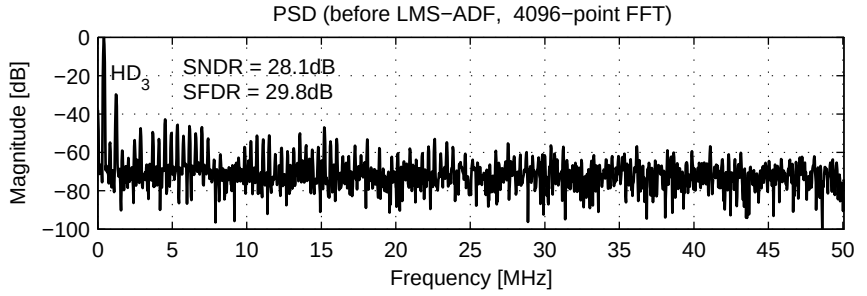


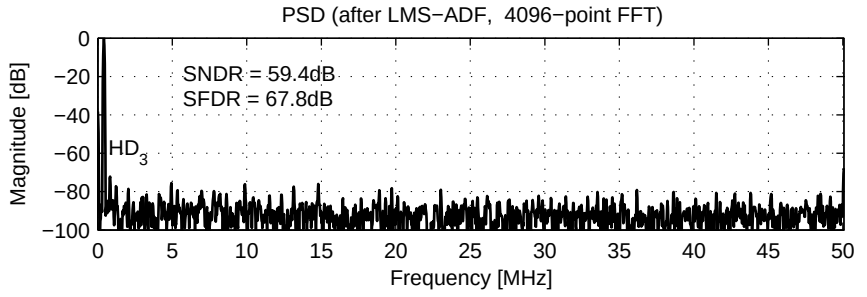
Figure 11.11: Measured DNL and INL after calibration.



(a)

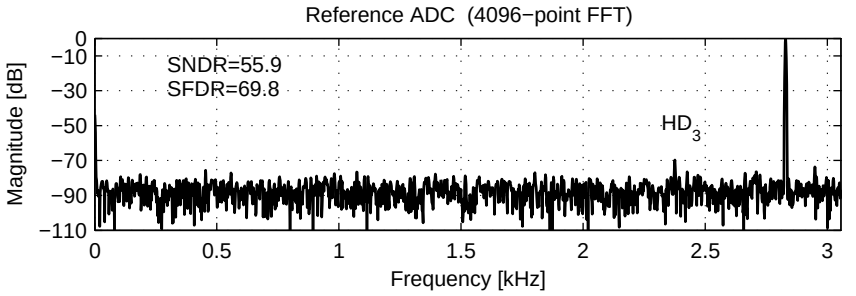


(b)

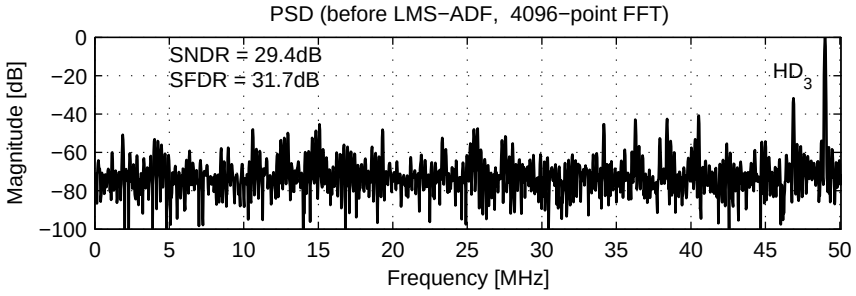


(c)

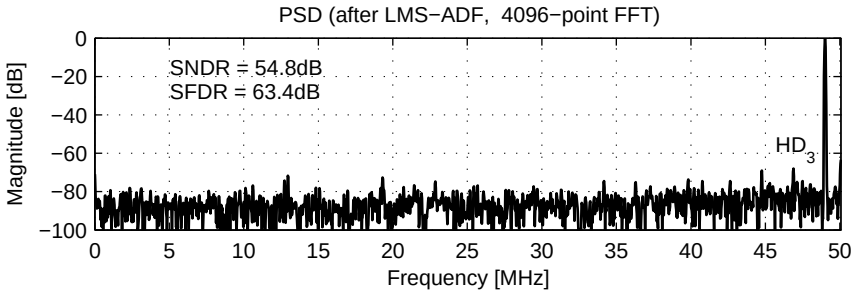
Figure 11.12: Measured ADC spectra for f_s=100MHz, V_{in}=0dBFS, f_{in}=411kHz: (a) Reference ADC, (b) before calibration, (c) after calibration.



(a)

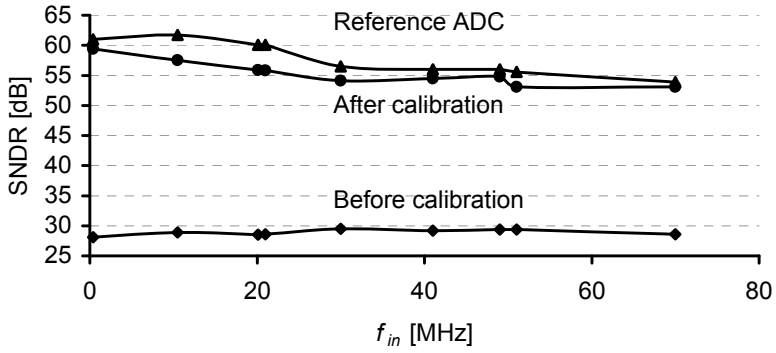


(b)

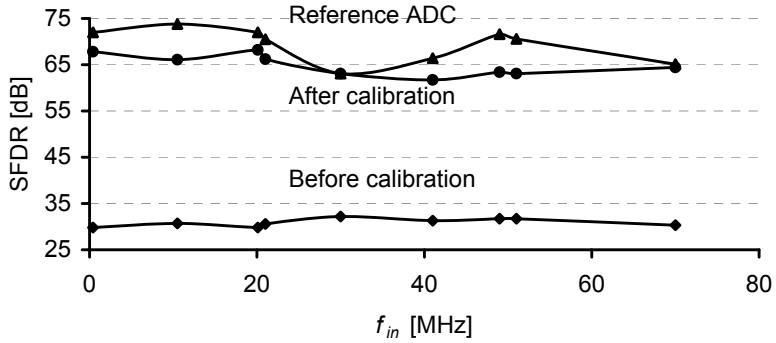


(c)

Figure 11.13: Measured ADC spectra for f_s=100MHz, V_{in}=0dBFS, f_{in}=49MHz: (a) reference ADC, (b) before calibration, (c) after calibration.



(a)



(b)

Figure 11.14: Measured performance at 100MS/s: (a) SNDR, (b) SFDR.

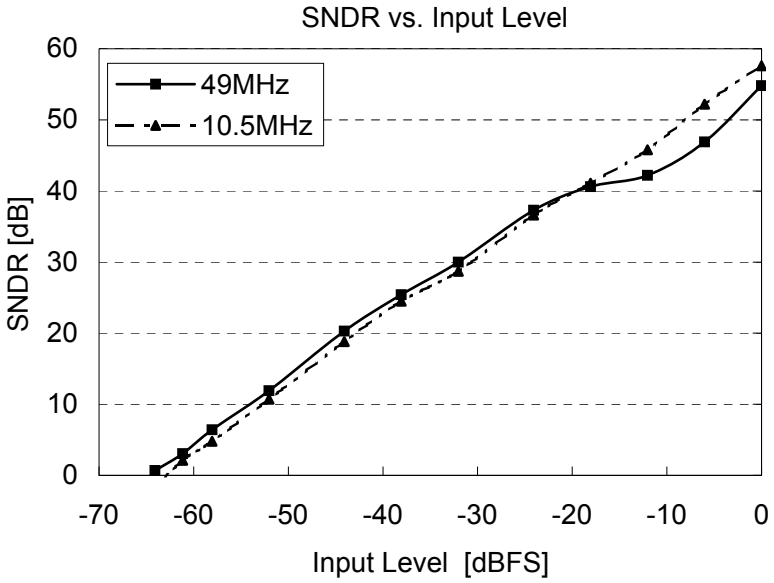


Figure 11.15: Measured SNDR after calibration versus input level at 100MS/s.

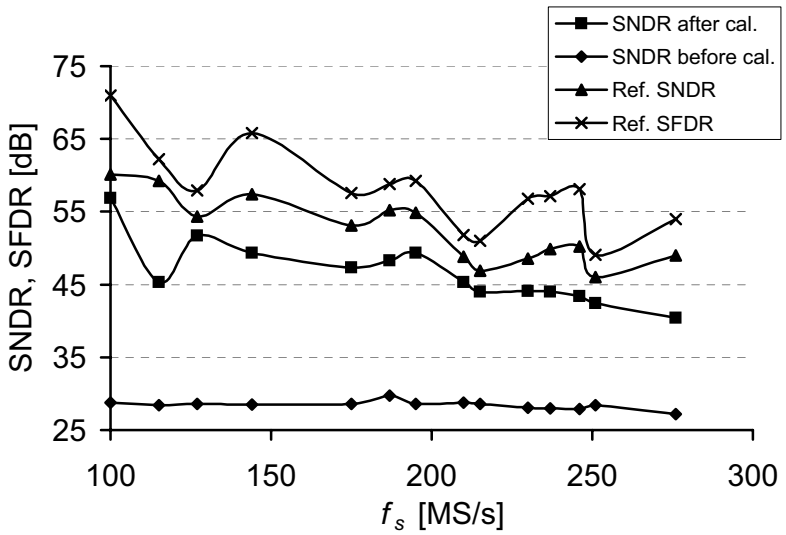


Figure 11.16: Measured SNDR versus f_s with 10MHz input.

SNDR and SFDR are relatively flat across frequencies. The SNDR after calibration drops gradually as f_{in} increases from DC to 70MHz. The SFDR after calibration is above 60dB in the same input frequency range. Figure 11.15 plots the SNDR vs. the input level with a 10.5MHz and a 49MHz input signals.

Measured Performance vs. f_s

Figure 11.16 plots the measured SNDR vs. the sampling frequency with a 10MHz input. The best performance is achieved at 100MS/s and then the performance drops gradually with increasing f_s. The degradation of performance vs. f_s tracks closely with the quality of the reference signal as shown in Figure 11.16. This experiment demonstrates that proposed LMS ADF is capable of correcting pipelined ADC residue amplifier errors with an accurate reference signal. The degradation in SNDR and SFDR of the reference ADC is believed to be lied in the dedicated front-end SHA.

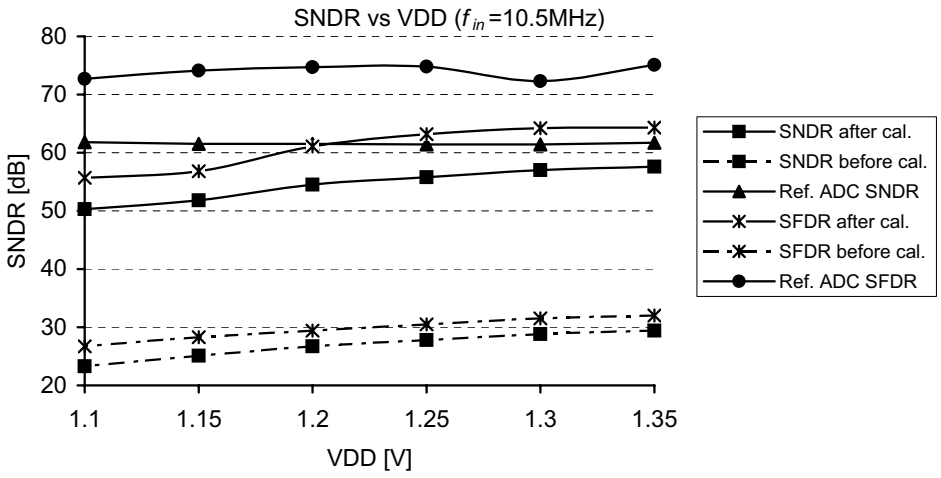


Figure 11.17: Measured SNDR after calibration vs. VDD for f_s=100MS/s, f_{in}=10.5MHz.

Measured Performance vs. *VDD*

To compare the performance at different supply voltages, Figure 11.17 shows the SNDR at 100MS/s with a 10.5MHz input at analog supply voltage from 1.1V to 1.35V. The reference ADC performance is insensitive to different supply voltages, but the SNDR and SFDR of the pipelined ADC before calibration reduces as the supply voltage is lowered. This is likely resulting from a design problem in OTAs in the residue amplifier. The problem is that the P-side cascode transistors of the OTAs are not biased correctly and are in linear region with a large differential output swing.

Nonlinear vs. Linear Calibration

Figure 11.18 compares the performance of the ADC with linear and nonlinear calibration. Only linear OTA gain error is corrected in the linear case whereas nonlinear OTA gain error in the first two stages is corrected in the nonlinear case. With a full-scale input voltage, f_s = 100MS/s, f_{in} = 10.5MHz, the SNDR improves from 53.9dB to 57.6dB

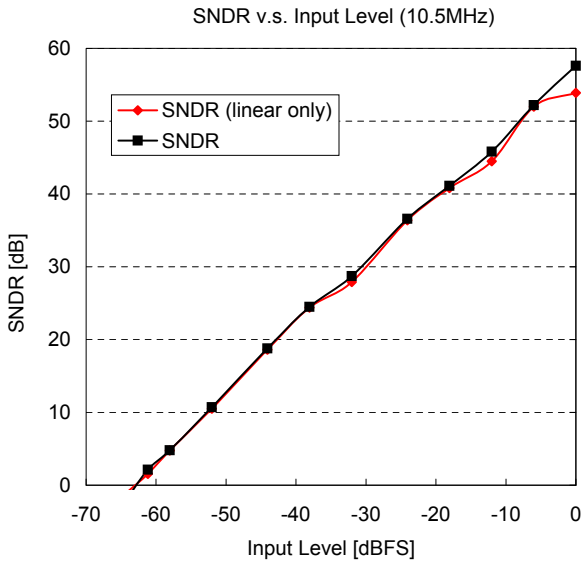


Figure 11.18: Measured SNDR with linear and nonlinear calibration vs. input level for f_s=100MS/s, f_{in}=10.5MHz.

from linear calibration to nonlinear calibration.

11.3.4 Performance Summary

Table 11.2 summarizes the measured performance of the prototype. The total power consumption consumption is 448mW at 100MS/s. The same analog supply is used to power the SHA and the pipelined ADC so their total power is reported together. The $\Sigma\Delta$ ADC only consumes 2.2% of the total power. The clock generation circuit is over-designed to operate above 400MHz, and power can be reduced if it is optimized for a smaller operating frequency range.

Table 11.2: Experimental Results.

	Before cal.	After cal.
Process	0.13μm digital CMOS	
Supplies: Analog/Digital	1.35V/1.2V	
Full-scale Input(pk-pk)	$\pm$0.5V	
Sampling Rate (f_s)	100MHz	
Chip Area	3.7mm$\times$4.7mm	
$\Sigma\Delta$ Power	10mW	
SHA + Pip. ADC Power	332mW	
Clock Gen. Power (DLLs+Buffer)	106mW	
Total Power	448mW	
SNDR(411kHz)	28.1dB	59.4dB
SNDR(49MHz)	29.4dB	54.8dB
SFDR(411kHz)	29.8dB	67.8dB
SFDR(49MHz)	31.7dB	63.4dB
HD_3(411kHz)	-29.8dB	-72.2dB
HD_3(49MHz)	-31.7dB	-68.0dB

Chapter 12

Conclusion

12.1 Conclusion

This dissertation has explored the possibility of using abundant digital gates available in deep sub-micron CMOS process to compensate errors in analog circuits, specifically, analog-to-digital converters. By employing the proposed digital calibration, the precise closed-loop gain requirement of MDACs in pipelined stages is greatly relaxed. Thus, simple low open-loop gain amplifiers are used. Amplifiers are faster and power efficient with relaxed gain so that the overall ADC conversion rate and the power efficient are improved. In addition to correcting the op-amp gain error, capacitors mismatch and switch charge injection are also corrected by the proposed method.

The calibration is transparent to users and is completely background and digital. The algorithm is capable of correcting errors from all stages at the same time; i.e. it does not require calibrating from LSB stages to MSB stages sequentially. Furthermore, nonlinear amplifier gain is also corrected by the proposed method. To demonstrate the

algorithm, a prototype in 0.13μm digital CMOS process was built and measured. Using op-amp only capable of producing 5-bit raw resolution in a pipelined ADC, the ADC achieved 10-bit resolution after calibration. In this project, we have demonstrated that the proposed method is effective to correct errors in MDAC. We can achieve high speed and high resolution simultaneously with the help of digital circuits. This technique will enable us to build high-speed, high resolution, and power efficient ADC in purely digital CMOS as CMOS technology continues to scale in the coming decade.

12.2 Key Accomplishments

- Demonstrated feasibility of using low-gain op-amp of high-resolution pipelined ADC. Only a single-stage op-amp with minimum channel devices is required in the residue amplification. In addition, we can continue to build low-speed reference ADCs in scaled CMOS. This architecture is going to benefit from scaling of CMOS technology.
- Demonstrated correction of nonlinear op-amp gain error.
- Designed a low-voltage low-power highly linear $\Sigma\Delta$ ADC
- Completed and assembled analog building blocks in the prototype
- Designed digital filters and implemented them in a FPGA
- Showed that the power penalty from the additional analog and digital circuits used for calibration is a small portion of the total power.

12.3 Suggestions for Future Work

We present some suggestions to improve the current technique and to further extend the technique to new areas:

- In the prototype, we have used two separate sampling networks for the SHA of the $\Sigma\Delta$ ADC and the sampling network pipeline stage 1. It is extremely difficult to exactly match the two paths. The mismatch of the two networks degrades the effectiveness of the digital calibration, especially with high frequency input. A method to merge the sampling networks can alleviate this mismatch problem.

- The similar algorithm can be extended to correct analog errors in other high-speed ADCs. For example, the idea can be used to remove nonlinear error from folders in folding ADCs. In addition, capacitor mismatch in high-speed SAR ADC can also be corrected.

- In the current algorithm, only static errors are calibrated. It will be interesting to further research to correct dynamic, frequency dependent errors.

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Appendix A

Prototype Chips Pin-out

A.1 Pin-out of the stand-alone 2-1 MASH ΣΔ ADC

The pin-out of the stand-alone ADC testing is shown in Table A.1. Pin 1 is located at the top left corner of the chip.

Table A.1: Pin-out of the stand-alone 2-1 MASH ΣΔ ADC.

Pin	Name	Remark	Pin	Name	Remark
1	VSSA	analog gnd	23	VSSIO4	
2	VSSA		24	VDDIO4	
3	VSSA		25	B2	stage 2 output bit
4			26	VSSAOUT	
5	VIN	Input	27	CLKOUT	output clock
6	VIP	Input	28	B1	stage 1 output bit
7	VSSA		29	VDDIO5	
8	VSSA		30	VSSIO5	
9	VSSIO1	gnd for IO ring 1	31	VDDD	
10	VDDIO1	supply for IO ring	32	VSSD	
11	ITEST	current mirror test pin	33		
12	IREF1	current reference for OTA1	34	VDDIO6	
13	VDDA	analog supply	35	VSSA5	
14	VSSA	analog gnd	36	VSSIO6	
15	VDDA	analog supply	37	VDDIO	
16	VSSA	analog gnd	38	VREFMID	
17	IREF2	current reference for OTA2	39	VREFP	
18	VDDA	analog supply	40	VREFN	
19	VSSA	analog gnd	41	VREFCM	
20	IREF3		42	VSSIO	
21	VDDIO3		43	VDDIO	
22	VSSIO3		44	CLK	input clock

A.2 Pin-out of the background calibrated ADC

The pin-out of the background calibrated ADC test chip is shown in Table A.2. Pin 1 is located at the top left corner of the chip.

Table A.2: Pin-out of the background calibrated ADC.

Pin	Name	Remark	Pin	Name	Remark
1	DLL1A		68	B20n	
2	DLL1B		69	B20p	
3	DLL_vduty_cycle	clk duty cycle	70	B11n	
4	SH_spd_ctrl		71	B11p	
5	DLLIMSBref2	I bias	72	B10p	
6	DLLILSBOut	I bias	73	B10n	
7	DLLOutLSBs	Control	74	VSS_LVDS	
8	DLL_Off_Buffer		75	VDD_LVDS	
9	DLLIbiasref	I bias	76	B72p	
10	DLL_reset		77	B72n	
11	DLL_VDD2	digital supply	78	B71p	
12	DLL_VSS2		79	B71n	
13	VDDIO2v5_1		80	Pipe_VSSD	
14	VSSIO_1		81	Pipe_VDDD	
15	VSSSUB_DLL	substrate bias	82	B70p	
16	DLLOutp	DLL output	83	B70n	
17	DLLOutn	DLL output	84	B62p	
18	SD_VSS_clk		85	B62n	
19	SD_VDD_clk		86	VDDIO2v5_3	
20	SD_VDD_comp		87	VSSIO_3	
21	SD_VSS_comp		88	B61p	
22	SD_Vrefn		89	B61n	
23	SD_Vrefp		90	B60p	
24	SD_Vicm		91	B60n	
25	SD_Vmid		92	B52p	
26	SD_VSSA		93	B52n	
27	SD_VDDA	analog supply	94	B51p	
28	SD_vdd1	N-well bias	95	B51n	
29	SD_VSSA		96	VSSSUB_LVDS	
30	SD_VDDA		97	VSS_LVDS	
31	SD_bias1	OTA1 I bias	98	VDD_LVDS	
32	SD_bias2	OTA2 I bias	99	B50n	
33	SD_bias3	OTA3 I bias	100	B50p	
34	VSSSUB_Pipe	substrate bias	101	B42n	
35	VDDIO2v5_2		102	B42p	
36	VSSIO_2		103	B41n	
37	Pipe_VSSA		104	B41p	
38	Pipe_VDDA	analog supply	105	B40n	

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Pin	Name	Remark	Pin	Name	Remark
39	SHA_Ibias	I bias	106	B40p	
40	Pipe_Ibias1	I bias	107	VDDIO2v5_3	
41	Pipe_Ibias2	I bias	108	VSSIO_3	
42	Pipe_VSSA		109	SHA_clkoutp	
43	Pipe_VDDA		110	SHA_clkoutn	
44	Vinp	signal input	111	Pipe_clkoutp	
45	Vinn	signal input	112	Pipe_clkoutn	
46	VDDIO2v5_3		113	VDD_LVDS	
47	VSSIO_3		114	VSS_LVDS	
48	SD_clkoutp		115	Pipe_VrefpR	ref for SUBADC
49	SD_clkoutn		116	Pipe_VrefnR	ref for SUBADC
50	SD1p		117	Pipe_Vrefp	
51	SD1n		118	Pipe_Vrefn	
52	SD2p		119	Pipe_VDDA	
53	SD2n		120	Pipe_VDDA	
54	VSS_LVDS		121	Pipe_Vcm	
55	VDD_LVDS		122	Pipe_Ibias3	
56	B32p	pipe stage 3 bit 2	123	VDD_Nwellbypass	N-well bias
57	B32n	pipe stage 3 bit 2	124	Pipe_VSSA	
58	B31p		125	Clk_inp	input clock
59	B31n		126	Clk_inn	input clock
60	B30p		127	VDDIO2v5_4	
61	B30n		128	VSSIO_4	
62	B22p		129	VSSSUB_pipe	
63	B22n		130	DLL_VDDA	input clock
64	VDDIO2v5_3		131	DLL_VSSA	
65	VSSIO_3		132	DLL_IMSBref1	
66	B21n		133	DLL_ILSBref	
67	B21p		134		