0.35 µm CMOS PROCESS ON SIX-INCH WAFERS, Baseline Report VII.

Laszlo Petho

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2009-163
http://www.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-163.html

December 7, 2009

0.35 µm CMOS PROCESS ON SIX-INCH WAFERS

Baseline Report VII.

L. Petho

College of Engineering / ERSO
University of California at Berkeley

December, 2009

Abstract: This report details the fifth six-inch baseline run, CMOS192, fabricated in the UC Berkeley Microlab. A moderately complex 0.35 µm twin-well process, developed and fine-tuned in earlier runs, was used. Different research circuits were placed in the drop-in area: ring oscillators, different memory circuits, a MEMS design, features for carbon nanotube integration and nanowire-based molecular sensors.

Table of contents

List of figures

List of tables

1. Introduction

The CMOS baseline test chip fabrication in the Microfabrication Laboratory at the University of California, Berkeley has provided an excellent tool for continuous monitoring of process modules and equipment.

CMOS baseline runs were processed regularly on 4 inch wafers since 1992 in the Microlab. In 2001 the baseline process was transferred onto six-inch wafers [1]. This was followed by a new and more advanced 0.35 μm process, which produced the first sub-half micron devices [2]. Device parameters were successfully improved and a triple metal process was implemented in successive runs [3]. The latest run focused on a Mix&Match process among the 6" lithography tools and ensured threshold voltage targeting [4].

This is the seventh baseline report submitted. The baseline run, CMOS192, described in this report, will serve as a starting point to compare process functionality as developed in the Microlab, to the start up run in the new facility, the Marvell Nanofabrication Laboratory.

2. CMOS Baseline Fabrication Process

The CMOS192 process flow consists of 66 steps including the triple metal module. The current 0.35 μm process contains N-channel and P-channel MOSFET devices, as well as some simple circuits. First electrical testing was performed at step 52, post Metal1 etch and sintering, yielding well with functional devices.

The starting material for the process were 6" P-type double polished wafers with the following parameters: <100> orientation, 20-60 Ωcm resistivity, 635±25 μm thickness and a total thickness variation <7 μm.

This process utilizes thin gate oxide, lightly doped drain structure, PECVD oxide sidewall spacers, titanium silicide S/D, and poly work function engineering. A 250 nm thick layer of undoped polysilicon was deposited, then patterned and etched to form the gate electrode structures. These poly gates were then selectively implanted to have their work function adjusted and matched for desired V_t values, based on earlier simulation results. This was achieved by exposing the N- and P-channel gate electrodes selectively during their respective source/drain implant steps. CMP and PECVD TEOS intermetal dielectric was used for the triple metal version of the 0.35 μm process.

Step	**Resist**	**Mask**	**Hard bake**
Zero layer photo	MF26A DUV	Zero layer mask PM marks	UVBake, program U
N-well photo	MF26A DUV	NWELL mask (Dark field)	UVBake, program J
P-well photo	MF26A DUV	PWELL mask (Clear field)	UVBake, program J
Active area photo	MF26A DUV	ACTIVE mask (Clear field)	UVBake, program J
P-well field implant photo	MF26A DUV	PFIELD mask (Clear field)	UVBake, program J
NMOS Vt adj. implant photo	MF26A DUV	PWELL mask (Clear field)	UVBake, program J
PMOS Vt adj. implant photo	MF26A DUV	NWELL mask (Dark field)	UVBake, program J
Poly gate photo	BARC + MF26A DUV	POLY mask (Clear field)	UVBake, program U
P-type LDD implant photo	MF26A DUV	PSELECT mask (Dark filed)	UVBake, program J
N-type LDD implant photo	MF26A DUV	NSELECT mask (Dark field)	UVBake, program J
P+ Gate & S/D photo	MF26A DUV	PSELECT mask (Dark filed)	UVBake, program J
N+ Gate & S/D photo	MF26A DUV	NSELECT mask (Dark field)	UVBake, program J
Contact photo	MF26A DUV	CONTACT mask (Dark field)	UVBake, program U
New PM marks	MF26A DUV	Zero layer mask PM marks	UVBake, Program U
Metal1 photo	BARC + MF26A DUV	METAL1 mask (Clear field)	UVBake, program U
Via1 photo	MF26A DUV	VIA1 mask (Dark field)	UVBAKE program U
Opening 4 dies for PM marks	MF26A DUV	Blank mask	UVBake, Program U
Metal2 photo	BARC + MF26A DUV	METAL2 mask (Clear field)	UVBake, program U
Via2 photo	MF26A DUV	VIA2 mask (Dark field)	UVBake, program U
Opening 4 dies for PM marks	MF26A DUV	Blank mask	UVBake, Program U
Metal3 photo	BARC + MF26A DUV	METAL3 mask (Clear field)	UVBake, program U

Table 1. Lithography steps and related information

Lithography: The CMOS192 process included 19 lithography steps. Some of the masks were used on two layers, which brought the total number of masks down to 13, including the zero layer mask. Table 1. lists all the lithography steps used for the fabrication of CMOS192, as well as the corresponding mask ID and the photoresist hard bake methods. All steps were done on the DUV 248 nm ASML stepper. As indicated, a BARC layer (Bottom Anti-Reflective Coating; Shipley ARC-600) was applied at some of the lithography steps.

The photoresist used for baseline processing is Rohm Haas UV210-0.6. Before the current run has started, the developer LDD-26W was replaced to MF-26A on the SVGDev6 track due to safety regulations. When BARC was applied, the HMDS coating step was skipped.

Appendix B shows the ASML mask plate layouts with four quadrants each; used during processing of the current baseline run.

Implantation: The baseline process required 9 ion implantations, all of which were performed at Core Systems (Sunnyvale, CA). The list of the implantation steps, including implant parameters and blocking materials are shown in Table 2. All of the implant steps were done at a standard 7^{o} tilt to prevent channeling. Different inline test wafers were used to monitor S/D and poly gate doping (wafers labeled as PCH, NCH, Tpoly1 and Tpoly2).

Step	**Species**	**Dose (cm^{-2})**	**Energy (KeV)**	**Masking materials**
N-well implant	Phosphorus	1E13	150	220 nm Si_3N_4 + PR (UVBake)
P-well implant	Boron	5E12	60	220 nm Si_3N_4 + PR (UVBake)
P-well field implant	Boron	2E13	80	25 nm pad oxide + PR (UVBake)
NMOS Vt implant	BF2	3E12	50	25 nm pad oxide + PR (UVBake)
PMOS Vt implant	Phosphorus	2E12	30	25 nm pad oxide + PR (UVBake)
P-type LDD implant	BF2 BF2	5E13 5E13	10, 0º 10, 180º	PR (UVBake)
N-type LDD implant	Arsenic Arsenic	5E13 5E13	30, 0º 30, 180º	PR (UVBake)
P+ Gate & S/D implant	Boron	3E15	20	PR (UVBake)
N+ Gate & S/D implant	Phosphorus	3E15	40	PR (UVBake)

Table 2. List of implantation steps and parameters

Tool set: The list of equipment used for the fabrication of the CMOS192 run is listed in Table 3. Detailed tool information is available at http://microlab.berkeley.edu/text/labmanual.html

Process module	Equipment	Process step
Lithography	ASML 5500/90 DUV stepper	Listed in Table 1.
	SVGCoat6	PR/BARC spinning
	SVGDev6	PR develop
	Matrix	PR removal
	Technics-C	PR removal, descum
	UVBake	Hardbake
Plasma etch	AMAT Centura-MxP+	Nitride etch
		Oxide/spacer etch
	AMAT Centura metal	Aluminum etch
	Lam 3	Aluminum etch
	Lam 5	Poly-Si etch
High temperature treatment	Tystar 1	Gate oxidation
	Tystar 2	Wet/dry oxidation
	Tystar18	Sintering
	Heatpulse 3	Annealing
	Heatpulse 4	Silicidation
CVD	AMAT P-5000 (PECVD)	Spacer/intermetal TEOS deposition
	Tystar 9 (LPCVD)	Nitride deposition
	Tystar 10 (LPCVD)	Poly-Si deposition
	Tystar 11 (LPCVD)	PSG deposition
Thin film systems	Novellus	Ti deposition
		Al deposition
Wet etch and cleaning	Sink 6	Pre-furnace piranha clean
		HF dip (10:1, 25:1)
		Rinse, spin dry
	Sink 7	Hot phosphoric etch
		Ti wet etch
	Sink 8	Post-lithography piranha clean
		Buffered HF etch (5:1)
		Rinse, spin dry
	Sinkcmp	Post-CMP clean
Metrology and testing	ASIQ	Surface profiling
	Nanospec	Thin film thickness
	Leo	SEM
	4pt probe	Sheet resistance
	Autoprobe	Electrical parameters
	SCA	Gate oxide quality
	Sopra	Ellipsometer
Planarization	CMP	Mechanical polishing

Table 3. Process tool set

3. Baseline chip layout

The CMOS192 chip layout, shown in Fig. 1., includes the standard groups of baseline transistor sets; test structures (contact resistors, contact chains, contact holes), basic test circuits (NOR and NAND gates), ring oscillators, a MEMS structure, features for carbon nanotube integration and nanowire-based molecular sensors.

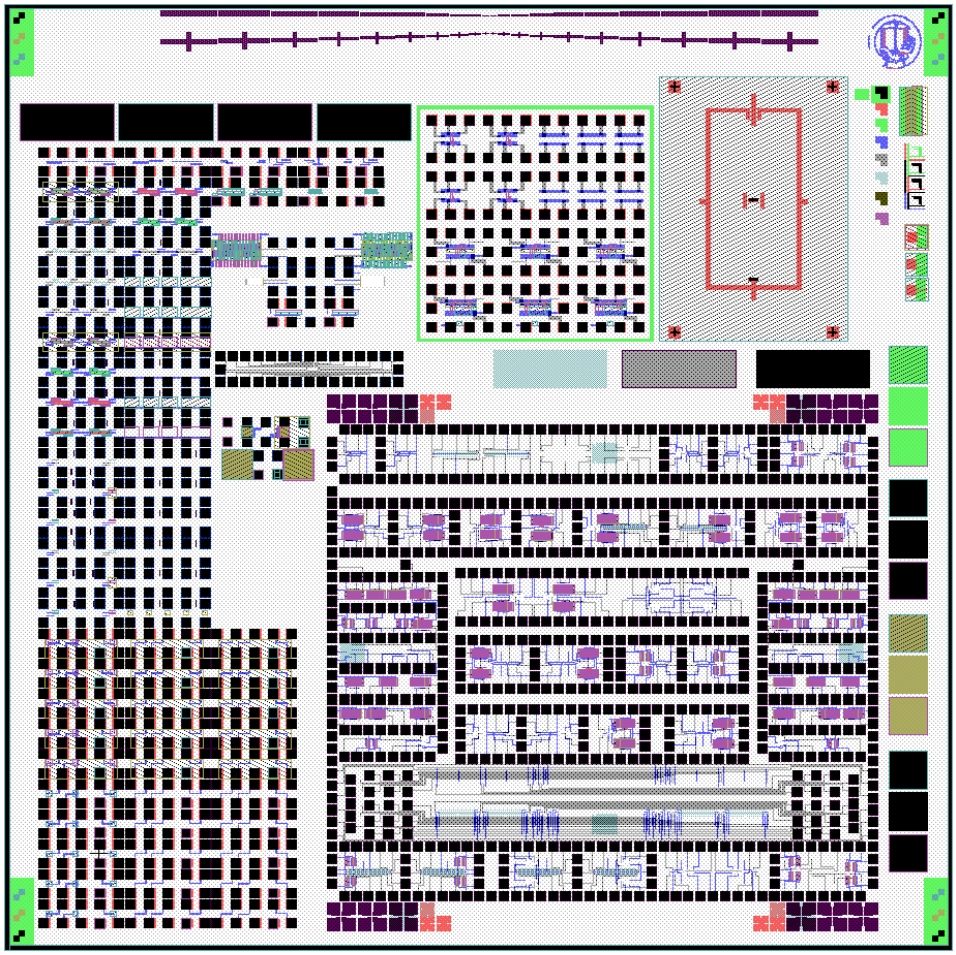


Fig. 1. Layout of the CMOS192 Baseline chip

- The **single transistor section** of the die consists of three groups differentiated by their design rules. Each column is based on a 5x3 array of PMOS and NMOS transistors, which are varying in channel length (L = 0.3, 0.35, 0.4, 0.5, and 1 µm) and channel width (W = 2.5, 5, and 7.5 µm).

  The first column on the left side used a more robust design rule basically following the old transistor layout; which had been tested and proven by the CMOS160 run. This design was scaled down by 2 in CMOS170 and remained as is in successive runs. These transistors do not follow any specific industrial layout design rules; gates are reduced while their contacts, active areas and metal lines are kept within safe processing limits.

On the second and third groups a more aggressive lambda scale design approach was applied. The column 2 transistors in the middle received Hewlett Packard's λ=0.5 μm design rules, while transistors on the third column followed HP design rules for λ=0.35 μm.

- The main purpose of the **CNT design structure** is to investigate the process compatibility of carbon nanotubes and CMOS circuitry [5]. Nanotubes will be locally synthesized after the CMOS process is done. The poly layer in the CMOS process is used as the necessary CNT growth structure in the post-processing CNT growth. There are four different design units:

  Design 1&2 are one-stage and two-stage CMOS amplifiers, respectively. They are essentially the same as in CMOS180 while some minor layout corrections were made.

  Design 3 is a new amplifier structure: this system features full CMOS realization including an active resistor (saturated CMOS transistors). Theoretically no external device would be needed to make it work.

  Design 4 is a self-stop circuitry; this design will be used during the CNT synthesis. It includes a simple feedback circuitry which can automatically stop the heating resistor after the CNT is formed.

- The second drop-in area of the baseline chip consists of a platform for testing **nanowire-based molecular sensors** [6]. It is composed of 20 μm and 200 μm, gated and non-gated Wheatstone bridges connected to pads and/or CMOS circuits. These bridges will be used to sense molecules or gases depending on how the nanowires are functionalized and the contact metals used. They have an extra ground terminal that can be used for manual offset cancellation.

  The CMOS circuits are included with bridges to provide amplification and impedance conversion for easier readout of the generated signals. Currently there are 4 types of circuits: a 667/1 μm PMOS source follower, a simpler 42/1 μm PMOS source follower, a 70/0.5 μm PMOS differential pair; a 6.25/1 μm NMOS and PMOS source follower combination for higher bandwidth.

  The lower portion of the chip also includes a series of bridges with a distance of about 2.5 mm from their connecting pads; this portion will be used for integration with a microfluidic channel. In some versions of the chip, a very fine dummy fill is used for all metal layers to study the effect on chemical-mechanical polishing performance and subsequent nanowire printing.

- The **MEMS structure** included in the CMOS192 layout is an electrostatic mono-directional in-plane displacement microactuator (EMDIPDM) [7]. This particular device enables the evaluation of the fracture strength of a given thin film material. Previous devices fabricated can measure Young's modulus, and material fatigue properties, as shown in Fig. 2. A variety of different thin film materials can be tested; the only primary requirement being that the material is electrically conductive. Silicon carbide, silicon

germanium, and poly-silicon are examples of materials that may be evaluated with the EMDIPDM device.

The fabrication steps of the EMDIPDM MEMS structure are performed in parallel with the CMOS Baseline process. A predetermined "split" occurs from the batch of CMOS wafers being processed, and a MEMS-only process flow ensues on selected wafers. The MEMS process steps consist of a simple test-material deposition, pattern, etch, and release to produce the final device.

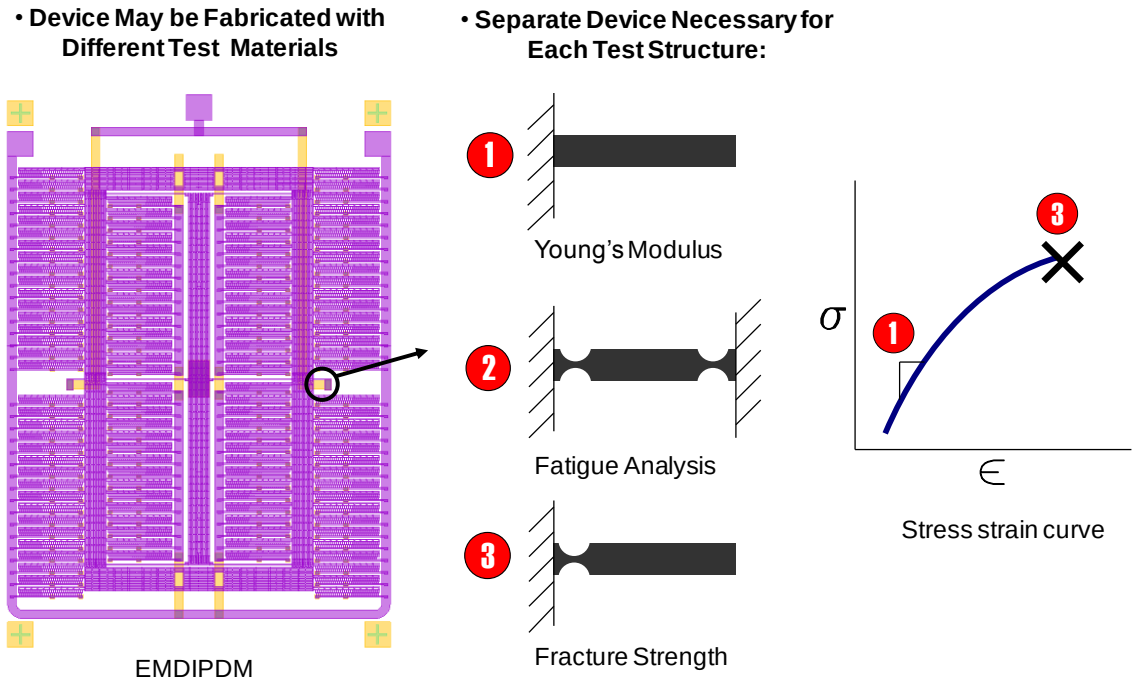


Fig. 2. The electrostatic monodirectional in-plane displacement actuator (a) and evaluation of: (1) Young's modulus from the elastic bending of a beam, (2) fatigue, and (3) fracture strength.

Each type of measurement requires fabrication of a separate device. The latest EMDIPDM device was designed to measure fracture strength. Previous devices fabricated with the CMOS180 baseline measure Young's modulus and fatigue.

4. Processing and device parameters of CMOS192

The process flow of the current baseline run is detailed in Appendix A. The flow includes equipment and recipe information, process parameters and target specification for each step.

The following paragraphs detail device parameters and measurement results gathered after finishing Metal1/Metal2 layers or from inline monitor wafers.

4.1. Electrical measurements

I–V results: Graphs show typical I–V characteristics of the CMOS192 transistors measured on 0.3 µm drawn channel length and 2.5 µm width transistors. Fig. 3. and Fig. 4. demonstrate I_d–V_g; Fig. 5. shows I_d–V_d curves. V_t targeting for 2.5/0.3 µm devices is shown on Fig. 6.

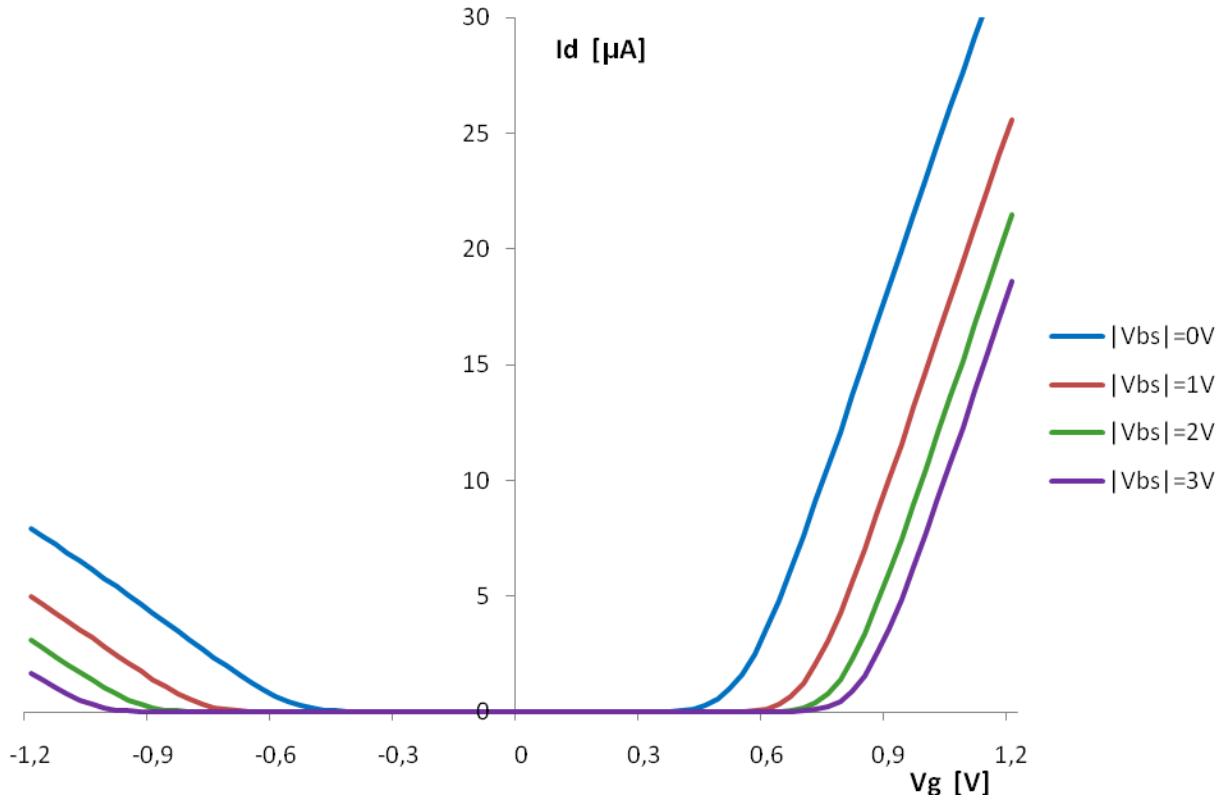


Fig. 3. Drain current vs. gate voltage at varying substrate bias on PMOS and NMOS transistors in the linear region ($|V_d|$=50 mV, L=0.3 µm, W=2.5 µm)

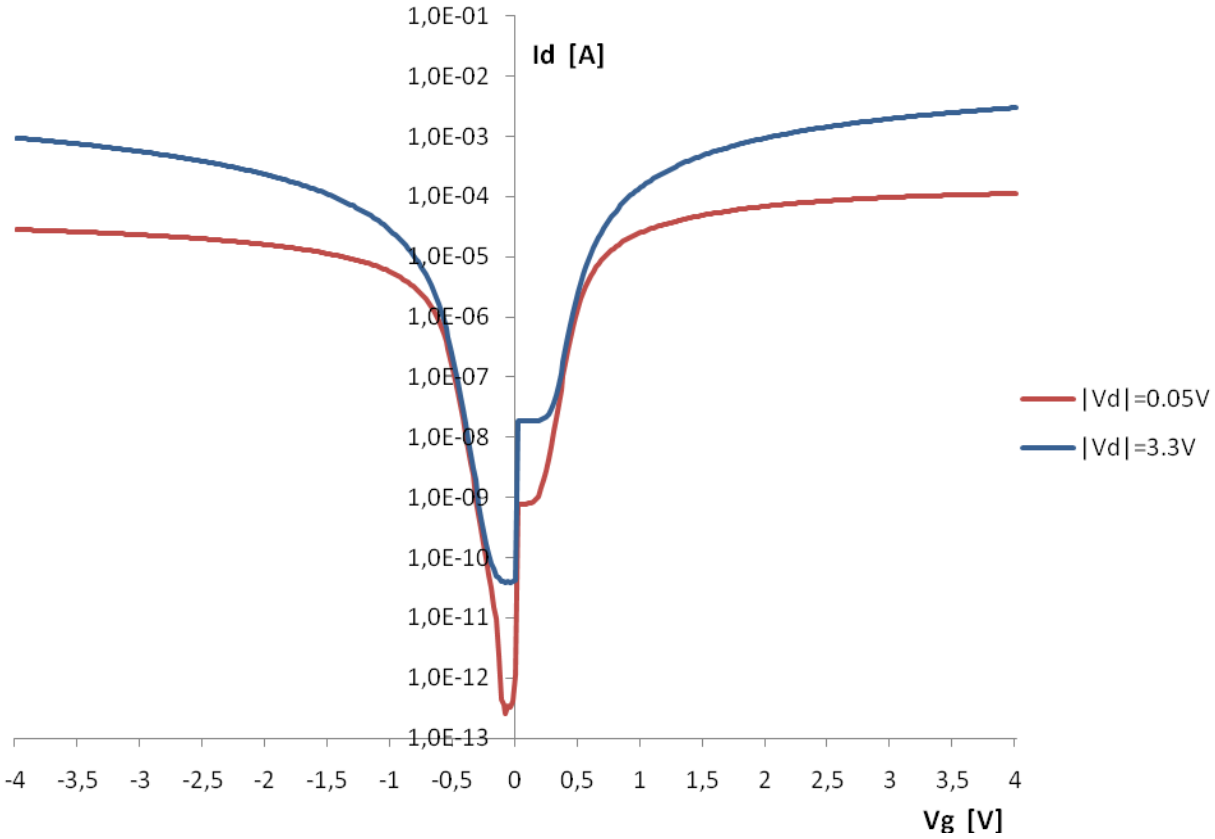


Fig. 4. PMOS and NMOS sub-threshold characteristics

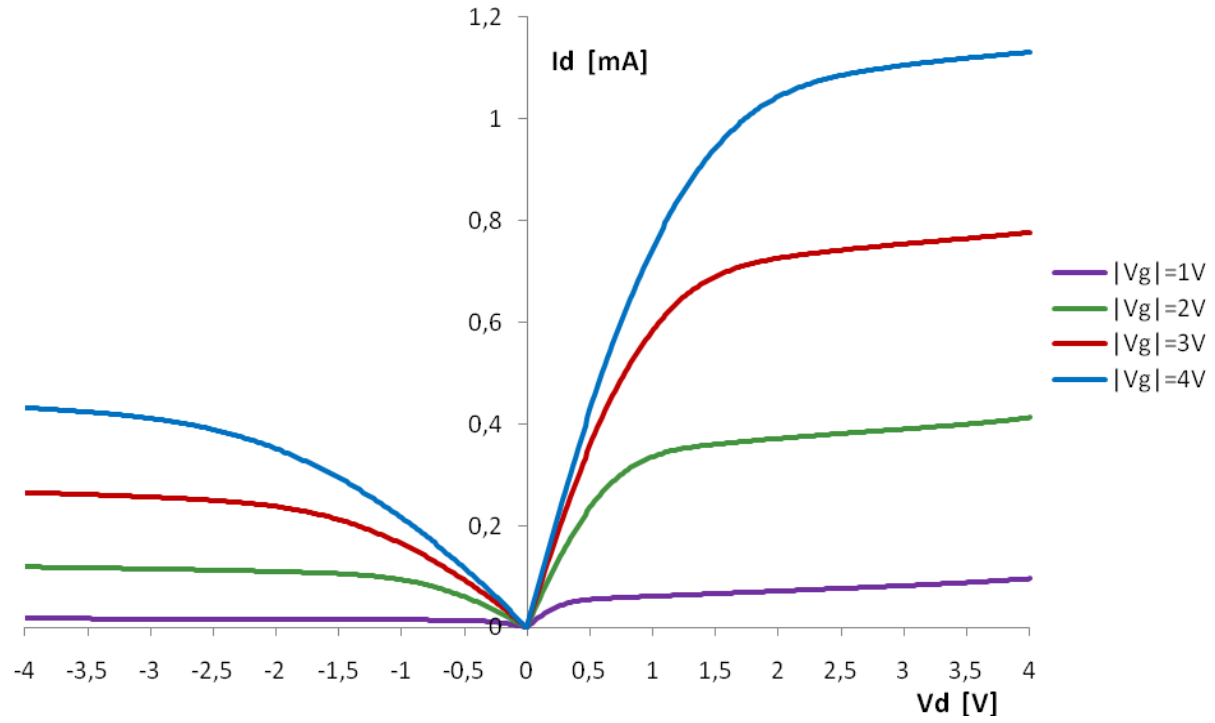


Fig. 5. Drain current vs. drain voltage characteristics of PMOS and NMOS devices

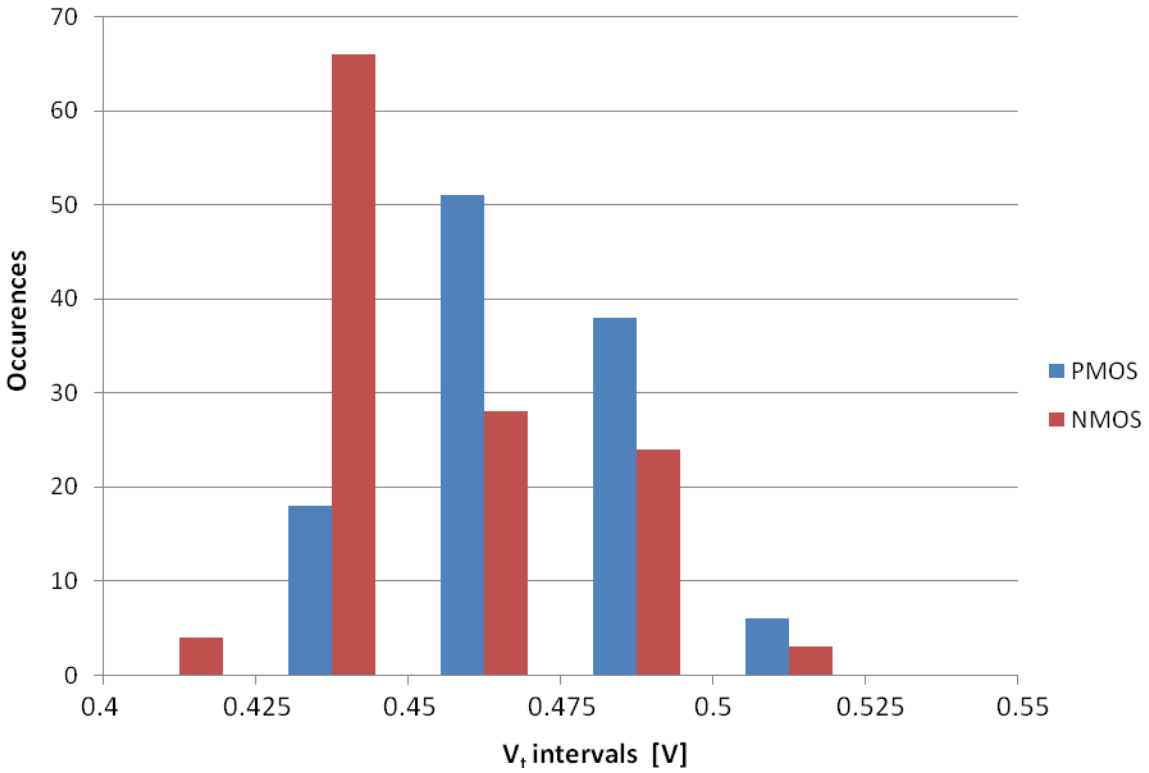


Fig. 6. Threshold voltage targeting for 2.5/0.3 µm devices

Ring oscillators: Following the completion of the second metal layer, ring oscillators were tested. Various types and gate length ring oscillators are available on the test chip; 0.35 µm, 0.5 µm, 1 µm and 2 µm gate length conventional; as well as 1.2 µm gate length voltage controlled ring oscillators (VCO). Each device consists of 31 stages. Average oscillation frequencies and calculated gate delays are shown in Table 4.
Fig. 7. shows a screenshot of an oscilloscope connected to a 1 µm gate length conventional ring oscillator. Oscillation period times and frequencies were measured at different driving voltage values on a 1.2 µm gate length VCO; plotted on Fig. 8.

Type	Conventional				VCO
Gate length (µm)	2	1	0.5	0.35	1.2
Contact size (µm)	2	2	1	0.7	1.2
Frequency (MHz)	**58.5**	**70.8**	**195.6**	**309.1**	**15.3**
Gate delay (ns)	0.28	0.23	0.08	0.05	1.05

Table 4. Ring oscillator frequencies and gate delays

Fig. 7. Snapshot of the oscilloscope screen showing the signal generated by a 1 µm gate ring oscillator

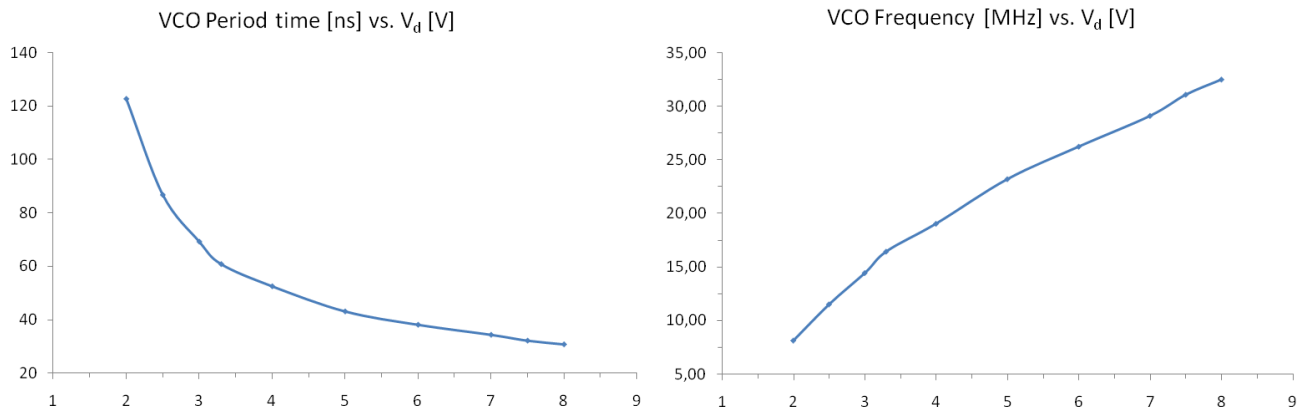


Fig. 8. VCO period times and frequencies versus drive voltage

4.2. Spreading Resistance Analysis (SRA)

The spreading resistance analysis was carried out by Solecon Laboratories Inc. (Reno, NV). Graphical presentation of the measurement results, carrier concentration vs. implant depth profiles are shown on Fig. 9. and 10.

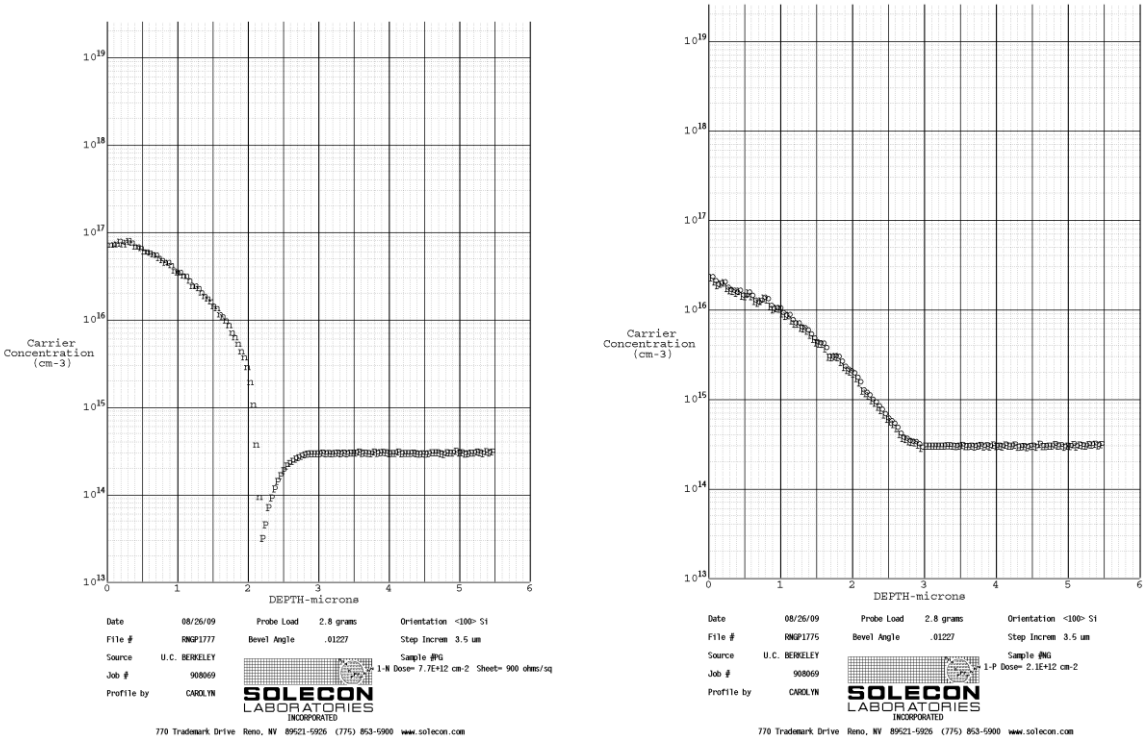


Fig. 9. P-channel (left) and N-channel (right) doping profile under gate oxide

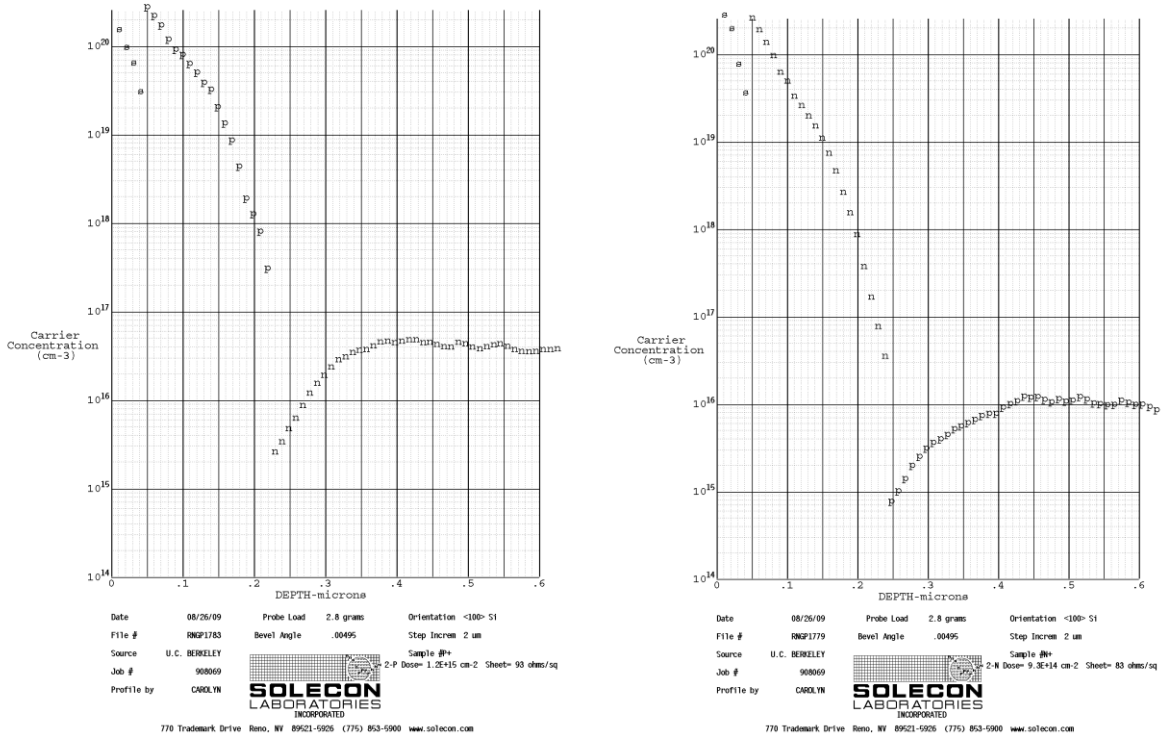


Fig. 10. P+ source-drain (left) and N+ source-drain (right) doping profile

4.3. Process and device parameters

Table 5. shows the summary of various measurements and test results of the CMOS192 process. Values shown in this table were extracted from measurements on L=0.3 µm, W=2.5 µm devices. Methods, measurement conditions, and explanations for obtaining the parameters in Table 5. are discussed in [8].

No.	Parameter	Unit	NMOS	PMOS
1	V_t	V	0.46	-0.48
2	Sub-threshold slope	mV/decade	95	85
3	K (μC_{ox})	$\mu A/V^2$	130	33
4	γ_1 ($\|V_{sb}\|$=1 V)	$V^{1/2}$	0.13	-0.41
5	γ_2 ($\|V_{sb}\|$=3 V)	$V^{1/2}$	0.27	-0.25
6	Surface dopant concentration	atoms/cm^3	2E16	7E16
7	Substrate dopant concentration	atoms/cm^3	1E16	3E16
8	T_{ox} (Gate)	nm	7.4	7.4
9	X_j (S-D depth)	µm	0.24	0.23
10	X_w (Well depth)	µm	3.0	2.3
11	R_{diff} (Sheet resistance, S-D)	Ω/square	48	41
12	R_{poly} (Sheet resistance, gate)	Ω/square	420	230
13	R_{well} (Sheet resistance, well)	Ω/square	830	730
14	R_c M1-diff	Ω	0.7	0.6
15	R_c M1-poly	Ω	0.6	0.7
16	| S-D breakdown |	V	>14	>11
17	S-D leakage (V_{ds}=3.3 V, V_{gs}=0 V)	1/µm	35 nA	90 pA
18	Effective mobility (V_{bs}=0 V, V_{gs}=1 V)	cm^2/V sec	234	61
19	Ring oscillator frequency (1 µm gate, 2 µm contact)	MHz	70.8	

Table 5. Process and device parameters of CMOS192 (W=2.5 µm and L=0.3 µm)

Electrical measurements were obtained using an automated test method; the Model 2001X Electroglas probe station (autoprobe) was connected to a semiconductor parametric test system. A PC based measurement software [9] controls the switching matrix and a modular DC source/monitor unit. All the test structures and transistors were configured with proper pad array

on the chip that would support a 2x5 pin probe card. The PC based Metrics software, which includes measurement modules, was used for parametric testing and data analysis.

1. Threshold voltages were measured by the autoprobe V_t module using the linear extrapolation method.

2. Sub-threshold slope values are hand calculated based on the Autoprobe DIBL (Drain induced barrier lowering) module. A $\log(I_{ds})$ vs. V_{gs} graph was plotted when the device was operating in the linear region; $|V_{ds}|$=50 mV. By picking a decade of I_{ds} change on the Y scale, the corresponding V_{gs} difference was read from the X scale.

3. K values (gain factor in the linear region) were obtained by hand calculation based on the Autoprobe I_{ds}–V_{gs} measurements when devices were operating in the linear region. Using the V_t module on the autoprobe, I_{ds} vs. V_{gs} and G_m vs. V_{gs} curves were plotted simultaneously ($|V_{ds}|$=50 mV). The I_{ds} and the corresponding V_{gs} values were picked where G_m maximized. Using the equations $K = \mu C_{ox}$, and

$$I_{ds} = \mu C_{ox} W/L \, (V_{gs} - V_t - V_{ds} / 2) \, V_{ds}$$

values were substituted and K was extracted.

4-5. γ_1 and γ_2 (body effect parameters at different body biases) were obtained by hand calculation based on the Autoprobe V_t measurements at different body biases. Using the V_t module, threshold voltage values were defined under different body bias conditions ($|V_{bs}|$= 0V, 1V, 3V). Using

$$V_t = V_{t,0V} + \gamma \, ((|2\Phi_B| + |V_{bs}|)^{1/2} - (|2\Phi_B|)^{1/2})$$

and

$$\Phi_B = kT/q \ln (N_{well} / n_i)$$

γ was extracted for $|V_{bs}|$ = 1 V and 3 V values.

6-7. Surface dopant concentration numbers are based on the SRA results (Fig. 9. and Fig. 10.).

8. Gate oxide thickness was measured by the Sopra ellipsometer during processing.

9-10. Well depth and the source-drain depth data arise from SRA graphs (Fig. 9. and Fig. 10.).

11-13. Sheet resistance values were obtained by four point probe measurements during processing from inline monitor wafers.

14-15. Contact resistances were measured on designated test structures by the Autoprobe CONTR_SCB module.

16. Source-drain breakdown measurements were taken using the Autoprobe.

17. Source-drain leakage values were calculated based on the graphs given by Autoprobe DIBL module. Using the log (I_{ds}) vs. V_{gs} graph, the value of I_{ds} was read at V_{gs}=0 V point on the V_{ds}= 3.3 V curve.

18. μ_{eff} (effective mobility) data came from Autoprobe measurements using the EFFMOB module. Measurement values were modified to reflect the actual C_{ox} value. The originally measured value with the EFFMOB module was multiplied by the factor of 1.23. This ratio was found between the "ideal" C_{ox} value and the lower C_{ox} value that C–V measurement showed in inversion (for "t_{ox}" = t_{ox} + partially depleted poly gate thickness). The factor of 1.23 multiplication was applied because C_{ox} is in the nominator in the μ_{eff} equation:

$$\mu_{eff} = g_d / C_{ox} (W/L) (V_g - V_{to})$$

19. The ring oscillator frequency was calculated using the autoprobe RingOsc module. An oscilloscope has to be connected the CML port of the HP4085A Switching Matrix.

4.4. Yield

Wafer maps showing transistor yield were taken by the autoprobe. Threshold voltage values for PMOS and NMOS MOSFET devices are shown in Fig. 11. V_t was measured on W=2.5 µm and L=0.3 µm devices designed with in-house design rules.

Contamination was discovered on few of the wafers, which affected the yield. The material observed was most probably of organic origins, consisting of approximately 100 nm size particles; located in a circular shape in the central area of the wafers. The contamination was discovered between steps 22-24, prohibiting gate oxide formation for a few devices in step 29.

Lower yield was seen on the edges of wafers compared to earlier runs. This resulted due to decreased uptime and working conditions of photoresist tools, SVGCoat6 and SVGDev6. Inadequate photoresist uniformity and particles were seen along the edge and wafers had to be reworked at most of the lithography steps.

A hot aluminum process split was implemented for the Metal1 layer in the Novellus m2i sputtering system. Wafers with a two-layered hot metal yielded better compared to standard deposition due to a better contact fill. Successive baseline runs will use the hot aluminum process.

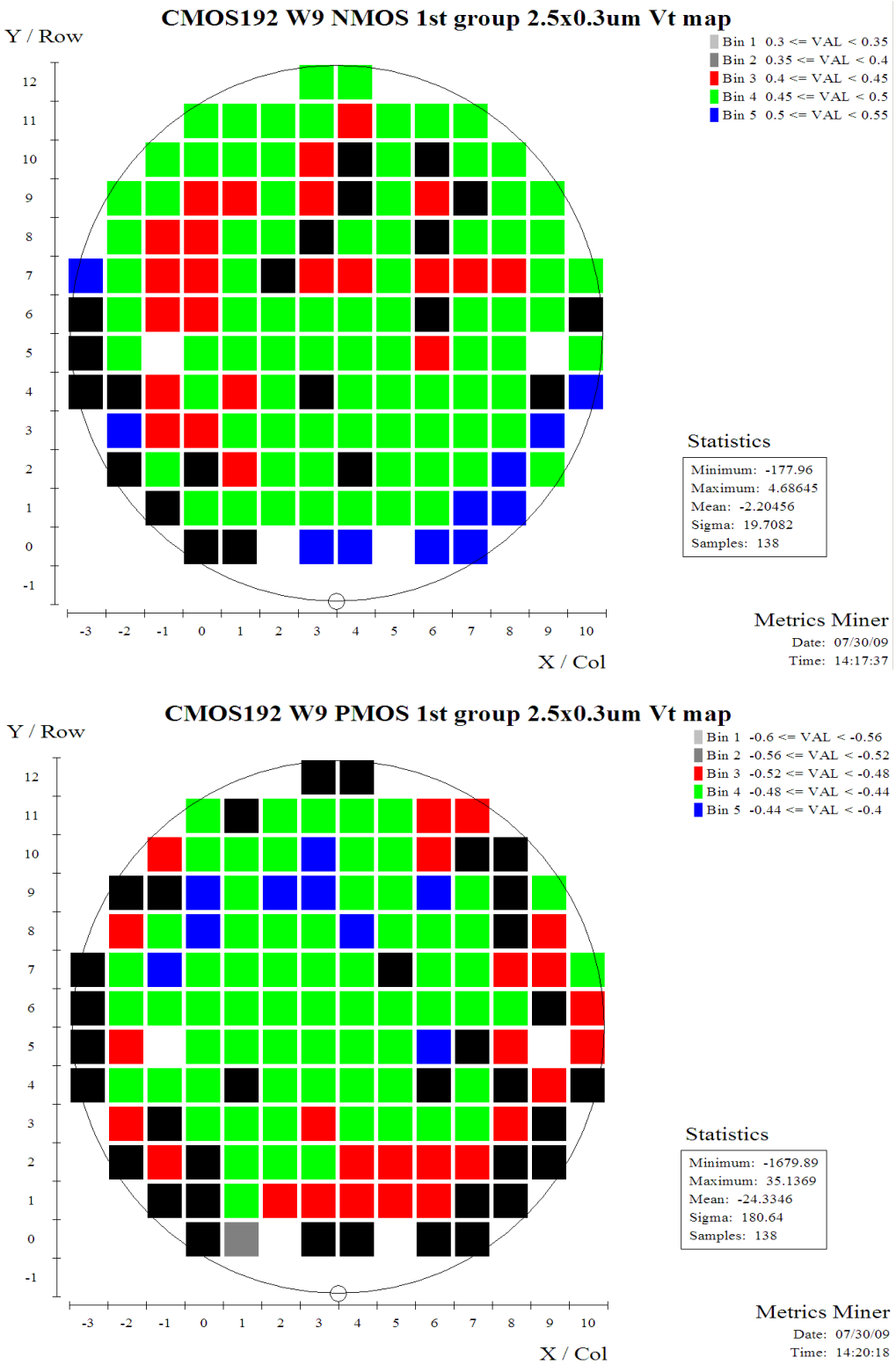


Fig. 11. Threshold voltage maps of NMOS and PMOS MOSFETS at 2.5/0.3 µm designed with in-house design rules

5. Future work

The current baseline run, CMOS192 will be repeated with the same process flow and parameters to serve as a starting point and to ensure proper equipment functionality in the new Marvell Nanofabrication Laboratory. The primary purpose of the next baseline run is to compare parametric results of the process developed in the Microlab to the start up run in the new nanofabrication facility, the Marvell Nanolab.

6. References

[1] L. Voros, S. Parsa: *Six-inch CMOS Baseline process in the UC Berkeley Microfabrication Laboratory*, Memorandum No. UCB/ERL M02/39, Electronics Research Laboratory, University of California, Berkeley (December 2002)

[2] A. Horvath, S. Parsa, H. Y. Wong: *0.35 μm CMOS process on six-inch wafers, Baseline Report IV.*, Memorandum No. UCB/ERL M05/15, Electronics Research Laboratory, University of California, Berkeley (April 2005)

[3] A. Pongracz, G. Vida: *0.35 μm CMOS process on six-inch wafers, Baseline Report V.*, Memorandum No. UCB/EECS-2007-26, Electrical Engineering and Computer Sciences, University of California, Berkeley (February 2007)

[4] L. Petho, A. Pongracz: *0.35 μm CMOS process on six-inch wafers, Baseline Report VI.*, Memorandum No. UCB/EECS-2008-168, Electrical Engineering and Computer Sciences, University of California, Berkeley (October 2008)

[5] K. Takeshi, C. Y. Cho, L. Lin: *In-situ Controlled Growth of Carbon Nanotubes by Local Synthesis*, IEEE MEMS 2007, p. 831-834

[6]E. Stern, J. Kleminc, D. Routenberg: *Label-free immunodetection with CMOS-compatible semiconducting nanowires*, Nature 445, p. 519-522

[7] R. Cambie, F. Carli, C. Combi: *Evaluation of mechanical properties by electrostatic loading of polycrystalline silicon beams*, Proceedings of the 2003 International Conference on Microelectronic Test Structures, p. 3-39

[8] D. Rodriguez: *Electrical Testing of a CMOS Baseline Process*, Memorandum No. UCB/ERL M94/63, Electronics Research Laboratory, University of California, Berkeley (August 1994)

[9] Metrics ICS and Metrics I/CV from Metrics Technology, Inc. http://www.metricstech.com/ics/ics.shtml

Acknowledgements

The author is grateful to Sia Parsa, Process Engineering Manager and Katalin Voros, Microlab Operations Manager for their guidance, encouragement and valuable support. Special thanks to Robert M. Hamilton, Microlab Equipment and Facilities Manager, and the rest of the equipment and process engineering staff for their enthusiastic help.

Biography

Laszlo Petho earned his M.S. degree in Engineering Physics in 2007 from the Technical University of Budapest, Hungary. Laszlo has been working as a baseline process engineer in the UC Berkeley Microfabrication Laboratory since November 2007. His main tasks include CMOS device fabrication and testing, training and equipment characterization.

Appendix A – CMOS Baseline 192 Process flow

Step Nr.	Process step	Substeps	Equipment / recipe	Target and process specification	Notes
0	**STARTING WAFERS**		20-60 Ω-cm, P-type, <100>, 6"		14 wafers + 2 monitor (PCH, NCH)
1	**INITIAL OXIDATION**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	1 dummy for PM etch characterization
		b) Standard cleaning	Sink 6	Piranha + 25:1 HF until dewets	
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 250 A 950C, 30 min; 20 min N2 annealing	Measure oxide thickness
2	**ZERO LAYER PHOTO**		ASML	COMBI mask UVBAKE pr. J	Defines ASML alignment PM marks
3	**SCRIBE WAFERS**		Diamond pen	Scribe numbers into photoresist	
4	**ZERO LAYER ETCH**	a) Etch through oxide	Centura-MxP+, recipe: MXP_OXSP_ETCH	250 A etch	
		b) Etch PM marks	Lam5, recipe: 5003	1200 A etch	
		c) Photoresist strip	Matrix	2.5 min O2 ash	
		d) Measure etch depth	ASIQ		
5	**PAD OXIDATION / NITRIDE DEPOSITION**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 350 A 1000C, 29 min; 15 min N2 annealing	Include NCH, PCH, measure ox. on them
		d) Nitride deposition	Tystar9, 9SNITA	Target: 2200 A	Do not include NCH, PCH, measure nitride
6	**N-WELL PHOTO**		ASML	Mask: NWELL UVBAKE pr. J	
7	**NITRIDE ETCH**		Centura-MxP+, recipe: MXP_NITRIDE_OE	Monitor endpoint	Measure oxide on each wafer (critical for impl.) Target: 250 A
8	**N-WELL IMPLANT**		CORE Systems	Specie/Dose/Energy: P, 1E13, 150 keV	Include PCH
9	**NITRIDE REMOVAL**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Nitride wet etch	Sink7	160C fresh phosphoric acid, ~4 hours	
		d) Pad oxide wet etch	Sink8	5:1 BHF until dewets	Include PCH, NCH
		a) TLC clean	Tystar2, 2TLCA	2 hrs of cleaning	

10	**PAD OXIDATION / NITRIDE DEPOSITION**	b) Standard cleaning	Sink8 + Sink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 350 A 1000C, 29 min; 15 min N2 annealing	Include NCH, PCH, measure ox. on them
		d) Nitride deposition	Tystar9, 9SNITA	Target: 2200 A	Do not include NCH, PCH, measure nitride
11	**P-WELL PHOTO**		ASML	Mask: PWELL UVBAKE pr. J	
12	**NITRIDE ETCH**		Centura MxP+, recipe: MXP_NITRIDE_OE	Monitor endpoint	Measure oxide on each wafer (critical for impl.) Target: 250 A
13	**P-WELL IMPLANT**		CORE Systems	Specie/Dose/Energy: B, 5E12, 60keV	Include NCH
14	**NITRIDE REMOVAL**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Nitride wet etch	Sink7	160C fresh phosphoric acid ~4 hours	
		d) Pad oxide wet etch	Sink8	5:1 BHF until dewets	Include NCH, PCH
15	**WELL DRIVE-IN**	a) TLC clean	Tystar2, 2TLCA	2 hrs of cleaning	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Well drive-in	Tystar2, 2WELLDR	1100C, 150 min; 15 min N2 annealing	Measure oxide thickness
		d) Oxide wet etch	Sink8	5:1 BHF until dewet	Measure Rsq on NCH, PCH
16	**PAD OXIDATION / NITRIDE DEPOSITION**	a) TLC clean	Tystar2, 2TLCA	2 hrs of cleaning	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH and dummies
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 350 A 1000C, 21 min; 15 min N2 annealing	Measure oxide thickness
		d) Nitride deposition	Tystar9, 9SNITA	Target: 2200 A	Measure nitride
17	**ACTIVE AREA PHOTO**		ASML	ACTIVE mask UVBAKE pr. U	Use BARC if needed. Stop 4 wafers for STI process before this step
18	**NITRIDE ETCH**		Centura MxP+, recipe: MXP_NITRIDE_OE	Monitor endpoint, allow some overetch	
19	**P-WELL FIELD IMPLANT PHOTO**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Lithography	ASML	Mask: PFIELD UVBAKE pr. J	
20	**P-WELL FIELD IMPLANT**		CORE Systems	Specie/Dose/Energy: B, 2E13, 80keV	

21	**LOCOS OXIDATION**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + 10 sec dip in 25:1 HF	Include NCH, PCH
		d) Wet oxidation	Tystar2, 2WETOXA	Target: 5500 A 1000C, 120 min; 20 min N2 annealing	Measure oxide
22	**NITRIDE REMOVAL / PAD OXIDE REMOVAL**	a) Oxide wet etch	Sink 6	10:1 HF for ~60 sec until dewets	Remove thin ox from nitride
		b) Nitride wet etch	Sink 7	160C fresh phosphoric acid	Measure pad ox. on ACTV area to make sure nitride is gone
		c) Oxide wet etch	Sink 6	10:1 HF for ~60 sec until dewets	Etch pad oxide
23	**SACRIFICIAL OXIDATION**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	Sink 6	Piranha + 10 sec dip into 25:1 HF	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 250 A 900C, 40 min; 1 sec (meaning zero) N2 annealing	Measure oxide on ACTV area
24	**SCREEN OXIDATION**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	Sink 6	Piranha + 25:1 HF dip until NCH, PCH dewet	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 250 A 900C, 40 min; 15 min N2 annealing	Measure oxide on ACTV area
25	**NMOS Vt IMPLANT PHOTO**		ASML	Mask: PWELL UVBAKE pr. J	
26	**NMOS Vt IMPLANT**		CORE Systems	Specie/Dose/Energy: BF2, 3E12, 50keV	Include NCH
27	**PMOS Vt IMPLANT PHOTO**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Lithography	ASML	Mask: NWELL UVBAKE pr. J	
28	**PMOS Vt IMPLANT**		CORE Systems	Specie/Dose/Energy: P, 2E12, 30keV	Include PCH
29	**GATE OXIDATON / POLY DEPOSITION**	a) TLC clean	Tystar1, 1TLCA	2 hours of cleaning	
		b) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha + dip in 25:1 HF until NCH, PCH dewet	Include NCH, PCH, Tox, Tpoly1, Tpoly2
		c) Gate oxidation	Tystar1, 1THIN-OX	Target: 80 A 850C, 30 min oxidation; 900C, 30 min N2 anneal	Include NCH, PCH, Tox, Tpoly1, Tpoly2

		d) Poly-Si deposition	Tystar10, 10SUPLYA	Target: 2500 A Dep. Time: ~ 28 min	Include Tpoly1, Tpoly2 and dummy wafers
		e) Measurements	Sopra, Rudolph	Measure oxide thickness on Tox	
			SCA	Measure Dit, Qox, Nsc, Ts on Tox	
			Nanospec		
			4PTPRB	Strip oxide from NCH and PCH; measure Rsq	
30	**POLY GATE PHOTO**		ASML	Mask: POLY UVBAKE program U	Use BARC if needed
31	**POLY ETCH**	a) Poly etch	Lam5, recipe 5003	Monitor endpoint, ~50% over etch	Etch through BARC
		b) Photoresist strip	Matrix	2.5 min O2 ash	
		c) Standard cleaning	Sink7 + Sink 8	100:1 HF dip to remove polymers formed in Lam5, Piranha	
		d) Measure channel length with SEM	Leo	Check Poly-Si lines with SEM	
32	**PMOS LDD IMPLANT PHOTO**		ASML	Mask: PSELECT UVBAKE pr. J	
33	**PMOS LDD IMPLANT**		CORE Systems	Specie/Dose/Energy: BF2, 5E13, 10keV, +7º tilt @ 0 orientation; BF2, 5E13, 10keV, -7º tilt @ 180 orientation	Include PCH, Tpoly1
34	**NMOS LDD IMPLANT PHOTO**	a) Photoresist strip	Matrix	Std. 2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Lithography	ASML	Mask: NSELECT UVBAKE pr. J	
35	**NMOS LDD IMPLANT**		CORE Systems	Specie/Dose/Energy: As, 5E13, 30keV, +7º tilt @ 0 orientation; As, 5E13, 30keV, -7º tilt @ 180 orientation	Include NCH, Tpoly2
36	**LDD SPACER DEPOSITION**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha	
		c) TEOS deposition	P-5000; recipe AH-USG	Target: 4000 A; Dep. rate: ~80 A/sec	
		d) Annealing	Tystar2; 2HIN2ANA	900C, 30 min	
		e) Measurement	Nanospec		
37	**LDD SPACER FORMATION**		Centura MxP+, recipe: MXP_OXSP_ET_EP	Monitor endpoint, stop etch when drops	Verify completion of etch on ACTV area, cross-sectional SEM

38	**P+ GATE & S/D PHOTO**		ASML	Mask: PSELECT UVBAKE program J	
39	**P+ GATE & S/D IMPLANT**		CORE Systems	Specie/Dose/Energy: B, 3E15, 20keV	Include PCH, Tpoly1
40	**N+ GATE & S/D PHOTO**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Lithography	ASML	Mask: NSELECT UVBAKE pr. J	
41	**N+ GATE & S/D IMPLANT**		CORE Systems	Specie/Dose/Energy: P, 3E15, 40keV	Include NCH, Tpoly2
42	**BACK SIDE ETCH**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8	Piranha	
		c) Coat wafers	SVGCOAT6	No litho step UVBAKE pr. J	Coat front side
		d) Oxide wet etch	Sink8	5:1 BHF until backside dewets	Dip off native oxide
		e) Poly-Si etch	Lam5 recipe 5003	No overetch step	Etch to endpoint plus 10 sec
		f) Oxide wet etch	Sink8	5:1 BHF until backside dewets	Include NCH, PCH, Tpoly1, Tpoly2
43	**GATE & S/D ANNEALING**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha	Include NCH, PCH, Tpoly1, Tpoly2
		c) RTA annealing	Heatpulse3, recipe 1050RTA6.RCP	450C 30 sec, 900C 10 sec, 1050C 5 sec	Device chamber, N2 atmosphere
		d) Measurement	4PTPRB	Measure Rs on NCH, PCH, Tpoly1, Tpoly2	For gate <250 Ohm/sq, for S/D <100 Ohm/sq
44	**SILICIDATION**	a) Sputter etch	Novellus, recipe ETCHSTD	1 min etch	Sputter etch, include a dummy
		b) Ti deposition	Novellus, recipe TI300STD	25 sec deposition	Measure Rsq of Ti film
		c) RTA annealing	Heatpulse3, recipe 650RTA6.RCP	450C 20sec, 650C 15sec	Silicide chamber, N2 atmosphere
		d) Wet etch Ti & TiN	Sink7	Remove unreacted Ti and TiN in fresh piranha	Measure field ox on LOCOS area to check etch completion
45	**PSG DEPOSITION & DENSIFICATION**	a) Standard cleaning	Sink 6	Piranha (NO HF dip)	Include PCH, NCH, Si and TiSi test wafers
		b) PSG deposition	Tystar11, recipe 11SDLTOA	Target: 7000 A ~45 min, 450C	
		c) Coat wafers	SVGCOAT6	No litho step UVBAKE pr. J	
		d) Oxide wet etch	Sink8	5:1 BHF until backside dewet	Dip off native oxide
		e) Photoresist strip	Matrix	2.5 min O2 ash	

		f) Standard cleaning	Sink8+Sink6	Piranha	
		g) RTA annealing	Heatpulse3, recipe 900RTA6.RCP	450C 30 sec, 900C 10 sec	Silicide chamber, N2 atmosphere
		h) Measurement	Nanospec		Measure LOCOS+TEOS on a LOCOS area
			4PTPRB		
46	**SECOND PM MARK PHOTO AND ETCH**	a) Litho	ASML	Mask: COMBI UVBAKE pr. U	Define 4 new PM marks
		b) PM mark etch	Centura-MxP+, recipe: MXP_OXSP_ETCH	1200 A etch	
		c) Photoresist strip	Matrix	2.5 min O2 ash	
47	**CONTACT PHOTO AND ETCH**	a) Standard cleaning	Sink8 + Sink 6	Piranha, NO HF	
		b) Litho	ASML	Mask: CONTACT UVBAKE pr. U	Overexpose contact (30-40 mJ/cm2)
		c) Contact etch	Centura-MxP+, recipe: MXP_OXSP_ET_EP	Allow 15 sec after signal drops	
		d) Measurement	Manual probe		ACT+CONT and POLY+CONT areas
48	**METAL 1 DEPOSITION**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha, NO HF	Include a dummy. HF damages silicide!
		c) Sputter etch	Novellus, recipe: ETCHSTD	1 min etch	
		d) Al deposition	Novellus: Ti liner (TI300STD) Al/2%Si (AL6KGV)	Target: 6000 A	
		e) Measure Rs	4ptprb		Estimate thickness
49	**METAL1 PHOTO**		ASML	BARC litho, Mask: METAL1 UVBAKE pr. U	
50	**METAL1 ETCH**	a) Al etch	Lam3, Standard recipe	allow 50% overetch	No need to etch BARC separately
		b) Measurement	Manual probe		R=inf on LOCOS area required
51	**SINTERING**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Rinse	Sink8	Rinse and spin dry, no piranha or HF	
		c) Sintering	Tystar18, recipe: H2SINT4A.018	20 min, 400C	
52	**TESTING**		Autoprobe	Test devices with 1 metal layer	Vt, IdVd, Isat, EffMob, Body effect
53	**DIELECTRIC DEPOSITION AND PLANARIZATION**	a) TEOS deposition	P-5000, recipe: AP-USG2	Target: 2um; Dep. rate: ~80 A/sec (No LTO allowed, only TEOS!)	Measure total oxide thickness on MET2+VIA2 area before and after deposition

		b) Planarization	CMP, recipe: oxide_st00	1 um removal	Measure oxide thickness on MET2+VIA2 for CMP removal
54	**VIA1 PHOTO**	a) Rinse wafers	Sink8	Rinse and spin dry, no piranha or HF	Dehydrate wafers in 120C oven for 30 min
		b) Lithography	ASML	Mask: VIA1 UVBAKE pr. U	
55	**VIA1 ETCH**	a) Oxide etch	Centura-MxP+, recipe: MXP_OXSP_ET_EP	Monitor endpoint, allow 15 sec overetch after signal drops	
		b) Measurement	Manual probe		MET1+VIA area
56	**METAL 2 DEPOSITION**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Sputter etch	Novellus, recipe ETCHSTD	1 min etch	
		c) Al deposition	Novellus, Std. Al process	Target: 9000 A	Measure Rsq of Al film
57	**METAL2 PHOTO**	a) Opening PM marks	ASML	Mask: blank UVBAKE pr. U	
		b) Etch Al from 4 dies	Lam3, Standard recipe		
		c) Photoresist strip	Matrix	2.5 min O2 ash	SVC-14 at 80C for 10 min for dense structures
		d) Metal2 lithography	ASML	BARC litho, Mask: METAL2 UVBAKE pr. U	
58	**METAL2 ETCH**	a) Al etch	Lam3, Standard recipe	allow 50% overetch	watch PR thickness
		b) Measurement	Manual probe		MET2 area
		c) Photoresist strip	Matrix	2.5 min O2 ash	
59	**TESTING**		Probe station	Test devices with 2 metal layers	M1-M2 contact resistors and chains, ring oscillators
60	**DIELECTRIC DEPOSITION AND PLANARIZATION**	a) TEOS deposition	P-5000, recipe: AP-USG2	Target: 2 um	Measure total oxide thickness on MET3 area before and after deposition
		b) Planarization	CMP, recipe: oxide_st00	1 um removal	Measure oxide thickness on MET3 for CMP removal
61	**VIA2 PHOTO**	a) Rinse wafers	Sink8	Rinse and spin dry, no piranha or HF	
		b) Lithography	ASML	Mask: VIA2 UVBAKE pr. U	
62	**VIA2 ETCH**	a) Oxide etch	Centura-MxP+, recipe: MXP_OXSP_ET_EP		Use patterned test wafers to verify endpoint
		b) Measurement	Manual probe		MET2+VIA2 area
63	**METAL 3 DEPOSITION**	a) Photoresist strip	Matrix	2 min O2 ash	
		b) Sputter etch	Novellus, recipe ETCHSTD	1 min etch	

		c) Al deposition	Novellus, Std. Al process	Target: 9000 A	Measure Rsq of Al film
64	**METAL3 PHOTO**	a) Opening PM marks	ASML	Mask: blank UVBAKE pr. U	
		b) Etch Al from 4 dies	Lam3, Standard recipe		
		c) Photoresist strip	Matrix	2.5 min O2 ash	SVC-14 at 80C for 10 min for dense structures
		d) Metal2 lithography	ASML	BARC litho, Mask: METAL3 UVBAKE pr. U	
65	**METAL3 ETCH**	a) Al etch	Lam3, Standard recipe	allow 50% overetch	PR thickness!
		b) Measurement	Manual probe		MET3 area
		c) Photoresist strip	Matrix	2.5 min O2 ash	
66	**TESTING**		Probe station	Test devices with 3 metal layers	M2-M3 contact resistors and chains

Appendix B – ASML mask layouts

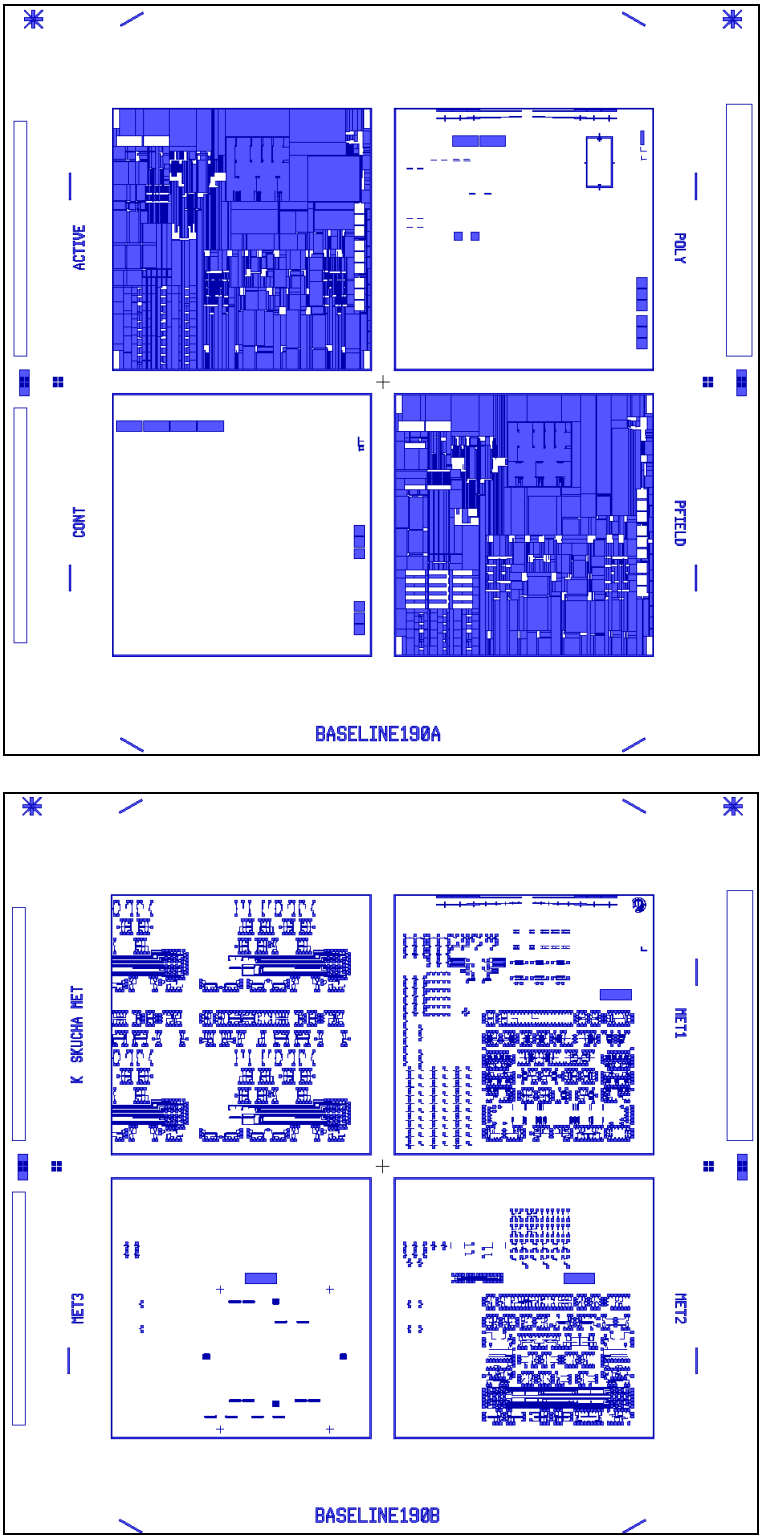


Fig. 12. Tape-out mask plates fabricated by Benchmark Technologies; including Active, Poly, Contact, P-field and Metal layers.

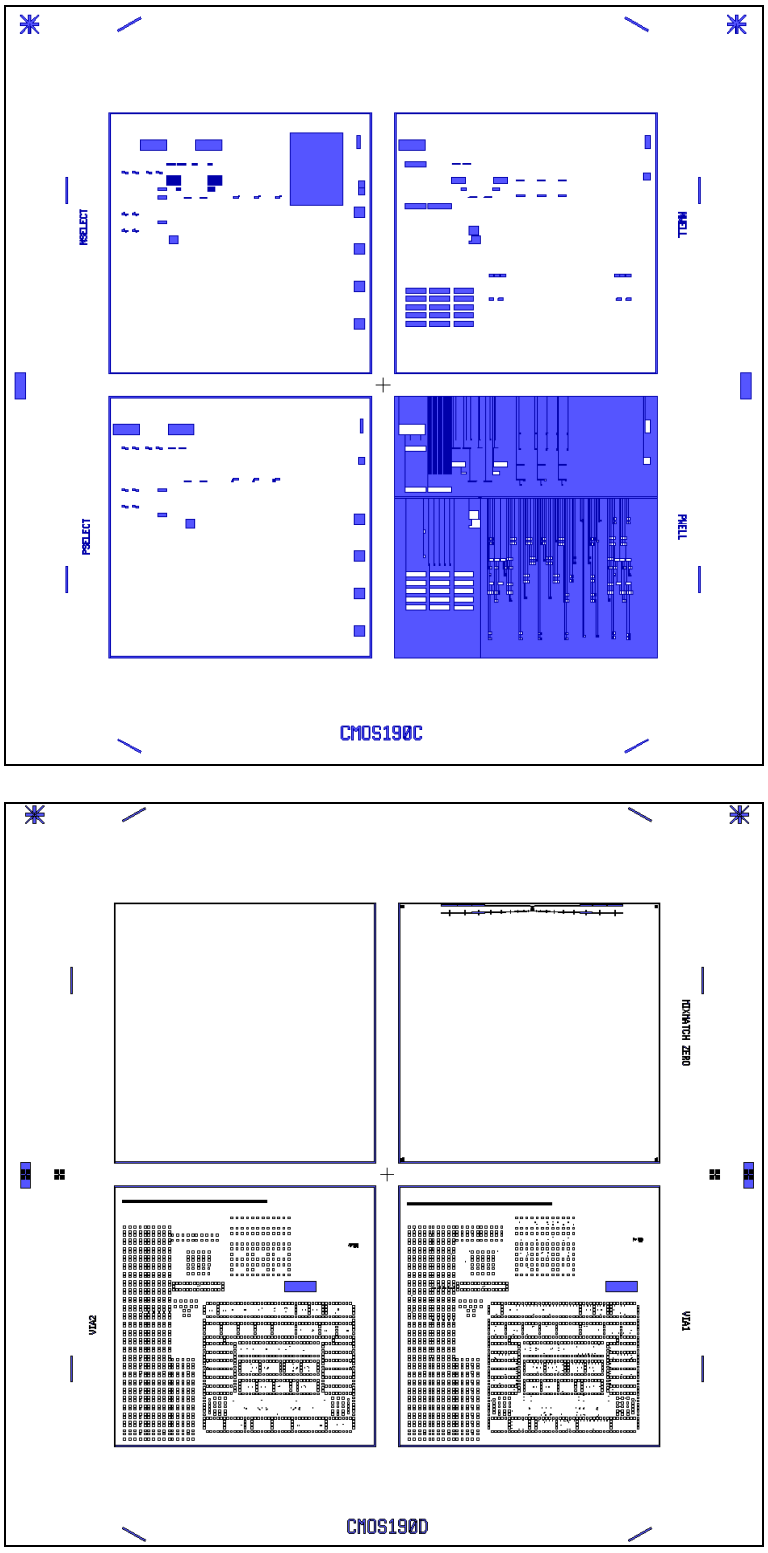
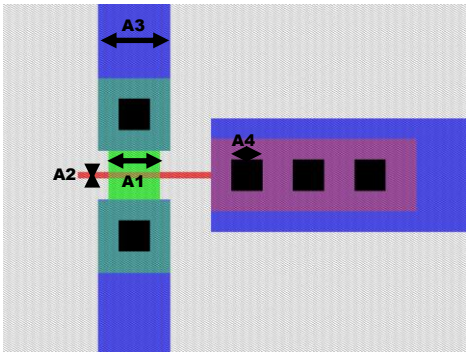


Fig. 13. Mask plates made in the Microlab by the GCA3600 pattern generator; quadrants include the multiple use N-select, P-select, N-well and P-well layers and the Via layers.

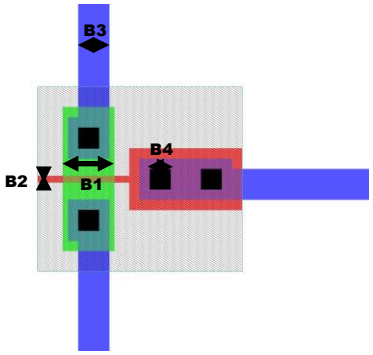
Appendix C – Layout design rules

1st column of transistors with robust design (In house design rules applied)



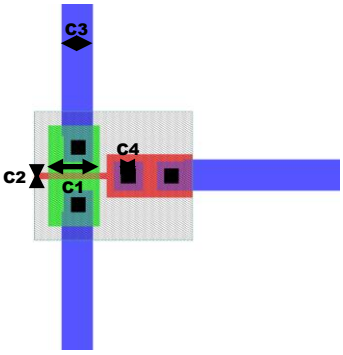
A.1. Gate width: 2.5 µm
A.2. Gate length: 0.3 µm
A.3. Metal line width: 3.5 µm
A.4. Contact hole: 1.5 µm

2nd column of transistors with λ=0.5 µm (HP design rules applied)



B.1. Gate width: 2.5 µm
B.2. Gate length: 0.3 µm
B.3. Metal line width: 1.5 µm
B.4. Contact hole: 1 µm

3rd column of transistors with λ=0.35 µm (HP design rules applied)



C.1. Gate width: 2.5 µm
C.2. Gate length: 0.3 µm
C.3. Metal line width: 1.5 µm
C.4. Contact hole: 0.7 µm