A Statistical Flicker Noise Analytical Model in Scaled Bulk MOSFETs

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Acknowledgement

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Research Project

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Contents

I. INTRODUCTION

The continuous downscaling of CMOS technologies has resulted in a strong improvement in the RF performance of MOS devices [1]. The scaling of CMOS leads to MOSFET with high unity-gain frequencies, which becomes very attractive option for analog RF applications and RF systems-on-chip. [2], [3]. The statistical flicker noise (1/f noise) in planar bulk MOSFET has received increasing attention with the proliferation of RF applications. At low frequencies, 1/f noise is the dominant source of noise in MOSFET devices [1]. The low frequency 1/f noise in deep-submicron MOSFET causes a significant increase in noise that impacts the performance of analog and RF CMOS circuits, such as high performance operational amplifiers, precision ADC/DACs, and low IF mixers [4]. Flicker noise has a serious impact on RF CMOS circuits such as voltage-controlled oscillators (VCOs), where it causes a significant increase in the phase noise [1], [4]. Accurate modeling of flicker noise in modern CMOS technologies is a prerequisite low-noise RF circuit design.

Flicker noise exhibits different characteristics for large and small MOSFETs. For a large device, flicker noise shows a clean 1/f behavior across all frequency range shown in Fig. 1(a)[1]. As a device scales down and the transistor area becomes smaller, flicker noise begins to exhibit more Lorenztian-like shape and thus more device-to-device variation characteristics shown in Fig. 1(b) [5]. Due to this large noise variation in scaled MOSFETs, it is necessary to develop a feasible statistical flicker noise compact model. In Fig. 1, noise power can be denoted as either the current noise power $S_{Id}(f)$ or the input referred noise power $S_{Vg}(f)$. The relationship between $S_{Id}(f)$ and $S_{Vg}(f)$ is $S_{Vg}(f) = S_{Id}(f)/g_m^2$, where g_m is the MOSFET trans-conductance [1]. In this report, noise power is expressed as current noise power $S_{Id}(f)$.

W/L=10μm/0.28μm

W/L = 0.16μm/0.13μm
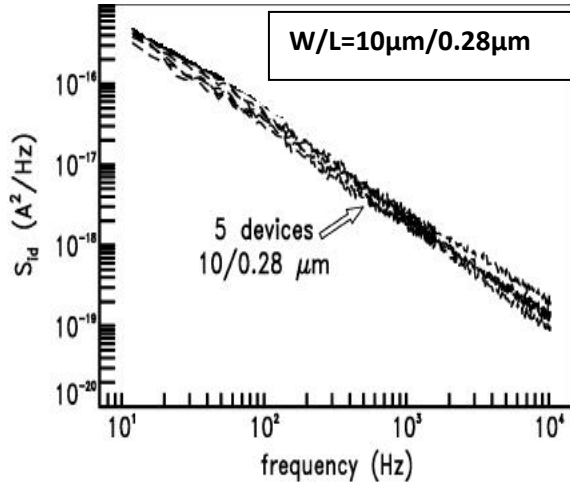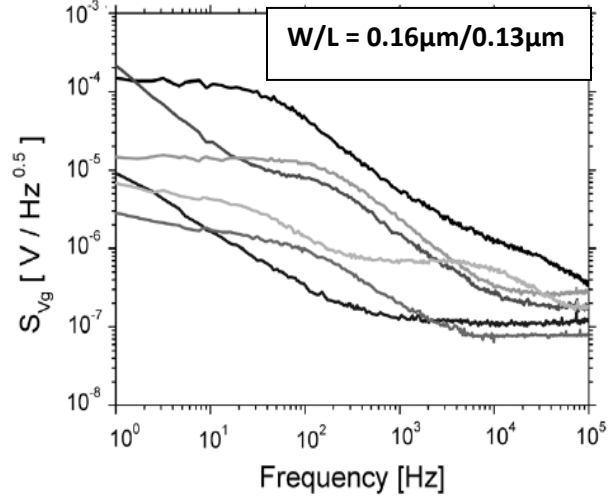
(a)   (b)

Figure 1: Measured flicker noise characteristics for (a) large area devices which shows clean 1/f shape [1], and for (b) small area devices which shows Lorenztian-like shape with large device-to-device variation [5].

This report is organized into eight sections. Section I introduces the significance of accurate statistical noise compact model. Section II reviews the most commonly accepted mechanism of flicker noise and the cause of differences in noise spectra between large and small area devices. Section III discusses the three key variables in the previously developed statistical Monte Carlo model. Section IV proposes the new statistical Analytical model for flicker noise in scaled MOSFET. Section V discusses three important experimental observations. In Section VI, the experimental data which supports and verifies the Analytical model is presented. Section VII proposes the future usage and application of the Analytical model. Section VIII concludes the paper.

II. FLICKER NOISE MECHANISM

According to the Carrier Number Fluctuation Theory, the flicker noise is attributed to the trapping and detrapping of charge carriers in traps located in the gate dielectric [1]. Fig. 2 shows a schematic drawing of charge carrier exchange process between the oxide traps and the inversion layer in a MOSFET. Every single trap that is located in the dielectric oxide leads to a Lorentzian noise power spectrum. For a uniform spatial trap distribution, the Lorentzian spectra add up to give a 1/f characteristic [1].
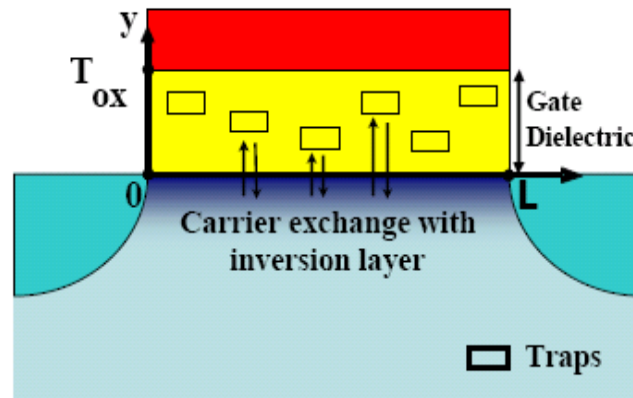
Figure 2: Schematic of traps in the dielectric oxide layer in a MOSFET. Flicker noise is caused by carrier trapping and detrapping process according to the Carrier Number Fluctuation Theory.

Although a quantitative understanding of the flicker noise generation mechanism has not been fully established, the prevailing mechanism points to the trapping and de-trapping of charge carriers from the oxide dielectric for both NMOS and PMOS. The capture and emission of a carrier by the trap result in discrete modulations of the channel current referred to as Random Telegraphic Noise (RTN) in the time domain [6]. Flicker noise is the frequency domain representation of RTN, which is measured by total drain current noise power, S_{Id} (f).

The current Unified model describes the measured 1/f noise characteristics of both large area NMOS and PMOS using a single model [1]. The Unified model extends the Carried Number Fluctuation Theory to include carrier mobility fluctuation due to Coulombic scattering effect of the fluctuating oxide charge [7]. Therefore, both the number of charge carriers in the channel and their mobility fluctuations are correlated since they originate from the same source [1]. The Unified model can predict the correct magnitude and bias dependence of parameters used for modeling the flicker noise [7]. This model is used in many of today's compact MOSFET models, such as BSIM3 and BSIM4.

A. Single Trap Random Telegraphic Noise (RTN)

The origin of flicker noise comes from carrier captured and emitted by the traps in the oxide. Since carrier capture and emission processes are primarily tunneling process, each trap is associated with a specific tunneling rate. The probability of a charge carrier penetrating into the oxide decreases exponentially with the increasing distance from the silicon interface to the gate interface. The tunneling rate decreases exponentially with the increase of the depth of the trap in the dielectric (y) from the silicon-oxide interface. Thus, the trapping/tunneling time constant (τ), which is the inverse of the tunneling rate, increases exponentially with the increase of y.

$$\tau = \tau_0 e^{\gamma \cdot y} \qquad (1)$$

τ_0 is defined as the trapping time constant at the silicon-oxide interface, γ is the tunneling or attenuation coefficient [7] , and y is the depth of the trap in the dielectric measured from the silicon-dielectric interface. γ depends on temperature, frequency, and material properties [8]. Typically, τ_0 is 10^{-10} sec and γ is 10^8 cm^{-1} for SiO$_2$ dielectric.

Every single trap that is located in the dielectric oxide leads to a Lorentzian noise power spectrum. RTN for a single trap level which is associated with a time constant τ is responsible for each Lorenzian noise. According to the Carrier Number Fluctuation Theory, RTN can be expressed by [9], where ω is the angular frequency which is equal to $2\pi f$.

$$RTN \quad \propto \quad \frac{\tau}{1 + \omega^2 \tau^2} \qquad (2)$$

B. Flicker Noise S_{Id} (f) for both Large and Small Area Devices

In MOSFET, multiple-trap levels contribute to the total drain current noise power, S_{Id} (f). In a large area device, flicker noise is the integral of RTN over the total dielectric depth T_{ox}. Assuming a spatially uniform trap density inside the dielectric, the flicker noise for a large area device can be written as [7]:

$$S_{Id}(f) = \int_0^{T_{ox}} RTN dy \qquad (3)$$

For a small area device, there are only a few traps present in the gate dielectric and the spatially uniform trap density assumption in large area device may not be entirely valid for small area device. S_{Id} (f) is the numerical discrete sum of the RTN from all individual traps in the dielectric.

$$S_{id}(f) = \sum_{i=0}^{i=N_{tr}} RTN_i \, dy \qquad (4)$$

For each trap, the noise power spectrum shows a Lorenztian shape associated with a specific corner frequency defined by the trapping time constant in Eq. 1. The origin of flicker noise for both large and small area devices is illustrated in Fig. 3. For a large area device with

uniform density traps, the sum of many Lorenztian spectra with corner frequencies that are

exponentially distributed yields a 1/f straight line as shown in Fig. 3(a). Since the number of

traps in large area device is large, device to device variation is small because the sum of all

Lorenztian averages out the trap variations. However, for a small area device, even though the

origin of noise is the same, the noise characteristics look dramatically different. For a small area

device with few traps, only a few time constants exist and S_{Id} (f) yields a Lorenztian-like
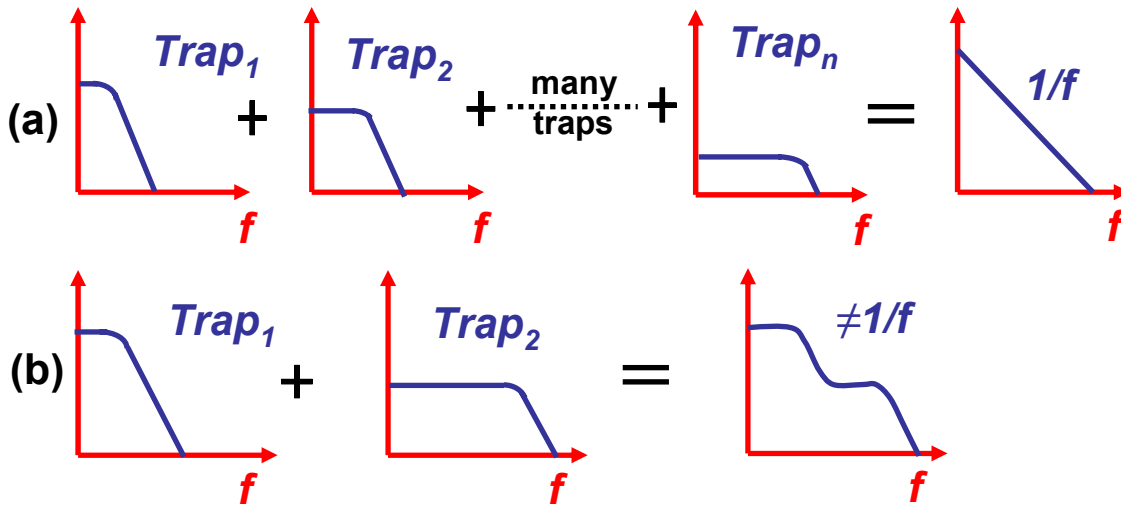
spectrum shown in Fig. 3(b).

Figure 3: Schematic illustration of (a) 1/f noise in a large area device and (b) Lorenztian-like
noise spectrum in a small area device. The individual Lorentzian represents the RTN from a
single trap in the dielectric. Flicker noise is the discrete number of RTN from all traps.

This discrete sum flicker noise concept can explain the large variation observed in small

area devices. For two small devices of the same area, even though the number of traps could be

identical, the location of the traps may be different resulting in different RTNs. Hence, the same

number of traps in different small area devices may have different impact on noise, which can

result in very different Lorenztian spectra. The discrete sum flicker noise concept is used as a

foundation to build both the statistical Monte Carlo and the Analytical compact models.

III. KEY VARIABLES IN THE MONTE CARLO MODEL

Statistical Flicker Noise Monte Carlo Compact Model introduced by Dunga Mohan, Ph.D consists of three key variables. The three key variables are the number of traps (N_{tr}), the location of traps along the dielectric oxide depth (y), and the energy level of traps (E_{tr}).

The first variable is N_{tr}. Due to the discrete nature of the number of traps, N_{tr} is expected to follow Poisson statistics [5]. The average number of traps $< N_{tr} >$ has an expected value of WLN_t, where WL is the device area and N_t is the average trap density fixed for all devices in a given technology. When applying the Monte Carlo process, if the random number generator produces a cumulated probability of 0.82, the random device sample with $<N_{tr}> = 5$ will have 6 traps based on Poisson statistics.

The second variable is the trap location inside the insulator (y). Large area 1/f noise in MOSFETs has a spectrum with a slope that varies between ~-0.8 and ~-1.2 on a double-log plot [10]. In the unified model, the model parameter EF represents the slope of the 1/f line shown in Fig. 4, which can be extracted from large area device noise spectrum. A uniformly spatial density of traps (EF=1) is a special case and yields 1/f noise for large device. However, the measurement of noise in large area devices allows for $1/f^{EF}$ suggesting a non-uniform trap distribution. EF not equaling to 1 suggests non-uniform trap density in the dielectric [10]. To describe the trap distribution along the depth of the dielectric, an exponential trap distribution model is proposed below [11].

$$N_{tr} = N_{T0} \, e^{\gamma(EF - 1)y} \qquad (5)$$

N_{T0} represents the trap density at silicon-oxide interface and γ is the attenuation coefficient of the electron wave function in the oxide. When EF=1, the exponential term is reduced to 1 and $N_{tr} =$

N_{T0} in all y direction, which indicates that the trap distribution is uniform along y axis. When EF<1, the number of traps exponentially decreases from the substrate surface to the gate surface. When EF>1, the number of traps exponentially increase from the substrate surface to the gate surface. The distribution of traps as a function of EF is illustrated in Fig. 5.
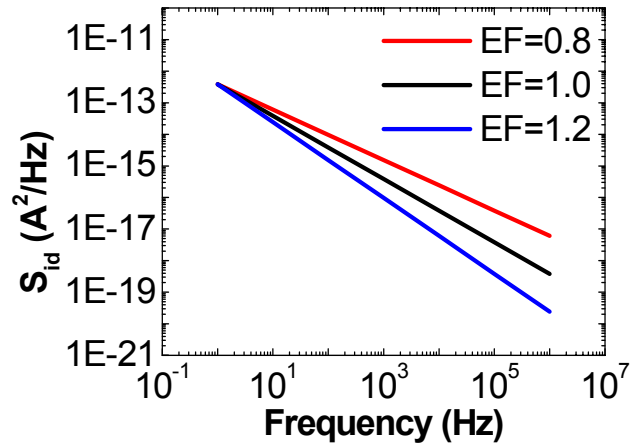

Figure 4: EF represents the slope of 1/f line in noise spectrum double-log plot and has a typical value between ~0.8 and ~1.2 [10].
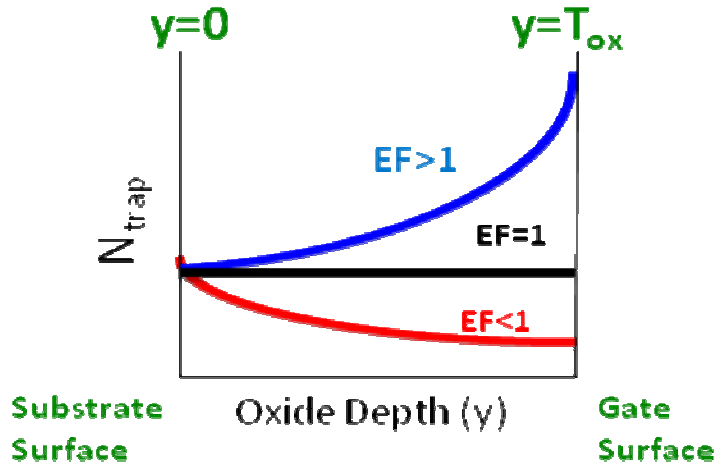

Figure 5: Trap density distributions can be represented as a function of y and EF in the flicker noise statistical model. The exponential trap density distribution enables the modeling of experimentally observed $1/f^{EF}$ noise spectrum where EF$\neq$ 1.

The third variable is the trap energy (E_{tr}) associated with each trap. The difference between the energy of the trap level and the Fermi-level of the device (E_f) has an impact on the magnitude of noise. The trap energy levels which are located close to E_f exchange carriers easily and contribute more to noise. The traps energy levels which are away from E_f are relatively inactive and contribute less to noise. The trap contributes maximum noise when its energy is aligned with E_f. The impact on noise decreases exponentially as the trap moves away from E_f [12]. In the Monte Carlo model, trap energy is assumed to be uniformly distributed. By changing gate bias (Vg), one can modulate the trap energy level and thus its impact on noise [13].

IV. STATISTICAL ANALYTICAL MODEL

The Analytical model which describes the mean and the standard deviation can be used as an alternative to the Monte Carlo model. The population mean describes the central location, which is the arithmetic average of the all noise powers from all devices across the frequency range. The standard deviation is the most common indicator of the dispersion of the noise, measuring how widely the noise power spreads. With the correctly modeled mean and standard deviation, it is sufficient to describe the flicker noise statistics.

A. Statistical Mean, $<S_{Id}(f)>$

The statistical mean $<S_{Id}(f)>$ of flicker noise is the arithmetic average noise power generated by all devices of a same area in a given technology (Eq. 6), where N is the number of devices in a small area device sample.

$$< S_{Id}(f) >= \frac{\sum_{i=1}^{i=N} S_{Id}(f)_i}{N} \qquad (6)$$

Conceptually, if many small-area devices of the same area are placed side by side, the resultant combined device area will be large, which is equivalent to a single large-area device.

Equivalently, the numerical summation of all Lorenztian-shape spectrums observed in small devices will be a single 1/f straight line shape observed in large area device. Therefore, the average small area noise power $<S_{Id}(f)>$ will resemble large area device noise characteristics, in which there is a single 1/f straight line. Since the currently available Unified model can model large-area device flicker noise accurately and has been successfully used in the industry for many years, small area device flicker noise mean $<S_{Id}(f)>$ should be modeled by the Unified model as well. Alternatively, if the Unified model can accurately simulate noise for a large area device, the same model parameters in the Unified model can also be used to predict $<S_{Id}(f)>$ of the small area devices in the same technology.

B. Statistical Standard Deviation, σ (f)

In statistics, standard deviation is defined as the root-mean-square (RMS) deviation of the values from the mean. Since $<S_{Id}(f)>$ has the 1/f shape resembling large area noise simulated by the Unified model, the standard deviation σ (f) which is defined as in Eq. 7 [5] also has the 1/f characteristics, and thus is a function of the frequency.

$$\sigma(f) = \sqrt{<S_{Id}(f)^2> - <S_{Id}(f)>^2} \qquad (7)$$

Since both σ(f) and $<S_{Id}(f)>$ are frequency-dependent and follows similar 1/f shape, it is convenient to model the normalized standard deviation σ_n defined by the ratio of the standard deviation to the mean [5].

$$\sigma_n = \frac{\sigma(f)}{<S_{Id}(f)>} \qquad (8)$$

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Previously, we have showed in Eq. 4 that small area device noise power S_{Id} (f) is the summation of each RTN from all N_{tr} traps. For the same reason, the mean $< S_{Id}$ (f)$>$ is also proportional to the average number of traps $<N_{tr}>$.

$$< S_{Id}(f) > \propto < N_{tr} > \qquad (9)$$

Since $<S_{Id}$ (f)$>$ is proportional to the average trap number $<N_{tr}>$, the variance of the noise $\sigma(f)^2$ is also proportional to the variance of trap number $\sigma_{Ntr}{}^2$.

$$\sigma(f)^2 \propto \sigma_{N_{tr}}{}^2 \qquad (10)$$

We have also stated previously that the number of trap N_{tr} can be described by Poisson statistic. In Poisson statistics, the variance of a Poisson random variable, which is the square of standard deviation, is equal to its mean value shown in Eq. 11 [14].

$$\frac{\sigma_{N_{tr}}}{< N_{tr} >} = \frac{\sqrt{< N_{tr} >}}{< N_{tr} >} = \frac{1}{\sqrt{N_{tr}}} \qquad (11)$$

Combining Eq. 9, 10, and 11, we obtain that the normalized standard deviation $\sigma_{n,}$ which is inversely proportional to the square root of average trap number $<N_{tr}>$.

$$\sigma_n = \frac{\sigma(f)}{<S_{Id}(f)>} = \frac{\sigma_{N_{tr}}}{< N_{tr} >} = \frac{1}{\sqrt{< N_{tr} >}} \qquad (12)$$

Although the number of traps varies from device to device, the average number of traps $<N_{tr}>$ for a device is fixed for a given technology, which depends on the existing fabrication

process. $<N_{tr}>$ can be further defined as a function of average trap density N_T and the transistor area WL, where W is the gate width and L is the gate length [14].

$$< N_{tr} > \propto N_T \times W \times L \tag{13}$$

The tunneling time constant τ can be expressed as the inverse of frequency:

$$\tau = \frac{1}{f} \tag{14}$$

and

$$\tau_0 = \frac{1}{f_0} \tag{15}$$

In Eq. 1, the time constant can be replaced by the frequency terms:

$$\frac{1}{f} = \frac{1}{f_0} e^{\gamma \cdot y} \tag{16}$$

Plug Eq. 16 into Eq. 5:

$$N_{tr} = N_{T0} e^{\gamma (EF-1)y} = N_{T0}(e^{\gamma \cdot y})^{EF-1} = N_{T0}(\frac{f_0}{f})^{EF-1} \tag{17}$$

From Eq. 17, we obtain N_{tr} as a function of frequency:

$$N_{tr} \propto f^{1-EF} \tag{18}$$

Combining Eq. 13 and Eq. 18, N_{tr} has a final expression:

$$N_{tr} \propto N_T \times W \times L \times f^{1-EF} \tag{19}$$

Substitute N_{tr} from Eq 19 into Eq. 12, σ_n can be expressed as:

$$\sigma_n \propto \frac{1}{\sqrt{N_{tr}}} \propto \left(\frac{1}{\sqrt{N_T \times W \times L \times f^{1-EF}}} \right) \tag{20}$$

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Here, a new parameter NOIS is introduced and defined in Eq. 21. NOIS, like many other parameters in the model card, needs to be extracted in order to use this statistical Analytical model.   Here we have assumed that NOIS is a constant and does not have a bias dependence. The bias dependence of σ (f) originates from the bias dependence of $<S_{Id} (f) >$ only.

$$NOIS = \frac{1}{\sqrt{N_T}} \qquad (21)$$

$$\sigma_n = \frac{\sigma(f)}{< S_{Id}(f) >} = \frac{NOIS}{\sqrt{W \times L}} f^{\frac{EF-1}{2}} \qquad (22)$$

Eq. (22) is the final form of the model and σ_n is inversely proportional to the square root of the device area and has a frequency dependence. For small area devices, noise variance σ_n^2 is large. As the device area gets larger, the noise variance becomes smaller. Fig. 6 illustrates the relationship between σ_n and EF.
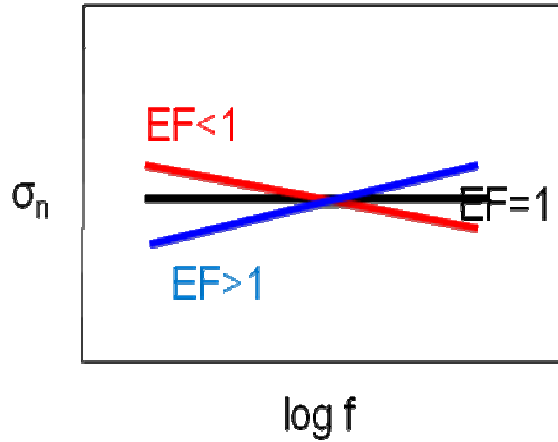

Figure 6: Schematic representation of normalized standard deviation σ_n vs. frequency on a log scale. σ_n is a function of EF for devices of the same area.

For EF=1, the traps are uniformly distributed along the dielectric depth y. Since the number of traps contributing to all frequency noise is the same, σ_n is a constant for all frequencies. For EF<1, there are more traps close to the substrate-oxide surface, the number of

traps contributing to high frequency noise is larger, and thus σ_n at high frequency is smaller than that at low frequency. For EF>1, there are more traps close to the gate-oxide surface, the number of traps contributing to the low frequency noise is large, and σ_n at low frequency is smaller than that at high frequency. The slope of the σ_n vs. frequency in the log scale plot is (EF-1)/2.

V. EXPERIMENTAL DATA OBSERVATIONS

The statistical noise behavior of the 90nm CMOS technology was experimentally characterized. A total of 175 devices of two area sizes were selected from the center dies of a wafer to minimize the variation due to different locations in the wafer. The minimum printable transistor size for this 90nm node is W = 0.22 μm and L = 0.1 μm and 90 transistors were measured. The next transistor size is W = 1 μm and L = 0.1 μm and 85 transistors were measured. The gate oxide thickness T_{ox} is 2.8 nm and the supply voltage Vdd is 1.2 V. Flicker noise is measured in the saturation mode from 4 Hz to 102.4 KHz at room temperature at Vds = Vgs = Vdd. The noise spectra for both areas are plotted in Fig. 7. The devices of both areas are considered as small area devices because the majority of the noise exhibits Lorentzian characteristics and the variation is relatively large. There are three interesting observations from the noise data and each observation will be discussed below in detail.
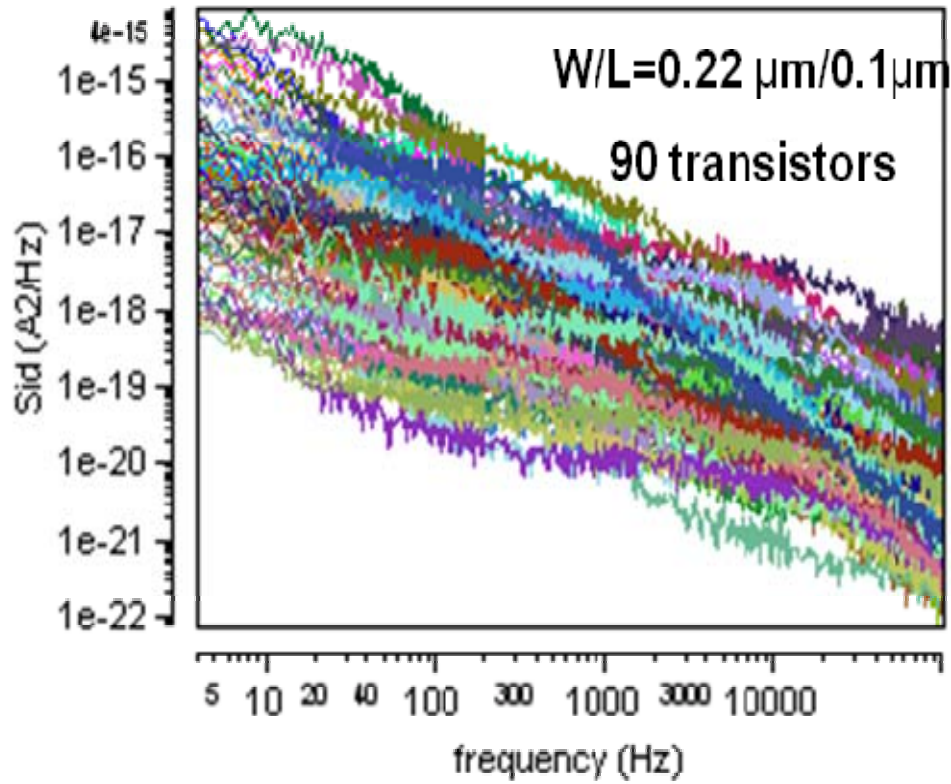
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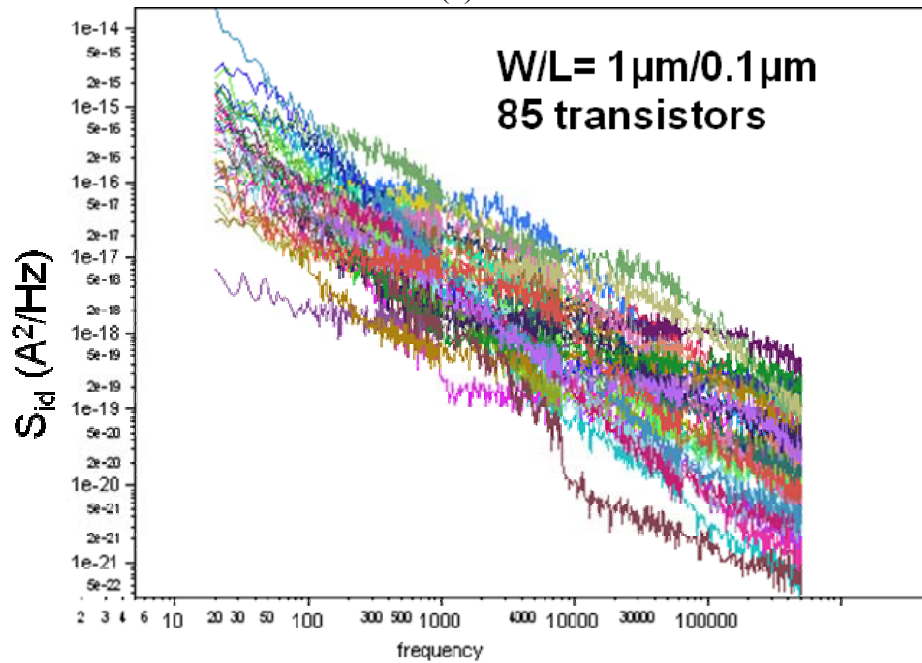
(b)

Figure 7: Flicker noise spectra (a) for all 90 transistors with W/L = 0.22 μm /0.1 μm and (b) for all 85 transistors with W/L = 1 μm /0.1 μm. For devices in both areas, each transistor exhibits Lorentzian characteristic noise.

A. Poisson Statistics Assumption of the Number of Traps, N_{tr}

First observation is that there is no trap-free device in the data set, even in the minimum area devices. If each bend in the Lorentzian noise spectrum at a specific corner frequency represents the presence of a trap, we can estimate the number of traps for each sample device from the noise spectrum.   For example, in Fig. 8, (a) represents a sample device with two traps which have two corner frequencies of $f_1 < 1Hz$ and $f_2 \sim 8000Hz$ whereas (b) presents a sample device with only one trap which has one corner frequency at around 4000Hz.
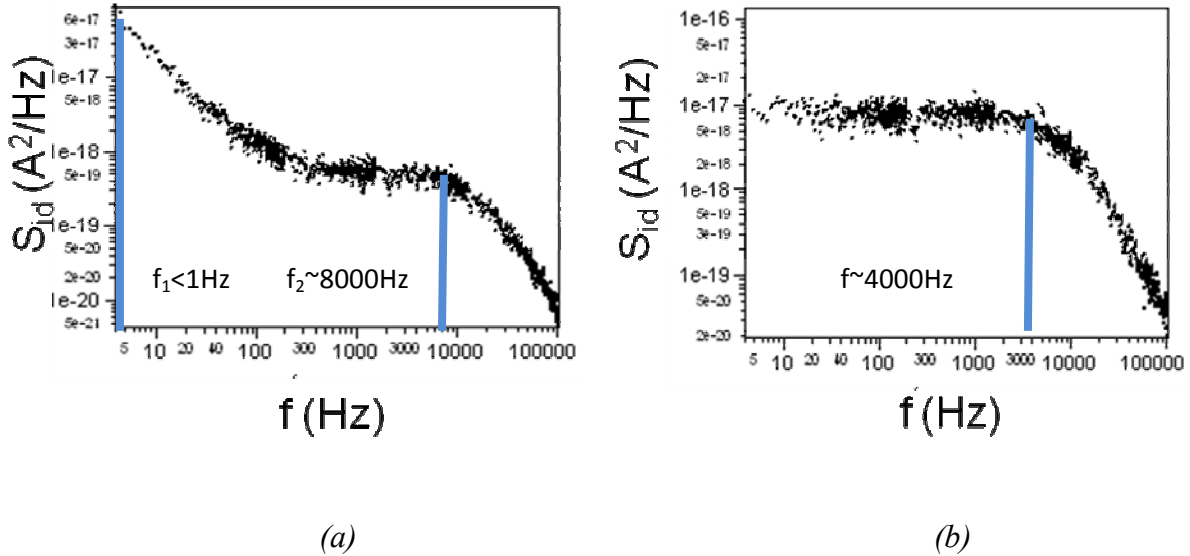

<div align="center">(a)</div>

Figure 8: Examples of Lorentzian spectra for single sample device from the minimum size transistor (W/L = 0.22 μm /0.1 μm). One can extract the number of traps from the spectra. In (a), the device may have 2 traps with two corner frequencies of f1<1 Hz and f2~8000Hz. In (b), the device may have only one trap with one corner frequency f~4000Hz.

When one follows the methodology described in Fig. 8 to estimate the number of traps for all the 90 sample devices from the minimum size area (W = 0.22 μm and L = 0.1 μm), the average number of traps $<N_{tr}>$ is estimated to be 2.6. For $<N_{tr}> = 2.6$, Poisson statistics predicts there will be 7.4% of devices with less than 0.1 traps. Thus, for the total 90 samples, if the

number of traps is a pure Poisson statistics variable, one will observe at least 6 sample devices (90 X 7.4%) that are trap-free, which does not generate flicker noise. Since a trap free device is not observed in the experiment, the assumption of pure Poisson statistics for the number of traps N_{tr} may not be an entirely correct assumption.

One hypothesis that our group propose to explain this observation of the absence of trap free devices is that the mechanism of trap formation may be different between the interior and at the corners of the gate dielectric. The traps formed in the interior of the gate dielectric may be described by the conventional Poisson statistics. However, the four corners of the gate dielectric may have a higher chance to form traps due to its unique geometry. If this is true, a pure Poisson statistic assumption may not be appropriate to describe the number of traps formed at the corners. As the transistor scales down, the interior area of the dielectric shrinks dramatically but the four corners of the rectangular gate will still remain.

B. Single Short Time Constant Assumption

The second interesting observation made from the noise spectra is that there is not a single device that has only one short time constant. The simulated noise spectrum which assumes the probability of having single short time constants shown in Fig. 9 (a) is compared to the experimental noise spectrum data in Fig. 9 (b). The two spectra look very different. Fig. 9 (a) was simulated using the statistical Monte Carlo model with an average trap number $<N_{tr}>$ = 2.6 and EF=1. In the Monte Carlo model, the assumption of single short time constant is a used and some Lorentzian spectra flatten out at a high corner frequency due to this assumption. Comparing Fig. 9 (a) to Fig. 9 (b), the single short time constant assumption predicts much larger variation for low frequency noise.
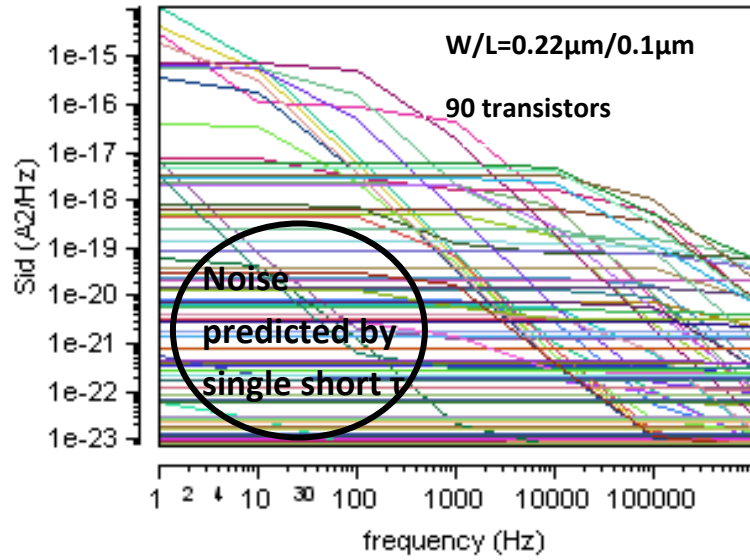
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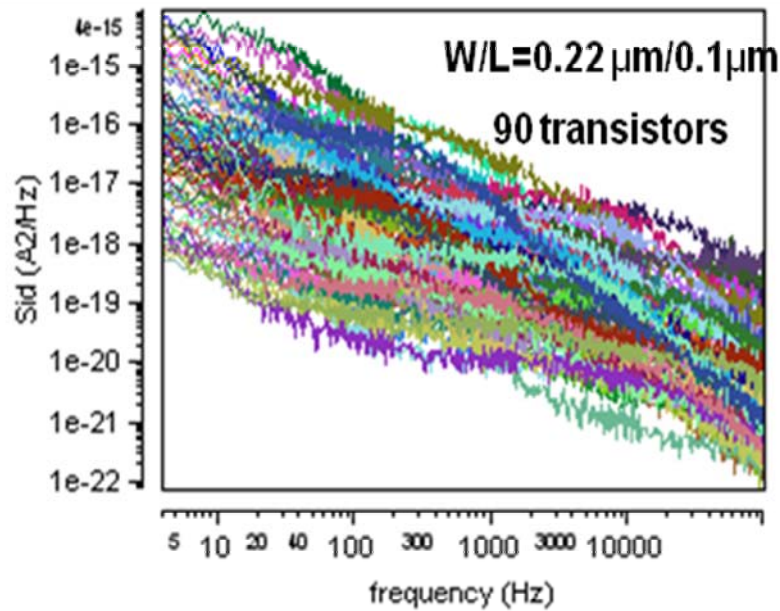
(b)

Figure 9: Comparison between (a) simulated noise spectrum with the single time constant assumption and (a) the experimental noise spectrum. The single time constant assumption predicts large variation for low frequency noise, which was not observed in experimental data.

Based on the conventional assumption of time constant, single short time constant means that there is only one trap in the device and that trap is located very close to the substrate surface. However, in the experimental data, when there is a short time constant (or large corner frequency), it is always associated with a second or third larger time constants (or smaller corner frequencies). As a result, the noise power spectrum in the low frequency range does not have a large variation as expected in Monte Carlo simulation. Since the possibility of having only one trap that is close to the substrate surface exists, we could hypothesize that single trap may be associated with more than one time constant. If there is a possibility that a second electron may get trapped after the trapping of the first electron, a single trap may have more time constants reflecting the additional electron/electrons trapped. In this case, the time constant of the second electron getting trapped will depend on the charge state (+, 0, -) of the trap.

C. *Lognormal Distribution of Flicker Noise at Each Frequency*

The third observation is very crucial in developing the Analytical model. We have discovered that at each frequency the distribution of the noise power follows a lognormal statistics. Lognormal distribution is a single-tailed probability distribution of a random variable whose logarithm is normally distributed. Flicker noise power is a lognormal distribution at each frequency observed from the experimental data, which means that the natural log of noise power is normally distributed. A randomly selected example at frequency f = 13056 Hz from the minimum device size (W/L = 0.22μm/0.1μm) is shown in Fig. 10. In the histogram, when the number of transistors (90 transistors total) is plotted against the natural log of flicker noise power, the distribution is normal with R^2 = 0.97 suggesting a good fit.
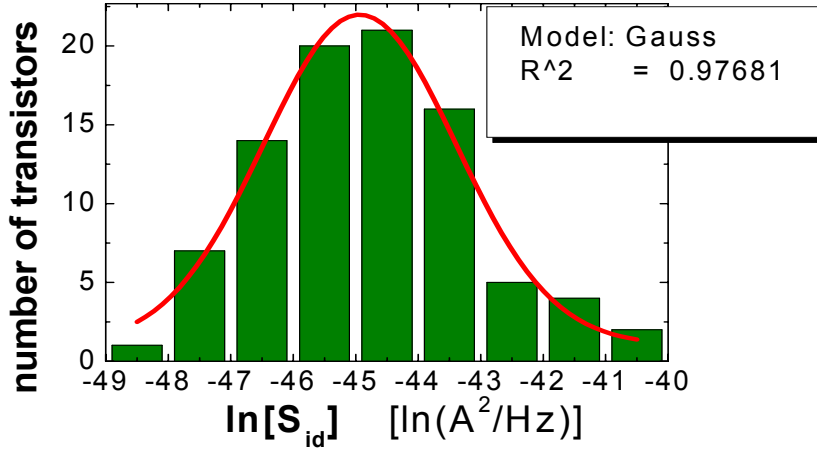
Figure 10: At a randomly selected frequency (f = 13056 Hz), the flicker noise from the 90 transistors with device area W/L = 0.22µm/0.1µm is best fitted by lognormal distribution with R^2= 0.97.

If a random number X is perfectly lognormal distributed, one can obtain the mean μ_{log} and the standard deviation σ_{log} of ln(X) from the mean μ and the standard deviation σ of X. The relationships among μ_{log} , μ ,σ_{log} , and σ are shown in Eq. 23 and Eq.24 [15].

$$\mu_{\log} = \ln(\mu) - \frac{1}{2}\ln(1 + \frac{\sigma^2}{\mu^2}) \tag{23}$$

$$\sigma_{\log} = \sqrt{\ln(\frac{\sigma^2}{\mu^2} + 1)} \tag{24}$$

One can also use a cumulative distribution function (CDF) to describe the accumulated probability distribution of a lognormal random variable. CDF is the probability that the variable takes less than or equal to a specific value [16]. CDF for a lognormal distribution is defined as a

function of μ_{log} and σ_{log} in Eq. 25 [15]. Thus, if one can obtain μ_{log} and σ_{log}, a lognormal CDF plot can be constructed easily.

$$CDF = \frac{1}{2} + \frac{1}{2} erf \left[\frac{\ln(x) - \mu_{log}}{\sigma_{log} \sqrt{2}} \right]$$

(25)

Fig. 11 shows that the CDF of the experimental flicker noise data at a randomly selected frequency is best fitted by lognormal. Lognormal CDF is extremely useful for quickly finding the flicker noise magnitude corresponding to any given percentile. For example, in Fig. 11, from the CDF plot for a device with W/L = 0.22µm/0.1µm and f = 13056 Hz, the median (50th percentile) of the noise distribution corresponds to 3.315e-20 A^2/Hz and 90th percentile corresponds to 3.521e-19 A^2/Hz.
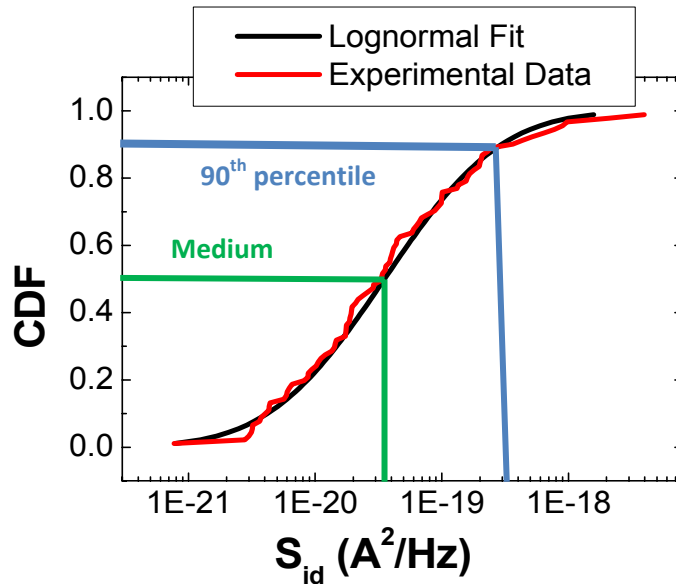

Figure 11: At any randomly selected frequency, the CDF of experimental noise data is best fitted by a lognormal CDF. For the CDF produced by flicker noise from W/L = 0.22µm/0.1µm and f = 13056 Hz, the median (50th percentile) of the noise distribution corresponds to 3.315e-20 A^2/Hz and 90th percentile corresponds to 3.521e-19 A^2/Hz.

The observation of lognormal distribution of noise at each frequency is important. If one can relate the mean $<S_{Id}(f)>$ and standard deviation $\sigma(f)$ of the flicker noise modeled in Section IV to the lognormal statistics parameters μ_{log} and σ_{log} that allow us to construct the lognormal CDF plot, one can predict noise power magnitude at any percentage yield of CDF. The relationship of μ_{log}, σ_{log}, $<S_{Id}(f)>$, and $\sigma(f)$ is proposed in Section VI.

VI. ANALYTICAL MODEL VERIFICATION

The verification of the Analytical model using the experimental data is done in two steps. First, we verified the modeled mean $<S_{Id}(f)>$ by plotting it on a regular noise spectrum double-log plot. It should be a linear 1/f line even though the flicker noise from each individual device sample exhibits Lorentzian characteristics. Second, we verified the modeled standard deviation $\sigma(f)$ by the following process. The new model parameter NOIS is extracted from the minimum size transistor noise data. With the known model parameter NOIS, we can predict the standard deviation for the other larger transistor size. The predicted $\sigma(f)$ using the Analytical model will be compared to the experimentally measured $\sigma(f)$ for model verification.

A. Mean $<S_{Id}(f)>$ Verification

In the Analytical model, $<S_{Id}(f)>$ should be correctly predicted by the current Unified model. Since the Unified model is not a simple expression but involves the use of many model card parameters that must be accurately extracted from IV, CV, and noise data, direct verification of $<S_{Id}(f)>$ using unified model is difficult. An alternative way to verify $<S_{Id}(f)>$ is to examine whether the mean has the 1/f shape as predicted in the unified model in large area device. In Fig. 12, both $<S_{Id}(f)>$ s of the two area transistors have 1/f characteristics with

slopes close to 1 (0.984 for W/L=0.22μm/0.1μm and 0.98 for W/L=1μm/0.1μm, respectively).

$<S_{Id}(f)>$ of W/L=1μm/0.1μm is larger than that of W/L=0.22μm/0.1μm for all frequency

because there are more traps in the larger area of W/L=1μm/0.1μm devices.

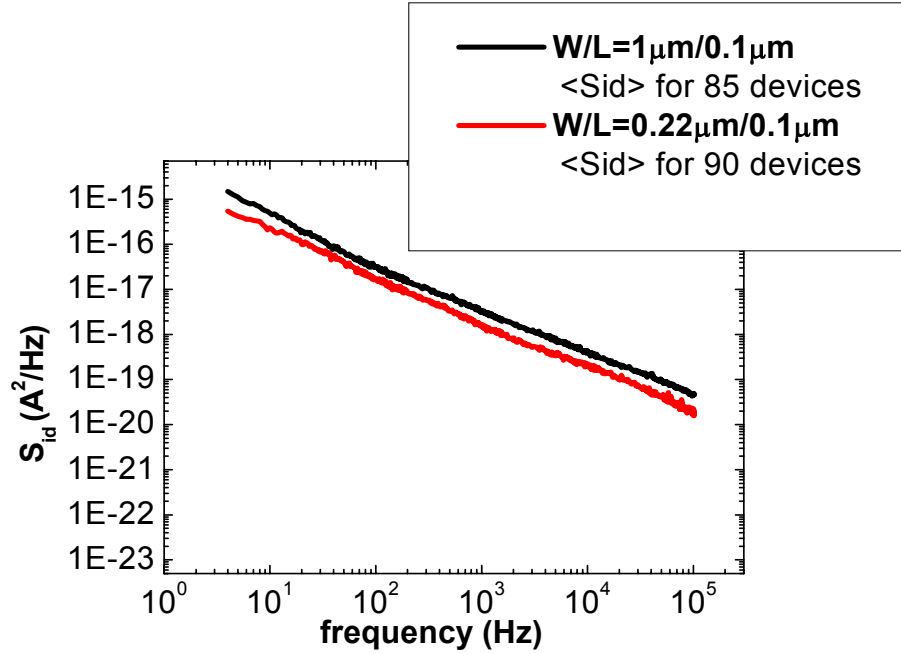Figure 12: The $<S_{Id}(f)>$s of W/L=1μm/0.1μm and W/L=0.22μm/0.1μm show 1/f characteristics. $<S_{Id}(f)>$ of W/L=1μm/0.1μm is larger than that of W/L=0.22μm/0.1μm indicating the presence of more traps in the larger area devices.

B. *Parameter NOIS Extraction*

In order to complete the model, the new parameter NOIS needs to be first extracted from

the minimum area noise data. For the W/L=0.22um/0.1um data set, since we know $<S_{Id}(f)>$ and

σ (f), NOIS can be calculated by plugging in W, L, and EF. Note EF is very close to 1 (0.984),

so the frequency term in Eq. 22 can be approximated to 1. NOIS is calculated to be 3.324e-10

and the model is simplified to Eq. 26.

$$\sigma_n = \frac{\sigma(f)}{<S_{Id}(f)>} = \frac{3.324e-10}{\sqrt{W \times L}} \qquad (26)$$

The normalized standard deviation σ_n vs. frequency is shown in Fig. 13 (a). Because EF is close to 1, dependence of frequency on σ_n is very small and σ_n is close to a constant. The experimental and modeled $<S_{Id}(f)>$s and $\sigma(f)$s are plotted in Fig. 13 (b). The good overlap between the experimental data and the model prediction indicates that the NOIS is extracted correctly.
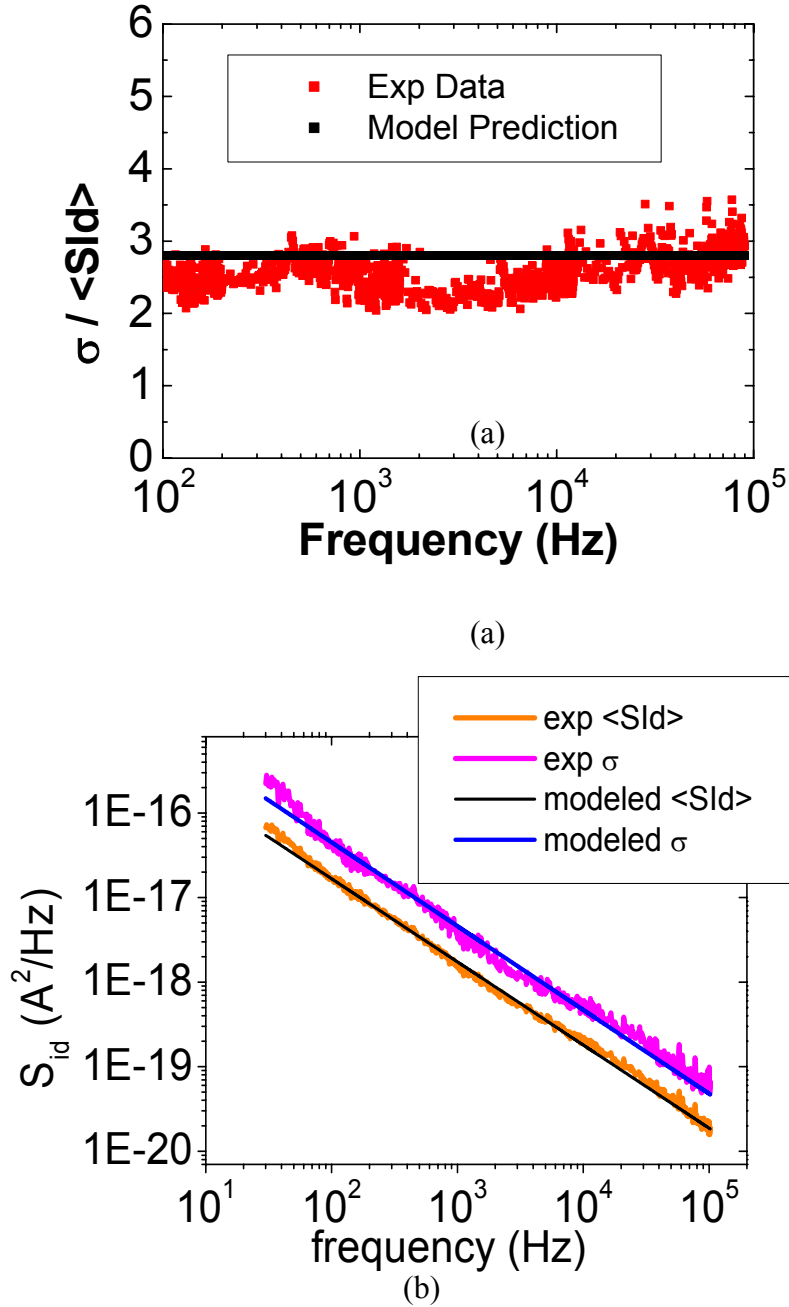

(a)

(b)

Figure 13: W/L=0.22µm/0.1µm (a) modeled σ_n as a constant overlaps with experimental σ_n (b) modeled $\sigma(f)$ overlaps with experimental $\sigma(f)$. Both graphs indicate NOIS is extracted correctly.

Because the flicker noise is best fitted by lognormal distribution at each frequency, we could use $<S_{Id}(f)>$ and $\sigma(f)$ to model the lognormal CDF as well. Although noise is best fitted by lognormal distribution, it is not perfectly lognormal distributed ($R^2 = 1$). Thus, a slight modification is introduced in the equations (Eq. 23 and Eq. 24) to find μ_{log} and σ_{log}. The modification is to multiply $\sigma(f)$ by a constant and the constant is empirically found to be 2.

$$\mu_{log} = \ln(< S_{Id}(f)>) - \frac{1}{2}\ln(1 + \frac{[2\sigma(f)]^2}{< S_{Id}(f)>^2}) \tag{27}$$

$$\sigma_{log} = \sqrt{\ln\left(\frac{[2\sigma(f)]^2}{< S_{Id}(f)>^2} + 1\right)} \tag{28}$$

After the modifications in Eq. 27 and Eq. 28 are introduced, μ_{log} and σ_{log} are calculated and lognormal CDF is modeled using Eq. 25. In Fig. 14, the modeled CDF and the experimental CDF overlap nicely for both low frequency and high frequency noise.
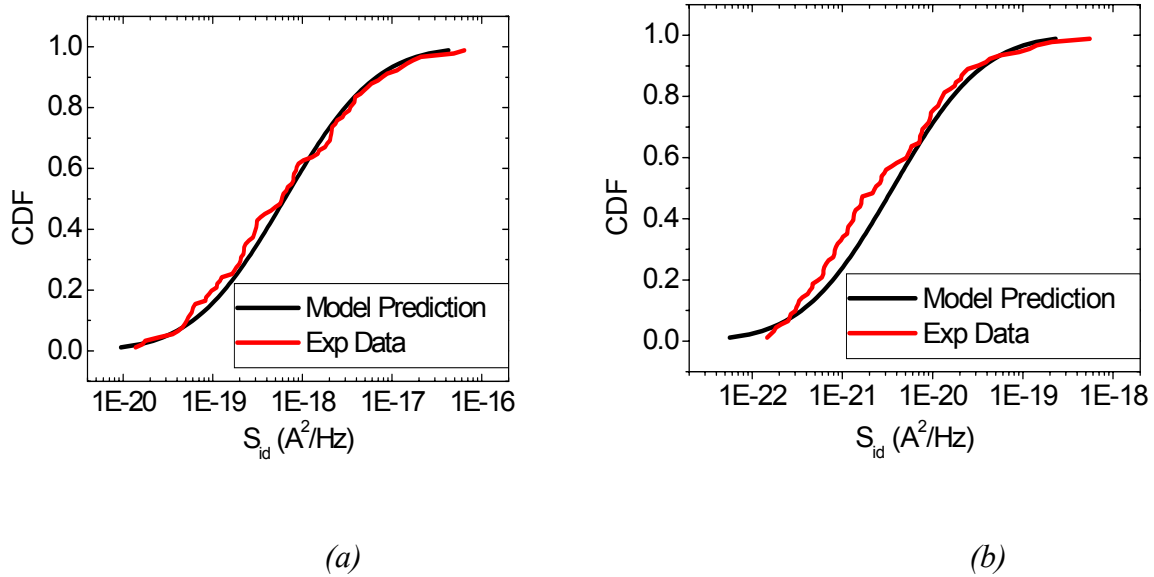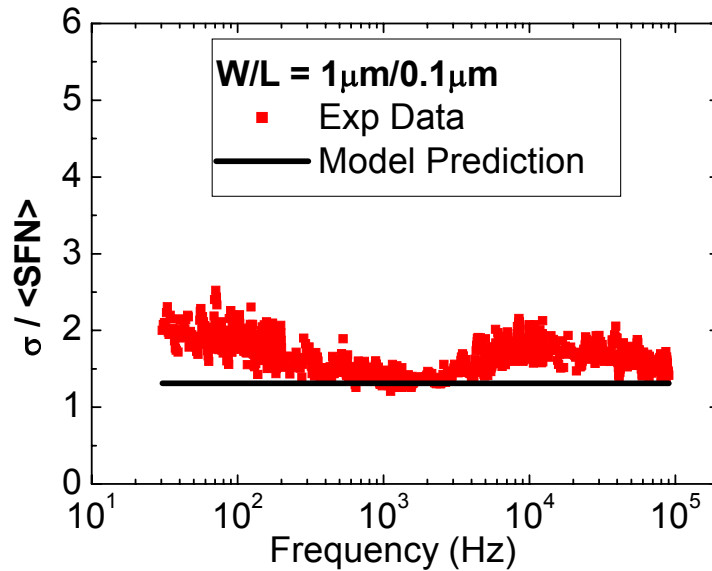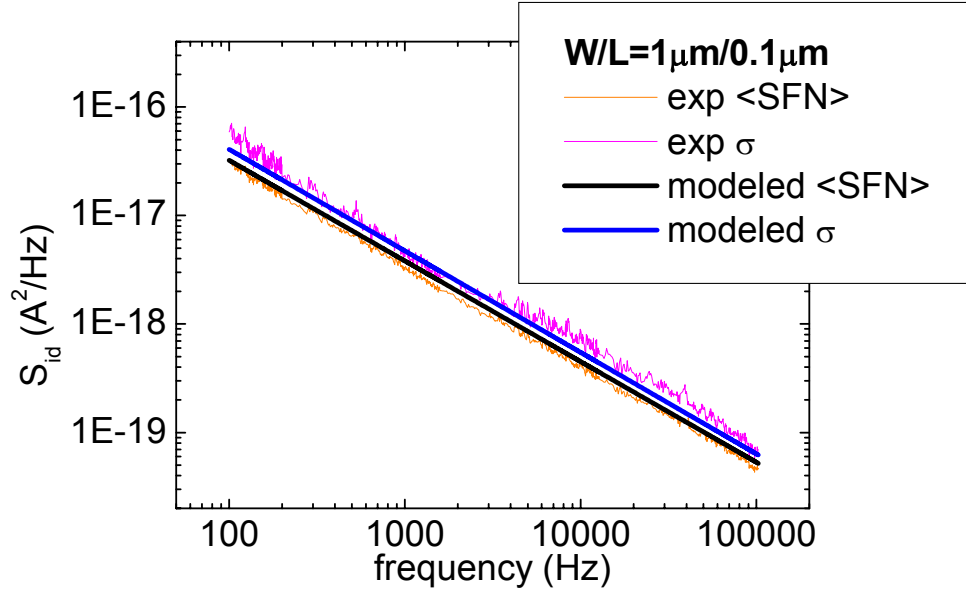

(a)   *(b)*

Figure 14: For W/L=0.22µm/0.1µm, modeled CDF and the experimental CDF overlap for both low frequency and high frequency noise. (a) f = 500Hz (b) f =100096Hz.

C. Standard Deviation σ (f) Verification

Once the model is completed as in Eq. 26, it can be used to predict σ (f) of devices with any area size in that technology. Here, we used the completed model with the extract NOIS from the minimum area (W/L=0.22μm/0.1μm) to predict σ (f) for the larger area device (W/L=1μm/0.1μm). In Fig. 15, assuming $<S_{Id}$ (f)$>$ is modeled correctly by the unified model, σ $_n$ and σ (f) are predicted using the completed Analytical model and compared to the experimental σ_n and σ (f). The σ_n and σ (f) nicely predicted by the Analytical model overlap with the experimental counterparts, which verifies the accuracy of the model.


(a)

(b)

Figure 15: noise spectrum of W/L=1μm/0.1μm (a) model-predicted σ_n as a constant overlaps with experimental σ_n (b) model-predicted σ (f) overlaps with experimental σ (f). Both graphs indicate the Analytical model is accurate in predicting standard deviation.

Using predicted σ (f), one can model CDF as discussed in the previous section. Fig. 16 shows for the larger area (W/L=1μm/0.1μm), the model-predicted CDF and the experimental CDF overlap nicely for both low frequency and high frequency noise.
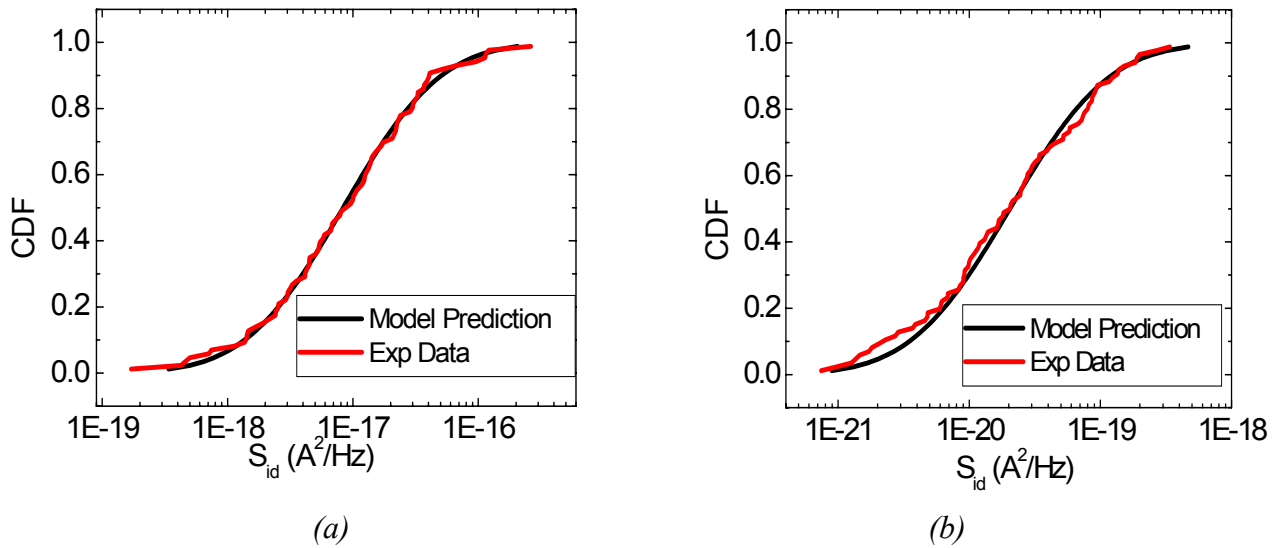
(a)

(b)

Figure 16: For W/L=1μm/0.1μm, model-predicted CDF and the experimental CDF overlap for both low frequency and high frequency noise. (a) f = 147Hz (b) f =100608Hz.

VII. PROPOSED ANALYTICAL MODEL USAGE

A. NOIS Extraction Procedure

In order to extract the new Analytical model parameter NOIS, one needs to initially measure the flicker noise from a statistical sample of small area transistors to get $<S_{Id}(f)>$ and σ (f). The minimum sample size is determined when $<S_{Id}(f)>$ is approaching a linear 1/f shape. As long as $<S_{Id}(f)>$ has the 1/f characteristics, it can be modeled by the current BSIM 4 Unified flicker noise model (UFN). In the first scenario, if the noise simulation from UFN (FNOIMOD=1) agrees with $<S_{Id}(f)>$ as in the theory, NOIS can be extracted directly from Eq. 22. In the second scenario, if $<S_{Id}(f)>$ and the noise simulation from UFN does not agree with each other, then the Unified model noise parameters such as EF, NOIA, NOIB, NOIC need to be re-extracted to well fit $<S_{Id}(f)>$ instead.   The purpose of modeling $<S_{Id}(f)>$ well by UFN is because σ (f) in the Analytical model is very sensitive to the change in $<S_{Id}(f)>$. If $<S_{Id}(f)>$ cannot be accurately modeled by UFN, σ (f) cannot be accurately modeled. NOIS can be extracted when the re-extracted noise parameters can fit $<S_{Id}(f)>$. Fig. 17 summarizes the procedure to exact NOIS in BSIM4.
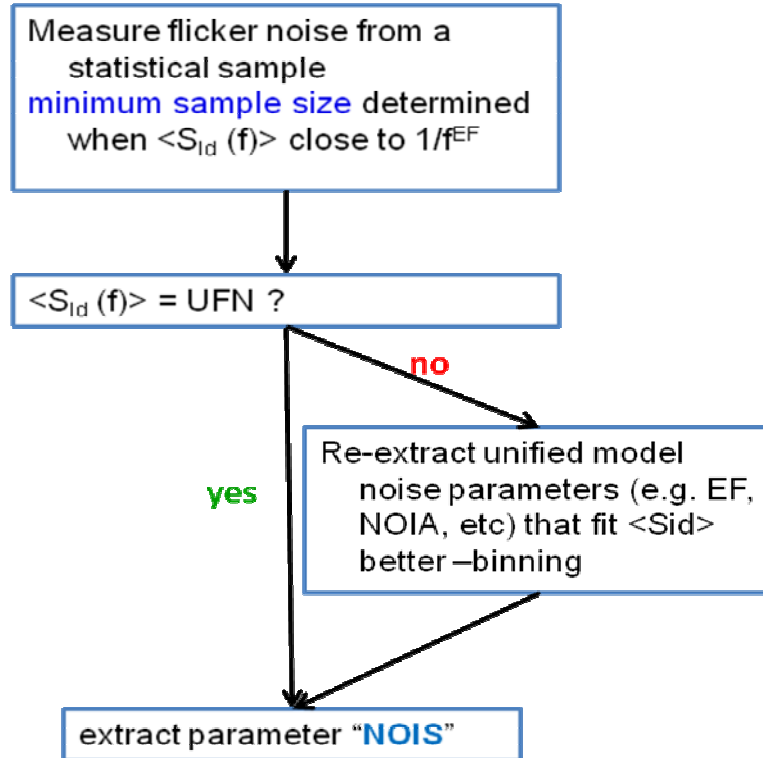
Figure 17: NOIS extraction procedure in BSIM4.

B. *Proposed Analytical Model User Input and Output*

The user input and output for the Analytical model should be simple. In BSIM4, the

Analytical model will be activated by selecting FNOIMOD=X where X indicates the Analytical

model in BSIM. Input parameters will be the frequency (f) and the percentage yield of CDF (%).

BSIM will first calculate $<S_{Id}(f)>$ using the existing flicker noise UFN. With the extracted

NOIS, BSIM then calculates $\sigma(f)$ using the Analytical model. Once $<S_{Id}(f)>$ and $\sigma(f)$ are

obtained, they can be transformed into lognormal mean μ_{log} and standard deviation σ_{log} as in Eq.

27 and 28. μ_{log} and σ_{log} are used to construct the lognormal CDF at the requested frequency f.

The noise magnitude at the requested percentage yield of CDF will be calculated using the

inverse function of CDF ($CDF^{-1}(\%)$). The final output will be $<S_{Id}(f)>$, $\sigma(f)$, and the noise

magnitude at the percentile yield CDF at frequency f. Fig. 18 outlines the input and output of the

analytical flicker noise model in BSIM4.

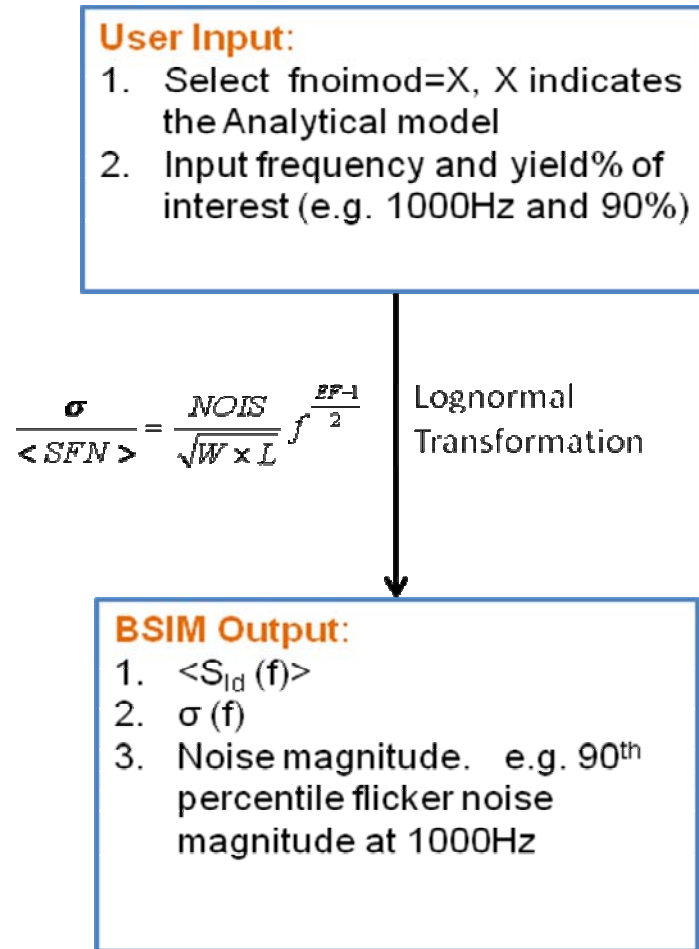$$\frac{\sigma}{<SFN>} = \frac{NOIS}{\sqrt{W \times L}} f^{\frac{EF-1}{2}}$$

Figure 18: Input and output of the Statistical Flicker Noise Analytical model in BSIM4

The Analytical model accurately predicts flicker noise magnitude for a single bulk

MOSFET. Because this model offers detailed statistics for a single device, the potential

application for the model is very specific. In order to use this model, circuit designers will need

to identify the most critical one or two transistors that they are most concerned about noise.

VIII. CONCLUSION

A novel Statistical Flicker Noise Analytical Compact Model for scaled transistor is presented. The model includes an analytical mean and a standard deviation with just one new model parameter. The extraction of the new parameter requires a statistical noise data of at least one small device size. Because the standard deviation is sensitive to the model error of the mean, it is advisable to model the mean well. The model can predict noise magnitude at given frequencies and yield percentiles in CDF, which will serve as a valuable guide for circuit designers in their analog and RF design.

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        < http://en.wikipedia.org/wiki/Cumulative_distribution_function >.