Downconverting Sigma-Delta A/D Converter for a Reconfigurable RF Receiver

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Downconverting Sigma-Delta A/D Converter for a Reconfigurable RF Receiver

by

Renaldi Winoto

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Committee in charge:

Professor Borivoje Nikolić, Chair
Professor Ali Niknejad
Professor Daniel Tataru

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University of California, Berkeley

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by

Renaldi Winoto

Abstract

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The proliferation of a multitude of wireless standards as well as the interest in cognitive radios have resulted in the need for a highly reconfigurable radio-frequency (RF) receivers. Reconfigurability in an RF receiver has to be obtained with a negligible degradation in circuit performance, power consumption and silicon area. Digital signal processing offers a degree of flexibility that is perhaps unmatched by analog circuits. Nevertheless, a strategy of processing an RF signal entirely in the digital domain would place an incredible burden in the analog-to-digital converter circuits.

A novel receiver architecture is proposed in this work, where a high performance analog-to-digital converter is tightly integrated within the RF circuit. In the proposed architecture, a signal at a radio frequency is directly converted to digital domain using a down-converting sigma-delta ($\Sigma\Delta$) modulator. A $\Sigma\Delta$ A/D converter is well-suited for an RF receiver. First, it minimizes aliasing due to the high sampling-rate. Second, it enables high-resolution conversion of the desired signal with low-resolution components. A direct-conversion to DC architecture greatly simplifies frequency planning of this flexible receiver, as it eliminates problems related to image frequency bands.

A circuit prototype demonstrating the proposed concept has been designed, fabricated and measured. The test-chip prototype is able to maintain an SNR of greater than +59dB

across a 4-MHz bandwidth with a programmable center frequency of 400MHz to 1.7GHz. As illustrated in this work, the tight integration of the $\Sigma\Delta$ modulator within the RF receiver also enables the receiver to achieve a very good linearity. An IIP3 of +19dBm and an out-of-band 3-dB desensitization level of +6dBm is measured in this test-chip prototype.

Professor Borivoje Nikolić
Dissertation Committee Chair

To my dad, for teaching me to be curious.

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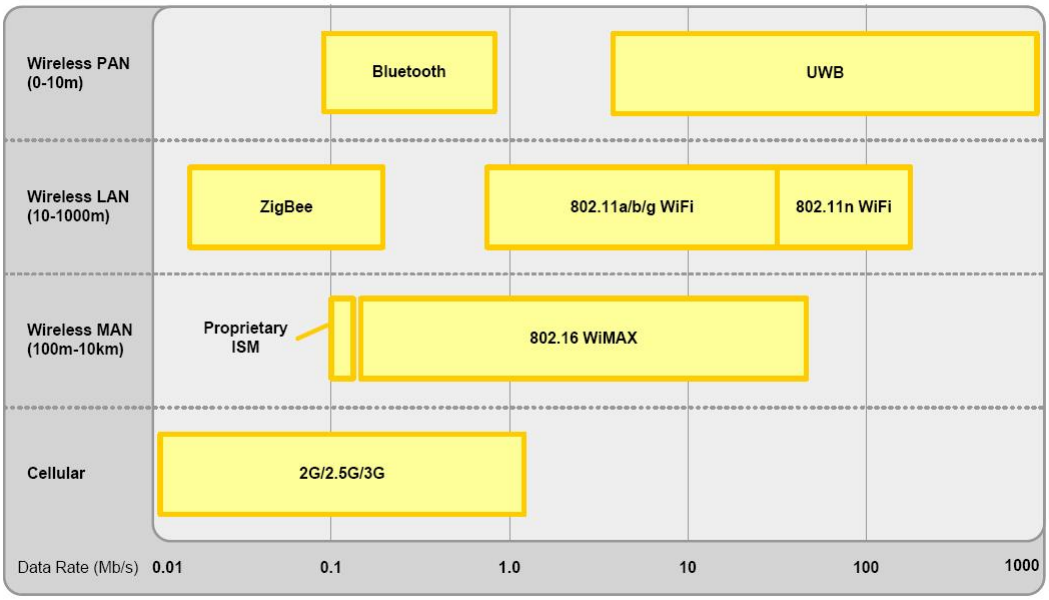
Chapter 1

Introduction

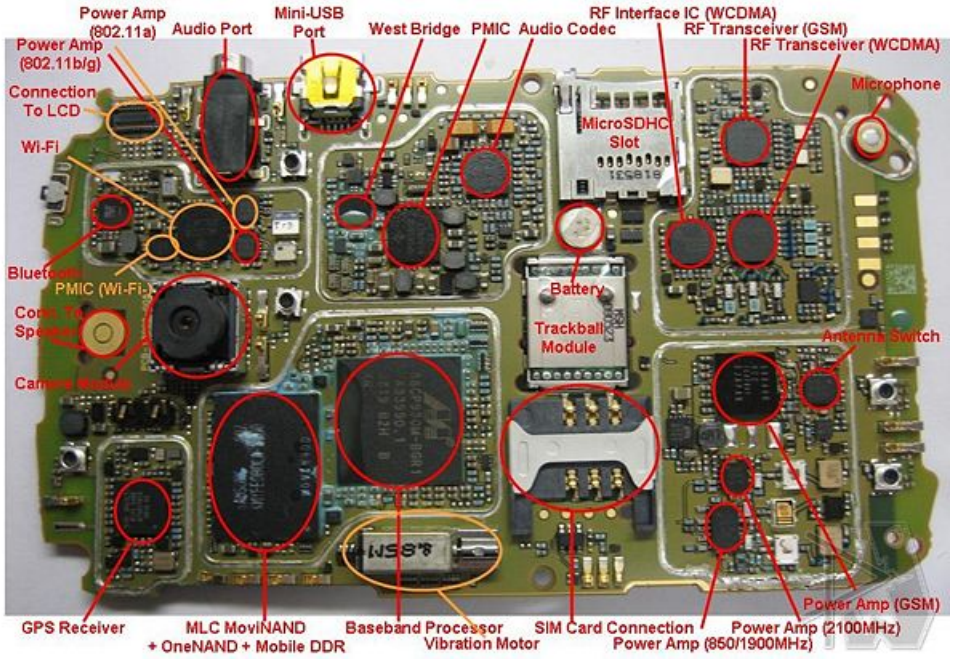
The past decade has witnessed an immense growth of wireless connectivity. This growth has been driven by the continuous reduction of the cost of the underlying hardware as well as the seemingly unending desire to untether every electronic device. In order to tailor to a specific usage scenario, a multitude of wireless standards have arisen, each categorized by the data rate and the range of communications (Fig. 1.1(a)). Each of these communication standards is optimized for the lowest power and lowest cost.

Supporting this multitude of wireless standards has become a significant design challenge in current and future wireless devices. A high-end cellular handset today supports more than five different wireless standards, operating at more than ten frequency bands. Dedicated transceiver ICs along with the necessary peripheral components are typically needed in order to support each wireless standards. Despite the apparent increase in complexity (Fig. 1.1(b)), the continuous cost reduction afforded by the continuous scaling of CMOS technology will only accelerate the demand for these multi-standard capable wireless devices in the future.

Furthermore, looking towards the future, there is a push for a more flexible spectrum allocation. There is a significant amount of allocated spectrum that is poorly utilized [57]. At the same time, the limited spectrum that is unallocated is auctioned off for a very high price. A flexible spectrum allocation holds the promise of a much more efficient, and



(a) Comparison of wireless technologies [4]



(b) PCB of a high-end cellular telephone [7]

Figure 1.1. Cellular telephone supporting multiple wireless standards

therefore cost-effective use of the radio-frequency spectrum. This new paradigm would require RF transmitters and receivers that are sufficiently flexible to communicate in any available frequency band. This is in contrast with contemporary wireless communication schemes, where the communication occurs in limited and very well-defined frequency bands.

For the two reasons mentioned above, a reconfigurable transceiver is desired. The goal is to have a single, but flexible, signal-processing path in order to support all current and future wireless standards. This technology would streamline the design of multi-standard wireless devices as well as enable the deployment and adoption of a flexible spectrum allocation scheme.

This work would particularly be concerned with the development of a highly reconfigurable RF receiver. The focus would be on the 0-2.4-GHz frequency-range where most of today wireless communication standard reside.

Flexibility and reconfigurability in an RF receiver have to be obtained with a negligible decrease in the circuit performance and a minimum increase in power consumption or silicon area. Digital signal processing offers a degree of flexibility that is perhaps unmatched by analog circuits. Nevertheless, a strategy of processing an RF signal entirely in the digital domain would place an incredible burden in the analog-to-digital converter circuits. Since an RF signal is continuous time and continuous amplitude in nature, an analog-to-digital converter is needed in order to translate it to a digital representation.

A receiver architecture is proposed in this work, where a high performance analog-to-digital converter is tightly integrated with circuitry that is usually categorized as an RF circuit. In the proposed architecture, a signal at a radio frequency is directly converted to digital domain using a down-converting sigma-delta ($\Sigma\Delta$) modulator. A $\Sigma\Delta$ A/D converter is well-suited for an RF receiver; it minimizes aliasing due to the high sampling-rate and it has a high dynamic-range in the frequency band of interest. Final signal selection is performed in the digital domain, where the signal bandwidth can be easily adjusted through a change of digital filter coefficients. A direct-conversion to DC receiver architecture greatly

simplifies frequency planning of this flexible receiver, as it eliminates problems related to image frequency bands.

A circuit prototype demonstrating the proposed concept has been designed, fabricated and measured. The test-chip prototype is able to maintain an SNR of greater than +59dB across a 4-MHz bandwidth with a programmable center frequency spanning from 400MHz to 1.7GHz. As will be illustrated in this work, the tight integration of a $\Sigma\Delta$ modulator within an RF receiver also enables the receiver to achieve a very good linearity performance. An IIP3 of +19dBm and an out-of-band 3-dB desensitization level of +6dBm is measured in this test-chip prototype.

1.1 Related Work

There are three notable examples of reconfigurable, or software-defined, RF receivers (SDR) [29, 10, 80]. All three use a similar architecture, where a single-conversion mixer is followed by a high-order low-pass filter prior to A/D conversion. Unlike the other two receivers, the one by UCLA [10] contains a passive, discrete-time low-pass filter.

Passive switched-capacitor filter is an old concept that has gained renewed interest, especially for use as a baseband filter in an RF receiver [65, 62, 10, 47]. This technique enables precise control of the filter's critical frequencies, without the stringent amplifier settling-time requirement associated with an active switched-capacitor filter. Furthermore, an all-zero FIR filter, a type of filter that is suitable for an anti-aliasing filter needed in an RF receiver, can be easily implemented using this technique [66]. For example in [65], a simple passive switched-capacitor moving-average filter is used as an anti-aliasing filter prior to sample-rate downconversion in a baseband filter in a Bluetooth receiver.

The resurgence of interest for passive switched-capacitor filters in RF receivers can be partly attributed to the use of a sampling-mixer or charge-sampling circuit. A sampling mixer eliminates the need for a power-hungry sample-and-hold circuit that is needed prior to any discrete-time system. The concept of sampling mixer was first introduced by Yuan

[116]. Variations of this concept is used in Texas Instruments' DRP receivers [65, 62], the UCLA software-defined receiver [10] and several other published circuits [40, 41].

In this work, an RF signal is directly sampled at a radio-frequency using a sampling mixer. The output of the sampler is then digitized at the same frequency using a high-speed $\Sigma\Delta$ modulator. In this manner, much of the signal processing can be performed in the digital domain, where flexibility can be more easily obtained. For example, a change of filter bandwidth can be accomplished simply by loading a different set of filter coefficients.

It has been stipulated that a 'true' software-defined radio would require a high-resolution, high-speed A/D converter [60]. A high sampling rate is necessary in order to avoid undesired aliasing of blockers as well as to avoid the problem of noise folding that is prevalent in subsampling receiver architecture [39, 83, 53]. A high resolution conversion is necessary in order to maintain an acceptable SNR for successful demodulation of the desired signal in the presence of large blocker signals. The problem with this approach is that such a high-speed, high-resolution A/D converter is not practically realizable [95].

We circumvent this problem by enclosing a high-speed, but low-resolution, A/D converter inside a $\Sigma\Delta$ modulator loop. It is important to recognize that an RF signal has a property that is in some ways compatible to an oversampling $\Sigma\Delta$ A/D converter: the bandwidth of the RF signal is relatively narrow when compared to its center frequency. Sampling the RF signal at a radio frequency would minimize aliasing and undesired folding. However, a high dynamic-range conversion is only needed in a narrow bandwidth relative to the center frequency; it is not necessary to maintain the high dynamic range across all frequencies.

Downconverting $\Sigma\Delta$ A/D converters have been published previously [14, 103, 70, 17]. The work of Namdar [70] and Tao [103] have a mixer that is enclosed within the $\Sigma\Delta$ modulator loop. However, the two circuits have limited bandwidths of 40KHz and 200kHz respectively, and center frequencies of less than 400MHz. The other two circuits by Breems [14] and Chen [17] actually consist of a mixer followed by a $\Sigma\Delta$ A/D converter. As will be seen in chapter 3, putting a mixer inside the $\Sigma\Delta$ loop has the advantage that the mixer switches only processes the error signal which is much smaller than the desired signal. This

subtle difference can result in higher linearity due to reduced signal range in the mixer switches.

1.2 Thesis Organization

Chapter 2 of this dissertation presents an in-depth overview of the problem to be addressed by this dissertation. A set of system requirements is derived, a survey of state-of-art solutions is presented and several practical performance limitation is analyzed.

Chapter 3 of this dissertation is concerned with the system design aspect of the proposed architecture. The $\Sigma\Delta$ receiver architecture is introduced. All pertinent analysis is presented. The chapter ends with a derivation and selection of important circuit parameters for implementation.

Chapter 4 of this dissertation discusses the circuit implementation of the $\Sigma\Delta$ receiver. Detailed descriptions of the important circuit blocks are discussed. A novel gated-diode preamplifier circuit is presented, along with the pertinent analysis. The chapter concludes with a presentation of measurement results from the test chip.

Chapter 5 of this dissertation summarizes the important contributions of this work.

Chapter 2

Radio-Frequency Receiver Design

This section provides a brief introduction to RF receiver design. In particular, derivation of an A/D converter specification for an RF receiver is described in detail. A brief introduction to $\Sigma\Delta$ A/D converter and its relevance to an RF receiver is presented. Specifications for a reconfigurable RF receiver is developed based on a survey of requirements of today's wireless standards. A survey of state-of-art integrated circuit solutions is presented. An effort is made to predict the practical performance limitation of an RF receiver.

2.1 RF Receiver Design: A Mixed-Signal Perspective

A wireless communication system differs greatly from its wired counterpart because of the lack of implied control over the type, strength and frequency location of signals that are present in the wireless channel. As a result, RF receivers have to be designed with a much larger tolerance to accommodate the unknown.

A worst-case scenario is depicted in figure 2.1, which is commonly referred to the near-far problem. In this scenario, a far away base-station wishes to send a packet of information through the wireless medium. The radio signal is attenuated as it propagates through the medium. When the radio signal reaches the handset, its power level has experienced significant attenuation. On the other hand, other transmitters are present in the surrounding

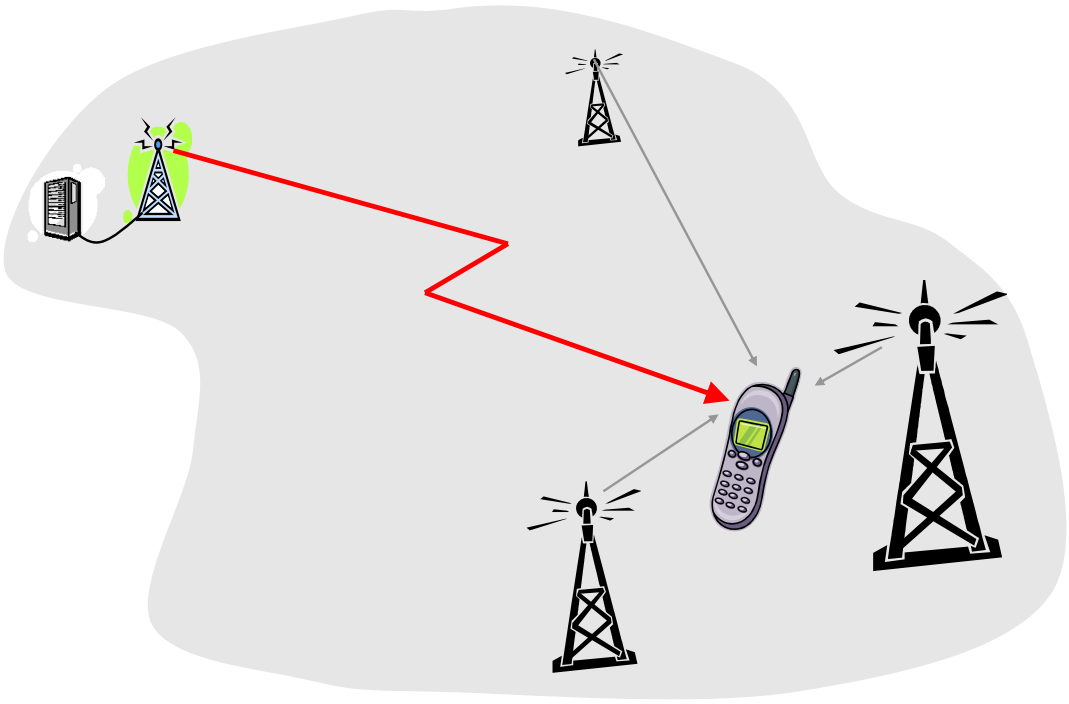


Figure 2.1. Near-far problem.

environment. Although these transmitters operate at different frequencies compared to the desired signal, they may be at a closer proximity when compared to the desired base station. As a result the power levels of these so-called blocker signals can be orders of magnitude higher than that of the desired signal. The RF receiver has to be sufficiently sensitive in order to be able to demodulate the weak desired signal and it has to be able to do so in the presence of strong undesired blocker signals.

In order for the radio receiver to correctly demodulate the received radio signal, a certain signal SNR, SNR_{min}, has to be maintained. This SNR is typically in the range of 5-20dB, depending on the wireless standard. The signal power incident at the receiver is determined by: (1) the transmitted power, and (2) the nature of the wireless medium, namely the communication distance and the presence of a line-of-sight path. On the other hand, noise at the RF receiver originates from two sources: (1) thermal noise incident to the receiver antenna and (2) the RF receiver circuit's own noise. Out of all the four factors determining the received signal SNR, the transmitter power and thermal noise incident at

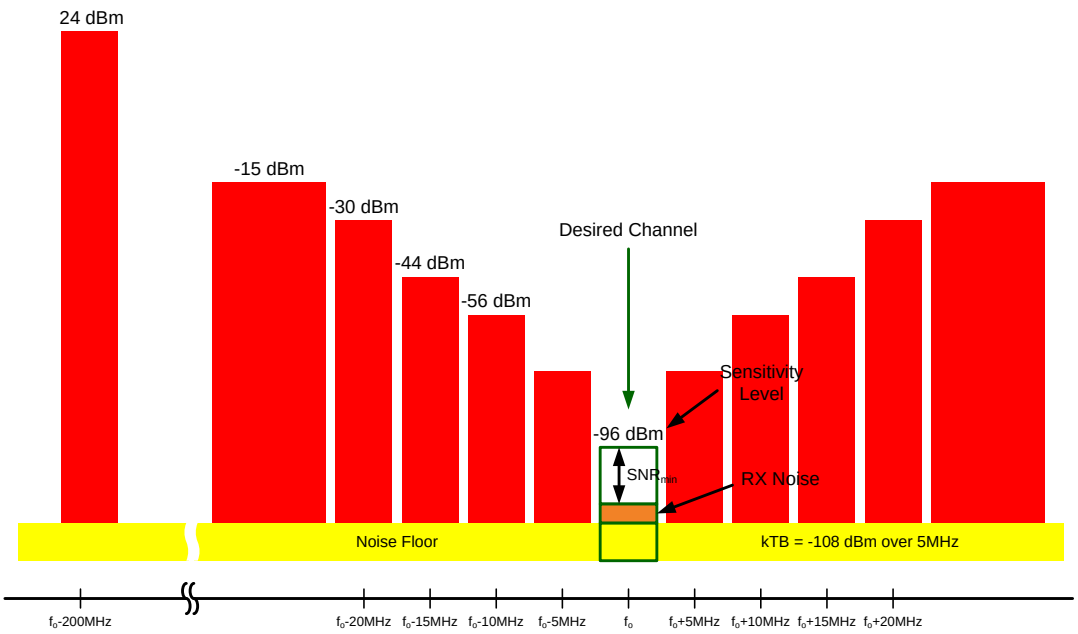


Figure 2.2. Blocking mask of a UMTS standard.

the antenna are not free variables. The remaining two variables are communication distance and the RF receiver's own circuit noise. For a given SNR_{min}, a lower circuit noise would make the receiver more sensitive, and therefore able to communicate over a longer distance. This is often desired because it can result in a better spectrum usage and more cost-efficient infrastructure deployment. For a particular RF receiver, the minimum signal power incident at the antenna that could result in correct demodulation is called the RF receiver *sensitivity level*.

The implication of the near-far problem to the resulting specifications of an RF receiver is best illustrated using a figure called a blocking mask (Fig. 2.2). In this representation, the desired signal is shown at the center of the plot and at its sensitivity level. The maximum power levels for signals at adjacent frequencies to the desired signal is also displayed. Other significant blocking signals at some large offset frequencies might also be displayed in this representation. The maximum power levels of adjacent frequencies can be set by either the wireless standard or by government regulations.

The blocking mask shown in figure 2.2 is taken from the UMTS standard. In this stan-

dard, each channel has a 3.84MHz bandwidth, with a 5-MHz channel-to-channel spacing. The standard dictates that the receiver sensitivity level has to be at least -96dBm. The closest four adjacent channels have maximum power levels that are set by the standard. Because the UMTS standard is a frequency-duplex system, it has to be able to receive while simultaneously transmitting signal back to the base station. For this reason, the largest blocker for the UMTS RF receiver is actually its own RF transmitter, which operates at a frequency offset of 200MHz from the receiver.

The ensuing discussion, along with the numerical example from the UMTS standard underlines the challenge of designing a radio-frequency receiver. A radio-frequency receiver has to maintain a very low noise level in order to meet the sensitivity requirements. However, there are blocking signals present in the environment; some of which can be 100dB larger than the desired signal. Therefore, the challenge in the design of an RF receiver is a challenge of *dynamic range*; how to maintain a low noise floor while at the same time having a sufficient full-scale range to avoid saturation due to the presence of very large signals at nearby frequencies.

All modern wireless standards employs complex modulation scheme in order to communicate more bits for a given signal bandwidth (spectral efficiency). Consequently, an equally complex demodulator is necessary in order to retrieve the pertinent information. The drive for spectrum efficiency is somewhat symbiotic with improvements in semiconductor technology (e.g. Moore's law), where, inexpensive, power-efficient digital signal processing capability is abundantly available. As a result, all modern RF receiver consists of a partition of analog and digital signal processing with an A/D converter in between the two domain[1].

In order to explore the optimal strategy for partitioning the analog and digital signal processing, it is appropriate to review the type of signal operations that are necessary in an RF receiver. A popular RF receiver architecture, commonly referred to a direct-conversion receiver architecture, is shown in figure 2.3. This architecture consists of a single

[1]Unless specified otherwise, the term RF receiver in this dissertation specifically refers to the analog portion of the signal processing path.

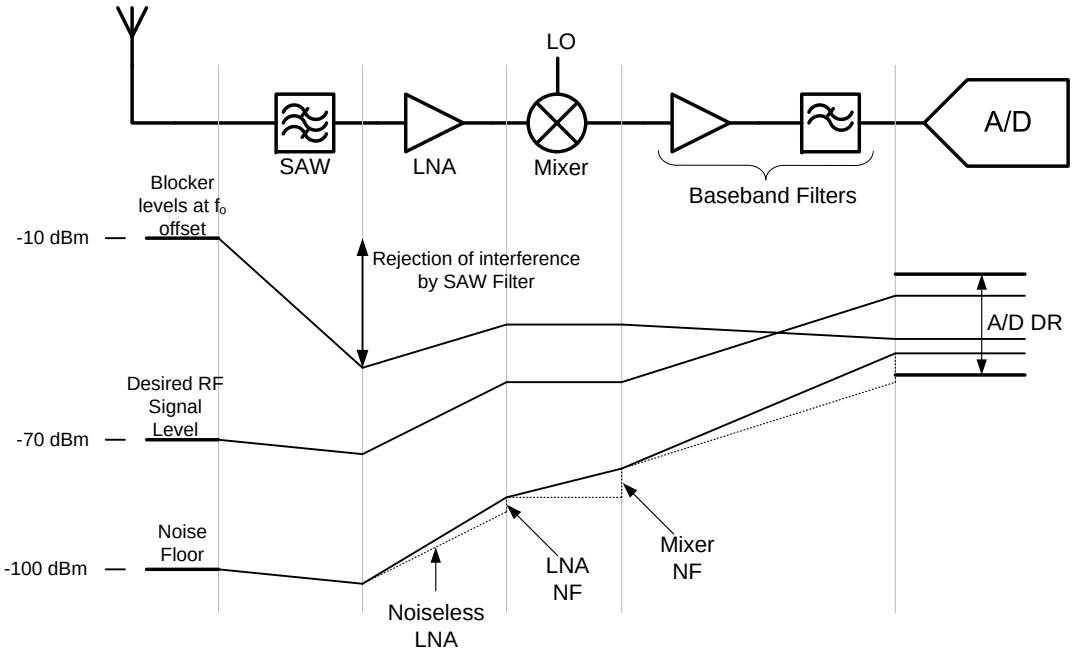


Figure 2.3. A direct-conversion receiver.

down-conversion mixer which translates the radio frequency signal down to DC or to a low frequency. Filtering can occur prior, after or both prior and after mixing. In the same figure, the amplitude of the signal of interest, the largest blocking signals and the noise floor level are also shown. Noise power are integrated over the bandwidth of interest, and it comprises of noise originating from preceding blocks as well as noise arising from the current block.

In many respect, modern RF receiver can be considered simply as a circuit to *pre-process* or *pre-condition* radio signals for A/D conversion [8]. A/D converter dynamic-range and sampling-rate limitations dictate the amount of signal processing, in particular the amount of filtering, that needs to occur in the analog domain. Since most A/D converter operates around DC, a mixer is needed to translate the signal from RF to baseband[2]. Recall that a sampling operation in an A/D converter would create aliasing, where signals spaced at integer multiples of the sampling-rate would be frequency-translated to overlap with each

[2]A class of subsampling RF receiver that relies on aliasing to demodulate an RF signal has been previously studied [39, 83, 53]. This type of receivers usually has a higher noise figure due to the problem of noise folding.

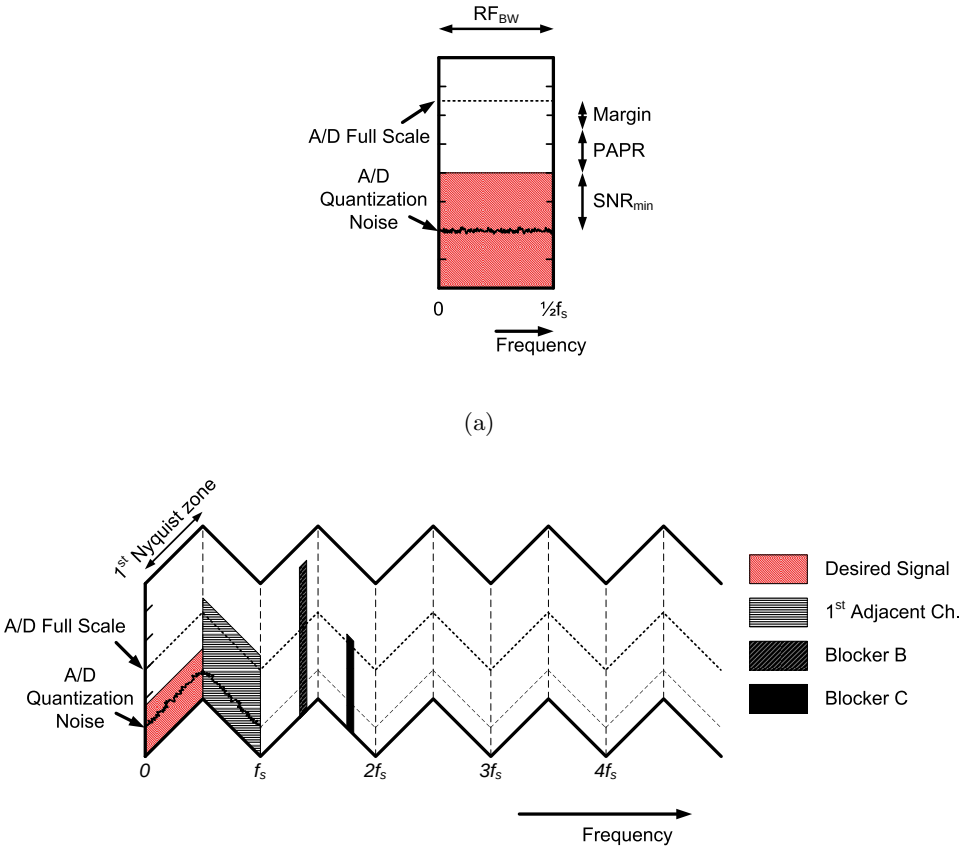


Figure 2.4. A/D converter specification: (a) minimum requirements, (b) signal folding due to sampling.

other. Proper anti-aliasing filters have to be designed such that undesired signal aliases are sufficiently attenuated prior to A/D conversion. Sufficient attenuation in this context is defined to be the point where the cumulative power of the undesired aliases is less than the quantization noise floor of the A/D.

In order to derive an A/D converter specification, one could begin by asking the question of what is the *minmum* necessary requirements for an A/D converter. There are only two important parameters in an A/D converter: sampling rate and resolution [108]. The minimum sampling rate necessary is set by Nyquist theorem [78]; sampling the signal at a rate of twice the signal bandwidth should be sufficient in order to digitize the information contained within the radio signal. On the other hand, the minimum resolution for the A/D

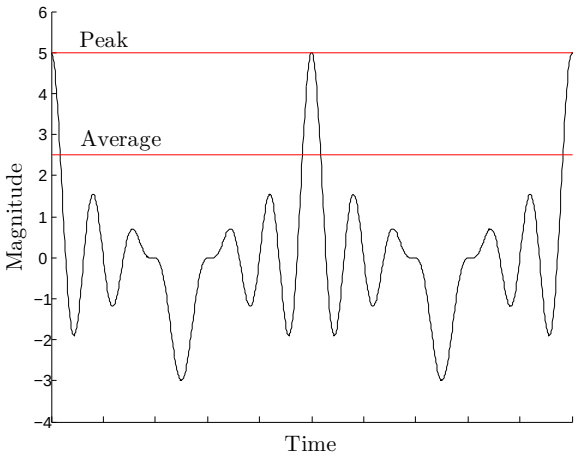


Figure 2.5. Illustration of peak-to-average power ratio problem.

converter is simply:

$$Minimum\ Resolution = SNR_{min} + PAPR \tag{2.1}$$

Since SNR_{min} relates to the *average* signal-to-noise ratio, a certain margin has to be allocated in order to accommodate the *maximum* RF signal level without saturating the A/D converter. This margin amounts to the peak-to-average power ratio (PAPR) of the RF signal (figure 2.5). Signals with large PAPR is often associated with complex, spectrally-efficient modulation schemes. For example, in orthogonal frequency division multiplexing (OFDM) modulation, N sinusoids or subcarriers are used to encode the information [105]. While the signal power of the N tones add in a root-mean-square manner ($O(\sqrt{N})$), the signal maximum is simply a result of the superposition of the N tones ($O(N)$). This results in an increasing PAPR as N, or the number of subcarriers, is increased.

One strategy for RF receiver design is to use an A/D converter with the minimum specifications set above. For this strategy to succeed, the RF signal has to be isolated from any other signals. After filtering, the total power of all other undesired signals has to be to be smaller than the desired signal by at least a factor of SNR_{min}. In this manner, the residuals of the undesired signal would be indistinguishable from the quantization noise floor upon folding due to the sampling operation. This strategy puts a demanding requirement on the baseband filters as it would necessitate a very selective filter. For example, the first

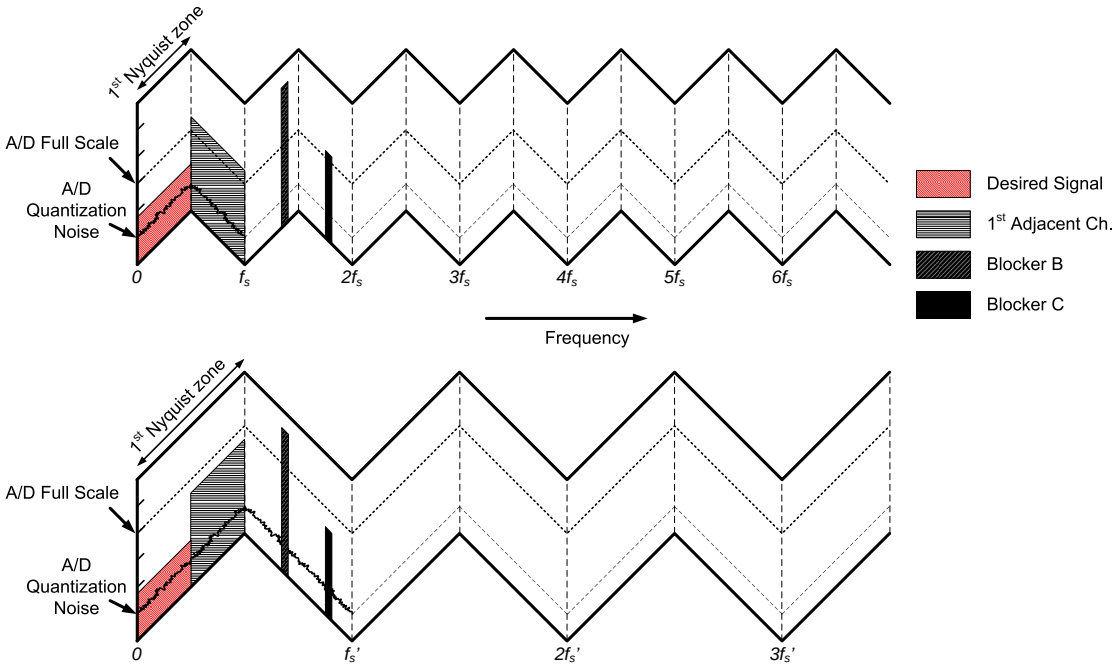


Figure 2.6. Doubling A/D sampling-rate to reduce aliasing.

adjacent channel, which could be only tens of kHz away needs to be significantly attenuated prior to A/D conversion. As a result this strategy would result in a high power consumption for the baseband filters.

A different strategy might be taken, where both the sampling-rate and the resolution of the A/D converter is increased. For example, if the sampling-rate of the A/D is doubled, then the first-adjacent-channel signal would not be aliased down to overlap with the desired signal (figure 2.6). Since the first-adjacent channel is at a very small frequency offset with respect to the desired signal, this strategy would significantly relax the filtering requirement prior to the A/D converter and therefore reduce the power consumption of the filter circuits. However, now the resolution of the A/D has to be increased; sufficient margin has to be allocated in order to accommodate the maximum power level of the first-adjacent signal. Whereas the baseband filter requirements are relaxed, a faster, higher resolution and higher power A/D converter is necessary with this strategy.

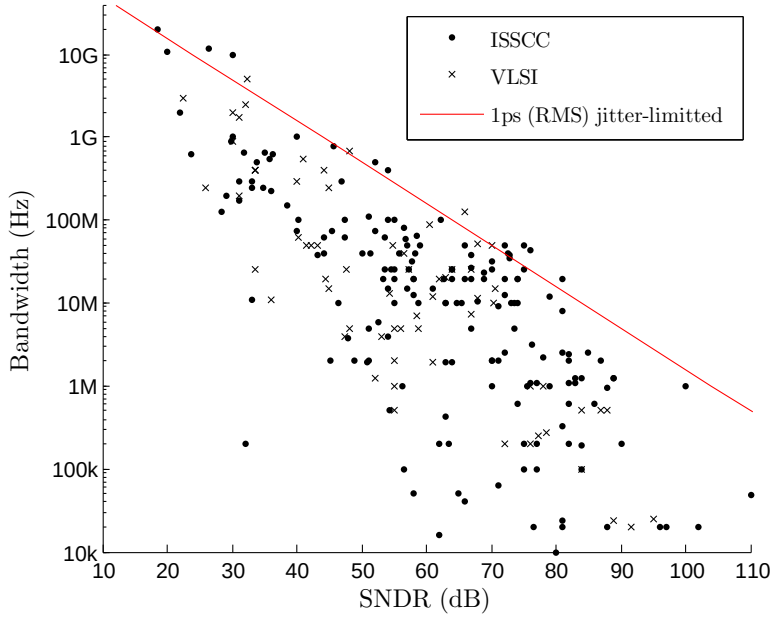
In the end the partition of analog and digital signal processing or the placement of an A/D converter is an optimization problem in power consumption. On one end of the

spectrum, an all-digital radio can be proposed where a minimum amount of filtering occurs prior to a high sampling-rate, high dynamic-range A/D conversion. Signal processing in the digital domain has the added advantages of: (1) it can be easily made programmable and (2) it can be potentially more power efficient, especially in an advanced CMOS process optimized for low-power digital operations. However, the A/D converter needed for such an architecture would consume a lot of power. On the other end of the spectrum, all filtering can be performed in the analog domain, and a power-efficient A/D converter with a Nyquist rate equal to the channel bandwidth can be used. The optimal solution would be somewhere in between these two extremes. Ultimately, the optimal solution is a system that has the lowest power for a given sensitivity level and blocker tolerance.

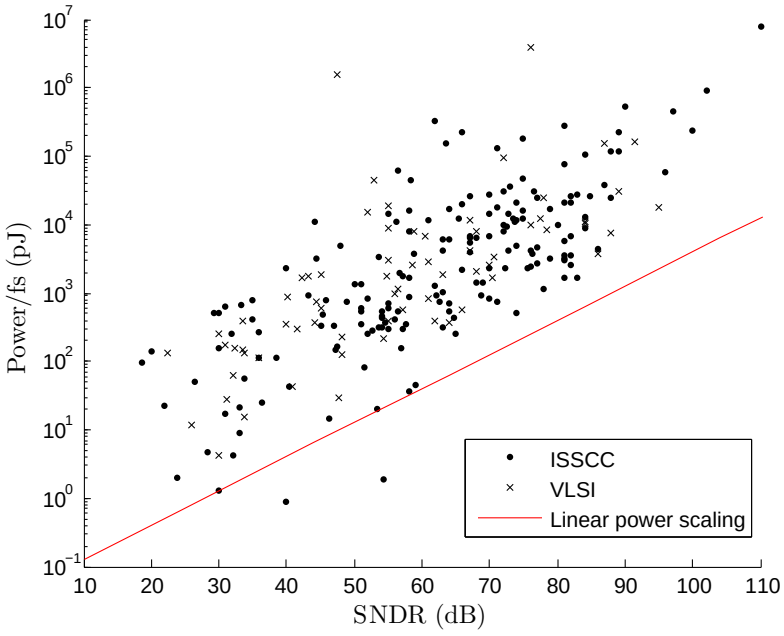
There are a number of A/D converter architectures, each of which has been shown empirically to be the most optimal at a certain range of conversion rate and resolution. These architectures can be generally classified into three categories: flash, multi-step and oversampled A/D converters [108, 42]. Flash A/D converters digitize the signal through comparing it with 2^N reference levels in parallel, where N is the number of bits in resolution. Flash A/D converters can be operated at a very high frequency, however they consume a lot of power and are limited to low resolution conversions. Multi-step A/D converters performs the comparison in multiple steps, where in each step only 2^M comparisons are made, where M is less than N. Multi-step A/D converters can be implemented iteratively (successive approximation algorithm) or in a pipelined manner. Multi-step converters are generally used for medium resolution, medium sampling-rate applications. Last, oversampling A/D converters, which will be discussed in greater detail in section 2.2.1, is suited for high-resolution, low-sampling-rate applications.

We will argue in section 2.2.1 that an oversampled $\Sigma\Delta$ converters offers a unique solution to the problem of partitioning analog and digital signal processing in an A/D converter. A $\Sigma\Delta$ A/D converter samples the input signal at a very high rate, which helps in reducing aliasing. However, it only provides a high dynamic-range A/D conversion around a small signal bandwidth where the signal of interest resides.

To end this section, a survey on the performance of contemporary A/D converters



(a) Bandwidth vs. resolution.



(b) Energy vs. resolution.

Figure 2.7. Survey of A/D converters performance [68].

and the associated power consumption is provided in figure 2.7. There are two important conclusions from this data: what level of performance is possible, and how much does it cost (power) to attain a particular performance level. First, it appears that the bandwidth vs. dynamic-range trade-off is empirically limited by sampling jitter. In this jitter-limited regime, a doubling of the sampling rate would equate to a resolution degradation of 1 bit. This trade-off demonstrates what specifications are attainable from a well-designed A/D converter. Second, this empirical data seems to suggest that there is a linear correlation between power and dynamic-range[3]. A doubling of the A/D dynamic-range (1-bit) would result in a doubling of circuit power. This holds especially true, based on the survey, for low- to medium-resolution converters. From the survey data, it seems that power efficiency is most easily obtained at less than 60dB dynamic range (SNDR).

2.2 Sigma-Delta A/D Converters

$\Sigma\Delta$ A/D have been gaining popularity as the A/D converter topology of choice for RF receivers. The increase in popularity of $\Sigma\Delta$ A/D is attributed to its low power consumption and the relaxed anti-aliasing filter requirements due to oversampling nature of $\Sigma\Delta$ A/D converters.

Extensive and excellent references on $\Sigma\Delta$ A/D converters are available elsewhere [75, 81]. However, due to the central nature of $\Sigma\Delta$ A/D conversion to this work, a brief introduction of $\Sigma\Delta$ A/D converter along with its relevance to RF receiver design is presented in this section. Relevant notations and terminologies of $\Sigma\Delta$ modulation is introduced.

2.2.1 Short Introduction to Sigma-Delta A/D Conversion

$\Sigma\Delta$ A/D conversion, or equivalently $\Sigma\Delta$ modulation, is a technique that enables high-resolution A/D conversion using low-resolution quantizer operated at a high speed. There

[3]This result is rather surprising, because theoretically a 1-bit increase in dynamic range would *quadruple* the power consumption of the converter [108].

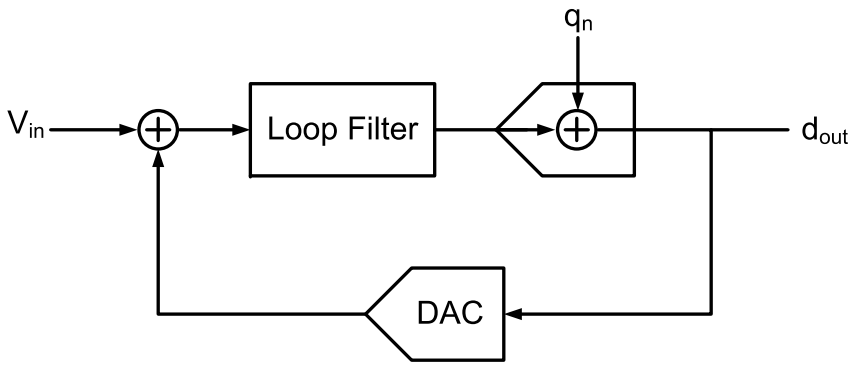


Figure 2.8. A low-pass/baseband ΣΔ modulator.

are two concepts central to the operation of a ΣΔ modulation, *oversampling* and *quantization noise shaping*.

Oversampling in an A/D converter, enables an increase in SNR simply by spreading the quantization noise over a larger bandwidth. If the signal is fully contained within a limited bandwidth of BW which is less than the Nyquist-rate of the quantizer ($\frac{f_s}{2}$), then only the quantization noise within the signal bandwidth of BW should be considered. All other signals, including the quantization noise, that resides at locations other than the frequency band of width BW can be discarded using digital filters. An oversampling ratio (OSR) is defined as the ratio between the Nyquist-rate ($\frac{f_s}{2}$) of the quantizer and the signal bandwidth (BW):

$$OSR = \frac{f_s}{2 \cdot BW} \tag{2.2}$$

An N-bit quantizer would have an SNR of $(1.76 + 6.02 \cdot N)$dB [108]. This quantization noise is spread over a bandwidth equal to $\frac{f_s}{2}$; i.e., the quantization noise is white[4]. Therefore, the achievable SNR with an oversampling ratio of OSR is:

$$SNR_{oversampled} = 1.76 + 6.02 \cdot N + 10 \cdot \log_{10}(OSR) \tag{2.3}$$

Thus, every doubling of the OSR would result in a 3dB improvement in SNR.

Quantization-noise shaping can further lower the quantization noise power within the

[4]The white-noise assumption does not necessarily hold true for low N, where the quantization noise is highly correlated with the input signal. However, for brevity of exposition of this chapter, a white quantization noise will be assumed. More information about the validity of this assumption can be found in [75, 31].

band of interest. This is achieved by moving the quantization noise away from the band of interest. When combined with oversampling, an improvement of more than 3dB per doubling of the OSR can be achieved.

Quantization-noise shaping can be accomplished by enclosing a (loop) filter around a mixed-signal feedback comprising of a quantizer and a feedback D/A converter (figure 2.8). The loop filter can take one or many poles, and it can have a low-pass or a band-pass frequency response. The frequency-response of the loop filter will determine the frequency characteristics of the loop gain of this feedback system.

For a low-pass type modulator, the large loop gain at DC will force force the feedback D/A converter's output signal to follow the input signal as faithfully as possible. This is only possible if the low-frequency component of the modulator's output $d_{out}[n]$ tracks the low-frequency component of the input signal. In other words, at low frequency, the quantization error is suppressed by virtue of the large loop gain. As the frequency of the input signal is increased, the loop gain at that frequency will diminish, and as a result the quantization noise will start to increase.

Mathematically, quantization noise can be modeled as an added white noise $q_n[n]$, that is introduced within the quantizer block[5]. The output of the modulator $d_{out}[n]$ is composed of the input signal $V_{in}[n]$ and the quantization noise $q[n]$. Because the two inputs are introduced at two different points within the loop, each of them will have a different transfer function to the output. The two different transfer functions, called the signal transfer function (STF) and noise transfer function (NTF), can be designed to have advantageous frequency characteristics.

For example, a first-order, low-pass $\Sigma\Delta$ modulator can be designed to have a first-order noise shaping. A first-order $\Sigma\Delta$ modulator consists of a single integrator as the loop filter.

[5]Since a $\Sigma\Delta$ A/D uses a low-resolution quantizer, the white-noise approximation is a rather poor approximation. For more information regarding the conditions on which this approximation is valid, the reader is referred to the work of Gray[31].

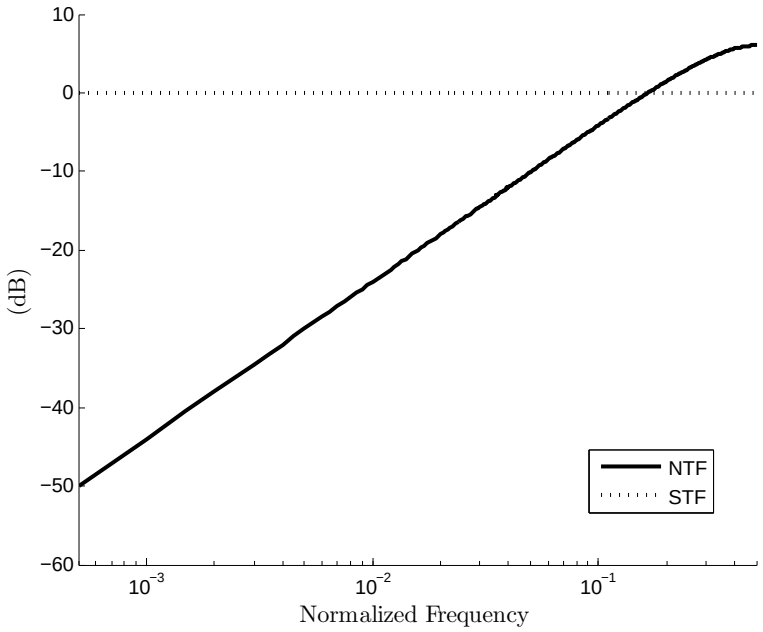


Figure 2.9. Signal and noise transfer functions for a first-order ΣΔ modulator.

The following STF and NTF can be achieved:

$$STF = 1 \tag{2.4}$$

$$NTF = 1 - z^{-1} \tag{2.5}$$

The STF is flat across frequency, while the NTF has a high-pass response (figure 2.9). In this manner, quantization noise is attenuated in the frequency of interest (low frequency), while the signal amplitude is maintained throughout the conversion. The power-spectral density plot of the output is shown in figure 2.10. A 20dB-per-decade rolloff of the quantization noise is observed as a result of a first-order noise shaping. Because the signal is oversampled, only quantization noise that resides at low frequencies matter in the resulting SNR.

Higher-order ΣΔ modulator can be built by cascading stages of integrators or resonators, for a low-pass and band-pass modulator respectively. However, since there are two or more poles in the loop, stability is no longer guaranteed. The feedback loop would then need to be compensated, either in a feedforward or in a feedback manner. The benefits and drawbacks of these two compensation techniques are discussed in the following references [75, 81].

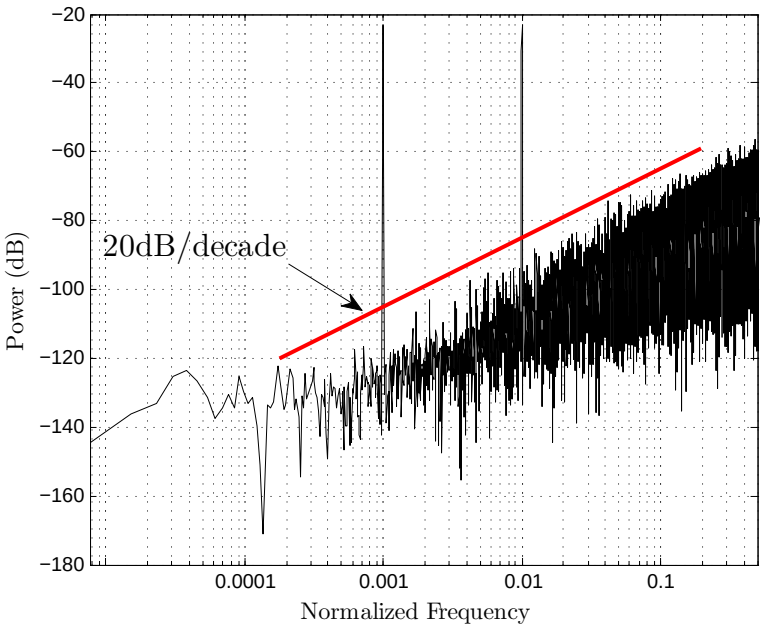


Figure 2.10. Output power spectral density of a simulated first-order ΣΔ modulator.

A ΣΔ A/D converter requires a reconstruction filter in the digital domain. Because the signal is oversampled, a sample-rate down-conversion is necessary in order to isolate and retrieve the signal of interest. The digital decimation filter, as the ΣΔ A/D reconstruction filter is often called, is usually not a dominant power consumption contributor. Modern CMOS process allows for a very power-efficient digital computation. Moreover, although the throughput of such a filter can be high, the output of a ΣΔ modulator has only a few bits. Therefore the signal-processing data path can be quite narrow.

2.2.2 Sigma-Delta A/D Converters in RF Receivers

As mentioned earlier, an oversampled ΣΔ A/D converter offers a unique alternative among a selection of A/D converter topologies for an RF receiver. In some ways, a ΣΔ A/D converter is able to break the trade-off between the need to have a fast, high resolution A/D converter and the need to have a very selective baseband filter in RF receiver.

The reason a ΣΔ A/D converter is appropriate for an RF signal is precisely because of the two reasons why this type of converter works so well: oversampling and noise-shaping.

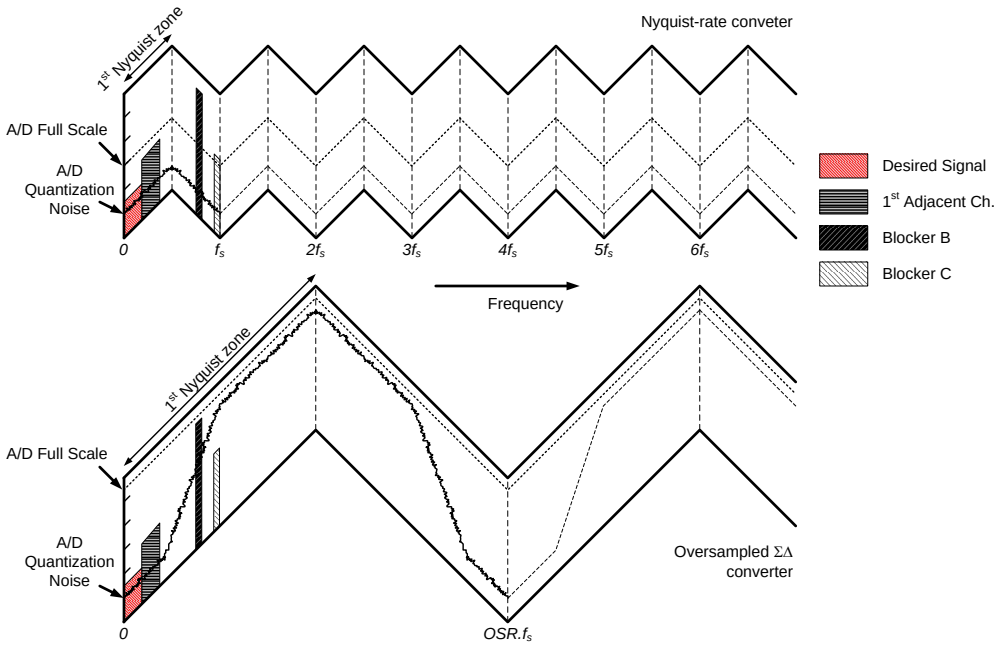


Figure 2.11. Comparison between a Nyquist-rate and a ΣΔ A/D converter.

Oversampling widens the first Nyquist zones, and therefore it reduces aliasing. In other A/D converter topologies, an increase in sampling-rate would require the converter's low noise floor to be maintained across a wider conversion bandwidth. To make matter worse, since the bandwidth of the input signal is wider, the input signal power is likely to increase. As argued in section 2.1, while the quantization noise floor needs to be kept low, now the full-scale range of the A/D converter has to be increased to accommodate large blocker signals. As a result, an increase in sampling-rate would be accompanied by a necessary increase in resolution as well. Both an increase in sampling rate and resolution would surely result in an increase in power consumption.

Recall that the low quantization noise floor is only needed in the frequency band of interest, for example, near DC for a low-pass modulator. Although the full-scale range of the A/D converter has to be set to accommodate large blocker signal outside the band of interest, the noise floor at those frequencies is not critical. This is where quantization noise shaping feature of a ΣΔ A/D converter really makes sense, as it provides a low quantization

noise floor *only* where it is needed. The quantization noise floor is not unnecessarily set to be at a very low level outside the band of interest.

For a comparable sampling rate and resolution, it has been shown that a $\Sigma\Delta$ converter with its associated reconstruction filter can achieve the same power efficiency as a Nyquist-rate data converter [61]. For this reason, it can be argued that the virtue of a $\Sigma\Delta$ A/D converter can be obtained for no additional cost. It is often stated that a $\Sigma\Delta$ A/D provides a *free* anti-alias filtering. This statement is not entirely correct. Anti-alias filtering in this type of system occurs in the digital domain.

Performing the anti-alias filtering in the digital domain has one additional advantage. In a $\Sigma\Delta$ converter, the signal bandwidth is not explicitly defined in the analog domain. The final signal selection is done in the digital domain, through the application of digital filters. This creates an opportunity for re-programming the digital filters to accommodate change of signal bandwidths. This feature is very amenable to a concept of reconfigurable RF receiver. It should be noted, however, that if the signal bandwidth is increased, more quantization noise is also integrated. If a high-order $\Sigma\Delta$ modulator is used, increasing signal bandwidth can come with a significant degradation in resolution as the quantization noise is shaped.

2.3 Reconfigurable RF Receiver Specifications

A survey of requirements for different wireless standards will be presented in this section in order to derive a set of requirements for the proposed reconfigurable RF receiver. As argued in section 2.1, the specification of an RF receiver is driven by the characteristics of the signals received at the antenna.

The RF signal characteristics for different standards can be summarized by a blocker mask and a sensitivity requirement. A comparison between blocker masks of three different wireless standards is shown in figure 2.12. A blocker mask provides a good representation as to the largest signals that can be expected at the antenna. Another set of requirements are derived based on the minimum SNR required for successful demodulation and the required

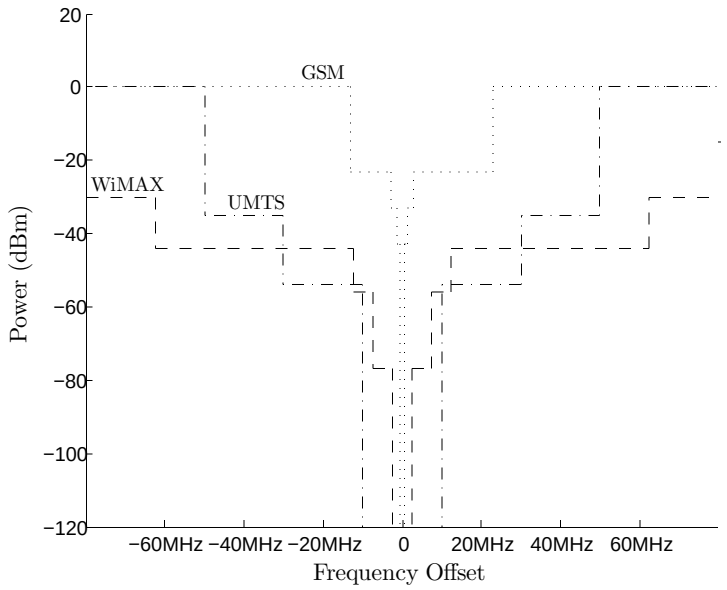


Figure 2.12. Comparison of blocker masks between different wireless standards.

Table 2.1. Comparison of sensitivity requirements for different wireless standards.

	Bandwidth	Sensitivity Level	Min. SNR	Max. NF
GSM	200kHz	-99dBm	9dB	12dB
UMTS	3.84MHz	-92dBm*	7dB	9dB
WiMAX	20MHz	-65dBm°	24dB	11dB

* Including 25dB de-spreading gain

° Highest data-rate, with 64-QAM and 3/4 coding rate

sensitivity of the particular wireless standard. A comparison of sensitivity levels between various standards are presented in table 2.1.

The three standards illustrated in figure 2.12 and table 2.1 are chosen specifically to illustrate the range of requirements that a reconfigurable RF receiver has to satisfy. On one end, the GSM standard is a narrow-band standard, with a 200kHz signal bandwidth. It is relatively easy to design a high-resolution A/D converter for this standard. However, the GSM standard has some of the most stringent blocker mask requirement; for example, a blocker signal 3MHz away could be more than +76dB larger than the desired signal. On the other end of the spectrum, a WiMAX standard is a high data-rate wireless standard,

Table 2.2. Requirements for a reconfigurable RF receiver.

Parameter	Value
Bandwidth	200k-20MHz
Max NF	9dB
Center Frequency	0-5.2GHz
IIP3	-5dBm
IIP2	65dBm
Max. Signal	0dBm

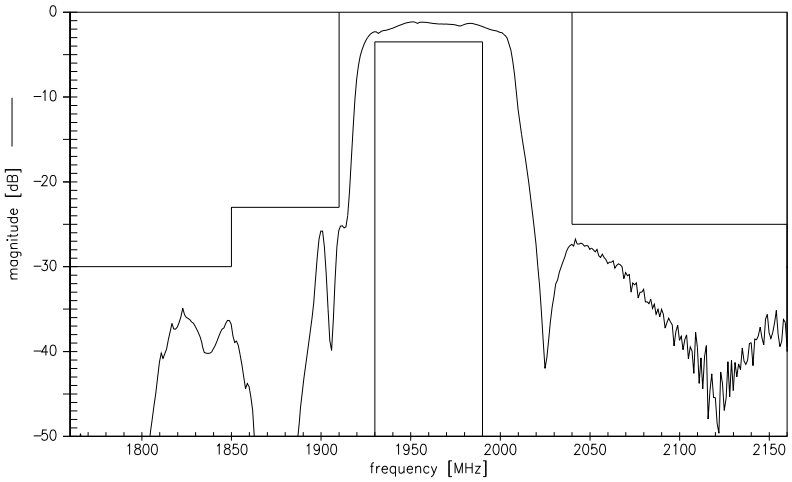


Figure 2.13. Frequency response of a SAW filter for a UMTS standard [26].

with a maximum throughput of more than 75Mbps. In order to achieve this data-rate, a wide signal bandwidth with a complex modulation scheme is used. As a result the WiMAX standard, at its highest data-rate mode, requires a 20MHz bandwidth with a minimum SNR of 24dB for successful decoding. However, the blocker mask requirement of a WiMAX standard is much less stringent than a GSM standard. For example, at greater than 10-MHz offset from the carrier, the maximum signal level of a WiMAX signal is more than 15dB lower than that of a GSM signal.

Based on this survey, a table of requirements for a reconfigurable RF receiver can be derived. These requirements are summarized in table 2.2.

It is important to mention that the high level of performance of today's RF receivers is partly due to the use of external passive filters, such as SAW filters. These passive filters

operate at RF, with less than 3dB insertion loss, and can have a rejection ratio of greater than 30dB (figure 2.13). These filters reduces the dynamic-range requirements of the RF receiver, as the filters eliminate much of the largest blockers with minimum degradation in sensitivity. However, the fixed-frequency nature of these filters make them incompatible with the desire for a universally reconfigurable RF receiver. While high-quality tunable RF filters are being researched [72], they are not yet widely available.

2.4 Performance Comparison of Integrated Receivers

In the last decade, a significant progress has been made in incorporating a complete RF receiver in a single monolithic die. Initially, short-range standards, such as 802.11 and Bluetooth, with less stringent performance requirements were integrated within a single-die. Today, single-chip solutions exist for most of the long-range cellular standards as well. The performance of these chips is outlined in table 2.3. The different performance metrics, such as noise-figure and input-intercept points, reported for a standard reflects the trade-offs involved in meeting the requirements of the particular standard. The reported performance reflects the design decisions that result in an optimized implementation of a particular standard. For example, the receiver which has the lowest noise figure is a GPS receiver, because in this application, sensitivity is of utmost importance. Similarly, mobile cellular receivers also have to achieve a very low sensitivity while at the same time maintain a low power consumption. On the other hand, in wireless LAN standards, data-rate is the most important metric, while communication range and power consumption is of secondary importance.

In order to maintain backward compatibility with earlier versions of the wireless standards, some of the radios listed in 2.3 are in a way already 'reconfigurable'. For example, the EDGE standard uses the same signal bandwidth as GPRS; however, EDGE uses a more advanced modulation scheme (8-PSK for EDGE, compared to GMSK for GPRS) in order to obtain a higher spectral efficiency. Although both standards occupy the same signal bandwidth, the linearity requirement for EDGE standard is somewhat more stringent than GPRS

Table 2.3. RF receiver performance comparison.

	Year	Standard	Technology	Power (mW)	NF (dB)	IIP3 (dBm)	IIP2 (dBm)
[64]	2004	Bluetooth	130nm	60			
[56]	2007	Bluetooth(EDR)	130nm	48		-18	
[59]	2005	802.11g	180nm	324	5.5		
[71]	2006	802.11a/b/g	180nm	310	5.5		
[82]	2006	802.11n	90nm	170	6		
[12]	2007	802.11n	130nm	275	4.5	5	
[23]	2008	802.11a/g/n	90nm	270	4		
[102]	2001	GSM	350nm	75	5	-16	
[63]	2006	GSM/GPRS	90nm	84	2	-25	46
[27]	2005	GSM/GPRS	180nm	256	2.7	-15	40
[48]	2005	GPRS/EDGE	BiCMOS	202	3	-9	
[21]	2008	GPRS/EDGE	130nm	140	2.5	-12	45
[9]	2005	CDMA	BiCMOS	151	3		
[38]	2006	WCDMA	BiCMOS	50*	9	0	55
[104]	2008	WCDMA	180nm	105	2.8	-2	65
[118]	2007	CDMA2000	130nm	150	9.2	1	51
[51]	2007	TD-SCDMA	BiCMOS	95	3.5	-14	25
[92]	2005	GPS	90nm	84	2	5	
[24]	2006	GPS	BiCMOS	20	5		

(* does not include synthesizer power)

Table 2.4. Comparison of multi-mode radios.

	Entry	Supported Standards	Frequency Bands
[15]	Broadcom BRCM2075	Bluetooth (EDR)	1
		GPS	1
		FM	1
[16]	Broadcom BRCM4329	802.11n	2
		Bluetooth (EDR)	1
		FM	1
[52]	Marvell	802.11	1
		WiMAX	1
[37]	Freescale	WCDMA/HSDPA	10
		GSM/GPRS/EDGE	4
[11]	TI/Univ. of Arizona	GSM/GPRS/EDGE	3
		CDMA2000	1
[100]	Skyworks	WCDMA/HSDPA/HSUPA	11
		GSM/GPRS/EDGE	4
[32]	Qualcomm	WCDMA/HSDPA/HSUPA	10
		GSM/GPRS/EDGE	4
		GPS	1

as a result of the more complex modulation scheme. In this case, the RF receiver front-end has to be designed to meet the more stringent EDGE requirement. This is reflected by the fact that EDGE receivers have higher IIP3 and IIP2 when compared to GPRS receivers. This underlines the point made earlier, that for each performance metric, a multi-standard receiver has to meet the most stringent requirement from all of the supported standards.

The initial impetus for a multi-standard receivers is the desire to maintain backward compatibility, as in the case with a GSM/EDGE receiver. From this starting point, several published examples have shown the integration of multiple radios spanning multiple standards on a single die. For the most part, cost reduction through higher integration is the reason behind the development of these multi-standard radios. A summary of multi-mode radios that have been published in the literature is presented in table 2.4.

There is a clear progression from the development of a single-chip radio, to a single-chip, multi-standard radio in the industry. There has also been a lot of research done in the realm of software-defined radio. In theory, a software-defined radio can communicate with any conceivable wireless device. However, in practice, most published examples of

Table 2.5. Comparison of published software-defined radios.

Standard	IMEC [29]			UCLA [10]			Bitwave [80, 22]		
	NF (dB)	IIP3 (dBm)	Power (mW)	NF (dB)	IIP3 (dBm)	Power (mW)	NF (dB)	IIP3 (dBm)	Power (mW)
GSM	2.8	-5	91	5	-3.5	52	3.4	-19	142
WCDMA							3.2	-18	244
LTE	2.4	-6	96						
CDMA2000							5	-13	
802.11	6.5	-9	116	5.5	-3.5	57	5.6	-20	
WiMAX	3.8	-11	105					-20	183
DVB-H	2.3	-5	101						

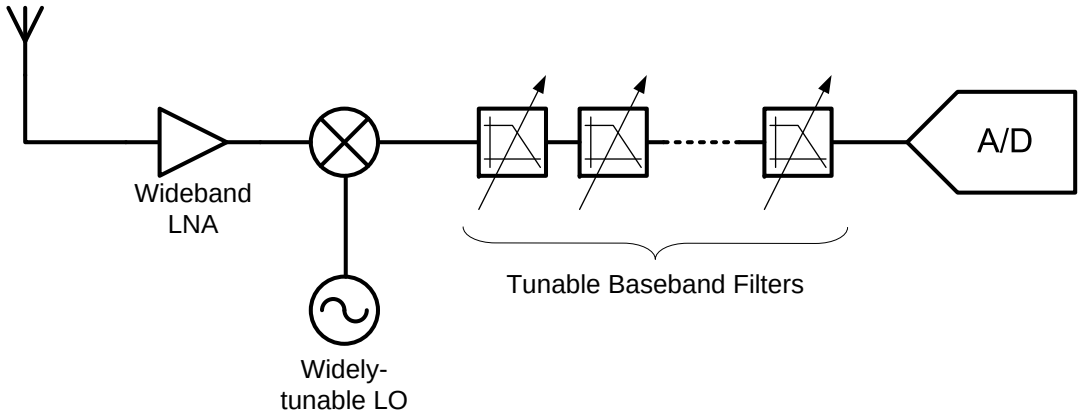


Figure 2.14. Conceptual diagram of a software-defined radio.

so-called 'software-defined radios' are simply designed to comply with the requirements of the wireless standards available *today*.

There are a number of examples of these software-defined radios in the literature, which are summarized in table 2.5. All three transceivers employ a common strategy of having a highly reconfigurable signal path. All of them uses a single-conversion receiver architecture followed by a tunable, high-order low-pass filter (figure 2.14). A single-conversion architecture is suitable in such a flexible radio, due to the ease of frequency planning, especially with respect to the location of image signals.

The UCLA receiver uses a wideband, noise-cancelling LNA. A harmonic-rejection mixer [113] is used to downconvert the RF signal to baseband, while avoiding the folding of signals

located at three times the LO frequency. The output of the mixer is filtered by a single, continuous-time RC pole before being sampled using a charge-sampling circuit [116]. A discrete-time system, consisting of a single IIR filter, two FIR filters and two sample-rate downconverters, precedes an A/D converter. The critical frequency of the discrete-time filter can be precisely tuned by changing the clock frequency and by changing the capacitance ratios within the filter. The discrete-time system used in this receiver is similar to the ones implemented in Texas Instruments' DRP receivers [65, 63]. The operation of this discrete-time system will be described in detail in section 3.2.

The IMEC receiver contains a low-band and high-band LNAs that are switched depending on the frequency band of interest. A passive mixer with a square-wave LO is used to downconvert the RF signal to baseband. The load of the passive mixer is implemented as a transimpedance amplifier biquad. The biquad is followed by a third-order low-pass filter, for a total of five poles in the receiver. The location of the five poles are programmable, however there is no discussion on the approach taken to tune the critical frequency of this filter. Finally, a variable-gain amplification (VGA) occurs prior to A/D conversion.

2.5 Performance Limitations of RF Receivers

In the preceding sections, a performance comparison of integrated receivers was presented. In an effort to predict an attainable level of performance for current and future RF receivers, several limitations, fundamental, practical or otherwise, will be evaluated in this section.

2.5.1 Linearity Limitation

A transistor is not a linear device. It is only approximately linear if operated under a limited operating conditions, namely under a very small input or output signal swing. However, operating with a limited signal range comes with a noise penalty as it limits the acceptable gain of the preceding circuit blocks. Thus this intrinsic transistor limitation

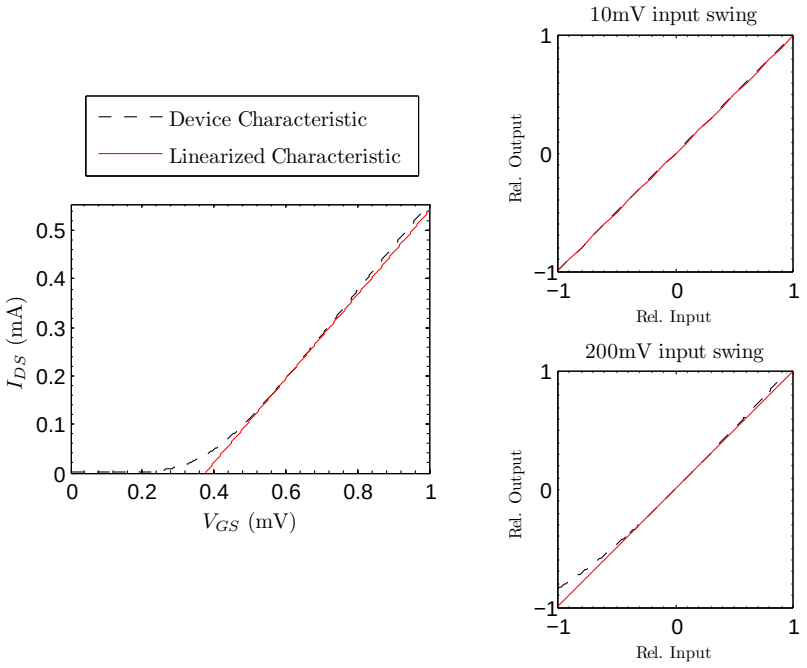


Figure 2.15. MOS transistor voltage-to-current conversion characteristics.

translates again into a dynamic-range limitation. There is an inherent trade-off between signal range, which is limited by distortion, to the resulting circuit noise.

One of the most fundamental operations in any circuit is a voltage-to-current conversion (V-to-I conversion). This is a natural operation for a MOS transistor, where a modulation of the gate voltage would result in a similar modulation of the drain-source current. The voltage-to-current transfer characteristic of a MOS transistor is illustrated in figure 2.15. The two insets in figure 2.15, displays the linearity of the V-to-I conversion under two different input signal ranges (plots are normalized in both axes). It can be clearly seen that operating under a larger input swing generates a larger deviation from a linear transfer characteristic.

Second- and third-order distortions typically dominate in an RF circuit. Distortion in a nonlinear device can be characterized using a polynomial expansion of the device transfer characteristics [73]. In theory, the polynomial expansion can be expanded into very high order; resulting in high-order (e.g. fourth, fifth, sixth, etc) distortion. However, in practice, second- and third-order distortions have much larger amplitude than the higher order terms,

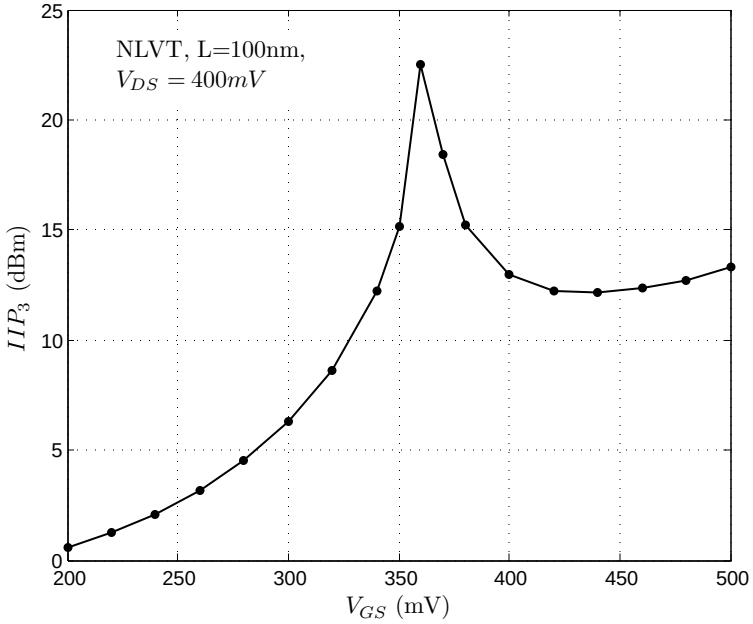


Figure 2.16. Achievable IIP3 from a deep sub-micron transistor.

making them the dominant distortion mechanisms. There are several metrics that can be used to characterize the 'magnitude' of the second- and third-order distortions. Two of the most commonly used are the input-intercept points, namely IIP2 and IIP3 for second- and third-order distortions respectively [49].

A characterization of the third-order distortion in a MOS V-to-I conversion is shown in figure 2.16. In this figure, an IIP3 resulting from a V-to-I conversion is plotted as a function of gate DC bias. The drain voltage of transistor is connected to an ideal voltage source to decouple the distortion resulting from drain-to-source voltage modulation. Although a peak IIP3 of more than +20dBm is theoretically possible, it is only achievable within a narrow window of DC bias. Such a narrow window would be hard to achieve in a production setting without calibration. From this analysis, one can assume that a realistic IIP3 from modern CMOS transistors would be in the +15dBm range[6].

In theory, spurious tones resulting from second-order (and all even-order) distortion can be completely eliminated in a fully differential topology. In other words, second-order

[6]The IIP3 presented here is evaluated for a differential input and output; which is the configuration used in this work. For a single-ended input, the achievable IIP3 shown above needs to be reduced by 6dB.

Table 2.6. Achievable SFDR for a +10dBm IIP3.

Input (dBm)	SFDR (dB)	
	HD3-limited	IM3-limited
0	< 20	< 30
-10	< 40	< 50
$<$ -25	70	80

distortion is not a fundamental limitation. In practice, a fully differential circuit is never perfectly symmetric, and thus second-order distortion tones can never be completely eliminated. Second-order distortion is particularly troublesome in direct-conversion mixers. Because of the second-order intermodulation mechanism, large blockers, regardless of the frequency location, can create spurious tones that overlap with the signal of interest. This mechanism, along with means to alleviate them is thoroughly explained in [55].

Input-intercept points are absolute metrics that are often used to characterize the intrinsic linearity of a device or circuit. However, the magnitude of the distortion generated by the circuit is also a function of the magnitude of the input signal. In other words, the *spurious-free dynamic-range* of the circuit is dependent on the signal amplitude. As the name implies, spurious-free dynamic range (SFDR) is often used to characterize the *relative* difference between the amplitude of the signal and the amplitude of the largest distortion product. Achievable SFDR for a device with +10dBm IIP3 is given in table 2.6. As seen in table table 2.6, a certain back-off must be applied in order to achieve a higher SFDR.

There is an inherent trade-off between achieving low noise and high linearity. As illustrated in table 2.6, higher spurious-free dynamic range can be achieved simply by reducing the input signal swing, or similarly by having a larger back-off. However, in order to maintain a constant SNR, a reduction in the input signal has to be accompanied by lowering of circuit noise. Hence, in effect the dynamic-range limitation in a radio receiver really originates from the limitation from the device level.

2.5.2 Frequency-Synthesizer Phase Noise

An accurate frequency reference is needed in an RF receiver in order to translate a radio frequency signal down to DC or some other low frequency. Typically, a phase-locked loop is used to up-convert a high-quality, low-frequency reference oscillation from a crystal to an oscillation at a radio frequency. Noise at the output of this frequency synthesizer originates from the voltage-controlled oscillator, crystal reference or any part of the loop circuitry.

An ideal frequency reference would consist of a single tone in the frequency domain, and all of the signal's energy is concentrated in an infinitely narrow bandwidth around the desired frequency. In the presence of noise, the energy becomes spread out around the singular tone at the desired frequency [34]. Timing error due to noise can be modeled by a random phase modulation $\phi(t)$ on the oscillatory signal. Suppose a frequency synthesizer has a sinusoid output waveform $LO(t)$, then the output (with noise) can be written as:

$$LO(t) = A \cdot sin(\omega_o t + \phi(t)) \tag{2.6}$$

where $\phi(t)$ is a random phase fluctuation due to the presence of noise in the system. Since $\phi(t)$ is small, equation 2.6 can be rewritten as:

$$LO(t) \approx A \cdot \sin(\omega_o t) + A \cdot \phi(t) \cdot \sin(\omega_o t) \tag{2.7}$$

Due to the presence of noise, the output of the frequency synthesizer consists of a single tone surrounded by noise that is up-converted to a frequency of ω_o.

A phase-noise plot describes the power spectral density of $\phi(t)$, $S_\phi(f)$ as a function of frequency. The x-axis is drawn as an offset frequency from the desired frequency ω_o, while the y-axis is in decibels relative to the total output power. A sample phase-noise plot is shown in figure 2.17 [1]. A typical phase-noise plot consists of a floor at large frequency offset and an elevated noise level at small frequency offset. For a review of phase-noise characteristic, the reader is referred to [90].

Phase noise in a frequency synthesizer can reduce the sensitivity of an RF receiver due to a mechanism called reciprocal mixing [49]. Suppose a desired signal $RF(t)$ is at a frequency ω_o and it is to be down-converted to baseband using a frequency synthesizer whose output

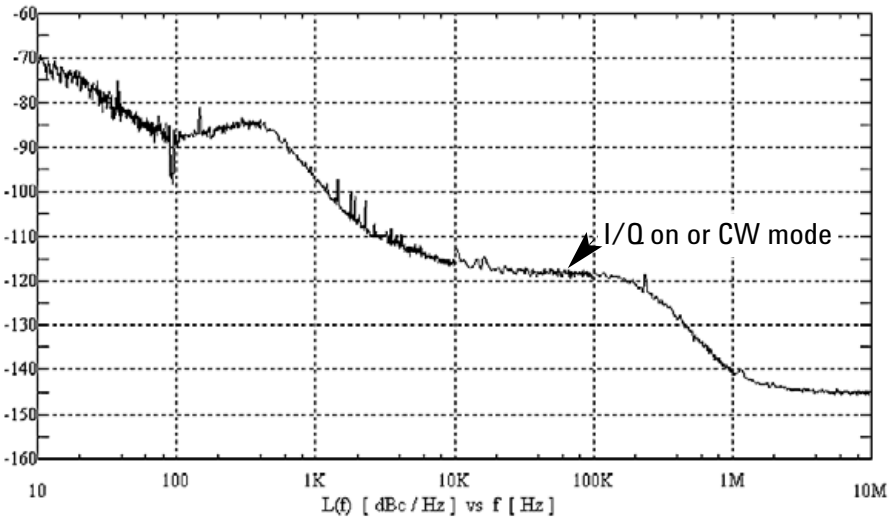


Figure 2.17. Phase-noise plot of an Agilent 4438C frequency synthesizer.

is described by equation 2.6;

$$\begin{aligned} y(t) &= RF(t) \cdot LO(t) \\ &= RF(t) \cdot A \cdot [\sin(\omega_o t) + \phi(t) \cdot \sin(\omega_o t)] \\ &= RF(t) \cdot A \cdot \sin(\omega_o t) \cdot [1 + \phi(t)] \end{aligned} \tag{2.8}$$

The desired down-converted term $RF(t) \cdot A \cdot \sin(\omega_o t)$ is accompanied with an undesired noise term of magnitude $RF(t) \cdot A \cdot \sin(\omega_o t) \cdot \phi(t)$ due to reciprocal mixing. Thus, in the presence of phase noise from the synthesizer, the resulting signal-to-noise ratio of the RF receiver is limited to:

$$SNR_{max} = \frac{1}{\int_0^{BW} S_\phi(f) \cdot df} \tag{2.9}$$

For the frequency-synthesizer in figure 2.17, the resulting SNR for a given bandwidth is given in table 2.7. The result shown underlines the importance of the close-in phase noise as it tends to dominate the achievable SNR. Because the magnitude of the close-in phase noise is so much larger than the far-out noise floor, the SNR for signal bandwidths of 2MHz and 20MHz only differs by 1dB.

This SNR limitation becomes a particular concern in the case when there is a large blocker that is very close in frequency to the desired signal. In other words, the signal $RF(t)$ contains both the desired signal at frequency ω_o, and a large blocker at a small

Table 2.7. Achievable SNR with an Agilent 4438C as a frequency reference.

Signal Bandwidth	Achievable SNR
2MHz	67dB
4MHz	66.8dB
8MHz	66.6dB
20MHz	65.9dB

frequency offset. Because of reciprocal mixing, the presence of this large blocker signal results in an increased noise floor at the desired frequency. As a result, the presence of this blocker signal can desensitize the receiver.

Chapter 3

Sigma-Delta Receiver

The previous chapter introduces the notion of an RF receiver as a signal pre-conditioner for an A/D conversion. We explore the design trade-off between obtaining frequency selectivity in the analog domain and using a faster, higher-resolution A/D converter. The discussion underlines the importance of baseband filters in an RF receiver as an anti-alias filter prior to A/D conversion. In section 2.2.1, we argued that a $\Sigma\Delta$ A/D converter is perfectly suited for an RF receiver, because of its oversampling and noise-shaping nature.

In this chapter, an RF receiver architecture is introduced based on a down-converting $\Sigma\Delta$ modulator. This system will subsequently be referred to as a $\Sigma\Delta$ receiver. A direct-conversion architecture is chosen in order to simplify the frequency planning for this reconfigurable RF receiver. Aliasing is minimized by keeping the sampling-rate equal to the LO rate. As a result no aliasing occurs, beside the folding due to a square-wave mixing. The high sampling rate also allows the use of a very simple, passive, switched-capacitor loop-filter in order to obtain a high SNR. Final baseband selection is performed in the digital domain, where the signal bandwidth can be re-programmed easily.

An overview of the system and how it operates is presented in the next section. Following that, a block-by-block analysis of the proposed architecture is presented. The result of the analysis is used to derive important parameters for circuit design.

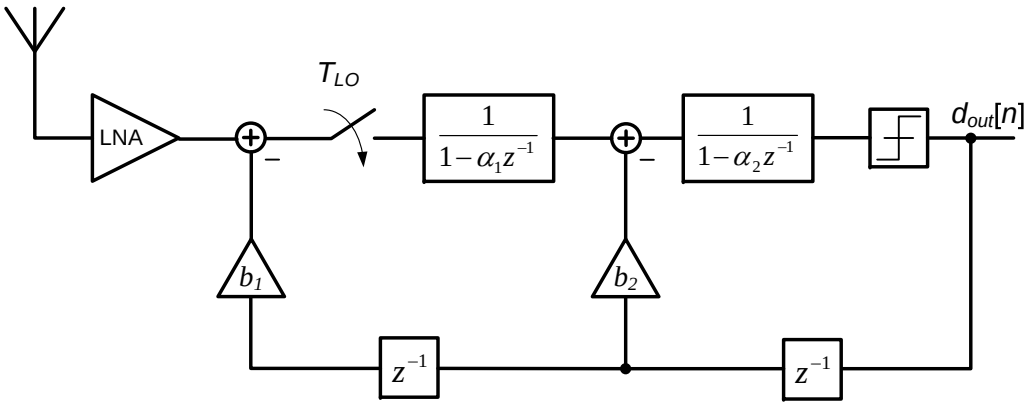


Figure 3.1. A ΣΔ receiver block diagram.

3.1 System Overview

The system proposed in this chapter is designed to take a signal at a radio frequency and converts it to a digital representation. A block diagram of a ΣΔ receiver is shown in figure 3.1. The receiver consists of a direct-conversion mixer enclosed within a second-order low-pass ΣΔ modulator. A low-noise amplifier (LNA) with a power gain of 20-30 dB is assumed to precede the system. The LNA is present to improve the overall sensitivity of the system as well as to provide an input impedance match to the receiver's antenna.

The output of a current-commutating mixer, evaluated at the right time instants, can be thought of as a sampled-and-held signal (section 3.2.1). In other words, the output of the mixer can be thought of a discrete-time signal sampled at the mixing rate (f_{LO}), which in this case is equal to the center frequency of the desired signal. Aliasing will occur, however it will occur with a periodicity of f_{LO} which is two or three orders of magnitude larger than the signal bandwidth.[1] In fact, using this interpretation, the radio signal at f_{LO} is effectively *aliased* down to baseband/DC. The resulting discrete-time signal is then processed by the ΣΔ modulator which is also run at a frequency of f_{LO}. In this manner, no further aliasing will occur; as a result, no additional anti-aliasing filter is necessary.

Conceptually, the difference between a ΣΔ and a conventional receiver architecture is

[1]Thorough analysis in section 3.2.1 will show that only signals at *odd* multiples of f_{LO} will overlap with each other. Signals at *even* multiples of f_{LO} will be filtered out prior to sampling.

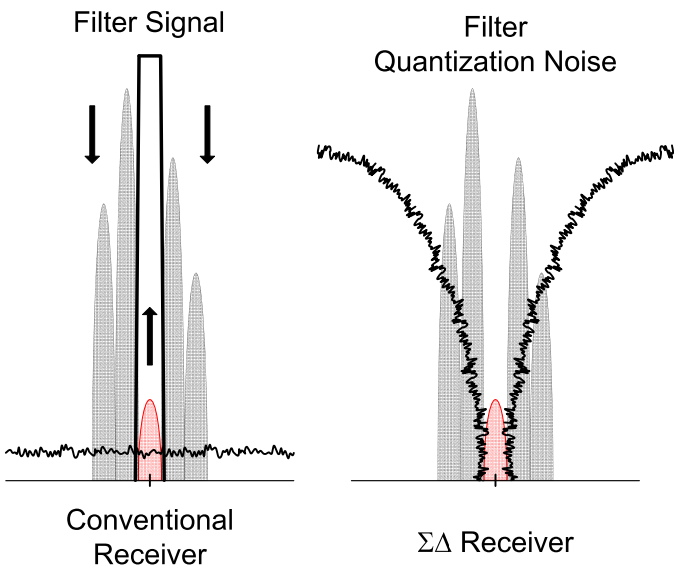


Figure 3.2. Comparison between a conventional and a ΣΔ receiver.

illustrated by figure 3.2. In a conventional receiver, the circuit amplifies the desired signal while at the same time attenuating large out-of-band blocker signals. This is done in order to pre-condition the signal for A/D conversion, which has a limited dynamic range and sampling rate. In contrast, in a ΣΔ receiver, the input signal is kept relatively constant, while the quantization noise is shaped/filtered. The quantization noise in the ΣΔ receiver is shaped such that the SNR is maximized around the desired signal.

Signal bandwidth in a ΣΔ receiver is not explicitly defined in the analog domain. Since the input signal is never filtered, there is no bandwidth limitation in the analog domain. Digital filters are used to eliminate out-of-band blockers and quantization noise, prior to digital demodulation. The use of digital filters results in a great flexibility on redefining signal bandwidth through re-programming of the digital filter. This fact makes this receiver architecture appropriate for use in a highly-reconfigurable RF receiver. On the other hand, due to noise shaping, the quantization-noise floor is frequency dependent. Therefore, if one were to integrate over an excessively large bandwidth, the resulting SNR would be quite poor.

The ΣΔ modulator in this architecture relies on a very large oversampling ratio in order to achieve a high dynamic range. As mentioned before, the frequency f_{LO} can be two or

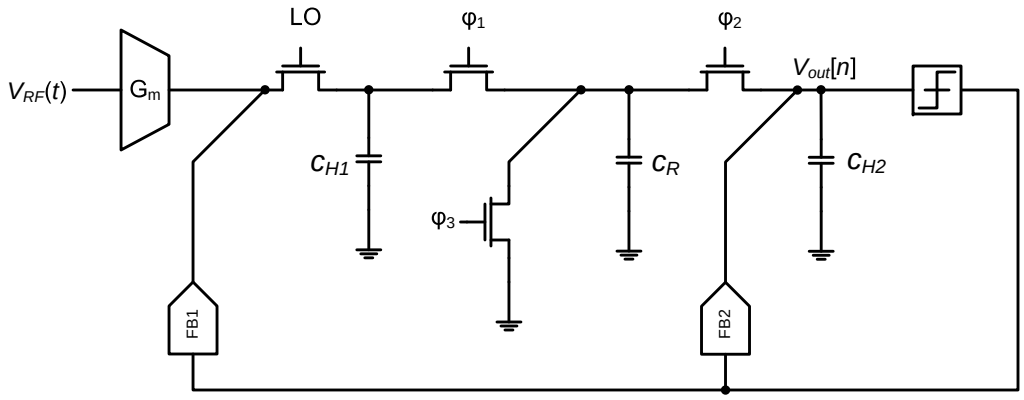
Table 3.1. Achievable SNR from a second-order ΣΔ A/D with a passive loop-filter, with f_{LO}=1GHz

Signal Bandwidth	Achievable SNR
2MHz	84dB
4MHz	80dB
8MHz	74dB
20MHz	61dB

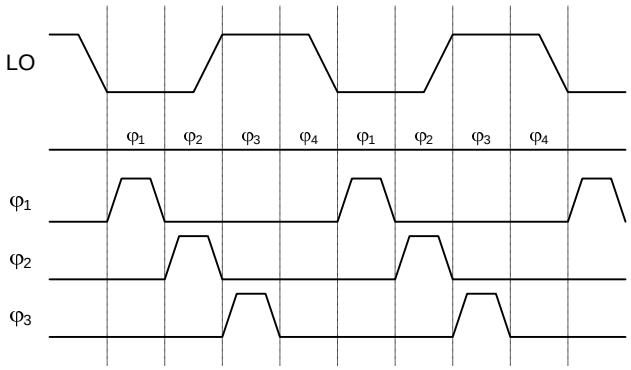
three orders of magnitude larger than the signal bandwidth. A simple second-order, passive loop filter with a single-bit quantizer is sufficient in order to achieve a very high dynamic range. Achievable SNR for a single-bit, second-order, passive ΣΔ modulator is shown in table 3.1. An SNR of 80dB for a 4-MHz bandwidth is achievable with f_{LO}=1GHz from this modulator configuration. As will be shown later, other noise sources, namely circuit noise and frequency-synthesizer noise, instead of quantization noise are the limiting factor to the overall attainable SNR.

The choice of a passive, switched capacitor loop filter is motivated by the impact of CMOS scaling towards the performance of various circuit elements. First, CMOS scaling has benefited the performance of MOS switches. This subject will be analyzed in greater detail in section 3.1.1. Second, design of a high-gain, highly linear amplifier is becoming more difficult in scaled CMOS technologies because of a reduced supply voltage and a lower transistor intrinsic gain [93, 96]. As a result, in this receiver architecture, the use of linear amplifier is avoided wherever possible. The architecture contains only a single linear amplifier; an input transconductance amplifier used to convert the RF voltage into current.

The gain necessary for the ΣΔ modulator loop is mostly provided in a mixed-signal domain; that is the signal gain occurs between the input of the 1-bit quantizer and the two feedback D/A converters. Because the loop-filter is passive, it is not able to provide any amplification. As a result, the signal amplitude at the output of the loop filter can be very small. However, at this point, the signal needs to be quantized with a 1-bit resolution; e.g. the system only needs to resolve if the signal is positive or negative. This task can be efficiently done with a regenerative comparator, which provides a full CMOS level output depending on the polarity of the input signal. In this sense, an unstable, highly non-linear



(a) Simplified circuit diagram.



(b) Simplified timing diagram.

Figure 3.3. Simplified circuit diagram of the ΣΔ receiver.

amplifier, is utilized in order to provide loop-gain within the modulator. The design of this comparator will be discussed in section 4.1.4.

A simplified circuit schematic of the ΣΔ receiver is shown in figure 3.3. A transconductance amplifier is needed in order to convert an input RF voltage into current. The current is then down-converted to DC using a passive mixer. The loop filter consists of three capacitors and three switches, which implement a second-order transfer function. Finally, the loop is enclosed by two feedback D/A converters. A feedback compensation scheme for ΣΔ modulator is chosen due to its resilience towards out-of-band blockers [84].

3.1.1 Scaling of the MOS switch

The basic argument that a metal-oxide-semiconductor (MOS) switch has benefited from gate-length scaling is due to the fact that its on conductance scales proportionally with the ratio of gate width over gate length (W/L), while the value of all other undesirable parameters or parasitics scale proportionally with the device area ($W \cdot L$).

It is safe to assume that an MOS switch will be operated in the strong inversion region in order to get the maximum on conductance. In this region, the inversion-layer charge is given as [106]:

$$Q_I = C'_{ox} \cdot W \cdot L \cdot (V_G - V_S - V_T) \tag{3.1}$$

where C'_{ox} is the gate-to-channel capacitance per unit area, V_G and V_S is the gate and source voltage respectively, and finally V_T is the extrapolated threshold voltage of the transistor. The gate voltage V_G is usually connected to the highest voltage available in order to maximize the conductance. Since an MOS device is symmetric with respect to the two ends of the conducting channel, the 'source' of the MOS switch is defined to be the end of the channel with the lower potential voltage.

The on conductance, G_{on}, of the switch is:

$$G_{on} = \mu \cdot C'_{ox} \cdot \frac{W}{L}(V_G - V_S - V_T) \tag{3.2}$$

where μ is the mobility of the carriers within the channel. Finally, the energy required for a single cycle of turning on and off an MOS switch, E_{sw}, can be calculated as (ignoring parasitics):

$$\begin{aligned} E_{sw} &= Q_I \cdot (V_G - V_S - V_T) \\ &= C'_{ox} \cdot W \cdot L \cdot (V_G - V_S - V_T)^2 \end{aligned} \tag{3.3}$$

In order to form an inversion-layer under the oxide with a total charge of Q_I, the same amount of charge has to be provided at the gate electrode. Similarly, when the switch is turned off, the gate has to be discharged. The energy consumed in the process of charging and discharging the gate of an MOS switch is E_{sw}. Subthreshold conduction is neglected

in this analysis, and therefore a gate voltage of $V_S + V_T$ is assumed to be sufficient to turn off the transistor. This assumption is not necessary, however it simplifies the ensuing derivation.

We are now in a position to make some general conclusions regarding scaling of MOS switch. If E_{sw} is normalized with respect to G_{on}, the following equation would result:

$$\frac{E_{sw}}{G_{on}} = L^2 \cdot \frac{(V_G - V_S - V_T)}{\mu} \tag{3.4}$$

The equation above states that for the same on conductance G_{on} the energy required per cycle is reduced quadratically as the gate length of the transistor is reduced. One can incorporate the effects of velocity saturation by a reduction in the carrier mobility μ; which would somewhat reduce the benefit of gate-length scaling.[2] The factor $(V_G - V_S - V_T)$ is an available parameter for circuit designers. This parameter tradesoff the MOS switch maximum signal handling capability with its on conductance.

Charge injection is a concern for precision analog circuits utilizing MOS switches. The severity of errors induced by charge-injection is proportional to the amount of inversion-layer charge [112]. After normalizing the inversion layer charge of an MOS switch with respect to its on conductance, the following expression results:

$$\frac{Q_I}{G_{on}} = \frac{L^2}{\mu} \tag{3.5}$$

A reduction in the minimum allowable gate length would mean that an MOS transistor with a quadratically smaller area can be used in order to achieve the same on conductance. Naturally, a smaller area transistor would contain less amount of inversion-layer charge.

Similar arguments can also be made for reduction in parasitic junction capacitances (to substrate) at the two ends of an MOS switch. The introduction of a new CMOS process usually incorporates a reduction in the minimum allowable diffusion width that is commensurate with the reduction in the transistor gate length. For this reason, a similar quadratic reduction in parasitic junction capacitances can be expected as the gate length

[2]Velocity saturation can be modeled by a drain-source voltage dependent mobility; $\mu(V_{DS}) = \frac{v_{dmax}}{\varepsilon_c + \varepsilon_x}$, where ε_x is the lateral electric field in the channel, v_{dmax} is the saturated carrier velocity, and ε_c is the critical electric field when velocity saturation occurs. [106]

is reduced. This analysis does not take into account the parasitic capacitances between the gate and the source/drain diffusion areas with their metal contacts. In the past, the parasitic capacitance per unit length of the transistor's gate has remained relatively constant across different process generations. However, in the near future, the capacitance per unit length might increase due to an increasing gate-structure height and a closer proximity between the gate and the source/drain metal contacts.

To summarize, MOS switches are a benefactor of CMOS scaling [19]. The availability of better MOS switches enables circuit designers to obtain a better trade-off among operating speed, voltage accuracy or resolution and power. For example in applications where the resolution is limited by charge-injection induced errors, scaling of MOS transistors would enable the use of an MOS switch with a smaller area, thereby reducing the errors related to charge-injection. In another application where a certain settling-time is desired; the use of a smaller MOS switch would allow simultaneous reduction in operating power as well as charge-injection induced errors. Ultimately scaling of MOS switches would be limited by the ever increasing leakage current that exists when the transistors are supposedly in its non-conducting state. Such a case might mandate the use of larger than minimum gate-length transistors in order to keep leakage current to a manageable level.

3.2 Discrete-Time Processing of RF Signals

3.2.1 Sampling Mixer

In this section the operation of a single-balanced, current-switching mixer with a single-ended output is examined. The output signal is mathematically re-formulated to emphasize that the output of a mixer can be interpreted as a sampled-and-held version of the continuous-time input signal [116, 66, 10, 114]. The choice of a single-balanced mixer – where, in one-half of the cycle, the input signal is shorted to ground – is merely for brevity of the ensuing discussions and derivations. The analysis shown below can be easily extended to a differential, double-balanced current-switching mixer as well.

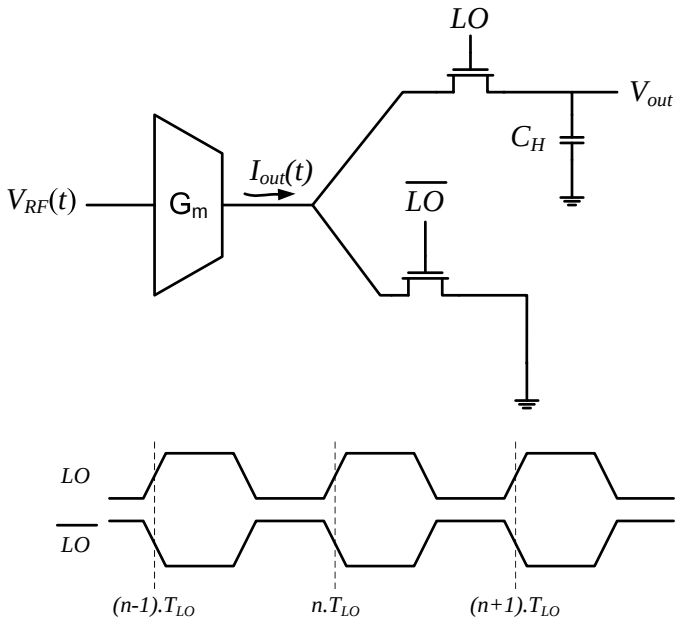


Figure 3.4. Single-balanced passive mixer with single-ended output.

Consider a single-balanced current-switching mixer shown in Figure 3.4. The input transconductance amplifier G_m converts the input voltage $V_{RF}(t)$ into output current $i_{out}(t)$. The large output impedance of the transconductance amplifier forces the resulting current to flow through either of the two switching transistors, depending on the local-oscillator (LO) phase. As a result, the output current i_{out} undergoes frequency downconversion and the resulting output is taken as a voltage accross the capacitor C_H.

The output voltage V_{out} is naturally segmented into two phases that are periodic in time. In the first phase, the transconductance amplifier is sourcing current into C_H, and therefore actively changing the output voltage V_{out}. In the second phase, where the transconductance amplifier is disconnected from C_H, the capacitor C_H is isolated from any external input, and the output voltage V_{out} is being held constant. These two phases can be referred to as the sample phase and the hold phase, respectively.

Let us define a discrete-time series $v_{out}[n]$, which describes the voltage $V_{out}(t)$ sampled during the hold phase of each LO period.

$$v_{out}[n] = \frac{q_{in}[n]}{C_H} + v_{out}[n-1] \tag{3.6}$$

$$q_{in}[n] = G_m \cdot \int_{nT_{LO}}^{nT_{LO}+\frac{T_{LO}}{2}} V_{RF}(\tau) \cdot d\tau \tag{3.7}$$

The formulation above divides the circuit operation into two parts. The first part is a charge-sampling operation, in which a charge packet $q_{in}[n]$ is created on each sampling instant [67]. The second-part implements a discrete-time integrator, in which incoming charge packets from each sampling instant are continuously added to a running-sum. In the frequency domain, an integrator realizes a low-pass filter.

The charge packet $q_{in}[n]$ can be further reformulated as a continuous-time convolution between the input signal $V_{RF}(t)$ and a pre-filter, or a windowing function $p(t)$.

$$q_{in}[n] = G_m \cdot \frac{T_{LO}}{2} \cdot \int_{-\infty}^{nT_{LO}+\frac{T_{LO}}{2}} V_{RF}(\tau) \cdot p\left(\left(nT_{LO} + \frac{T_{LO}}{2}\right) - \tau\right) \tag{3.8}$$

$$p(t) = \begin{cases} \frac{2}{T_{LO}}, & \text{if } 0 \leq t \leq \frac{T_{LO}}{2} \\ 0, & \text{otherwise} \end{cases} \tag{3.9}$$

The formulation above emphasizes that each charge-packet $q_{in}[n]$ is, in itself, a result of a two-step process: a continuous-time filtering of the input $V_{RF}(t)$ followed by an impulse-sampling operation. The pre-multiplication by the factor $\frac{2}{T_{LO}}$ to the filter $p(t)$ normalizes the DC gain of the filter to 0-dB. Furthermore, in this manner, the term $\frac{G_m \cdot T_{LO}}{2}$ in equation 3.8 simply denotes the voltage-to-charge-packet conversion gain of the mixer at DC.

The frequency response of the pre-filter $p(t)$, denoted $H_p(\Omega)$, is shown in Figure 3.5. This filter attenuates signals located at even-multiples of the LO frequency f_{LO}, and passes signals located at odd-multiples of f_{LO}. In other words, the pre-filter $p(t)$ implements a (partial) anti-aliasing filter needed prior to the sampling operation. The filter gain at frequency f_{LO} can be calculated to be $\frac{2}{\pi}$. Sampling the resulting signal at a rate of f_{LO} would finally downconvert the signal at frequency f_{LO}, and consequently all other signals at integer multiples of f_{LO}, to baseband. This re-formulation is consistent with what is expected as the output of a current-switching mixer. In a current-switching mixer, signals located at odd-harmonics of f_{LO} will be susceptible to folding, but signals located at even-harmonics of f_{LO} will not be susceptible to folding.

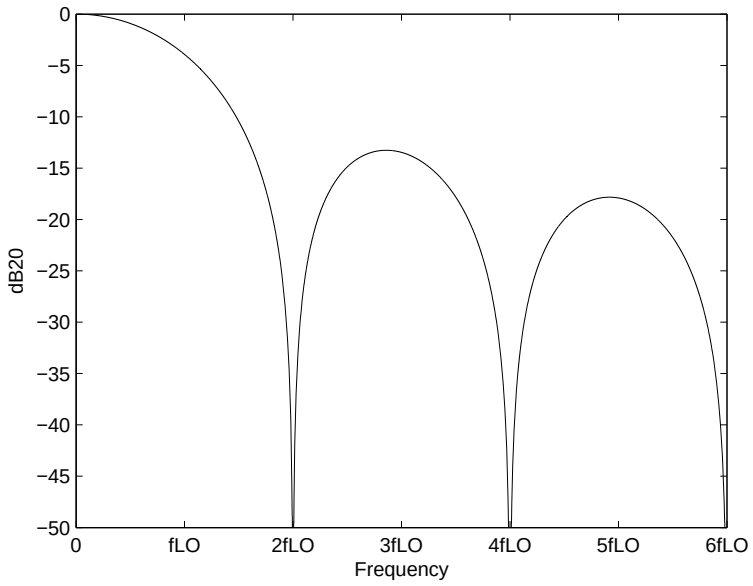


Figure 3.5. Frequency response of anti-alias pre-filter $p(t)$.

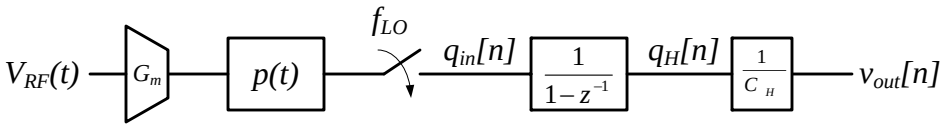


Figure 3.6. Signal flow-graph diagram of a sampling mixer.

Figure 3.6 displays a step-by-step process in forming the output voltage $v_{out}[n]$ using the formulation developed in this section.

The analysis presented in this section recasts a current-commutating mixer circuit as a sampler, complete with a built-in anti-aliasing filter. It is worthwhile to stress the importance of this observation. Traditionally, a sample-and-hold circuit is needed prior to a switched-capacitor filter. It is needed in order to sample new input signals on one phase, and to hold that value constant over the next phase for further processing. This sample-and-hold circuit consumes a lot of power and is usually the bottleneck for achieving higher speed of operation or better linearity. This analysis demonstrates that a mixer, which is already present in most RF receivers, also performs the same function.

This section also introduces the concept of a charge packet [67]. A charge-packet is a

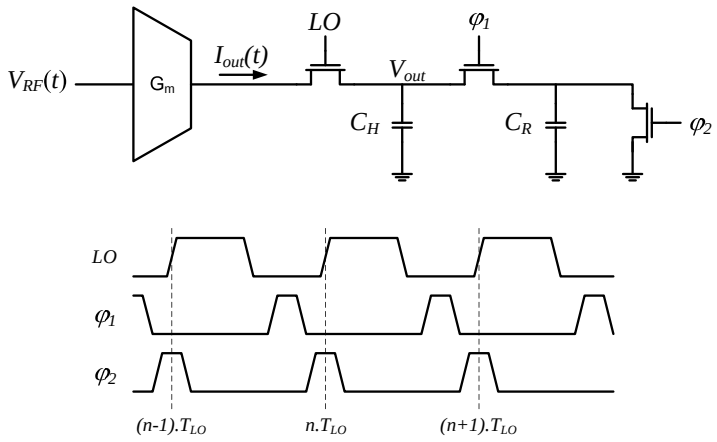


Figure 3.7. Lossy discrete-time integrator.

non-observable quantity, and, as the name implies, it is simply a signal expressed in the charge-domain. As will be seen in the sections to follow, charge-domain analysis lends itself naturally in understanding various switched-capacitor filter topologies [46]. As a result, the succeeding analysis will be done completely in the charge domain, with an appropriate conversion done at the input and output of the system, in order to relate the resulting charge-domain equations to observable quantities such as input and output voltages.

3.2.2 IIR Filter Synthesis

As mentioned before, the circuit given in Figure 3.4 contains both a discrete-time integrator and a sampler circuit. A capacitor C_{H1} forms a discrete-time integrator simply because it keeps a running-sum of input charge-packets over time. This statement can be formalized as follows; let us define $q_H[n]$ as the total charge contained within capacitor C_H at sample-time n. Therefore :

$$q_H[n] = q_H[n-1] + q_{in}[n] \tag{3.10}$$

The transfer function in the z-domain is :

$$\frac{Q_H(z)}{Q_{in}(z)} = \frac{1}{1-z^{-1}} \tag{3.11}$$

which is a transfer function of an ideal discrete-time integrator.

A lossy discrete-time integrator can be created by adding a second, smaller capacitor C_R to the same circuit. This is illustrated in Figure 3.7.[3] During φ_2, C_R is connected to ground, thus resetting the charge contained within it to zero. During φ_1, C_R is connected to C_H, and charge-sharing occurs in order to obtain voltage equilibrium between the two capacitors. The charge contained within C_H after equilibrium is:

$$q_H[n] = \alpha \cdot q_H[n-1] + q_{in}[n] \tag{3.12}$$

or equivalently, it can be expressed in the z-domain as:

$$\frac{Q_H(z)}{Q_{in}(z)} = \frac{1}{1-\alpha z^{-1}} \tag{3.13}$$

where $\alpha = \frac{C_H}{C_H+C_R}$, a value which is always smaller than unity. By connecting the two capacitors together, a part of the charge that originally resides in C_H is now transferred to C_R, creating a loss factor in an otherwise lossless integrator. Since C_R is subsequently reset to zero, the charge within C_R is forever removed from the system. The parameter α determines the DC gain of the integrator, or similarly the quality factor of the integrator. This parameter also determines the 3-dB bandwidth of the resulting first-order low-pass filter. In this chapter, the term loss factor will be used to refer to the α parameter.

The output of the lossless and lossy integrators above is typically taken as an output voltage. The output voltage $v_{out}[n]$ is :

$$v_{out}[n] = \frac{q_H[n]}{C_H} \tag{3.14}$$

The overall input-output voltage conversion gain G_c for a narrow-band input signal at frequency f_{LO} can be calculated as :

$$G_c = \underbrace{\frac{G_m T_{LO}}{2}}_{\substack{V\rightarrow Q \\ conv.\ gain\ at\ DC}} \cdot \underbrace{\frac{\pi}{2}}_{H_p(f_{LO})} \cdot \underbrace{\frac{1}{1-\alpha_1}}_{\substack{DT\ integrator \\ gain\ at\ DC}} \cdot \underbrace{\frac{1}{C_H}}_{\substack{Q\rightarrow V \\ conversion}} \tag{3.15}$$

Equation 3.15 consists of four terms. The first and the last terms are the voltage-to-charge conversion gain at DC and the charge-to-voltage conversion gain, respectively. The second term represents the frequency response of the pre-filter $p(t)$. And last, the third term

[3]For brevity, the $\overline{LO}$ switch is omitted in this figure and all subsequent figures

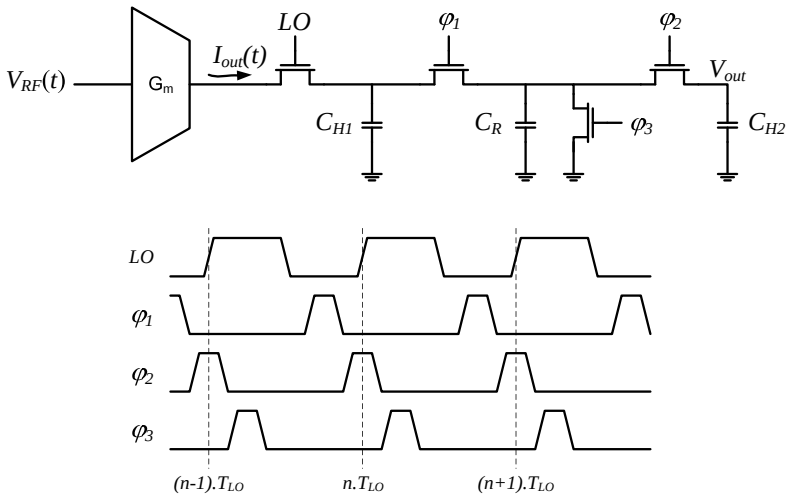


Figure 3.8. A cascade of two lossy discrete-time integrators.

is the gain of the discrete-time integrator at DC, or equivalently, equation 3.13 evaluated at $z = 1$.

Based on equation 3.15, an ideal sampling mixer, as shown in Figure 3.4, would have an infinite conversion gain. However, as will be shown in section 3.2.4, any realizable transconductance amplifier would have a finite output resistance, which would limit the achievable conversion gain.

Next, a mechanism to cascade two discrete-time integrators is needed in order to build a general IIR filter transfer function. The connection between the output of one integrator to the input of another has to be established without the need for any additional active element, such as a transconductance amplifier. This task can be accomplished by using one additional capacitor. In this role, the capacitor actually acts as a vessel in which charge-packets can be transported between two different integrators.

Figure 3.8 shows a cascade of two lossy integrators. The two capacitors C_{H1} and C_{H2} act as the first and second integrator respectively; while a third, and usually much smaller, capacitor C_R is used to link the two integrators together. In the first phase, φ_1, a discharged capacitor C_R is connected to capacitor C_{H1}. This process makes the first integrator lossy, with a loss factor of $\alpha_1 = \frac{C_{H1}}{C_{H1}+C_R}$. The amount of charge stored in capacitor C_R at the

end of φ_1 is proportional to the output of the first integrator $q_{H1}[n]$.

$$q_R[n] = \beta \cdot q_{H1}[n] \tag{3.16}$$

where

$$\beta = \frac{C_R}{C_{H1} + C_R} = 1 - \alpha \tag{3.17}$$

In the next phase, φ_2, capacitor C_R is connected to the second integrating capacitor C_{H2}. At this point, it might be helpful to (conceptually) make the distinction between the capacitor C_R as an empty charge-carrying vessel, and the charge packet $q_R[n]$ contained within it. As a discharged capacitor, C_R would make the second integrator lossy, with a loss factor of $\alpha_2 = \frac{C_{H2}}{C_{H2}+C_R}$. However, capacitor C_R contains an input charge packet $q_R[n]$, whose value is proportional to the output of the first integrator. Thus, in the latter role, capacitor C_R acts to relay the output of the first integrator to the input of the second integrator. The factor β indicates the gain between the two integrator stages. The term interstage gain will be used subsequently to refer to this parameter.

In the next phase, φ_3, capacitor C_R is reset, and the sequence repeats from the first phase φ_1. If a third integrator is to be cascaded, capacitor C_R can be connected to a fourth capacitor C_{H3} instead. Thus, a general mechanism of cascading multiple lossy integrators is realized.

The resulting signal flow-graph diagram for the two cascaded integrators is shown in Figure 3.9. The overall input-output voltage conversion gain G_c for a narrow-band input signal at frequency f_{LO} can be calculated as :

$$G_c = \underbrace{\frac{G_m T_{LO}}{2}}_{\substack{V\to Q \\ conv.\ gain\ at\ DC}} \cdot \underbrace{\frac{\pi}{2}}_{H_p(f_{LO})} \cdot \underbrace{\frac{1}{1-\alpha_1} \cdot \beta \cdot \frac{1}{1-\alpha_2}}_{\substack{Discrete-time\ filter \\ gain\ at\ DC}} \cdot \underbrace{\frac{1}{C_{H2}}}_{\substack{Q\to V \\ conversion}} \tag{3.18}$$

The method outlined above is by no means limited to an integrator with one input and one output. Multiple capacitors, each of which has a similar role to C_R, can be used to carry a plurality of input and output charge packets to and from a single integrating capacitor. Furthermore, the interstage gain β can also be negated by simply flipping the polarity of the capacitor C_R. This can be easily accomplished using cross-connected switches in a differential implementation.

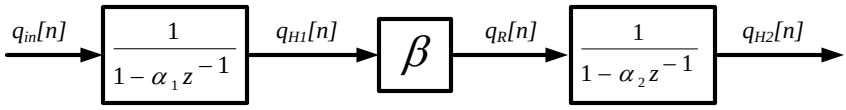


Figure 3.9. Signal flow-graph diagram of a cascade of two integrators.

At this point a major limitation of this passive filtering approach should become apparent. Propagation of signal in the filter is accomplished by physically moving charge from one integrator to the next. In other words, each integrator in the filter loses a fraction of its total charge on each sampling period, thus making it a lossy integrator ($\alpha < 1$). In fact, as shown in equation 3.17, the sum of the loss factor α and the interstage gain β of each integrator within the filter has to be equal to unity. This fact is a direct result of the charge conservation principle. The charge lost on each integrator acts as an input to the next integrator. For this reason, there is an inherent trade-off between the interstage gain between integrators and the quality factor of each integrator. In order to keep the integrator loss to a minimum, which is desired in many cases, then the interstage gain has to be kept very small.

The trade-off between the loss factor and the interstage gain does not become much of a problem if the IIR filter can be expressed as a feed-forward connection of integrators. The limitation would simply manifest itself as a limitation on the pass-band gain of the filter, which can be compensated for elsewhere. However, this trade-off poses a severe problem for other IIR filter structures, such as resonators, that inherently requires feedback connections. In this case the trade-off between having a low-loss integrator and a high interstage gain greatly limits the possible placement of poles and zeros, thereby significantly limiting the range of transfer functions that can be synthesized. For example, resonators with a reasonably high Q-factor cannot be created using this passive switched capacitor approach.[4] For this reason, an IIR filter using passive circuits is best suited for low-pass

[4]A resonator Q-factor is defined as the ratio between the resonator's center frequency to its bandwidth. Multi-rate techniques can also be utilized to synthesize a bandpass filter consisting of two time-interleaved low-pass filter [111, 77, 114].

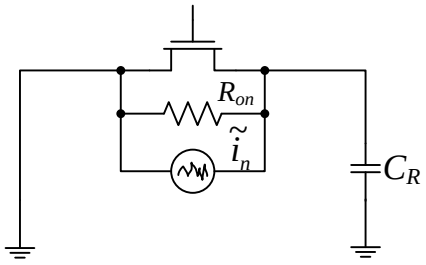


Figure 3.10. Noise on a single switched capacitor

filtering, where the natural frequency response of an integrator can be used without much of a modification.

3.2.3 Noise in Switched-Capacitor Filters

Noise in a passive switched-capacitor filter originates from the thermal noise within each of the constituent MOS switches. The total noise at the filter's output can be obtained by simply enumerating all the MOS switches in the filter and determining the noise transfer function from each MOS switch to the output [28].

Consider the circuit shown in Figure 3.10, which consists of one capacitor and one MOS switch. Noise generated in the reset phase of an IIR filter discussed previously can be modeled with this circuit. When the MOS switch is on, its inversion channel creates a connection between the top and bottom plates of the capacitor. Ideally this connection would short the two capacitor plates, therefore depleting all the charge stored within the capacitor C_R. However, thermal noise generated within the transistor's channel prevents this from happening perfectly. Since an MOS switch has a finite conductance, it is also susceptible to thermal energy fluctuation. This effect can be modeled as a noise current source in parallel with the MOS switch as shown in Figure 3.10 [110].

Noise generated inside the switch would continuously modulate the voltage across the capacitor C_R. At the instant when the switch is opened, the connection between the two plates and the noise source is cut off. The instantaneous noise charge stored within the capacitor remains in the capacitor C_R, effectively sampling the noise process $\tilde{i}_n$ at the exact

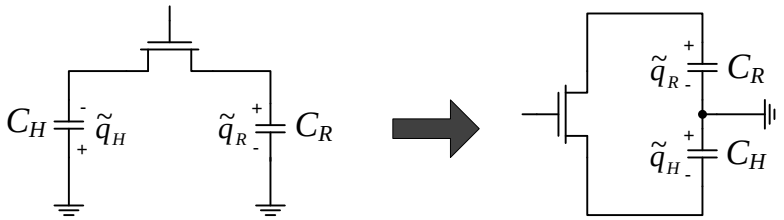


Figure 3.11. Noise on two switched capacitors

instant the switch is turned off. To quantify the preceding description, the on resistance of the MOS, R_{on}, and the capacitor C_R forms a low-pass filter. The total integrated noise represented as a voltage across the capacitor C_R has a variance of:

$$\begin{aligned} var(\tilde{v}_o) &= \int_0^\infty 4kTR_{on} \left| \frac{1}{1 + 2\pi j f R_{on} C_R} \right|^2 df \\ &= \frac{kT}{C_R} \end{aligned} \tag{3.19}$$

Where k is Boltzmann's constant and T is the temperature. The resulting discrete-time noise process has a flat power spectral density across frequency $(-\frac{f_s}{2}, \frac{f_s}{2})$, where f_s is the sampling frequency [45]. The noise voltage $\tilde{v}_o$ can be equivalently represented as a noise charge packet $\tilde{q}_R$ with a variance of kTC_R. This noise charge packet is stored within C_R and is generated every time C_R is reset. By casting the discrete-time noise process as a charge-packet generation mechanism, the noise source can be easily incorporated into the analysis framework developed so far.

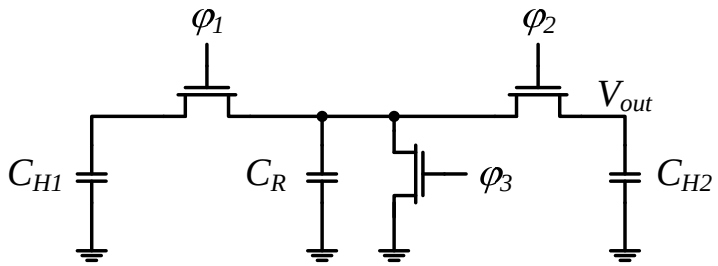
The same noise analysis can also be easily extended to cases where an MOS switch connects two capacitors together, as shown in Figure 3.11. When the MOS switch is turned on, it completes a loop which contains the two capacitors C_H and C_R in series with each other. Therefore, the MOS switch is effectively connected to an equivalent series capacitor of size $C_H||C_R = \frac{C_H \cdot C_R}{C_H + C_R}$. The noise voltage across this equivalent series capacitor has a variance of $\frac{kT}{C_H||C_R}$. Thus, each capacitor C_H and C_R contains an identical noise charge packet of variance $kT(C_H||C_R)$, with the polarity shown in Figure 3.11.

It turns out that noise analysis of these two seemingly simple circuits is sufficient to analyze and explain noise generation and propagation in more complicated switched-capacitor

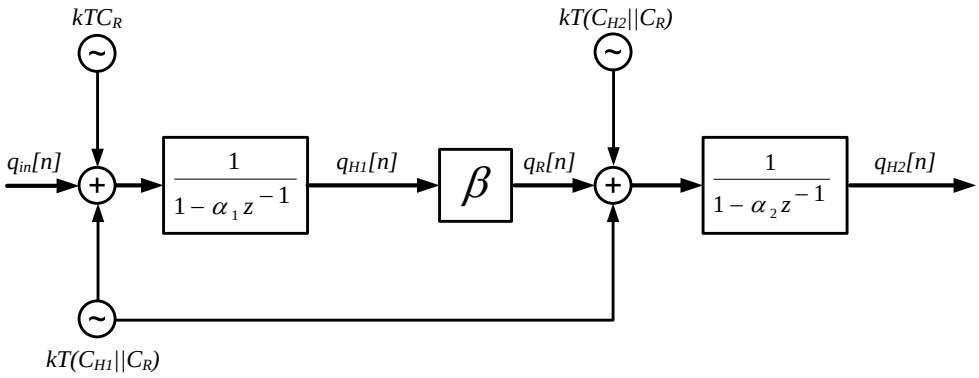
circuits. To illustrate this point, we will analyze an example circuit of a second-order, low-pass filter, which is shown earlier in Figure 3.8. Recall that this filter is a cascade of two lossy integrators; the first is composed of capacitor C_{H1}, and the second is composed of capacitor C_{H2}. A discrete-time signal flow-graph diagram has been developed and shown in Figure 3.9; the intention here is to incorporate the various noise sources into this diagram.

There are three MOS switches in the IIR filter circuit, and therefore there are three independent noise sources that need to be accounted for. The first noise source comes from the φ_3 switch. This switch would generate a noise charge packet of variance kTC_R which is then stored within capacitor C_R. Because the capacitor C_R is subsequently connected to capacitor C_{H1}, the noise charge packet generated during φ_3 will act as an input charge packet to the first discrete-time integrator. Second, during φ_2 phase, two noise charge packets of variance $kT(C_R||C_{H2})$ are generated and stored in C_{H2} and C_R. The first noise charge packet, stored in C_{H2}, can be easily modeled as an input to the second integrator. The noise charge packet in C_R generated during φ_2 is immaterial, because in the next phase φ_3, the capacitor C_R is reset. The last noise source is generated during the φ_1 phase. As in the φ_2 phase, two noise charge packets of variance $kT(C_R||C_{H1})$ are created, and stored within capacitors C_{H1} and C_R. The noise charge packet stored within C_{H1} can also be considered as an input to the first integrator. The noise charge packet in C_R will act as an input to the second integrator, since in the next phase, φ_2, capacitor C_R is connected to capacitor C_{H2}. It is very important to realize that the last two noise charge packets are a manifestation of the same noise process, namely one that originated from the thermal energy fluctuation within switch φ_1. For this reason, the noise source generated during φ_1, is most appropriately represented by a single noise source that is injected at two different locations in the signal flow-graph diagram. The polarity with which the noise source is injected is also of importance, as the incorrect polarity would alter the noise transfer function to the output. The updated signal flow-graph diagram, with the noise sources included, is shown in Figure 3.12(b).

Simulation of switched-capacitor noise can be performed using a combination of periodic steady-state (PSS) and periodic noise (PNOISE) analyses, which are available as part of



(a)



(b)

Figure 3.12. Noise in a second-order IIR filter: (a) circuit schematic; (b) signal flow-graph diagram.

Cadence SpectreRF circuit-simulation suite [101]. Periodic steady-state analysis is originally intended to analyze continuous-time circuit with periodic input signals or excitations. In order to simulate a switched-capacitor circuit appropriately, one needs to recognize that the output of a switched capacitor circuit is a discrete-time, instead of a continuous-time signal. This discrete-time signal should be treated as the output of the circuit sampled after it has settled to the final value for each sampling period. There are two techniques that one can use in order to force the simulator to evaluate the output signal correctly in the manner described [45]. First, in more recent versions of SpectreRF, PNOISE analysis provides a specialized time-domain analysis method that can be invoked by setting a simulation option `noisetype=timedomain`. By enabling this option, the simulator would only analyze noise at particular time instants parameterized by another simulation variable `noisetimepoints`. Second, on older versions of spectreRF, an explicit (ideal) sample-and-hold block can be used to similarly force the simulator to only evaluate the output of the circuit at the correct time-instants. Recall that a sample-and-hold would impose a zero-order-hold on a discrete-time signal; thus, the resulting sinc-shaped response in the frequency domain has to be compensated for.

3.2.4 Circuit Parasitics

The design of the input transcondutor circuit (G_m) has a large impact on the overall performance of the discrete-time filter. This section will focus on modeling the various non-idealities of the input transconductance amplifier and analyzing their impact on the overall filter transfer function. As in the previous sections, the goal is to incorporate the various circuit impairments to the analytical framework that has been developed so far.

The ideal transconductance amplifier would have zero output capacitance, denoted C_{par}, and an infinite output resistance, denoted R_{par}. The effect of a non-zero output capacitance can be easily incorporated into the analysis framework developed in section 3.2.2. On each sampling instant, charge sharing will occur between capacitor (C_{par}) and capacitor (C_H). Therefore, the integrator formed by capacitor C_H will become lossy, with a loss factor of $\alpha_C = \frac{C_{par}}{C_{par}+C_H}$.

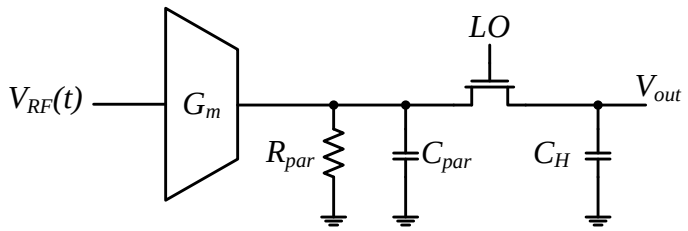


Figure 3.13. Input transconductance amplifier with finite output resistance and non-zero output capacitance

The presence of a finite transconductance amplifier output resistance, R_{par}, can be analyzed by starting with the differential equation that describes the circuit:

$$G_m V_{in}(t) = \frac{q_H(t)}{C_H R_{par}} + \frac{dq_H(t)}{dt} \tag{3.20}$$

Solving the differential equation above and sampling the resulting function at the correct time instants would result in the following equation:

$$q_H[n] = e^{-\frac{T_{LO}}{2R_{par}C_H}} \cdot q_H[n-1] + G_m \cdot \int_{nT_{LO}}^{nT_{LO}+\frac{T_{LO}}{2}} V_{RF}(\tau) \cdot e^{\frac{nT_{LO}+\frac{T_{LO}}{2}-\tau}{R_{par}C_H}} \cdot d\tau \tag{3.21}$$

Or, equivalently:

$$q_H[n] = \alpha_R \cdot q_H[n-1] + q_{in}[n] \tag{3.22}$$

where:

$$\alpha_R = e^{-\frac{T_{LO}}{2R_{par}C_H}} \tag{3.23}$$

$$q_{in}[n] = G_m \cdot \int_{nT_{LO}}^{nT_{LO}+\frac{T_{LO}}{2}} V_{RF}(\tau) \cdot e^{\frac{nT_{LO}+\frac{T_{LO}}{2}-\tau}{R_{par}C_H}} \cdot d\tau \tag{3.24}$$

The variable α_R is equivalent to the loss factor α, which is defined in section 3.2.2. It is simply a mathematical formulation to describe the amount of charge lost per sampling period. During the period when LO is high, current will flow through resistor R_{par}, which will slowly deplete the charge stored within capacitor C_H. Therefore, for each sampling period, a part of the charge inside capacitor C_H is lost.

The loss factor, α_R, can be combined with other loss mechanisms, such as one due to connecting and disconnecting a second capacitor, C_R (Figure 3.7), to result in an effective

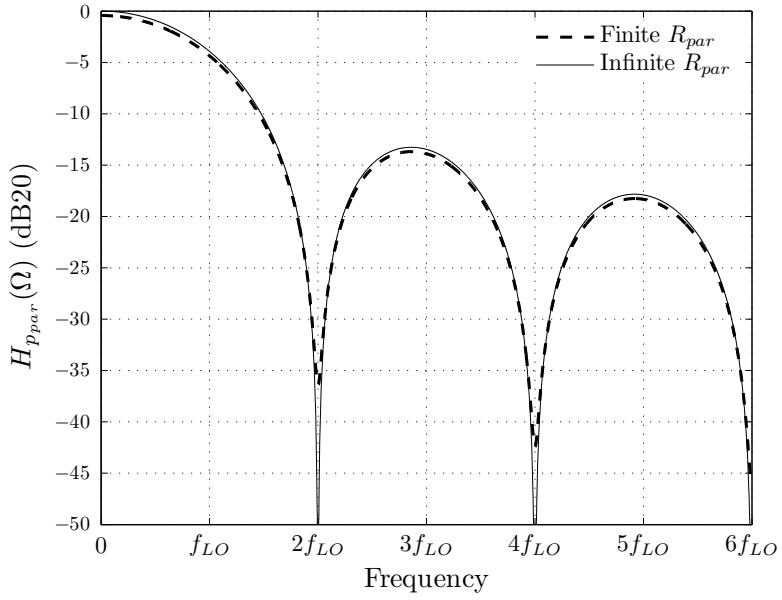


Figure 3.14. Impact of transconductance amplifier finite output resistance

loss factor α_{eff}. The effective loss factor α_{eff} can be computed by enumerating the total charge lost per period as a fraction of the total charge within capacitor C_H.

The generation of charge packet $q_{in}[n]$ in this scenario, can be similarly formulated as a convolution or a filtering operation between the continuous-time input signal with a windowing function (equation 3.9). In this case, the windowing function is:

$$p_{par}(t) = \begin{cases} \frac{2}{T_{LO}} \cdot e^{-\frac{t}{R_{par} \cdot C_H}}, & \text{if } 0 \leq t \leq \frac{T_{LO}}{2} \\ 0, & \text{otherwise} \end{cases} \tag{3.25}$$

The presence of a finite output resistance R_{par} modifies the anti-alias filter $p(t)$ to be the function $p_{par}(t)$. Note that, as R_{par} approaches infinity, the function $p_{par}(t)$ degenerates into the original anti-aliasing filter function $p(t)$. A comparison between the frequency response of the original pre-filter $p(t)$ and the resulting pre-filter $p_{par}(t)$ with a finite transconductance amplifier output resistance, R_{par}, is shown in Figure 3.14.

With the addition of the effect of finite transconductance amplifier output resistance,

the voltage conversion-gain formula from equation 3.15 can be updated as follows:

$$G_c = \frac{G_m T_{LO}}{2} \cdot H_{p_{par}}(f_{LO}) \cdot \frac{1}{1-\alpha_R} \cdot \frac{1}{C_H} \tag{3.26}$$

When R_{par} is sufficiently large, then $\frac{T_{LO}}{2R_{par}C_H}$ is much smaller than unity. If such is the case, then the following approximation can be used:

$$\frac{1}{1-\alpha_R} = \frac{1}{1-e^{-\frac{T_{LO}}{2R_{par}C_H}}} \approx \frac{2R_{par}C_H}{T_{LO}} \tag{3.27}$$

Therefore, the conversion gain from equation 3.26 can be approximated as:

$$G_c \approx \frac{G_m T_{LO}}{2} \cdot \frac{2}{\pi} \cdot \frac{2R_{par}C_H}{T_{LO}} \cdot \frac{1}{C_H} = \frac{2}{\pi} \cdot G_m \cdot R_{par} \tag{3.28}$$

This result is hardly surprising; it is identical to the conversion gain of a mixer.

It is important to realize that, in reality, the resistance R_{par} is not a physical resistance; it is merely a small-signal approximation. As such, the resistance value is susceptible to process, voltage and temperature variation. More importantly, the value of this resistance is signal dependent, which causes distortion. For this reason, although it is able to, R_{par} is rarely used as a parameter that sets the important filter parameters, such as bandwidth and gain. A filter circuit with a lossy integrator (Figure 3.7) is more widely used. The transconductance amplifier can be designed such that the effective loss factor $\alpha_{eff} \approx \frac{C_H}{C_H+C_R}$, which necessitates $R_{par}C_H \gg \frac{T_{LO}}{2}$. In this manner, the critical filter parameters, such as in-band gain and bandwidth, are purely determined by the ratio of capacitances, instead of being determined by the value of R_{par}. The disadvantage of such an approach is that the conversion gain of the circuit will be significantly reduced.

The load of the transconductance amplifier circuit consists of an MOS sampling switch and a switched-capacitor filter. This load circuit is actually a discrete-time system. As such, its frequency response is periodic in the continuous-frequency axis, with a period equal to the sampling frequency f_{LO}. This fact is illustrated in Figure 3.15. The overall frequency response of the circuit is a result of a pre-filtering operation with a windowing function $p(t)$, followed by a discrete-time low-pass filter with a sampling frequency of f_{LO}.

A beneficial consequence of the above concept is the fact that the low-pass filtering in the load circuit can be transformed back as a bandpass filtering at the output of the

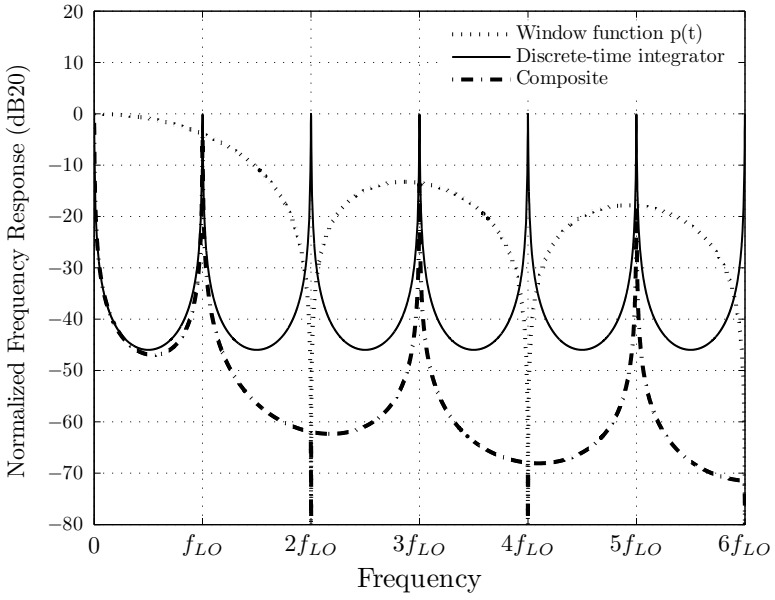


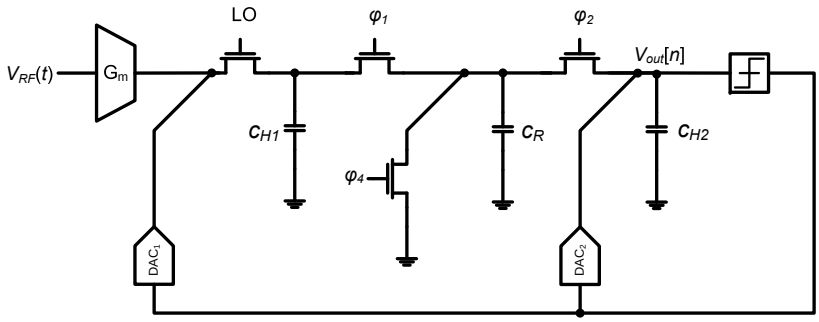
Figure 3.15. Frequency response of passive mixer

transconductance amplifier [20]. If the voltage-drop across the sampling switch is kept small, then the output voltage of the transconductance amplifier is set by the voltage across the capacitor C_H. However, the voltage across capacitor C_H only emerges after the discrete-time filtering operation. Thus, if a large out-of-band blocker were to impinge the transconductance amplifier, it would be filtered before it could cause large voltage swing at the output of the transconductance amplifier.

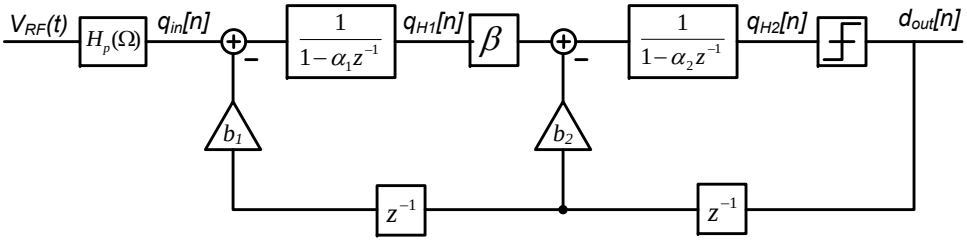
Finite rise- and fall-time of the LO signal would also affect the frequency response of the anti-alias pre-filter $p(t)$. This impairment can be modeled by modifying the impulse response $p(t)$ to have a trapezoidal shape, instead of a perfect rectangle. The overall impact is similar to that of a finite output impedance, in that it limits the rejection at even multiples of LO frequency.

3.3 System Design

The previous section presented design methodologies and the necessary tools to analyze the building blocks of a $\Sigma\Delta$ receiver. In this section, the tools developed in section 3.2



(a)



(b)

Figure 3.16. Second-order ΣΔ modulator: (a) circuit schematic; (b) signal flow-graph diagram.

is used in deriving the optimal circuit parameters and component sizing. In line with the methodologies developed thus far, the analysis is done using the notion of charge packet, which is a discrete-time, charge-domain quantity. A sampling gain function presented in equation 3.8 is used in order to refer any charge domain value to a continuous-time, voltage-domain signal at the input of the overall system.

3.3.1 Sigma-Delta Modulator Design

The frequency characteristics of a ΣΔ modulator is set by ratios of component parameters, all of which will be discussed in this section. The signal and noise transfer function responses are set by the ratio between capacitances of $\frac{C_R}{C_{H1}}$ and $\frac{C_R}{C_{H2}}$ as well as the ratio of the reference values for the two feedback D/A converters. The absolute value of the feedback D/A converters reference signal determines the full-scale range of the modulator.

A passive, second-order ΣΔ modulator used in the receiver is shown in figure 3.16. The

parameters shown in the system model (section 3.2) is repeated below for convenience:

$$\begin{aligned}\alpha_1 &= \frac{C_{H1}}{C_{H1}+C_R} \\ \alpha_2 &= \frac{C_{H2}}{C_{H2}+C_R} \\ \beta &= \frac{C_R}{C_{H1}+C_R}\end{aligned} \tag{3.29}$$

The parameter b_1 and b_2 determines the reference value for the first and second feedback D/A converters respectively. The signal and quantization noise transfer functions relating to this particular second-order modulator are:

$$STF(z) = \frac{\beta}{D(z)} \tag{3.30}$$

$$NTF(z) = \frac{(1-\alpha_1 z^{-1})\cdot(1-\alpha_2 z^{-1})}{D(z)} \tag{3.31}$$

where the common denominator $D(z)$ is

$$D(z) = 1-(\alpha_1+\alpha_2-b_2)z^{-1}+(\alpha_1\alpha_2+b_1\beta-b_2\alpha_1)z^{-2} \tag{3.32}$$

The modulator is designed such that the signal transfer function (STF) is flat across frequencies. In other words, the modulator is designed such that $D(z)=1$. This requirement requires the value of b_1 and b_2 to be:

$$b_1 = \frac{\alpha_1^2}{\beta} \tag{3.33}$$

$$b_2 = \alpha_1+\alpha_2 \tag{3.34}$$

The forward gain of the modulator is β across all frequencies, which is much smaller than unity. In fact, from section 3.2.2, the parameter β comes about because of a charge transfer necessary in order to connect the two stages of the loop filter. The feedback parameter b_1 is adjusted by a factor of $\frac{1}{\beta}$ because it is applied prior to the forward gain of β.

In this one-bit modulator, the frequency responses of the modulator is only set by the *ratio* of the feedback parameters b_1 and b_2. The gain of a one-bit quantizer is undefined, as it takes an input of arbitrary magnitude and outputs a valid logic level representing only the polarity of the input signal. As a result the signal gain between the input of the comparator to the outputs of the two feedback D/A converters are determined solely by the reference

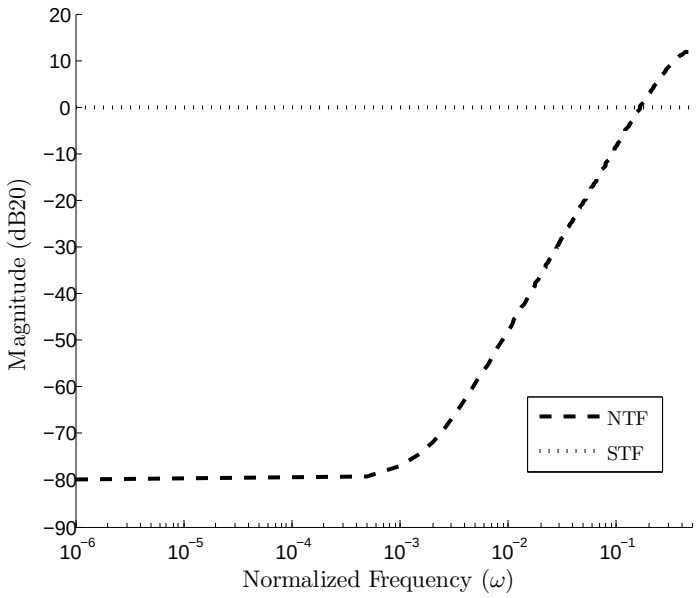


Figure 3.17. Signal and noise transfer functions of a passive second-order ΣΔ modulator.

levels of the two one-bit feedback D/A converters. The reference levels for the two feedback D/A converters effectively sets the full-scale range of the modulator.

The ratio between the two feedback parameters b_1 and b_2 is completely determined by the parameters of the switched-capacitor filters, namely α_1, α_2 and β. The ratio between the two feedback parameters is:

$$\frac{b_1}{b_2} = \frac{\alpha_1^2}{\beta \cdot (\alpha_1 + \alpha_2)} \tag{3.35}$$

The three parameters α_1, α_2 and β are chosen to have the following values:

$$\begin{aligned} \alpha_1 &= 0.99 \\ \alpha_2 &= 0.99 \\ \beta &= 0.01 \end{aligned} \tag{3.36}$$

which implies the following capacitance ratios:

$$\begin{aligned} C_{H1} &= C_{H2} \\ \frac{C_R}{C_{H1}} &= \frac{1}{100} \end{aligned} \tag{3.37}$$

Table 3.2. Achievable SNR from a second-order $\Sigma\Delta$ A/D with a passive loop-filter.

Oversampling Ratio	Achievable SNR
500	84dB
250	80dB
125	74dB
50	61dB

These values are chosen in order to have a sufficient loop gain, while at the same time maintaining a reasonable and realizable capacitance ratio of 100.

The resulting signal and noise transfer function for this modulator is shown in figure 3.17. Because of the lossy nature of the loop filter, the NTF does not have infinite rejection at DC. Furthermore, a maximum rejection of 80dB is achieved, because of the presence of two integrators, each with a DC gain of 100. The DC gain of each integrator is simply $\frac{1}{1-\alpha}$. A table of listing the achievable SNR for a given oversampling ratio for this modulator is given in table 3.2.

The preceding analysis has been done completely in the charge domain. In order to establish the absolute values for the feedback parameters b_1 and b_2, a voltage-to-charge-packet conversion gain needs to be established. Such a function has been derived in section 3.2, and is repeated here for convenience:

$$G_{V\rightarrow Q} = \underbrace{\frac{G_m T_{LO}}{2}}_{\substack{V\rightarrow Q \\ conv.\ gain\ at\ DC}} \cdot \underbrace{\frac{\pi}{2}}_{H_p(f_{LO})} \tag{3.38}$$

Equation 3.38 states that for a 1-V input signal, a charge-packet of size $\frac{\pi}{2} \cdot \frac{G_m T_{LO}}{2}$ Coulomb is created on each sampling period. Equivalently, if the modulator is designed to have an input full-scale range of $V_{RF(FS)}$ Volts, then the charge-packet input to the modulator on each sampling period is:

$$Q_{in(FS)} = \frac{\pi}{2} \cdot \frac{G_m T_{LO}}{2} \cdot V_{RF(FS)} \tag{3.39}$$

In order for the first feedback D/A converter to be able to track input charge-packets of this magnitude, then its reference signal has to have a magnitude of at least $Q_{in(FS)}$. If the feedback D/A is to be implemented as a current-switching D/A converter, then the

reference current should be:

$$\begin{aligned} I_{FB1_{REF}} &= \frac{Q_{in(FS)}}{T_{REF}} \\ &= G_m \cdot V_{RF(FS)} \cdot \frac{\pi}{4} \cdot \frac{T_{LO}}{T_{REF}} \end{aligned} \tag{3.40}$$

where T_{REF} is the time where the control signals are activated; e.g. $T_{LO} = T_{REF}$ for a full non-return to zero D/A converter. The reference value for the second feedback D/A converter is then obtained by scaling $Q_{in(FS)}$ by $\frac{b_1}{b_2}$.

There are two parameter values yet to be determined: the absolute values of transconductance G_m and capacitance C_{H1}. These two values will be determined in the next two sections.

3.3.2 Capacitor Sizing

The sizing of the loop filter capacitor is determined solely by noise considerations. A model for the second-order, low-pass filter with the relevant noise sources has been presented previously in figure 3.12. What is left to do is to enclose the filter circuit in a $\Sigma\Delta$ modulator and evaluate the overall noise contribution of the switched-capacitor filter at the output of the modulator. The result of this analysis can be expressed as an input-referred noise seen at the input of the system (V_{RF} in Volts), which would be beneficial in deriving the required component sizing based on an input-referred noise requirement.

There are three noise sources corresponding to three MOS switches in the switched-capacitor loop filter of the modulator. The frequency responses of each of these three sources can be calculated and referred back to the charge-domain input of the $\Sigma\Delta$ modulator, $q_{in}[n]$. The result of this analysis is shown in figure 3.18. Each of the three MOS switches are labeled with respect to the clock phase where it is conducting (refer to figure 3.16). From this analysis, it is apparent that, when enclosed in a $\Sigma\Delta$ feedback, only noise arising from the φ_1 and φ_2 MOS switches have significant contributions at low frequencies. Each of these two noise sources has an identical variance of $kT(C_{H1}||C_R)$, given that the sizes of capacitors C_{H1} and C_{H2} are equal.

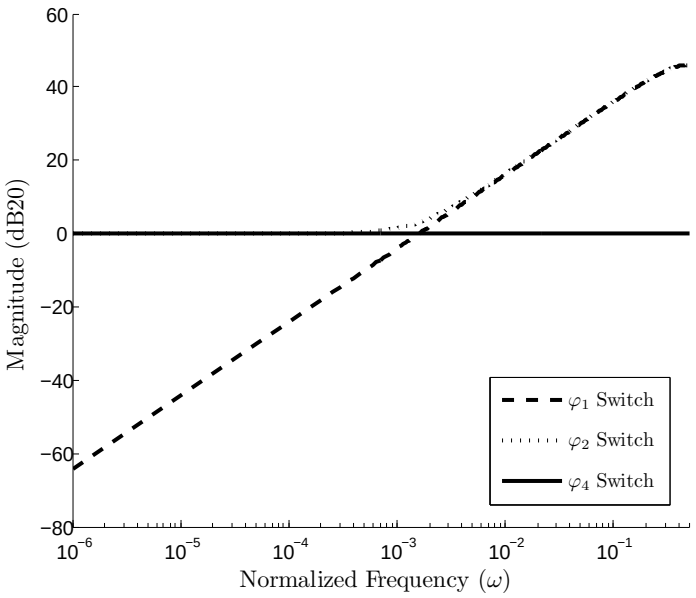


Figure 3.18. Switched capacitor noise in a second-order ΣΔ modulator.

The results derived from figure 3.18 can be easily reflected back to the input RF voltage $V_{RF}(t)$ by virtue of the sampling gain function derived in equation 3.38. Thus, the in-band, input-referred (voltage) noise due to the switched-capacitor loop filter within this second-order ΣΔ A/D converter is:

$$\widetilde{V}^2_{SCnoise} = \frac{2kT(C_{H1}||C_R)}{(\frac{\pi}{2} \cdot \frac{G_m T_{LO}}{2})^2} \tag{3.41}$$

Since the ratio of $\frac{C_{H1}}{C_R}$ is equals to 100, then the above equation can be re-written as:

$$\begin{aligned} \widetilde{V}^2_{SCnoise} &= \frac{2kTC_R\frac{100}{101}}{(\frac{\pi}{2} \cdot \frac{G_m T_{LO}}{2})^2} \\ &\approx \frac{2kTC_R}{(\frac{\pi}{2} \cdot \frac{G_m T_{LO}}{2})^2} \\ &= \frac{2kT}{C_R} \cdot \frac{1}{(\frac{\pi T_{LO}}{4} \cdot \frac{G_m}{C_R})^2} \end{aligned} \tag{3.42}$$

There are two free parameters in the above equation. It will be shown in the next section, that a constraint on linearity would impose a fixed ratio between G_m and C_R. Therefore, the noise arising from the switched-capacitor filter, $\widetilde{V}^2_{SCnoise}$, would be a function of only a single free parameter, which is chosen arbitrarily to be the size of capacitor C_R.

3.3.3 Transconductance Amplifier Design

There are three main constraints to consider in the design of the transconductance amplifier for the ΣΔ receiver: distortion, noise and power. A new parameter, $V_{out(FS)}$, is introduced to describe the maximum allowable output voltage swing of the transconductance amplifier. This constraint is introduced in order to avoid excessive distortion. The addition of this parameter is sufficient to constrain the problem so that only a single optimal solution can exist.

A dominant source of distortion in the transconductance amplifier is due to an excessive voltage swing at the output of the amplifier due to an in-band, full-scale input signal.[5] Large voltage excursions at the output of the amplifier can push some of the constituent transistors into linear region, which create a large change in the amplifier output impedance.

The voltage swing at the output of the amplifier consists of two parts, the voltage swing across capacitor C_{H1} and across the mixer LO switch (figure 3.16):

$$V_{out(FS)} = V_{H1(FS)} + G_m \cdot V_{RF(FS)} \cdot R_{sw} \tag{3.43}$$

where $V_{H1(FS)}$ is simply equal to the voltage stored across capacitor C_{H1}, $V_{H1(FS)} = \frac{Q_{H1(FS)}}{C_{H1}}$.

In the absence of the ΣΔ feedback loop, the voltage $V_{H1(FS)}$ has been calculated previously (equation 3.15) to be:

$$V_{H1(FS)} = \underbrace{\frac{G_m T_{LO}}{2}}_{\substack{V\rightarrow Q \\ conv.\ gain\ at\ DC}} \cdot \underbrace{\frac{\pi}{2}}_{H_p(f_{LO})} \cdot \underbrace{\frac{1}{1-\alpha_1}}_{\substack{DT\ integrator \\ gain\ at\ DC}} \cdot \underbrace{\frac{1}{C_{H1}}}_{\substack{Q\rightarrow V \\ conversion}} \cdot V_{RF(FS)} \tag{3.44}$$

Recall that the above equation contains a few part. First, there are the conversion gains from voltage (continuous-time) → charge-packets, and charge-packets → voltage (discrete-time). Second, there is the frequency response of the pre-filter $H_p(f_{LO})$. Last, there is the (discrete-time) integrator gain of $\frac{1}{1-\alpha_1}$. It is only this last part that changes significantly in the presence of the ΣΔ feedback loop.

[5] Other sources of distortion will be discussed in depth in section 4.1.

In order to characterize the effect of loop-gain, a parameter k_{SD} is introduced to replace the discrete-time integrator gain of $\frac{1}{1-\alpha_1}$. Therefore, equation 3.44 is rewritten as:

$$V_{H1(FS)} = \frac{G_m T_{LO}}{2} \cdot \frac{\pi}{2} \cdot k_{SD} \cdot \frac{1}{C_{H1}} \cdot V_{RF(FS)} \tag{3.45}$$

Since the ΣΔ modulator is modeled completely in the discrete-time domain (figure 3.16), only this discrete-time transfer function needs to be modified in the presence of the ΣΔ modulator feedback signal.

The exact value of parameter k_{SD} can be determined through system simulation of the ΣΔ modulator. Its value would be dependent only on the modulator structure and the scaling factor on each of its integrators [13]. The result of this analysis is shown in figure 3.19. This figure displays the distribution of output signal magnitude at the output of the first integrator, when the input is 3dB away from full-scale. The magnitude is normalized to a full-scale input of the modulator. Since the analysis is completely done in the charge domain, the input full-scale range corresponds to $Q_{in(FS)}$. The result of this analysis shows that for a full-scale input, the output signal of the first integrator would have an amplitude three times as large as the input full-scale range. In other words, it is determined empirically through simulation that $k_{SD} \approx 3$.

The presence of a ΣΔ loop feedback attenuates the full-scale voltage swing of the amplifier by $\frac{k_{SD}}{\frac{1}{1-\alpha_1}}$. Whereas k_{SD} takes a value of 3, the discrete-time gain $\frac{1}{1-\alpha_1}$ is equal to 100, given the parameters set in section 3.3.1. In the absence of a ΣΔ loop feedback, the system would continuously integrate the input charge-packets, with a resulting DC gain of $\frac{1}{1-\alpha_1}$. In contrast, the ΣΔ feedback loop tries to follow and cancel the input charge-packets through the application of the feedback signal. As a result, the signal present at the output of the amplifier in the presence of the ΣΔ feedback comprises of the *error* signal of the ΣΔ modulator, instead of the input signal. This is an important feature of this architecture, which enables the amplifier to have high gain while at the same time minimizing distortion.

Assuming that the IR drop across the LO switch can be made small through sizing of

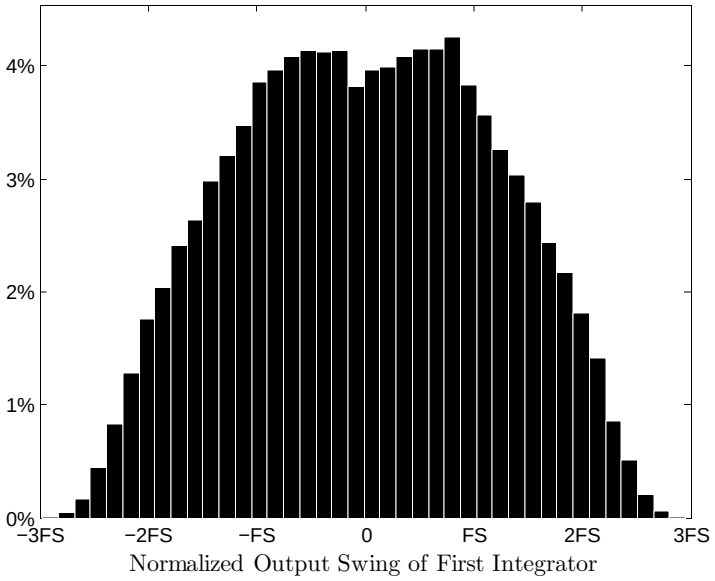


Figure 3.19. Normalized histogram of output values of Q_{H1}

the MOS switch, the full-scale output swing of the transconductance amplifier is therefore:

$$\begin{aligned} V_{out(FS)} &= \frac{G_m T_{LO}}{2} \cdot \frac{\pi}{2} \cdot k_{SD} \cdot \frac{1}{C_{H1}} \cdot V_{RF(FS)} \\ &= \frac{G_m}{C_R} \cdot \frac{\pi}{4} \cdot T_{LO} \cdot \beta k_{SD} \cdot V_{RF(FS)} \end{aligned} \tag{3.46}$$

The input-referred noise of the transconductance amplifier is a function of the value of its transconductance, G_m. The exact value of the noise contribution of this amplifier would depend on the topology of the amplifier. However, a simple input-referred noise model can be adopted, which is shown below:

$$\frac{\widetilde{V}^2_{GMnoise}}{\Delta f} = \frac{4kT\gamma}{G_m} \cdot n_F \tag{3.47}$$

The noise factor n_F is included in order to model the contributions of non-essential transistors, i.e. transistors other than those which are performing the voltage-to-current conversions.[6]

The combined noise arising from the transconductance amplifier and the switched-

[6]This analysis does not take into account the folding effect of the higher harmonics. This effect can also be incorporated into the noise factor n_F.

capacitor loop filter is:

$$\begin{aligned}\frac{\widetilde{V}^2_{noise}}{\Delta f} &= \frac{4kT\gamma}{G_m}\cdot n_F + \frac{2kT}{C_R}\cdot\frac{1}{(\frac{\pi T_{LO}}{4}\cdot\frac{G_m}{C_R})^2} \\ &= \frac{kT}{C_R}\left[\frac{4\gamma n_F}{\frac{G_m}{C_R}\cdot T_{LO}} + \frac{2}{(\frac{\pi T_{LO}}{4}\cdot\frac{G_m}{C_R})^2}\right] \end{aligned} \tag{3.48}$$

The ratio of $\frac{G_m}{C_R}$ can be obtained from equation 3.46:

$$\frac{G_m}{C_R} = \frac{V_{RF(FS)}}{V_{out(FS)}}\cdot\frac{4}{\pi T_{LO}}\cdot\frac{1}{\beta k_{SD}} \tag{3.49}$$

The parameters $V_{RF(FS)}$, T_{LO}, β and k_{SD} are fixed design parameters that have been previously set. Therefore, if one were to set a $V_{out(FS)}$ based on linearity considerations, the ratio of $\frac{G_m}{C_R}$ also becomes a fixed parameter. Thus the total noise from equation 3.48 becomes only a function of the size of capacitor C_R.

In the beginning of this section, it is stated that there are three important parameters in the design of the transconductance amplifier: distortion, noise and power. The constraint on distortion can be described by the maximum allowable signal swing at the output of the amplifier, $V_{out(FS)}$. This parameter imposes a limitation on the amount of transconductance G_m for a given capacitance C_R. Furthermore, this restriction also allows the total noise of the amplifier and the switched capacitor filter to be completely determined by the sizing of capacitor C_R. Larger capacitance C_R results in lower noise. However, larger capacitance C_R results in larger power. Larger capacitances would require a larger transconductance G_m in order to maintain the same conversion gain, as well as larger MOS switches in order to achieve the same settling time.

3.4 Mixed-Signal Design of the System

The design of the feedback D/A converter and the comparator needed in the $\Sigma\Delta$ receiver will be discussed in this section. Non-idealities from these two blocks will be discussed in relation to the overall performance of the system. A circuit specification for each of these blocks will be derived based on acceptable performance degradation due to these circuit non-idealities.

3.4.1 Feedback D/A Converter Design Considerations

The full-scale requirements for the first and second feedback D/A converters have been derived previously in section 3.3.1:

$$Q_{FB1(FS)} = \frac{\pi}{2} \cdot \frac{G_m T_{LO}}{2} \cdot V_{RF(FS)} \tag{3.50}$$

$$Q_{FB2(FS)} = \frac{\pi}{2} \cdot \frac{G_m T_{LO}}{2} \cdot \frac{\alpha_1^2}{\beta \cdot (\alpha_1 + \alpha_2)} \cdot V_{RF(FS)} \tag{3.51}$$

The above values serve as a starting point for the feedback D/A converter design process. The focus of this discussion will be on the design of the first feedback D/A converter circuit, due to its more stringent requirement. Noise and distortion introduced by the second feedback D/A converter are partly attenuated by the loop gain of the modulator. Because of this reason, the design requirements for the second feedback D/A converter are not as stringent as that of the first feedback D/A converter.

There are two types of feedback D/A converters in a $\Sigma\Delta$ modulator, continuous-time and switched-capacitor. In a continuous-time D/A converter, current is continuously applied across a prescribed amount of time in order to achieve charge transfer. On the other hand, in a switched capacitor implementation, a dummy feedback capacitor, C_{FB}, is pre-charged to a certain voltage value, then it is charge-shared with the integrating capacitors.

Switched-capacitor D/A converters are desired because it is less sensitive to jitter [75]. The total feedback charge applied in this method is simply $Q_{FB} = C_{FB} \cdot V_{FB_{ref}}$. As long as there is sufficient time to settle the capacitor voltage to $V_{FB_{ref}}$, then timing uncertainty does not affect the applied feedback value Q_{FB} at all.

Although a switched-capacitor D/A converter is more desirable from a jitter perspective, it can be shown that it is practically infeasible in this architecture. Recall that in a switched-capacitor D/A converter, a dummy capacitor C_{FB} is utilized as a vessel to store the feedback charge signal. For the first feedback D/A converter, the size of feedback capacitor C_{FB1}

needs to be:

$$\begin{aligned} C_{FB1} &= \frac{V_{FB_{ref}}}{Q_{FB1(FS)}} \\ &= \frac{V_{FB_{ref}}}{V_{RF(FS)}} \cdot \frac{4}{\pi G_m T_{LO}} \end{aligned} \tag{3.52}$$

Equation 3.52 can be combined with equation 3.49 to yield the following result:

$$\frac{C_{FB1}}{C_R} = \frac{V_{FB_{ref}}}{V_{out(FS)}} \cdot \frac{1}{\beta k_{SD}} \tag{3.53}$$

This analysis yields a ratio of the size of the feedback capacitor C_{FB1} with capacitor C_R. Recall that the size of capacitance C_R is set by noise and power considerations, and is of importance in deriving other circuit parameters.

The size of capacitor C_{FB1} should be of approximate size as capacitor C_R. Ideally they should be of the same size, such that capacitor C_R could be used both as part of the loop filter as well as the feedback D/A converter. In fact, from figure 3.16, phases φ_3 and φ_4 can be used in order to pre-charge the capacitor C_R to the voltage $V_{FB_{ref}}$.

Unfortunately, there is a ten-fold size mismatch between capacitor C_{FB1} and C_R. The relevant parameter values have been derived in section 3.3: $k_{SD} = 3$ and $\beta = 0.01$. Furthermore, assume that $V_{FB_{ref}} = V_{DD} = 3 \cdot V_{out(FS)}$. Using these assumptions, then the size of capacitor C_{FB1} has to be more than ten times larger than that of capacitor C_R. This large size mismatch rules out the possibility of using the same capacitor C_R in order to implement the feedback D/A converter. Furthermore, the presence of a feedback capacitor of this size would create a significant loss and therefore reduce the DC gain of the loop filter.

In contrast to a switched-capacitor feedback D/A converter, a continuous-time D/A converter operates by injecting a constant current over a predetermined amount of time:

$$Q_{FB} = I_{FB_{ref}} \cdot T_{ref} \tag{3.54}$$

The timing signal T_{ref} can be obtained from an external crystal reference or from a frequency synthesizer. Random fluctuations in this timing reference would translate into random fluctuations in the applied feedback charge-packets. Therefore, compared to a switched-capacitor D/A converter design, a continuous-time feedback D/A converter is more susceptible to timing jitter.

The advantage of a continuous-time feedback D/A converter is that it is relatively easy to implement, and it can be made to operate at very high frequencies. Unlike a switched-capacitor D/A converter which necessitates large drivers in order to maintain a short settling-time, on the first-order current-switching D/A converter does not have a stringent settling requirement [108]. A more detailed description on the design trade-offs and restrictions will be presented in section 4.1.

Timing Jitter

The sensitivity to timing jitter of a continuous-time feedback D/A is fully expressed in equation 3.54. In the presence of a timing variation of magnitude ΔT_{ref}, a variation in charge of magnitude:

$$\Delta q_{FB1} = I_{FB1_{ref}} \cdot \Delta T_{ref} \tag{3.55}$$

is injected in the modulator. The variation in ΔT_{ref} is a random process, and is referred to as *random timing jitter*. Let us denote $\widetilde{\Delta T}[n]$ as a random noise process representing the timing variation within T_{ref}. The noise process $\widetilde{\Delta T}[n]$ is an additive Gaussian noise process with mean zero, variance of $\sigma^2_{T_{ref}}$ and a power spectral density of $S_{T_{ref}}(\omega)$

In order to calculate the achievable SNR, it is important to note that the noise process $\widetilde{\Delta T}$ is a discrete-time noise process, whose energy is spread from DC to f_s, where f_s is the sampling rate. On each sampling instant the following (deterministic) feedback signal is applied:

$$Q_{FB1}[n] = d_{out}[n] \cdot I_{FB1_{ref}} \cdot T_{ref}[n] \tag{3.56}$$

In the presence of timing noise, the feedback charge contains a noise process of the following nature:

$$\widetilde{\Delta q}_{FB1}[n] = d_{out}[n] \cdot I_{FB1_{ref}} \cdot \widetilde{\Delta T}[n] \tag{3.57}$$

Therefore the achievable in-band SNR is:

$$\begin{aligned} SNR &= \frac{Q_{in(FS)}}{\widetilde{\Delta q}_{FB1}(in-band)} \\ &= \frac{T_{ref}}{\sqrt{\int_0^{\frac{BW}{2}} S_{D_{out}}(\omega) * S_{T_{ref}}(\omega)}} \end{aligned} \tag{3.58}$$

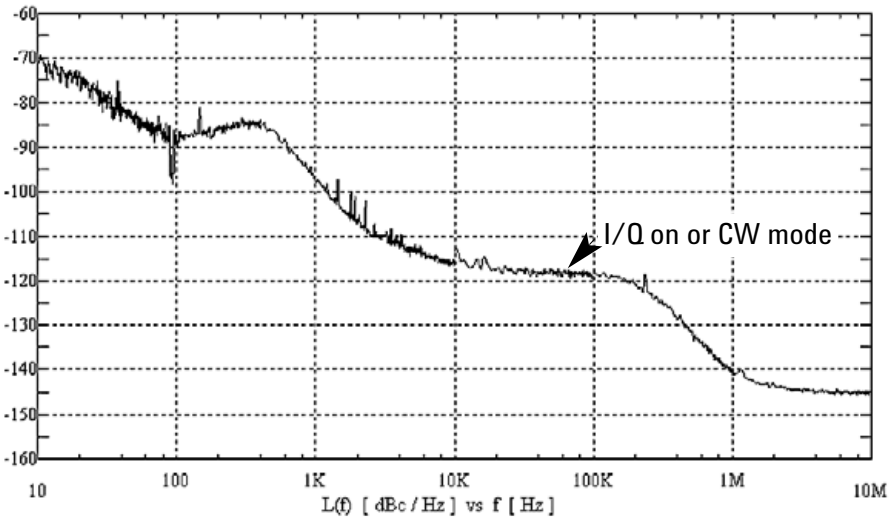


Figure 3.20. Phase-noise plot of a frequency synthesizer.

where $S_{D_{out}}(\omega)$ is the power spectral density of the $\Sigma\Delta$ modulator output, $d_{out}[n]$. If the $\widetilde{\Delta T}[n]$ noise process is white, then equation 3.58 simplifies to:

$$SNR = \frac{T_{ref}}{\sigma_{T_{ref}}} \cdot \frac{1}{OSR} \tag{3.59}$$

where OSR is the modulator's oversampling ratio.

The nature of the noise process ΔT_{ref} is dependent upon the system used to generate the timing reference T_{ref}. Nevertheless, in general, these timing reference generator is characterized by its phase noise performance, expressed in terms of the phase noise spectrum $S_\phi(\omega)$. The following relation is used to relate phase noise and jitter [5]:

$$S_{T_{ref}}(\omega) = \frac{S_\phi(\omega)}{(2\pi f_c)^2} \tag{3.60}$$

Therefore, the resulting spectrum of $\widetilde{\Delta q}_{FB1}[n]$ is simply the phase noise spectrum $S_\phi(\omega)$ convoluted with the spectrum of the $\Sigma\Delta$ modulator output scaled by $(2\pi f_c)^2$.

An example phase-noise spectrum plot from a high-performance vector signal generator, Agilent 4438C is shown in figure 3.20 [1]. Based on the above spectrum, the maximum achievable SNR, with an in-band, full-scale input is shown in table 3.3. Note that the effect of timing jitter on the feedback D/A converter is independent and is additive to the effect of phase noise to noise resulting from reciprocal mixing.[7]

[7]Since the timing reference for both the feedback D/A converter and the mixer originates from a single

Table 3.3. Achievable SNR with Agilent 4438C as a frequency reference.

Signal Bandwidth	Achievable SNR
2MHz	67dB
4MHz	66.8dB
8MHz	66.6dB
20MHz	65.9dB

Output Resistance

The effect of a current-switching D/A converter's output resistance has been studied previously [109]. It has been recognized that the output resistance of a current-switching D/A converter is code-dependent. The output impedance of a D/A converter is in parallel with the load resistance R_L. Therefore, the *effective* output impedance of the circuit is:

$$\begin{aligned} R_{out,eff} &= \frac{R_L \cdot R_{DAC}}{R_L + R_{DAC}} \\ &= \frac{R_L}{1 + \frac{R_L}{R_{DAC}}} \end{aligned} \tag{3.61}$$

where R_{DAC} is the D/A converter output resistance. A code-dependent $R_{out,eff}$ would generate distortion. In order to mitigate this effect, the output resistance of each unit cell within the D/A converter is typically made very large such that $\frac{R_L}{R_{DAC}} >> 1$; therefore $R_{out,eff} \approx R_L$ and the code-dependent nature of R_{DAC} would be inconsequential.

Similar conditions exist for the $\Sigma\Delta$ receiver system as well. This effect is particularly important for the first feedback D/A converter, whose full-scale range is much larger than the second feedback D/A converter. As a result a much larger D/A converter, with a much smaller output resistance, is needed for the first feedback D/A converter.

In order to analyze the effect of finite DAC output resistance R_{DAC}, let us analyze it in isolation by assuming that the transconductance amplifier is ideal with infinite output resistance R_{par} and zero output capacitance C_{par}. Consider a differential implementation of the system. A current *sink* D/A converter is switched between the positive and negative terminal of capacitor C_{H1} in order to inject a negative or positive feedback signal respectively

source, there is a significant amount of correlation between the two noise processes affecting the two circuits. The approach taken here is to take the worst case; i.e. to assume that both noise processes are perfectly uncorrelated. In this case, noise arising from reciprocal mixing and from the feedback D/A converter circuit simply adds in power.

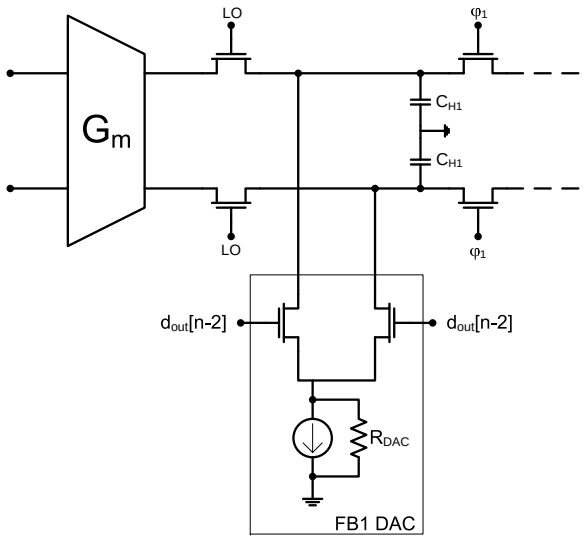


Figure 3.21. Circuit model of the first feedback D/A converter with finite output resistance.

(figure 3.21). If a negative feedback signal is to be applied, the current sink is connected to the positive node of capacitor C_{H1}. A finite output resistance of value R_{DAC} is therefore connected between the positive terminal of capacitor C_{H1} to a common ground. Therefore a charge amounting to:

$$Q_{RDAC}[n] = Q_{H1}[n] \cdot \exp(\frac{-T_{ref}}{C_{H1}R_{DAC}}) \cdot d_{out}[n-2] \tag{3.62}$$

is lost during the period where the feedback signal is applied. This charge is lost through discharging to ground through resistor R_{DAC}. Charge $Q_{H1}[n]$ is the initial charge stored in capacitor C_{H1} prior to the application of the feedback signal. When a positive feedback signal is applied, the same amount of charge is *injected* into capacitor C_{H1} instead of being lost, due to the difference in polarity of where the feedback signal is applied to the capacitor C_{H1}. The difference in polarity is reflected through the multiplication by a factor d_{out} which takes a value of +1 or -1, depending on the feedback signal being applied. This effect can be modeled by introducing a parameter β_{RDAC}:

$$\beta_{RDAC} = \exp(\frac{-T_{ref}}{C_{H1}R_{DAC}}) \tag{3.63}$$

A system diagram including the effect of finite D/A converter output resistance is shown in figure 3.22.

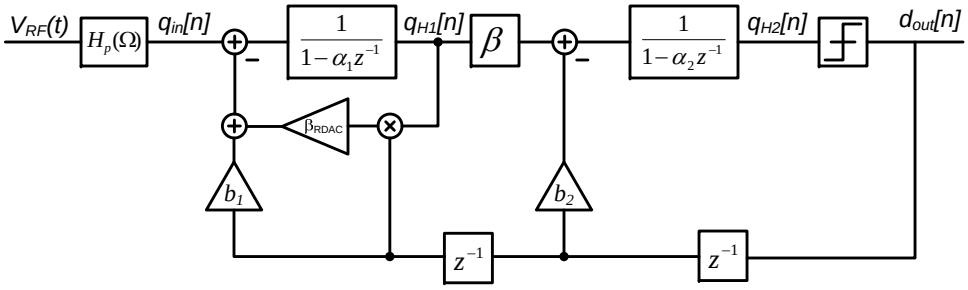


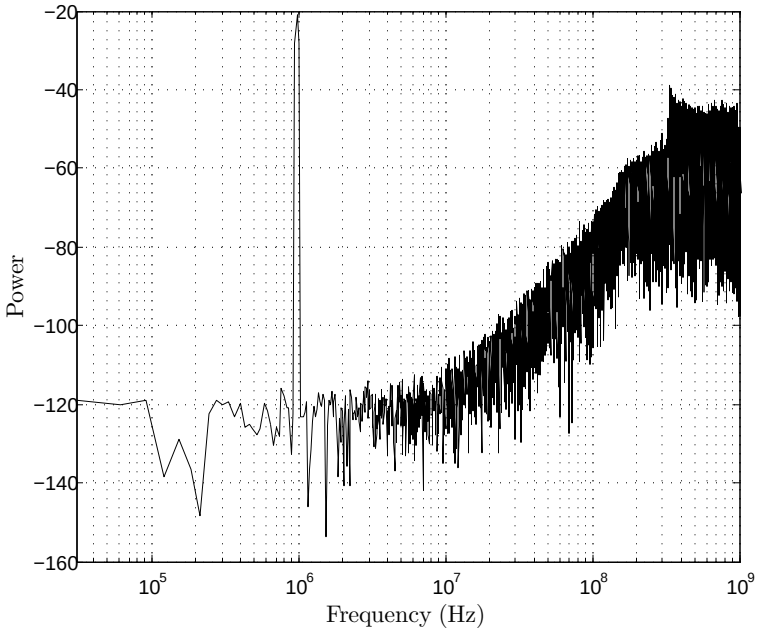
Figure 3.22. System model including the effects of feedback D/A converter finite output resistance.

The presence of a finite output resistance R_{DAC} would create distortion within the $\Sigma\Delta$ modulator. This is apparent from equation 3.62, where the signal d_{out} is multiplied with the signal Q_{H1}. Recall that both these quantities contains a large component of the input signal $V_{RF}(t)$. As a result, the error charge Q_{RDAC} contains a significant amount of second-order distortion of the input signal $V_{RF}(t)$.

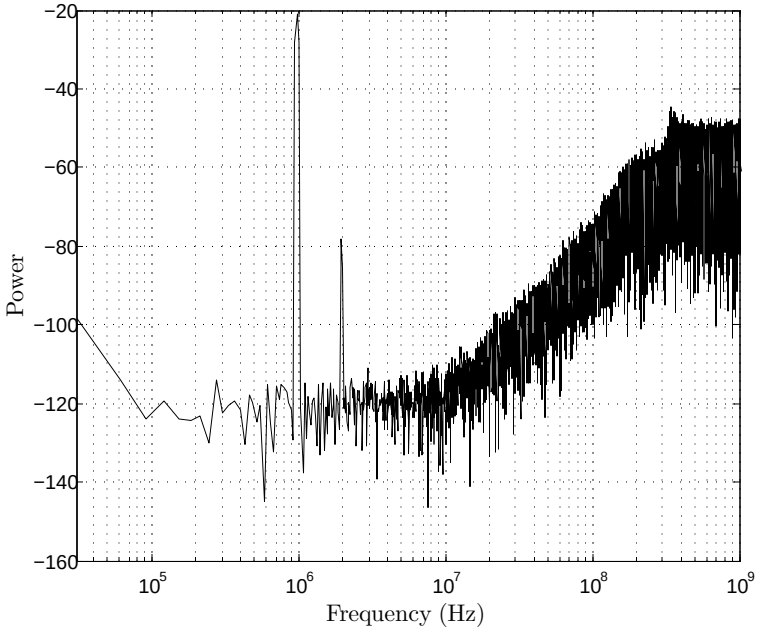
A high output resistance R_{DAC} is desired. In the limit that $R_{DAC} \rightarrow \infty$, then $\beta = 0$. In this case no second-order distortion would be created. A system simulation is used in order to derive the minimum R_{DAC} in order to achieve a certain SFDR performance. The result of the analysis described is shown in figure 3.24. In order to achieve an SFDR greater than 70dB, then a ratio of $\frac{T_{per}}{R_{DAC}C_{H1}}$ of less than 10^{-3} is needed.

3.4.2 Comparator Offset and Noise

Comparator noise and offset can be treated similarly, since both are injected at the same point within the $\Sigma\Delta$ modulator. The transfer function from the input of the comparator to the output $d_{out}[n]$ is simply the NTF of the modulator. In order to specify the maximum tolerable error, errors that originate from the comparator need to be referred back to input RF voltage, $V_{RF}(t)$. Suppose an input-referred error voltage of $V_{comperror}$ is used to represent both the comparator offset and comparator noise. Since the input of the comparator is connected to capacitor C_{H2}, an error voltage of $V_{comperror}$ is equivalent to an error *charge* of $Q_{comperror} = C_{H2} \cdot V_{comperror}$. Therefore, the comparator error referred to the input



(a)



(b)

Figure 3.23. $\Sigma\Delta$ modulator output spectrum: (a) with an infinite R_{DAC}; (b) with a finite R_{DAC}.

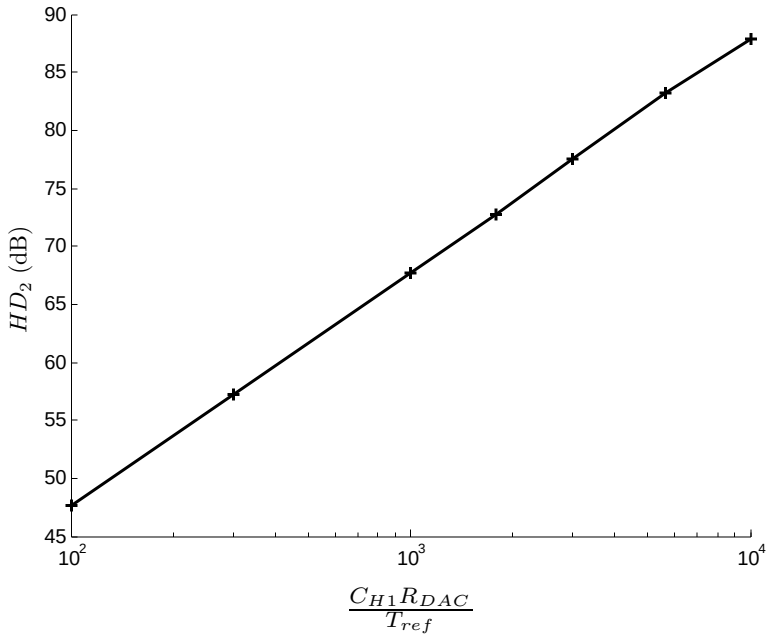


Figure 3.24. Second-order distortion due to a finite R_{DAC}.

voltage $V_{RF}(t)$ is:

$$V_{comperror@V_{RF}} = Q_{comperror} \cdot \underbrace{NTF}_{Q_{comperror} \rightarrow d_{out}} \cdot \underbrace{\frac{1}{STF \cdot \frac{G_m T_{LO}}{2} \cdot \frac{\pi}{2}}}_{d_{out} \rightarrow V_{RF}} \tag{3.64}$$

When the above equation is evaluated across the bandwidth of interest, the following would result:

$$V_{comperror@V_{RF}} = \frac{C_{H2}}{\frac{G_m T_{LO}}{2} \cdot \frac{\pi}{2}} \cdot \frac{(1-\alpha_1)(1-\alpha_2)}{\beta} \cdot V_{comperror} \tag{3.65}$$

Based on equation 3.65, specifications on maximum tolerable levels on comparator noise and offset can be derived.

3.5 Summary of Circuit Parameters

Based on the requirements analyzed on previous sections, we are now in a position to determine important circuit parameters in order to meet the requirements set in chapter 2.

There are a few parameters that has been set previously in this chapter; these parameters are listed below:

Parameter	Value
$\alpha 1$	0.99
$\alpha 2$	0.99
β	0.01

A high output resistance R_{par} from the transconductance amplifier is desired. As a result a cascode output stage might be necessary, in which case, the output voltage swing would be limited. An output swing of approximately 300mV can be expected from a cascode output stage. A margin of 50mV is allocated for the IR drop accross the LO switch. Therefore, the parameter $V_{out(FS)}$ can be set to be: The requirement on $V_{RF(FS)}$ is set by the system

Parameter	Value
$V_{out(FS)}$	250mV
$V_{RF(FS)}$	300mV

requirement set forth in chapter 2.

Sizing of the capacitor is a function of the noise requirement, which is described in equation 3.48. When equation 3.48 is evaluated with the values above, it turns out that the noise is dominated by the transconductance amplifier and not by the switched capacitor filter. Based on the requirement on input-referred noise, the following circuit parameters are found:

Table 3.4. Summary of circuit parameters.

Parameter	Value
G_m	6mS
C_R	50fF
C_{H1}	5pF
C_{H2}	5pF
R_{DAC}	$50k\Omega$

The output resistance of the feedback D/A converter is sized in order to obtain an SFDR greater than +70dB. Note that there are other distortion mechanism that could be more dominant than the one due to finite D/A converter output resistance.

Chapter 4

Experimental Prototype

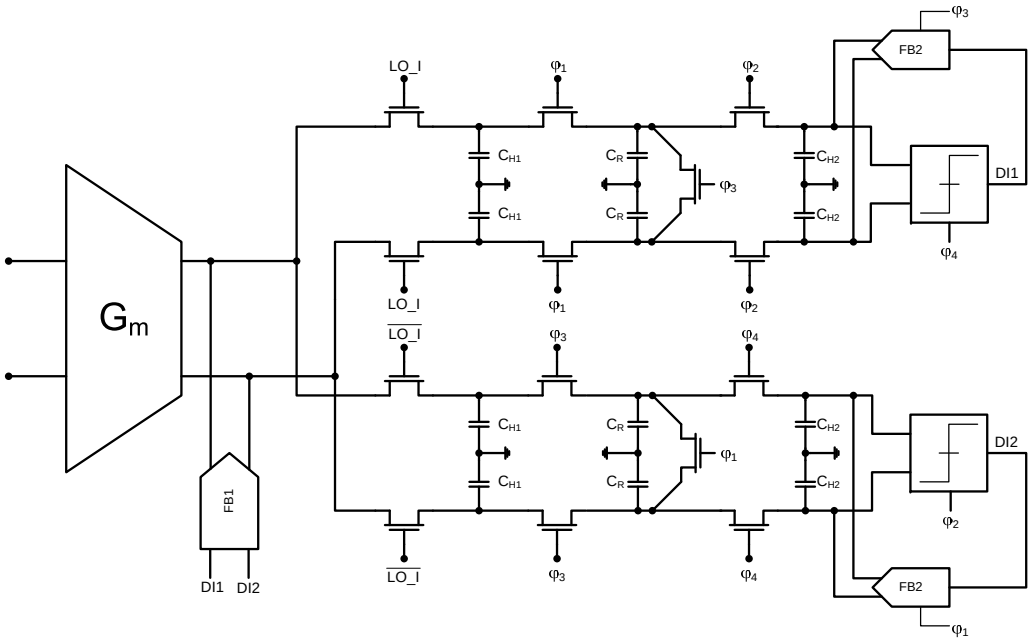
In this chapter, a prototype circuit of the $\Sigma\Delta$ receiver is presented. Parameter values and effect of circuit non-idealities derived from chapter 3 is used as a starting point for the circuit design.

A test chip demonstrating the important concepts for the $\Sigma\Delta$ receiver has been manufactured and tested. The measurement results is presented towards the end of this chapter.

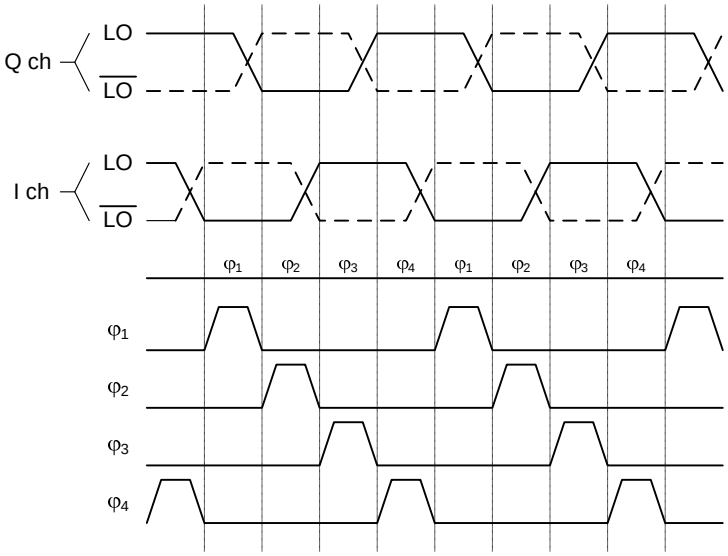
4.1 Circuit Design

The test-chip prototype consists of both I and Q quadrature channels. A complete circuit schematic of the I channel of the $\Sigma\Delta$ receiver is shown in figure 4.1. The schematic for the Q channel is identical with the exception that all the clock signals are delayed by a quarter of a period.

The circuit is implemented in a fully-differential configuration. Furthermore, for each of the I and Q channels, the signal path is further divided into the top and bottom paths. These two paths are time-interleaved, and the outputs are also evaluated in a time-interleaved manner. When the signal LO_I is high, the top path is tracking the input signal, while the bottom path is in its hold phase, and the output of the sampling mixer circuit is evaluated



(a) Detailed System Diagram.



(b) Timing Diagram.

Figure 4.1. Detailed system diagram of the ΣΔ receiver.

as a discrete-time signal. When the LO_I signal is low, then the opposite occurs. This time-interleaving scheme effectively doubles the sampling rate of the receiver.

In the succeeding sections, each of the circuit blocks denoted in figure 4.1 will be individually discussed. There are five important circuit blocks: the transconductance amplifier (Gm), the first and second feedback D/A converter (FB1 and FB2), the comparator circuit and the timing generation block.

4.1.1 Transconductance Amplifier

The ideal transconductance amplifier is a current-controlled current source. It should have an infinite output impedance, and the transfer function between input voltage and output current should be perfectly linear. The minimum allowable impedance is discussed in section 3.2.4. The presence of finite output resistance R_{par} and output capacitance C_{par} creates a path for charge loss in the integrating capacitor C_{H1}. Charge loss due to this mechanism should be much smaller than that due to capacitor C_R. In this manner, the corner frequency of the loop filter is still determined by the ratio of $\frac{C_R}{C_{H1}}$, instead of the values of R_{par} and C_{par}. In order for this to be accomplished, the following conditions have to be met:

$$\begin{aligned} C_R &\gg C_{par} \\ R_{par}C_{H1} &\gg \frac{T_{LO}}{2} \end{aligned} \tag{4.1}$$

Besides the output impedance requirement, the transconductance amplifier also needs to have sufficient output-to-input isolation. In an RF mixer, output-to-input isolation is important in order to minimize self-mixing and LO leakage to the RF port [55, 98]. This is especially important in the $\Sigma\Delta$ receiver, because the output of the transconductance amplifier is also the summing node for the $\Sigma\Delta$ modulator. As a result, significant quantization noise will be present in the output of the amplifier. This quantization noise should not leak back to the RF port.

Based on the considerations set above, a two-stage amplifier is chosen (figure 4.2). The first stage is a common-source amplifier that performs the voltage-to-current conver-

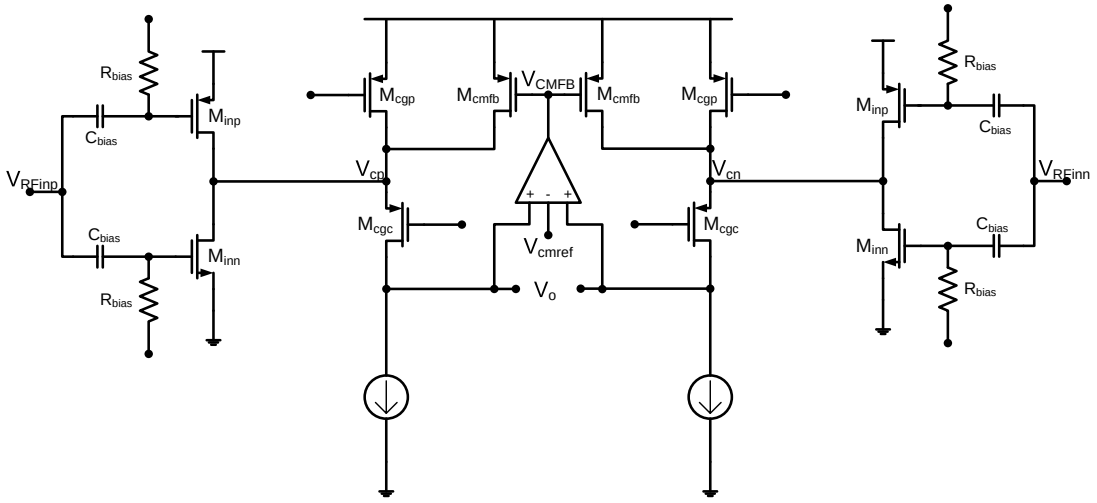


Figure 4.2. Transconductance amplifier circuit.

sion. A second-stage folded-cascode amplifier is designed in order to provide a high output impedance as well as a good isolation to the input port. The cascode transistor also helps in keeping the drain voltages of the common-source transistors relatively constant by providing a low impedance node. A pseudo-differential configuration is chosen in order to maximize the headroom. At radio-frequency, the common-mode rejection is determined by the parasitic capacitance at the virtual-ground node, which negates the benefits of a fully-differential structure [30].

The bias voltages of the NMOS and PMOS common-source transistors are provided independently using diode-connected transistors and external bandgap references. A high-swing cascode current-mirror bias circuit is used to generate the bias voltages of the common-gate stage [99].

Distortion in the common-source stage comes from two possible sources; nonlinearity from V_{GS} to I_{DS} and nonlinearity resulting from V_{DS} modulation[1]. Each of these two distortion mechanisms will be treated separately and in isolation of each other.

In short-channel devices, there are three regions of operation for the MOS transistor, depending on the drain-to-source voltage [106]. The three regions from small to large V_{DS}

[1]The subscript G, D, S and B, refer to the gate, drain, source and bulk of the MOS transistor respectively.

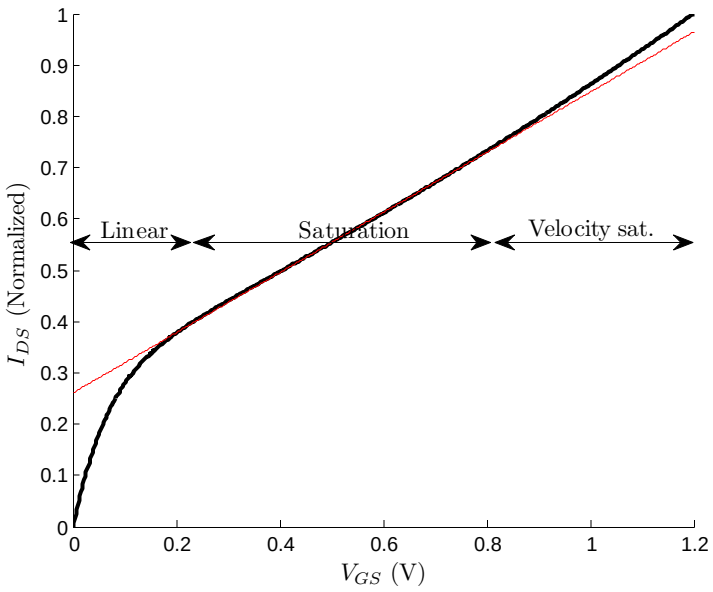


Figure 4.3. Drain voltage modulation on a MOS transistor.

are: linear, saturation and velocity saturation (4.3). MOS transistors are typically biased in the saturation region in order to achieve a large *and* linear output resistance ($\frac{\delta I_{DS}}{\delta V_{DS}}$). However, with the reduction in supply voltage and the reduction of the channel length, the width of the saturation region is decreasing. As a result, the width of the region where the transistor's output resistance is linear is reduced.

The best way to combat nonlinearity due to drain modulation is to try to keep the drain-node voltage constant. It is important to realize that, unlike gate modulation, drain modulation is an undesired side-effect of the four-terminal MOS transistor. It is therefore possible to retain the voltage-to-current conversion characteristics while maintaining a constant drain voltage. Keeping the drain-node voltage 'quiet' can be accomplished by providing a low-impedance path at the drain-node of the transistor.

Nonlinearity due to V_{GS} to I_{DS} transfer function is fundamental to the operation of MOS transistor and is unavoidable. This effect was briefly discussed in section 2.5.1. There are, however, a few techniques that can be utilized in order to *minimize* the resulting distortion. We will generally categorized these techniques into two categories: feedback and distortion cancellation.

A Taylor series expansion can be used to describe the nonlinear behavior of the MOS voltage-to-current conversion:

$$\begin{aligned} I_{DS} &= a_0 + a_1 \cdot v_{GS} + a_2 \cdot {v_{GS}}^2 + a_3 \cdot {v_{GS}}^3 + ... \\ I_{DS} &= I_{DS,Q} + g_m \cdot v_{GS} + g_{m2} \cdot {v_{GS}}^2 + g_{m3} \cdot {v_{GS}}^3 + ... \end{aligned} \tag{4.2}$$

The frequency-dependent distortion components are ignored in order to simplify the analysis. The first-order term corresponds to the small-signal linear transconductance g_m, around the operating point of $V_{GS,Q}$. The second-order term, which will be referred to g_{m2} is responsible for generating second-order distortion term at the current output of the transistor. Similarly, the third-order term g_{m3} is responsible for generating the third-order distortion.

Feedback can be utilized in order to reduce distortion in a MOS transistor, simply by reducing the voltage swing across the gate and source. The use of feedback can reduce the second-, and third-order distortion by the following amount [73]:

$$g'_{m2} = \frac{g_{m2}}{(1 + g_m f)^3} \tag{4.3}$$

$$g'_{m3} = \frac{g_{m3}(1 + g_m f) - 2g_{m2}^2 f}{(1 + g_m f)^5} \tag{4.4}$$

where f is the feedback factor.

The disadvantage of using feedback to linearize a transistor is that feedback also reduces the gain of the amplifier. Specifically the resulting small-signal transconductance is reduced by:

$$g'_{m1} = \frac{g_m}{1 + g_m f} \tag{4.5}$$

It is clear that a larger loop gain $g_m f$ would result in a more linear amplification. However, at the same time, a larger loop gain would further reduce the linear amplification gain g'_{m1}. If a certain transconductance is desired, the use of feedback would necessitate the use of larger devices with larger bias current. Therefore there is a power penalty in using a feedback linearization scheme. Furthermore, if the feedback network (henceforth represented by a simple linear gain f) is noisy, feedback linearization would also degrade the noise figure of the amplifier.

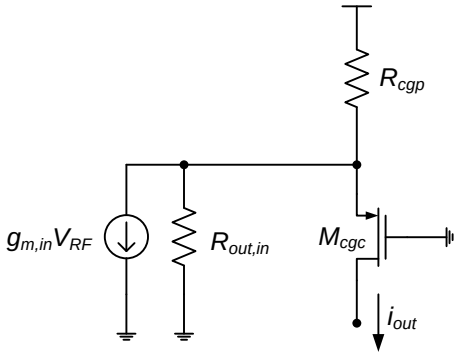


Figure 4.4. Common-gate cascode amplifier.

The simplest feedback linearization scheme is perhaps the source degeneration technique [30]. There are also a number of other feedback linearization techniques that have been published [58, 107, 44]. All of them achieves better linearity at the expense of a higher circuit noise and higher power consumption.

Distortion of a MOS transistor highly depends on the DC operating point of the transistor. This can be seen in figure 2.16, where the highest IIP3 is obtained at a DC bias point of 350mV. The optimal bias point can be determined by plotting the g_m, g_{m2} and g_{m3} curve as a function of the DC operating point $V_{GS,Q}$ [69, 18, 43]. Through optimizing the operating point of the transistor, a high linearity can be obtained. This technique is also known as distortion cancellation.

The distortion cancellation technique is chosen for this $\Sigma\Delta$ receiver implementation due to its minimum impact on power consumption and noise when compared to feedback linearization schemes. A PMOS/NMOS pair is used as a complementary transconductor in order to cancel their second-order distortion [18, 69]. Each of the PMOS and NMOS transistors is biased in the region that would minimize its third-order distortion.

The desired overall transconductance from this amplifier has been derived in section 3.5. The desired transconductance determines the sizing necessary for the NMOS and PMOS transistors in the first stage amplifier. The folded-cascode second-stage is sized in order to obtain an acceptable distortion level. Since the common-gate transistor operates in a

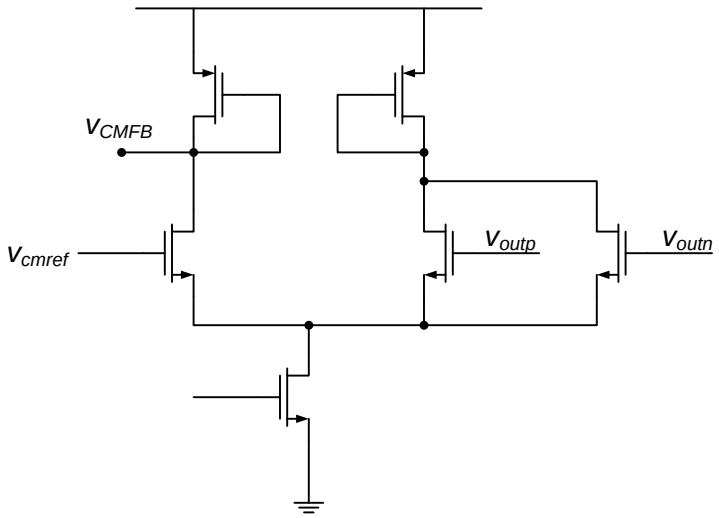


Figure 4.5. Common-mode feedback amplifier.

class-A mode, the bias current in the cascode stage has to be larger than the largest current swing from the first-stage, common-source amplifier, $I_{bias,cascode} > G_m V_{RF(FS)}$.

Nonlinearity resulting from the common-gate stage primarily occurs due to the varying transconductance of the transistor M_{cgc} (figure 4.4). The output current from the cascode amplifier is:

$$i_{out} = \frac{g_{m,cgc}}{g_{m,cgc} + \frac{1}{R_{out,in}} + \frac{1}{R_{out,cgp}} + \frac{1}{R_{out,cgc}}} \cdot g_{m,in} V_{RF} \tag{4.6}$$

where the transistor subscripts refer to the assignment set in figure 4.4. In order to achieve a linear transfer function, a large $g_{m,cgc}$ is desired, so that $i_{out} \approx g_{m,in} V_{RF}$. The large value of $g_{m,cgc}$ has to be maintained in the presence of a full-scale input signal. Based on this requirement, sizing of the second-stage cascode amplifier can be determined.

Distortion can also arise due to excessive voltage swing at the output. Large voltage swing at the output of the transconductance amplifier can push some of the devices out of saturation and therefore create distortion. As elaborated in section 3.3, the output voltage of the amplifier comprises of the *error* signal of the $\Sigma\Delta$ modulation, which is much smaller than the input signal. Furthermore, the load impedance at the output of the amplifier forms a bandpass frequency response [20], which helps in attenuating large out-of-band blocker signals. Because of these two reasons, excessive voltage swing at the output can be avoided.

A common-mode feedback stabilization scheme is established by sensing the differential output voltages on the gates of a differential amplifier (figure 4.5). The common-mode feedback signal is applied at the gate of transistor M_{cmfb}.

4.1.2 First Feedback D/A Converter (FB1)

The first feedback D/A converter, which will be called FB1 circuit from here on, is implemented using a continuous-time, current switching D/A converter. Excellent timing reference is available in an RF transceiver in order to meet the transmit mask requirement as well as to minimize the negative impact of reciprocal mixing. Thus, there is no added cost for generating a clean reference clock in order to drive a continuous-time feedback D/A converter. The necessary feedback current has been derived in section 3.4.1, and is repeated here:

$$\begin{aligned} I_{FB1_{ref}} &= \frac{Q_{FB1(FS)}}{T_{ref}} \\ &= \frac{\pi}{4} \cdot \frac{T_{LO}}{T_{ref}} \cdot G_m \cdot V_{RF(FS)} \end{aligned} \tag{4.7}$$

The necessary current reference for the FB1 circuit is of the same order with the bias current necessary for the cascode amplifier stage of the transconductance amplifier. Recall that the bias current of the cascode stage has to be sized such that it can accommodate a maximum current swing of $G_m V_{RF(FS)}$ without clipping or saturating. Assuming that $\frac{\pi}{4} \cdot \frac{T_{LO}}{T_{ref}}$ is a small constant close to unity, there is an opportunity to share bias current between the FB1 circuit and the transconductance amplifier. Sharing the bias current would not only save power, but it would also minimize the circuit parasitics at the output node (R_{par} and C_{par}).

Sharing of bias current can be accomplished by replacing the current-source load of the transconductance amplifier with a current-switching D/A converter. The full circuit diagram of the bias-current-sharing scheme is shown in figure 4.6. The FB1 circuit is implemented as a return-to-zero (RTZ) D/A converter. The RTZ coding scheme is selected due to its relaxed sensitivity to inter-symbol interference. In normal operation, equal amount of current flows on each of the differential branches. Depending on the feedback signal, a

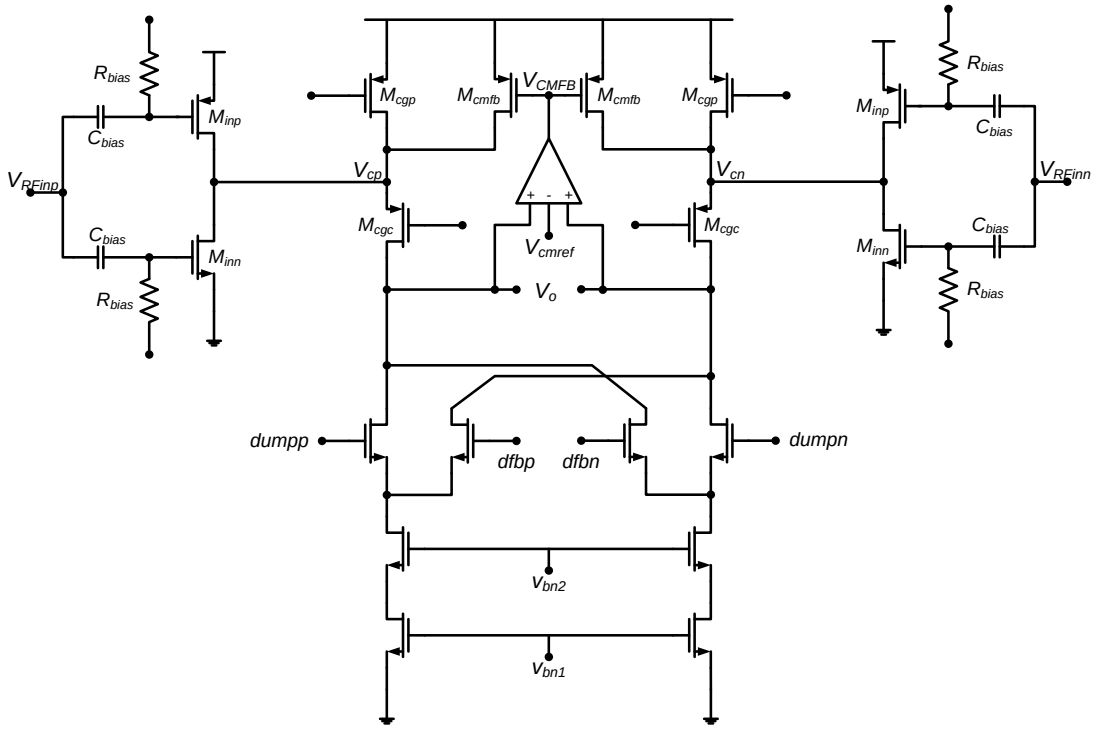


Figure 4.6. A combined transconductance amplifier and first feedback D/A converter circuit.

switching quad would direct the bias current so that more current would flow to one of the differential branches compared to the other. The reference current-source of the D/A converter circuit is cascoded in order to achieve a sufficiently high output resistance so as not to introduce distortion (section 3.4.1).

The FB1 circuit is actually divided into four equi-sized element. This is done in order to accomplish gain control and to minimize the impact of timing jitter when the input signal is known to be small. Recall that the full-scale range of the modulator is determined by the reference level of the feedback D/A converter (section 3.3). When a full-scale input signal is expected, all four D/A converter elements are switched together. If the input signal is known to be small, then only a single D/A converter element is used. Since only one-fourth of the maximum bias current is switched, the contribution of timing jitter would also be smaller by a factor of four. Similar segmentation scheme is implemented in the FB2 circuit. In this manner a gain-control function can also be embedded within the $\Sigma\Delta$ modulator.

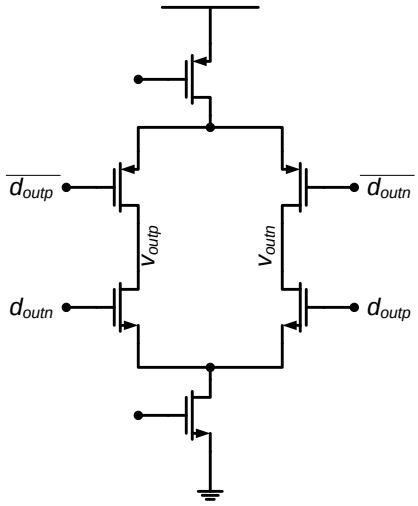


Figure 4.7. Second feedback D/A converter circuit.

4.1.3 Second Feedback D/A Converter (FB2)

The design constraints of the second feedback D/A circuit (FB2) is much less stringent than the FB1 circuit. The amount of charge that needs to be injected to the second integrator is smaller by a factor of β, which is set to take a value of 0.01, compared to the FB1 circuit. Furthermore, noise injected by the FB2 circuit experiences a first-order noise shaping, since it is injected after the first integrator.

The second feedback D/A circuit is shown in figure 4.7. It consists of a pair of NMOS and PMOS current sources along with a set of four switches. The FB2 circuit is also operated as a return-to-zero D/A converter. The presence of a complementary pair of NMOS and PMOS current sources, ensures that each current sources has a discharge path during the return-to-zero period. This prevents the drain voltages of the current sources to collapse during the return-to-zero period. The bias voltages for both the NMOS and PMOS current sources are generated from a single external bandgap reference.

4.1.4 Comparator

The design of the comparator is particularly challenging because of a small input signal amplitude and a very high operating speed. The comparator is enclosed within the $\Sigma\Delta$ feedback loop. As such, it has to complete a cycle of comparison, application of the D/A converter feedback signal and settling of the D/A converter signal within a single clock period. With a target clock period of up to 2GHz (500ps clock period), the comparator has to reach a valid logic level within a period of about 200ps[2]

Based on system simulation, a worst-case minimum input voltage of 10mV can be expected at the input of the comparator. This small input voltage has several important implications towards the design of the comparator. First, a larger gain is needed in order for the comparator to reach full logic levels at the output of the comparator. Second, the comparator is more susceptible to disturbances at the input, such as hysteresis, circuit noise and offset.

A dynamic regenerative latch is chosen for this design. Due to the unstable nature of the circuit, a regenerative latch can achieve a very fast latching speed [88, 42]. The impact of kickback is minimized because the input of the latch is connected to a large integrating capacitor C_{H2}.

The chosen latch circuit, which is called a double-tail latch, is shown in figure 4.8 [94]. The circuit consists of a dynamic preamplifier followed by a clocked SR latch. A transient simulation trace describing the operation of the circuit is shown in figure 4.9. When the $fire\_comp$ signal is low, the comparator is in the reset state. The preamplifier output nodes v_p and v_n is pulled high, and as a result the output nodes v_{lp} and v_{ln} is clamped low. When the $fire\_comp$ goes from low to high, the preamplifier circuit is activated. The two nodes v_p and v_n will be slowly discharged to ground. If there is a differential voltage at the input, the two nodes v_p and v_n will be discharged at a different rate. A differential voltage will develop across the v_p and v_n nodes; this differential voltage can be calculated to be $\frac{g_{m,in}}{g_{ds,in}} \cdot V_{in}$. The voltage difference across v_p and v_n will become the starting point for

[2] A 90nm general-purpose CMOS transistor has an f_T of 120GHz, or a transit time of 1.4ps. [6].

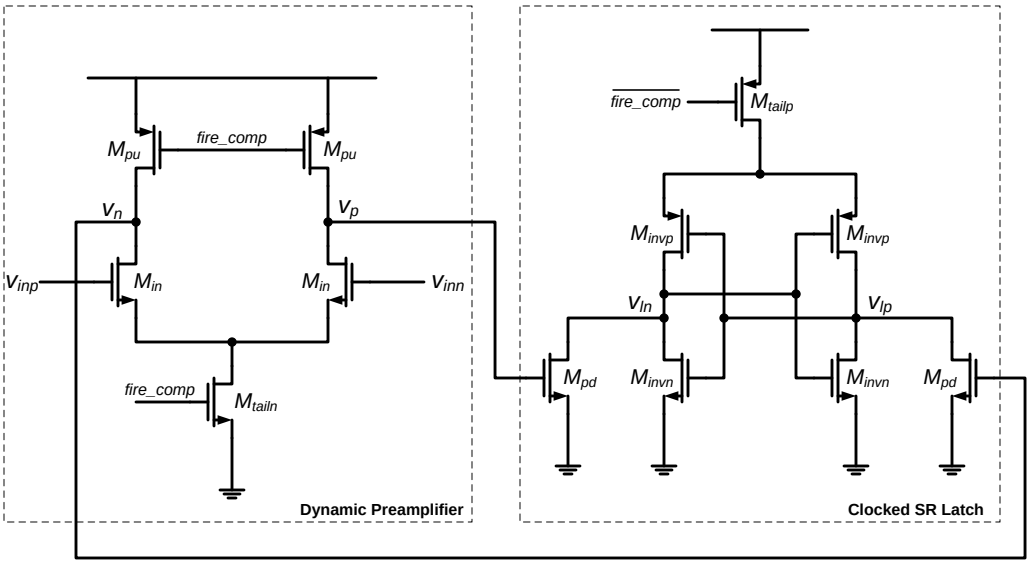


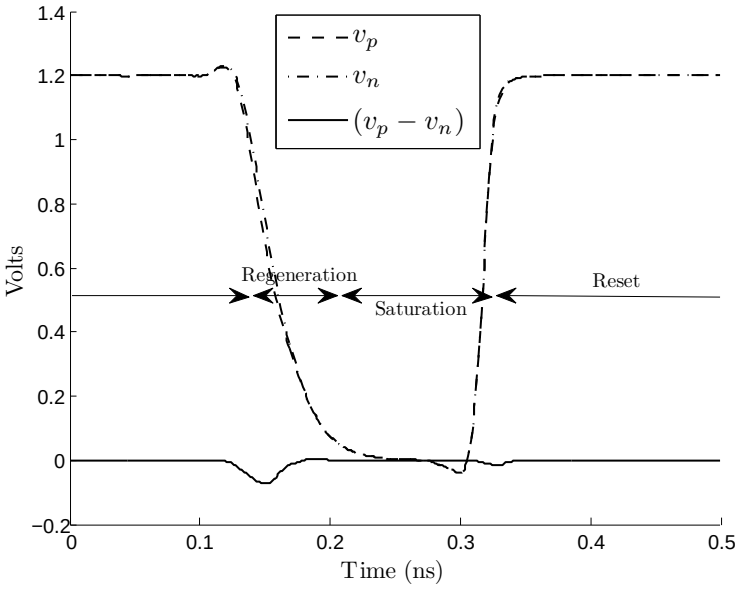
Figure 4.8. A double-tail latch-type voltage sense-amplifier.

the regenerative amplification that occurs within the clocked SR latch. Depending on the polarity of the input signal, a pulse would be generated at one of the differential output of this latch circuit.

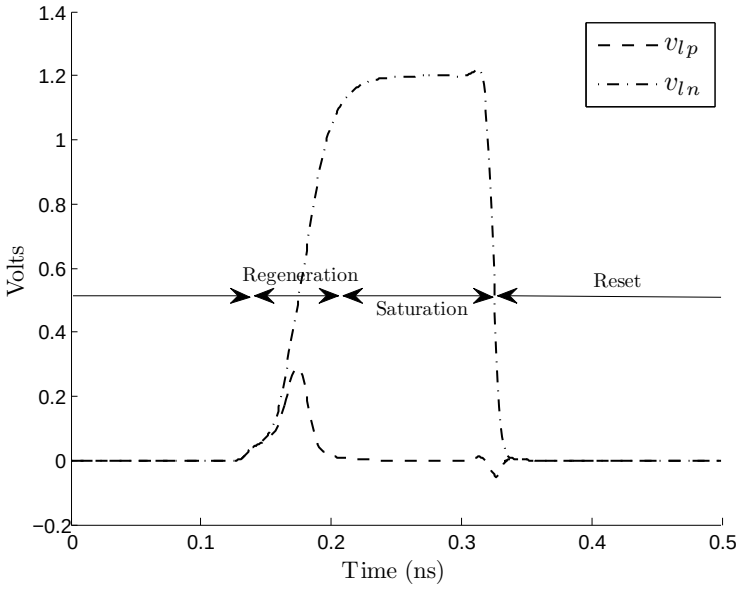
The pulse generated by the double-tail latch is buffered and is then used to drive a second static SR latch (figure 4.10). The output of the SR latch is a static logic level, which can only change once per conversion period. The first inverter in the buffer is skewed in order to avoid metastability. When there is not sufficient time for the comparator to reach a decision, a pulse would not be generated. As a result the static SR latch would not be tripped, and it would retain the last comparison result.

Hysteresis occurs when the comparator's current decision depends on the previous input or output values. The output decision of an ideal comparator with no hysteresis should only depend on its input signal at the current period. Typically hysteresis due to the persistence of the output decision levels is more significant than that due to the input. This is because the output decision levels take full logic values, whereas the input signal level is usually much smaller than a full logic level.

A model of a comparator with hysteresis is shown in figure 4.11. Based on this model,



(a)



(b)

Figure 4.9. Double-tail latch transient simulation.

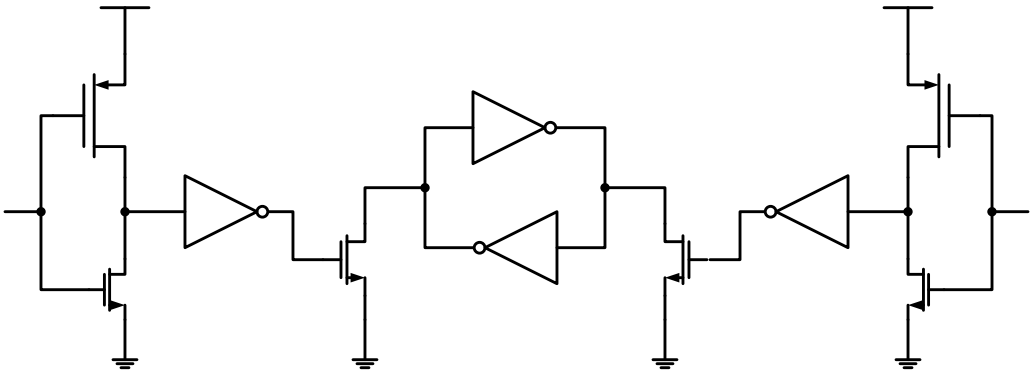


Figure 4.10. Buffer and second static latch following double-tail latch.

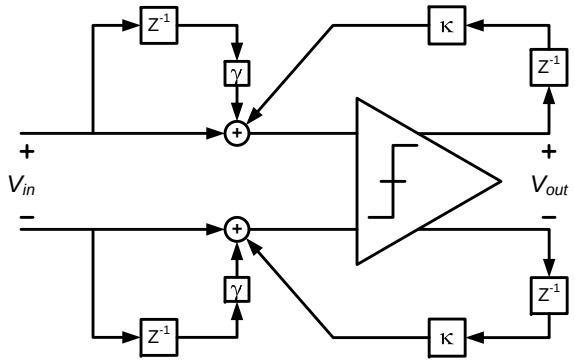


Figure 4.11. Model of a comparator with hysteresis.

acceptable levels of hysteresis, denoted by γ and κ, can be derived through system simulation.

There are a few possible sources of hysteresis. First, if the comparator circuit is not sufficiently reset, then the decision levels from the previous sample would persist. This can be avoided by extending the reset period, or by up-sizing the reset devices. Second, an undesired coupling might exist between the output and input. Undesired coupling can be avoided, or at least minimized, through careful layout.

A best effort is made in order to make the double-tail latch circuit layout to be as symmetric as possible (figure 4.12). This is done in order to minimize the offset of the latch circuit. The signal flow is arranged so that the output signal never crosses the input signal in order to minimize hysteresis. Transistors that are part of a differential pair are interleaved, with dummy transistors placed on both ends.

The comparator is sized based on noise considerations, which will be discussed shortly. A gated-diode preamplifier precedes the comparator circuit described here in order to relax the noise and offset requirements.

Regenerative Latch Noise Analysis

Noise analysis in a regenerative latch is rather complicated due to the fact that the circuit traverses multiple different operating regions. Because of this reason, linear analysis no longer applies. Furthermore, one can argue that the circuit is not even time-invariant. An impulse applied at the input during the reset phase and during the regeneration phase would result in a completely different response at the output.

It is desirable to model the input-referred noise of the latch as a discrete-time noise process. The output of a latch is a discrete-time signal, as it only changes once per conversion period. Furthermore, the input to a latch is usually already sampled and held [3]. The desired model for the comparator is shown in figure 4.13. Now, a method has to be established in

[3] If the input signal is continuous-time, the latch aperture function can be used in order to translate the continuous-time input signal into a discrete-time input signal [36].

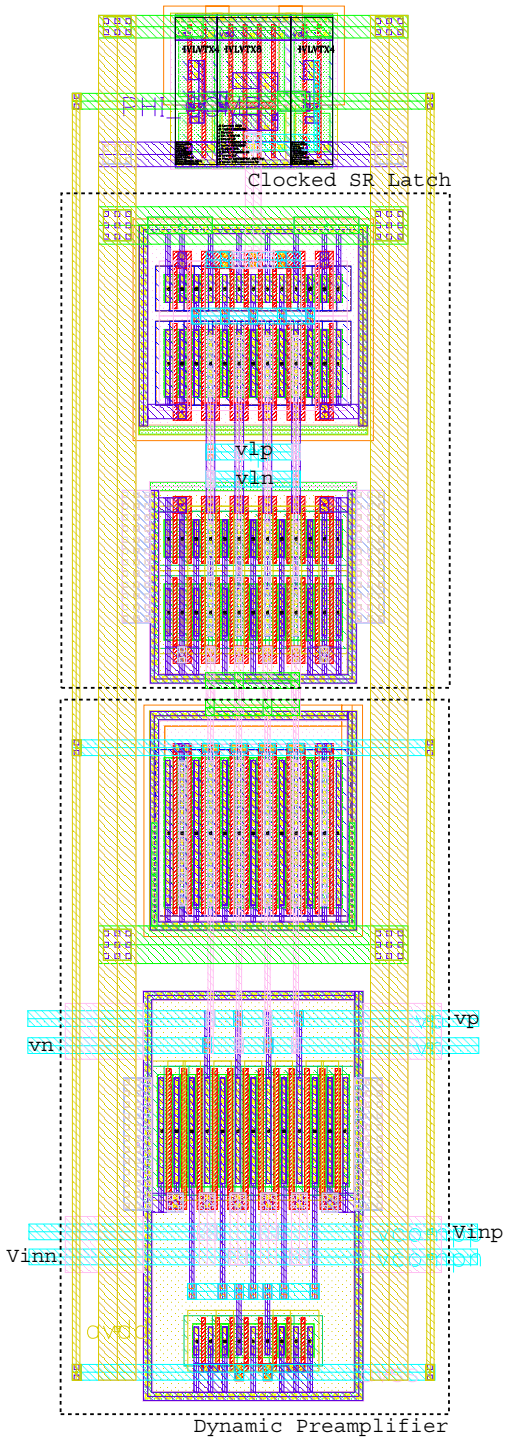


Figure 4.12. Layout of the double-tail latch circuit.

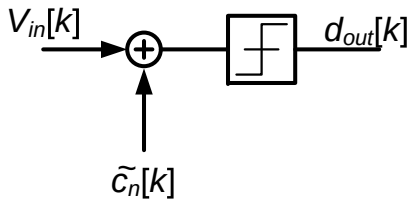


Figure 4.13. Comparator model with noise source.

order to derive the characteristic of this discrete-time noise process, denoted $c_n[k]$ in figure 4.13.

There are a number published approaches on the noise analysis of a regenerative latch [79, 76, 50]. The earliest published approach took a rather simplistic view; the input referred noise of a regenerative latch should be a function of the capacitance at the output node ($\frac{kT}{C_{out}}$) [79]. An approximate analysis is then performed in order to estimate the proper scaling factor, based on the circuit topology. While this approach is intuitively satisfying, it lacks the accuracy needed for proper design of the circuit. Furthermore it does not take into account the effect of flicker noise, which would be dominant in modern CMOS transistors.

The second published approach breaks the circuit analysis into many parts, corresponding to different operating regions of the circuit [76]. On each of these regions, a linear analysis is performed. The final solution of the analysis on each region is used as a starting point for the next region.

The best method to analyze analyze a regenerative latch circuit is to treat it as a linear periodically time-varying (LPTV) circuit [50]. In this manner, noise analysis of a regenerative latch can be performed using the tools of LPTV analysis [25]. It can be easily established that given a constant DC input, the output of a regenerative latch is a periodic signal. In fact, if the input to the comparator is a periodic signal, the output would still be periodic, with a frequency being the greatest common divisor between the frequency of the input signal and the clock period.

It is important to evaluate noise of the latch during the correct time period. Over

one conversion period, there are three distinct operating regions: reset, regeneration and saturation (4.1). During the reset phase, noise in the latch circuit should only matter to the extent that it provides a starting point/initial condition for the regeneration phase. Similarly, in the saturation phase, a valid decision has already been made. As a result some of the devices within the latch circuit are already in cutoff region. At this point, it is not possible for noise from the latch circuit to change the output decision.

It is only during the regeneration phase that random noise is likely to cause an erroneous decision level. During this phase, the input signal along with the circuit noise is exponentially amplified as time progresses. A valid decision level is reached when the result of this exponential amplification reaches a saturation level (V_{DD}). Because of the exponential behavior of the amplification, input signal and noise that are applied at the beginning of the regeneration phase affects the output decision level significantly more than input signal and noise that are applied later on in the regeneration phase. Because of this reason, noise contribution during the later parts of the regeneration period is actually of little importance. It is only noise at the beginning of the regeneration phase that can significantly impact the latch's output decision.

The LPTV analysis is most easily performed using PSS/PNOISE tool as part of SpectreRF simulation suite [101]. The simulation can be setup as follows. A small DC input signal is applied at the input in order to avoid the latch getting into a metastable state. Following the argument in the previous paragraph, circuit noise should be evaluated as a sampled/discrete-time noise process. To accomplish this, the PNOISE analysis can be set to sample the output of the latch circuit at a particular time instant using the `timedomain` options. The output should be sampled in the middle or towards the end of the regeneration phase. Since the dominant noise component is noise arising from the *beginning* of the regeneration phase, the selection of the exact sampling instant is not very sensitive, as long as it is sampled somewhere between the middle and the end of the regeneration phase [50].

The result of the PNOISE analysis is shown in figure 4.14. The dominant noise source is the input transistor pair,M_{in} , of the dynamic preamplifier. When reflected to the input,

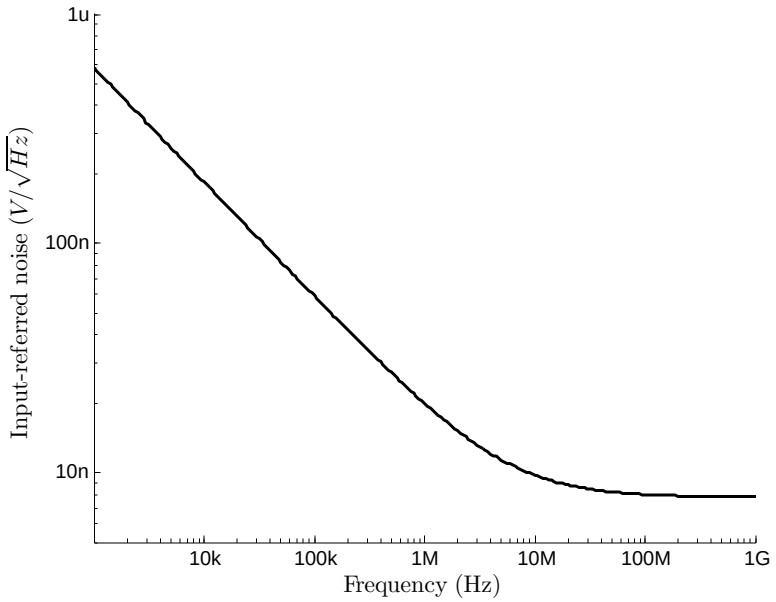


Figure 4.14. Input-referred noise of the double-tail latch (PNOISE simulation).

the noise contributions of the other transistors are attenuated by the gain resulting from the transistor M_{in}.

4.1.5 Gated-Diode Preamplifier

A charge-domain amplifier based on the nonlinear capacitance of the MOS capacitor has been previously proposed. It has been proposed as a sense-amplifier in a memory array under the name of *gated-diode* [54]. In the analog-circuit design community, such an amplifier is referred to as *parametric MOS amplifier* [87, 115]. In this dissertation, the term gated-diode will be used.

Capacitor-based parametric amplification, such as a gated-diode amplifier, achieves signal amplification by virtue of a change in a capacitance. Suppose, a charge Q_i corresponding to an input signal is stored in an isolated capacitor. This stored charge would result in a potential difference of $V_{out} = \frac{Q_i}{C}$, where C is the capacitance of the structure. If the parameter C is changed, then the potential difference across the structure would also change. An amplification is accomplished by sampling the input in a high-capacitance state, and

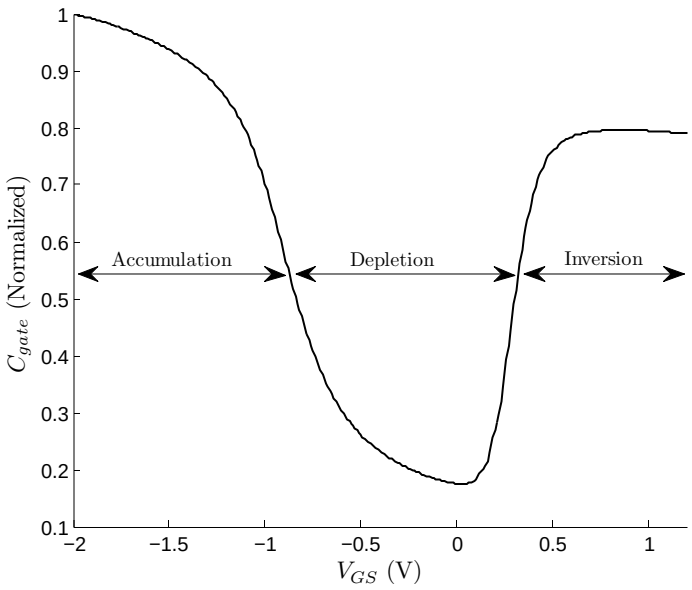


Figure 4.15. MOS transistor gate capacitance as a function of applied gate-source bias.

sampling the output in the low-capacitance state. Therefore a voltage expansion occurs due to a reduction in capacitance.

A MOS transistor, or perhaps more appropriately a MOS capacitor, can achieve parametric amplification due to the dependence of the gate capacitance, C_{gate}, to the applied gate-source voltage. If the input signal is assumed to be a small-signal perturbation around an operating point, $V_{GS,Q}$, then a change of capacitance in the MOS capacitor can be accomplished through changing the gate-source bias voltage. There are three distinct regions in a MOS capacitor: accumulation, depletion and inversion [106], all of which is shown in figure 4.15. In a gated-diode, the input signal is sampled in the inversion region (high capacitance), while the output is sampled in the depletion region (low capacitance).

A gated-diode amplifier is shown in figure 4.16. An amplification of an input voltage occurs in the following manner. First, an input voltage is sampled across the gated-diode and the load capacitance C_L. In this sampling phase, the *Boost* signal is held low, and the *Sample* signal is held high. The DC level of the input voltage is set somewhere mid-scale between 0 and V_{DD}, so that the small-signal operating point occurs in the inversion region. Then the sampling switch is opened, and the *Boost* signal is set to high. At this point

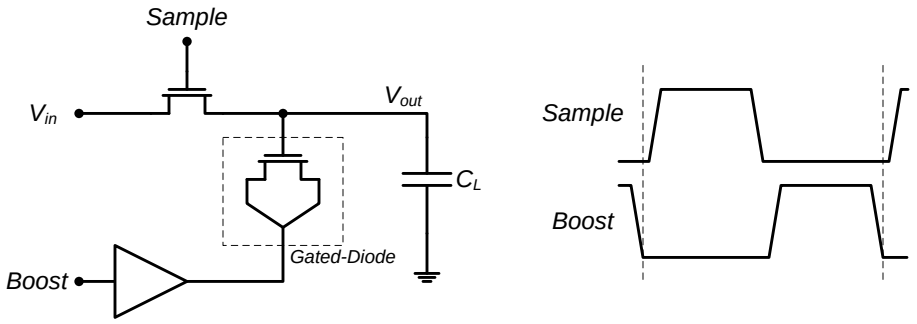


Figure 4.16. A gated-diode amplifier.

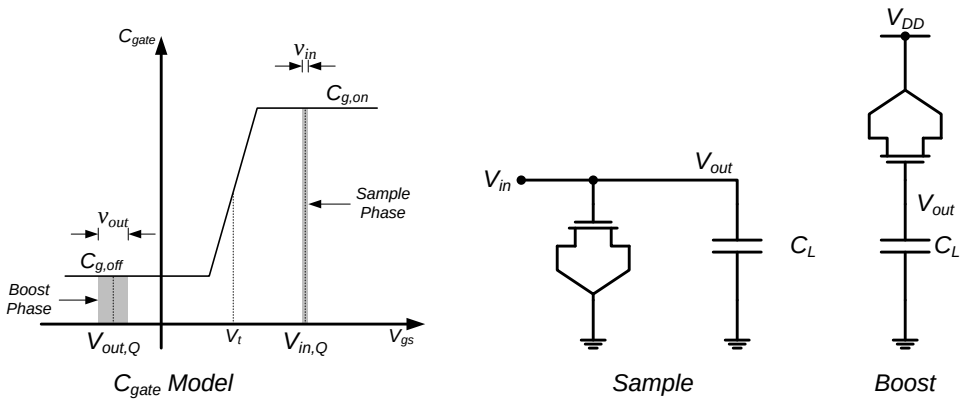


Figure 4.17. Operation of a gated-diode amplifier.

the input charge is trapped at the top plate of the gated-diode and the load capacitance C_L. The change of the *Boost* signal to a high state would also result in a DC bias change accross the gated-diode. As a result the bias point of the gated-diode would be moved to the depletion region.

The gate capacitance can be modeled using a piecewise linear model shown in figure 4.17. The mid-point of the transition between depletion and inversion region is marked by the threshold voltage (V_t) of the MOS transistor.

During the sample phase, the input voltage is sampled, and a charge of Q_i is stored in the gated-diode and the load capacitance:

$$Q_i = C_L V_{in} + C_{g,off} V_t + C_{g,on}(V_{in} - V_t) \tag{4.8}$$

During the boost phase, the charge stored in the system is:

$$Q_f = C_L V_{out} + C_{g,off}(V_{out} - V_{DD}) \tag{4.9}$$

However, since the V_{out} node is isolated during the boost phase, charge-conservation applies:

$$Q_i = Q_f \tag{4.10}$$

and therefore, the following equation would result:

$$V_{out} = \frac{C_{g,on} + C_L}{C_{g,off} + C_L} \cdot V_{in} - \frac{C_{g,on} - C_{g,off}}{C_{g,off} + C_L} \cdot V_t + \frac{C_{g,off}}{C_{g,off} + C_L} \cdot V_{DD} \tag{4.11}$$

Note that all the voltages above are large-signal quantity, and not a small-signal, linearized value.

The capacitance in the depletion region $C_{g,off}$ comprises of the overlap capacitance as well as the gate-to-bulk capacitance:

$$C_{g,off} = W \cdot C_{ov} + WL \cdot C_{gb} \tag{4.12}$$

where C_{ov} and C_{gb} is the overlap capacitance per unit length and the gate-to-bulk capacitance per unit area respectively. On the other hand, the capacitance in the inversion region $C_{g,on}$ corresponds to the inversion layer capacitance plus the overlap capacitance:

$$C_{g,on} = W \cdot C_{ov} + WL \cdot C_{ox} \tag{4.13}$$

where C_{ox} is the oxide capacitance per unit area. Note that $C_{ox} \gg C_{gb}$.

The small-signal gain of the gated-diode amplifier is:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{C_{g,on} + C_L}{C_{g,off} + C_L} \tag{4.14}$$

In order to obtain a large voltage gain, a large ratio of $\frac{C_{g,on}}{C_{g,off}}$ is desired;

$$\frac{C_{g,on}}{C_{g,off}} = \frac{\frac{C_{ov}}{L} + C_{ox}}{\frac{C_{ov}}{L} + C_{gb}} < \frac{C_{ox}}{C_{gb}} \tag{4.15}$$

A maximum gain of $\frac{C_{ox}}{C_{gb}}$ is achieved in the limit that $\frac{C_{ov}}{L} \to 0$. In other word, for a given input capacitance (similarly for a given area, $W \cdot L$), a long and narrow MOS capacitor

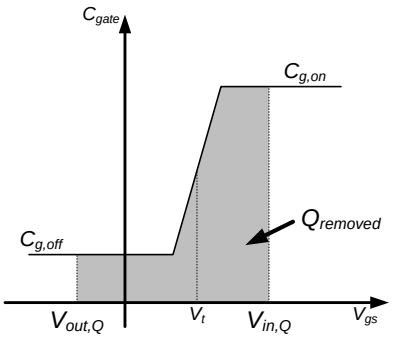


Figure 4.18. Charge removed during application of *Boost* signal.

structure is desired. The limit of this analysis occurs when the fringing capacitance between gate and the substrate, which is not included in this simplified analysis, becomes dominant.

Threshold voltage (V_t) mismatch is usually the dominant mechanism for offset in a differential amplifier. In a differential amplifier, mismatches in V_t is simply reflected to the input as an input-referred offset. From equation 4.11, the sensitivity of the output voltage to V_t variation is

$$\frac{\delta V_{out}}{\delta V_t} = \frac{C_{g,on} - C_{g,off}}{C_{g,off} + C_L} \tag{4.16}$$

Thus, the input-referred offset due to a V_t mismatch of this gated diode amplifier is:

$$\begin{aligned} V_{offset} &= \frac{\frac{\delta V_{out}}{\delta V_t}}{A_v} \cdot \Delta V_t \\ &= \frac{C_{g,on} - C_{g,off}}{C_{g,on} + C_L} \Delta V_t \end{aligned} \tag{4.17}$$

Since both $C_{g,off}$ and C_L are positive quantities, then $\frac{V_{offset}}{\Delta V_t} < 1$. In other words, the input-referred offset is smaller than the variance in V_t. Thus, for a same gate area, a gated-diode amplifier has a smaller input-referred offset compared to a differential-pair amplifier.

There is a movement of charge during the application of the *Boost* signal from ground to V_{DD}. The charge removed, $Q_{removed}$ is equivalent to the shaded area in figure 4.18:

$$\begin{aligned} Q_{removed} &= C_{g,off} \cdot (V_t - V_{out,Q}) + C_{g,on} \cdot (V_{in,Q} - V_t) \\ &= \frac{C_L \cdot (C_{g,on} + C_{g,off})}{C_L + C_{g,off}} \cdot (V_t - V_{in,Q}) - \frac{C_{g,off}^2}{C_{g,off} + C_L} \cdot V_{DD} \end{aligned} \tag{4.18}$$

The operating speed of the gated-diode amplifier depends on how fast the charge $Q_{removed}$

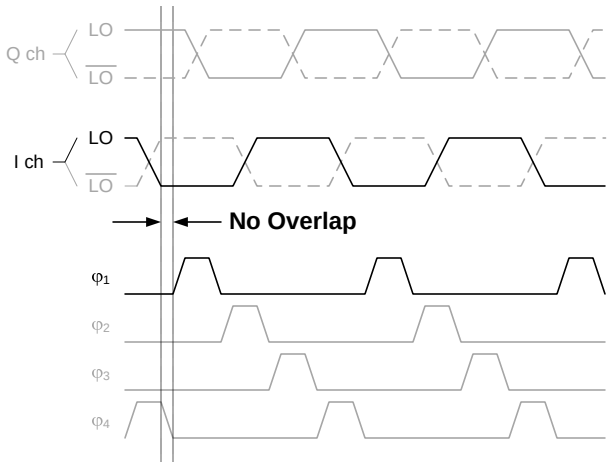


Figure 4.19. Non-overlap requirements in timing generation.

can be discharged from the gated-diode structure. Furthermore, the amount of charge removed also determines the power consumption of the gated-diode amplifier.

4.1.6 Clock Generation

Two sets of timing signals are needed for the proper operation of the ΣΔ Receiver (figure 4.1). The first set consists of the I and Q LO signals to drive the sampling mixer switches. There are four of such signals, LO_I, LO_Q and their complements. The second set of signals consist of four non-overlapping clock signals φ_1 to φ_4. There is only one alignment conditions; φ_1 can only go high after LO_I signal goes low (figure 4.19). As long as this condition is met, all other clock signals will be properly aligned. This occurs because each of the two sets of clocking signals, the LO and φ, consists of four identical and delayed signal waveform.

The general clock generation strategy is shown in figure 4.20. An external clock reference at twice the LO frequency is brought in to the chip to drive the clock generation circuits. The input clock arrives as a sine-wave at about 0dBm power level. This external clock reference is buffered and regenerated to a full CMOS level. The buffered clock signal is then split into two parts. The first part generates the four LO clock phases using a divide-

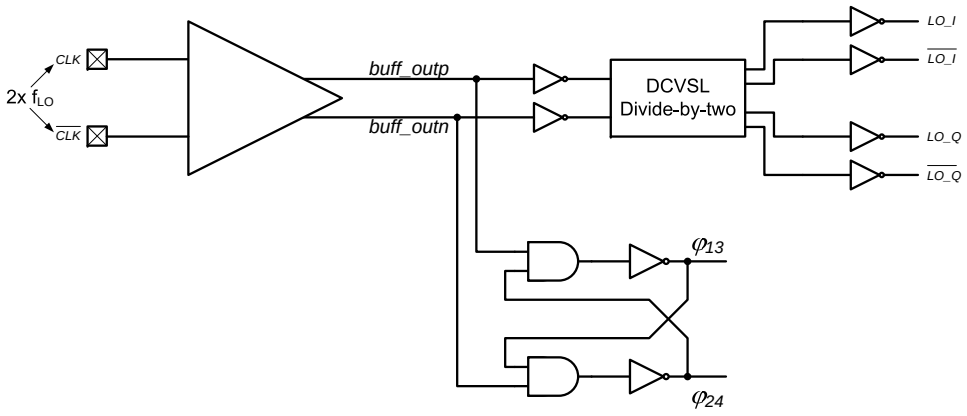


Figure 4.20. Clock generation strategy.

by-two circuit. The second part is used to generate the four non-overlapping clock phases φ_1 to φ_4.

As elaborated in chapter 3, the $\Sigma\Delta$ receiver is quite sensitive to timing jitter. Particular care has to be exercised such that the input clock buffer does not add a significant amount of jitter. Furthermore, the duty-cycle of the input clock reference is also of importance. If the duty-cycle of the input clock is not balanced, then there would exist a gain mismatch between the I and Q channels as well as within the top and bottom paths within each of the I and Q channels. This imbalance would result in a DC offset as well as a reduction in the image rejection ratio.

The input clock buffer circuit is shown in figure 4.21. A 50-ohm termination resistor is present in order to eliminate signal reflection. The test board on top of which the chip is mounted would have a 50-ohm impedance-controlled transmission line for the clock signals. The clock signals then undergoes linear amplification through two differential amplifiers. The goal is to sharpen the edge-transitions before the clock signal is fed into a CMOS inverter/buffer [33]. This scheme is done in order to minimize jitter as well as in order to reduce the duty-cycle mismatch resulting from threshold voltage variation from the CMOS inverters.

The outputs of the first inverters are tapped to drive a pair of dummy inverters. The outputs of these dummy inverters are low-pass filtered and is fed out to a pad. By noting

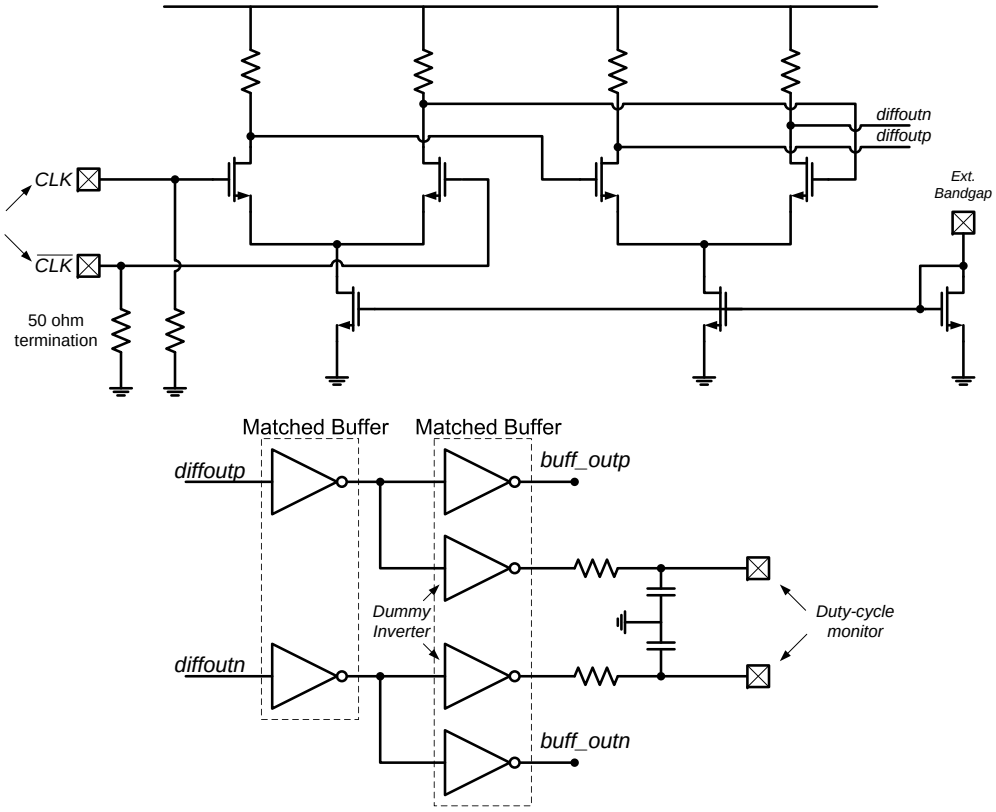


Figure 4.21. Input clock buffer circuit.

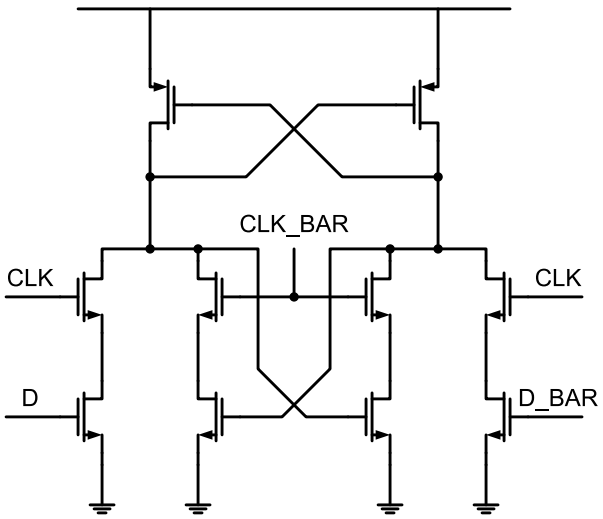


Figure 4.22. DCVSL D-latch.

the average DC voltage of the output of these two inverters, the duty-cycle error of the clock signal can be inferred. If a perfect 50-percent duty-cycle is achieved, then the output of both pads should be exactly at $\frac{V_{DD}}{2}$[4]. The layout of the matched CMOS inverters is interleaved in order to minimize device-to-device mismatch.

The divide-by-two circuit is composed of two back-to-back D-latches. The D-latch is implemented in a differential cascode voltage switch logic (DCVSL) logic style [86]. The circuit schematic of the D-latch is shown in figure 4.22. A time delay is introduced by inserting a buffer after the divider circuit. The time delay is necessary in order to ensure proper alignment between the LO and φ signals as illustrated in figure 4.19. Parasitic extraction was performed on the circuit layout, and simulations were performed across process corners in order to verify that the no-overlap condition is always met.

The φ signals are generated using a non-overlapping clock generator shown at the bottom of figure 4.20. The delay along the AND gate and the inverter ensures that there is a non-overlap period between the two output of this circuit. The φ signal is distributed across the chip as φ_{13} and φ_{24} in order to minimize the number of clock drivers. At the

[4]Duty-cycle correction is not done automatically on-chip. Duty-cycle error is corrected on the test-board by changing the DC bias of the positive and negative inputs of the differential CLK signal.

destination, the φ_1 to φ_4 signal is generated by putting the φ_{13} or φ_{24} through an AND gate with one of the appropriate LO signal. For example, the φ_3 signal is generated by putting φ_{13} and LO_I signal through an AND gate (refer to figure 4.19).

4.2 Test-Chip Prototype

The $\Sigma\Delta$ receiver circuit is fabricated in ST Microelectronics, seven-metal layers, triple-well 90nm CMOS technology. The technology features a multiple V_t option. Low V_t devices are used extensively in order to get the maximum transistor f_T. No other special process options were used in this test chip.

A floorplan of the test-chip is shown in figure 4.23. As mentioned earlier, both I and Q channels are implemented in the chip. The two channels are identical, except that the timing signals for the Q channels are delayed by a quarter of a period. The input reference clock is fed to the chip from the left side, while the input signal is fed from the right side. All the analog block is placed in a compact area between the large loop-filter capacitors. In this manner, all signals are routed across a compact area.

The clock generation circuits are located in between the two I and Q channels. This arrangement is chosen to minimize the clock skew between different parts of the chip. The output of the clock generation block is buffered before being distributed across the I and Q channels. Standard-cell library CMOS inverters are used as clock buffers in the distribution network.

The total output data rate of the chip is $4 \cdot f_{LO}$. There are four paths in the receiver, two on each I and Q channels, each of which is run at f_{LO}. With a maximum f_{LO} of 1.7GHz, an output data-rate of 5.6Gbps can be expected. Sixteen LVDS driver pairs are used in order to drive the data off-chip. A four-to-one serial-to-parallel conversion is done in order to bring the data rate down to 425Mbps per LVDS pin pair.

A custom FPGA-based data-acquisition system, called the interconnect Breakout Board (iBOB), is used to interface with the chip [3]. A master clock is generated inside the test-

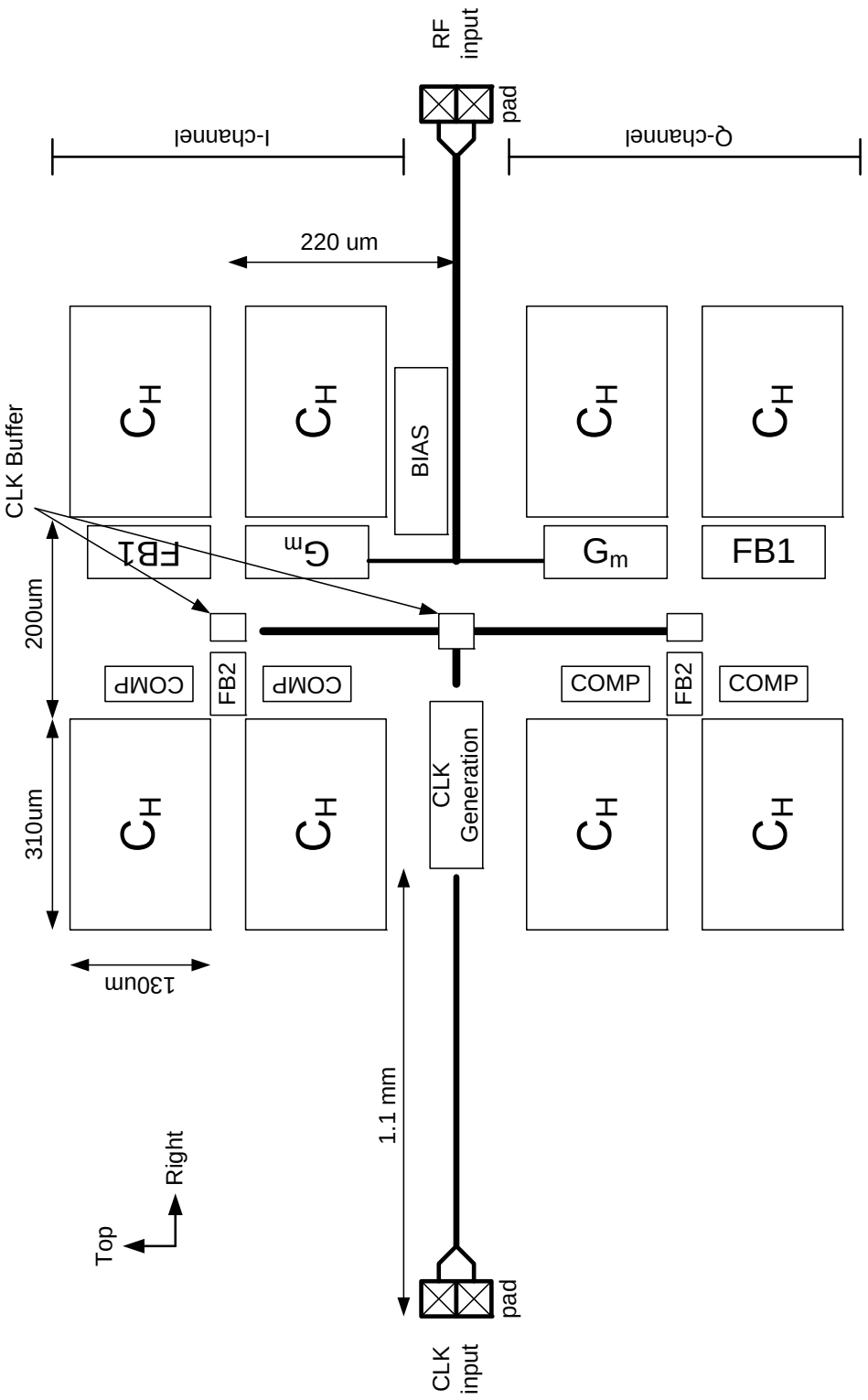


Figure 4.23. Floorplan of test-chip (not to scale).

chip by dividing the LO signal by a factor of four. This master clock is then used by the data-acquisition system to synchronize the data transfer. A divide-by-eight option is also implemented in the chip in order to accommodate a double-data-rate (DDR) mode. In the DDR mode the FPGA within the acquisition system can be run at a rate of $\frac{f_{LO}}{8}$ instead of $\frac{f_{LO}}{4}$, while maintaining the same input throughput.

There are three ground references and three supply voltages in the test chip: analog ground (AVSS), digital ground (DVSS), pad ground (VSS_2V5), analog supply (AVDD), digital supply (DVDD) and pad supply (VDD_2V5). Both AVDD and DVDD is designed to take 1.2V supply. On the other hand, the pad driver requires a supply voltage of 2.5V. The substrate is connected to DVSS.

All analog circuits are enclosed in n-well tubs to minimize undesired coupling, especially from the clock buffers and the LVDS drivers. The presence of the n-well tub also enables the analog ground to be separated from the digital and pad ground. The library pad drivers are also enclosed in dedicated n-well tubs, which provides further isolation from the sensitive analog circuits.

Except for the last-stage clock buffer, which is tied to analog supply and ground, all clock buffers are connected to the digital supply and ground.

The three supply voltages are generated on the test board; each with a dedicated voltage regulator. The AVSS and DVSS ground references are tied together at the test board at a single point. An RF choke is used to short together these two references at DC, while providing isolation at high frequency. The pad ground is referenced to the ground signal of the acquisition board.

A microphotograph of the test-chip is shown in figure 4.24. The test-chip measures 2.4mm by 1.6mm. The core area is 1mm by 0.8mm.

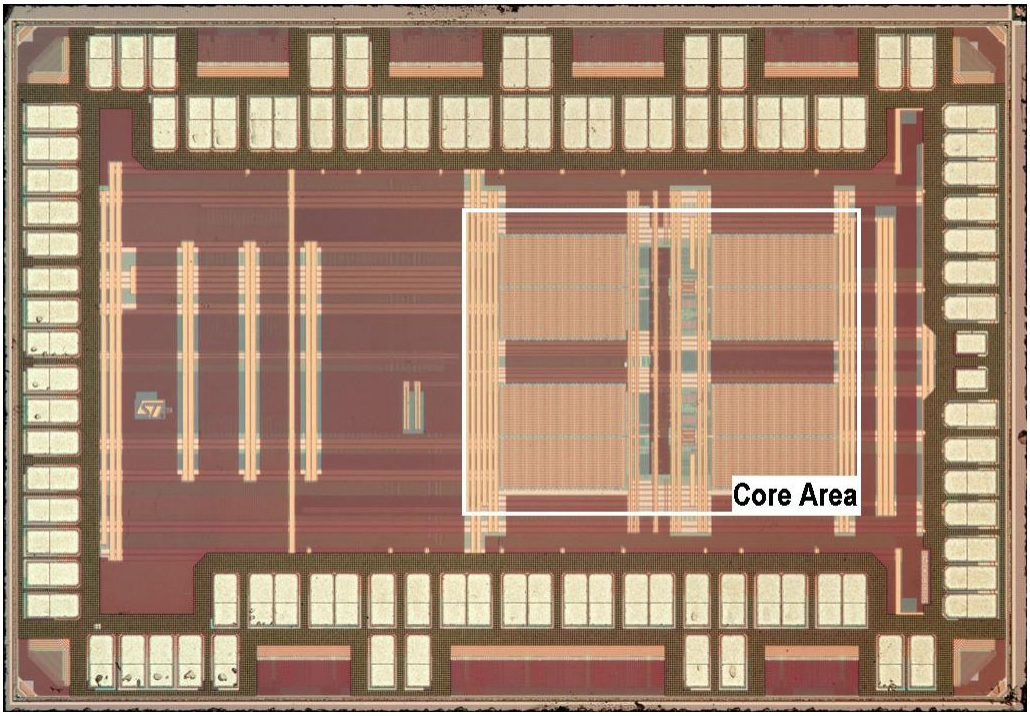


Figure 4.24. Microphotograph of test-chip.

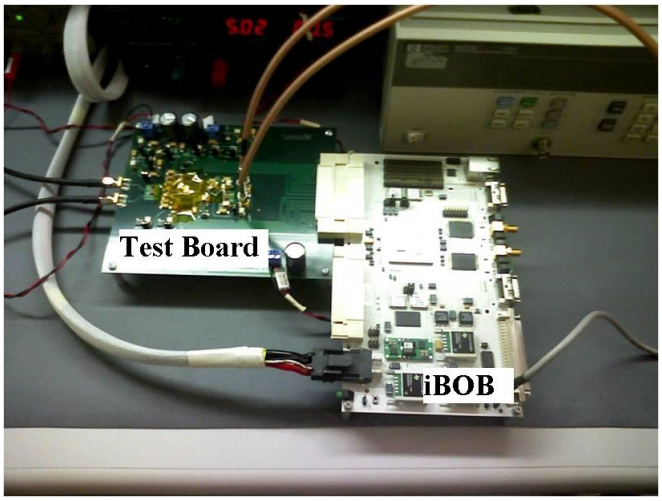


Figure 4.25. Test Setup.

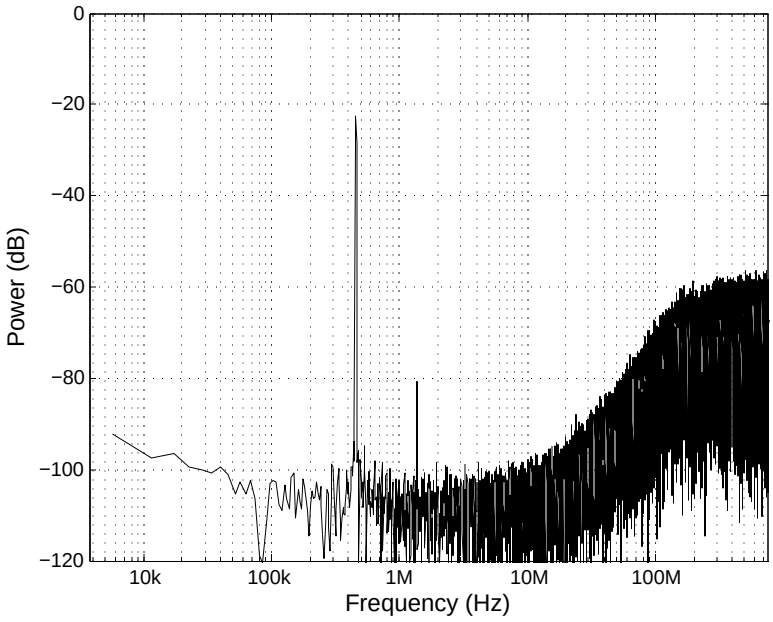


Figure 4.26. Power-spectral density of output data at $f_{LO} = 1.5$GHz.

4.3 Measurement Results

An Agilent 4438C signal generator with low-jitter option is used to provide a clean timing reference [1]. The phase-noise profile of this synthesizer has been previously shown in figure 2.17. A custom FPGA-based data-acquisition system is used to download the data to a PC, where further analysis is performed.

A perfect brick-wall filter is assumed in all measurements. DC offset at the output is nulled out in all spectrum plots. Losses in baluns and bias-T as part of the measurement setup have been taken into account in the presentation of the measurement results.

Figure 4.26 shows the output spectrum of the $\Sigma\Delta$ receiver, taken with an f_{LO} of 1.5GHz. The input signal is located at 1GHz + 312kHz. A 40-dB noise shaping profile can be observed; which confirms the second-order noise-shaping properties of the modulator. A dominant third-order distortion is observed. The third-order distortion term is a result of the nonlinear voltage-to-current conversion in the transconductance amplifier.

A sweep of SNR and SNDR as a function of input power is shown in figure 4.27. A

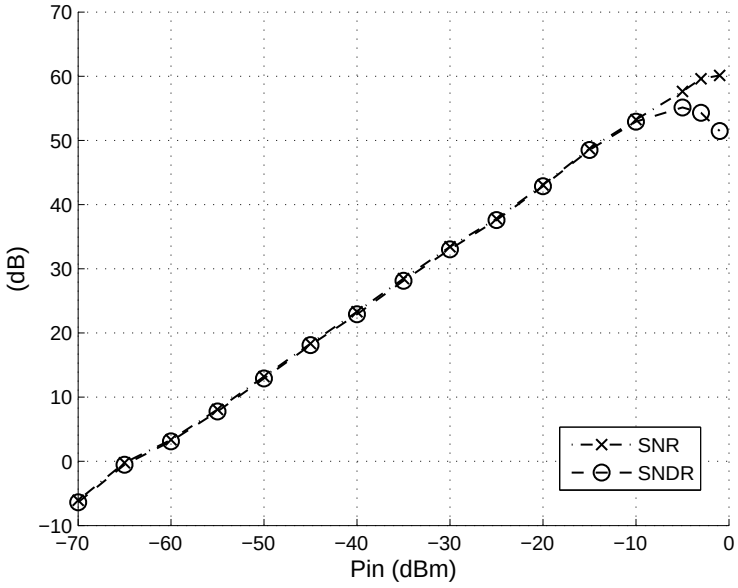


Figure 4.27. SNR and SNDR as a function of input power at $f_{LO} = 1.5$GHz.

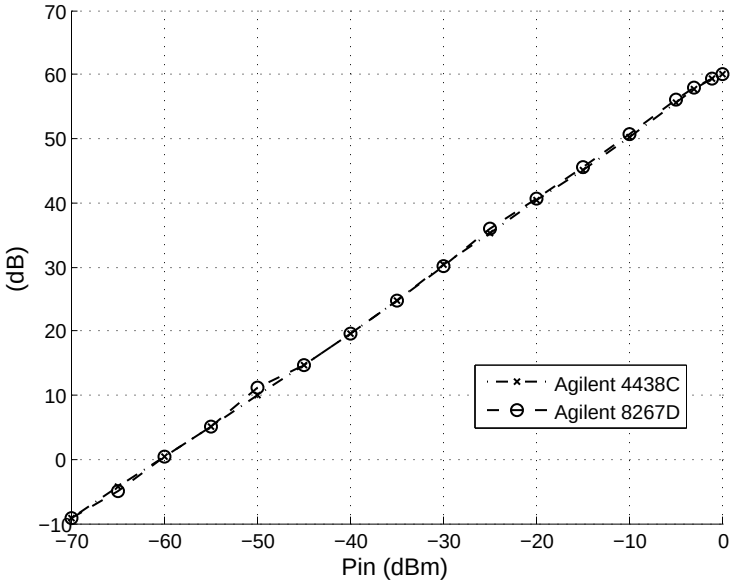


Figure 4.28. Performance comparison of the ΣΔ receiver with two different clock sources [1, 2].

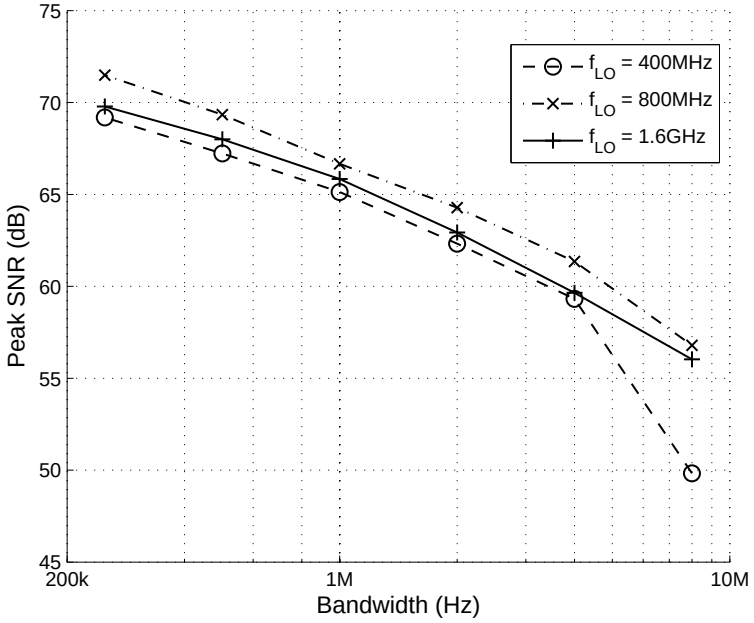


Figure 4.29. SNR as a function of signal bandwidth at different f_{LO} frequencies.

peak SNR of +60dB is achieved at $f_{LO} = 1.5$GHz. A peak SNDR of +55dB is achieved at the same frequency. The dominant distortion term is the third-order distortion term, which is also present in figure 4.26. Noise is dominated by timing uncertainty or timing noise arising from the input clock reference. Timing uncertainty from the reference, degrades the SNR of this receiver through two mechanisms: reciprocal mixing and jitter at the feedback D/A converter. This test was also performed using another signal generator, which yields a similar result (figure 4.28).

A characterization of the noise profile across different signal bandwidths is presented in figure 4.29. Peak SNR is recorded for different signal bandwidth, assuming a perfect brick-wall filter. The overall noise profile is white up to a signal bandwidth of 8MHz. A 3-dB SNR penalty occurs per doubling of the signal bandwidth. For a low f_{LO} rate of 400MHz, quantization noise dominates the SNR at high bandwidth, due to the low oversampling ratio.

The center frequency of the down-converting $\Sigma\Delta$ modulator is set by the LO frequency. A characterization of the performance of the circuit as a function of LO frequency is dis-

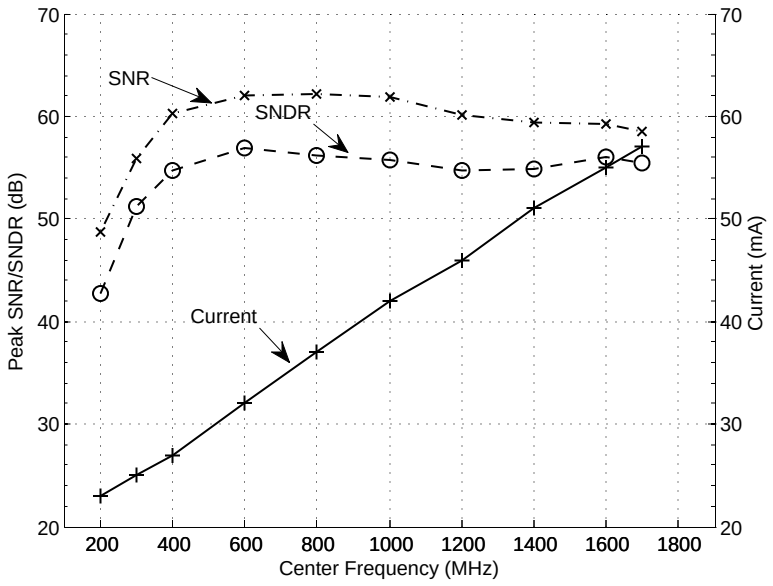


Figure 4.30. SNR, SNDR and power consumption at different f_{LO} frequencies for a 4-MHz bandwidth.

played in figure 4.30. SNR is greater than +59dB at LO frequencies ranging from 400MHz to 1.7GHz. At low LO frequencies, quantization noise starts to dominate due to the low oversampling-ratio at that conversion rate. Above 1.7GHz, the modulator starts to break down due to insufficient time to complete a cycle of comparison and application of feedback signal within a single conversion period. Power consumption of the circuit as a function of the conversion rate is also displayed, where the supply voltage is 1.2V. Because of the use of a switched-capacitor loop filters, there is a linear increase in power consumption as the conversion rate is increased (CV^2f).

A breakdown of the chip's power consumption is illustrated in figure 4.31. A large portion of the power is consumed in the clock buffers, needed to distribute a high-speed clock across the chip.

The receiver linearity can be measured by means of its 3-dB desensitization level. A 3-dB desensitization level is a level at which the SNR (or SNDR) of the receiver degrades by 3-dB. The measurement is setup as follows; first, a small in-band tone is inserted, and the resulting SNR is measured. Then, two tones at 100kHz apart is injected with a total power of P_{in}, at some offset frequency from the carrier. For each offset frequency, the input

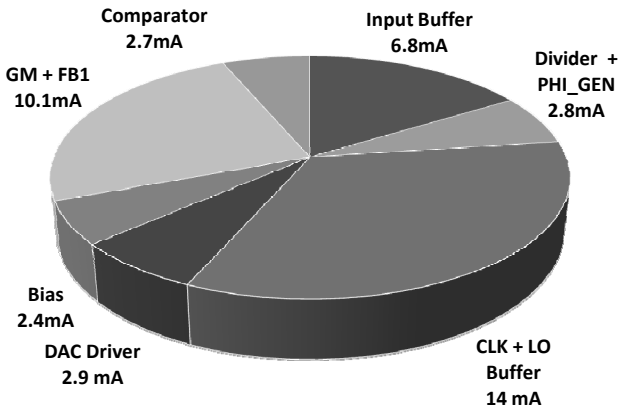


Figure 4.31. Breakdown of power consumption at $f_{LO} = 1\text{GHz}$ ($V_{DD} = 1.2\text{V}$).

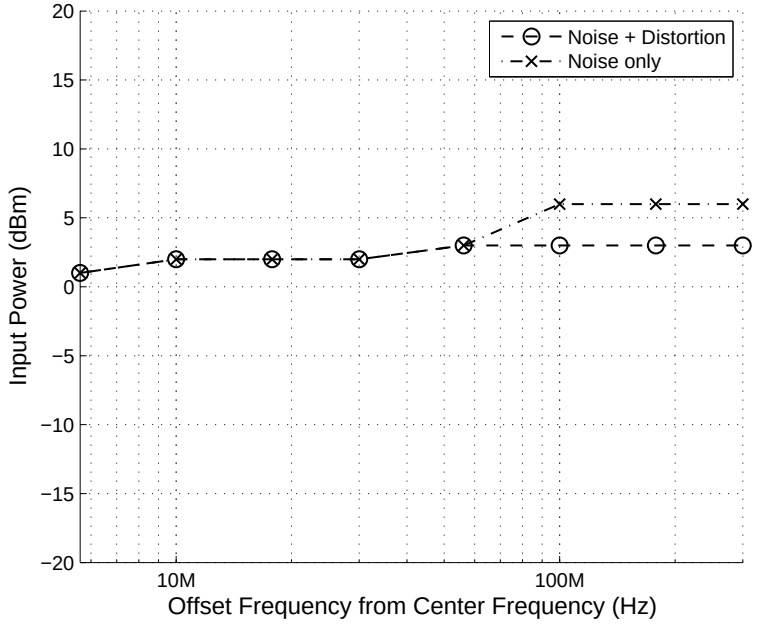


Figure 4.32. Out-of-band 3-dB desensitization levels with a 4-MHz bandwidth.

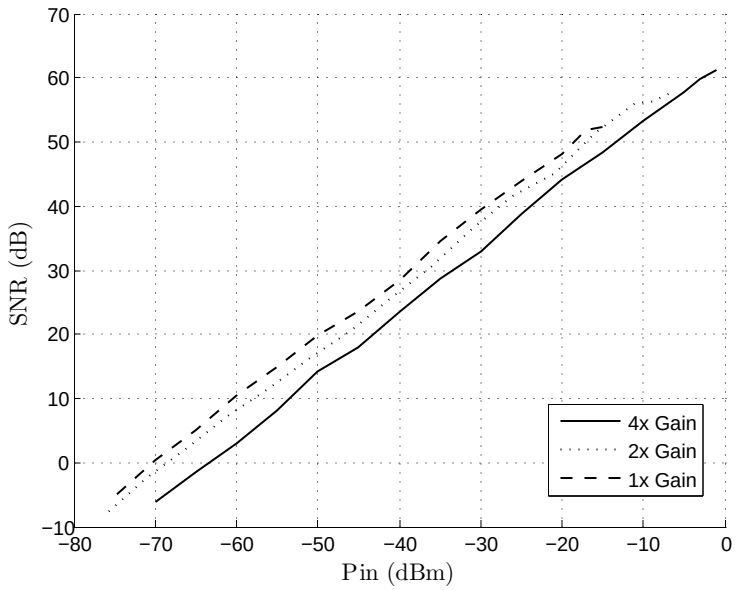


Figure 4.33. Gain control and the resulting SNR.

power of the two tones, P_{in}, is increased to the point where its SNR (or SNDR) degrades by 3dB. That input power level is called the 3-dB desensitization level.

The 3-dB desensitization level for this downconverting $\Sigma\Delta$ modulator is set by the modulator overload level. The SNDR 3-dB desensitization level is set by the second-order intermodulation product.

The $\Sigma\Delta$ receiver has a built-in gain control, by virtue of changing the reference current of the feedback D/A converter. This feature is characterized in figure 4.33. Since jitter is

Table 4.1. Performance summary of the $\Sigma\Delta$ receiver.

Parameter	Value
Bandwidth	up to 8MHz
Center Frequency	400MHz-1.7GHz
IIP3	+19dBm
IIP2	+70dBm*
SFDR	57dB
Min. input-ref. noise	$45\text{nV}/\sqrt{Hz}$
Power Consumption	50mW (@f_{LO} = 1GHz)

* Limited sample of two dies

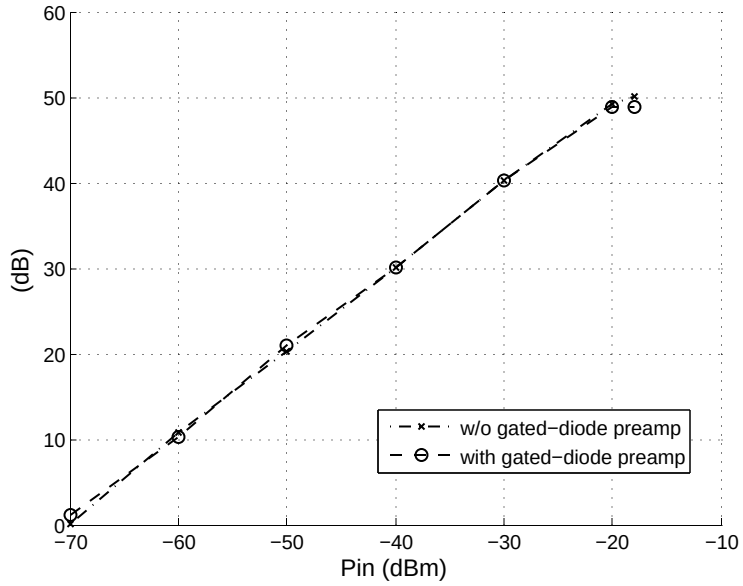


Figure 4.34. SNR improvement due to gated-diode amplifier, taken at the minimum gain setting.

the dominant noise source, reducing the feedback D/A converter reference current improves the SNR at lower input power, at the expense of a lowered full-scale range. However, as the D/A converter reference current is further reduced, other noise source, such as thermal noise and flicker noise, becomes dominant. The minimum achievable input noise floor is $45\text{nV}/\sqrt{Hz}$.

The application of the gated-diode amplifier improves the SNR by less than 0.5 dB at the gain setting corresponding to the highest sensitivity level (figure 4.34). Even at this gain setting, noise from the comparator circuit is not a dominant noise source. Therefore, the application of the gated-diode amplifier only present a marginal improvement in the overall noise of the system.

4.3.1 Comparative Analysis

The $\Sigma\Delta$ receiver is designed to take a signal at the output of an LNA and converts it to a digital representation. It is assumed that an LNA with a 20-30dB power gain precedes the $\Sigma\Delta$ receiver circuit. When the gain of the LNA is taken into account, table 4.1 needs to

Table 4.2. Performance summary of the ΣΔ receiver evaluated at the antenna with a 20dB-gain LNA.

Parameter	Value
IIP3	-1dBm
IIP2	+50dBm*
SFDR	57dB
Min. input-ref. noise	$4.5\text{nV}/\sqrt{Hz}$

* Limited sample of two dies

be re-derived to reflect the receiver's performance evaluated at the antenna. The result of the aforementioned conversion is presented in table 4.2. The result of this analysis is highly dependent on the assumed gain of the LNA. A higher LNA gain would make the noise of the ΣΔ receiver circuit less significant, however it would also reduce the full-scale of the overall receiver.

Comparing table 4.2 with the performance requirement set in table 2.2, it is clear that the ΣΔ receiver in its present version comes short in a few key specification in order to support some of today's most challenging wireless standards. The ΣΔ receiver does not have a sufficient dynamic-range in order to support these standards.

The ΣΔ receiver achieves an IIP3 of +19dBm, which is competitive when compared to published circuits. Since the proposed circuit operates at the output of an LNA, it is fair to compare it with published example of mixer circuits. A comparison of IIP3 of published mixer circuits is shown in table 4.3.

The high in-band IIP3 of this receiver is accomplished due to the presence of the ΣΔ modulator feedback. Typically, linearity of a mixer is limited by output compression. However, as discussed earlier in this chapter, the passive mixer circuit actually only processes the error-signal of the ΣΔ modulation, which is much smaller than the input signal. As a result the voltage swing at the output of the transconductance amplifier is much reduced when compared to a typical mixer configuration.

Using IIP3 as proxy for measuring linearity, one can argue that the dynamic-range limitation of the ΣΔ receiver is not due to the full-scale range, but more from an insufficiently

Table 4.3. IIP3 comparison of published down-conversion mixer.

Author	IIP3	Supply Voltage
[91] Sacchi	-1dBm	1.8V
[117] Zhou	+5dBm	1.8V
[55] Brandolini	+14dBm	1.8V
[89] Razavi	+3dBm	1.5V
[97] Shahani	+10dBm	1.5V
[85] Poobuapheun	+11dBm	1.5V
This Work	+19dBm	1.2V

low noise-floor. This can also be observed from the minimum input-referred noise magnitude of 45nV/$\sqrt{Hz}$. As a reference, 50-ohm noise of the antenna corresponds to a spot noise of 0.9nV/$\sqrt{Hz}$. Thus in order to achieve a sub 3-dB noise figure, a large LNA gain of more than 30dB is necessary.

The dominant source of noise in the receiver comes from timing jitter. The chosen topology is particularly sensitive to jitter due the use of a single-bit D/A converter with a return-to-zero coding. A choice of a non-return-to-zero coding combined with a multi-level D/A converter would significantly reduce the jitter sensitivity of the receiver architecture.

It should also be noted that the maximum *in-band* SNR is ultimately limited by reciprocal mixing. As discussed in section 2.5.2, the maximum achievable SNR at a 4-MHz bandwidth is 67dB. It is important to realize that the noise arising from reciprocal mixing is dominated by the close-in phase noise of the frequency synthesizer. Whereas jitter would present a noise floor regardless of the input signal; SNR limitation due to reciprocal mixing only applies to cases where there is a large *in-band* signal.

4.3.2 Possible Improvements

The first problem to be addressed of the current circuit implementation is to lower its sensitivity to timing jitter. Random timing variation modulates the location of the edges of the output waveform of the feedback D/A converter. As a result the amount of feedback charge injected into the system is modulated by this random noise process (section 3.4.1). In order to mitigate the effect of timing jitter, one can either reduce the number of

Table 4.4. Potential improvement in SNR due to a multi-bit ΣΔ architecture with an NRZ coding.

Number of D/A converter steps	Improvement from a 2-step D/A converter
2	0dB
3	2.3dB
4	4dB
8	10.6dB

transitions or reduce the step size of each transition. This can be accomplished by using a non-return-to-zero coding scheme and by using a multi-bit ΣΔ modulator topology [81].

In an NRZ-coded waveform, there can only be at most one transition per clock period, compared to exactly two transitions per clock period for RTZ-coded waveform. An NRZ coding scheme would lower the resulting noise arising from timing jitter by 3dB (assuming jitter is a white noise process). Furthermore, if the output data does not change from the previous period, then no transition would occur. This would again reduce the resulting noise from timing jitter.

A multi-bit ΣΔ modulator design would further reduce the sensitivity to clock jitter by reducing the step-size per transition. Because of oversampling, it is very unlikely for a transition to span more than one LSB. Using system simulation, a potential improvement due to a multi-bit architecture is summarized in table 4.4 [5]. When a 3-bit or 8-step feedback D/A converter is used, an improvement of more than 10dB can be expected.

The power consumption of the current implementation of the ΣΔ receiver is dominated by the power consumed by the clock buffers. A continuous-time implementation of the loop filter can be explored to lower the power consumption of the receiver. However, care must be taken in the implementation of a continuous-time loop filter, such that signal aliases are sufficiently attenuated prior to sampling. Recall that in this discrete-time implementation, the problem of aliasing is completely avoided by keeping the sampling rate of the ΣΔ modulator to be exactly the same as that of the LO frequency.

Last, a higher-order loop filter can be implemented in order to achieve a higher signal

[5] This simulation result is only approximate, since the result is dependent upon the characteristics of the input signal

bandwidth. The second-order loop filter used in this design is capable of reaching an SNR of 60 dB across a 20MHz bandwidth (table 3.2). A higher-order loop filter would enable a higher dynamic-range across the same bandwidth.

Chapter 5

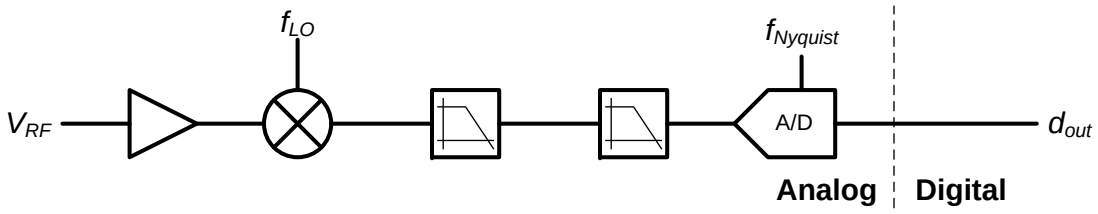
Conclusion

5.1 Summary

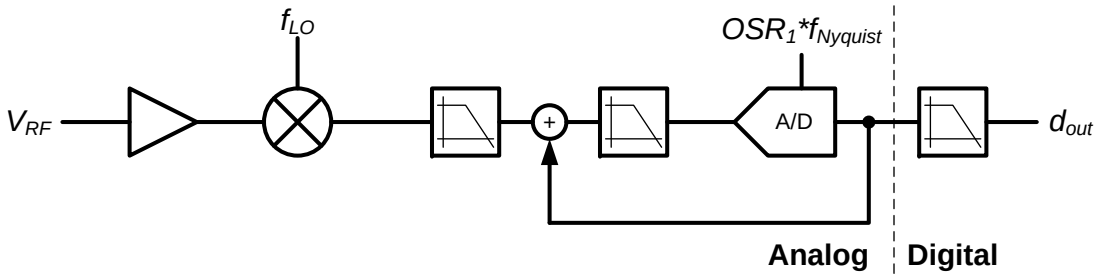
In this work, we present a downconverting $\Sigma\Delta$ A/D converter as a highly reconfigurable RF receiver. An oversampled, noise-shaping $\Sigma\Delta$ A/D converter is the ideal choice for A/D conversion of a radio-frequency signal. Oversampling is necessary in order to avoid signal and noise folding. Quantization-noise shaping provides a high-resolution conversion only in the frequency-range of interest and it avoids the need for a high-speed *and* high-resolution quantizer.

We recognized that the output of a mixer driven by a square-wave local-oscillator (LO) signal is already a discrete-time signal. This mixing process already results in undesired signal folding. As a corollary to this assertion, the output of a mixer is already a band-limited signal, with a bandwidth spanning from DC to f_{LO}. Thus, in this respect, sampling in an RF receiver occurs much earlier than where it is traditionally recognized, which is within the A/D converter.

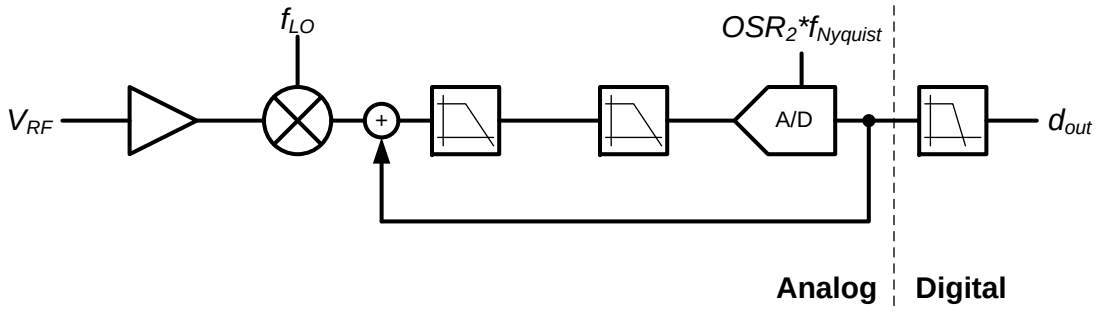
A receiver architecture is developed where a sampling-rate of f_{LO} is maintained within the receiver. Since there is no additional frequency down-conversion, no additional aliasing or folding occurs. Furthermore, the high sampling rate allows the use of a very simple, passive switched-capacitor filter as a loop filter for the $\Sigma\Delta$ modulator.



(a) An RF receiver with a Nyquist-rate A/D converter



(b) An RF receiver with an oversampled ΣΔ A/D converter



(c) A ΣΔ receiver architecture

Figure 5.1. Comparison of three RF receiver architectures

The use of an oversampled ΣΔ converter has resulted in modifications of RF receiver architectures. Whereas in the past a Nyquist-rate converter follows a high-order low-pass filter (figure 5.1(a)), the relaxed anti-aliasing requirement of a ΣΔ A/D converter allows for a simpler/lower-order baseband filter design (figure 5.1(b)). The work of this dissertation takes the evolution of RF receiver architectures one step further by completely eliminating all baseband filters. The RF signal is directly converted to digital at the output of the down-conversion mixer (figure 5.1(c)).

There has been a long discussion as to the effort of moving A/D conversion in an RF receiver closer to the antenna [95]. Given the prevalence of ΣΔ A/D converter in today's receiver design [63, 11, 48, 65, 56, 35], this work demonstrates that perhaps what is needed is to move the feedback D/A converter of a ΣΔ modulator closer to the antenna. In this manner, a high-speed but low-resolution A/D converter is needed. This type of converter is compatible with the advancements of CMOS technology, where fast, low-gain amplifiers are easy to design.

Closing the ΣΔ feedback loop closer to the antenna allows for a more aggressive stage-scaling in the forward path. The forward path in a ΣΔ modulator only processes the error signal, which is much smaller than the full-scale input signal. Thus, for a given output swing limitation, a larger gain can be applied in the foremost amplifier. As a result the noise contribution of the succeeding stages becomes less significant. Therefore the power consumption of the overall circuit can be reduced. Alternatively, with the same gain, the output swing will be much reduced, resulting in a higher linearity.

The expense of such an approach is that more burden is placed in the design of the feedback D/A converter design. As the feedback D/A converter of the ΣΔ modulator is moved closer to the antenna, the dynamic-range requirement of the feedback D/A converter becomes more stringent. Noise and distortion generated by the feedback D/A converter is directly applied to the input of the modulator.

At this high sampling-rate, a continuous-time feedback D/A converter has to be used. The noise arising from such a scheme arise from random variations in the timing and current

reference. In some ways, a good timing reference is already needed in an RF receiver for the purpose of meeting the transmit spectral mask as well as to minimize the impact of reciprocal mixing. Furthermore, we have demonstrated a bias current sharing technique between an amplifier and the feedback D/A converter of a $\Sigma\Delta$ modulator. Using these two techniques, we argue that the associated cost, in power and silicon-area, of implementing a high dynamic-range D/A converter in an RF receiver can be amortized across other elements that are already present in an RF receiver.

We have shown in this work that a single-bit feedback D/A converter driven by an instrument-grade frequency-synthesizer [1] is not sufficiently low noise. It should be stated that this is not a fundamental limitation of this architecture, and it can be solved using different circuit techniques. For example, a multi-bit feedback D/A converter can be used to reduce the sensitivity of the architecture to timing jitter.

5.2 Specific Contributions

- Design of a multi-gigahertz down-converting $\Sigma\Delta$ A/D converter with up to 8MHz bandwidth.
- Design of a passive switched-capacitor filter operated at a gigahertz rate.
- A bias current sharing technique between an amplifier and a feedback D/A converter in implementing a $\Sigma\Delta$ summing node.
- Increased linearity of a down-conversion mixer aided by a $\Sigma\Delta$ feedback loop.
- Use of a gated-diode amplifier as a preamplifier for a comparator.
- An input-referred offset analysis of a gated-diode preamplifer due to V_t mismatch.

5.3 Future Work

- Increasing the operating frequency of the $\Sigma\Delta$ receiver in the current form by replacing the static SR latch in the receiver with a latch taken from a sense-amplifier-based flip-

flop [74]. The maximum operating frequency of the receiver is currently limited by the delay needed to complete a cycle of comparison and application of feedback D/A converter signal.

- A multi-bit implementation of the $\Sigma\Delta$ receiver. A multi-bit feedback D/A converter would lower the system's sensitivity to clock jitter. It has been shown that a $\Sigma\Delta$ A/D converter with a 4-bit continuous-time feedback D/A converter can achieve an 80-dB SNR across a 20MHz signal bandwidth with a competitive power consumption [61].

- Linearity of a receiver is ultimately limited by the voltage-to-current conversion operation within the mixer circuit. We have demonstrated a technique that relaxes the linearity limitation due to output compression. Some form of feedback linearization can be used in order to achieve a more linear voltage-to-current conversion. Or, if the mixer can be made sufficiently low noise, the LNA can be completely eliminated. This would reduce the maximum input signal power, therefore improving linearity.

Bibliography

[1] Agilent 4438c esg vector signal generator. Web.

[2] Agilent 4438c psg vector signal generator. Web.

[3] Interconnect breakout board. Web.

[4] Wireless Technology Comparison. web.

[5] Application note 3359: Clock jitter and phase noise conversion. Web, December 2004.

[6] Rf and a/ms technologies for wireless communication 2005, 2005.

[7] Blackberry Bold Teardown. web, November 2008.

[8] A. Abidi. The path to the software-defined radio receiver. *Solid-State Circuits, IEEE Journal of*, 42(5):954–966, May 2007.

[9] V. Aparin, N. Kim, G. Brown, Y. Wu, A. Cicalini, S. Kwok, and C. Persico. A Fully-Integrated Highly Linear Zero-IF CMOS Cellular CDMA Receiver. In *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pages 324–601 Vol. 1, Feb. 2005.

[10] R. Bagheri, A. Mirzaei, A. Chehrazi, M. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. Abidi. An 800-MHz-6-GHz Software-Defined Wireless Receiver in 90-nm CMOS. *IEEE Journal of Solid State Circuits*, 41(12):2860–2876, December 2006.

[11] B. Bakkaloglu, P. Fontaine, A. Mohieldin, S. Peng, S. J. Fang, and F. Dulger. A 1.5-V multi-mode quad-band RF receiver for GSM/EDGE/CDMA2K in 90-nm digital CMOS process. *Solid-State Circuits, IEEE Journal of*, 41(5):1149–1159, May 2006.

[12] A. Behzad, K. Carter, E. Chien, S. Wu, M. Pan, C. Lee, T. Li, J. Leete, S. Au, M. Kappes, Z. Zhou, D. Ojo, L. Zhang, A. Zolfaghari, J. Castanada, H. Darabi, B. Yeung, R. Rofougaran, M. Rofougaran, J. Trachewsky, T. Moorti, R. Gaikwad, A. Bagchi, J. Rael, and B. Marhoiev. A Fully Integrated MIMO Multi-Band Direct-Conversion CMOS Transceiver for WLAN Applications (802.11n). In *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, pages 560–622, Feb. 2007.

[13] B. Boser and B. Wooley. The Design of Sigma-Delta Modulation Analog-to-Digital Converters. *Solid-State Circuits, IEEE Journal of*, 23(6):1298–1308, Dec 1988.

[14] L. Breems, E. van der Zwan, and J. Huijsing. A 1.8-mW CMOS $\Sigma\Delta$ modulator with integrated mixer for A/D conversion of IF signals. *Solid-State Circuits, IEEE Journal of*, 35(4):468–475, Apr 2000.

[15] Broadcom Corp. *BRCM2075 Product Brief.*

[16] Broadcom Corp. *BRCM4329 Product Brief.*

[17] F. Chen and B. Leung. A 0.25-mW Low-Pass Passive Sigma-Delta Modulator with Built-in Mixer for a 10-MHz IF Input. *Solid-State Circuits, IEEE Journal of*, 32(6):774–782, Jun 1997.

[18] W.-H. Chen, G. Liu, B. Zdravko, and A. Niknejad. A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation. *Solid-State Circuits, IEEE Journal of*, 43(5):1164–1176, May 2008.

[19] Y. Chiu, B. Nikolic, and P. Gray. Scaling of Analog-toDigital Converters into Ultra-Deep-Submicron CMOS. In *IEEE Custom Integrated Circuits Conference*, pages 375–382, 2005.

[20] B. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. S. Pister. Low-Power 2.4-GHz Transceiver with Passive RX Front-End and 400-mV Supply. *IEEE Journal of Solid State Circuits*, 41(12):2757–2766, December 2006.

[21] H. Darabi, A. Zolfaghari, H. Jensen, J. Leete, B. Mohammadi, J. Chiu, T. Li, Z. Zhou, P. Lettieri, Y. Chang, A. Hadji, P. Chang, M. Nariman, I. Bhatti, A. Medi, L. Serrano, J. Welz, K. Shoarinejad, S. Hasan, J. Castaneda, J. Kim, H. Tran, P. Kilcoyne, R. Chen, B. Lee, B. Zhao, B. Ibrahim, M. Rofougaran, and A. Rofougaran. A Fully Integrated Quad-Band GPRS/EDGE Radio in 0.13μm CMOS. In *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pages 206–607, Feb. 2008.

[22] G. Dawe. Application of SDR Softranscievers to 4G Markets. GIRAFE: 4G RF Forums in International Solid-State Circuits Conference, 2009.

[23] O. Degani, M. Ruberto, E. Cohen, Y. Eilat, B. Jann, F. Cossoy, N. Telzhensky, T. Maimon, G. Normatov, R. Banin, O. Ashkenazi, A. Ben Bassat, S. Zaguri, G. Hara, M. Zajac, E. Shaviv, S. Wail, A. Fridman, R. Lin, and S. Gross. A 1x2 MIMO Multi-Band CMOS Transceiver with an Integrated Front-End in 90nm CMOS for 802.11a/g/n WLAN Applications. In *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pages 356–619, Feb. 2008.

[24] V. Delia Torre, M. Conta, R. Chokkalingam, G. Cusmai, P. Rossi, and R. Svelto. A 20mW 3.24mm^2 Fully Integrated GPS Radio for Cell-Phones. In *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, pages 1902–1911, Feb. 2006.

[25] A. Demir and A. Sangiovanni-Vincentelli. *Analysis and Simulation of Noise in Nonlinear Electronic Circuits and Systems*. Kluwer Academic Publishers, 1998.

[26] EPCOS. *EPCOS B9419 - SAW Rx Filter*.

[27] O. Erdogan, R. Gupta, D. Yee, J. Rudell, J.-S. Ko, R. Brockenbrough, S.-O. Lee, E. Lei, J. L. Tham, H. Wu, C. Conroy, and B. Kim. A Single-Chip Quad-Band GSM/GPRS Transceiver in 0.18 μm Standard CMOS. In *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pages 318–601 Vol. 1, Feb. 2005.

[28] J. Fischer. Noise sources and calculation techniques for switched capacitor filters. *IEEE Journal of Solid State Circuits*, SC-17(4):742–752, August 1982.

[29] V. Giannini, P. Nuzzo, C. Soens, K. Vengattaramane, M. Steyaert, J. Ryckaert, M. Goffioul, B. Debaillie, J. Van Driessche, J. Cranickx, and M. Ingles. A 2mm^2 0.1-to-5GHz SDR Receiver in 45nm Digital CMOS. In *International Solid-State Circuits Conference*, pages 408–409, 2009.

[30] P. Gray, P. Hurst, S. Lewis, and R. Meyer. *Analysis and Design of Analog Integrated Circuits*. Wiley, 2001.

[31] R. Gray. Quantization Noise Spectra. *Information Theory, IEEE Transactions on*, 36(6):1220–1244, Nov 1990.

[32] A. Hadjichristos, A. Cassia, H. Kim, and C. Park. Single-Chip RF CMOS UMTS/EGSM Transceiver with Integrated Receive Diversity and GPS. In *International Solid-State Circuits Conference*, pages 118–119, 2009.

[33] M. Hajimorad. Analysis of Jitter Propagation in Differential Clock Drivers. Master's thesis, University of California, Berkeley, 2005.

[34] D. Ham and A. Hajimiri. Virtual Damping and Einstein Relation in Oscillators. *Solid-State Circuits, IEEE Journal of*, 38(3):407–418, Mar 2003.

[35] J. Jarvinen and K. Halonen. A 1.2V Dual-Mode GSM/WCDMA $\Sigma\Delta$ Modulator in 65nm CMOS. In *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, pages 1972–1981, Feb. 2006.

[36] M. Jeeradit, J. Kim, B. Leibowitz, P. Nikaeen, V. Wang, B. Garlepp, and C. Werner. Characterizing Sampling Aperture of Clocked Comparators. In *VLSI Circuits, 2008 IEEE Symposium on*, pages 68–69, June 2008.

[37] D. Kaczman, M. Shah, M. Alam, M. Rachedine, D. Cashen, L. Han, and A. Raghavan. A SingleChip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver with DigRF 3G Interface and +90 dBm IIP2. *Solid-State Circuits, IEEE Journal of*, 44(3):718–739, March 2009.

[38] D. Kaczman, M. Shah, N. Godambe, M. Alam, H. Guimaraes, L. Han, M. Rachedine, D. Cashen, W. Getka, C. Dozier, W. Shepherd, and K. Couglar. A Single-Chip Tri-Band (2100, 1900, 850/800 MHz) WCDMA/HSDPA Cellular Transceiver. *Solid-State Circuits, IEEE Journal of*, 41(5):1122–1132, May 2006.

[39] S. Karvonen, T. Riley, and J. Kostamovaara. A Low Noise Quadrature Subsampling Mixer. In *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, volume 4, pages 790–793 vol. 4, May 2001.

[40] S. Karvonen, T. Riley, and J. Kostamovaara. A cmos quadrature charge-domain sampling circuit with 66-db sfdr up to 100 mhz. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 52(2):292–304, Feb. 2005.

[41] S. Karvonen, T. Riley, and J. Kostamovaara. Charge-domain fir sampler with programmable filtering coefficients. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 53(3):192–196, March 2006.

[42] H. Khorramabadi. EE247 : Analog-Digital Interfaces in VLSI Technology Lecture Notes, 2004.

[43] T. W. Kim, B. Kim, and K. Lee. Highly Linear Receiver Front-End Adopting MOSFET Transconductance Linearization by Multiple Gated Transistors. *Solid-State Circuits, IEEE Journal of*, 39(1):223–229, Jan. 2004.

[44] F. Krummenacher and N. Joehl. A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning. *Solid-State Circuits, IEEE Journal of*, 23(3):750–758, Jun 1988.

[45] K. Kundert. Simulating switched-capacitor filters with SpectreRF. The Designer's Guide Community, 2005.

[46] C. Kurth and G. Moschytz. Nodal analysis of switched-capacitor networks. *IEEE Transactions on Circuits and Systems*, CAS-26(2):93–105, February 1979.

[47] H. Lakdawala, J. Zhan, A. Ravi, S. Anderson, B. Carlton, R. Nicholls, N. Yaghini, R. Bishop, S. Taylor, and K. Soumyanath. Multi-Band (1-6GHz), Sampled, Sliding-IF Receiver with Discrete-Time Filtering in 90nm Digital CMOS Process. In *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, pages 230–231, 0-0 2006.

[48] Y. Le Guillou, O. Gaborieau, P. Gamand, M. Isberg, P. Jakobsson, L. Jonsson, D. Le Deaut, H. Marie, S. Mattisson, L. Monge, T. Olsson, S. Prouet, and T. Tired. Highly Integrated Direct Conversion Receiver for GSM/GPRS/EDGE with On-Chip 84-dB Dynamic Range Continuous-Time $\Sigma\Delta$ ADC. *Solid-State Circuits, IEEE Journal of*, 40(2):403–411, Feb. 2005.

[49] T. H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits.* Cambridge University Press, 2 edition, 2003.

[50] B. Leibowitz, J. Kim, J. Ren, and C. Madden. Characterization of Random Decision Errors in Clocked Comparators. In *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, pages 691–694, Sept. 2008.

[51] Z. Li, W. Ni, J. Ma, M. Li, D. Ma, D. Zhao, J. Mehta, D. Hartman, X. Wang, K. O, and K. Che. A Dual-Band CMOS Transceiver for 3G TD-SCDMA. In *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, pages 344–607, Feb. 2007.

[52] L. Lin, N. Wongkomet, Y. D., C. Lin, M. He, B. Nissim, S. Lyuee, P. Yu, T. Sepke, S. Shekarchian, L. Tee, P. Muller, J. Tam, and T. Cho. A Fully Integrated 2x2 MIMO Dual-Band Dual-Mode Direct-Conversion CMOS Transceiver for WiMAX/WLAN Applications. In *International Solid-State Circuits*, 2009.

[53] S. Lindfors, A. Parssinen, and K. Halonen. A 3-V 230-MHz CMOS decimation sub-sampler. *IEEE Transactions on Circuits and Systems - II*, 50(3):105–117, March 2003.

[54] W. Luk and R. Dennard. Gated-Diode Amplifiers. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 52(5):266–270, May 2005.

[55] D. Manstretta, M. Brandolini, and F. Svelto. Second-Order Intermodulation Mechanisms in CMOS Downconverters. *Solid-State Circuits, IEEE Journal of*, 38(3):394–406, Mar 2003.

[56] B. Marholev, M. Pan, E. Chien, L. Zhang, R. Roufoogaran, S. Wu, I. Bhatti, T.-H. Lin, M. Kappes, S. Khorram, S. Anand, A. Zolfaghari, J. Castaneda, C. Chien, B. Ibrahim, H. Jensen, H. Kim, P. Lettieri, S. Mak, J. Lin, Y. Wong, R. Lee, M. Syed, M. Rofougaran, and A. Rofougaran. A Single-Chip Bluetooth EDR Device in 0.13μm CMOS. In *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, pages 558–759, Feb. 2007.

[57] M. McHenry, D. McCloskey, D. Roberson, and J. MacDonald. Spectrum Occupancy Measurements. Chicago, Illinois, November 16-18, 2005. web.

[58] I. Mehr and D. Welland. A CMOS Continuous-Time Gm-C Filter for PRML Read Channel Applications at 150 Mb/s and Beyond. *Solid-State Circuits, IEEE Journal of*, 32(4):499–513, Apr 1997.

[59] S. Mehta, D. Weber, M. Terrovitis, K. Onodera, M. Mack, B. Kaczynski, H. Samavati, S. Jen, W. Si, M. Lee, K. Singh, S. Mendis, P. Husted, N. Zhang, B. McFarland, D. Su, T. Meng, and B. Wooley. An 802.11g WLAN SoC. In *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pages 94–586 Vol. 1, Feb. 2005.

[60] J. Mitola. The Software Radio Architecture. *Communications Magazine, IEEE*, 33(5):26–38, May 1995.

[61] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani. A 20-mW 640-MHz CMOS Continuous-Time *sigmadelta* ADC with 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB. *Solid-State Circuits, IEEE Journal of*, 41(12):2641–2649, Dec. 2006.

[62] K. Muhammad, Y.-C. Ho, J. Mayhugh, T.L., C.-M. Hung, T. Jung, I. Elahi, C. Lin, I. Deng, C. Fernando, J. Wallberg, S. Vemulapalli, S. Larson, T. Murphy, D. Leipold, P. Cruise, J. Jaehnig, M.-C. Lee, Staszewski, R.B., R. Staszewski, and K. Maggio. The first fully integrated quad-band GSM/GPRS receiver in a 90-nm digital CMOS process. *IEEE Journal of Solid State Circuits*, 41:1772–1783, August 2006.

[63] K. Muhammad, Y.-C. Ho, T. Mayhugh, C.-M. Hung, T. Jung, I. Elahi, C. Lin, I. Deng, C. Fernando, J. Wallberg, S. Vemulapalli, S. Larson, T. Murphy, D. Leipold, P. Cruise, J. Jaehnig, M.-C. Lee, R. Staszewski, R. Staszewski, and K. Maggio. The First Fully Integrated Quad-Band GSM/GPRS Receiver in a 90-nm Digital CMOS Process. *Solid-State Circuits, IEEE Journal of*, 41(8):1772–1783, Aug. 2006.

[64] K. Muhammad, D. Leipold, B. Staszewski, Y.-C. Ho, C. Hung, K. Maggio, C. Fernando, T. Jung, J. Wallberg, J.-S. Koh, S. John, I. Deng, O. Moreira, R. Staszewski, R. Katz, and O. Friedman. A Discrete-Time Bluetooth Receiver in a 0.13μm Digital CMOS Process. In *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pages 268–527 Vol.1, Feb. 2004.

[65] K. Muhammad, D. Leipold, and R. Staszewski. A Discrete-Time Bluetooth Receiver in a 0.13μm Digital CMOS Process. In *2004 IEEE International Solid-State Circuits Digest of Technical Papers*, volume 47, 2004.

[66] K. Muhammad and R. Staszewski. Direct RF Sampling Mixer with Recursive Filtering in Charge Domain. In *Proc. International Symposium on Circuits and Systems*, pages 577–580, 2004.

[67] K. Muhammad, R. Staszewski, and D. Leipold. Digital RF processing: Toward low-cost reconfigurable radios. *IEEE Communications Magazine*, pages 105–113, August 2005.

[68] B. Murmann. Adc performance survey 1997-2008. [Online]. Available: http://www.stanford.edu/ murmann/adcsurvey.html.

[69] I. Nam, B. Kim, and K. Lee. CMOS RF Amplifier and Mixer Circuits Utilizing

Complementary Characteristics of Parallel Combined NMOS and PMOS Devices. *Microwave Theory and Techniques, IEEE Transactions on*, 53(5):1662–1671, May 2005.

[70] A. Namdar and B. Leung. A 400-MHz, 12-bit, 18-mW, IF Digitizer with Mixer Inside a Sigma-Delta Modulator Loop. *Solid-State Circuits, IEEE Journal of*, 34(12):1765–1776, Dec 1999.

[71] L. Nathawad, D. Weber, S. Abdollahi, P. Chen, S. Enam, B. Kaczynski, A. Kheirkhahi, M. Lee, S. Limotyrakis, K. Onodera, K. Vleugels, M. Zargari, and B. Wooley. An IEEE 802.11a/b/g SoC for Embedded WLAN Applications. In *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, pages 1430–1439, Feb. 2006.

[72] C. Nguyen. *Micromechanical Signal Processor*. PhD thesis, University of California, Berkeley, 1994.

[73] A. Niknejad. EE142 : Integrated-Circuits for Communications Lecture Notes, 2004.

[74] B. Nikolic, V. Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu, and M. Ming-Tak Leung. Improved sense-amplifier-based flip-flop: design and measurements. *Solid-State Circuits, IEEE Journal of*, 35(6):876–884, Jun 2000.

[75] S. R. Norsworthy, R. Schreier, and G. C. Temes. *Delta-Sigma data converters: Theory, design, and simulation*. IEEE Press, 1997.

[76] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas. Noise Analysis of Regenerative Comparators for Reconfigurable ADC Architectures. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 55(6):1441–1454, July 2008.

[77] A. Ong and B. Wooley. A two-path bandpass $\Sigma\Delta$ modulators for digital IF extraction at 20 MHz. *IEEE Journal of Solid State Circuits*, 32(12):1920–1934, December 1997.

[78] A. Oppenheim, R. Schafer, and J. Buck. *Discrete-Time Signal Processing*. Prentice Hall, 2 edition, January 1999. 1999.

[79] I. Opris. Noise Estimation in Strobed Comparators. *Electronics Letters*, 33(15):1273–1274, Jul 1997.

[80] E. Org, R. Cyr, G. Dawe, and J. Kilpatrick. Software Defined Radio Architectures for Mobile Commercial Applications. [online].

[81] M. Ortmanns and F. Gerfers. *Continuous-time sigma-delta A/D conversion: Fundamentals, performance limits and robust implementations*. Springer, 2006.

[82] Y. Palaskas, A. Ravi, S. Pellerano, B. Carlton, M. Elmala, R. Bishop, G. Banerjee, R. Nicholls, S. Ling, S. Taylor, and K. Soumyanath. A 5GHz 108Mb/s 2x2 MIMO Transceiver with Fully Integrated +16dBm PAs in 90nm CMOS. In *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, pages 1420–1429, Feb. 2006.

[83] H. Pekau and J. Haslett. A 2.4 GHz cmos Sub-Sampling Mixer with Integrated Filtering. *Solid-State Circuits, IEEE Journal of*, 40(11):2159–2166, Nov. 2005.

[84] K. Philips, P. Nuijten, R. Roovers, A. van Roermund, F. Chavero, M. Pallares, and A. Torralba. A Continuous-Time $\sigma\delta$ ADC with Increased Immunity to Interferers. *Solid-State Circuits, IEEE Journal of*, 39(12):2170–2178, Dec. 2004.

[85] N. Poobuapheun, W.-H. Chen, Z. Boos, and A. Niknejad. A 1.5-V 0.72.5-GHz CMOS Quadrature Demodulator for Multiband Direct-Conversion Receivers. *Solid-State Circuits, IEEE Journal of*, 42(8):1669–1677, Aug. 2007.

[86] J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits*. Prentice-Hall, 2003.

[87] S. Ranganathan and Y. Tsividis. A MOS Capacitor-Based Discrete-Time Parametric Amplifier with 1.2 V Output Swing and 3μW Power Dissipation. In *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*, pages 406–502 vol.1, 2003.

[88] B. Razavi and B. Wooley. Design Techniques for High-Speed, High-Resolution Comparators. *Solid-State Circuits, IEEE Journal of*, 27(12):1916–1926, Dec 1992.

[89] B. Rezavi. A 1.5 V 900 MHz Downconversion Mixer. In *Solid-State Circuits Conference, 1996. Digest of Technical Papers. 42nd ISSCC., 1996 IEEE International*, pages 48–49, Feb 1996.

[90] U. Rohde, A. Poddar, and G. Bock. *The Design of Modern Oscillators for Wireless Applications: Theory and Optimization.* Wiley Interscience, 2005.

[91] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello. A 15 mW, 70 kHz 1/f Corner Direct Conversion CMOS Receiver. In *Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003*, pages 459–462, Sept. 2003.

[92] D. Sahu, A. Das, Y. Darwhekar, S. Ganesan, G. Rajendran, R. Kumar, B. Chandrashekar, A. Ghosh, A. Gaurav, T. Krishnaswamy, A. Goyal, S. Bhagavatheeswaran, K. M. Low, N. Yanduru, S. Dhamankar, and S. Venkatraman. A 90nm CMOS Single-Chip GPS Receiver with 5dBm out-of-band IIP3 2.0dB NF. In *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pages 308–600 Vol. 1, Feb. 2005.

[93] S. Sakurai and M. Ismail. *Low-Voltage CMOS Operational Amplifiers.* Kluwer Academic Publishers, 1995.

[94] D. Schinkel, E. Mensink, E. Kiumperink, E. van Tuijl, and B. Nauta. A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time. In *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, pages 314–605, Feb. 2007.

[95] R. Schreier. ADCs and DACs: Marching Towards the Antenna. GIRAFE Forum in International Solid State Circuits Conference, February 2003.

[96] W. Serdjin. *Low-Voltage Low-Power Analog Integrated Circuits.* Kluwer Academic Publishers, 1995.

[97] A. Shahani, D. Shaeffer, and T. Lee. A 12-mW Wide Dynamic Range CMOS Front-End for a Portable GPS Receiver. *Solid-State Circuits, IEEE Journal of*, 32(12):2061–2070, Dec 1997.

[98] O. Shana'a. EE290C: Advanced Circuit Design for Wireless Communications, 2005.

[99] N. Sooch. High swing cmos cascode cirrent mirrot. US Patent No. 4583037, April 1986.

[100] T. Sowlati, J. Agarwal, J. Cho, T. Obkircher, and M. El Said. Single-Chip Multi-band WCDMA/HSDPA/HSUPA/EGPRS Tranceiver with Diversity Receiver and 3G DigRF Interface without SAW Filters in Transmitter/3G Receiver Paths. In *International Solid State Circuits Conference*, pages 116–117, 2009.

[101] C. D. Systems. Virtuoso spectrerf simulation option user guide, November 2005.

[102] S. Tadjpour, E. Cijvat, E. Hegazi, and A. Abidi. A 900-MHz Dual-Conversion Low-IF GSM Receiver in 0.35μm CMOS. *Solid-State Circuits, IEEE Journal of*, 36(12):1992–2002, Dec 2001.

[103] H. Tao and J. Khoury. A 400-Ms/s Frequency Translating Bandpass Sigma-Delta Modulator. *Solid-State Circuits, IEEE Journal of*, 34(12):1741–1752, Dec 1999.

[104] B. Tenbroek, J. Strange, D. Nalbantis, C. Jones, P. Fowers, S. Brett, C. Beghein, and F. Beffa. Single-Chip Tri-Band WCDMA/HSDPA Transceiver without External SAW Filters and with Integrated TX Power Control. In *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pages 202–607, Feb. 2008.

[105] D. Tse and P. Viswanath. *Fundamentals of Wireless Communication*. Cambridge University Press, 2005.

[106] Y. Tsividis. *Operation and Modelling of the MOS Transistor*. McGraw-Hill, 2003.

[107] Y. Tsividis, Z. Czarnul, and S. Fang. MOS Transconductors and Integrators with High Linearity. *Electronics Letters*, 22(5):245–246, 27 1986.

[108] R. van de Plassche. *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*. Springer, 2007.

[109] A. van den Bosch, M. Steyaert, and W. Sansen. SFDR-Bandwidth Limitations for High Speed High Resolution Current Steering CMOS D/A Converters. In *Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on*, volume 3, pages 1193–1196 vol.3, 1999.

[110] A. van der Ziel. *Noise in Solid State Devices and Circuits*. Wiley, 1986.

[111] D. von Grunigen, R. Sigg, J. Schmid, G. Moschytz, and H. Melchior. An integrated CMOS switched-capacitor bandpass filter based on N-path and frequency-sampling principles. *IEEE Journal of Solid State Circuits*, SC-18(6):753–761, December 1983.

[112] G. Wegmann, E. Vittoz, and F. Rahali. Charge injection in analog mos switches. *IEEE Journal of Solid State Circuits*, SC-22(6):1091–1097, December 1987.

[113] J. Weldon, J. Rudell, L. Lin, R. Sekhar Narayanaswami, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and P. Gray. A 1.75 ghz highly-integrated narrow-band cmos transmitter with harmonic-rejection mixers. In *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*, pages 160–161, 442, 2001.

[114] R. Winoto. A Radio-Frequency Bandpass $\Sigma\Delta$ A/D Converter. Master's thesis, UC Berkeley, May 2006.

[115] A. Yoshizawa and S. Lida. A Gain-Boosted Discrete-Time Charge-Domain FIR LPF with Double-Complementary MOS Parametric Amplifiers. In *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pages 68–596, Feb. 2008.

[116] J. Yuan. A charge sampling mixer with embedded filter function for wireless applications. In *Proc. 2nd, Int. Conf. Microwave and Millimeter Wave Technology*, pages 315–318, Beijing, China, 2000.

[117] S. Zhou and M.-C. Chang. A CMOS Passive Mixer with Low Flicker Noise for Low-Power Direct-Conversion Receiver. *Solid-State Circuits, IEEE Journal of*, 40(5):1084–1093, May 2005.

[118] J. Zipper, R. Vazny, L. Maurer, M. Wilhelm, T. Greifeneder, and A. Holm. A single-Chip Dual-Band CDMA2000 Transceiver in 0.13μm CMOS. In *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, pages 342–607, Feb. 2007.