Scaling of Inkjet-Printed Transistors using Novel Printing Techniques

Huai-Yuan Tseng

Electrical Engineering and Computer Sciences
University of California at Berkeley

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by

Huai-Yuan Tseng

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Professor Tsu-Jae King Liu

Professor Costas P. Grigoropoulos

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Abstract

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There has been a great interest in the realization of low-cost electronic applications such as item-level RFID tags and smart labels. Printed electronics has become the most promising technology due to its lithography- and vacuum-free processing. In this regard, solution-processed materials have been advanced rapidly to enhance the performance of printed devices. However, the poor resolution of state-of-the-art printing techniques such as inkjet and gravure printing has necessitated the use of large channel lengths in transistors and large gate to source/drain overlap to compensate for the poor layer-to-layer registration capability. These large dimensions have limited the speed improvement in printed transistors, despite the improvements in materials. Therefore, this thesis focuses on circumventing the printing resolution challenges using novel printing techniques. Scaling of the critical dimensions as well as improvement of the switching speed was achieved with a purely printing process.

To reduce the parasitic capacitance of printed transistors, a wetting-based roll-off technique has been applied to achieve self-alignment of transistor source/drain electrodes to the gate, resulting in a minimum overlap. Minimum overlap of 0.47 µm was achieved, contrasted to the >10 µm typically required in conventional printed transistors. The technique has also been applied to realize a fully printed inverter circuit. For further scaling of the transistor dimension, shrinking of the printed gate electrodes is required. Therefore a novel printing technique combining inkjet printing and mechanical pen dragging was proposed. Printed gate lines as narrow as 2.75 µm were demonstrated. Printed transistors combining the highly-scaled gate lines and self-alignment were demonstrated. Transistors with channel lengths as small as 200 nm to 2.75 µm showed the highest cut-off frequency reported to date of 1.6 MHz. The performance is expected to be improved further by using the most advanced materials. This high speed operation will enable the realization of fully printed RFID and other printed applications in the foreseeable future.

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Chapter 1 Introduction

Modern electronics has revolutionized day-to-day life. As information has become increasingly ubiquitous, portable consumer electronic systems such as laptops, tablets, and smartphones have provided convenience to users. For example, headline news, local maps and driving directions, restaurant ratings, and a wealth of other resources are available within seconds using a smartphone. This unprecedented convenience was made possible by advances in silicon technology, in which miniaturized integrated circuits (ICs), consisting of billions of transistors, enabled the integration of wireless communication, global positioning systems (GPS), and a digital camera into a pocket-size, mobile device.

In parallel with the advancement of portable devices, yet another revolution is currently taking place. Namely, traditional materials printed on paper are being replaced by electronics. The best examples are the Universal Product Code (UPC) barcode on consumer goods replaced by Radio Frequency Identification (RFID) tags, and traditional books replaced by an E-book. The deployment of item-level RFID tags will significantly improve inventory control for retailers, as well as expedite the checkout process for customers, e.g. a simple walk through an electronic counter instead of waiting in a long line for all items in the cart to be scanned individually [1]. Shopping thus becomes a more pleasant experience. A lightweight E-book with a large, thin, and flexible display can replace an entire collection of heavy and bulky books to deliver an interactive, fast access and comfortable reading experience.

In the revolution of portable electronic devices, novelty and versatility are the primary attractions as opposed to replacing a traditional solution. Despite smartphones having monthly data plans costing considerably more than traditional voice-only cell phone plans, the former still have a strong and growing market. Consumers have clearly demonstrated a willingness to pay for the added functionality associated with smartphones, maintaining the demand in this particular market. On the other hand, cost will be the major challenge for item-level RFID tags and E-books to replace their long-time paper-based counterparts. In order to break into the current market, an item-level RFID tag needs to cost less than one cent to become cheaper than a paper barcode. In order to massively replace traditional books, a small-size E-book needs to deliver a cost similar to a paperback novel, or a large size E-book needs to cost less than a typical textbook. While this goal is extremely challenging, the enormous market value has shown the demand.

Traditionally, the cost of electronic devices is reduced by increasing the IC density on a single silicon wafer. However, the cost of silicon per area remains high. Therefore, conventional processes are not cost effective for the fabrication of item-level RFID tags because the size of the tags—determined by antenna area—is relatively large. Although there has been a hybrid process combining a printed antenna and bonding of a low-cost silicon chip, the overall cost remains prohibitive due to a non-scalable bonding cost. In the case of the E-book, the display—typically 6 to 10 inches—remains the major cost bottleneck. The active matrix thin film transistor (TFT) array used for the display backplane is fabricated with conventional lithographical and vacuum processing, introducing unavoidable high-cost semiconductor processing. Furthermore, conventional processing temperatures are too high for plastic substrates, required for realizing flexible displays.

Clearly, a new technology for low-cost and large area applications is required to fill the bottom cost gap associated with conventional silicon and TFT processing techniques. Printed

electronics has the potential to fulfill this requirement, and is thus becoming the most promising candidate to achieve the next electronic revolution.

1.1. Printed electronics

Printing techniques have been industrialized and become an essential part of publishing and transaction printing for a century. In recent years, printing techniques have been utilized to directly deposit electronic materials on a substrate in order to build electronic devices such as passive resistors, capacitors, inductors, and active transistors [2], [3].

Conventionally, the fabrication of ICs used extensively in electronic devices involves a series of thin film deposition steps using vacuum processing, along with a series of lithography processes that include spin-coating photoresist, exposure, development, etching and photoresist-stripping in order to define the thin film into a desired pattern. This subtractive patterning method not only requires several layers of costly masks, but also wastes the etched materials, increasing the total processing cost. On the contrary, printed electronics utilizes printing techniques such as inkjet, gravure, and offset printing to additively deposit materials into a pre-designed pattern. The advantage of combining thin film deposition and patterning into a single step eliminates the major cost points seen in conventional vacuum and lithographic processing.

Furthermore, printed electronics may begin to exploit high-throughput roll-to-roll processing similar to that found in the publishing industry. Roll-printing processes have been demonstrated to print circuits as fast as five meters per minute, a speed quite capable of competing with parallel vacuum deposition processes [3]. Roll-to-roll printing in electronics is made possible through flexible substrates such as plastic or paper, which cost much less than silicon wafers and glass. However, low temperature processing becomes necessary as typical plastic substrates undergo a glass transition around 150-200℃, and the subsequent deformation may destroy the printed devices [4]. Fortunately, the development of the low-temperature compatible inks has been successful in recent years. These inks have enabled low-temperature annealing or sintering of the semiconductor and metal nanoparticles, respectively [5], [6].

In sum, with advantages such as high-throughput, low-temperature, and inline packaging, printed electronics has become the most suitable technology for realizing the low-cost and large area applications such as printed RFID tags and flexible displays.

1.2. Applications

1.2.1. Printed RFID

The item-level RFID system is designed to replace the UPC barcode on individual consumer goods to improve automation and inventory control. With item-level RFID tags, no individual scans on items are required during the checkout process. Simply walk past a tag reader with all of your items and a bill will become available for the customer in mere seconds. Furthermore, item-level RFID tags can potentially be integrated with a spoilage sensor and low-cost display to provide real-time product information such as expiration date and price. The improved automation can also minimize human handling, further reducing overall cost.

Most economic analysis suggests that the cost of each tag needs to be less than one cent to become economically viable, since the individual tagged product typically has a price floor in the

range of few cents to few tens of cents [7]. Therefore, by deploying an RFID tag with a cost less than one cent allows a reasonable margin.

The carrier frequency of the RFID system is regulated by Federal Communications Commission (FCC) and is allowed in the following four communication bands: 2.4 GHz, 900 MHz, 13.56 MHz and 135 kHz. For long distance RFID applications such as pallet-level RFID or electronic toll collection system, higher frequency is favorable since the power can be delivered to the tag at a longer distance with a higher antenna quality factor. High frequency also allows smaller passive component area and is therefore dominated by conventional silicon technology. On the other hand, item-level RFID requires a shorter working distance (in the range of one meter) to avoid an accidental readout from other checkout counters, for example. For short distance applications, near-field inductive coupling is used for power coupling, unlike the use of electromagnetic-wave propagation in far-field coupling. In such cases, lower frequency is favorable as more power can be supplied to the tags which reply using near-field coupling [8]. As a result, 135 kHz and 13.56 MHz can both be attractive for item-level RFID applications. However, using 135 kHz generally requires a large inductor, decreasing the areal efficiency of the circuit. On the other hand, an RFID tag with 13.56 MHz carrier frequency will have a small size (around two centimeters per side), and will work well in water- and metal-contaminated environments. Therefore, 13.56 MHz is the ideal frequency for item-level RFID applications.

The RFID system comprises of two main components to provide wireless communication: a tag/transponder and a reader/interrogator, as illustrated in Figure 1.1. A third essential component not shown in the figure is the host computer that manages the data output from the reader. The reader initializes the communication by providing a clock signal and power to the tag. Next, the data inside the tag is sent back to the reader through a modulation scheme. The product information is thus captured in a manner similar to the scanning of a barcode.

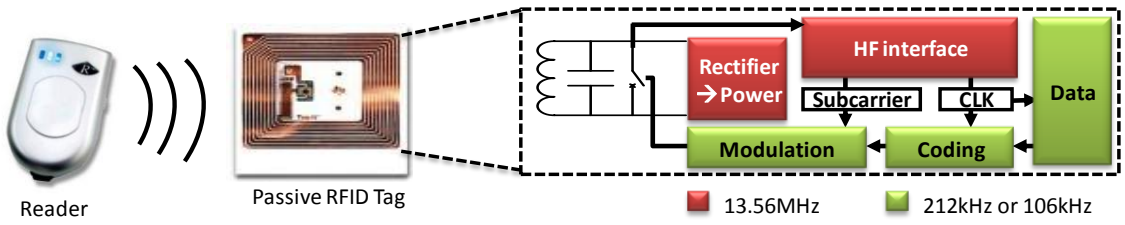

Figure 1.1 A basic RFID system comprises a reader and a passive tag.

The tags are passive for item-level RFID system, i.e. no active energy source or battery is used to power the circuit in the tag. Instead, the power is drawn from the reader through an inductive coupling. To maximize the efficiency, the inductor and capacitor on the tag are designed to resonate at 13.56 MHz. A rectifier circuit is then used to convert the resonant RF signal into a DC power source to supply the circuit. The circuitry inside the tag (shift registers, memory arrays, coding and modulation circuits) requires a clock to operate.

In the case of synchronous RFID tags, a high frequency (HF) interface divides down the 13.56 MHz signal to provide the clock for internal circuit as well as the sub-carrier for the modulation circuit. The clock frequency in the internal circuit is typically 106 kHz or 212 kHz. Unfortunately, the transistors produced by printing techniques typically show a switching speed about two or three orders of magnitude slower than the aforementioned clock frequency. Although the clock could be furthered divided down to accommodate the printed circuit at a lower frequency, the tag will suffer from lower data rate, i.e. longer tag readout time. However,

as previously described, the HF divider circuit will unavoidably have to operate at 13.56 MHz to successfully divide down the RF signal. Clearly, printed transistors will need to operate at 13.56 MHz in order to realize fully-printed synchronous RFID tags.

Asynchronous RFID is the other approach to accommodate the slow transistor speed. Instead of dividing down the 13.56 MHz frequency, a local clock is generated by an internal circuit. Thus, the speed constraint can be lowered to few hundreds of kHz, which is feasible for printed transistors. However, the local clock frequency is prone to deviate from tag to tag, due to the printing-process variations. This complicates the data readout and thus requires a new reader design and/or new RFID protocol to properly communicate with the asynchronous tag.

It is currently unclear whether synchronous or asynchronous tags will be deployed for item-level printed RFID system. Nonetheless, in either case, the performance of the printed transistors will require a breakthrough in order to meet these demands. Therefore, scaling of the printed transistor was pursued in this thesis work to achieve high speed operation. More details regarding the speed enhancement via scaling will be discussed in section 4.

1.2.2. Display

Display technology has advanced rapidly and become an essential component of portable electronic devices, as many devices reply upon displays to convey information and interact with users. Major display technologies used for modern portable electronic devices are liquid crystal display (LCD), organic light emitting diode (OLED), and electrophoretic display (EPD). These technologies all have an active matrix (AM) TFT array in common, which acts as a backplane to precisely control the display media. Figure 1.2(a) shows the basic architecture of an AM-TFT LCD, comprising of a backlight source, a first polarizer, a TFT array with liquid crystal, a color filter and a second polarizer. The operation principle is as follows. To begin, the first polarizer polarizes the backlight into a single orientation. Next, the liquid crystal is used to rotate the polarization of the light by 90 degrees. The TFTs control the liquid crystal alignment by changing the electric field across the liquid crystal to determine whether the polarization of the light is rotated. If the light retains the same polarization as transmitted out of the first polarizer, the light will be blocked by the second polarizer, which is orthogonal to the first one. This represents a dark pixel, with no light passing through. A color filter is then used in each pixel to select the wavelength of light to present individual red, green and blue sub-pixels. The sub-pixels are then used to construct a final color to display. Figure 1.2(b) shows the pixel schematic, consisting of one TFT, a storage capacitor (C_{ST}), and another parasitic capacitor from the liquid crystal (C_{LC}). The gate of the TFT is connected to the horizontal scan line that turns on the TFT row by row. When the pixel is selected, the data line connected to the drain of the TFT supplies the voltage to charge or discharge the storage capacitor. The voltage stored in the capacitor is used to provide the electric field with respect to the common electrode at the other side of the liquid crystal. As a result, the stored voltage in the capacitor determines the brightness or gray-scale of the pixel. For AM-TFTLCD, the fact that light has to pass through several layers before displaying to the human eye limits the overall brightness. The reason is that a portion of incoming light is blocked by opaque metal layers used for bus lines, TFT, and capacitors. Therefore, higher aperture ratio, a ratio of the transparent area to the total area of a pixel, is required to maximize the brightness as well as contrast of the AM-TFTLCD.

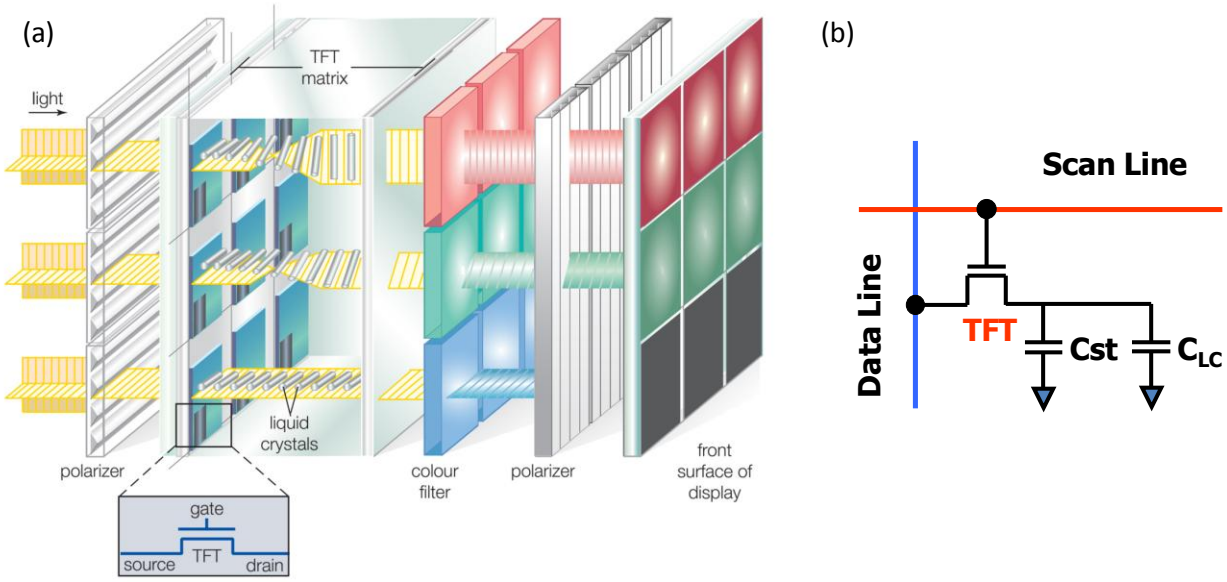

Figure 1.2 (a) Basic architecture of an AM-TFTLCD (Image courtesy of 2010 Encyclopedia Britannica, Inc.) (b) Schematic diagram of an AM-LCD pixel.

Unlike LCD technology which requires a backlight source, AMOLED is a self-emitting technology showing an advantage of higher contrast, wider viewing angle and faster response time. Figure 1.3(a) shows the basic architecture of the AMOLED display, comprising an AM-TFT array and an OLED component. The OLED typically consists of an electron transport layer, an organic emitter, and a hole injection layer. The emitting layer of the OLED is controlled by the supplying current using a TFT pixel as shown in Figure 1.3(b). TFT1 and the storage capacitor function similar to those in AM-TFTLCD to control the voltage storage in the pixel. The stored voltage is then applied to the gate of TFT2 as a gate controlled current source in order to determine the OLED emitting current, as the brightness of the OLED is directly proportional to the current. Typical AMOLED displays are bottom-emitting type, i.e. the light emits toward the bottom through a transparent anode and TFT backplane as illustrated in Figure 1.3(a). The reason is twofold. First, the transparent anode, typically indium tin oxide (ITO), is conventionally sputtered first before depositing OLED materials to avoid the sputter-induced damage to the OLED. Secondly, the cathode requires a low resistance to avoid a voltage drop across the display panel. Therefore, an opaque metal layer with low resistivity is used as opposed to ITO. In such cases, maximizing aperture ratio becomes challenging as one more TFT is required per pixel compared to an LCD. Fortunately, this can be overcome by using a top-emitting OLED structure, made possible by using a transparent top electrode and a reflective bottom electrode. However, top-emitting OLEDs are restricted to small size applications where the voltage drop across the resistive transparent top electrode is insignificant.

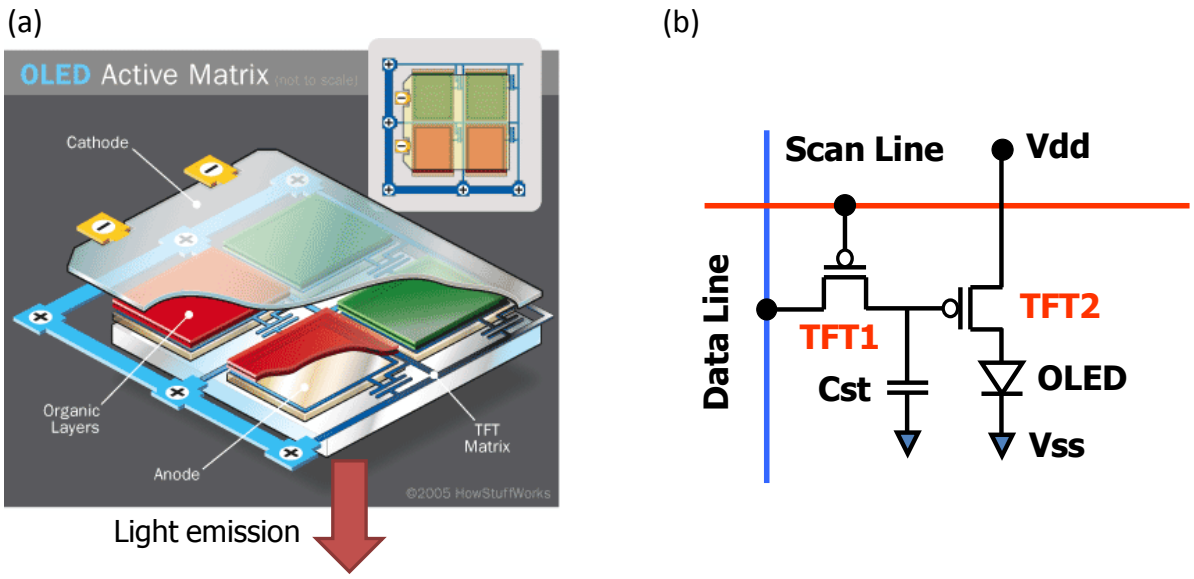

Figure 1.3 (a) Basic architecture of an AM-OLED (Image courtesy of 2005 www.HowStuffWorks.com) (b) Schematic diagram of an AM-OLED pixel. Transistors shown are p-type.

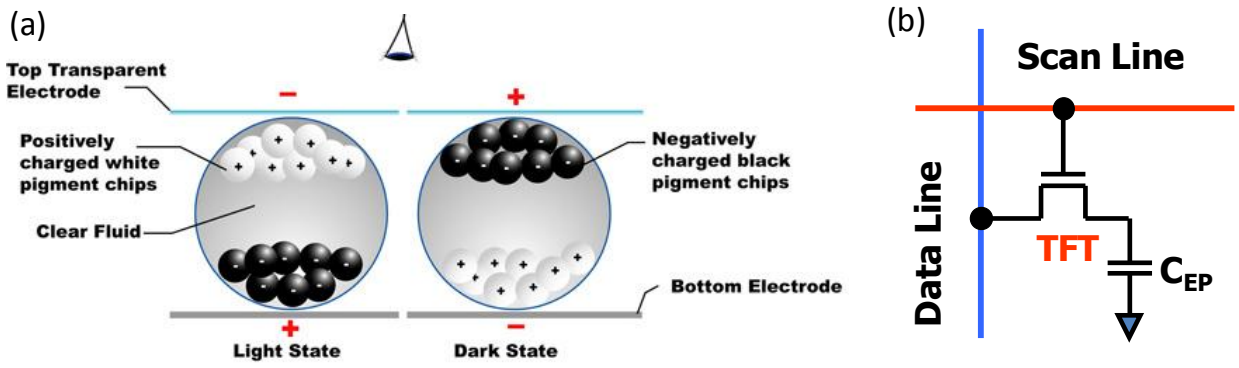

Figure 1.4 (a) Electrophoretic displays (Image courtesy of Pervasive Displays) (b) Schematic diagram of an AM-EPD pixel.

A third type of display technology has neither a backlight source nor light emitting component. Instead, electrophoretic displays (EPD) utilize the reflective daylight to mimic the appearance of ordinary printed paper. EPD can be read under direct sunlight and requires no power to maintain the display content, making it the most promising technology for E-book applications. Figure 1.4(a) shows the cross-sectional structure of the EPD, which is composed of millions of microcapsules sandwiched by two parallel electrodes. Each microcapsule contains positively charged (white) and negatively charged (black) pigment chips suspended in a clear liquid. Applying a negative electric field (with respect to the top electrode) results in an appearance of white dots on the top. Conversely, applying a positive electric field results in a black pixel. The simple operation of EPD results in a pixel with only one TFT as illustrated in Figure 1.4(b). Aperture ratio is no longer a concern in designing such pixels as the display is purely a reflective type.

The cost of the display component is significant in relation to the overall system cost, and this fact holds for both higher resolution tablet displays and lower resolution E-book displays. The display technologies introduced previously all employed AM-TFT array as a backplane, which is fabricated by a process consisting of lithography and vacuum-process steps. As previously discussed, utilizing a printing process to eliminate these major cost points can potentially lower the display manufacturing cost. Nevertheless, for high resolution displays, manufacturing an AM-TFT array via a printing-only process remains challenging due to the poor resolution achievable [9]. As a result, printing is more feasible for realizing low-cost and low-resolution displays. Unfortunately, lower resolution limits the display content, which in turn contradicts the increasing demand for information. Therefore, a flexible or roll-able display, which allows the use of a large display area as well as a minimum storage size when folded, has become a solution to this dilemma.

The flexible display uses a less expensive plastic substrate, which allows the incorporation of roll-to-roll and high throughput processing to further reduce the manufacturing cost. The technologies implemented in the flexible display will most likely be AMOLED and AMEPD, as the technical obstacle in integrating a backlight source into a flexible display still exists. Although AMEPD is promising to realize low-cost and flexible display, the monochrome display content limits its use to E-book applications. For flexible AMOLED, a large display area necessitates the use of the bottom-emitting type structure. As indicated previously, maximum aperture ratio is favorable to achieve high brightness and contrast. This can be made possible by scaling down the printed transistor size, i.e. channel length and width, to obtain the same current level with much smaller occupying area. Scaling will also help achieve higher resolution AM-TFT array by printing technique.

Unlike the printed RFID application, which requires high-speed printed transistors, displays only require an operation speed of 10-100 KHz. Consequently, the speed-limiting gate-to-source/drain overlaps have been used by the design rule to compensate for the poor registration capability of printing technique. However, these parasitic capacitances can disturb the voltage stored in the C_{ST} via capacitive-coupling from the scan line. This well-known feed-through problem can limit the employment of higher gray scale [10]. As a result, printed transistors with minimum parasitic capacitance are favorable. The approach in achieving a minimum overlap capacitance will be discussed in Chapter 3.

1.3. Printing techniques

A variety of techniques have been used in the printing industry, including screen printing, offset printing, gravure, flexography, inkjet printing, etc. Screen printing has been largely employed in the application of printed circuit boards, in which a thicker and lower resolution film is deposited. However, among the various printing techniques, gravure and inkjet printing are the most attractive systems to realize printed electronics due to their relatively high printing resolution.

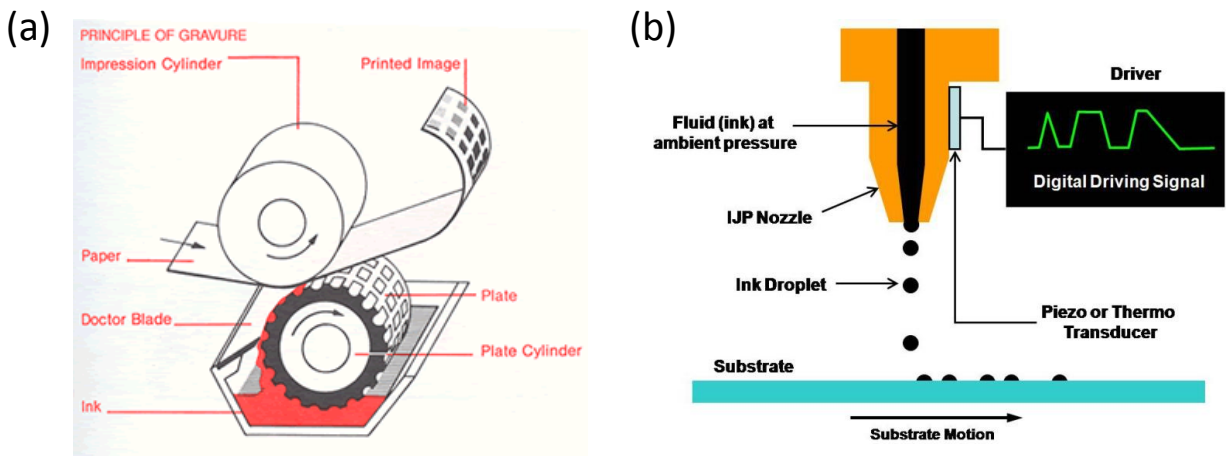

Figure 1.5 (a) Principle of gravure printing (Image courtesy of Prism Pak, Inc.) (b) Inkjet printing system

Figure 1.5(a) shows a typical gravure system, consisting of a plate cylinder, a doctor blade, and an impression cylinder. The plate cylinder has a pre-defined pattern on the surface, typically consisting of various size wells. The ink is coated on the cylinder as it turned through a reservoir. The excess ink on the cylinder surface is then wiped off by the doctor blade. The remaining ink filled inside the wells is then transferred to the substrate as it turns and contacts the substrate. As a result, the pre-defined pattern is printed on the substrate in a high-throughput fashion. Unlike gravure printing, in which cylinder-substrate contact is necessary for pattern transfer, inkjet printing is purely non-contact printing. As illustrated in Figure 1.5(b), inkjet printing uses piezoelectric or thermal actuation to eject ink from a reservoir and to deposit the droplet on the substrate. A pattern is then generated by either moving the inkjet nozzle or substrate to enable drop-on-demand printing. The flexibility of the inkjet system allows the pattern to be adjusted on-the-fly. This in turn eliminates the turn-around time for the pattern adjustment required by any other pre-defined pattern system. This non-contact and additive printing feature is well-suited for sensor applications, in which various sensing materials are printed separately without interfering with each other. Furthermore, the inkjet system has been utilized in the display industry to deposit polymer OLEDs and color filters on the AM-TFT array [11]. More inkjet details will be discussed in Chapter 2.

While the gravure system is attractive for industrial high speed manufacturing, the fundamental mechanism of ink transfer for highly-scaled features remains unclear. Therefore in this thesis, inkjet printing was used extensively for the study of printed transistor scaling, as the mechanism of droplet and line/pattern formation were well understood [12], [13]. However, the serial printing characteristic of the inkjet system limits the throughput of the printing. To overcome this disadvantage, there have been inkjet systems utilizing hundreds to thousands of nozzle to realize throughput enhancement via parallelization [14]. Whether this multi-nozzle inkjet system will be feasible to realize low-cost printed electronics is currently uncertain. Nevertheless, the flexibility of the inkjet system is still best suitable for a research purpose.

1.4. Scaling of the printed transistors

Scaling down transistors has traditionally been pursued to enhance the transistor performance by lowering the inherent and parasitic capacitances. For printed transistors, solution-processable materials have advanced rapidly to enhance the performance of printed devices [15]. However, the poor printing resolution of state-of-the-art printing techniques has necessitated the use of large channel length and large gate-to-source/drain overlap to compensate the miss-alignment resulting from the poor layer-to-layer registration capability. These large dimensions have prevented printed transistors from gaining commensurate speed improvement via advanced materials. As a result, scaling of the printed transistor is pursued, in a similar fashion to silicon technology, to enhance the transistor performance in achieving higher operation speed.

The speed of the transistor is conventionally determined by measuring the oscillating frequency of a ring oscillator consisting of odd stages of inverter circuits. This requires the implementation of a printed ring oscillator, which is beyond the scope of this thesis. Instead, the propagation delay of a single stage inverter as well as the cut-off frequency of a single transistor is reported. Both inverter delay and cut-off frequency show a relation proportional to $\mu V_{DD}/L(L+L_O)$, where μ, V_{DD}, L *and* L_O are the mobility, the voltage supply of the circuit, the channel length, and the total overlap length between gate and source/drain of the transistor, respectively. In order to maximize the speed, V_{DD} could be increased. However, as higher voltage leads to increased power consumption, this is generally not an acceptable solution. Maximizing mobility is thus a promising pathway to achieve high speed. Given this need, there has been significant amount of research demonstrating high-mobility printable materials [16], [17]. However, these materials were mostly demonstrated using test structures consisting of a thermally grown oxide and evaporated gold electrodes with modified surfaces. It is currently unclear whether the high performance characteristics can be transferred to a fully printed structure. Therefore, this thesis will focus on the scaling of channel length as well as minimizing the overlap capacitance to achieve high speed operation in fully-printed transistors.

1.5. Thesis organization

This thesis is organized in the following manner. Chapter 2 will introduce the inkjet printing system as well as inkjet fundamentals. Basics of electronic inks, wetting behavior on surfaces and transistor operations will be reviewed. Baseline inkjet printing process required for a printed transistor will be discussed. Chapter 3 will introduce and discuss a novel self-aligned printing technique to achieve minimal overlap capacitance in printed transistors. Optimization of printed inverters will be discussed. Chapter 4 will introduce a novel print-and-drag technique to scale down the printed gate line to surpass the limitation of conventional printing resolution. Various printing parameters associated with the printed features will be discussed. Chapter 5 will introduce and discuss novel processes for achieving channel length scaling. Highly-scaled fully-self-aligned printed transistors with cut-off frequency over 1 MHz will be demonstrated. Chapter 6 will conclude the thesis and outline the potential future work.

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Chapter 2 Inkjet-Printed Transistors: The Basics

2.1. Introduction

As discussed in the previous chapter, inkjet printing is attractive due to its additive and contact-less processing. Moreover, the flexibility of pattern adjustment has significantly reduced the research time required from idea to proof-of-concept demonstration. Therefore, there has been increasing research studying passive and active printed devices using inkjet exclusively [1–4]. Simultaneously, advances in nanoparticle synthesis and ink formulation have made printable materials such as metal inks widely available. This allows the printing of more sophisticated structures, including highly-scaled transistors and integrated circuits. It is thus necessary to understand and optimize the baseline process of individual printed layers, as well as inter-layer integration by inkjet printing.

Therefore, in this chapter, we will first introduce the inkjet technology as well as the printer systems used extensively in this thesis work. The inkjet waveform used by the piezoelectric inkjet nozzle will be reviewed in the following section. The fundamentals of printable ink, ink-surface interactions and the operation principles of printed organic thin film transistors will be reviewed. Finally, baseline inkjet printing processes required for a printed transistor will be discussed.

2.2. Inkjet technology

Consumer inkjet printers today mainly use two different inkjet nozzle technologies: thermal-bubble jets and piezoelectric jets. A thermal-bubble jet nozzle consists of an ink reservoir and a heating element as sketched in Figure 2.1(a). The operation principle is as follows: To eject a droplet, a pulse of current is passed through the heating element to rapidly vaporize the nearby ink. A bubble forms and expands, creating a pressure wave to push out the ink into a droplet. The heating element then cools down rapidly, resulting in a vacuum that refills the ink reservoir.

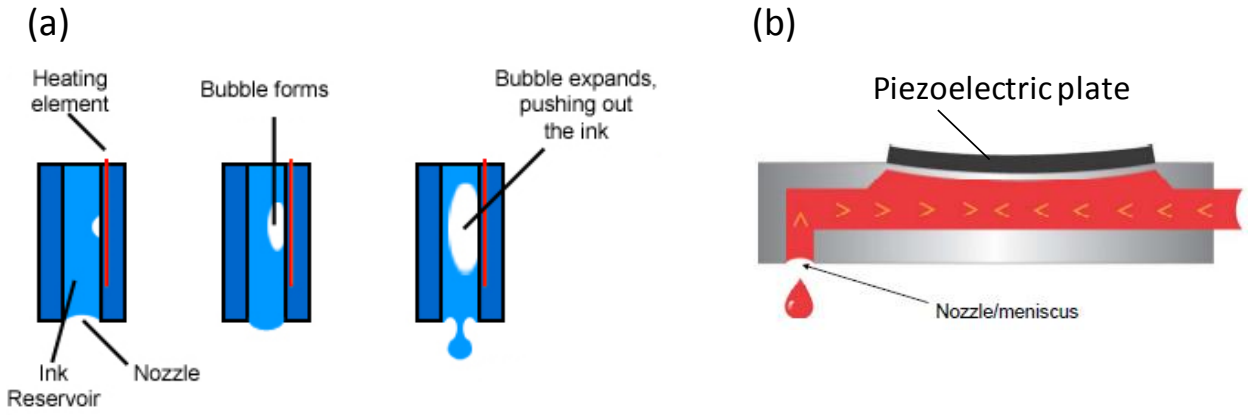

Figure 2.1 (a) Schematic diagram of a thermal-bubble type inkjet nozzle (b) Schematic diagram of a piezoelectric type inkjet nozzle.

The heating elements are resistive heaters typically made from poly-silicon. Hence, the nozzles can be fabricated using conventional silicon and MEMS (microelectromechanical systems) processing. As a result, this type of nozzle is typically cheaper to manufacture, as no special materials such as piezoelectric crystals are required. Due to the low cost, the print heads can be disposed when the nozzles are clogged or become otherwise nonfunctional. Therefore, majority of the consumer inkjet printers available today utilize thermal-bubble technology. Another advantage of the thermal-bubble jet is that the chamber is insensitive to trapped air within the chamber, as the jetting does not rely on the mechanical compression of the ink.

Thermal-bubble jet has several disadvantages. The nozzles typically suffer from a short life-span due to residue build-up on the heating element. Also, special ink is required to resist rapid thermal change. For these reasons, thermal-bubble jets are not suitable for printing electronic devices, where the inks used are not compatible with the sudden heat change, e.g. metal nanoparticles can be sintered due to the heat, resulting in deposition of metal layers on the heating elements. This can reduce the heating efficiency of the heating element due to a resistance drop, and eventually causes the malfunction of the nozzle.

For piezoelectric jets, a piezoelectric plate is used as an actuator inside the ink chamber, as shown in Figure 2.1(b). To eject a droplet, a voltage pulse is applied to the piezoelectric plate to cause a deflection, creating an acoustic wave that propagates inside the chamber to eject the droplet. Due to the fast actuation of the piezoelectric plate (~μs), the piezoelectric nozzle can jet faster than the thermal-bubble type, where the latter is limited by the extra time required in the cooling step. Unlike thermal-bubble jet, a piezoelectric inkjet applies no thermal stress to the ink. Therefore, a wider range of inks can be used to print electronic devices. All of the inkjet printing studies in this thesis were performed using piezoelectric nozzles. The details of piezoelectric jetting will be discussed in section 2.3.3.

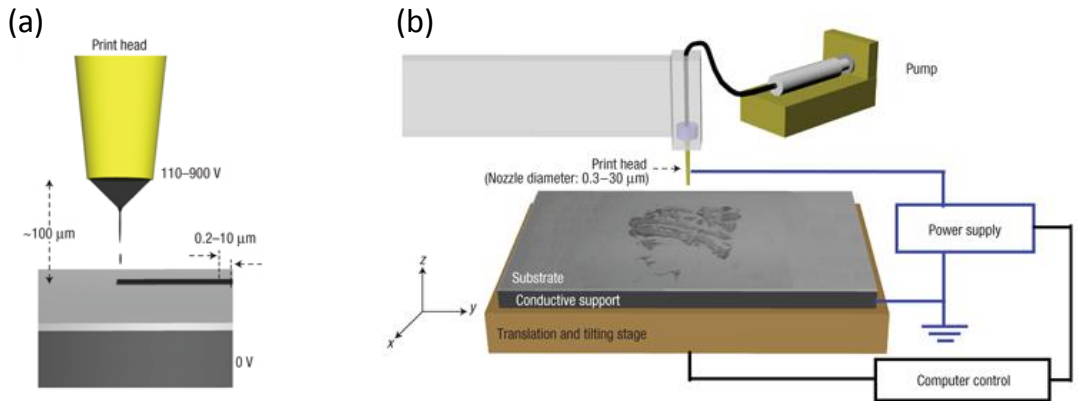

Figure 2.2 Electrohydrodynamic inkjet system (a) nozzle and substrate configuration (b) printer setup.

The inkjet printing resolution is fundamentally limited by the minimum drop volume delivered by a system, typically a few picoliters to few tens of picoliters for piezoelectric nozzles. To overcome this limitation, electrohydrodynamic inkjet systems use electric fields, rather than thermal or acoustic energy, to create drop volumes down to the range of femtoliters to print high resolution patterns [5], [6]. Figure 2.2(a) and (b) shows the setup of such a system, consisting of a gold-coated glass micro-capillary nozzle as a print head and a substrate supported by an electrically grounded plate. A high voltage is applied between the nozzle and the substrate to

deform the meniscus from the nozzle tip and to force out a small droplet. These droplets then eject onto the substrate to produce high resolution patterns. The lines printed in this fashion can be as small as 700 nm in width. However, the small drop volume necessitates multi-pass printing to produce a conductive metal line for device applications [6]; this limits the throughput of the printing. Moreover, the requirement of a metal ground plate under substrates can complicate the implementation of roll-to-roll printing. Therefore, whether the system can be scaled up to large area, high speed and multi-nozzle printing remains questionable.

2.3. Inkjet printers

The inkjet printers used in this thesis are all piezoelectric jet systems, including a Dimatix DMP series and a custom-built inkjet printer. The DMP system was used for all the line printing, due to its smaller drop volume and hence smaller achievable linewidth. The custom-built printer was used for printing semiconductor only. Both systems have advantages and disadvantages, and will be discussed in the following section. The details of both printers can be found elsewhere [7], [8].

2.3.1. Dimatix

The Dimatix DMP-2800 series is a state-of-the-art commercial research inkjet printer. It is a self-contained system with a chamber consisting of a letter-size substrate, a cartridge holder module, a drop watcher module, etc. as shown in Figure 2.3(a) and (b). The stage motor has a 5 µm resolution and repeatability of ±25 µm. This resolution and mechanical accuracy is not high enough to achieve consistent alignment in printing highly-scaled devices. Therefore, self-aligned printing was pursued in Chap. 3 to overcome this limitation. The substrate stage can be heated up to 60 ℃, which is insufficient for in-situ sintering (often requires >100 ℃) of the nanoparticle ink. Additionally, the substrate heating can unintentionally raise the nozzle temperature and degrade the jetting stability, due to fast solvent evaporation at the nozzles. This is difficult to prevent, as no cooling (only heating) module is implemented into the nozzles to stabilize the jetting temperature. Therefore, the use of substrate heating is limited to slightly enhance the drop drying to improve the drop pinning on dewetting surfaces.

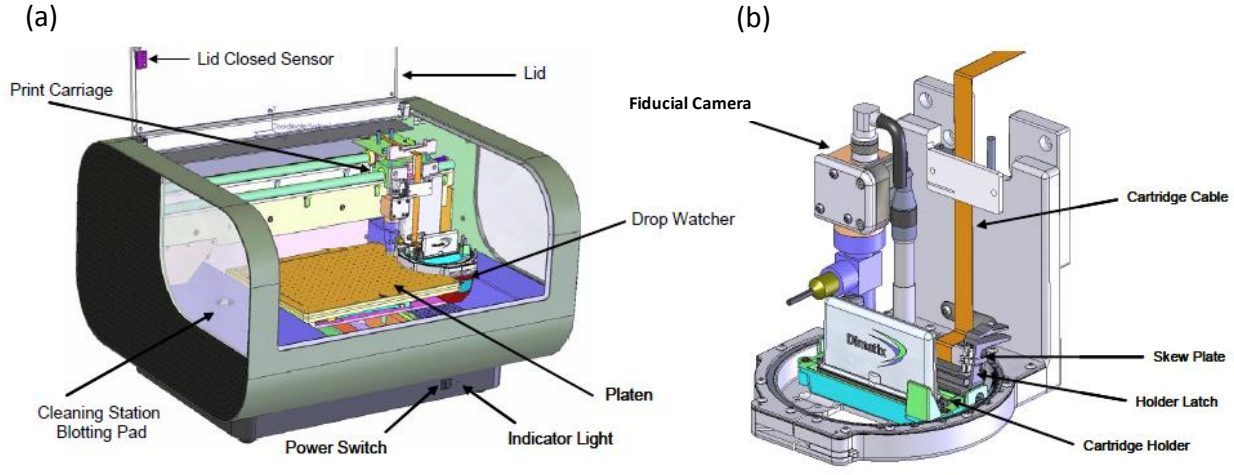

Figure 2.3 (a) Dimatix material printer (b) printer cartridge assembly [7].

The cartridge consists of a fluid module with a built-in fluid bag, and a jetting module with 16 piezoelectric jetting nozzles, each with an integrated reservoir and heaters. Note that the heaters are only used to elevate the jetting temperature to lower the viscosity of viscous fluid to obtain stable jetting. The nozzles can deliver a drop volume of 10 pL; 1 pL nozzles, although available, were not used in this work due to the high evaporation rate at the meniscus, causing frequent clogging of the nozzles. The desired printing pattern can be generated using the built-in software or by converting a bitmap pattern file. However, the pattern can only be printed in a raster manner, i.e. one row at a time, even when printing a vertical line. This has restricted the printing of single pixel lines used in highly-scaled printed devices to be horizontal, as the printing of vertical lines can show rough edges. The X-axis and Y-axis drop spacing are coupled by the original design, which is unfavorable for printing line arrays with various drop-spacings when testing a baseline process. Despite with these limitations, however, the DMP printer provides a platform for robust printing routine, due to its high usability: The built-in software provides a fast alignment function through a theta calibration. A cartridge with pre-loaded ink requires only minutes to start printing on regular substrates, as 16 nozzles in a cartridge provides redundancy, i.e. even with clogging nozzles, stable jetting can still be found on several nozzles to perform stable printing. Standard nozzle cleaning routines including spit, purge and blot of the nozzles are well established, allowing for an efficient cleaning procedure. A wide range of fluids can be used in the DMP though optimization of the jetting waveform, which will be discussed in section 2.3.3. Overall, DMP system, albeit with limitations in pattern flexibility, is reliable and suitable for printing all the baseline electrodes for electronic devices.

2.3.2. Custom-built inkjet printer

A custom inkjet printer was built by various researchers in our group, and it is one of the first research-oriented inkjet printers built in the last decade [8]. Figure 2.4(a) and (b) shows a schematic diagram and a photograph of the system, consisting of a single Microfab piezoelectric inkjet nozzle, and a high precision moving stage. A side camera is used to inspect the meniscus and monitor the drop velocity. Another camera is used to observe and monitor the printed pattern on underlying substrates.

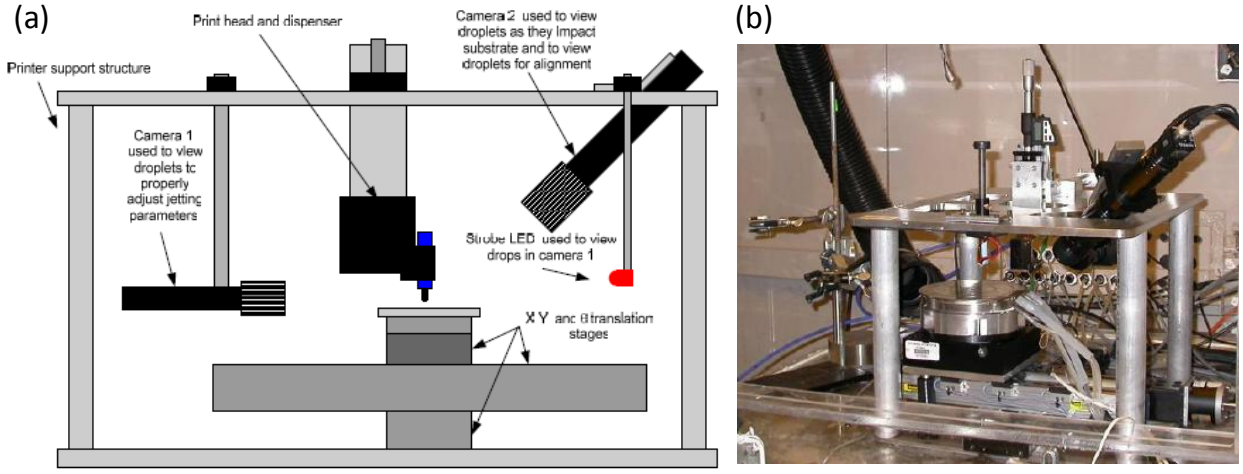

Figure 2.4 The custom-built inkjet system using a Microfab inkjet nozzle [8].

Unlike the Dimatix, which uses a raster printing method, this printer uses a vector printing method. This is made possible by implementing drop-on-demand printing using a fixed-position nozzle and a moving stage with X and Y stepper motors. This design is not common in industrial inkjet printers, as the substrates are typically large to move; on the other hand, the nozzles or print heads are typically lightweight and hence are more efficient to move. In our printer, the substrate has a small size similar to a 6 inch wafer, and therefore the design consisting of a stationary nozzle and a moving stage is simpler. Using this design, the stage can move without restrictions and thus arbitrary patterns such as spiral and zigzag patterns can be printed in a single printing pass. The advantages offered by this flexible patterning scheme allow the methodology of inkjet-pattern generation to be studied [9].

The moving stage has a precision of 1.3 µm in both X-Y directions. While this resolution is high, drop placement can still vary ±10 µm due to variation in jetting angular deviation [10]. This again suggests that self-aligned printing is necessary to achieve highly-scaled devices. The stage also has a rotational stepper motor with 0.5 arcminutes of angular precision. The rotation is used to align the printing direction to substrates with pre-patterned layers.

The substrate can be elevated to a high temperature of 300℃, with a water-cooling circulation system to protect the motor underneath the heated substrate surface. The high temperature heating can be used to sinter nanoparticles as well as crosslink polymer insulators. A heater and water-circulation are also implemented into the nozzle holder, allowing stabilization of the jetting temperature even with the substrate heated.

The drop volume of the nozzle is 80 pL. The relatively large drop volume is best suited for depositing a planar thin film rather than electrodes with highly-scaled dimensions. The ink delivery path and the glass nozzle can resist aggressive solvent such as toluene, which is a common organic solvent used for jetting organic semiconductors. Therefore, this printer was used to print the semiconductor layer exclusively in this work.

2.3.3. Jetting waveform

The jetting in the piezoelectric nozzle is controlled by a waveform applied to the piezoelectric plate. Both inkjet systems mentioned previously have similar waveforms; thus the waveform used in the Dimatix will be reviewed. For the Dimatix system, the ink reservoir was fabricated using silicon MEMS processes to create an internal chamber and a membrane designed to be deflected by a piezoelectric material, PZT (Lead zirconate titanate). As illustrated in Figure 2.5, droplet formation is driven by a waveform that can be divided into four segments. The amplitude and the slew rate of the waveform determine the amount and the rate of the PZT deflection respectively. In the first phase, a decreased voltage is applied to retract the PZT to draw fluid into the pumping chamber, followed by a settling time. This section creates two in-phase acoustic waves that propagate from both ends of the chamber and travel in opposite directions. The duration of the first phase is thus selected such that at phase two, the PZT expands precisely when the two waves meet at the center to push out a droplet with its maximum energy [11]. Higher droplet energy can be also achieved by using a steeper slope in phase two, resulting in a faster PZT deflection. At phase three, the PZT retracts slightly from phase two to break the droplet from the chamber. The intermediate voltage in phase three also provides a damping effect to prevent air from being sucked back into the chamber. Finally, the voltage returns back to the standby state in phase four.

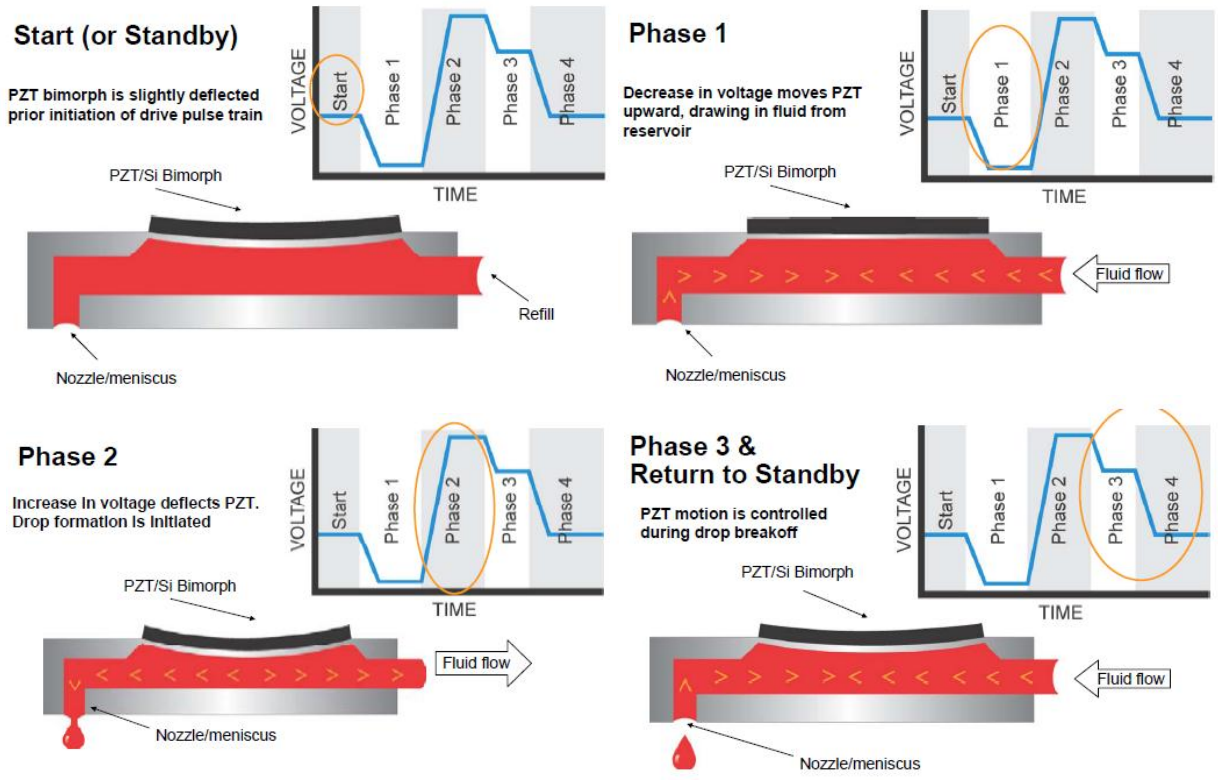

Figure 2.5 The diagram of a piezoelectric nozzle chamber showing the 4 phases of the jetting waveform and their corresponding PZT deflection [7]

Drop velocity is an important parameter typically used to evaluate droplet jetting. The jetting waveform is typically optimized such that efficient jetting is achieved by obtaining the desired drop velocity using a minimum voltage. Higher drop velocity is desired, as the jetting accuracy can be improved by a reduced time-of-flight of the drop [10]. In addition, the drop velocity needs to be stabilized, as variations in drop velocity can result in variations in drop position, based on the relative motion between the nozzle and the stage. Moreover, in a multi-nozzle system, drop velocities between nozzles need to be matched in order to prevent variations in drop positions [12]. Therefore, the drop velocity is typically monitored before and during the printing to ensure a reliable printing process.

The drop velocity is a function of the firing voltage, ink viscosity and surface tension. In the DMP system, a drop velocity of 6-10 m/s is desired; therefore, an ink with viscosity of 10-12 cP and surface tension of 28-33 dyn/cm is recommended to obtain stable jetting [7].

2.4. Inkjet printing for electronic applications

Printing electronic devices is more challenging than printing media for human eyes. The former requires optimized jetting as well as good film qualities (i.e. good electrical properties and smooth surfaces), while the latter requires mainly a precise color mixture and drop positioning. Therefore for inkjetting electronic devices, the engineering of ink and ink-surface interaction are crucial in achieving an optimized thin film. Thus, the following sections will introduce electronic inks and discuss the wetting characteristic of inks on surfaces.

2.4.1. Electronic ink

Among the various printed electronic devices, active components such as transistors require the most layers of materials. In order to inkjet-print a transistor, three categories of inks are needed: conductor, insulator and semiconductor inks.

There are organic and inorganic types of conductor inks. The most common organic conductor ink is poly(3,4-ethylenedioxythiophene) doped with polystyrenesulfonic acid (PEDOT:PSS), where PSS is used to improved the conductivity of PEDOT [13]. PEDOT:PSS is a transparent conducting polymer that is widely used in OLED and solar cell applications as transparent electrodes [14]. PEDOT:PSS is soluble in water, therefore water can be used as the solvent for inkjetting. This is beneficial as water is widely used as a solvent in traditional graphic media printing; hence the conventional printing knowhow can be applied. However, the conductivity of PEDOT:PSS is in the range of 0.001-2 S/m, which is insufficient for the applications of S/D electrodes and interconnects.

The most commonly used inorganic conductor ink is nanoparticle-based ink. In such an ink, nano-crystals of metallic particles are encapsulated using an organic encapsulant/dispersant. The nanoparticles can then be dispersed in common organic solvents for inkjetting. After printing of such an ink on a substrate, a heating step is used to firstly drive off the solvent, followed by the disassociation of the encapsulant, and finally the merging/melting of metallic particles results in a metal thin film. The process is illustrated in Figure 2.6 (The growth of particles has also been reported to occur with the presence of attached encapsulant. The detailed discussion can be found elsewhere [15]). The melting particles can regain the conductivity of the bulk counterpart. Sintered gold nanoparticle has been demonstrated with a conductivity as high as 3×10^7 S/m (70% of bulk gold conductivity) [4]. Therefore, nanoparticle inks are promising for producing electrodes for printed devices through printing.

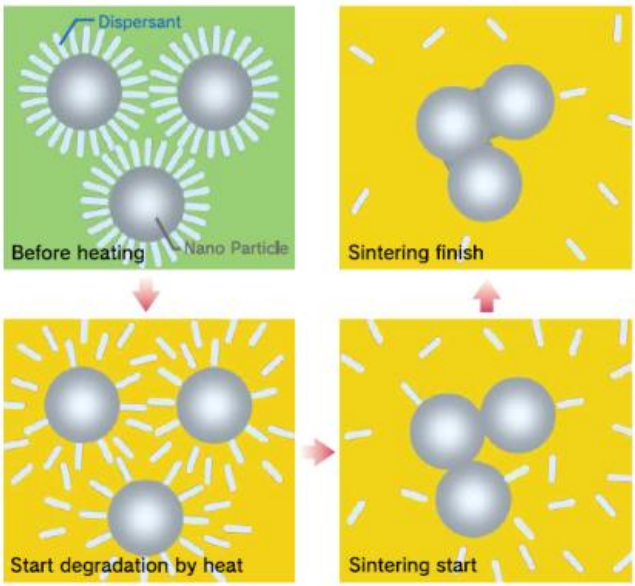

Figure 2.6 Schematic illustration of a general sintering process of nanoparticle inks [16]

The sintering temperature of the nanoparticles is determined by the size of the particles and the encapsulant. Due to a high surface-to-volume ratio, the melting point of metal nanoparticles is significantly reduced relative to the bulk melting point. Butane-thiol encapsulated gold nanoparticles with 1.5 nm size have been demonstrated to sinter at a plastic compatible temperature of 120 ℃ [17]. With the dual advantages of high conductivity and low sintering temperature, nanoparticle inks are used exclusively in this thesis for baseline electrode printing.

For the insulator ink, organic dielectric materials are more widespread than their inorganic counterparts. The most commonly used polymer dielectric is Poly(4-vinylphenol) (PVP), with its chemical structure shown in Figure 2.7(a). PVP has been used as a standard dielectric in studying organic transistors for years [18]. Poly(melamine-co-formaldehyde) (PMF) is typically used as a crosslinking agent to chemically crosslink the PVP into an electrical insulator, with a heating step of 180 ℃. The chemical structure of PVP crosslinked by PMF is shown in Figure 2.7(b).

PVP can be dissolved in alcohol based solvents for inkjetting. The advantage of inkjetting a polymer comparing to a nanoparticle ink is that the viscosity can be adjusted directly by changing the polymer concentration in the solvent. As shown in Figure 2.7(c), the viscosity of the ink with PVP dissolved in 1-hexanol increases with PVP concentration. Using this relation, 7.6 wt% PVP dissolved in 1-hexanol was used to obtain a viscosity ~10 cP, required by Dimatix print-heads. PMF with a concentration of 0.6 vol% was also added into the ink as a baseline crosslinking agent.

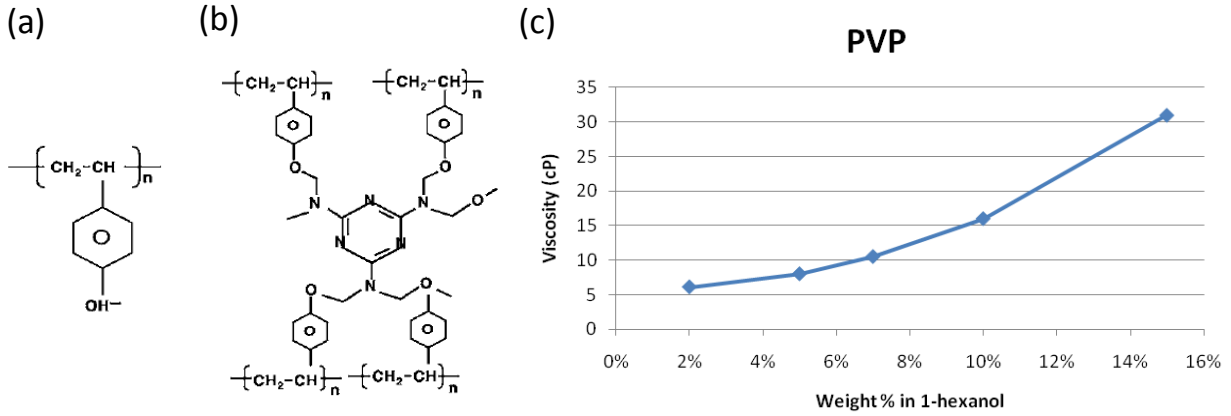

Figure 2.7 Chemical structure of (a) Poly(4-vinylphenol) and (b) PVP cross-linked by poly(melamine-co-formaldehyde) [19] (c) Ink viscosity as a function of PVP concentration in 1-hexanol [20].

Semiconductor inks typically consist of an organic semiconductor dissolved in one or more organic solvents. Among the various organic semiconductors studied to date, pentacene is the most studied material that has exhibited the highest mobility for years [21], [22]. Furthermore, pentacene has better oxygen and moisture stability than most soluble organic semiconductors. Therefore, there have been several attempts to synthesize soluble pentacene for achieving inkjet-printable and high performance materials.

The first approach was to synthesize a soluble pentacene precursor [23]. The chemical structure of the pentacene precursor is shown in Figure 2.8(a). The precursor can be inkjet-printed, and a high quality pentacene thin film can then be produced by a thermal conversion as illustrated in the reaction diagram in Figure 2.8(a). With this precursor, a fully inkjet-printed high performance transistor has been demonstrated [24]. The impact of annealing temperature and

time to the mobility has been studied in detail [25]. A high temperature ~160 ℃ and short annealing time is desired to promote the formation of a monolayer. Conversely, high temperature and long annealing time can cause the film dewetting, resulting in low mobility.

The second approach was to develop TIPS (triisoprophylsilylethynyl) pentacene [26]. Unlike the aforementioned pentacene precursor, which requires a heating step to be converted back to pentacene, TIPS pentacene has two bulky functionalized groups that attaches to the pentacene backbone permanently, as shown in Figure 2.8(b). These functionalized groups not only impart the solubility of the molecule, but also can induce strong π-π stacking to enhance intermolecular orbital overlap. As a result, TIPS pentacene was demonstrated with a solution process and showed a high mobility >1 cm^2/Vs [27]. It is thus attractive to explore inkjetted TIPS pentacene in printed transistors.

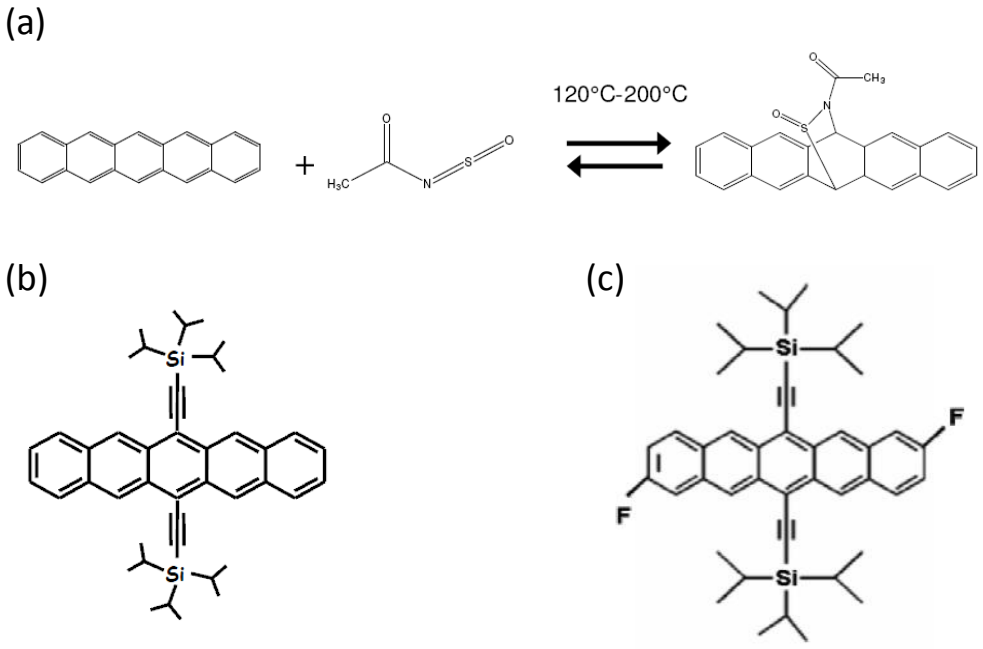

Figure 2.8 (a) Chemical structure and the reaction diagram of the pentacene precursor. Chemical structures of (b) TIPS pentacene and (c) TIPS-CFP

TIPS-CFP (triisoprophylsilylethynyl cata-fluoro-pentacene) shown in Figure 2.8(c) is an alternative to TIPS pentacene. In this molecule, two fluorine atoms were functionalized to the pentacene backbone to enhance the interaction with fluorine-treated S/D electrodes to improve contact resistance and effective device mobility [28]. Additionally, the addition of fluorine atoms can improve molecular stability in solvents due to the presence of electron withdrawing fluorine substituents [29].

Both pentacene precursor and TIPS pentacene are highly soluble in apolar organic solvent such as anisole and chloroform. Hence the formulation of semiconductor inks is more straight-forward. However, the wetting and drying behavior of the inkjetted TIPS pentacene is critical to achieve good mobility, as the TIPS pentacene crystallizes upon drying. More discussions on the inkjetting of pentacene will be provided in section 2.6.3.

2.4.2. Wetting of inks on surfaces

The wetting characteristics of inkjetted drops on surfaces are crucial for controlling the formation of lines and thin films. The drop has two wetting regimes: partial wetting and total wetting as illustrated in Figure 2.9(a) [30]. A spreading parameter *S* is defined to distinguish the wetting behavior. *S* measures the difference between substrate surface energy γ_{SO} and the sum of ink surface tension γ and solid-liquid interaction γ_{SL}, as shown in Figure 2.9(a). When *S* is negative, the drop forms a spherical cap on the substrate with an equilibrium contact angle θ_E. This is favorable in printing lines for electrode applications, as the thickness and the linewidth can be controlled with varying drop spacing and layers (will be discussed in section 2.6.1). When *S* is positive, the liquid can spread completely in order to minimize its surface energy. This is desirable for printing thin insulators and semiconductors. However, the resulting thin layer typically exhibits a coffee ring effect due to an enhanced evaporation at the contact lines, which will be discussed later.

To change the wetting characteristics, substrate surface treatments are typically used to change the contact angle. As illustrated in Figure 2.9(b), a contact angle θ_E is determined by Young's relation, describing the balanced tension between γ_{SO}, γ and γ_{SL}. To improve the wetting, a higher γ_{SO} surface or equivalently a more hydrophilic surface is preferred (assuming a hydrophilic ink for now). An example of rendering the surface more hydrophilic can be found in section 2.6.2. On the contrary, a lower γ_{SO} surface or a more hydrophobic surface can be used to reduce the size of a pinned drop, in achieving smaller printed lines. However, when θ_E is larger than 90°, the drop become unstable and can dewet the surface. Therefore, for a surface consisting of both hydrophobic and hydrophilic regions, e.g. a hydrophobic PVP with hydrophilic sliver S/D surfaces, optimization of surface treatment is required to obtain uniform wetting of inks on such surfaces. Section 2.6.3.2 will discuss the optimization in detail.

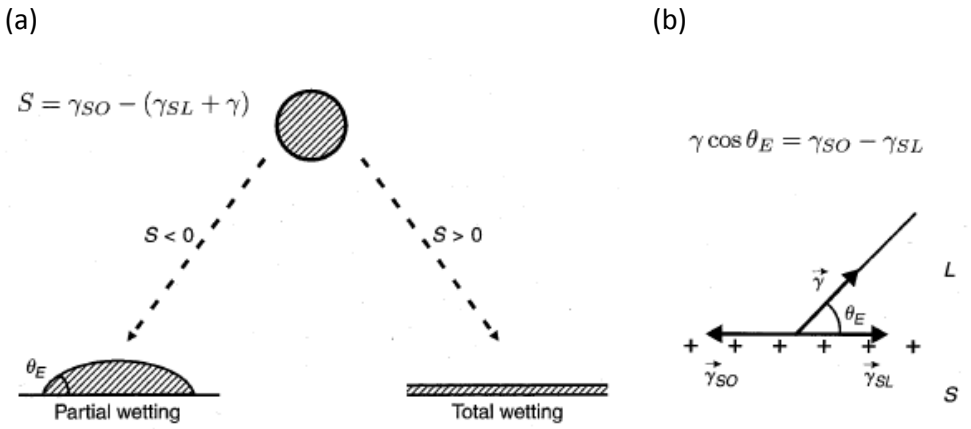

Figure 2.9 (a) The two wetting regimes for a drop (b) Equilibrium contact angle determined by Young's relation [30].

As previously mentioned, a coffee ring effect can easily occur when the inkjetted drop completely wets the surfaces. The coffee ring effect was first explained by Deegan et al. [31], stating that the non-uniform drying of a drop can lead to an excess of solute at the edges, as shown in Figure 2.10(a). This is due to higher evaporation at the pinned contact lines, causing outward convective flow to replenish the lost solvent at the edges. This flow also carries the

solute in the drop and thus results in the accumulation of solute at the edges. The coffee ring is detrimental to film formation, as relatively thicker films are deposited at the edges. An example of channel leakage current induced by the coffee ring can be found in section 2.6.3.1.

The coffee ring effect can be mitigated using several methods. Reducing the substrate temperature has been demonstrated to eliminate the coffee ring [32]. In such case, the cooled substrate can retard the rim evaporation much more than in the center, resulting in reduced outward flow and hence reduction of coffee ring formation. Another method incorporates the use of a co-solvent system to suppress coffee ring [33]. Figure 2.10(b) illustrates the principle. The general idea is to add another solvent with a higher boiling point and a lower surface tension. Due to higher evaporation at the contact lines, the solvent compositions at the edges become mainly the solvent with high boiling point. As a result, the solvent at the edges has a lower surface tension than in the center, resulting in a surface tension gradient. A surface-tension-driven Marangoni flow then occurs to carry the solute inward to the center [34]. This flow can thus offset the outward convective flow, eliminating the coffee ring effect. A co-solvent has been used to print TIPS-CFP in this thesis to obtain a coffee-ring-free semiconductor layer (section 2.6.3.2).

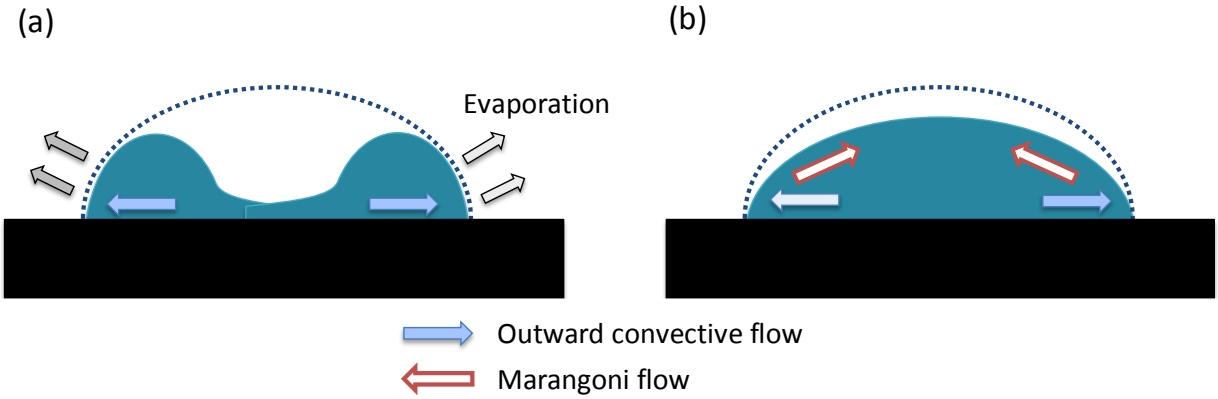

Figure 2.10 (a) Schematic illustration of the coffee ring formation (b) Schematic illustration of the coffee ring suppressed by Marangoni flow. Dotted lines represent the drop shape before drying.

2.5. Basics of organic thin film transistors

Prior to the discussion of inkjet printed transistors and the corresponding inkjetting processes, it is necessary to review the basics of organic thin film transistors (OTFTs). Therefore, in this section, various structures of OTFTs will be discussed at first. Carrier transport and contact barriers in OTFTs will then be reviewed. Finally, basic operations of OTFTs will also be introduced.

2.5.1. OTFTs structures

Various structures of OTFTs have been used depending on the purposes of the studies. Each structure has its advantage and disadvantages. For inkjetting processes, the solvent interaction

between layers is critical; therefore different structures of OTFTs will be reviewed to determine the best suited structure for the ongoing work in this thesis.

The most commonly used structure is the back-gate and bottom-contact type as illustrated in Figure 2.11(a). This structure is widely used to test the performance of semiconductor materials. A heavily doped silicon wafer is typically used as the mechanical substrate as well as the back-gate electrode. The insulator is typically thermally grown oxide. The S/D electrodes are typically evaporated gold, patterned by a lift-off method. The semiconductor can be spin-coated or printed at the end to form a complete transistor. This structure is used in this thesis for developing the analytical compact model of OTFTs with various channel lengths (see Appendix A). Due to the complete overlap between the S/D and back-gate, the structure is not suitable for testing transistor speed.

A bottom-gate and bottom-contact type OTFT is shown in Figure 2.11(b). Different from the previous one, this structure uses a patterned gate electrode, resulting in significant reduction of overlap capacitance. Solvent compatibility among layers is the main concern for inkjet printed transistors, i.e. the deposited layers can be re-dissolved by subsequent printing if non-orthogonal solvent were used. Thus, this structure is favorable for printing processes, as the semiconductor is printed at last, avoiding solvent attack from other layers.

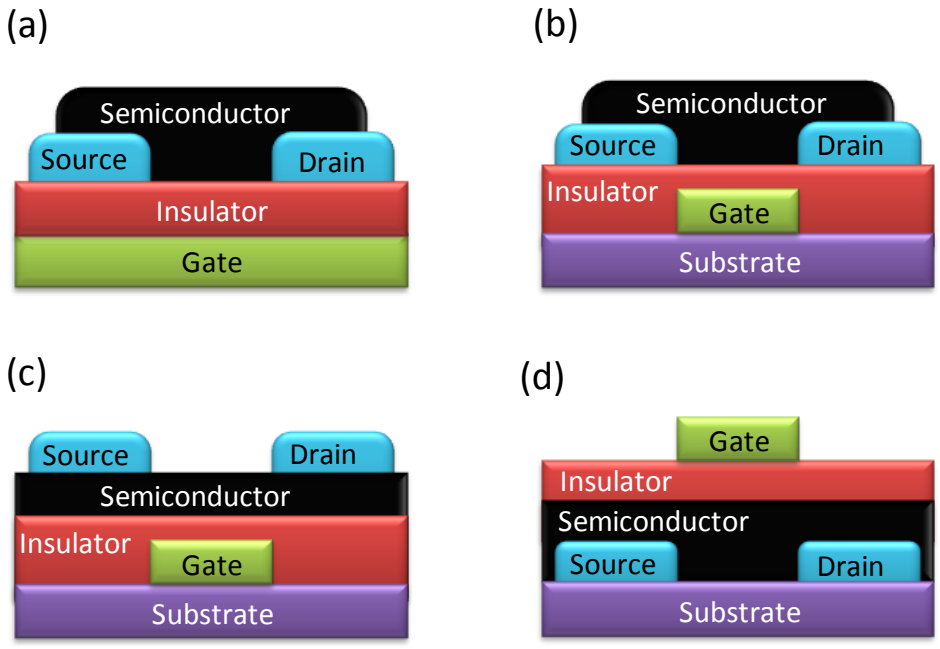

Figure 2.11 Various common OTFTs structures (a) back-gate and bottom-contact (b) bottom-gate and bottom-contact (c) bottom-gate and top-contact (d) top-gate and bottom-contact.

The third type of structure is the bottom-gate and top-contact type, as shown in Figure 2.11(c). The structure is different from the previous one in that the S/D electrodes are printed after the semiconductor layer. This structure can reduce the contact resistance between the S/D and the semiconductor, as a larger contact area is formed. However, the solvent of the S/D ink needs to be orthogonal to the semiconductor, which limits the choice of conductor inks. Furthermore, typical organic semiconductors have a hydrophobic surface, which can cause the S/D to dewet, resulting in the loss of line integrity.

Finally, a top-gate and bottom-contact structure is shown in Figure 2.11(d). This structure is the most challenging in terms of process integration, as the semiconductor layer is deposited as the second layer. The subsequent printing and heating steps can potentially degrade the semiconductor. Therefore, the selection of materials and solvents is crucial. However, this structure offers inherent encapsulation of organic semiconductors, which are typically sensitive to oxygen and moisture.

To conclude, the aforementioned bottom-gate and bottom-contact structure is most attractive in light of the semiconductor-last processes. With this structure, optimizing the transistor performance by modifying or altering semiconductor materials required less integration experimentation. Therefore, this structure is used exclusively in this thesis.

2.5.2. Charge transport in OTFTs

Organic semiconductors are conjugated π-electron systems with sp^2 hybridized carbon-carbon bonds. Figure 2.12(a) shows the classic example of a benzene ring, where a π-electron cloud is formed between π-orbitals, allowing for the delocalization of electrons through bond resonance. The π-orbitals are out-of-plane with the atoms, meaning that the conjugated π-electron cloud can interact with π-electron clouds on neighboring molecules. Due to the interaction, periodicity of molecules can result in a split of the molecular orbitals into energy bands, namely a highest occupied molecular orbital (HOMO) energy band and a lowest unoccupied molecular orbital (LUMO) energy band, which are equivalent to the valence band and conduction band in inorganic semiconductors, respectively. Unlike inorganic semiconductors, where the energy bands are formed with a large crystalline lattice of atoms, the energy bands in organic semiconductors are formed with a handful of molecules, weakly bound by van der Walls forces, resulting in narrower energy bands and lower density of states comparing to inorganic semiconductors. LUMO and HOMO levels of pentacene are shown in Figure 2.12(b).

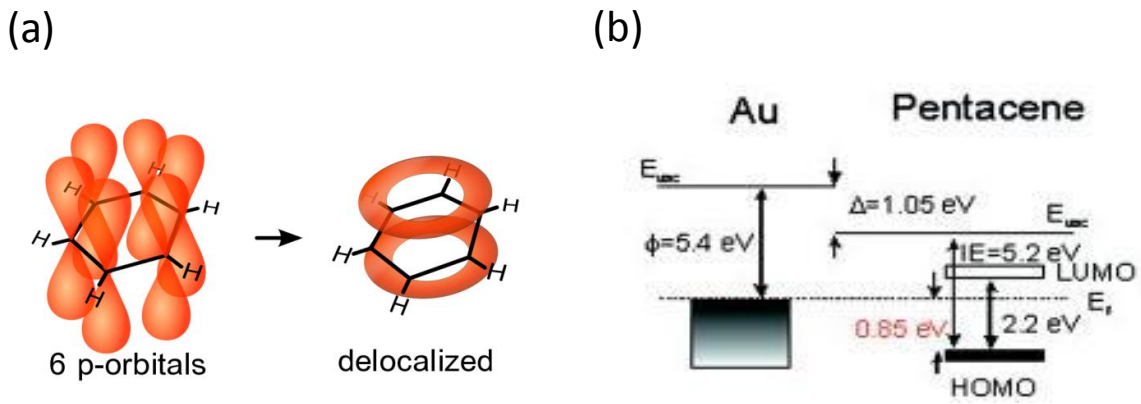

Figure 2.12 (a) Schematic illustration of the π-orbital hybridization in a benzene ring (b) Energy diagrams of interfaces formed between Au and pentacene [35].

The conduction mechanisms in organic semiconductors are commonly modeled by variable range hopping (VRH) [36] and multiple trap and release (MTR) [37]. While these models were originally developed to describe the carrier transport in amorphous silicon TFTs, the models are

found to be applicable to OTFTs due to the similarity of abundant trap states within the energy gap.

The VRH model assumes the bandgap is full of deep trap states, which prevent the conduction of carriers in the conduction band. As a result, the carriers transport through hopping in between the localized deep trap states. Conversely, the MTR model assumes that conduction in the delocalized band can still occur. However, due to the abundant trap states near the conduction band edge, carriers are periodically trapped and released. Both model suggest a field dependent mobility, based on the fact that higher gate bias causes the Fermi level to move closer to the conduction band edge, resulting in more trap filling and a more band-like transport. Additionally, both models suggest a temperature enhanced mobility, which is in contrast to the case of conventional silicon, where higher temperature causes the reduction of mobility due to phonon scattering. Here, higher temperature can enhance the hopping and trap-release processes such that the effective mobility is increased due to a higher current flow. These models are used to model the gate-bias dependent mobility in Appendix A.

The contact quality between the metal electrodes and the organic semiconductor has a significant impact on the carrier transport. A high contact barrier can result in poor injection of carriers, leading to low effective mobility. To minimize the contact barrier, metals with work function matching to the HOMO level of p-type organic semiconductors are commonly used. For the case of pentacene, gold is conventionally used as the S/D electrode material to form good contacts, as gold has a high work function of 5.4 eV. Ideally, the HOMO level of pentacene can align closely to the Fermi level of gold. However, the alignment of the Fermi level across the interface requires an electron charge transfer from the organic to the metal. The charge comes from the interface states, and the interface organo-metallic molecule can be ionized to form dipoles [35]. These dipoles result in an offset in the vacuum level between both sides as illustrated in Figure 2.12(b). As a result, a contact barrier exists for holes injecting from gold to pentacene. To solve this problem, organic mono-layers have been used to modify the S/D surfaces to reduce the contact barrier to enhance the charge injection [27]. Moreover, encapsulant of nanoparticles has been utilized to modify the formation of interface dipoles to improve the charge injection between printed S/D electrodes and organic semiconductors [38].

2.5.3. Basic operation and parameter extraction of OTFTs

OTFT operation is similar to the general principle of conventional field-effect transistors, where the channel carriers are induced in the channel by a gate bias. Unlike single crystal systems, in which the channels are typically turned on by inverting the semiconductor, OTFTs turn on by accumulating charge in the channel, as inversion is prohibited by the abundant mid-gap trap states. Due to a similar bias operation to general transistors, the output characteristics (I_{DS}-V_{DS}) of OTFTs exhibit a linear region, and also a saturation region due to pinch-off near the drain side (Figure 2.13). A contact barrier is often observed in OTFTs under low drain bias, as illustrated in Figure 2.13. This is due to the offset in vacuum levels as discussed in the previous section. The contact barrier can result in an under-estimation of extracted mobility at low drain bias. Therefore, the mobility is typically extracted in saturation region, i.e. at high drain bias. A conventional square-law saturation current equation is used in the extraction:

$$I_{DS} = \frac{W}{2L}\mu \cdot C_{OX}\left(V_{GS} - V_T\right)^2$$

where W, L, Cox have their typically meaning. As shown in the equation, the current in the saturation is independent of drain bias; therefore the mobility extraction is immune to the effect of contact barriers. The mobility is then extracted by plotting square root of I_{DS} versus V_{GS}; the slope of the curve extrapolated at high gate bias can thus be used to calculate mobility, given the information of W, L and Cox. The extraction at high gate bias is based on the fact that mobility is gate-bias dependent, as suggested by the MTR and VRH models; therefore the mobility extracted at high gate bias is conventionally used to compare among various OTFTs. The threshold voltage V_T is typically defined as the x-intercept of the tangent line extrapolated at high gate/drain bias of the $\sqrt{I_{DS}}$-V_{GS} curve. The extraction of V_T is purely empirical, as no clear definitions of channel turn-on is developed in the accumulation mode of OTFTs. On/off ratio and sub-threshold slope are typically extracted for comparison between OTFTs. On/off ratio is defined by the ratio of the maximum current divided by the minimum current observed in the transfer characteristics (I_{DS}-V_{GS}). Sub-threshold slope is defined at the maximum slope of the log(I_{DS})-V_{GS} curve, and the inverse slope with the unit of volt-per-decade (V/Dec) is reported.

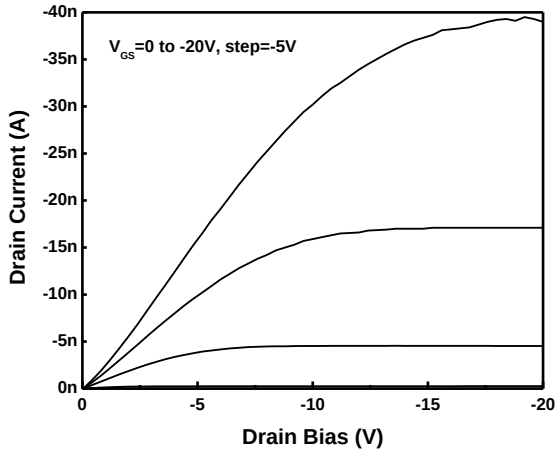

Figure 2.13 Output characteristic of an OTFT

2.6. Process integration of inkjetted transistors

Inkjet printing process of OTFTs with bottom-gate and bottom-contact structures will now be discussed, particularly with respect to the optimization of individual layers as well as the integration between layers. Printed OTFTs are composed of printed electrodes, insulators and semiconductors; therefore, the following discussions will be separated into three sections.

2.6.1. Printed electrodes

Printed electrodes are essential for OTFTs to form the gate and S/D. Various metallic printable inks consisting of dispersed metal nanoparticles have become commercially available. In this work, two types of silver inks were used: CCI-300 (Cabot Corporation), and SunJet-U5603 (SunChemical). While CCI-300 and U5603 contain identical silver nanoparticles, the ink formulations are slightly different. The detailed composition is proprietary in both cases, so the difference is unknown. Fortunately, these inks behave nearly identically in terms of their printability and conductivity. Both inks partially-wet on various substrates, including oxidized

silicon wafers, glass and Polyethylene naphthalate (PEN). No additional treatment on the surface is required to eliminate the coffee ring to print smooth, continuous lines [39]. Therefore, both inks were used extensively as a baseline throughout this thesis.

To obtain stable jetting, the viscosity needs to be adjusted to match the inkjet nozzle needs. The silver ink consists of silver nanoparticles with an average size of 80 nm. From the material safety datasheet (MSDS), the ink was found to have an alcohol-based solvent composition, as shown in the inset table of Figure 2.14(a). Therefore, water was conveniently used to adjust the ink viscosity, as the ink is completely water miscible. Figure 2.14(a) shows the silver ink viscosity as a function of the volume percent of water. The viscosity was measured by a Brookfield DV-III Ultra Rheometer at a shear stress of 10.32 pascal. The ink was clearly diluted by water and thus showed a lower viscosity at a higher water volume percent. Therefore the viscosity of the silver ink can be adjusted to the optimum jetting condition for a specific inkjet nozzle using the quasi-linear relation shown in Figure 2.14(a).

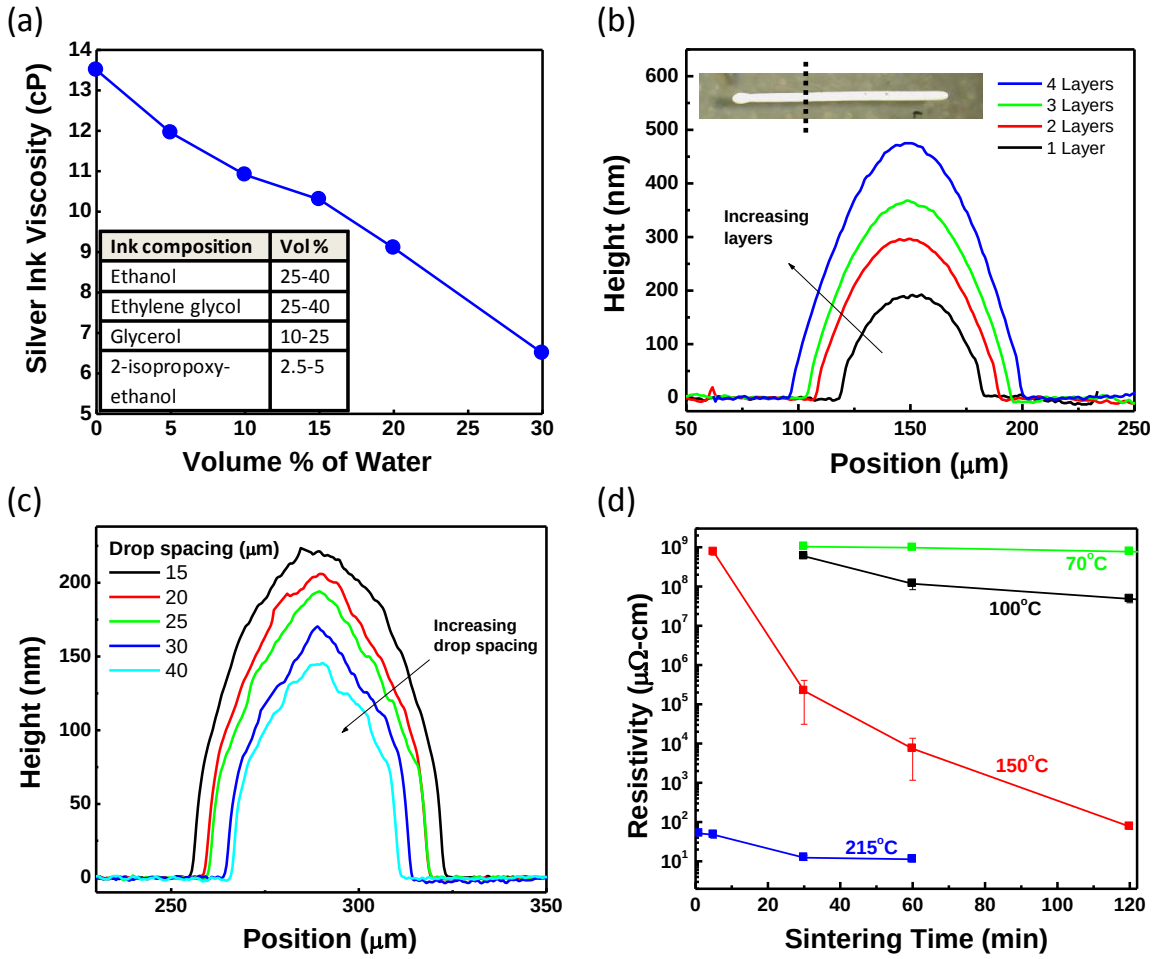

Figure 2.14 (a) Silver ink viscosity as a function of added water vol%. Inset table shows the composition of the silver ink U5603 from its MSDS (b) Cross-sectional view of the printed silver lines with various layers. The lines were printed with a drop spacing of 30 μm. (c) Cross-sectional view of the printed silver lines with various printed drop spacing (d) Printed silver resistivity as a function of sintering temperature and time.

The geometry of the printed gate electrodes is important, as it can affect the deposition of layers on top of the gate. Ideally, the bottom gate should be as thin as possible, such that the S/D and semiconductor can be deposited on a planar insulator to minimize the complication of electric field on a curve surface. The thickness of the printed silver can be controlled by the number of layers and the printing drop spacing, as shown in Figure 2.14(b) and (c) respectively. Printing another layer is equivalent to doubling the ink volume in a printed line, and can thus increase the thickness in a digital fashion. On the other hand, changing the drop spacing can alter the ink volume in a line continuously, resulting in a finer control of the line thickness. Due to a fixed equilibrium contact angle, the printed line width also increases with the thickness when more ink volume is deposited.

For gate electrodes, the conductivity requirements are lower than for S/D electrodes, as the voltage drop in the gate is minimal due to a negligible gate current. To optimize the conductivity of the electrodes, the sintering of the silver lines is then characterized. Here, resistivity was measured on printed lines with a length of 1 mm and a thickness of 180 nm using a four point probe method. Figure 2.14(d) shows the printed silver resistivity as a function of sintering temperature and time. After sintering for 10 minutes at 215 ℃, a lowest resistivity was obtained, corresponding to a conductivity of 6×10^6 S/m (10% of bulk silver conductivity). This conductivity is sufficiently for gate, drain and source electrodes of printed transistors, where the channel resistance is the limiting factor. For a plastic-substrate-compatible process, the sintering temperature needs to be lowered to ~150 ℃ or less. However, longer sintering time is required to gain an acceptable conductivity for the S/D electrodes.

For printing S/D electrodes, a precise alignment is required. However, the accuracy of the printer is insufficient to achieve an excellent alignment; instead, overlaps between gates to S/D are typically used to compensate the jetting deviation. Therefore, in Chap. 3, we will introduce a printing technique to achieve self-alignment between the gate and the S/D electrodes, in order to minimize the overlap capacitances.

2.6.2. Printed insulator

An optimum printed insulator should be uniform and conformal to the gate electrodes. Furthermore, a thinner dielectric is favorable in achieving a good electrostatic control of the gate. The PVP ink used in this work has a complete wetting behavior on a variety of substrates including silicon dioxide, glass and metal. As previously discussed, the printed PVP forms a large coffee ring as shown in the inset picture of Figure 2.15(b). Although the formation of coffee ring is generally unfavorable, the PVP is thinner at the center than edges after the solvent evaporated, resulting in a smooth and conformal layer on the gate electrode; as long as the coffee ring is formed outside of the active device area, the coffee ring is not a concern in this layer. Therefore the suppression of the PVP coffee ring was not performed in this work.

The thickness of the PVP can be controlled by both changing the printing drop spacing and ink concentration, as reported in previous work (Figure 2.15(a)[1], [40]). Larger drop spacing causes reduction in the amount of ink deposited per unit area and hence results in a reduction of the thickness. Similarly, a reduced concentration results in a thinner film by depositing less PVP materials. PVP with thickness as thin as 25 nm has been demonstrated by inkjet printing [40].

The uniformity of the printed PVP film can be improved by using multiple nozzles in Dimatix printer. Due to the relatively small drop volume in Dimatix nozzles, single nozzle

printing can result in a one-side-thicker film due to greater evaporation at the first contact line (top edge in a square, Figure 2.15(b)). As a result, a convective flow toward the first contact line occurs and carries the PVP to that edge, causing a thicker film at one edge. Conversely, printing with multiple nozzles causes more symmetrical evaporation at both contact lines, resulting in two balanced convective flows and hence a more uniform coffee ring and PVP in the center, as depicted in Figure 2.15(b).

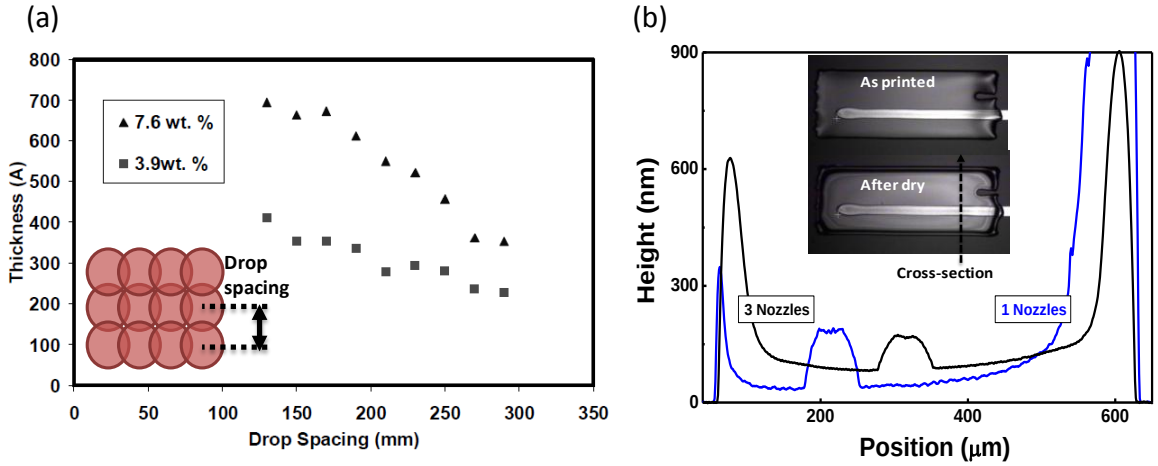

Figure 2.15 (a) Printed PVP thickness as a function of printing drop spacing. Two ink concentrations are shown. [40] (b) The profilometry of the printed PVP with one and three nozzles printing simultaneously. The inset shows the optical micrograph of a printed PVP layer with three nozzles printed at the same time.

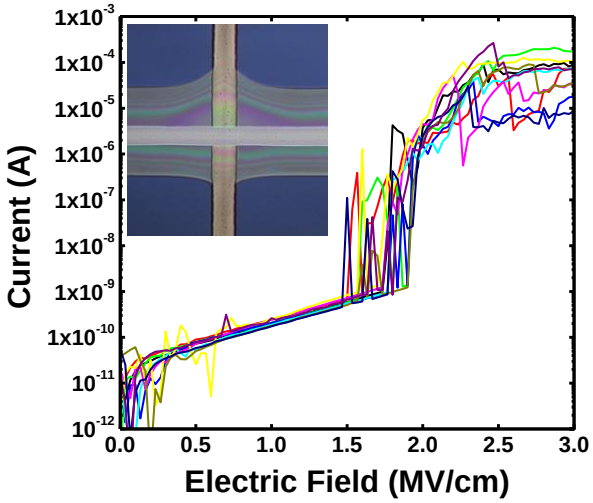

Figure 2.16 Typical leakage and breakdown curves of ten PVP capacitors with printed top and bottom silver electrodes. Inset shows the optical micrograph of the capacitor.

A cross-bar capacitor consisting of a printed PVP layer sandwiched by two printed silver electrodes (inset optical micrograph of Figure 2.16) is typically used to characterize the quality of the printed insulator, e.g. breakdown field. Figure 2.16 shows the typical leakage current of 10

printed capacitors. The breakdown field is defined at the abrupt increase of leakage current. PVP shows a typically breakdown field of 1.5-2 MV/cm with printed silver lines as bottom electrodes. The breakdown field can be improved by using bottom electrodes with smoother surface roughness. The average roughness of the printed silver surface is ~15 nm, limiting by the relatively large nanoparticle size. The roughness can be potentially improved by using a metallic ink with smaller nanoparticle sizes (this will be discussed in Chap. 5). The impact of subsequent surface treatment on the breakdown field will be discussed in the following paragraph.

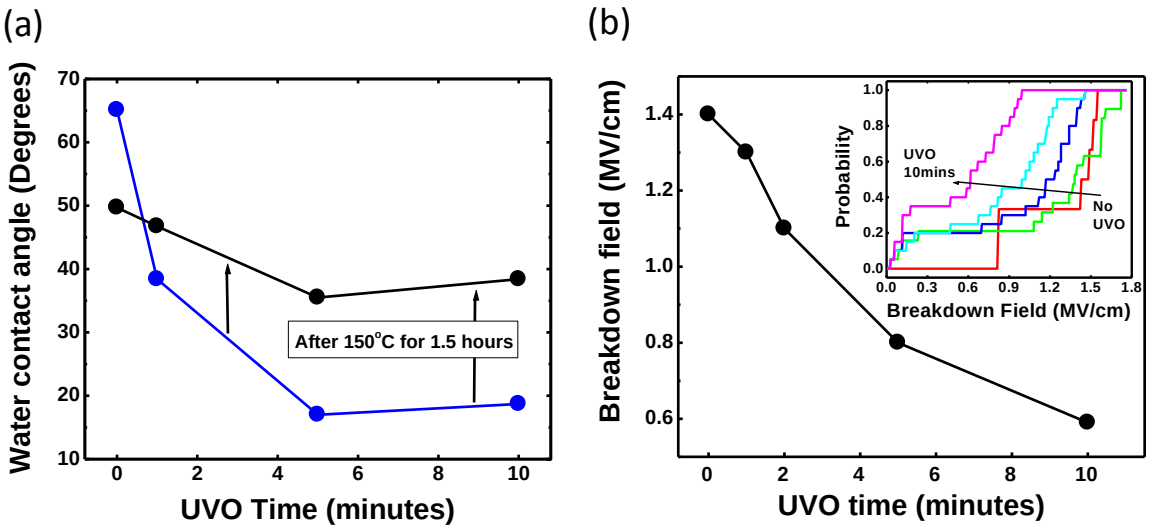

Figure 2.17 (a) Water contact angle on PVP as a function of UVO exposure time (b) Breakdown field as a function of UVO exposure time on the PVP. Inset shows the cumulative plot of the PVP breakdown with various UVO time (Courtesy of Gerd Grau).

A surface treatment is often necessary to control the wetting behavior of the subsequent printed layers. A layer of crosslinked PVP showed an intermediate hydrophobic surface with a water contact angle in the range of 50-60 degrees, thus requiring a hydrophilic treatment to promote the wetting of aqueous inks. UV-ozone (UVO) exposure is a well-known method to render the surface more hydrophilic. Figure 2.17(a) shows that the water contact angle can be reduced significantly by exposing the film of PVP to UVO. The reduction saturates at 5 minutes exposure, indicating that the surface of the PVP has been fully oxidized after 5 minutes of treatment. Interestingly, the surface energy can be recovered by subsequently heating the film to 150 ℃ for 1.5 hours, as shown in Figure 2.17(a). While the temperature is not high enough to re-crosslink the PVP that might have been damaged by the UV energy, the recovery of the surface energy is mostly likely due to the hydroxyl group loosely attached to the PVP surface being driven off by the heat. The evidence of PVP being damaged by the UVO is shown in Figure 2.17(b). The representative breakdown field extracted at the knee of the cumulative plots was significantly reduced by the UVO exposure. Reduction of the breakdown field implies that the PVP film became less cross-linked. In contrast to the surface energy which saturated after 5 minutes of UVO treatment, the breakdown field continued to degrade with after 5 minutes. This supports the fact that the cross-linking of PVP was internally damaged by the UV energy. To conclude, excess UVO exposure on PVP is detrimental to its dielectric breakdown, and therefore optimizing exposure time is necessary.

To achieve high mobility in organic semiconductors, a hydrophobic surface is reported to improve the molecular packing [41]. To enhance the PVP surface hydrophobicity, monolayers such as octadecyltrichlorosilane (OTS) and hexamethyldisilazane (HMDS) have been reported to self-assemble on the PVP surface [18]. The increase of water contact angle implies that OTS or HMDS can attached to the hydroxyl group on the PVP surface.

2.6.3. Printed semiconductor

Printing semiconductor is the last step in the transistor processes. As previously mentioned, the PVP surface is often treated with a monolayer to improve the performance of semiconductor. However, the treatment can significantly change the wetting of the semiconductor inks on PVP and silver S/D, affecting the coverage of the channel surface. Therefore, optimization of the surface treatment for achieving both high mobility and good wetting behavior will be discussed in this section.

2.6.3.1. Printing pentacene precursor

To print pentacene precursor, 1.5 wt% of pentacene precursor (purchased from Sigma Aldrich, anhydrous 99.7%) dissolved in anisole was used as the baseline ink. Anisole was selected due to its high boiling point (150 ℃) that can minimize the evaporation and the nozzle clogging. The printing of pentacene precursor was done with Microfab nozzles.

The substrate was typically treated with HMDS prior to the inkjetting of pentacene to improve the mobility as previously mentioned. The HMDS treatment renders the surface of both PVP and silver more hydrophobic (will be discussed further later). As a result, the hydrophobic anisole ink shows a complete wetting behavior on both PVP and silver, resulting in a uniform coverage of the channel. However, similar to the printed PVP film, the printed pentacene film showed a coffee ring, as illustrated in the inset of Figure 2.18(b), where excess pentacene can be observed at the edges of the printed layer. This resulted in two relatively thick (and thus more conductive) regions at the both ends of the channel. Consequently, a transfer characteristic with two early turn-on parasitic transistors can be observed at a low drain bias, as seen in Figure 2.18. This is unfavorable, as the increased off-state leakage current can deteriorate the signal integrity in LCD and circuit applications. A co-solvent system used to eliminate the coffee ring effect will be discussed later.

The printed pentacene precursor was annealed at 150 ℃ for 25 minutes in a nitrogen glovebox to convert back to pentacene. A high mobility of 0.1 cm^2/Vs has been demonstrated with the combination of inkjet printed pentacene and PVP in previous work [1]. However, the mobility obtained in this work was significantly lower, due to the use of silver source and drain electrodes instead of the gold electrodes used previously. The work function mismatch between pentacene and silver can result in a contact barrier that limits the charge injection, as previously suggested. The contact barrier can be mitigated by a surface treatment on S/D, which will be discussed in the next section.

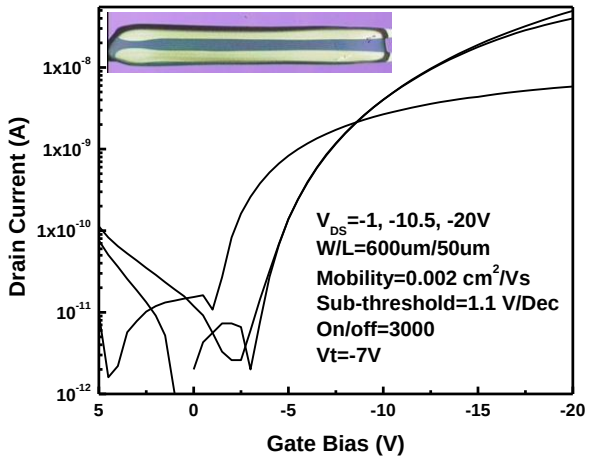

Figure 2.18 Transfer characteristic of the inkjet-printed pentacene transistor. Inset shows an optical micrograph of the transistor with a printed pentacene, printed silver S/D, spin-coat PVP and a heavily doped silicon wafer as a planar back gate

2.6.3.2. Printing TIPS-based pentacene

In our baseline printing, TIPS-CFP was used due to its superior stability in solvents versus TIPS pentacene [29]. To inkjet-print, 1 wt% of TIPS-CFP dissolved in dichlorobenzene was used as the solvent. The printing was performed using a Microfab nozzle in our custom-built printer. TIPS-CFP was then printed on the bottom-gate and bottom-contact structures for optimizing both the wetting and mobility. The S/D electrodes were prepared by inkjet printing sliver ink on the printed PVP. Silicon wafer was used as a back gate.

Due to the hydrophobicity of dichlorobenzene, printed drops on S/D and PVP surfaces showed various wetting behaviors with different surface treatment, as summarized in Figure 2.19. Non-treated silver S/D and PVP show hydrophilic and hydrophobic surface respectively. The hydrophilicity of the silver surface can be explained by the presence of the hydroxyl group on the nanoparticle encapsulant to promote its dispersion in the alcohol-based solvent. As a result, TIPS-CFP drops prefer to wet on PVP than on silver. This is unfavorable, as the minimal contact area between TIPC-CFP and silver can cause severe contact resistance. On the contrary, if the S/D and PVP were both treated by UVO, TIPS-CFP drops prefer to wet on S/D than PVP, as the S/D becomes hydrophobic and PVP becomes hydrophilic. The hydrophobic silver S/D after the UVO treatment can be explained as the encapsulant residues being removed by the treatment; therefore a native silver surface energy was obtained. If the S/D and PVP were both treated with HMDS, the surface become similarly hydrophobic, hence a TIPS-CFP drop can wet uniformly on the S/D and PVP, consistent with the case seen in the pentacene precursor as discussed previously. Finally, PFBT (pentafluorobenzenethiol) has been reported to improve the carrier-injection at the S/D-TIPSCFP interface [27]. If both surfaces are treated with PFBT (pentafluorobenzenethiol), the silver become more hydrophobic than PVP. This is due to a better interaction between sulfur and silver, causing better bonding between PFBT and silver. The printed TIPS-CFP drop can dewet from the silver S/D slightly, due to the high hydrophobicity of fluorine atoms on PFBT. Nevertheless, the highest mobility can be achieved using the PFBT treatment, due to an optimized S/D contact.

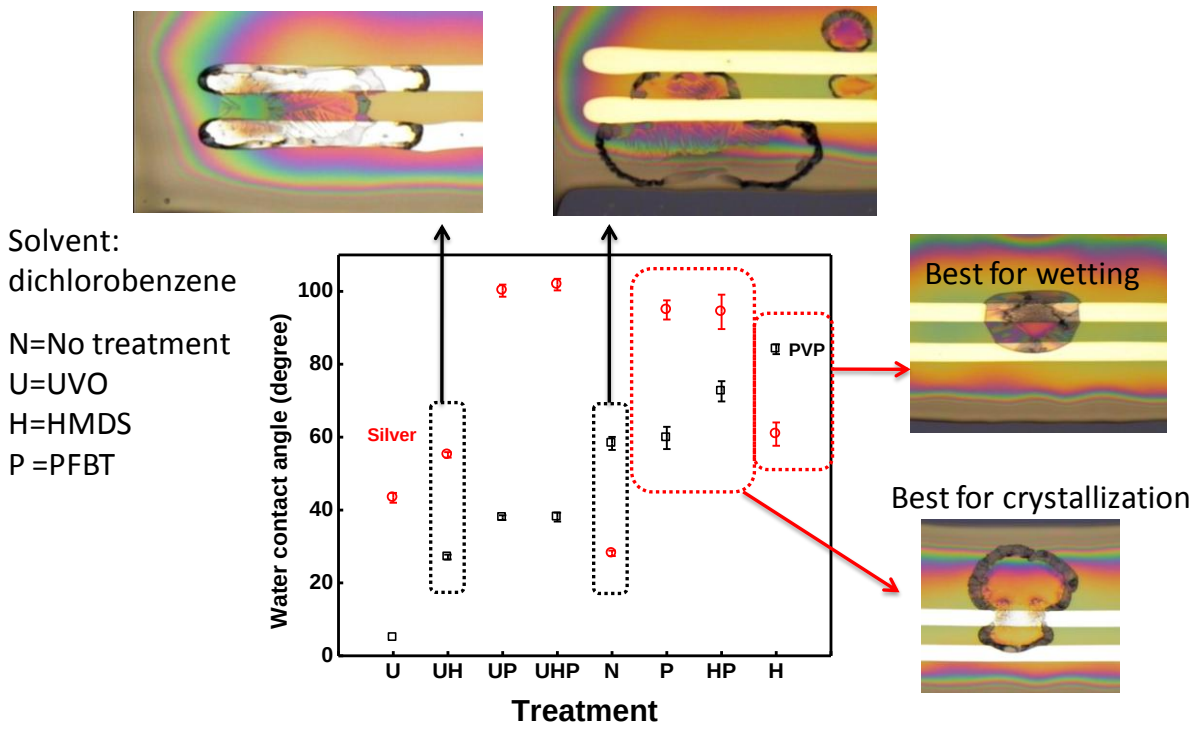

Figure 2.19 Water contact angle on silver and PVP with various surface treatment. The optical micrographs show the TIPS pentacene printed with dichlorobenzene on various treated surfaces.

The mobility versus various surface treatments was then compared. The results are categorized based on surface cleaning, PVP surface treatment and S/D treatment. For the cleaning step, N and U denote no-treatment and UVO treatment respectively. For PVP surface treatment, H and N denote HMDS and no-treatment respectively. For S/D treatment, N and P denote no-treatment and PFBT treatment respectively. The mobility was extracted by measuring the transistor transfer characteristics. Although HMDS treatment can achieve the most uniformity drop wetting as previously indicated, the resulting mobility is low, as shown in Figure 2.20. On the other hand, PFBT treatment can enhance the mobility independent of whether the HMDS or UVO treatment was performed, indicating the treatment on S/D is crucial.

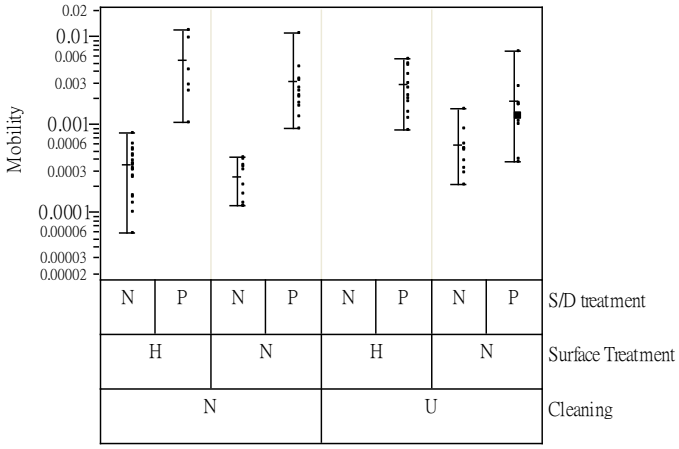

Figure 2.20 Variability chart of the mobility on various treated S/D and PVP surfaces.

The highest mobility obtained was 0.01 cm^2/Vs, significantly lower than the previous report [27]. This was later diagnosed to be caused by inaccuracy in channel width extraction. Due to the coffee ring effect observed in Figure 2.19, TIPS-CFP was only deposited at the periphery of the drop. Therefore, including the drop-center into the channel width extraction results in 7-8 times lower mobility. Therefore, the coffee ring can cause difficulty in controlling the channel width. A co-solvent system was then utilized to mitigate the coffee ring issue. A solvent mixture of dichlorobenzene:dodecane (3:1 vol. ratio) was reported to eliminate the coffee ring by introducing a reverse Marangoni flow [42]. 1 wt% of TIPC-CFP dissolved in dichlorobenzene:dodecane was then used for baseline inkjet printing. Using this solvent, the printed drop exhibits a coffee-ring-free behavior. However, the drop had difficulty in pinning on the S/D and PVP surfaces, i.e. a drop landing on the S/D and PVP could randomly move to other positions. The de-pinning can be explained by the dewetting of dodecane on the partially dried TIPS-CFP surface. Although the de-pinning phenomenon was not fully understood, the drop position can be temporarily controlled by heating the substrate to 60 ℃ while printing. The heated substrate can accelerate the solvent evaporation and inhibit the drop movement. Transistors with inkjet printed TIPS-CFP will be demonstrated and discussed in Chap. 4 and 5.

2.7. Summary

In this chapter, components required for inkjetting organic transistors were comprehensively reviewed and discussed. Inkjet technologies including thermal-bubbles jets, piezoelectric jets and electrohydrodynamic jets were reviewed. The piezoelectric jet is the most promising candidate for inkjetting materials used for printed electronics. Dimatix and custom-built inkjet printers utilizing the piezoelectric nozzles were introduced along with a detailed explanation of their jetting operation. The custom-built printer discussed herein will be used as a platform for demonstrating a novel print-and-drag technique in Chap. 4. Basics of electronic inks and the ink-surface interaction were then reviewed. Important wetting phenomena such as the so-called coffee ring along with their impact on film formation of insulators and semiconductors were discussed. The methods used to suppress coffee ring in printing semiconductors were also reviewed in this context. Operation principles of OTFTs were reviewed to provide the basic information for readers. Methods used to extract parameters of OTFTs throughout this thesis were then introduced. Finally, the inkjetting processes used to fabricate a bottom-gate and

bottom-contact OTFT were discussed from the standpoint of process integration. Inkjetting parameters were optimized to achieve good printed gate electrodes and insulators. The optimization will also be applied to realize a self-aligned printing in Chap. 3. Optimization of surface treatment was executed in order to print a uniform semiconductor layer with desired wetting characteristics. In sum, the conceptual basis, understanding and optimization provided in this chapter is essential to the remaining chapters in this thesis.

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Chapter 3 All Inkjet-Printed, Fully Self-Aligned Transistors

3.1. Introduction

Printing techniques were traditionally employed to print content for human reading. Any object below 100 µm is hardly visible to unaided human eyes. This has made the down-scaling of conventional printing resolution below 100 µm unnecessary. Consequently, the resolution of conventional printing techniques remained coarse for printing electronics devices. Although there have been demonstrations of all printed passive devices [1], [2] and active transistors [3] by using state-of-the-art printing technique such as inkjet [4], rotogravure [5] and offset printing [6], the printed transistors typically suffer from large channel length and very high overlap capacitance [7–9], limited by the coarse resolution of the printer. To overcome the limitation, printed transistors have been demonstrated with channel length below 1 µm by using a self-aligned printing technique to realize feature separation and definition in individual layers [10–12]. However, the poor layer-to-layer registration of printing techniques remains a tremendous bottleneck in printed devices. While some efforts have been made to realize self-aligned registration, these have necessitated the use of lithographic techniques [12–14], which are not cost-effective. Furthermore, the use of lithography processing could potentially damage the organic materials during the back side exposure and photoresist developing processes.

Given this need, in this chapter, we demonstrated the self-alignment of the source and drain (S/D) to the gate of fully-printed organic transistors using wetting-based roll-off techniques [15]. Using such techniques, we demonstrated fully self-aligned transistors and circuit elements in an all inkjet-printed process, without the need for any lithography or vacuum processing. We achieved a minimum overlap of 0.47 µm between the gate and S/D, contrasted to the >10 µm typically required in conventional printed transistors [14], resulting in overlap capacitance as low as 0.14–0.23 pF mm^{-1}. As a result, the speed of the printed transistor is significantly enhanced since the overlap capacitances are minimized. We further extend this technique to demonstrate self-alignment across circuits consisting of multiple devices, including formation of transistors, interconnects, and vias.

3.2. Speed limitations of printed transistors

As discussed in Chap. 2, jetting accuracy is often degraded due to the angular jetting deviation of typical inkjet printers, resulting in a ±10 µm variation of drop positioning [14]. Although this variation can be slightly mitigated by reducing the distance between nozzles and substrates, the design rules for printed transistors still require a large gate-linewidth and large gate-to-S/D overlaps to avoid the shorting of the source and drain electrodes, and also to avoid underlaps between the gate and S/D, respectively. The resulting large dimensions can significantly degrade the speed of the transistors. Figure 3.1(a) illustrates the definition of channel length L and gate-to-S/D overlap L_{OV} (assuming the overlaps are symmetric for simplicity), and their impact on the cut-off frequency f_T. As indicated in the equation in Figure 3.1(a), f_T can be clearly reduced by large dimensions, as f_T is inversely proportional to L and L_{OV}. By inserting a typical V_{DD} of 20 V and a typical mobility of 0.2 cm^2/Vs into the equation, the relation between f_T and L and L_{OV} can be plotted in Figure 3.1(b). Clearly, the speed can be dramatically enhanced by reducing the dimensions. Mega-Hertz operation is achievable by reducing the L_{OV} under 1 µm and shrinking L to the single micron range. Therefore in the following sections, we will

demonstrate the use of novel self-alignment techniques to achieve a gate-to-S/D overlap below 1 µm. The shrinking of L will then be discussed in the next chapter.

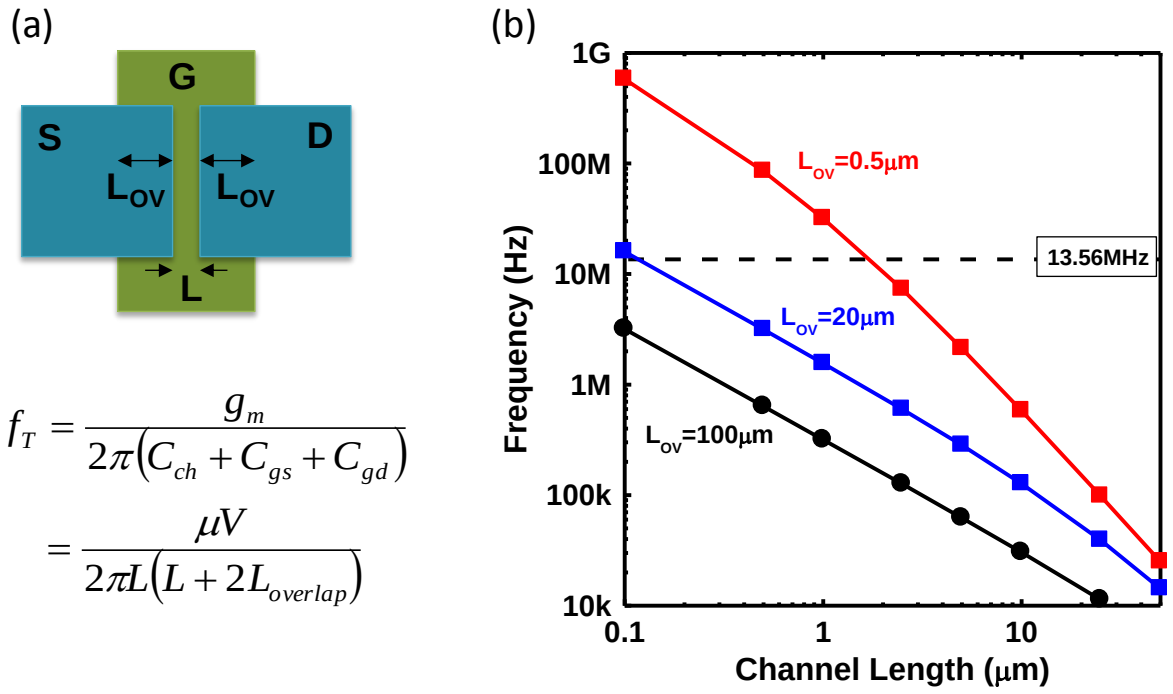

Figure 3.1 (a) Schematic illustration of channel length L and gate-to-S/D overlap L_{OV}. Equation of the cut-off frequency f_T is also shown. (b) Cut-off frequency as a function of L and L_{OV}.

3.3. Inkjet printing process for transistors

Figure 3.2 shows the complete process flow of an inkjet printed transistor. An N-type silicon wafer with thermally grown oxide of 100 nm was used as underlying mechanical substrate. Silver nanoparticle ink (Suntronic U5603) was printed as a gate electrode with a drop spacing of 30 µm, and subsequently sintered at 200 ℃ for 10 minutes. Baseline PVP ink was printed atop the gate and cross-linked at 200 ℃ for 10 minutes. Five nozzles were used simultaneously to print the PVP layer with a drop spacing of 30 µm, resulting in a dielectric thickness of 110 nm. Silver ink was then printed to form source and drain electrodes with a drop spacing of 20 µm. This was followed by a sintering step identical to that used for the gate electrode. The PVP surface was then treated with hexamethyldisilazane (HMDS) vapor to obtain a low energy channel-surface with a water contact angle of 66°. Finally, baseline pentacene precursor ink was printed as a p-type semiconductor. The precursor was annealed at 150 ℃ in a nitrogen ambient with a 10 ppm oxygen level. All inkjetting was performed using a Dimatix DMP-2800 printer and a jetting frequency of 2 kHz was used at all times.

While the peak-process temperature was 200 ℃, primarily set by the high-temperature annealing step of PVP, the process will be applicable to sub-150 ℃ processing as well, as required for polyethylene terephthalate (PET) substrates, by using lower temperature sintering dielectrics, which have been developed recently [16]. In addition, PVP has also been

demonstrated to work with a cross-linker that requires much lower cross-link temperature at 130-150 ℃ [17]. Therefore, the overall process temperature is expected to be reduced in the future.

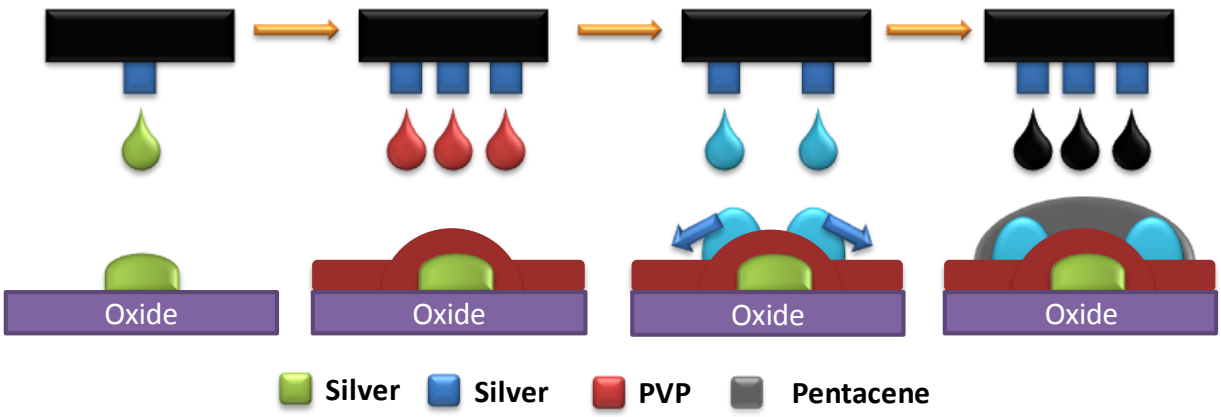

Figure 3.2 Inkjet transistor process, consisting of four layers of printing.

3.4. Self-Alignment

The general concept of wetting-based self-alignment was first introduced by H. Sirringhaus et al. [4], [18] and applied to the formation of narrow-gap source-drain structures. In their work, the authors started with a lithographically patterned spacer as a hydrophobic mesa structure. A conducting polymer poly-(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (PEDOT/PSS) was then inkjet printed on the mesa structure. The hydrophilic PEDOT/PSS then dewetted the mesa structure and self-aligned the spacer to form S/D electrodes. The transistor was then completed by spin-coating of semiconductor, dielectric, and inkjet-printed top gate. Here, we apply the concept of wetting-based self-alignment to solve the critical issue of layer-to-layer alignment. We inkjet-printed silver as a bottom gate, followed by a PVP insulator, thus forming a mesa structure. A surface energy contrast was serendipitously discovered during the printing of silver top electrodes to form cross-bar capacitors. Some portion of the printed silver dewetted and rolled off the mesa structure. However, this dewetting was not consistent, indicating an optimization was required to facilitate the roll-off and to achieve consistent self-alignment. The optimization was executed by firstly analyzing of the interfacial tension on the drop/mesa interface. Figure 3.3(a) illustrates the interfacial tension components of a source or drain drop on the side slope or the mesa-like structure of a printed transistor. Note the hydrostatic pressure was neglected, due to a small drop volume of 10 pL [19]. By Young's relation, the equilibrium of the drop is maintained by balancing the silver ink surface tension γ, PVP surface energy γ_{SO} and a liquid-solid interaction γ_{SL}. To maximize roll-off, it is therefore desirable to decrease γ_{SO}; unfortunately, the printed silver line integrity is often degraded if the surface energy becomes too low, as the printed line can break into separate droplets. Therefore, to facilitate the roll-off of the printed S/D, we have optimized the inkjet process to achieve roll-off without degrading line morphology by (i) increasing the silver ink surface tension (ii) optimizing the PVP thickness, and (iii) increasing the step height.

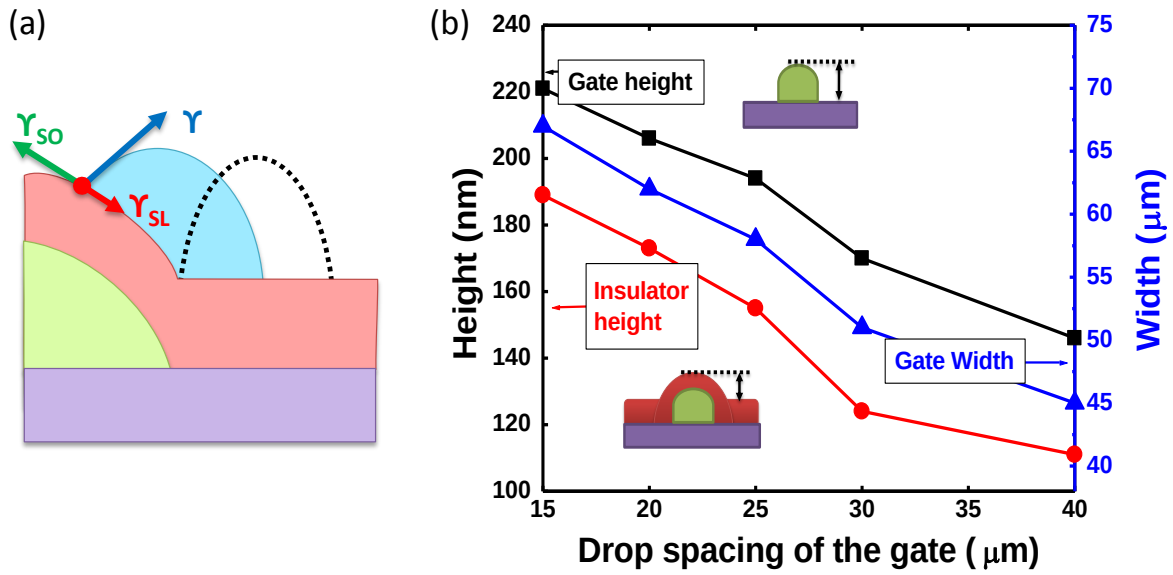

Figure 3.3 (a) Diagram showing the interfacial tension of a printed source or drain on the mesa structure. (b) Gate height, insulator height or mesa thickness and gate linewidth as a function of printed drop spacing of the gate.

The silver ink has a surface tension of 30 dyn cm^{-1}. Recalled from chapter 2, the viscosity can be adjusted by adding a portion of water, as the ink is water miscible. In addition, water has a high surface tension of 70 dyn cm^{-1}, and is therefore the best additive to increase the overall surface tension. However, adding water reduces the ink viscosity and results in a degraded jetting stability, as discussed in chapter 2. Therefore, an upper bound of 15 vol% water was then added into the silver ink while maintaining the optimum viscosity of 10 cP in this work. The step height of the mesa structure was naturally created by printing PVP atop the bottom gate. As discussed in chapter 2, printed PVP film formed a big coffee ring after the solvent evaporated, resulting in a conformal coverage of the bottom gate and a mesa-like structure. As indicated by previous work [18], a thicker mesa structure promotes dewetting. However, thicker dielectrics degrade device performance due to poorer gate capacitive coupling. Therefore, the PVP gate dielectric was kept as thin as possible to preserve the mesa geometry while maintaining good dielectric properties and device electrostatic integrity. Here, 110 nm of PVP was printed. The mesa structure was thickened by increasing the gate height, achieved by reducing the printing drop spacing of the gate. Reducing drop spacing increases the deposited drop volume, resulting in a thicker gate profile. Figure 3.3(b) shows the mesa structure thickening monotonically with increasing gate height due to the conformality of PVP. However, as indicated in Figure 3.3(b), line width also increases with step height, resulting in a slightly larger channel length. In order to obtain optimized dewetting without compromising the device speed through increased channel length, the gate line of 50 μm was printed by a 30 μm drop spacing throughout this work.

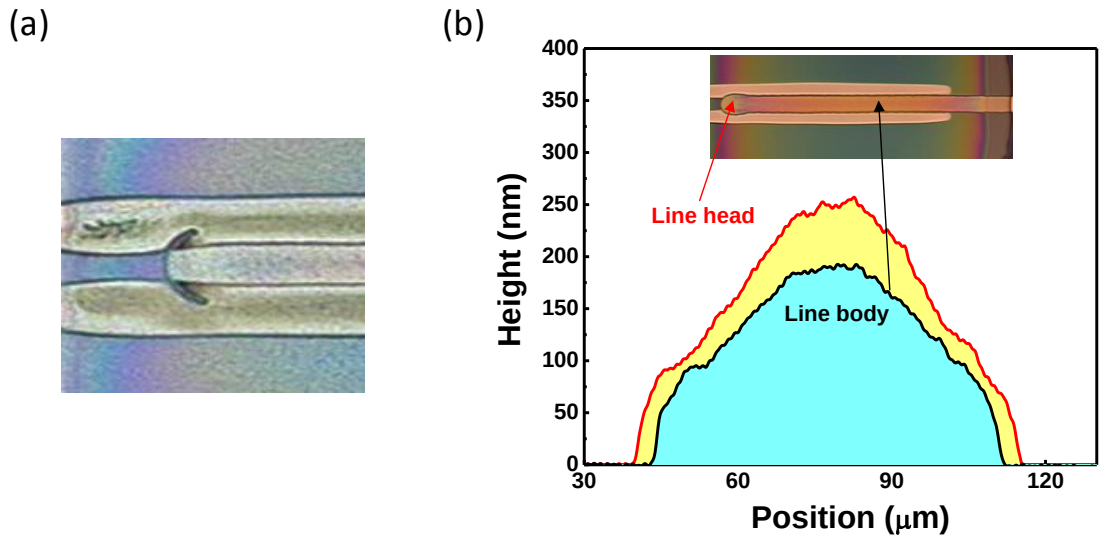

Figure 3.4 (a) Optical micrograph capturing the initial location of the dewetting. (b) Profilomery of a printed line head and body, and the corresponding location shown in the inset.

With the optimization, the printed S/D overlaps the gate initially and starts to dewet gradually with time. Interestingly, the dewetting mostly initiates at the head of the printed gate line. As shown in Figure 3.4(a), the printed S/D was sintered immediately after the dewetting initiated, in order to freeze the S/D pattern. Initial dewetting was clearly observed at the line head. This can be rationalized by the thicker mesa structure at the line head, originated from a larger drop volume. Figure 3.4(b) shows the profilometry measured by Alpha-Step IQ (ASIQ) Surface Profiler, illustrating that the printed line head is thicker and wider than the line body. Similar results showing a larger line head have been reported and modeled in detail in a previous work [20]. As a result, it is energetically favorable for the S/D to dewet starting at the head.

Figure 3.5(a) shows the optical micrographs of three post-S/D-sinter transistors, with different waiting time between printing and sintering. If sintered immediately after printing, the S/D remained overlapped over the gate; if 9 minutes of waiting are followed by sintering, the S/D partially dewets the gate. After 15 minutes, the S/D completely dewets and self-aligns to the gate. The overlap between the S/D and the gate was characterized using profilometry. Figure 3.5(b) shows the cross-sectional profile of a printed transistor, depicted by superimposing two ASIQ scans perpendicular to the printed lines, i.e. a first scan across the gate electrode only and a second scan across the S/D electrodes with insulator and gate below. The overlap between S/D and gate was then determined by the horizontal offset from the edges of three electrodes. The relation between overlap length and the waiting time is shown in Figure 3.5(c). A reduction of the S/D-to-gate overlap was clearly observed with increasing waiting time. A minimum overlap of 0.47 μm was achieved, in contrast to typical overlap of >10 μm in a printed devices. Note the measured overlap is somewhat scattered after 9 minutes of waiting time, due to the variation of ASIQ scan position. Therefore, to demonstrate the overall improvement by self-alignment, overlap capacitance was measured. An Agilent 4285A was used to measure capacitance. A small signal of 100 mV and 75 kHz was used as the input. Two co-axial probes connect to the 4285A were connected to the gate and drain electrodes respectively. Before the measurement, calibration was performed to cancel out the parasitic components resulting from the cable and oxide substrate. The measurement was then performed on five to ten different devices and

statistically consistent results were obtained. The measured capacitance was then normalized by channel width.

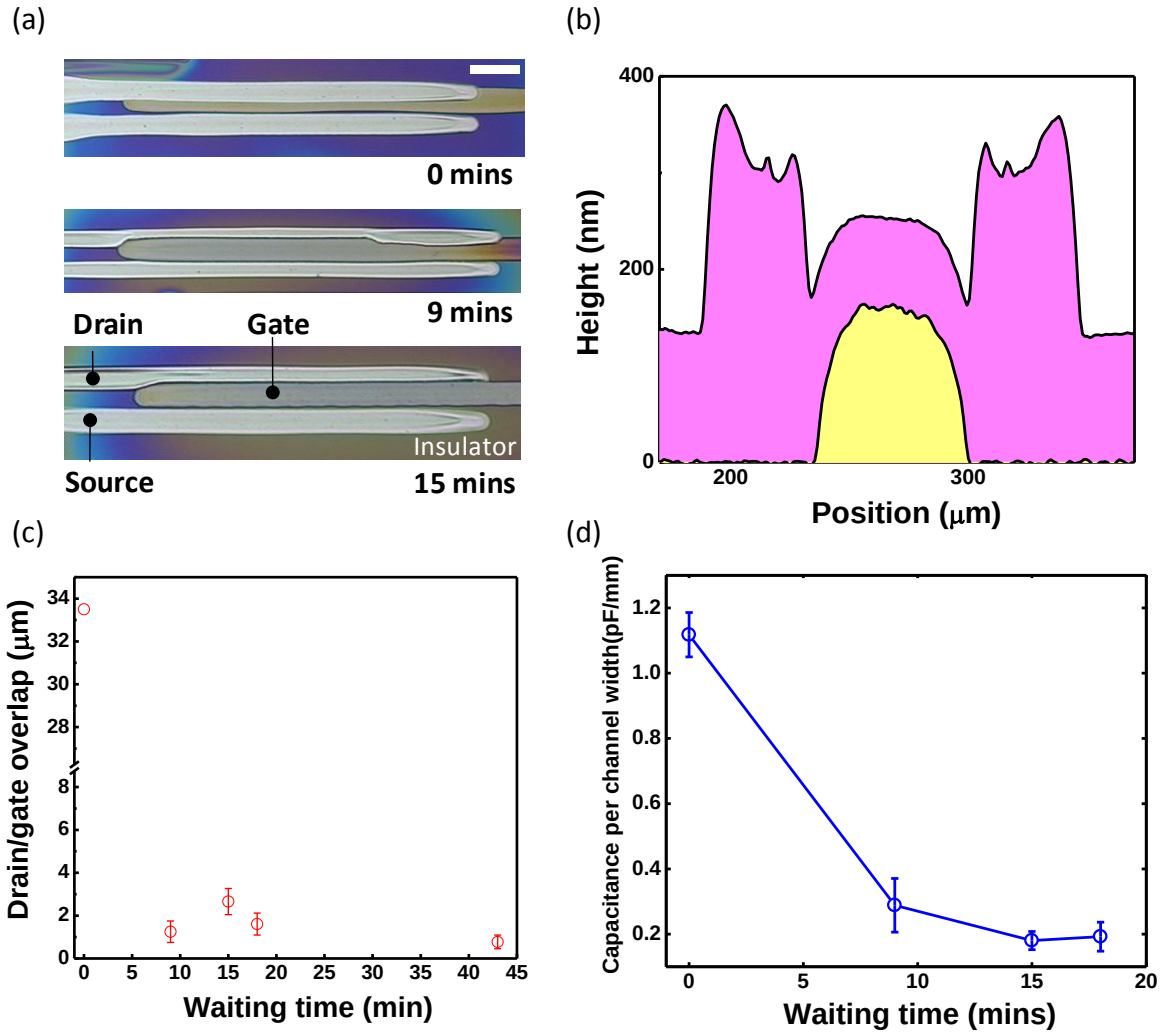

Figure 3.5 (a) Optical micrographs of three post-S/D-sinter transistors, with three different waiting time between printing and sintering. The scale bars represent 100 μm. (b) Profilometry of a printed transistor (c) S/D to gate overlap length versus drying time. (d) Measured overlap capacitance per channel width as a function of waiting time between printing and sintering.

As shown in Figure 3.5(d), the overlap capacitance reduced with increasing waiting time and saturated after 15 minutes, matching the observation from Figure 3.5(a). An average overlap capacitance as low as 0.185 pF mm^{-1} with a standard deviation of 0.031 pF mm^{-1} was achieved purely by printing, substantially surpassing the previous results obtained by a lithography-reliant and semi-printing process [12].

The general mechanism of self-alignment is related to the drop roll-off from the gate, followed by pinning at the gate corner. There are several candidate physical phenomena that govern the rolling-off behavior (1) The force gravity of the drop causes the S/D to minimize the potential energy by moving down the mesa structure. However, a calculation of the gravitational force from the volume and density of the ink indicates that the force is merely 5.9 x 10^{-7} dyn cm^{-1},

which is negligible comparing to the ink surface tension and PVP surface energy. (2) The surface energy of PVP could be locally reduced due to its interactions with the underlying gate line, causing the S/D drop to minimize the energy by migrating to a much higher energy surface. This can be made possible by the encapsulant of the silver nanoparticle diffusing up to the surface of PVP. However, we have found no specific evidence showing that the underlying gate alters the chemical structure of the PVP yet, though this effect is a subject of current investigation. (3) The geometry of the corner of the mesa structure could induce a capillary force to locally break the S/D drop into two parts [21]. Subsequently, the ink located on the channel surface contracts upon evaporation, while the ink at the side of the mesa structure remained pinned. While this appears likely, and is consistent with time-resolved optical micrographs of the self-alignment process, it is possible that the actual self-alignment is in fact a combination of these effects. More study and the proposed mechanism of the self-alignment will be discussed in Chap. 5. Overall, however, the self-aligned process is repeatable over more than 6 months of device printing.

3.5. Transistors characteristics

Figure 3.6(a) and (b) show the transfer and output characteristics of a printed self-aligned transistor with a channel width and length of 600 µm and 50 µm respectively. An Agilent 4156C semiconductor parameter analyzer was used to measure the transfer and output characteristics of the printed transistor and the voltage transfer characteristics of the printed inverter. The mobility was extracted from slope of the square-rooted drain current at a drain voltage of 40 V, and the threshold voltage was extracted from the x-intercept of the same fitting line. In contrast to the results shown in chapter 2, the transistor shows an output characteristic without a contact barrier, implying an ohmic contact formed between the pentacene precursor-based channel and the silver electrodes. This can be explained by a possible adjustment of the silver work function through an interfacial dipole, as previously reported [22]. Therefore the mobility obtained was slightly higher than the one in chapter 2, due to an enhanced carrier injection from S/D. The average value of mobility, on/off ratio, threshold voltage and sub-threshold swing are 0.01 $cm^2\ V^{-1}\ s^{-1}$,1440, -1.5 V and 4.28 V $decade^{-1}$ respectively. The statistical data is listed in

Table 3.1. The degraded mobility, on/off ratio and the sub-threshold swing are likely caused by the annealing temperature of pentacene precursor (150 ℃), approaching the glass transition temperature of PVP (170 ℃), resulting in degraded dielectric interfacial quality [23]. This can be potentially improved by using state-of-the-art inkjet printable organic semiconductor materials requiring low annealing temperatures, such as 6,13-bis(triisopropyl-silylethynyl) (TIPS) pentacene which has been demonstrated to offer high mobility and low sub-threshold swing on PVP dielectrics [9], [24], [25].

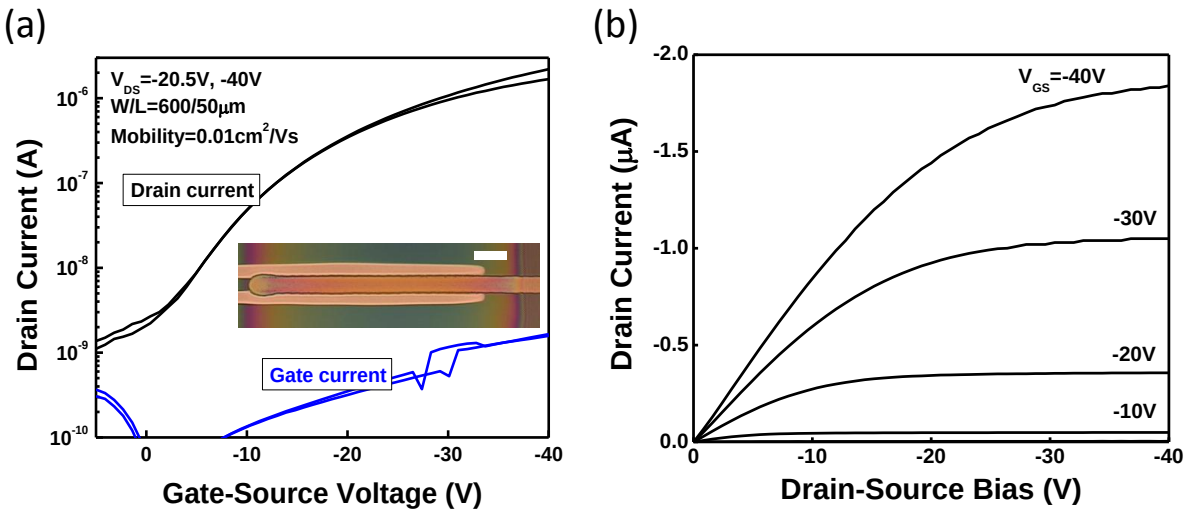

Figure 3.6 (a) Transfer characteristics of the printed self-aligned transistor. Inset shows the optical micrograph of the printed transistor. Top layer of printed pentacene was neglected for the clarity of the self-alignment. (b) Output characteristics of the printed self-aligned transistor.

	Mobility	On/Off ratio	Threshold voltage	Sub-threshold swing	W	L
Unit	$cm^2 V^{-1} s^{-1}$	-	V	V $decade^{-1}$	μm	μm
Average	0.01	1440	-1.5	4.28	612.33	51.36
Standard deviation	0.0015	352	1.0	1.44	7.98	1.95

Table 3.1 Statistical data calculated from several printed transistors. The results are obtained from 20 measured transistors.

Another possible explanation for the degraded mobility is the residue on the channel surface. To verify, atomic force microscopy (AFM) was used to characterize the surface morphology of the PVP. Figure 3.7(a) shows two transistors with S/D printed by a self-split technique (will be discussed shortly after). AFM image of PVP surface near the channel area is shown Figure 3.7(b), illustrating a clean and smooth surface. From optical microscopic image, the channel surface also appeared to be clean. However, residues were clearly observed from AFM image shown in Figure 3.7(b). Some spikes as tall as 60nm were observed from the cross-sectional profile shown in Figure 3.7(c). This surface residue can result in the random packing or crystallization of the deposited organic semiconductor. Therefore a surface cleaning step is required to obtain a smoother and cleaner channel surface. Oxygen plasma can be potentially used to etch off a thin layer of PVP on the surface, with an optimized plasma power.

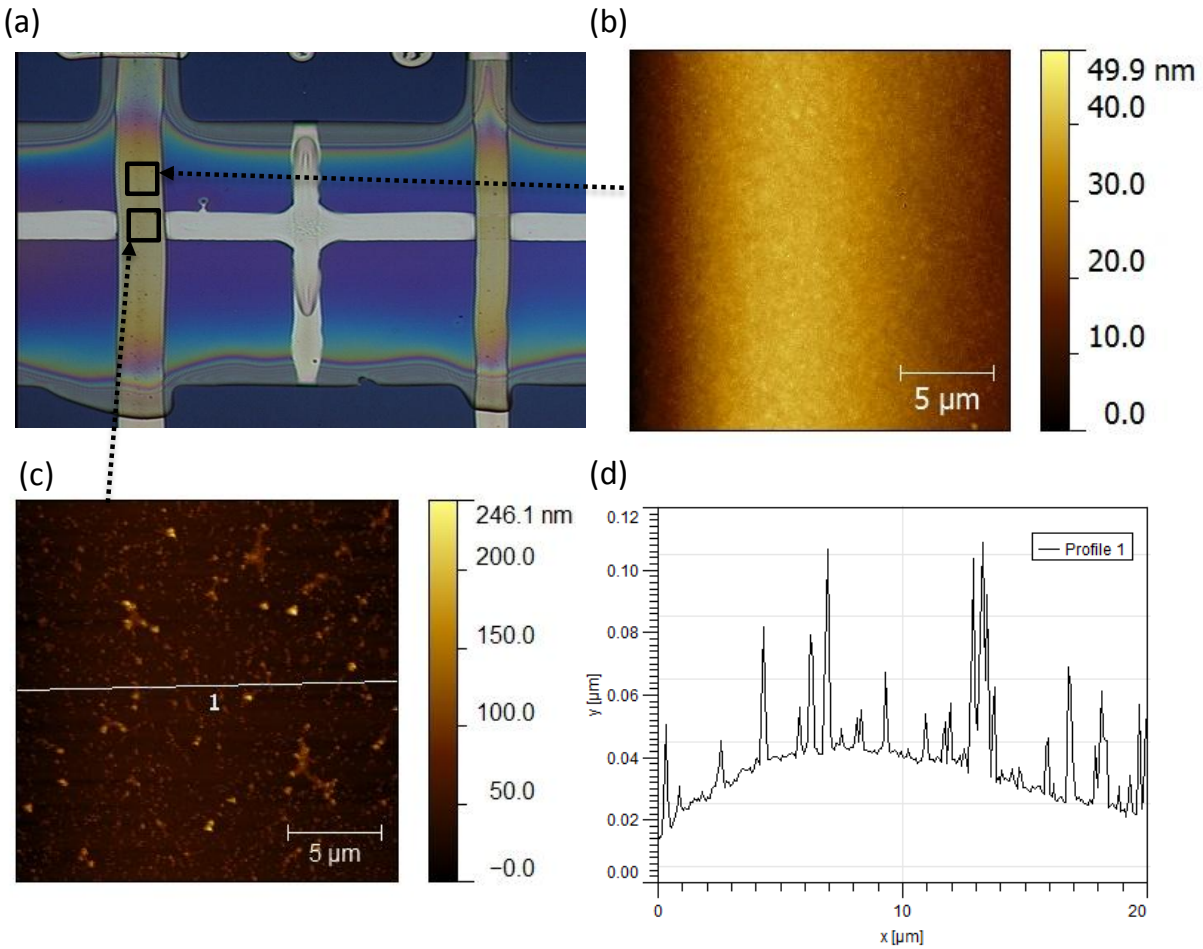

Figure 3.7 (a) Optical micrograph of two transistors with self-split S/D. The square indicates the area scanned by AFM (b) AFM image of the PVP surface near the channel area (c) AFM image of the channel area (d) Cross-sectional profile of the channel surface cut through the position noted in part (c).

3.6. Self-split alignment

The principle of dewetting the source and drain was extended beyond the single transistor level to entire circuit blocks, through a novel printing process – a self-split S/D device. The concept is to integrate the printing of S/D and interconnection to reduce the printing steps and enhance the throughput. The printing flow is illustrated in Figure 3.8(a), starting with the printing of gate, followed by the printing of PVP. The same optimization was performed on the gate, PVP and S/D to facilitate self-alignment. A perpendicular silver line was then printed across the gate line. The silver line initially connected, start to gradually dewet the channel surface. After a wait time of 70 seconds, the silver line self-split into S/D while simultaneously self-align the gate as shown in Figure 3.8(b). The process was then continued with a sintering of the S/D. Finally, baseline pentacene precursor was printed on the top followed by an annealing step. Figure 3.8(c) and (d) show the transistor characteristics. The transistor has a similar mobility of 0.01 cm^2/Vs. The channel width and length are 59 µm and 61 µm respectively.

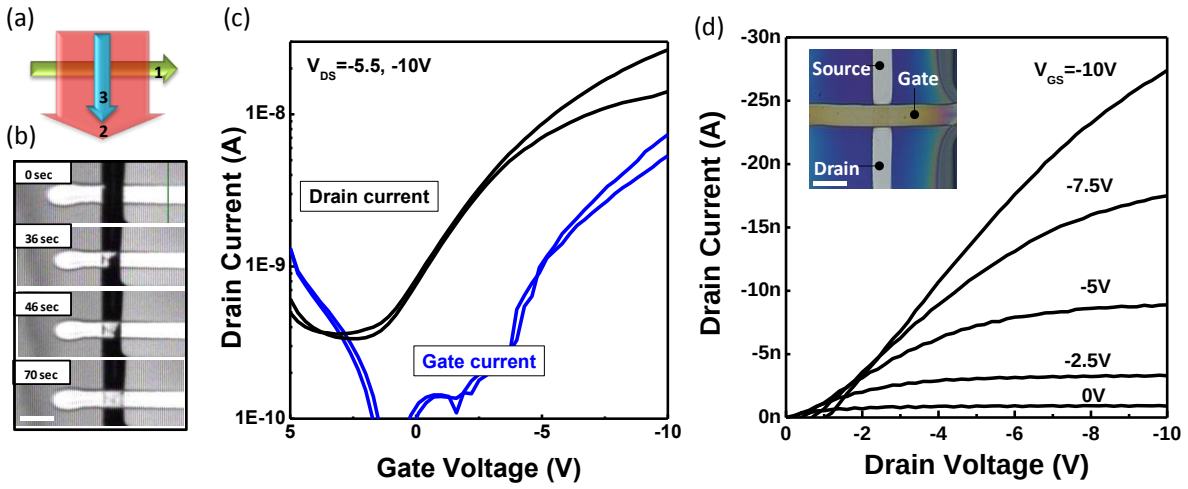

Figure 3.8 (a) Printing flow of a self-split transistor (b) Time-lapse optical micrographs captured by the Dimatix printer showing the process of S/D self-splitting with time. (c) transfer and (d) output characteristic of a printed self-split transistor. All scale bars represent 100 µm.

The self-split technique is highly compatible with integrated circuit fabrication. The S/D formed by self-splitting can be used as the interconnection with other circuits. Figure 3.9(a) shows two transistors with an inverter-like connection realized by the self-split S/D. Circuit structures required strings of transistors can be printing using minimized steps. Figure 3.9(b) shows a transistor array printed using the self-split technique. The vertical silver lines were printed and self-split into segments to become S/D, connecting adjacent transistors. The equivalent circuit is shown in Figure 3.9(c).

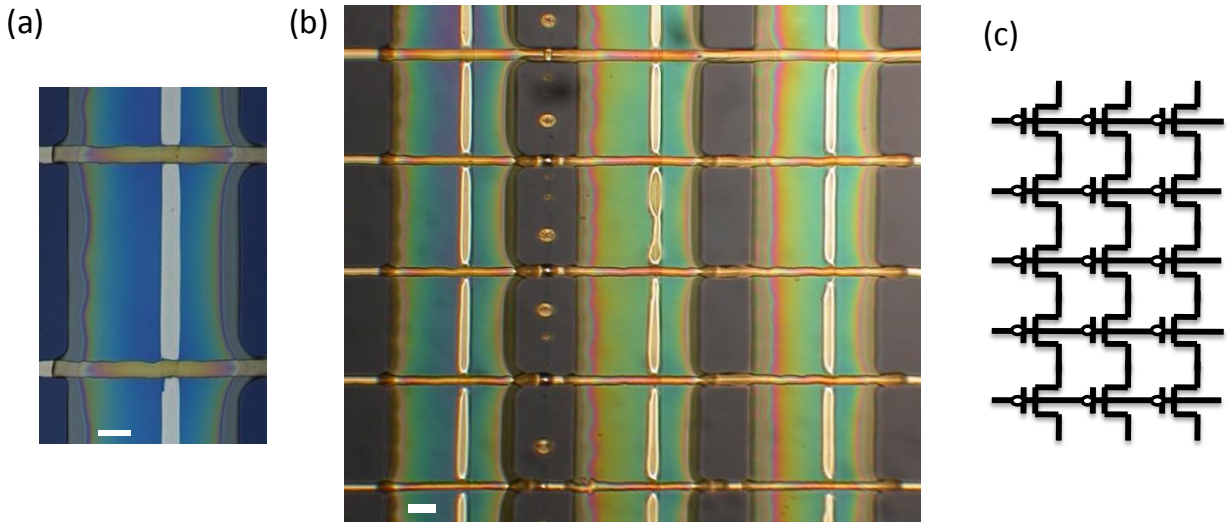

Figure 3.9 (a) Optical micrograph of an inverter structure printed using self-split S/D. (b) Optical micrograph of the printed self-split transistor array. (c) The equivalent circuit of the transistor array. All scale bars represent 100 µm.

3.7. Printing interconnect

To demonstrate more circuit integration, the self-splitting technique has further been utilized for printing of interconnection. Without a self-aligned interconnect, connecting discrete printed transistors becomes challenging. Short/open circuits caused by poor printing registration can dramatically deteriorate the fabrication yields. Here, a self-split/self-align interconnect using the principal of selective wetting was demonstrated. Figure 3.10(a) shows the time-lapse optical micrographs captured by the fiducial camera on Dimatix printer. A perpendicular interconnect was printed, intending to connect three adjacent printed post-S/D-sinter transistors. Instead of manually patterning the line into segments to align to the S/D pad of each transistor, a straight line was printed across all three transistors. Similarly to the aforementioned self-split S/D, the silver dewets the channel of each transistor and spontaneously flows perpendicularly into the S/D electrodes, forming good contacts with no needed pad area. The resulting S/D electrodes completely split while three transistors are connected in a cascade scheme, resulting in borderless contacts with excellent alignment.

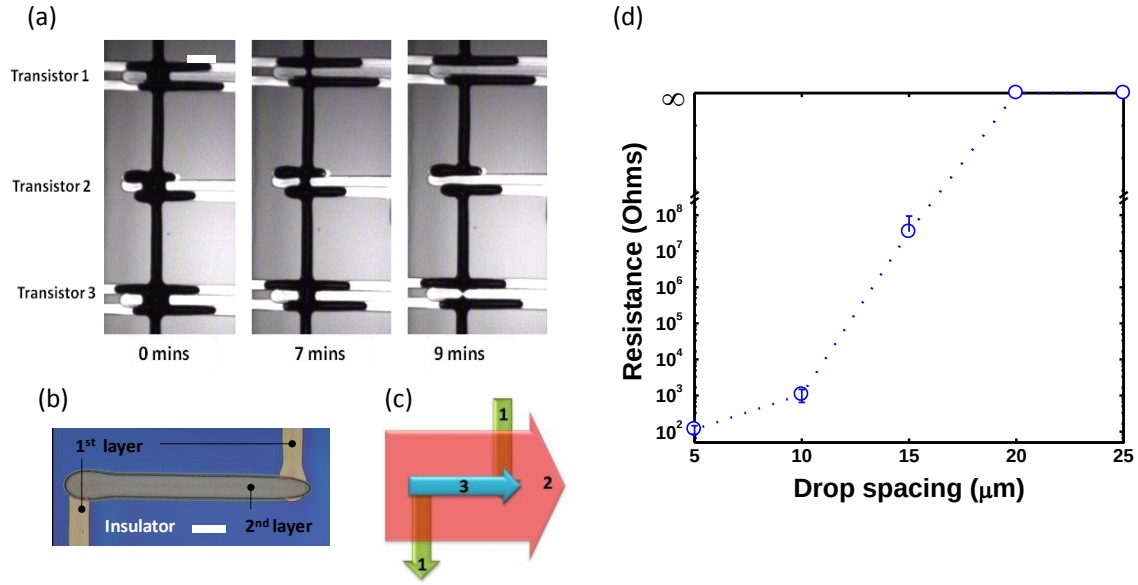

Figure 3.10 (a) Time-lapse optical micrographs captured by the Dimatix printer, showing the process of self-split/self-aligned interconnect. (b) Optical micrograph of a printed contact chain. (c) Printing flow of the contact chain. (d) Resistance of the contact chain versus the drop spacing of the horizontal line. All scale bars represent 100 μm.

A complete process module for interconnection requires a printable via technique to allow for interconnection between layers separated by a dielectric. The first printed via-hole was demonstrated by H. Sirringhaus et al., using a good solvent of isopropanol to dissolve PVP and form a crater-like via-hole [26]. Here, we demonstrated a novel semi-additive via process combining the printing of a via-hole with the printing of an interconnect line. Figure 3.10(b) shows the optical micrograph of a printed contact chain demonstrating the connection of two metal layers through a sandwiched PVP insulator. The printing flow is illustrated in Figure 3.10(c), starting with the printing of two vertical silver lines, followed by sintering and the printing of PVP insulator. Then, a horizontal silver line was printed prior to cross-linking the PVP to dissolve the same and deposit silver nanoparticle simultaneously, followed by a single

heating step to cross-link the PVP and sinter the silver. The horizontal line was printed with various drop spacing and the corresponding resistances of the contact chain are shown in Figure 3.10(d). Smaller drop spacing results in larger deposited solvent volume and silver concentration, and therefore the contact chain becomes conducting below drop spacing of 15 µm. The minimum resistance of 100 Ω, which is negligible comparing to the transistor resistance, is obtained at 5 µm drop spacing. Rough surface of the horizontal lines were typically observed. This can be caused by the non-uniform surface of PVP dissolved unequally by the solvent. Therefore, the measured resistance of the horizontal lines was typically higher due to the roughness. As a result, the resistance of the contact chain is limited by the horizontal line, rather than the contact resistance between two metal layers.

3.8. Printed inverter

Finally, a printed inverter was demonstrated using both the self-aligned and self-split S/D along with the printed interconnect introduced previously. A conventional inverter consists of a pull-up transistor and a pull-down transistor in the Complementary metal–oxide–semiconductor (CMOS) circuit, where a p-type transistor is used to pull the output voltage to highest voltage or V_{DD} and an n-type transistor is used to pull the output voltage to the lowest voltage or V_{SS} (replaced by a ground in digital circuits). Here, however, n-type transistors were not available as the majority of available organic semiconductors are p-type, due to a more efficient hole-hopping conduction mechanism [27]. Additionally, electron rich n-type materials are typically unstable in the presence of oxygen. Therefore, inverters with p-type-only transistors are used in this work. Due to lack of n-type transistors, the pull-down transistor needs to be replaced by an equivalent component, i.e. a pull-down resistor or a cut-off connected transistor or a diode-connected transistor [28]. As discussed in a previous report, using a cut-off connected transistor where the gate is connected to the output node, high gain can be achieved. However, this requires the size of the pull-down transistor to be very large, i.e. hundred to thousand times larger channel width than the pull-up transistor. Therefore, the cut-off connected scheme is difficult to implement. As a result, pull-down component using a resistor and a diode-connected transistor will be simulated, printed and discussed.

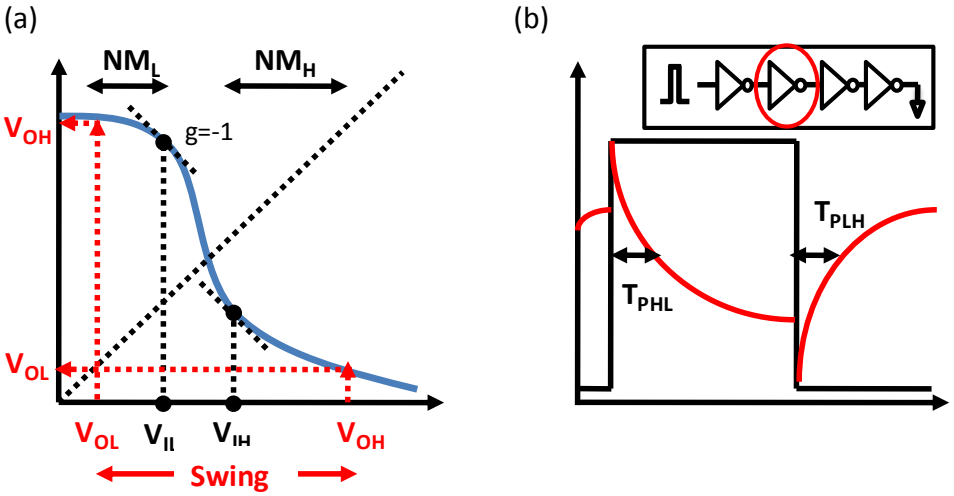

Figure 3.11 (a) Voltage transfer characteristic of a p-type only inverter. Various parameters were defined. (b) Transient response of an inverter. Propagation delay was defined by the average of the two delay time.

An inverter is conventionally evaluated by examining its voltage transfer characteristic (VTC) and transient response. Figure 3.11(a) shows VTC of a p-type only inverter. Various parameters including noise margin and voltage swing are defined in the figure using the conventional methods [29]. Figure 3.11(b) shows the transient response of an inverter. An inverter chain consists of four identical inverter in-series was used in the simulation, and the input and output waveform of the second stage inverter was used to determine its propagation delay by averaging the low-to-high and high-to-low delay [29].

Figure 3.12(a) shows a circuit schematic of an inverter consisting of a pull-up transistor and a pull-down resistor. In order to perform a circuit simulation to optimize the inverter, the transistor I-V characteristics were described using a custom-built verilog-A behavior model (see Appendix I). The inverter was then simulated using H-SPICE simulator to obtain the VTC and transient response. Figure 3.12(c) and (d) shows the various inverter parameters extracted from the simulated VTC and the transient response. Noise margin, voltage swing, and voltage gain all increases with higher pull-down resistance. However, larger pull-down resistance reduces the switching speed due to a slower pull-down of the output voltage. Therefore, a tradeoff exists in optimizing the voltage gain and switching speed. Here, we chose to maximize the switching speed with an acceptable voltage swing and noise margin by using a pull-down resistor of 100 MΩ.

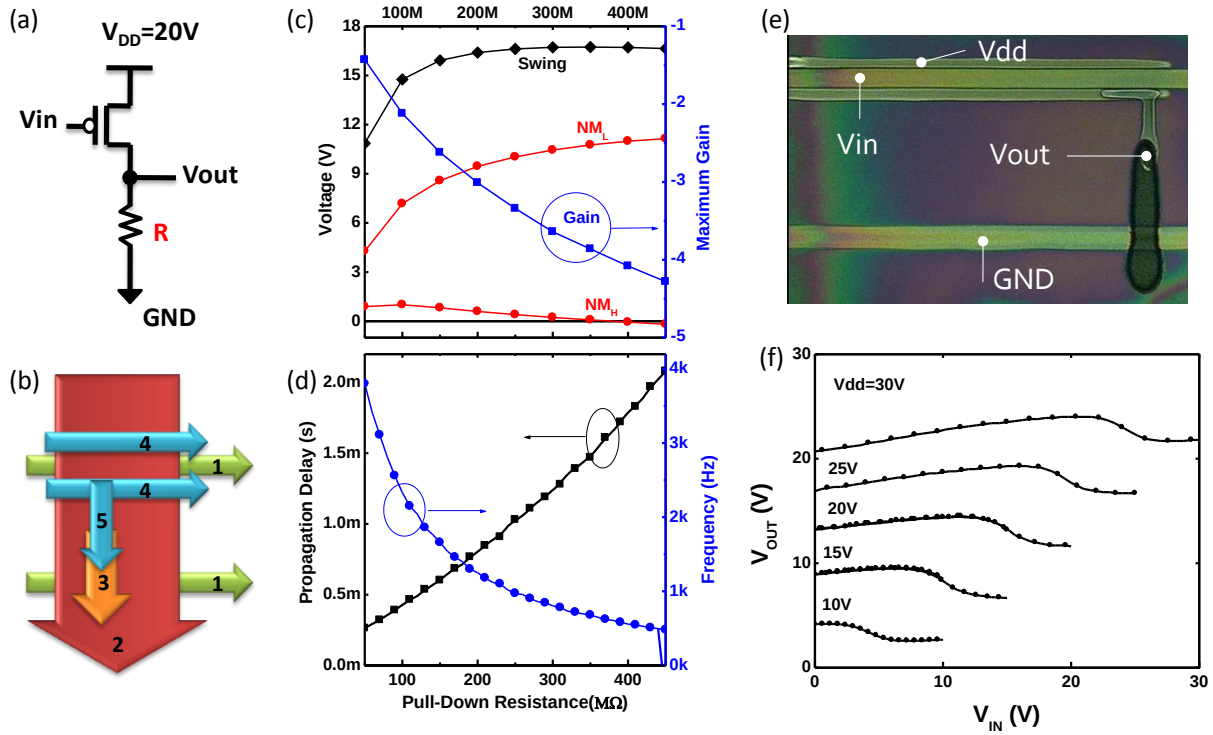

Figure 3.12 (a) The circuit schematic of an inverter with a pull-down resistor (b) printing sequence of the inverter (c) Maximum voltage gain, swing and noise margin as a function of pull-down resistance. (d) Propagation delay as a function of pull-down resistance. (e) Optical micrograph of a printer inverter consisting of a pull-up transistor and a pull-down resistor. (f) VTC of the inverter with various V_{DD}.

The inverter with a pull-down resistor was then printed using a printing sequence illustrated in Figure 3.12(b), where the number 1 to 5 denotes the printing of silver gates, PVP, a resistor, S/D, and interconnect respectively. Note that the step 3 has combined the printing of the resistor and interconnection (to the bottom-gate through dissolving PVP as introduced previously). Based on Figure 3.10(d), a drop spacing of 15 µm was used when printing the resistor in step 3 to produce a 100 MΩ resistor. The optical micrograph and the measured VTC of the printed inverter are shown in Figure 3.12(e) and (f) respectively. Unfortunately, the results were unsuccessful. The printed resistor was unable to pull down the output voltage to ground, despite the corrected pull-down resistance was measured. A positive slope from the VTC curve indicates the presence of a leakage path between Vout and Vin. As a result, despite an inverting behavior as observed in the VTC, a parasitic pull-up via the leakage path dominates the operation. The leakage was verified to be the PVP leakage current from the transistor. In addition to the PVP leakage, the inverter with pull-down resistor, although simple, was difficult to implement in our case, as the resistance matching between the transistor and the resistor by printing is challenging. Therefore, a diode-connected pull-down transistor was then used.

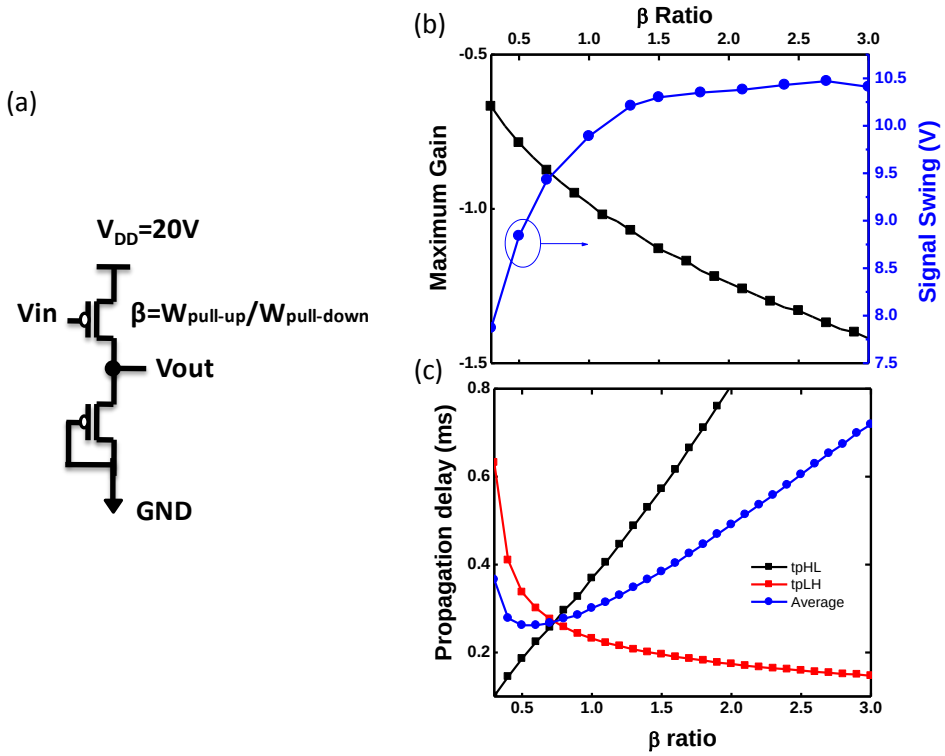

Figure 3.13 (a) Circuit schematic of an inverter with diode-connected pull-down transistor. (b) Maximum voltage gain and swing as a function of β. (c) Propagation delay as a function of β.

The inverter with diode-connected pull-down transistor was then simulated and printed. Similarly, to optimize inverter gain and switching speed, the β ratio (the channel width ratio of the pull-up transistor to the pull-down transistor) was varied in the H-SPICE simulation. Figure 3.13(b) and (c) shows the simulated results indicating a maximum gain and swing can be obtained by choosing a β ratio of 3. The gain can be potentially higher if using a larger β ratio,

with a sacrifice of the switching speed. Therefore an inverter with higher β ratio was demonstrated first.

Figure 3.14(c) illustrates the printing sequence of the inverter. The number 1 to 5 denotes the printing of silver gates, PVP, via, S/D, and interconnects respectively. The pull-down transistor was formed by the self-split technique while printing the interconnection in step 5. The optical micrograph and measure VTC of the inverter are shown in Figure 3.14(b) and (d) respectively. A β ratio of 15 was obtained in this inverter. The VTC curves still show a positive slope at lower Vin, indicating that the leakage of PVP still disturbed the voltage inverting. Fortunately, the pull-up and pull-down transistor had a better matching resistance; therefore a clean inverting VTC was obtained. The voltage gain with various V_{DD} shown in Figure 3.14(e) is lower than expected, due to the extra leakage path that prevents the output voltage from pulling down to ground.

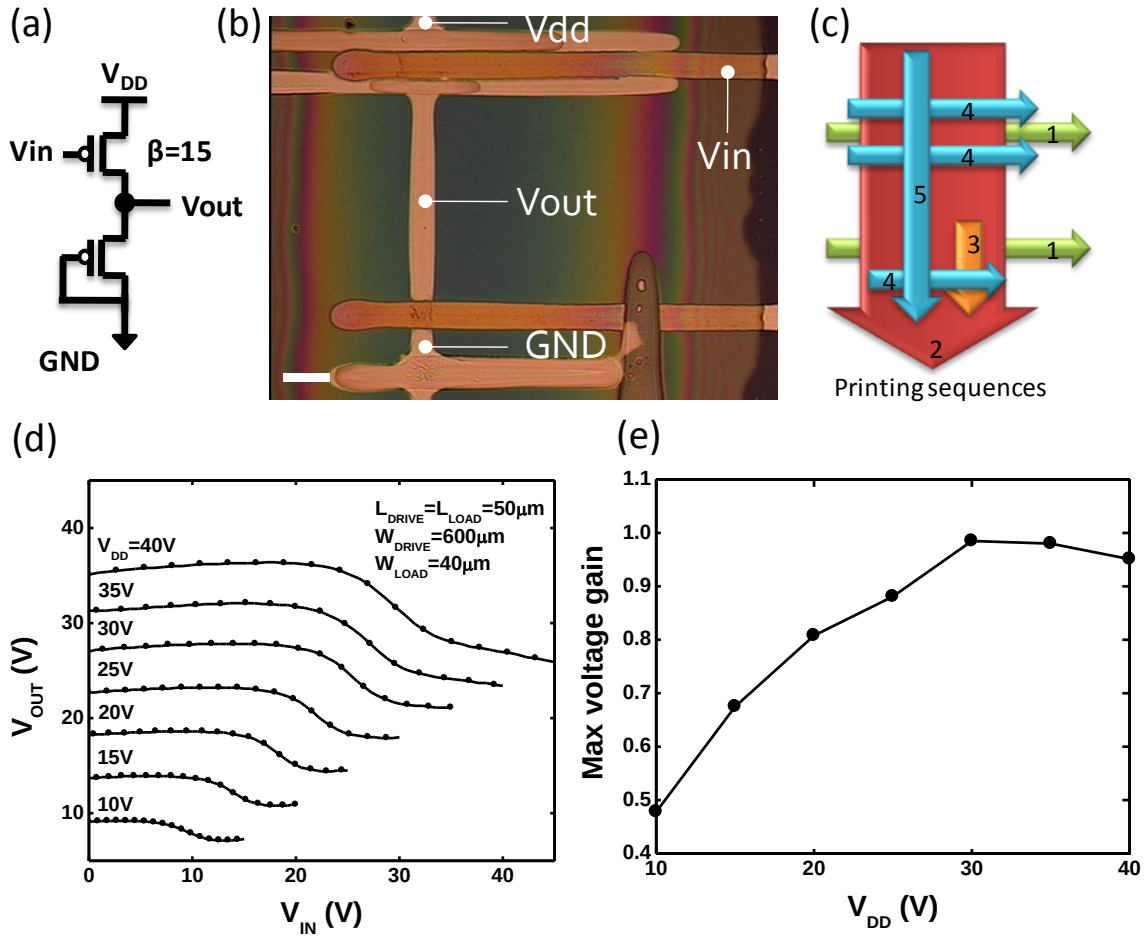

Figure 3.14 Printed inverter with self-split a load transistor (a) The circuit schematic of the printed inverter. (b) Optical micrograph of the inverter. The scale bar represents 100 μm. (c) Printing flow of the inverter. (d) Measured voltage transfer characteristic of the inverter with various V_{DD}. (e) Maximum voltage gain as a function of V_{DD}

To demonstrate an inverter with optimized voltage gain and switching speed, an inverter with a diode-connected pull-down transistor with a β ratio of 3 was printed. The printing sequence shown in Figure 3.15(c) combines all the printing technique that introduced in this chapter,

therefore the detail processing steps are described as follows: The processes started with a printing of silver as gate electrodes, followed by sintering at 200 ℃ for 10 minutes. PVP was then printed atop the gate as a gate insulator. Before cross-linking the PVP, a printed via and interconnect (step 3) was used to connect the gate and source of the load transistor to form a diode-connect configuration. A heating step of 200 ℃ was performed for 10 minutes to cross-link PVP and sinter the silver. S/D electrodes of both the drive and load transistors were then printed, self-aligning the gate, followed by sintering at 200 ℃ for 10 minutes. An interconnect line was then printed to self-split and self-align the two transistors. Finally, pentacene precursor was printed on the transistor channel, followed by an annealing step of 150 ℃ for 25 minutes. The VTC of the printed inverter measured with various V_{DD} is shown in Figure 3.15(d). Voltage gain of -1.26 was obtained, slightly lower than the simulated results. Maximum voltage gain of -1.46 was achieved under V_{DD} of 50 V as shown in Figure 3.15(e). Detail parameters of the printed inverter are outline in Table 3.2.

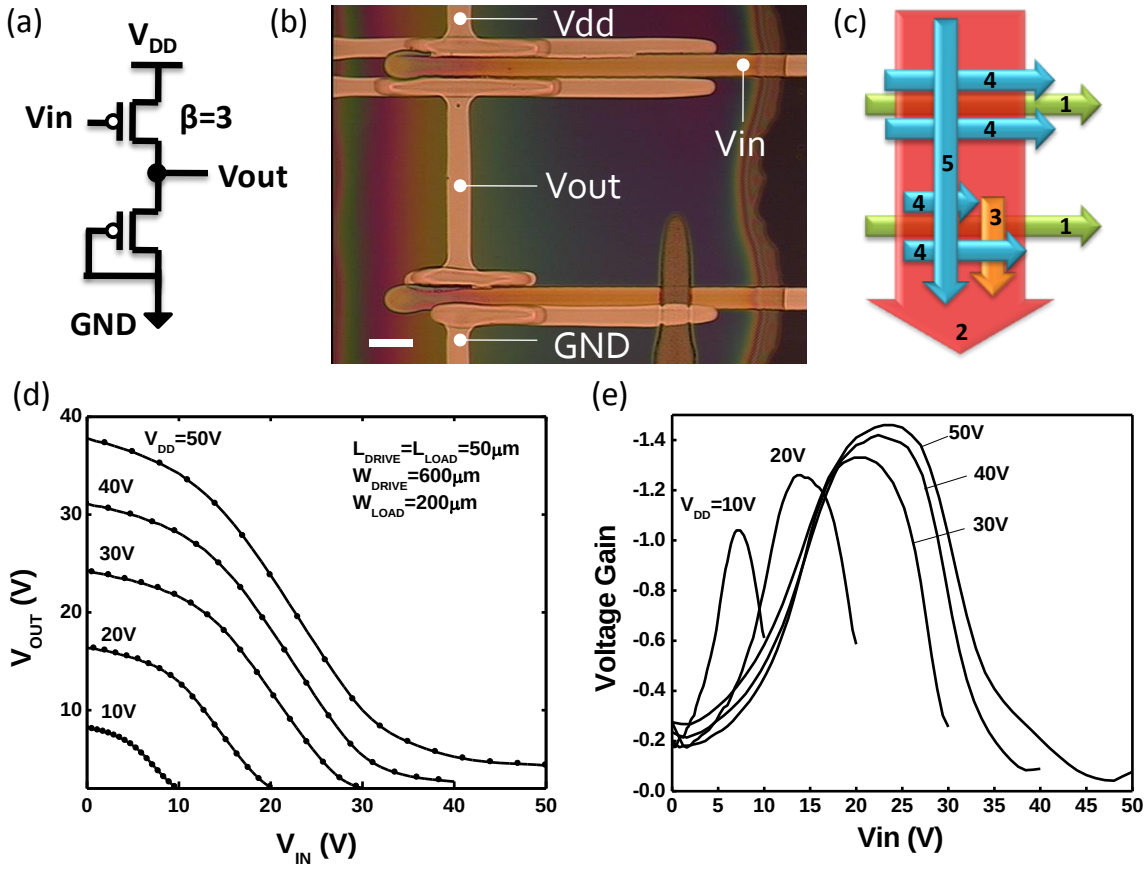

Figure 3.15 (a) The circuit schematic of the printed inverter. (b) Optical micrograph of the inverter. The scale bar represents 100 μm. (c) Printing sequence of the inverter. (d) Measured voltage transfer characteristic of the inverter with various V_{DD}. (e) Inverter voltage gain as a function of input voltage and Vdd.

Vdd	VOH	VOL	VIH	VIL	NML (VIL-VOL)	NMH (VOH-VIH)	Swing (VOH-VOL)	Max gain
10	6	5.5	7.97	6.5	1	-1.97	0.5	-1.04
20	13.5	9	18	11	2	-4.5	4.5	-1.26
30	21.7	9.5	26.1	14.9	5.4	-4.4	12.2	-1.33
40	30	5.5	28.87	14.91	9.41	1.13	24.5	-1.42
50	36	6.2	30.1	14.92	8.72	5.9	29.8	-1.46

Table 3.2 Detail parameters of the inverter as a function of Vdd.

The performance of the inverter was then determined by measuring the propagation delay time between an input square wave and the output waveform. For the transient output measurement of the inverter, the 4156C was used to bias the circuit. The input square wave of 200 Hz was provided by an Interstate Electronics Corporation F34 function generator. The output was buffered by an operational amplifier Burr Brown OPA602BP and the waveform was measured using an Acute DS-1202 Oscilloscope. As shown in Figure 3.16(b), a low-to-high delay of 0.3 ms and a high-to-low delay of 1.65 ms are measured at 10V, resulting in an average propagation delay of 0.975 ms. Due to the extra loading caused by the parasitic capacitance between the output electrode and the bottom silicon wafer, the output load was equivalent to a fan-out of 2 ($C_{load}/C_{in}=2$). Since propagation delay is proportional to the product of the equivalent resistance and the load capacitance ($T_p \sim R_{eq}C_{load}$), the inverter is expected to have a smaller propagation delay of 0.488 ms at a fan-out of 1 ($C_{load}=C_{in}$). The propagation delay corresponds to a switching speed of 2 kHz. While this performance level is suitable for many low-cost electronic applications, and is already competitive with the best fully printed circuits reported to date [30], [31], the inverter gain can be further improved by enhancing the transistor performance and optimizing circuit design to maximize the product of g_m (transconductance) and R_{out} (output resistance). The noise margin can also be improved by reducing the sub-threshold leakage of the transistor. Furthermore, the gate delay is expected to be improved by downscaling of the channel length, improved mobility and the use of CMOS circuits in the future. Despite this, however, the benefits of self-alignment in terms of parasitic capacitance reduction are clear.

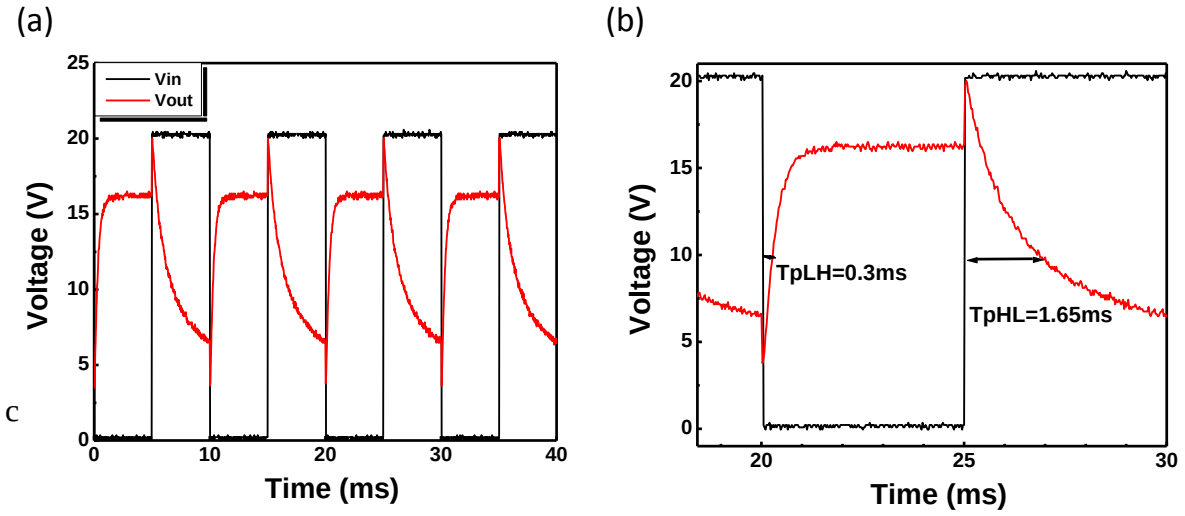

Figure 3.16 (a) Transient response of the inverter. (b) Extraction of the propagation delay.

3.9. Summary

We have demonstrated various novel printing techniques including self-aligned S/D to gate, self-split S/D and self-aligned interconnection for the first time. Using these, we demonstrate overlap capacitances as low as 0.14–0.23 pF mm^{-1} achieved by a purely printing process. We also demonstrated a fully printed inverter with a switching speed of 2 kHz, despite the use of relatively low performance materials. The performance of the transistor as well as the switching speed of the inverter is expected to be further improved by scaling down the channel length. Therefore, in the next chapter, we will introduce a novel printing technique to scale down the printed gate linewidth. Combining this with minimized overlap capacitance, faster switching speed will be demonstrated.

3.10. References

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Chapter 4 Organic Transistors Fabricated using a Novel Hybrid-Printing Technique

4.1. Introduction

In the previous chapter, we demonstrated the self-alignment of printed S/D patterns to gate electrodes to achieve transistors with minimum overlap capacitances [1]. However, in those self-aligned transistors, the performance was limited by the scalability of the gate line, as the channel length is defined by the gate linewidth. Therefore, scaling down the printed linewidth is pursued in this chapter to improve the transistor performance.

Scaling down the printed gate line necessitates the printing of an ultra narrow conductive track, which is difficult to achieve using conventional printing systems. Among the various printing techniques commonly used for printing electronics, inkjet has been shown to have a relatively high printing resolution. Recalled from Chap. 2, an inkjet printed line can be scaled down by increasing inkjet drop spacing, as shown in Figure 4.1. However, when drop spacing is larger than the size (diameter) of a single drop, the printed lines are no longer continuous and become separate drops. Therefore the drop size determines the minimum achievable linewidth.

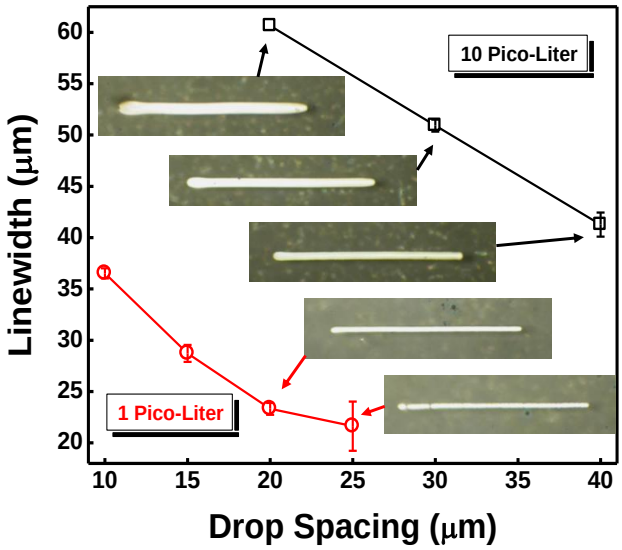

Figure 4.1 Printed linewidth as a function of drop spacing. Optical micrographs corresponding to each drop spacing and drop volume are shown.

To further reduce the linewidth, a smaller drop size is required. This can be done by reducing the drop volume. Unfortunately, the minimum drop volume of state of the art inkjet systems is one picoliter, resulting in printed dots with a diameter of ~20 μm on regular substrates (Figure 4.1). This has prohibited the scaling of printed lines below ~20 μm. Although the printed features can be scaled down by further reducing the drop volume, it is difficult to reduce the drop volume below one picoliter since the droplet size is fundamentally limited by the surface tension. While there have been demonstrations of femtoliter and attoliter inkjet heads using electrohydrodymanic techniques, scaling of the complex patterns necessary to realize circuits has remained elusive due to the difficulty in controlling the landing and positioning of such small

drops [2], [3]. Thus, to achieve highly scaled and high performance printed transistors using a low-cost approach has remained challenging. Therefore, in this chapter, we demonstrated a novel hybrid-printing technique to realize printed features as narrow as 5 µm using a state-of-the-art printer. Using this technique, we demonstrated all printed highly scaled transistors and inverters. Due to the substantially reduced capacitance and reduced linewidth, demonstrated fully printed inverters have a propagation delay as low as 15 µs, in contrast to the typical value of ~0.01 s obtained by previously reported all-printed processes [4–6]. We thus demonstrated orders of magnitude improvement in performance relative to other reported fully printed circuits.

4.2. PND Technique

4.2.1. PND concept

The novel hybrid-printing technique was inspired by dip-pen nanolithography, in which molecules are delivered from an atomic force microscope tip to a solid substrate of interest via capillary transport [7]. Here, we implemented the technique in a low-cost manner by merging a multi-nozzle inkjet head with a mechanical probe system to provide both the high throughput of inkjet and the feature scalability of a mechanical pen. The process consists of two steps − print and drag (PND) as illustrated in Figure 4.2(a).

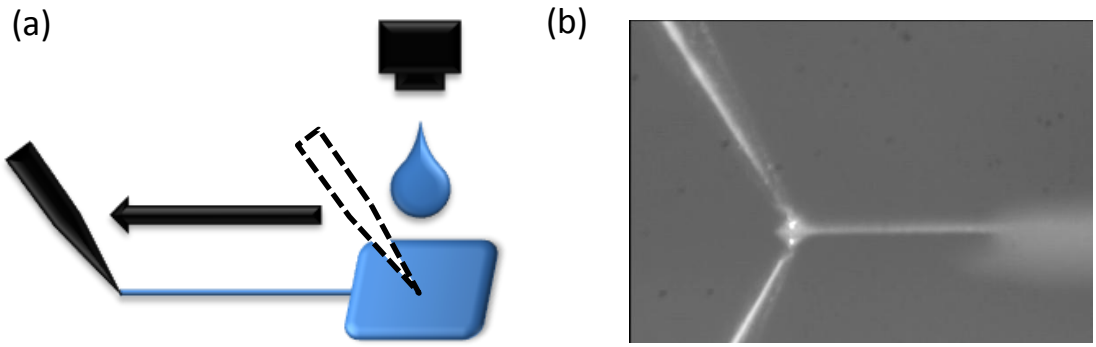

Figure 4.2 (a) A diagram showing the inkjet printing and mechanical pen dragging process (b) Microscopic image showing the ink dragged out by the probe tip

First, large pads and other large features were printed on a conventional Dimatix DMP-2800 inkjet printer equipped with a 10 pL piezoelectric head, using silver nanoparticle ink (Suntronic U5603). The silver ink solvent evaporates slowly and thus allows the pads to act as ink reservoirs for the subsequent process. Next, a micron-scale mechanically controlled tungsten probe was used as a pen to drag through the pad to create a highly scaled feature. The ink flow is facilitated by the meniscus formed between the tip and the pad. Figure 4.2(b) shows the microscopic image captured while the line was dragging out from the pad. The meniscus between the ink and the tip is clearly seen. Due to this, actual contact between the probe tips and the surfaces is not necessary. Thus the PND technique is also expected to be applicable to surfaces such as soft plastic substrates.

4.2.2. PND setup

The PND concept was initially verified in a probe station: a probe manipulator was used to manually contact the probe tip on a pre-printed silver pad, followed by a chuck movement to create a PND line. However, the process was not repeatable due to an inconsistent human control. Therefore, a PND system was built to precisely control the dragging process. A custom-built printer, originally built to perform inkjet printing using a Microfab nozzle or a Dimatix cartridge, was modified to fit this need.

Figure 4.3 shows the PND setup. A top camera with direct light source was used to monitor the top-view of the PND process. The top camera has a maximum magnification of 45X. A side camera was used to observe the tip-ink contact and meniscus. The stage from the original printer was utilized for an X-axis, Y-axis, and theta movement. A probe holder with an integrated L-arm was used to hold the probe tip. The vertical position (Z-axis) of the tip was controlled using a stepper motor with 1 μm resolution. Using this setup, the dragging speed can be precisely controlled by varying the moving velocity of the stage. Dragging parameters associated with the PND process can then be studied.

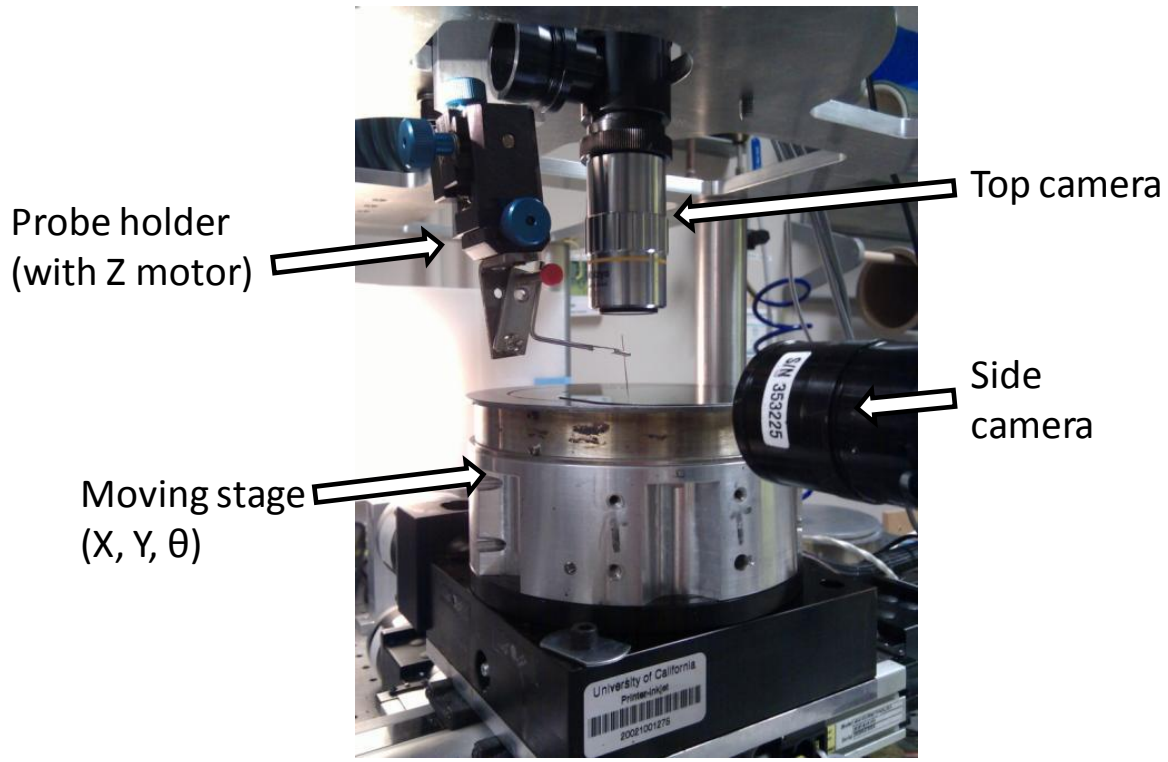

Figure 4.3 Photograph of the PND setup on a inkjet printer system.

4.2.3. PND process parameters

Using the side camera, we can clearly observe and monitor the dragging process. Figure 4.4(a) shows the image captured when the probe tip landed on a printed pad. The shape of the meniscus is determined by the ink-tip and ink-surface contact angle. The equilibrium was reached in less than a second after the contact. When the dragging process is initiated by the stage movement, the meniscus height (H_M) as well as the meniscus width (W_M) started to reduce as soon as the tip left the printed pad. This is due to loss of the ink supply from the pad. Figure 4.4(b) illustrates the process where H_M and W_M are both reduced if the tip is further from the pad. This explains the typical shape of the dragged lines shown in Figure 4.4(d) and (e), where the linewidth is reducing from the pad to the line-tip. Figure 4.4(c) shows an optical image of the probe tip, matching the diagram shown in Figure 4.4(b). The fact that the tip shape is tapered causes the linewidth to reduce toward the line-tip in addition to the ink loss. Figure 4.4(d) and (e) shows the dragged lines with the dragging direction to the left and right respectively. The asymmetric lines can be explained as follows: Due to the tip-surface angle shown in Figure 4.4(a), H_M is higher on the left side than on the right side, in order to maintain a constant ink-tip contact angle. Therefore, more ink can be carried out of the pad when dragging to the right, resulting in longer and wider lines.

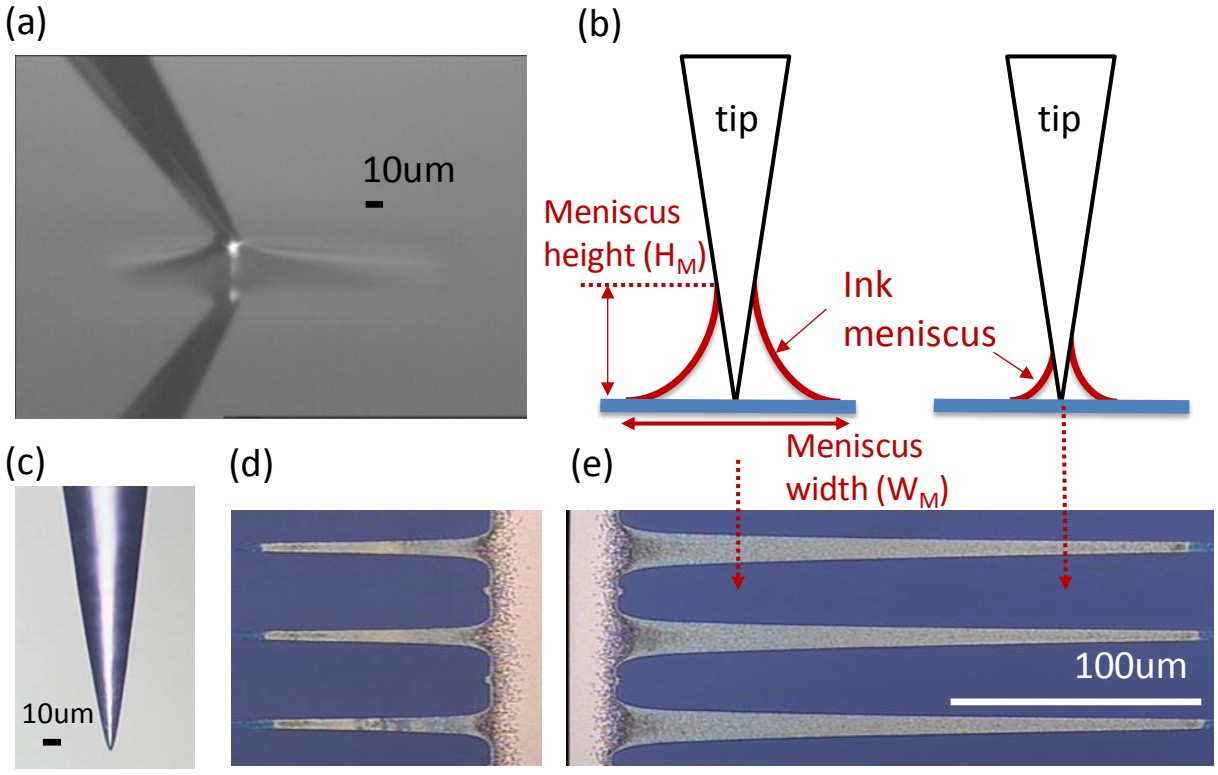

Figure 4.4 (a) Microscope image showing a meniscus formed between the pad and the probe tip. (b) Cross-sectional diagram showing the level of the meniscus with respect to the line position (c) Optical micrograph of the probe tip (d) Optical micrograph of the PND lines created by dragging to the left and (e) to the right.

The optical micrograph in the inset of Figure 4.5(a) shows a typical dragged line. The length (L), line-tip width (W_T) and line-base width (W_B) were defined (W_B was measured right at the line-pad junction). The line geometry as a function of tip-surface distance, dragging speed, probe tip radius, and ink concentration was then studied.

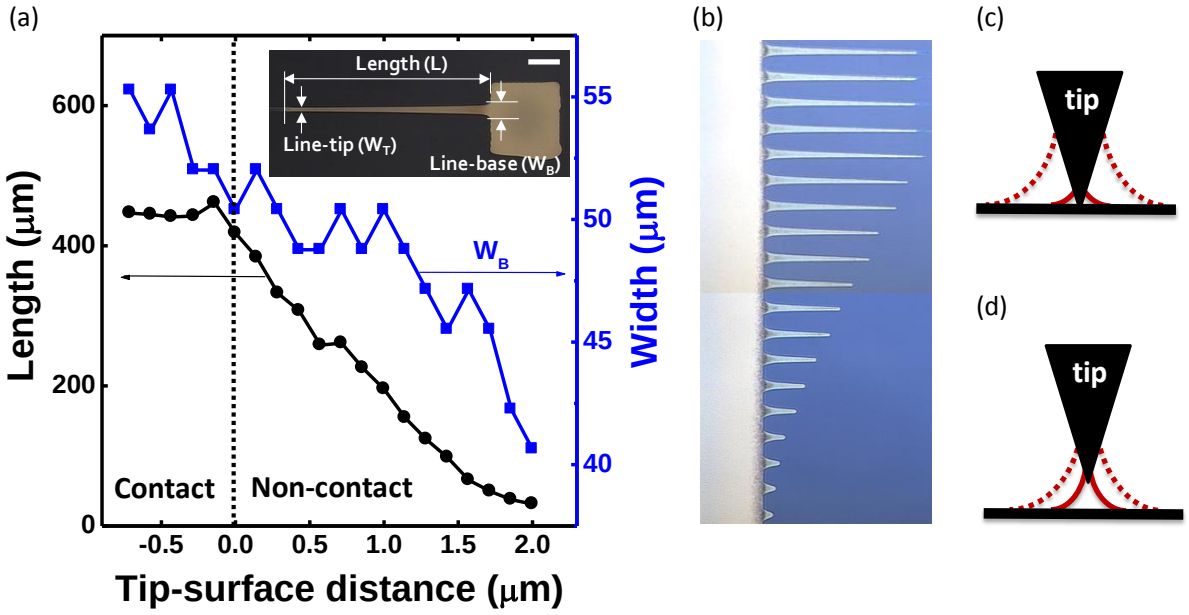

Figure 4.5 (a) L and W_B as a function of tip-surface distance. The inset optical micrograph shows a typical dragged line with the definitions of L, W_B, and W_T shown. The scale bar is 100 μm long (b) Optical micrograph of the dragged lines with various tip-surface distances. (c) A schematic diagram showing the tip contacting the surface and the corresponding meniscus. (d) A schematic diagram showing the tip raised 2um above the surface and the corresponding meniscus.

To examine the effect of tip-surface distance, multiple PND lines were produced with the tip-surface distance varying from 2 μm to zero (fully-contact) by a sub-micron decrement. The sub-micron resolution was achieved by slightly tilting the stage surface vertically, and then dragged lines horizontally in parallel. Figure 4.5(b) shows an optical micrograph of the dragged lines. The line at the bottom was dragged using a tip-surface distance of 2 μm, while the line on the top was dragged using a full-contact mode. Figure 4.5(a) shows the L and W_B as a function of the tip-surface distance. Both L and W_B increase with reducing tip-surface distance. When the tip contacts the surface, L becomes a constant, with only some noticeable variations. This can be explained using the diagrams illustrated in Figure 4.5(c) and (d). When the tip is 2 μm above the surface, the meniscus only forms on the utmost tip. In this case, although H_M can be identical to the case when the tip was fully contacting the surface, the tapered tip-shape results in a smaller W_M and hence a smaller W_B. Additionally, L was shorter due to the meniscus losing contact with the tip earlier than the fully-contact case. The W_B slightly increases after the tip-surface contact, possibly due to a reduction of the tip-surface contact angle and hence a larger initial W_M. Overall, full-contact can be used to compensate the variation of the L if the stage is not perfectly leveled.

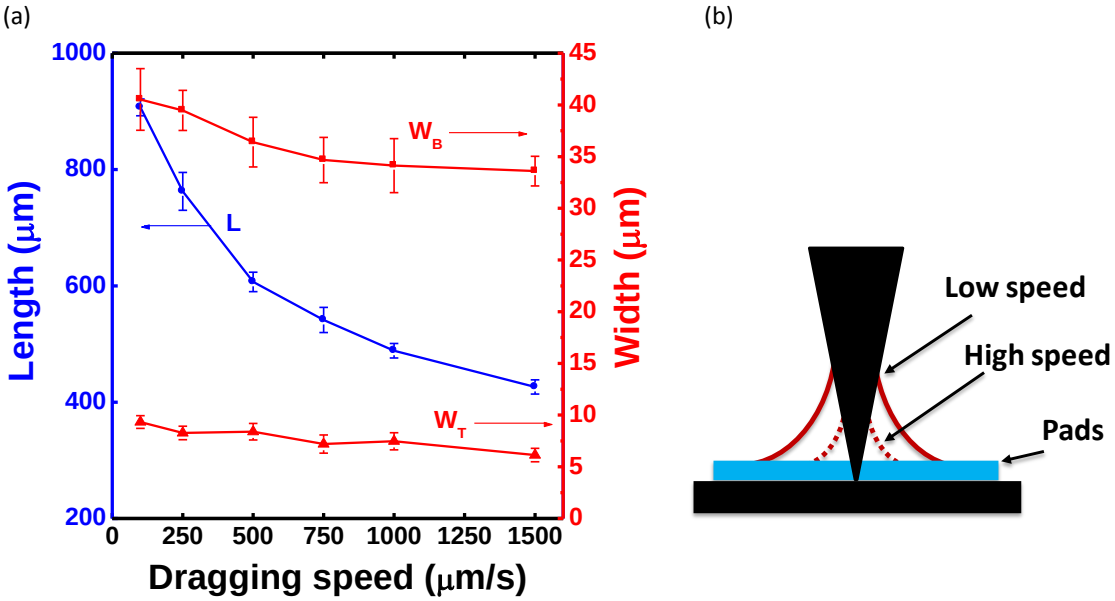

Figure 4.6 (a) L, W_B, W_T as a function of dragging speed. (b) Schematic diagram showing the different meniscus formed at different dragging speed.

The effect of dragging speed on the line geometry was then examined. PND lines with various dragging speed were produced, followed by the extraction of L, W_B and W_T. The average and standard deviation from 20 measured lines in each dragging speed were used for the following discussion. As shown in Figure 4.6(a), increasing dragging speed reduces the length of the feature, as well as both W_B and W_T. From the previous discussion, the increase of W_B indicated a possible change in the tip-surface contact angle. However, those changes were not clearly observed under a microscope with a 45X magnification. Therefore it is possible that when dragging at a higher speed, the meniscus had an insufficient time to reach the equilibrium height, resulting in a relatively smaller H_M and W_M and thus a smaller L, W_B and W_T. Although higher dragging speed is desired to enhance the process throughput, the resulting shorter lines are unfavorable, as shorter lines make the alignment of S/D difficult. Fortunately, this can be compensated by using a larger tip. Therefore, the effect of the tip radius on the dragged lines will be discussed in the following paragraph.

Since PND process relies on the formation of meniscus, the printed lines are expected to strongly correlate with the contact method and the probe tip radius. As discussed previously, the initial H_M and W_M are sensitive to the tip-surface contact angle. Therefore, the contact angle was kept constant as possible. The effect of probe tip radius was examined by dragging multiple lines at a fixed dragging speed of 1000 μm/s using different tips. Distribution statistics of L, W_B and W_T were then extracted. Probe Tips with three different point radii were used in this study: (1) Cascade PTT-120-25, point radius 12 μm (2) Cascade PTT-24-25, point radius 2.4 μm (checked out from Nanolab inventory) (3) Micromanipulator model 7s, point radius 0.35 μm, Tungsten tip, Nickel shank. The relation between L, W_B, W_T and tips radius is plotted in Figure 4.7(a). Clearly, L, W_B and W_T all scale with the tip radius. This was expected from the previous discussion, which implied smaller H_M and W_M with smaller tips. Dragged lines as narrow as 5um can be consistently formed using a probe tip with 0.3 μm tip-radius (inset of Figure 4.7(a)).

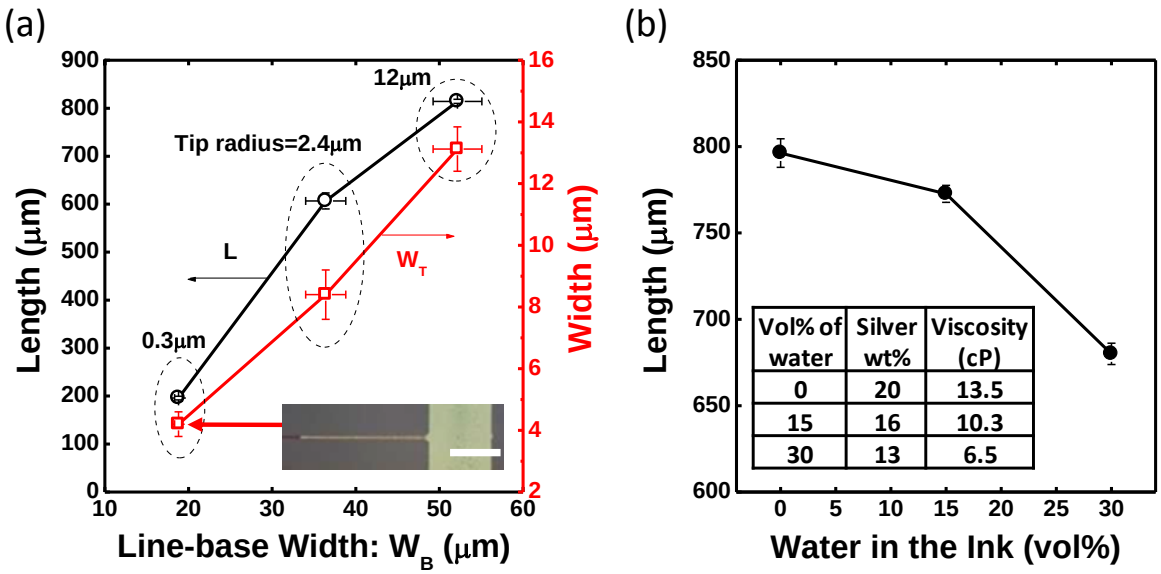

Figure 4.7 (a) L and W_T as a function of W_B. Three data sets correspond to three probe tip radius respectively. Inset: the dragged line with a 5 µm linewidth. The dragging speed is 1000 µm/s. The scale bars represent 100 µm. (b) Dragged length as a function of water vol% in the ink. The ink concentration and the corresponding viscosity are listed in the inset table.

The ink concentration also affects the dragged feature. Recall from Chap. 2 that the ink can be diluted by adding water to adjust the viscosity. Using this method, three different concentrations were formulated and the corresponding viscosities were obtained (listed in the inset table of Figure 4.7(b)). Square pads were printed with three different ink concentrations, followed by the dragging process using a fixed speed of 500 µm/s to produce multiple lines. The W_B and W_T were then verified to be independent of ink concentration, indicating the contact condition was consistent. Higher ink concentration or higher viscosity results in longer dragged lines as shown in Figure 4.7(b). This is possibly caused by a slower dropping rate of H_M during the dragging process, due to a slower ink-flow (higher viscosity). However, the measured viscosities do not account for changes in ink concentration occurring prior to and during the PND process due to evaporation. Therefore, further experimentation is required to verify the cause.

The unique shape of the PND lines (i.e. a wider and thicker line-base than the line-tip) is not ideal for applications of gate electrodes. Fortunately, the difference in line-thickness should not affect the insulator thickness atop if a conformal layer such as PVP is used. The difference in linewidth, however, could result in a non-uniform channel length if a self-aligned S/D is applied [8]. The tapered linewidth can be mitigated by producing a longer line, where the transition from W_B to W_T takes place over a longer distance, resulting in a more uniform linewidth. Moreover, the gate lines can be dragged from two pads in opposite directions and merged in the middle as shown in Figure 4.9(b). Using this method, the PND lines become more uniform and symmetric in the middle for gate electrode applications.

4.2.4. PND lines scaling

As previously indicated, further scaling should be possible by using a smaller probe tip. PND lines as small as 5 µm were demonstrated previously. However, conductivity measurements showed that the yield dropped significantly when the PND lines were narrower than 10 µm in W_T. Consequently, only 3% of the 5 µm lines were conductive. To investigate the failure, AFM was used to examine the surface morphology as well as profilometry of the PND lines.

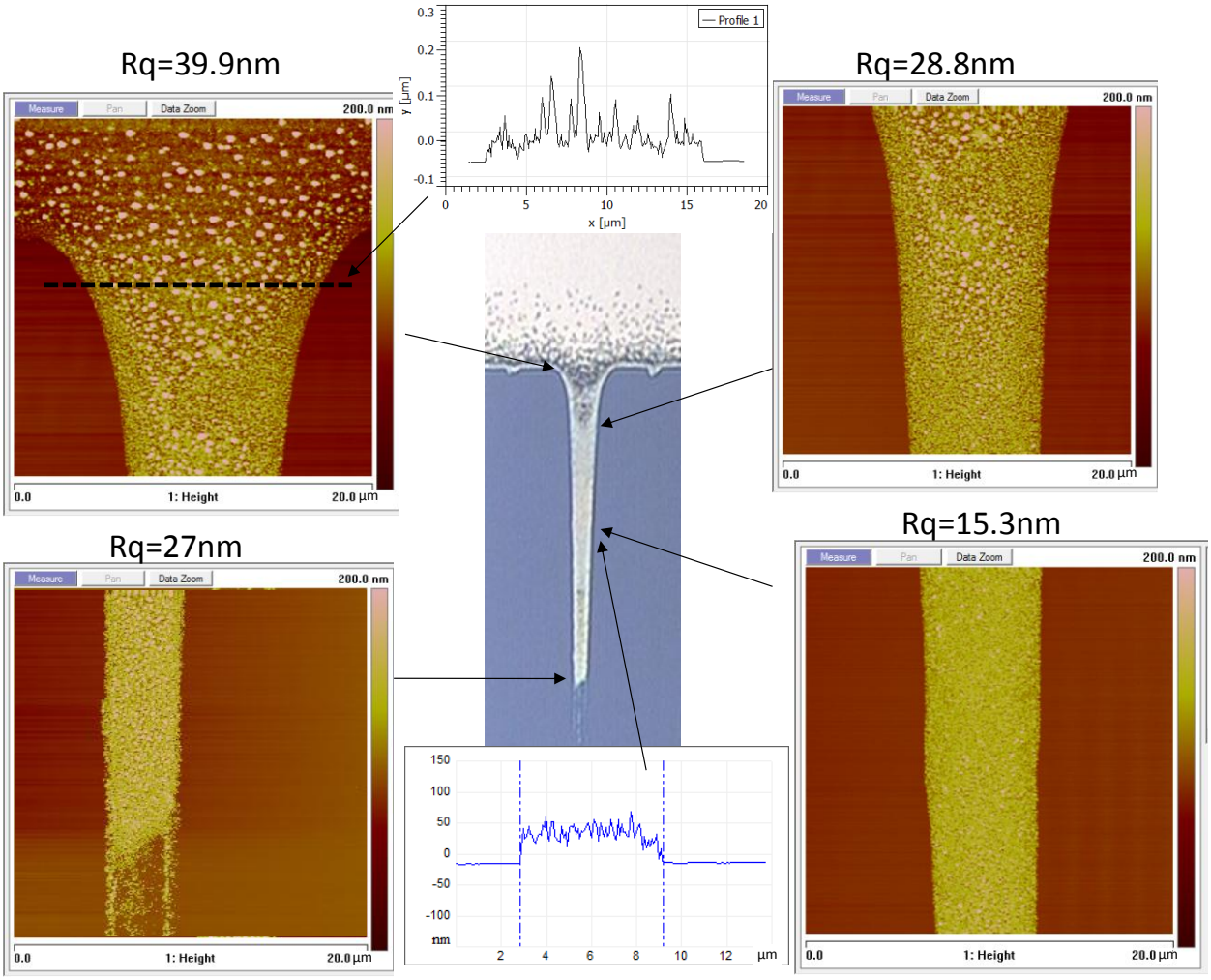

Figure 4.8 AFM images showing the surface morphology and profilometry of various positions in a PND silver line. Root-mean-square surface roughness (Rq) is also shown.

Figure 4.8 shows the AFM images correspond to various positions in a PND silver line. Root-mean-square surface roughness (Rq) of each segment is also shown. At the line-tip, a rough and non-uniform film was observed due to the depletion of ink supply at the end of the dragged line. The middle of the line shows a thickness around 70 nm and Rq of 15.3 nm. Note that the average silver nanoparticle size is also 70 nm, indicating the line consists of only a single to few layers of nanoparticles. However, the middle part seen in the AFM shows a dense surface, implying a

continuous film was formed. It is noticeable in the AFM images that the line becomes rougher toward the line-base. A cross-sectional profile near the line-base shows large spikes and voids with an average film thickness of 50 nm. The resulting sparse percolation network near the line-base is likely to be the cause of low conductive-yield. The results of a rougher and thinner line-base can be explained using the Laplace pressure: The hydrostatic pressure that built-up at the boundary of two fluids is equal to the product of the surface tension γ and the curvature of the surface *C* [9]:

$$\Delta p = \gamma \left(\frac{1}{R} + \frac{1}{R'} \right) = \gamma C$$

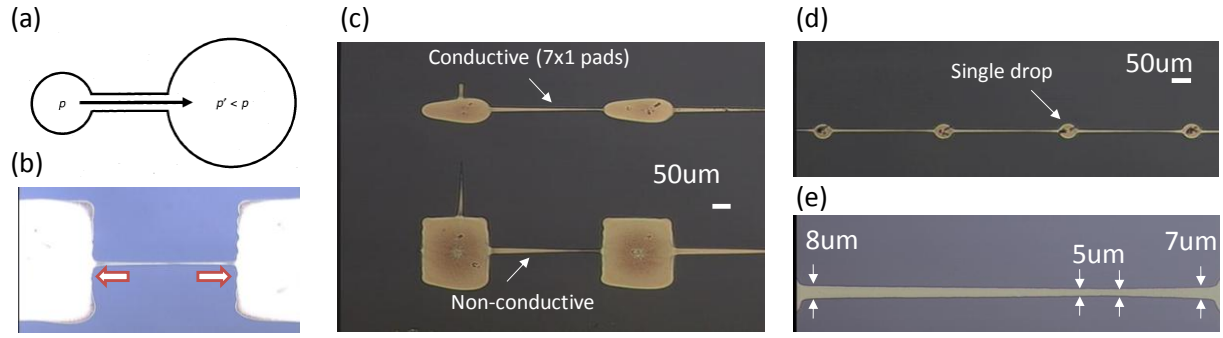

Figure 4.9 (a) A diagram illustrating the Laplace pressure: Small bubbles empty themselves into larger ones [9]. (b) Optical micrograph showing an analogous case to part (a). (c) Optical micrograph of two groups of PND lines with different pad size. (d) Optical micrograph of PND lines with single-drop pads. (e) Higher magnification of the part (d).

As a result, the fluid on the smaller curvature side will have a tendency to flow toward the large curvature side to minimize the pressure, as illustrated in Figure 4.9(a). Therefore, the small PND lines with large pads can be analogous to the case seen in Figure 4.9(a), where the ink with a smaller curvature is pushed back to the pads (Figure 4.9(b)). This can result in a lower concentration of the silver nanoparticles at the lines-pads boundary, matching the rougher and thinner region observed in AFM previously. Consequently, in order to achieve a smaller PND lines with high yield, the pads size needs to be scaled down as well. Figure 4.9(c) shows two groups of PND lines with 9 µm linewidth with different printed pads size. In this representative comparison, the lines with smaller pads are conductive, where the lines with larger pads are not conductive. This result verifies the theory explained previously.

To further scale down the linewidth and the corresponding pad size, the silver pads were printed on a HMDS treated oxide surface. As the surface become more hydrophobic, the printed drop sizes are reduced due to a higher ink-surface contact angle. Single drops were then used as the pads to minimize the hydrostatic pressure difference. PND was then performed to produce small lines. The PND lines are shown in Figure 4.9(d) and (e) with low and high magnification respectively. Since the curvature difference between the lines and pads is significantly reduced, the 5 µm lines have smooth surfaces without rough regions at the line-pad boundaries. By properly scaling down the pad size, the yield of the 5 µm lines was improved to 25%.

Although the yield was improved by considering the relevant fluid dynamics, the yield is still unacceptable for gate line applications. The low-yield is possible due to the use of relatively

large size nanoparticles, resulting in a poor percolation network. Therefore, smaller nanoparticle systems will be used, attempting to scale down the PND lines further. More scaling discussion will be continued in Chapter 5. Here, we will focus on the integration of PND lines in printed transistors and inverters.

4.3. Printed transistors using PND S/D

4.3.1. PND source and drain

The PND technique can be used to print the source and drain (S/D) electrodes of transistors, as fine S/D lines can minimize the overlap to the gate electrodes, resulting in minimum parasitic capacitance. Additionally, small spacing between two PND lines can be formed by optimizing the process parameters. The S/D electrodes produced by the PND technique are illustrated in Figure 4.10(a). Two silver pads were first inkjet printed, followed by the PND process to drag out the S/D electrodes from each pad. From previous discussions, the length of the dragged lines can be control by dragging speed, tip radius, tip-surface distance. Here the dragging speed was optimized to account for the asymmetric length from the two opposite directions in order to form a close spacing between the two electrodes. Figure 4.10(b) shows the PND S/D electrodes with a spacing of 2.5 µm. This spacing determines the channel length of the transistor. Figure 4.10(c) shows the histogram of the 35 channels created by the PND technique. A median channel length of 8um and a minimum of 2 µm were produced.

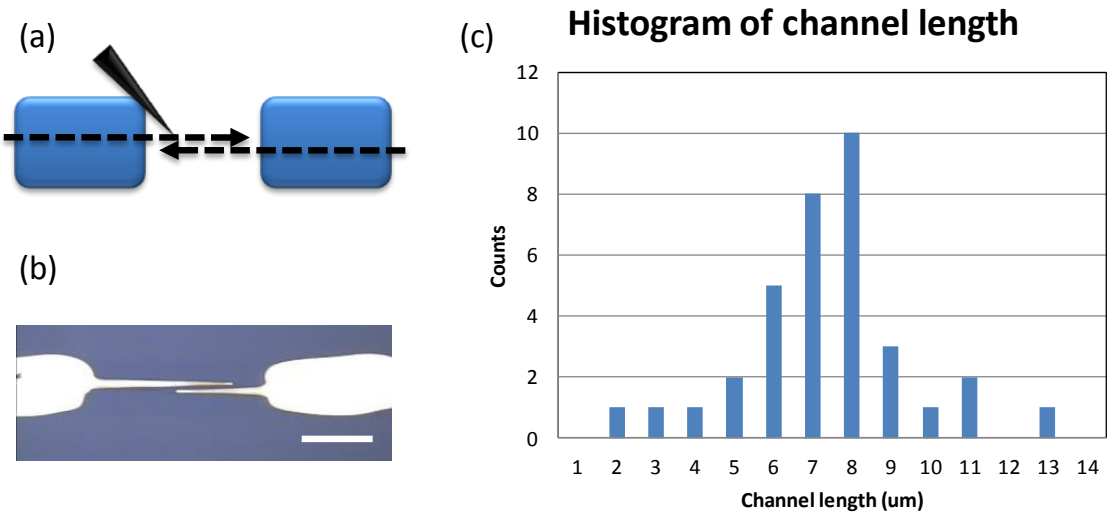

Figure 4.10 (a) Schematic diagram illustrating the S/D electrode produced by PND techniques (b) optical micrograph of PND S/D. The scale bar represents 100 µm (c) Histogram of channel length produced by PND S/D.

Using the structures above, back-gated organic transistors were then demonstrated. Figure 4.11(a) shows the cross-sectional structure of the transistor. An N-type heavily doped silicon wafer was used as a back gate electrode. Thermal oxide of 100 nm was grown as a gate dielectric. The S/D were then produced using the PND technique. Instead of using pentacene precursor as used in previous chapters, TIPS CFP (triisoprophylsilylethynyl cata-fluoro-pentacene) was used

as a p-type semiconductor material. TIPS CFP has been demonstrated to show high mobility due to its high tendency to crystallize upon solvent evaporation [10]. After the S/D sintering step, the S/D electrodes were treated with PFBT (pentafluorobenzenethiol) to form good contacts with the TIPS based materials [11]. PFBT was deposited in an ethanol solution with 10mM concentration, followed by an ethanol wash step. The transistor was then completed by inkjet printing TIPS CFP dissolved in a cosolvent of dichlorobenzene:dodecane (3:1 vol. ratio) to cover the S/D. The co-solvent has been reported to suppress the coffee ring effect and thus allow the deposition of a more uniform film [12]. As described in Chap. 2, the printing of TIPS CFP was done at the substrate temperature of 60℃ to facilitate the pinning of the drop and the crystallization simultaneously. Figure 4.11(c) and (d) shows the transfer and output characteristics of the printed transistor. The transistor showed a field effect mobility of 0.12 cm^2/Vs, and an on/off ratio of 10^7. No contact barrier was observed, attesting the well-behaved nature of this highly-scaled device produced by the novel PND technique.

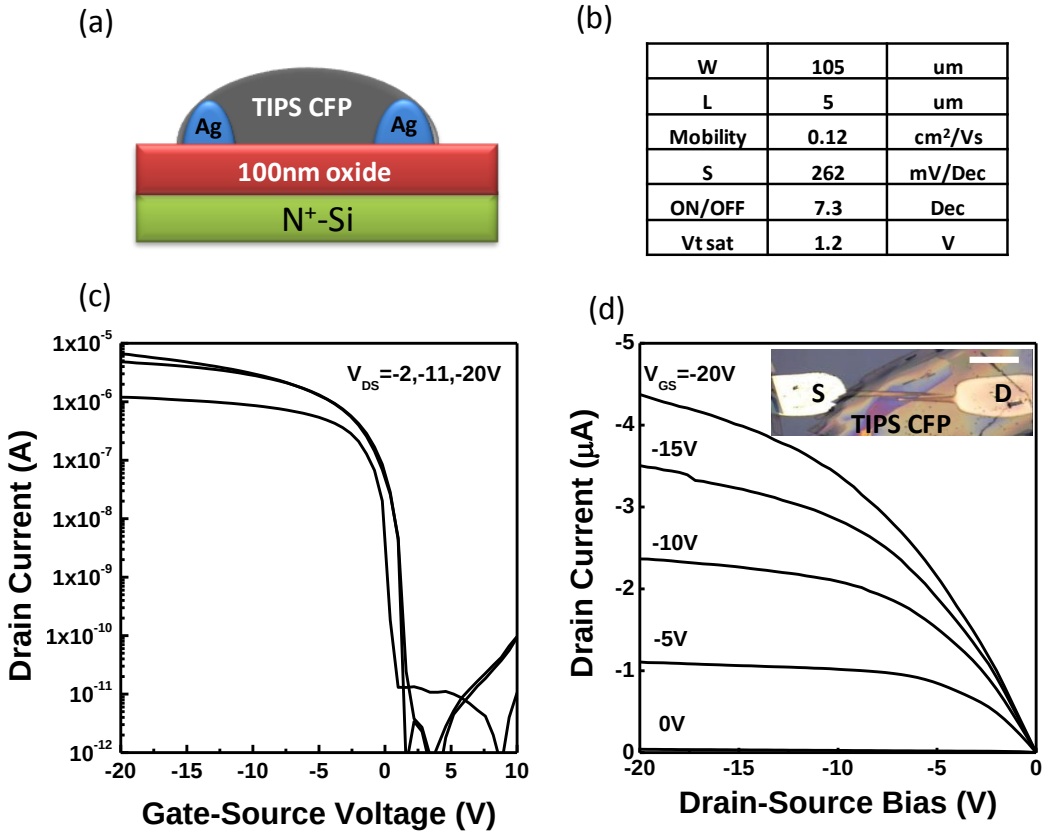

Figure 4.11 (a) Cross-sectional schematic of a printed transistor fabricated on a heavily doped silicon wafer with a 100 nm thermal oxide on top (b) A table with the transistor parameters (c) transfer and (d) output characteristics of the transistor. The scale bar represents 100 μm

4.3.2. Fully printed transistor using PND S/D

To demonstrate the minimization of the gate-to-S/D overlap capacitance using PND S/D, a fully-printed transistor was then fabricated. The process started with an inkjet-printed silver line with a 30 μm drop spacing, resulting in a line with 50 μm width and 170 nm height. After the sintering step, PVP was then inkjet printed perpendicular to the gate line to form a dielectric

layer. After the cross-linking step, two silver pads were then printed on both sides of the gate for the subsequent PND process. S/D electrodes were then dragged out using the printed silver pads to form two close spacing lines. A soft tip with a point radius 0.35 µm was used here (Micromanipulator model 7s, Tungsten tip, Nickel shank) in order to minimize the force applied to the PVP surface. After the S/D sintering step, PFBT was then deposited as above. TIPS CFP was then inkjet-printed on the channel region to complete the transistor fabrication. Figure 4.12(a) and (b) shows the transistor top-view before the printing of TIPS CFP. 20 transistors with channel length from 3 to 8 µm were produced with a median channel length of 6 µm. Figure 4.12 (c) and (d) shows the transfer and output characteristics of the printed transistor, respectively. Although a fully-printed transistor with PND S/D was successfully demonstrated, the mobility was significantly lower than the similar devices printed on oxide dielectrics using silicon back-gates. This could be the result of much smaller PND S/D lines, originally aiming to reduce the overlap capacitance. The smaller S/D lines are highly resistive, and therefore can introduce a high contact resistance between TIPS CFP and S/D. The output characteristics, which show evidence of high contact resistance at high gate-bias, support this explanation. This transistor structures also suffers from low yield, due to non-conductive S/D lines. As previously discussed, although the yield of the PND lines can be improved by scaling down the pad sizes, it is challenging to precisely drag two lines from small pads and form a close spacing. Therefore, these transistors are not suitable for highly-scaled dimensions.

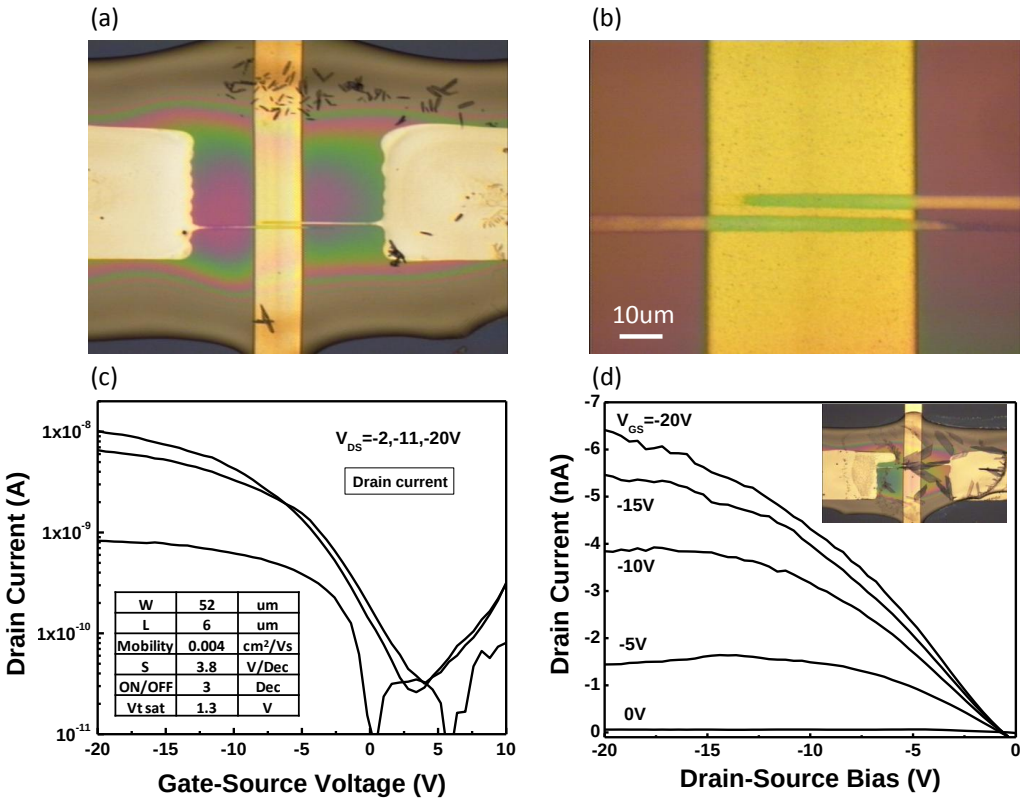

Figure 4.12 (a) Optical micrograph of a fully-printed transistor with PND S/D. (b) A higher magnification image showing the close spacing of the PND S/D as well as minimized gate-to-S/D overlap. (d) transfer and (d) output characteristics of the printed transistor. Inset of (d) shows the optical micrograph of the transistor with printed TIPS CFP on top.

4.4. Fully printed transistors using PND gate electrodes

Fully printed, highly-scaled, p-type bottom-gate bottom-contact transistors were then demonstrated using PND gate electrodes. The printing process flow is similar to the previous chapter except that the downscaled gate lines were produced by the PND technique. An N-type silicon wafer with thermally grown oxide of 1 µm was used as an underlying mechanical substrate. Silver nanoparticle ink (Suntronic U5603) was used to print the large pads for the PND process. The silver pads were then dragged using a tungsten tip with 2.4 µm point radius at 100 µm/s to create a long gate line. The gate electrode was then sintered at 150 ℃ for 20 minutes. Baseline PVP ink was printed atop the gate and cross-linked at 200 ℃ for 10 minutes. Five nozzles were used simultaneously to print the PVP layer with a drop spacing of 30 µm, resulting in a dielectric thickness of 110 nm. Silver ink was then printed to form source and drain electrodes with a drop spacing of 20 µm. This was followed by a sintering step identical to that used for the gate electrode. The S/D electrodes were then treated with PFBT to form good contacts with the TIPS CFP. The transistor was then completed by inkjet printed TIPS CFP dissolved in a cosolvent of dichlorobenzene:dodecane (3:1 vol. ratio) to cover the S/D. All inkjetting was performed using a Dimatix DMP-2800 printer with a jetting frequency of 2 kHz except the TIPS CFP, which was inkjet printed using a custom-built printer with a Microfab nozzle (80 µm orifice).

The cross-sectional structure of a single printed transistor is shown in Figure 4.13(a) and an optical micrograph of the transistor is shown in Figure 4.13(b). Figure 4.13(c) and (d) show the transfer and output characteristics of the printed transistor, respectively. The transistor shows a mobility of 0.05 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of almost 10^5 as outlined in the inset table of Figure 4.13(d). Statistical data was measured from 20 separate transistors; the summarized statistics are listed in Table 4.1.

	Mobility	On/Off ratio	Threshold voltage	Sub-threshold swing
Unit	$cm^2\ V^{-1}\ s^{-1}$	Decade	V	$V\ decade^{-1}$
Average	0.017	4.48	1.75	1.1
Standard deviation	0.02	0.67	1.67	0.49

Table 4.1 Statistical results as measured from 20 separate printed transistors.

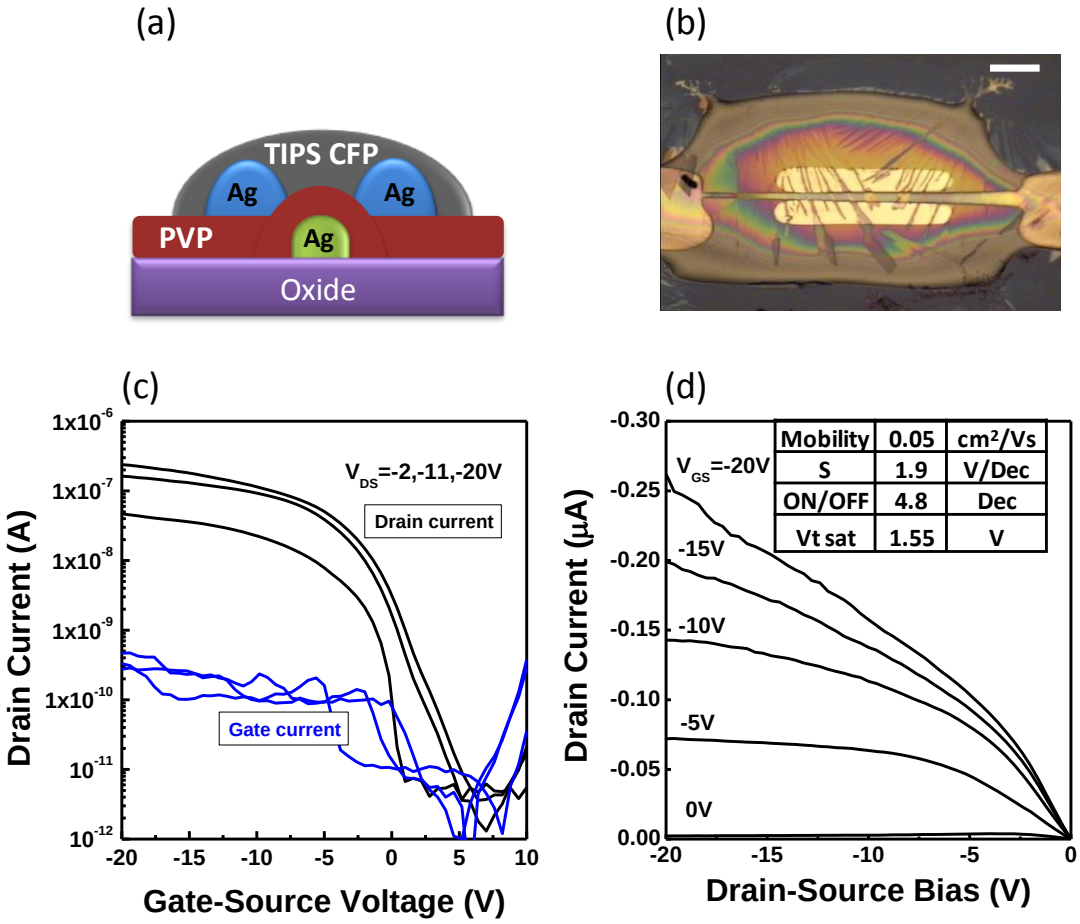

Figure 4.13 (a) Cross-sectional view of a fully printed transistor. Chemical structure of TIPS CFP is also shown. The transistors and inverters were fabricated on 1 µm oxide wafers (b) the optical micrograph of the fully printed transistor. The scale bar represents 100 µm. (c) transfer characteristics with the gate current (d) output characteristics of the transistor. The channel length of the transistor is 14 µm.

The mobility obtained in this work is similar to previous work using TIPS CFP [10]. This indicates that TIPS CFP also forms good contacts with PFBT treated silver electrodes. However, the output characteristic still show evidence of contact resistance at high gate bias, implying the contact can be further optimized by an alternative treatment. The on/off ratio is not as high as devices fabricated using thermal oxide gate insulators due to increased gate leakage current through the printed PVP film; however, in general, the obtained electrical characteristics are consistent with other reported results using PVP. The threshold voltage of 1.55 V and the average sub-threshold swing of 1.1 V/Dec are also similar to previous work using a complete solution process [13], indicating the combination of TIPS-based pentacene and PVP can yield a good channel interface. The channel length and width are 14 µm and 243 µm respectively. Note that the channel width was measured from the effective coverage of the printed TIPS CFP on the channel.

4.5. Fully printed inverters

In order to demonstrate the speed improvement of the transistors with down-scaled gate lines, inverters were then printed for the testing of propagation delay. Following the inverter discussion in Chap. 3, inverter structures consisting of one pull-up transistor and one diode-connected pull-down transistor were chosen. The β ratio (the channel width ratio of the pull-up transistor to the pull-down transistor) was designed to be 1 to maximize the switching speed of the inverter. A four-stage inverter chain was printed for characterizing propagation delay.

An N-type silicon wafer with thermally grown oxide of 1 µm was still used as a substrate. The gate electrodes were produced by the PND technique with a dragging speed of 100 µm/s. PVP dielectric was printed to cover both gate lines, followed by a cross-linking step. Dewetting of the printed PVP film was observed between the PND electrodes as shown in Figure 4.15(a) and (b). This is due to the fact that PVP preferentially wets silver lines over oxide. Nevertheless, the overall printed PVP film was smooth and conformal. The RMS surface roughness of the PVP film was 2.6 nm, as measured by AFM. The S/D electrodes and the interconnection were then printed to align to the gate, followed by a sintering step. The baseline pentacene ink was then printed using a Microfab inkjet nozzle to deposit a drop volume of 800 pL (10 drops). The pentacene was then annealed at 150 ℃ for 25 minutes. Figure 4.14(a) and (b) shows the transistor characteristics with a poor mobility, poor sub-threshold slope, and a significant contact barrier. The degraded performance was later diagnosed to be caused by degraded pentacene precursor material.

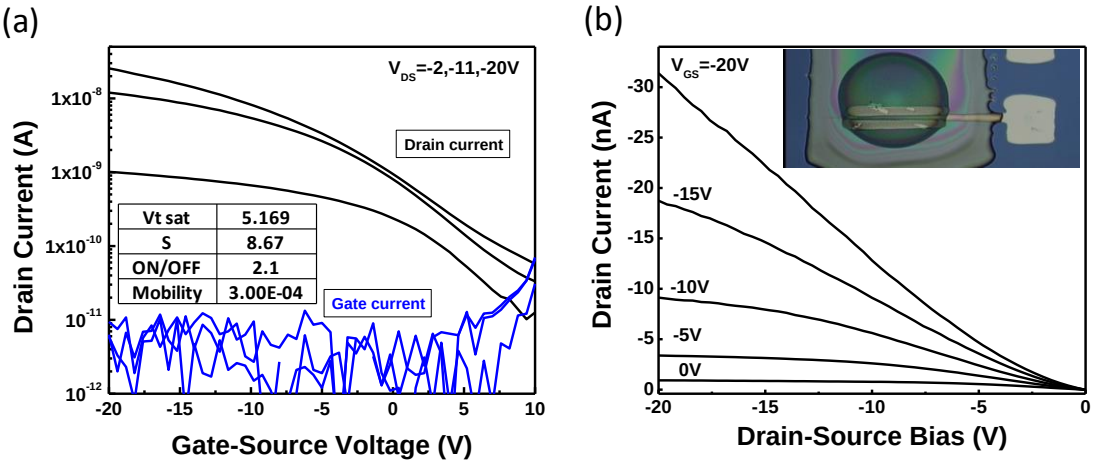

Figure 4.14 (a) transfer characteristics with the gate current (d) output characteristics of the transistor. The channel length of the transistor is 15 µm.

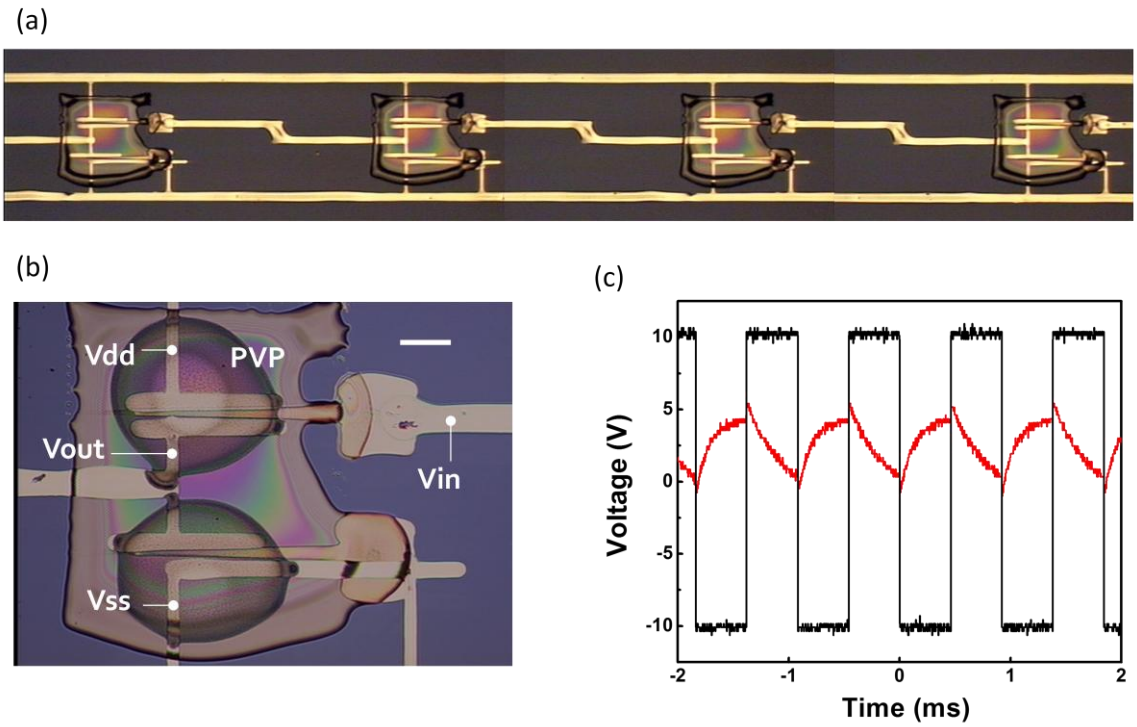

Figure 4.15 (a) Optical micrograph of a four-stage inverter chain. (b) Optical micrograph of a printed inverter with pentacene precursor on top. (c) Transient response of the inverter.

As a result, although the channel length was successfully scaled down to 15 µm, implying a potential ten-time-faster switching speed comparing to the result in Chap. 3, the measured switching speed was lower due to a much lower mobility. Figure 4.15(a) shows the printed four-stage inverter chain. The switching speed was measured by providing a 20 Vp-p square wave input to the first stage, and the propagation delay between the input and output of the second stage was extracted. This setup was selected to match the circuit simulation conditions. Unfortunately, the noise margin of each inverter was too small, hence the square wave failed to propagate to the output of the second stage. Therefore, the delay between an input square-wave and the output of first-stage was measured. As shown in Figure 4.15(c), the voltage swing is only 5 V with an input of 20 Vp-p. The measured propagation delay is 1.45 ms, corresponding to a 690 Hz switching speed. The poor performance is expected from the degraded mobility, despite the use of highly-scaled transistors.

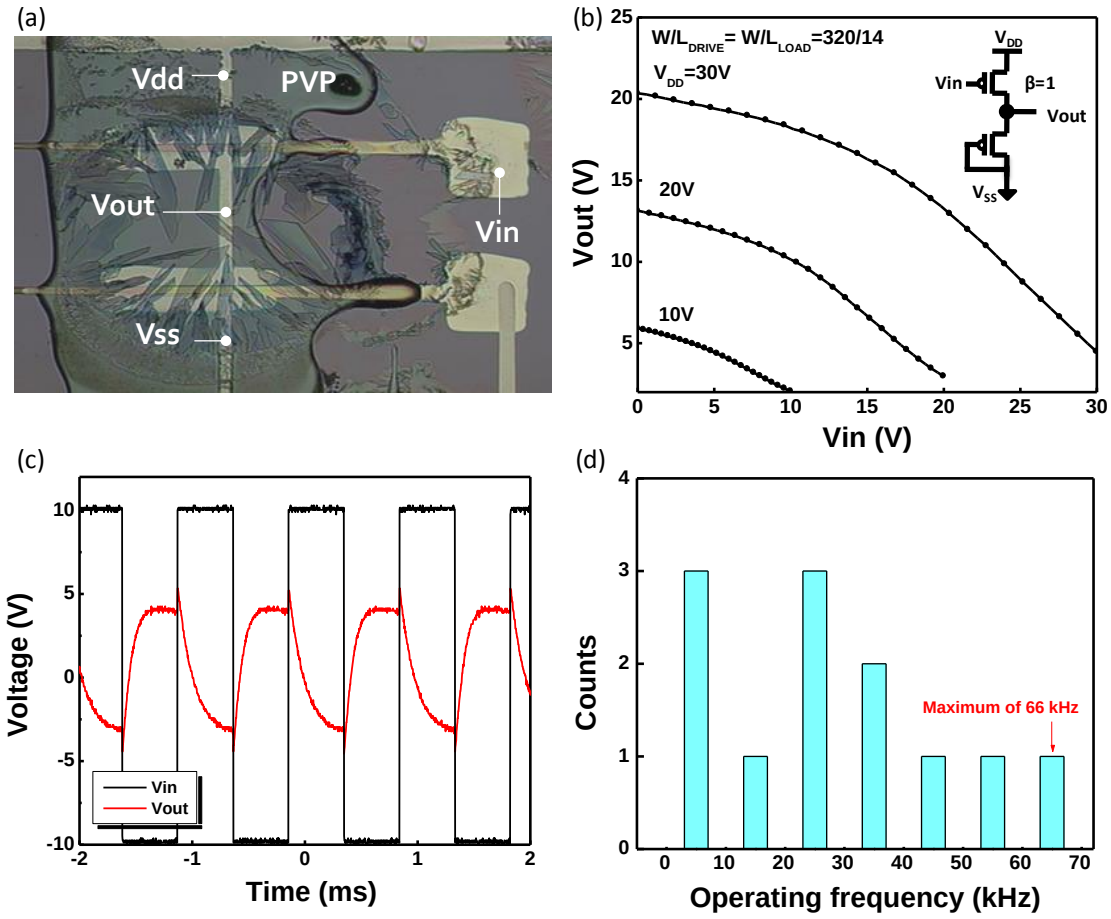

Figure 4.16 (a) Optical micrograph of a fully printed inverter. TIPS CFP was printed in the form of a big drop to cover both transistor channels. The scale bar represents 100 µm. (b) Voltage transfer characteristics of the printed inverter. Inset shows the equivalent circuit of the inverter. (c) Transient characteristics of the printed inverter showing a 1 kHz and 20 V_{P-P} square wave input. The inverted output waveform was measured at a fan-out of 6. (d) Distribution of the maximum operating frequency of 11 printed inverters, showing best-case operation at 66 kHz at the fan-out of 1. The variation is primarily due to variations in coverage and resulting mobility of TIPS CFP.

To achieve a better mobility to demonstrate the speed improvement by scaling, TIPS CFP was then used. Prior to printing of TIPS CFP, the S/D was treated with PFBT to form a good contact to TIPS CFP. TIPS CFP was then inkjet printed with the drop size controlled to cover the two transistors. As shown in Figure 4.16(a), higher evaporation at the drop edge causes the TIPS CFP to crystallize from the perimeter towards the center, resulting in symmetric coverage of both transistors. The printed TIPS film showed a large crystallize size, which is beneficial for obtaining high mobility, but also resulted in device-to-device variation. Fortunately, the uniformity can be improved in the future by using a polymer-small molecule blend while also maintaining high performance [14]. The transistor characteristics were similar to those shown in Figure 4.13 and Table 4.1. Figure 4.16(b) shows the voltage transfer characteristics (VTC) and the equivalent circuit of the inverter with a β ratio of one. The inverter shows a significant improvement in the voltage swing due to the use of transistors with better sub-threshold slope. Figure 4.16(c) shows the transient characteristics of the inverter. To measure the inverter transient

output, an Agilent 4156C was used to provide 20 V and ground. An input square wave of 1 kHz was provided by an Interstate Electronics Corporation F34 function generator. The output was buffered by an operational amplifier Burr Brown OPA602BP and the waveform was measured using an Acute DS-1202 Oscilloscope. Due to the extra parasitic capacitance from the bottom silicon wafer, the inverter has a fan-out of 6 (C_{OUT}/C_{IN}=6). The average propagation delay from Figure 4.16(c) is 90 µs, indicating that the inverter at a fan-out of 1 will have a propagation delay as low as 15 µs. The propagation delay corresponds to an operation frequency of 66 kHz. Figure 4.16(d) shows the histogram of the switching speed over 11 measured inverters. Clearly, the speed improvement is achieved despite the relatively low mobility of the semiconductor used here, attesting to the beneficial impact of PND-based scaling.

To further verify the speed improvement, the switching speed was then calculated using the following equations:

$$Max.frequency = \frac{1}{intrinsic\ delay} = \frac{1}{R_{ON} \cdot C_{load}}$$

The load capacitance is assumed to be identical to the input capacitance, as is the case for an inverter chain with fanout of one. Therefore, C_{load}=C_{in}:

$$R_{ON} \cong \frac{V_{dd}}{I_{dsat}} = \frac{V_{dd}}{\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{dd} - V_T)^2} \cong \frac{2}{\mu C_{ox}\frac{W}{L}V_{dd}}$$

$$C_{load} = C_{gs} + C_{ds} = C_{ox}WL + C_{ox}WL_{overlap}$$

where $L_{overlap}$ accounts for the total overlap from gate-to-S/D. The other symbols have their typical meaning. By substituting R_{ON} and C_{load} in the first equation:

$$Max.frequency = \frac{\mu V_{dd}}{2L(L + L_{overlap})}$$

The maximum frequency can then be determined using the average mobility of 0.02 cm^2/V-s, V_{dd} of 20 V, L of 14 µm and $L_{overlap}$ of 5 µm. This gives a maximum operating frequency of 75 kHz which is in good agreement with the measured frequency results.

4.6. Summary

In this chapter, we have developed and demonstrated a new technique that provides an alternative low-cost solution to create highly-scaled printed features. Using a combination of inkjet printing and mechanical pen dragging, we demonstrate features as small as 5 µm while exploiting the benefits of multi-nozzle inkjet printing. Using this technique, we have successfully demonstrated highly scaled transistors and inverters with sufficient performance for the realization of the low-cost electronics. The performance can be expected to improve by further scaling down. Therefore, in the next chapter, we will discuss the approaches to achieve sub-micron inkjet printed transistors.

4.7. References

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Chapter 5 Inkjet-Printed, Self-Aligned Transistors Operating >1 MHz

5.1. Introduction

In the previous chapter, we successfully demonstrated printed gate lines as narrow as 5 µm using a novel print-and-drag printing technique [1]. Unfortunately, the self-split printing techniques introduced in Chap. 3 have not been proven to be applicable to a gate linewidth under 10 µm, so such advances in linewidth do not result in commensurate switching performance improvement. Therefore in this chapter, we introduce and demonstrate a novel self-aligned (SA) printing process that can successfully align the S/D to gate lines as narrow as 2.75 µm, while also producing channel lengths as small as 200 nm to 2.75 µm. With such highly scaled dimensions, we demonstrate, for the first time, printed organic transistors operating at 1.6 MHz. These are, to the best of our knowledge, by far the fastest organic transistors fabricated without any lithography and vacuum processing.

5.2. Highly-scaled PND lines

As discussed in Chap. 4, PND lines can be scaled down by using a smaller tip radius. In addition, the printed pads need to be scaled down accordingly to minimize the hydrostatic pressure at the line-pad boundary. However, dragged lines under 10 µm still show a poor yield ~25%, due to the use of inks formulated using relatively large nanoparticles. Therefore, in this chapter, a commercial gold ink (Harima NPG-J) with average nanoparticle size of 5 nm will be used to achieve high yield PND lines under 10 µm.

Corning 1737 glass was used as the substrate for this work. The glass substrates were cleaned by rinsing with DI-water, acetone and IPA, followed by a 10 minute UV ozone treatment. After initial cleaning, lines were printed using the PND technique introduced and discussed in Chap. 4 [1]. First, contact pads were inkjet printed using Dimatix DMP-2800 10pL heads with the Harima gold ink; second, the pads were dragged using a probe tip (Cascade PTT-24-25, point radius 2.4 µm) in a single pass to produce small features as illustrated in Figure 5.1(a). Unlike the results in Chap. 4, where small radius tips were used to create small features, large tips were used here. This is due to the fact that the lines produced by small radius tips are typically too short. Short lines can result in difficulties in the subsequent alignment. As a result, a large radius tip is preferred here to produce a longer line. Furthermore, we have found that small features can also be produced by dragging at much higher speed. As shown in Figure 5.1(b), although a wider line-pad junction (W_B) is observed, linewidth shrinks towards the line-tip rapidly, resulting in a highly scaled feature. A dragging speed of 10000 µm/s was used here, significantly faster than the typical speed of 200-1000 µm/s demonstrated in Chap. 4. High speed dragging can also enhance the throughput of the process. After the PND process, the lines were then sintered at 230℃ for 30 minutes. The lines shown in Figure 5.1(a) have an average linewidth of 9 µm (measured at the line tip where the transistors will be fabricated). The lines are 100% conductive, significantly surpassing the results in Chap. 4. This also attests to the benefits of using a small nanoparticle ink.

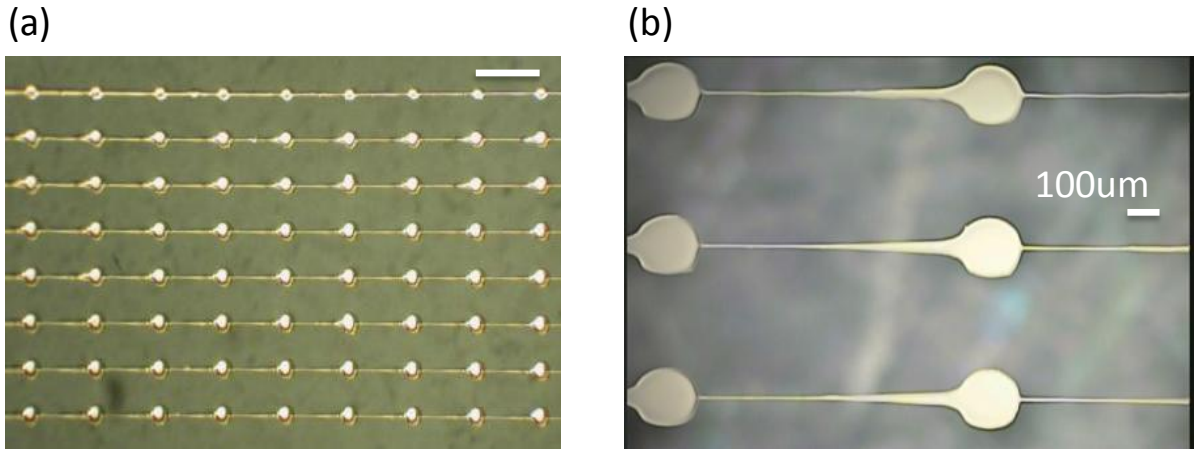

Figure 5.1 (a) Optical micrograph of the PND line array. The scale bar represents 1 mm. (b) Optical micrograph of the PND line array with higher magnification.

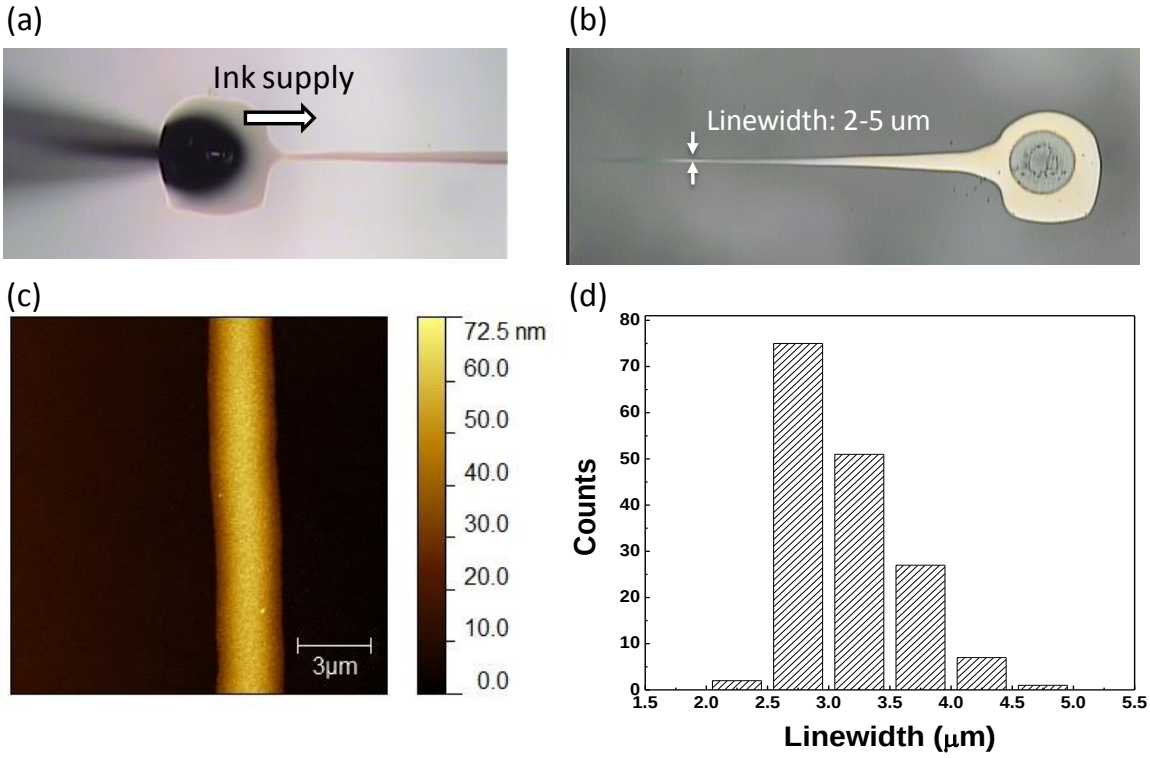

Figure 5.2 (a) Optical micrograph illustrating the ink flow from the pad toward the dragged line (b) Optical micrograph of a down-scaled PND line (c) AFM image of a PND gate line showing a line tip with a uniform linewidth of 2.75 μm (d) Histogram of the PND line width. The linewidth was measured at the line-tip.

While 9 μm lines are attractive and sufficiently small for demonstrating transistors with highly-scaled dimensions, the lines are expected to be scaled down further. The pads were printed originally with a pitch equal to or smaller than the length of the PND lines in order to

confirm whether the lines were conductive. However, as shown in Figure 5.2(a), when the lines were dragged out and reached the adjacent pad, an ink-flow supplied from the adjacent pad was observed during monitoring of the process. Consequently, this resulted in an increase of the ink volume at the line-tip. Therefore, the line became wider due to this ink flow. To suppress this effect, the pads were then printed with larger pitch to avoid the overlap between lines and pads. As a result, a smaller linewidth was achieved as the small features at the line-tip were preserved without being perturbed by the ink flow (Figure 5.2(b)). Smaller PND lines were therefore produced with this optimization. Figure 5.2(c) shows an AFM image of a PND line-tip with a uniform linewidth of 2.75 µm and a smooth surface with RMS-roughness of 6.27 nm. Figure 5.2(d) shows the histogram of the linewidth measured from 160 lines, attesting to the robustness of this technique.

5.3. Scaling down of PVP

Scaling down of the channel length requires commernsurate downscaling of the dielectric thickness in order to achieve good electrostatic control of the channel. For a channel length of L, the dielectric thickness needs to be less than αL to suppress short channel effects, where α is in the range of 0.2-0.5 [2]. Our baseline back-gate transistors with a spin-coated pentacene precursor and an oxide thickness of 100 nm showed well-behaved transistor characteristics without severe short channel effects when scaling down to 1 µm channel length (see Appendix A). This implies that 100 nm thick PVP should be sufficient for printed transistors to be scaled down to 1 µm channel length, as PVP has a similar dielectric constant to silicon dioxide [3].

Capacitors with PVP dielectric sandwiched by printed gold lines were made to characterize the leakage and breakdown of PVP with various thicknesses. Bottom electrodes were printed using the PND technique to form narrow gold lines. To obtain a smooth and uniform PVP film across all substrates, spin-coated PVP was used as the gate dielectric. 7wt% of PVP dissolved in propylene glycol methyl ether acetate with 0.75wt% of cross-linker poly-(melamine-co-formaldehyde) was spin-coated on the gold lines as the gate insulator. The thickness was controlled by spin-coating at the following speeds: 1000, 2000, 4000 and 6000 rpm, resulting in the following thicknesses: 290, 230, 150 and 110 nm respectively. All PVP films were cross-linked at 180℃ for 30mins. Top electrodes were inkjet printed using Harima gold, followed by a 180℃ and 30mins sintering step. An optical micrograph and a cross-sectional diagram of the capacitor are shown in Figure 5.3(a). The current density as a function of electric field from the measurement of 40 capacitors is shown in Figure 5.3(b). With the 150 nm thick PVP, only 4 capacitors showed clear breakdown behavior with an abrupt increase of the current, indicating the high quality of the PVP layer (note that many organic dielecrics do not show clear hard breakdown; rather, the current flow increases due to hopping as traps are generated at high fields). To statistically illustrate breakdown versus film thickness, the electric field corresponding to a passed current density of 1 µA/cm^2 was chosen to be the breakdown field (if the abrupt current-increase was not observed), as suggested by a conventional definition [4]. The cumulative breakdown for various thicknesses was then plotted in Figure 5.3(c). Consistent intrinsic breakdown fields of ~2.5MV/cm across all thicknesses were achieved. The high yield is attributed to the smooth gate surfaces and the uniform PVP layer. The dielectric constant as a function of frequency was then characterized to estimate the speed limit. Figure 5.3(d) shows that the PVP is suitable for high speed operation up to the range of MHz, despite a slightly dielectric constant drop above 1MHz.

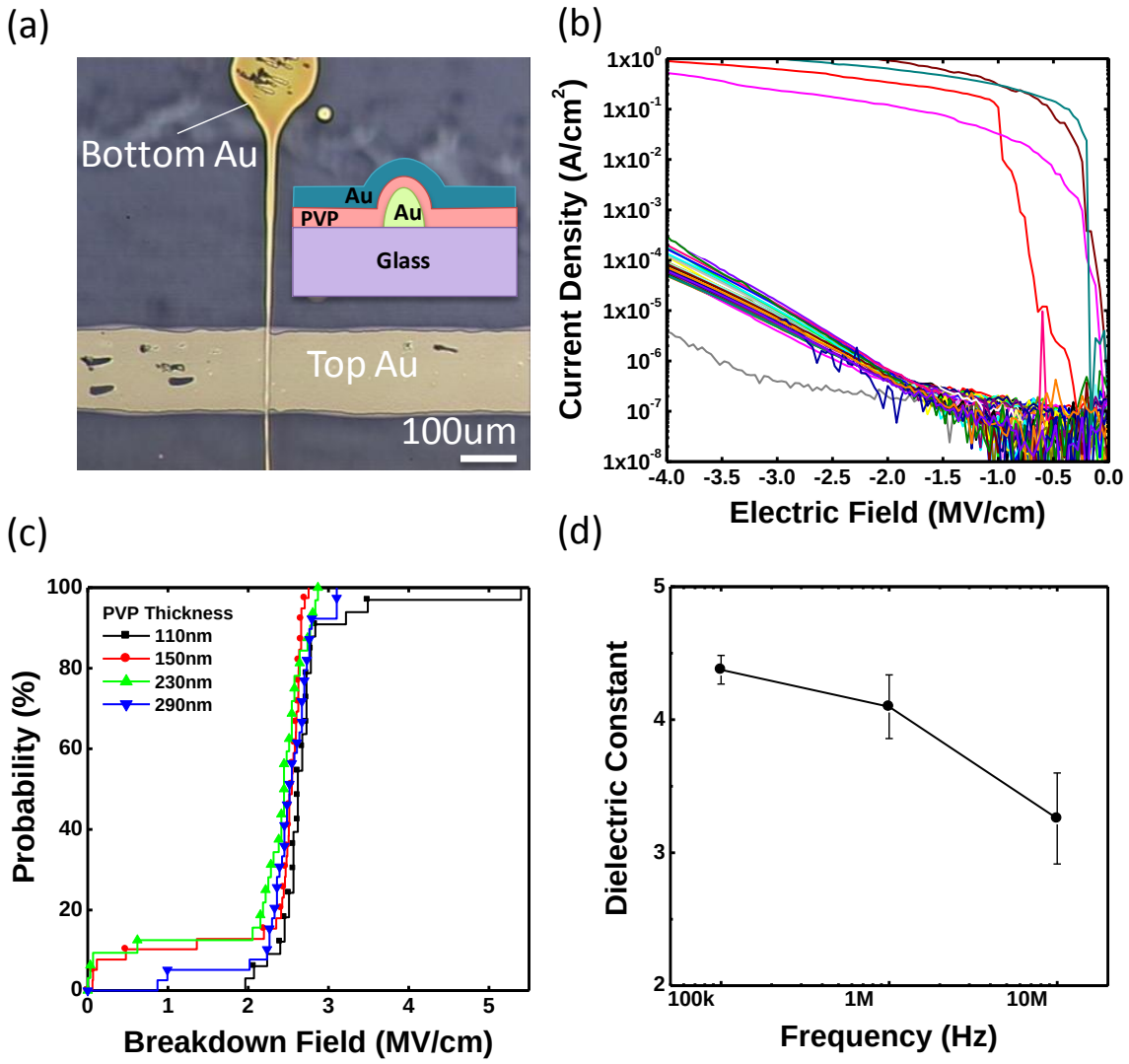

Figure 5.3 (a) Optical micrograph of a printed capacitor with top and bottom gold-electrodes. The inset shows the cross-sectional diagram of the capacitor (b) Leakage current of 40 printed capacitors. The PVP thickness is 150nm (c) Cumulative plot of the breakdown field of the printed capacitors with various PVP thicknesses (d) Dielectric constant of PVP as a function of small signal frequency.

5.4. Transistors with few microns channel length

Having a successfully scaled gate lines and a robust dielectric, a printed transistor with highly-scaled channel length can potentially be demonstrated. Gate lines as small as 2.75 µm were achieved previously, indicating a channel length of 2.75 µm can be produced by applying the self-aligned S/D process as introduced in Chap. 3. However, as discussed in Chap. 3, the self-alignment requires dewetting of the ink from the channel surface, leaving some residues that can potentially deteriorate the mobility of the semiconductor. Therefore in this chapter, we have developed a new self-alignment technique to achieve minimum channel length and gate-to-S/D overlap, while avoiding any ink residue on the channel surface.

5.4.1. New self-alignment process

Here, a novel self-aligned printing process is described which utilizes the hydrophobicity of both the gold ink and the PVP surface. Harima gold ink exhibits a total wetting behavior on the PVP surface. As a result, printed drops on PVP will advance the contact line until the solvent evaporates and forms a coffee ring. Using this characteristic, two drops of gold ink were first printed at some distance from the gate line, as illustrated in Figure 5.4(a). Then, the drops started to expand on the PVP and the drop edges pinned to the gate edges after 3 minutes. Figure 5.4(b) and (c) clearly show the pinning of the drops (the mechanism that causes the drop-pinning will be discussed below).

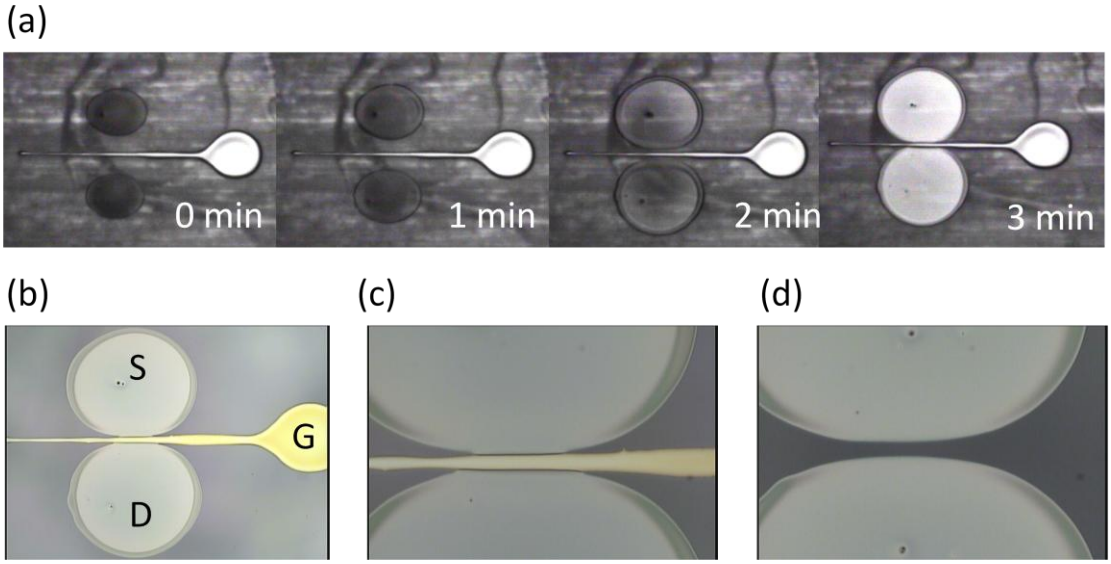

Figure 5.4 (a) Time-lapse photographs showing the advancing of the drops toward the gate line. (b) Optical micrograph of the self-aligned S/D. (c) High magnification micrograph showing the pinning of the drops at the line edges. (d) Two printed drops without the presence of the gate line underneath the PVP.

The self-alignment shown here is in reverse to the technique introduced in Chap. 3; the drops advanced towards the line instead of rolling off the lines. Therefore, the channel surface is expected to be clean, as no ink-channel contact has occurred. The two drops can then be used as S/D electrodes after a sintering step. Due to the coffee ring effect, the S/D was expected to be conductive only at the periphery. Unfortunately, as illustrated in Figure 5.4(c), the two drops show an absence of the coffee ring in proximity to the gate line. This indicates the gold nanoparticles were not accumulated near the gate line; instead, only a thin layer of material was deposited. The absence of the coffee ring near the gate line can be explained as follows: When the two drops were approaching each other, the coffee ring was formed at the periphery of both drops, as shown in the 2 minutes case of Figure 5.4(a). When two drops reached a close spacing, the region between the two drops experienced an increase in equilibrium vapor pressure, to which the evaporation of both sides contributed. This could retard the vaporization of the solvent in that region compared to other locations. Consequently, the outward convection flow, which replenishes the solute was reduced, resulting in the absence of the coffee ring where the two drops are closest. To confirm that the absence of the coffee ring was not related to the gate line

underneath the PVP, two drops were printed on blank PVP without any pattern below. Figure 5.4(d) shows the result, which is similar to Figure 5.4(c), with no coffee ring formed in between two closely spaced drops, verifying that the effect was not related to the drop-gate interaction.

As a result, the region near the gate line was not conductive after the sintering step. This made the S/D unusable despite the fact that successful self-alignment was achieved. To overcome this issue, we will then print the drop on one side first to achieve a self-aligned and conductive source electrode.

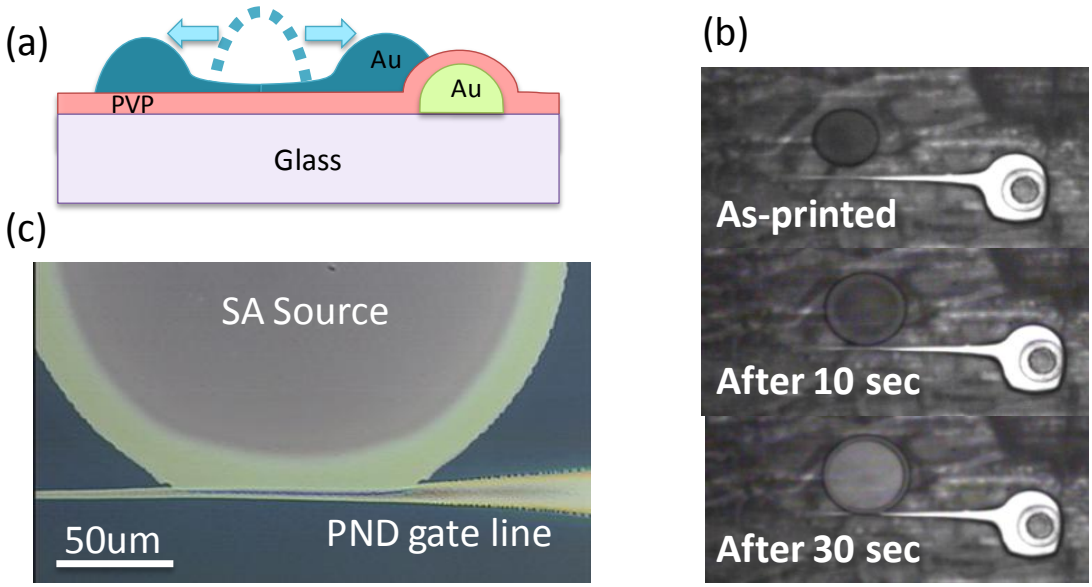

Figure 5.5 Self-alignment of the printed source electrode. (a) Schematic diagram illustrating the self-alignment process (b) Time-lapse optical micrographs captured by the Dimatix printer showing the process of printed source advancing and self-alignment to gate (c) Optical micrograph with higher magnification showing the self-alignment

As shown in the Figure 5.5(a), a gold drop was printed on one side of the gate line. Similar to the process discussed previously, the drop expanded due to its complete-wetting characteristic on PVP. Figure 5.5(b) shows the process of the expanding drop, and a coffee ring formed during the expansion. After 30 seconds, the drop ceased the expansion and aligned to the gate. The drop was then sintered at 185℃ for 30 minutes. Figure 5.5(c) shows the optical micrograph of the pinned drop. The drop edge clearly conforms to the PND gate line, resulting in successful self-alignment. The coffee ring was also present at the drop-line boundary, indicating a conductive source electrode was achieved. The yield of the self-alignment was then determined by printing 325 devices with various PVP thicknesses. Failure of the self-alignment was defined if a complete drop-to-gate underlap was observed due to jetting instability, or if a portion of the drop flowed over the gate lines as shown in Figure 5.7(c). Interestingly, the yield becomes higher with a thinner PVP layer, as shown in Figure 5.6. An average yield of 78% was achieved, attesting to the reproducibility of the process.

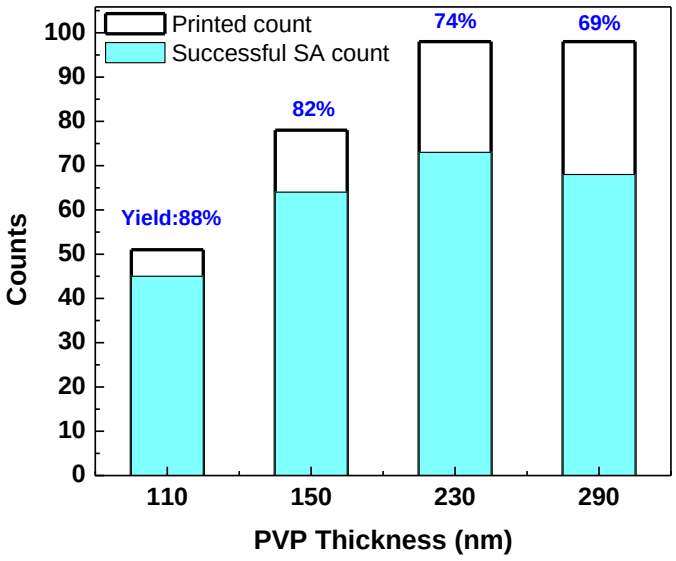

Figure 5.6 Yield of the source side self-alignment.

To better interpret the yield, two geometrical parameters A and B were defined to represent the limitation of the self-alignment, as illustrated in Figure 5.7(a). Parameter A denotes the distance between the center of the drop to the gate line. Parameter B denotes the maximum length the drop can align to the gate without the ink flowing over. Figure 5.7(b) and (c) show the examples of the successful and failed self-alignment, respectively. The data was then collected from 40 printed devices with 150 nm PVP layer, and the associated A and B values were then plotted in Figure 5.7(d). A smaller A means that the drop was printed closer to the gate, and thus resulted in a larger B. A clear boundary between the self-aligned points and the non-self-aligned points can be observed. Therefore, B_{MAX}, representing the maximum length a drop edge can successfully self-align to a gate, was then extracted from the graph. Then, the extracted B_{MAX} for each PVP thickness was plotted in Figure 5.7(e). Clearly, B_{MAX} increased with thinner PVP. This helps explain the higher yield with thinner PVP discussed previously. Larger B_{MAX} increases the tolerance of jetting instability, i.e. despite any jetting-deviation causing the drop to land closer to the gate, the drop can still self-align to the gate. The possible reason by which a thinner PVP can promote self-alignment will be discussed in the next section.

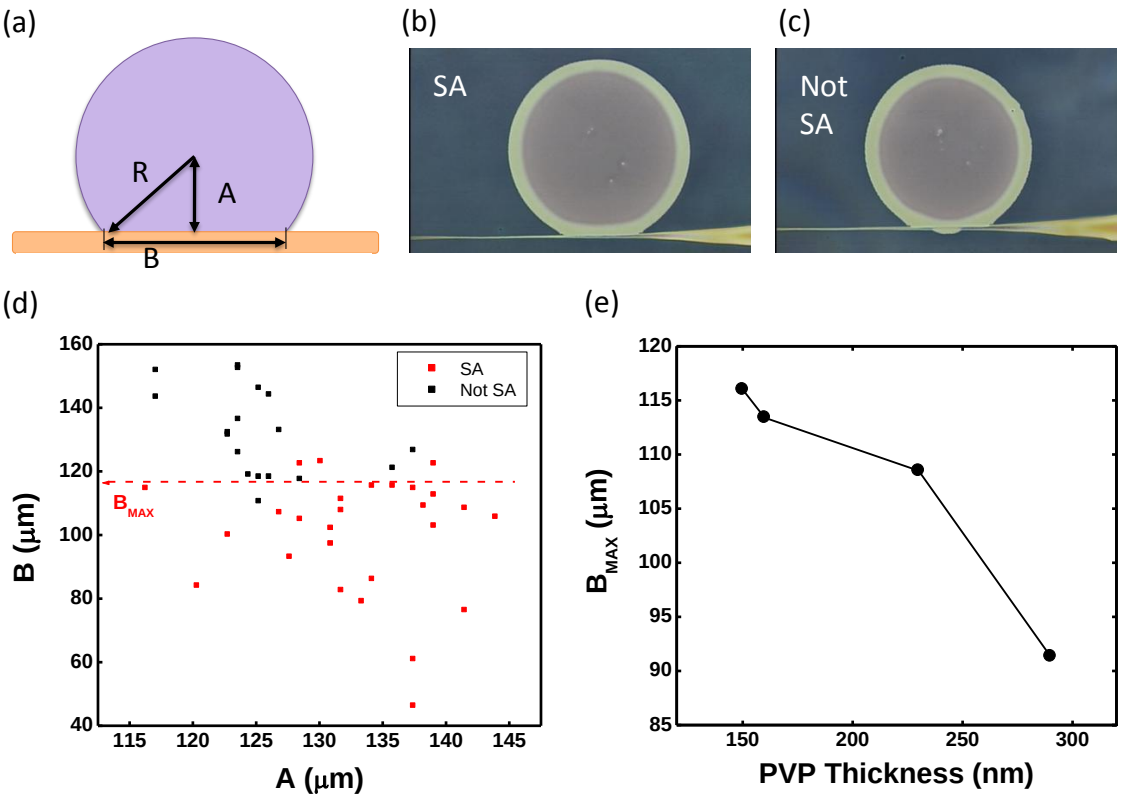

Figure 5.7 (a) Schematic diagram showing the definition of the parameters A and B. (b) Optical micrograph of the successfully self-aligned source. (c) Optical micrograph of a source with a failed alignment (d) The plot of A versus B (e) B_{MAX} as a function of PVP thickness.

5.4.2. Self-alignment mechanism

The self-alignment achieved here is attractive for realizing highly-scaled and fully self-aligned printed transistors. However, neither the mechanism of the self-alignment introduced in Chap. 3 nor the one discovered here was clearly understood. Both self-alignment phenomena share the common mechanism of providing an energy contrast on a PVP surface, i.e. a more hydrophobic PVP on the gate to induce the roll-off of the hydrophilic silver ink; or a more hydrophilic PVP on the gate to stop the expanding of the hydrophobic gold ink. Note the self-alignment works on both hydrophilic and hydrophobic ink systems, so long as the same ink was used in both the gate and S/D. This suggests that a physical mechanism is likely to be the cause, independent of the chemical components in the PVP and both ink systems. In this regard, physical factors that can possibly govern the self-alignment will be discussed firs. AFM was used to examine the surface of PVP with a gate below. This was to verify whether a geometrical defect such as a groove was present and caused the drop to pin on the defect. Figure 5.8(a) shows a representative AFM image out of ten imaged PVP surfaces. The result clearly excludes the possibility of a geometrical defect, since the cross-sectional profile shows a smooth and continuous PVP surface.

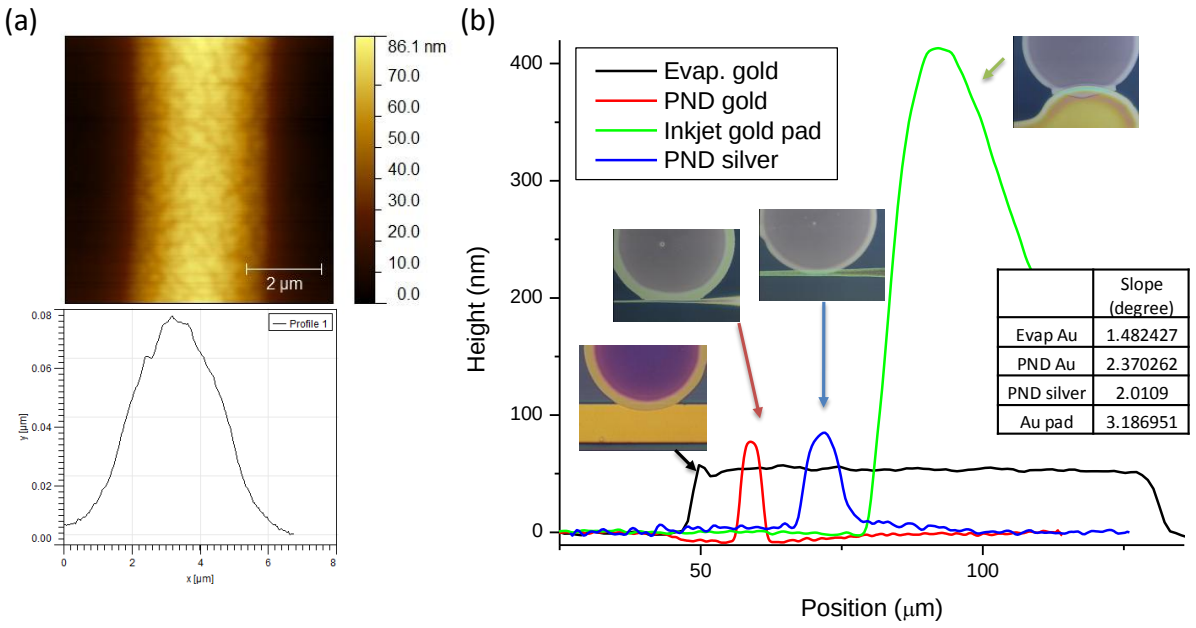

Figure 5.8 (a) AFM image of a PVP surface with a PND line underneath. The PVP thickness is 150 nm. (b) Cross-sectional profile of various electrodes. Inset table shows the side slope of various electrodes.

Another possible physical factor is the height of the gate line. Figure 5.8(b) shows a representative cross-sectional profile of various gate electrodes. Optical micrographs of printed drops on each electrode are also shown. The drop shows a self-alignment on the PND gate line, but not on the printed gold pad used for the PND process. The gold pad is 400 nm at the edge, much thicker than the PND line, indicating the height is irrelevant to the mechanism of the self-alignment. Similarly, the thicker PND silver line shows a non-self-aligned drop on top, further implying the irrelevance of the height. The side slope of the line is also listed in Figure 5.8(b). Likewise, the side slope can be determined to be irrelevant by comparing the slope of PND gold and the printed gold pad. To test whether the self-alignment originates from the surface energy contrast between the printed gold and glass substrate, a thermally evaporated gold electrode was used as a comparison, as shown in Figure 5.8(b). With an identical spin-coated PVP on the top, the self-aligned printing performed on the evaporated gold showed a zero yield from 20 devices. This concludes that the presence of the gold was not sufficient to induce the self-alignment; instead, the chemical components of the gold nanoparticle inks could play an important role, including the ligands and/or the surfactants. Detailed studies in this are currently underway.

The physical factors examined previously failed to explain the cause of the self-alignment mechanism. Therefore, the following discussion will focus on the chemical factors. The surface energy of the PVP was tested with or without the printed gold underneath. Harima gold ink was printed on the glass substrate to form discrete big pads, followed by a sintering step of 230 ℃ and 30 minutes. PVP was then spin-coated on top with various speeds to form a thickness of 130, 160 or 310 nm, followed by a cross-linking step of 180 ℃ and 30 minutes. Water contact angle was then measured on the region with and without the printed gold pads below. The results are shown in Figure 5.9.

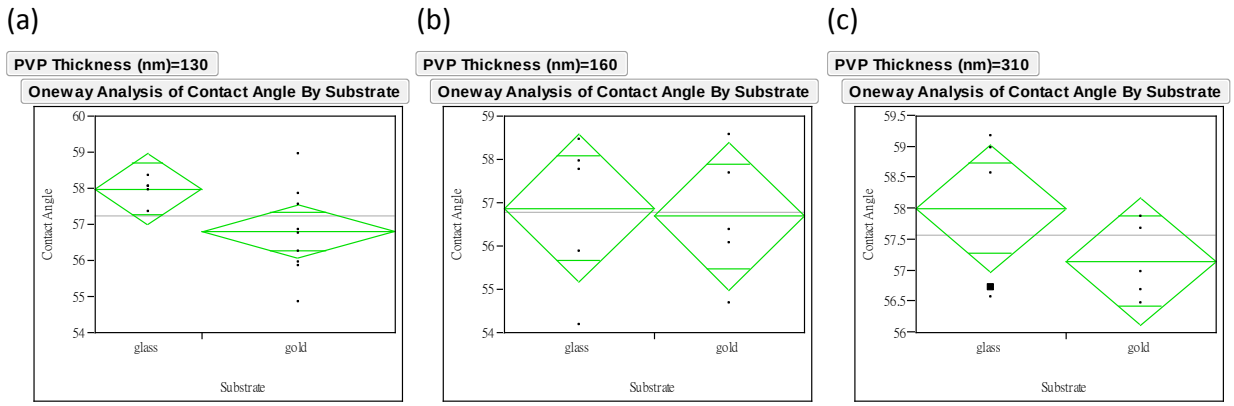

Figure 5.9 Water contact angle on PVP with or without Harima gold underneath. The PVP thickness is (a) 130 nm and (b) 160 nm and (c) 310 nm.

Although a slightly lower water contact angle was observed with the gold under the PVP, indicating a possible lower surface energy, the difference is not statistically significant. In other words, the surface energy on PVP is similar with or without the presence of printed gold below. This unfortunately contradicts the previous explanation, where the surface energy contrast was used to rationalize the self-alignment. A possibility exists that the water contact angle was measured at a much larger scale, where 2 μL of water were dropped on the PVP, covering a few millimeters of area. On the other hand, the self-alignment of the drops took place in a region of a few microns. This difference in area could cause the discrepancy of the surface energy contrast. In other words, the water contact angle measurement was possibly not a good representation of the self-aligned testing.

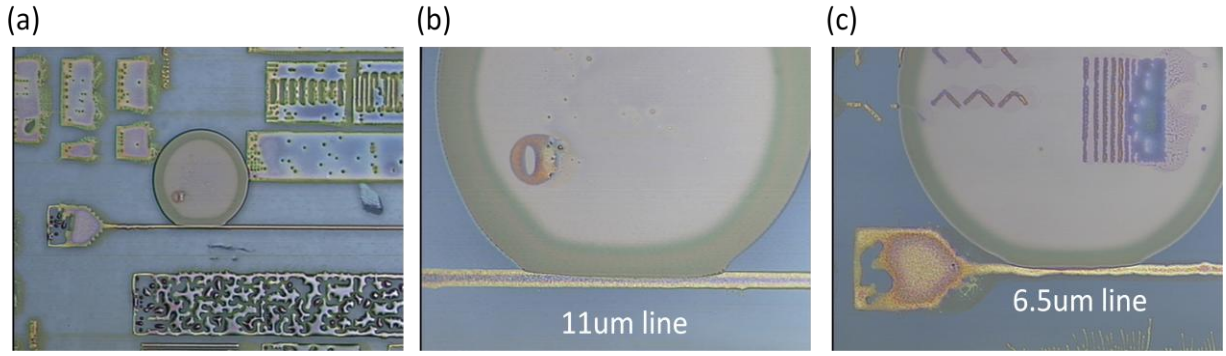

Figure 5.10 Optical micrograph of a self-aligned drop on a gravure-printed silver line (a) with lower magnification and (b), (c) with higher magnification.

To again confirm whether the gold nanoparticle or gold were the necessary component to induce the self-alignment, Harima silver ink consisting of silver nanoparticle were printed using a gravure technique. Figure 5.10(a)-(c) shows the optical micrographs of the gravure printed silver lines covered by spin-coating 150 nm of PVP. The Harima gold ink was then printed on the PVP to align to the silver line using the identical self-aligned process. The results show a clean self-alignment of the drops to the lines with both the linewidth of 11 and 6.5 μm. This concludes that the gold or gold nanoparticles are not necessary to achieve the self-alignment. Instead, the chemicals on the nanoparticles are the key parts. Unfortunately, the composition of

the Harima silver and Harima gold nanoparticles are both proprietary, and thus the details are unclear. Nevertheless, we can assume that both nanoparticles use the same encapsulant system, as they both have a similar shelf-life, sintering temperature and nanoparticle size as outlined in the data sheet [5]. Furthermore, the fact that the self-alignment can be demonstrated on lines printed using both Harima gold and Harima silver suggested the same surfactant and/or encapsulant in both inks are the crucial component. Therefore, the possible mechanism could be the diffusion of the surfactant or the encapsulant into the PVP and causing the PVP to change its surface energy locally. Note that the concentration of the surfactant in the solvent is typically low, hence the diffusion of the surfactant into a 110 nm PVP could hardly change the chemical energy of the PVP. On the other hand, the encapsulant is abundant enough to diffuse into the PVP and alter the behavior of the printed drops through a long range force [6]. This can help explaining the fact that thinner PVP is favorable for high yield self-alignment, since the long range force can be reduced with longer distance. Alternatively, the encapsulant could also diffuse through the entire PVP layer to the surface, and repel the printed drops directly. This could also help explaining the PVP thickness dependence of self-alignment yield, as thicker PVP prohibits the diffusion to the surface.

To conclude, the detailed mechanism remains unclear, although we have excluded some factors and narrowed it down to the encapsulant of the nanoparticles. The exact mechanism requires a detailed chemical analysis to discover the true cause. This was beyond the scope of this thesis. Therefore, this chapter will continue to focus on the integration of the self-aligned S/D into a highly-scaled and high speed printed transistor. Future work in understanding the self-alignment will be outlined in Chap. 6.

5.4.3. Self-aligned transistors

To continue with the self-aligned transistor process, a self-aligned drain electrode was then inkjet printed. Similar to the source side printing, two drops of the Harima gold ink were printed on the drain side, with a distance apart from the gate. This allowed the drain drop to expand and approach the gate line. In order to achieve a symmetric gate-to-S/D alignment, we have treated the PVP surface to reduce the drop expansion as well as the drop size to obtain a finer control. After the self-aligned printing of the source electrode and the sintering step, the entire surface was then modified by immersing in an IPA solution with 10mM of perfluorodecanethiol (PFDT) for 40 minutes. PFDT was reported to modify the surface to become highly hydrophobic to repulse the gold ink in a previous work [7]. After the treatment, the gold drop printed on PVP had a smaller drop size and shorter expanding distance. We then printed the drain drop starting at a distance from the gate line, and gradually approaching the gate line, as illustrated in Figure 5.11(a). This typically requires a printing of 5-7 drops and ends in proximity to the gate line. Due to the gate-drain interaction, the drain drop can pin to the gate edge to achieve the drain side self-alignment. Although the drop roll-off was also observed when the drop initially overlapped the gate line, similar to the work done in Chap. 3, the roll-off was not favorable due to the unwanted residue on the channel surface. Therefore, the printing was typically stopped when observing the drop-to-gate pinning. The resulting self-alignment is shown in Figure 5.11(b), with the edge of the drain clearly conformal to the gate line. Using this technique, the channel length was then determined by the gate linewidth.

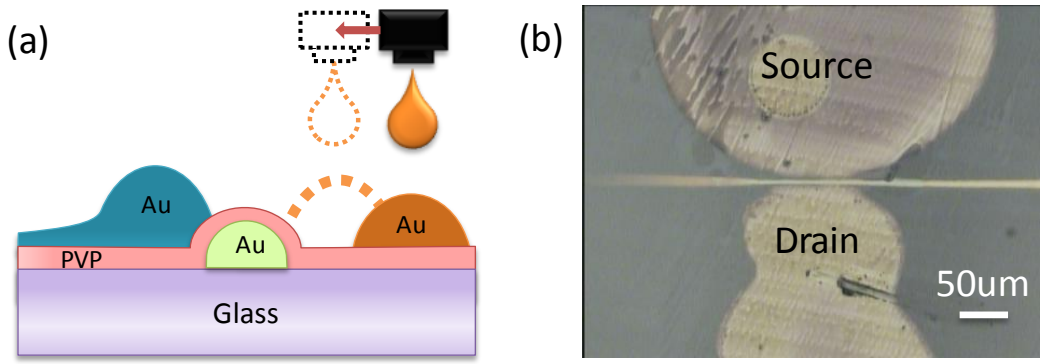

Figure 5.11 (a) Schematic diagram showing the process of the drain self-alignment (b) Optical micrograph showing the result of self-aligned drain to gate

A triisoprophylsilylethynyl (TIPS) pentacene semiconductor was then deposited using a solution shearing method similar to previous work [8]. The details of the solution shearing can be found in Appendix B. 50 µL of 1 wt% TIPS pentacene dissolved in toluene was drop-cast onto the substrate and followed by solution shearing with a parallel top substrate with CYTOP coating. The gap between the two substrates, the bottom substrate temperature and the translation velocity were 125 µm, 60℃ and 520 µm/s respectively. The solution shearing allows a large crystal to grow in one direction and is compatible with roll-to-roll processing. Figure 5.11(b) shows the printed transistor covered by a uniform layer of TIPS pentacene with the shearing direction from top to bottom. The gate contact and channel region were then isolated to minimize the leakage current.

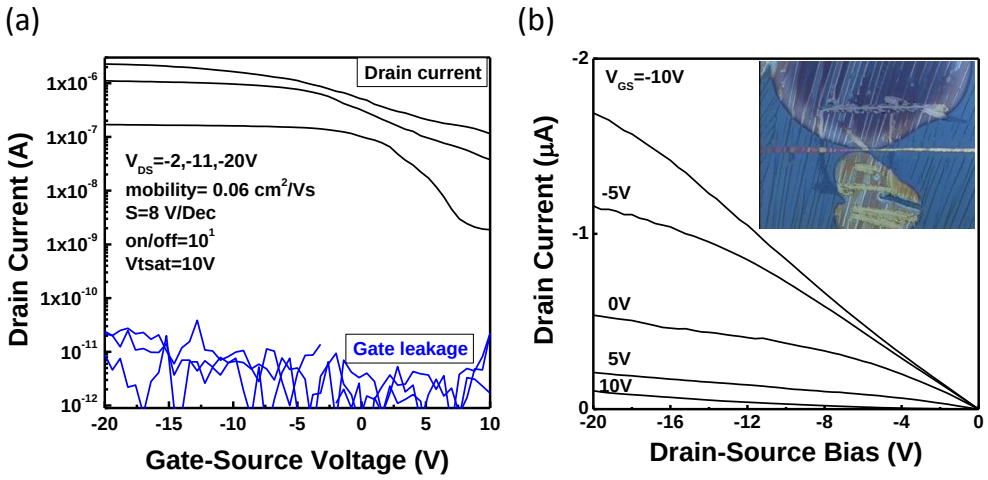

Figure 5.12 (a) Transfer characteristics of the printed transistor with a channel length of 2.75 µm and a channel width of 26 µm. PVP thickness is 150 nm (b) Output characteristics of the printed transistor. Inset shows an optical micrograph of the printed transistor.

Figure 5.12(a) and (b) show the transfer and output characteristics of the transistor, respectively. The transistor has a channel width and length of 26 µm and 2.75 µm, and a PVP thickness of 150 nm. The saturation-region mobility is 0.06 cm^2/Vs. Low gate leakage current was observed, resulting from the high quality PVP dielectric. No severe short channel effect was observed, as the saturation regions are clearly observed in the output characteristic. This agrees

with the expectation discussed previously, where a 150 nm dielectric is thinner than αL, where α is 0.2-0.5 and L is 2.75 µm here. However, off-state leakage of the transistor is high, resulting in the poor sub-threshold slope and on/off ratio. The high leakage current is possibly due to the relatively large crystal thickness of the TIPS, resulting in significant back-channel conduction. Moreover, the rigid crystal of TIPS can result in the layer growing across the S/D without contacting the channel surface. To confirm, the channel surface profile was then measured by AFM. Figure 5.13(a) shows the AFM image of a channel surface with gold S/D on PVP, covered by the TIPS deposited by the solution shearing method. The S/D was created by a mechanical-splitting technique which will be introduced in the next section. The technique can produce a closely spaced S/D with a coffee-ring-like S/D-channel boundary. Therefore, the structure with an abruptly changing height profile can be used to test the conformality of the TIPS layer on the channel. The cross-sectional profiles of scan-1, scan-2, and scan-3 are shown in Figure 5.13(b), where scan-2 and scan-1 are the horizontal profile across the S/D with and without the TIPS layer on top, respectively. The scan-3 is a vertical profile showing the film thickness of the TIPS layer. The matching profile between scan-1 and scan-2 indicates that the TIPS is conformal to the S/D-channel interface. This excludes the previous assumption where the TIPS failed to contact the channel surface at a small channel length. Scan-3 shows the TIPS with a thickness of 60 nm, matching the other assumption. The channel layer contributing to the current conduction is typically few nm [9]. Therefore the TIPS is significantly thicker than the required conduction layer. As a result, the top layer of TIPS or the back-side of the channel is poorly controlled by the gate, resulting in the high off-state leakage current through the back-side of the channel. This is expected to be improved by reducing the thickness of the semiconductor layer.

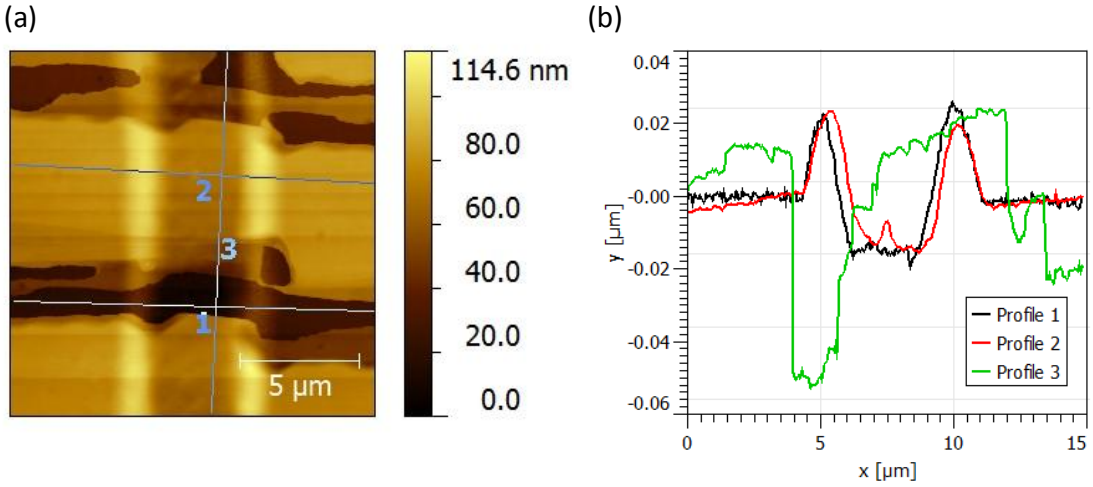

Figure 5.13 (a) AFM image of a channel surface covered by TIPS pentacene. (b) Cross-sectional profile extracted from the AFM image.

The speed of the transistor was then characterized by measuring its cut-off frequency. The cut-off frequency is defined when the current gain of the transistor is equal to one i.e. the output current is identical to the input current. The measurement setup is schematically illustrated in Figure 5.14(a). The input current was calculated using the relation of $V_{in} \times j\omega C_{in}$, where C_{in} denotes the input capacitance. The input capacitance was measured directly on the transistor using an Agilent 4285A LCR meter. The output current was measured from the quotient of the output voltage (V_{out}) and the load resistor (R). R is chosen to be ten times smaller than the

channel resistance, so that the output resistance is dominated by R. The transistor was then biased at V_{GS}=-6V and V_{DS}=-20V using an Agilent 4156C to operate at the max transconductance (g_m). An AC small signal of $2V_{p-p}$ was applied on top of the DC gate bias with varying frequency using a HP 33120A function generator. The V_{out} was then measured from the amplitude of the output signal using an Acute DS1202 USB oscilloscope. The V_{out} signal was confirmed to be in the range similar to the product of $g_m V_{in} R$, with an inverting phase with respect to the input small signal. The input and output small signal current as a function of frequency is plotted in Figure 5.14(b).

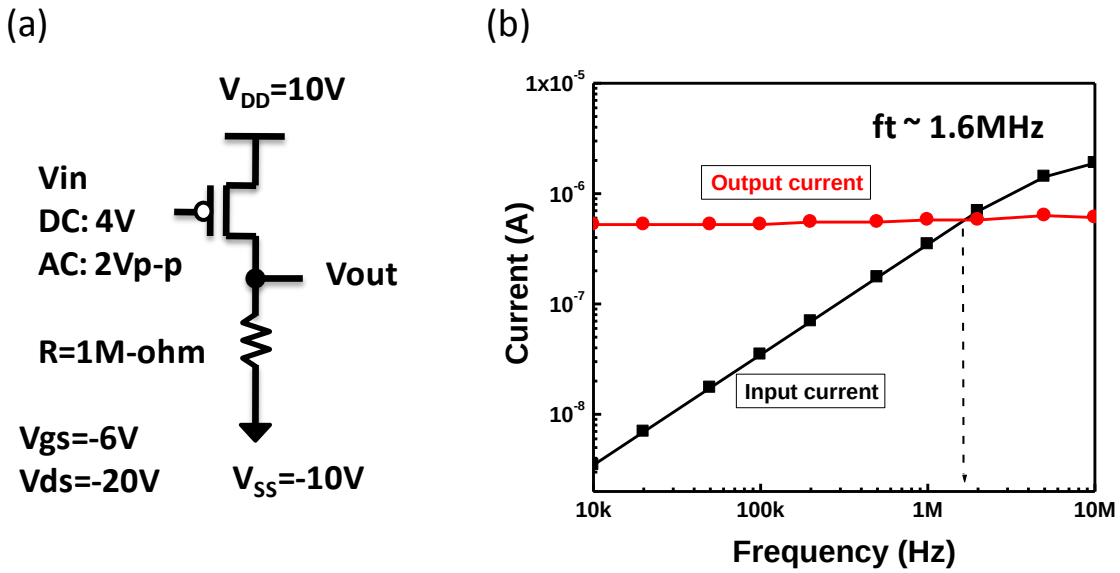

Figure 5.14 (a) The circuit setup of the cut-off frequency measurement (b) Cut-off frequency of the printed transistors showing the speed of 1.6MHz

The intersection of the two currents determines that the transistor has a cut-off frequency of 1.6 MHz. The theoretical cut-off frequency can be calculated using the following equation:

$$\text{Cut-off frequency} = \frac{g_m}{2\pi(C_{gs}+C_{gd})} = \frac{\mu V_{dd}}{2\pi L(L+L_{overlap})}$$

By inserting the mobility of 0.06 cm^2/V-s and Vdd of 20 V and L of 2.75 µm ($L_{overlap}$ is neglected due to a minimum overlap obtained from the self-alignment), the calculated cut-off frequency is 2.53 MHz. The calculated value is slightly higher than the measured value, possibly due to an under-estimate of the $L_{overlap}$. Overall, however, the calculation is in good agreement with the measured result. The high speed is a result of the highly scaled channel length and the minimum overlap capacitance achieved, despite the use of the relatively low mobility material. This is the highest transistor speed achieved using a lithography- and vacuum-free process at the time of this writing.

5.5. Sub-micron channel length

With successfully down-scaled gate linewidth and channel length, the performance of the printed transistors demonstrated here has reached the MHz speed range. The speed is expected to be improved further by down-scaling the channel length into the sub-micron range. Therefore in this section, we will introduce two techniques to create a fine separation between the source and drain. Combining this with the highly-scaled gate line, we can potentially achieve even higher transistor speed.

5.5.1. Mechanical-split technique

We have developed a new mechanical splitting technique to create small gaps. The mechanical splitting technique utilizes a probe tip to cut an originally continuous line into segments, as illustrated in Figure 5.15(a). This technique was discovered serendipitously during the PND processing. Recalling from the first section of this chapter, the PND started with inkjet printing of gold pads. Unlike the silver ink (CCI-300) which evaporates slowly, the Harmia gold ink dried in 30 minutes. Therefore, if the dragging process was done within 10 minutes after printing, highly-scaled lines could be dragged out. However, 30 minutes after the pad-printing, the pads become gel-like. In other words, the line can no longer be dragged out; instead, the probe tip that dragged through the pads could split the pads into two separate ones.

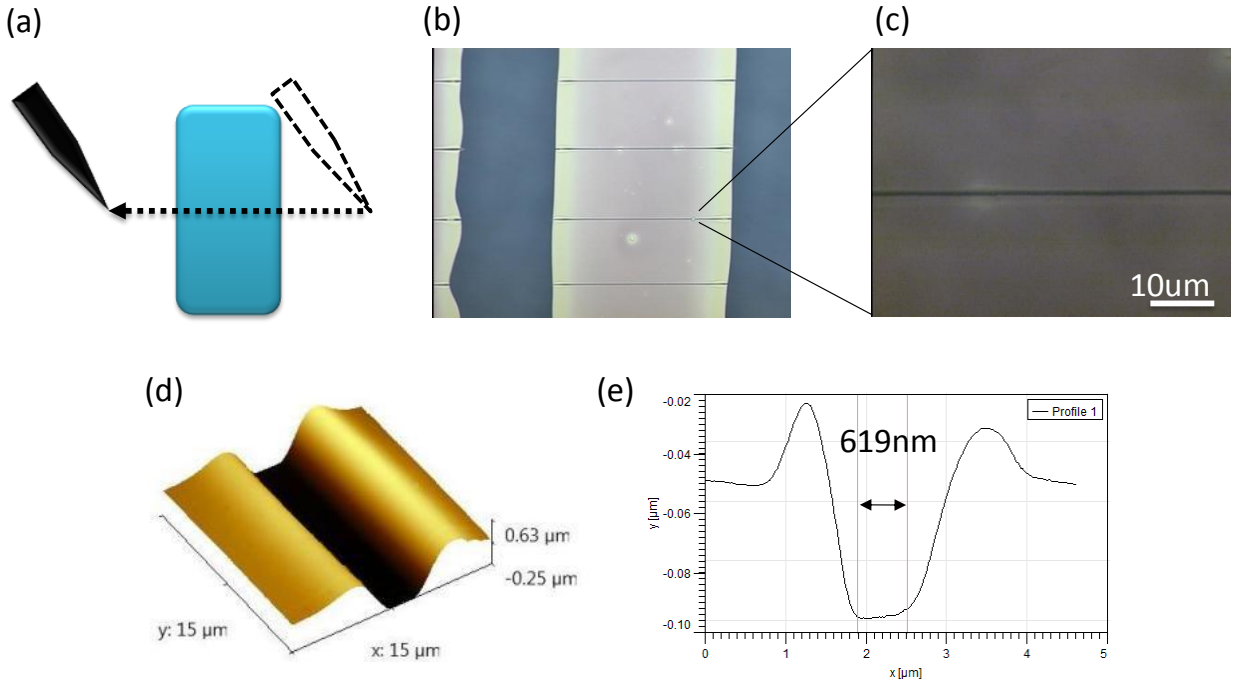

Figure 5.15 (a) A diagram of the mechanical-split process. (b) Optical micrograph of the printed gold line with the splitting. (c) Higher magnification of the part (b). (d) AFM profile of the separation. (e) Cross-sectional profile of part (e).

Figure 5.15(b) shows the mechanical-split of a gold line on a glass substrate. The gold line was inkjet printed using Harima ink, followed by a 30 minutes wait-time. Then the tip was used to cut through the line at a speed of 1000 µm/s. The lines were then sintered at 250 ℃ for 30

minutes. A clear separation created by the process is shown in Figure 5.15(c). To further examine the separation, AFM was used to inspect the profile. Figure 5.15(d) and (e) show the separation with coffee-ring-like edges on both sides. This was caused by a mechanical pushing of the material to both sides by the probe tip. Separations as small as 619 nm were achieved, using a probe tip with 2.4 µm point radius. With the pad thickness of merely 50 nm, only the bottom-most part of the tip was contacting and splitting the printed pads. Therefore, the separation in the sub-micron range was completely expected.

The technique can thus be used in creating short channel transistors. For a top gate device, where the S/D are produced first, there are no concerns of the tip contacting the substrate, since the semiconductor is deposited afterwards. However, for the bottom-gate and bottom-contact device used exclusively in this thesis, the mechanical splitting was done after the deposition of PVP. Whether the mechanical contact of the tip can damage the PVP surface thus becomes a concern. To clear this concern, the force applied to the surface by the mechanical splitting was characterized first. Then, the impact of the mechanical splitting on PVP breakdown field was examined.

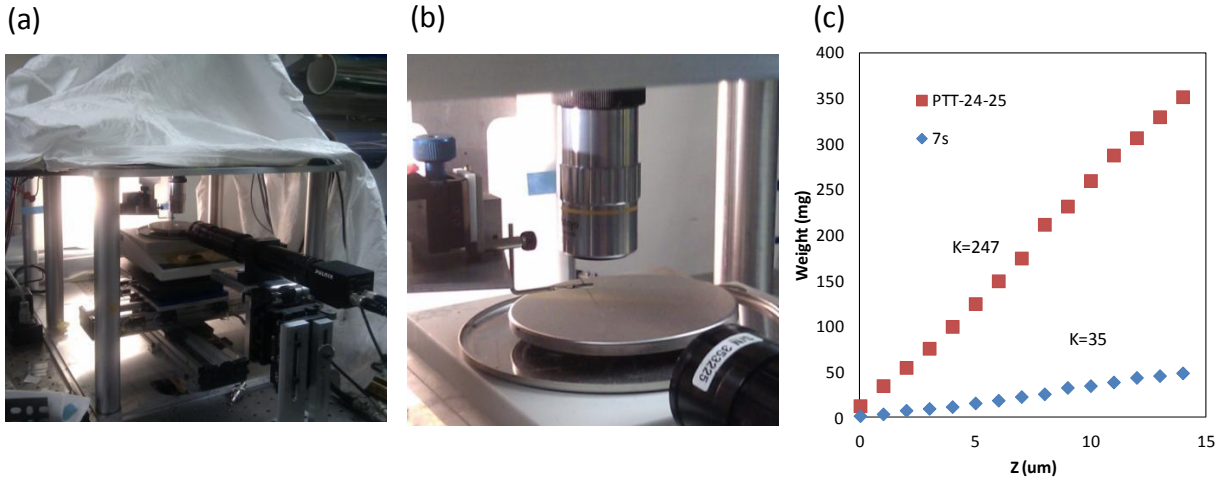

Figure 5.16 (a) Photograph showing the chuck of the PND system replaced by an electrical scale. (b) Closer view of the setup. (c) Weight of the tip as a function of vertical displacement.

The PND setup used in Chap. 4 was slightly modified to measure the force. The chuck on the X-Y motor was replaced by an electrical scale, as shown in Figure 5.16(a) and (b). The probe tip then approached the surface of the scale via controlling the Z-motor. When the tip contacted the surface, the Z-displacement was defined as 0. The tip was then dropped in one micron steps, and the corresponding effective weight of the tip as measured by the scale was then recorded. Figure 5.16 (c) shows the weight as a function of Z with two different probe tips, namely Cascade PTT-24-25 and Micromanipulator model 7s. Note the slope of the graph corresponding to the spring constant of both tip setups. By using a tip with a smaller spring constant, we can minimize the force applied to the surface. Moreover, the force can be controlled accurately despite of the presence of Z deviation. Therefore, the tip 7s will be used for the following experiment.

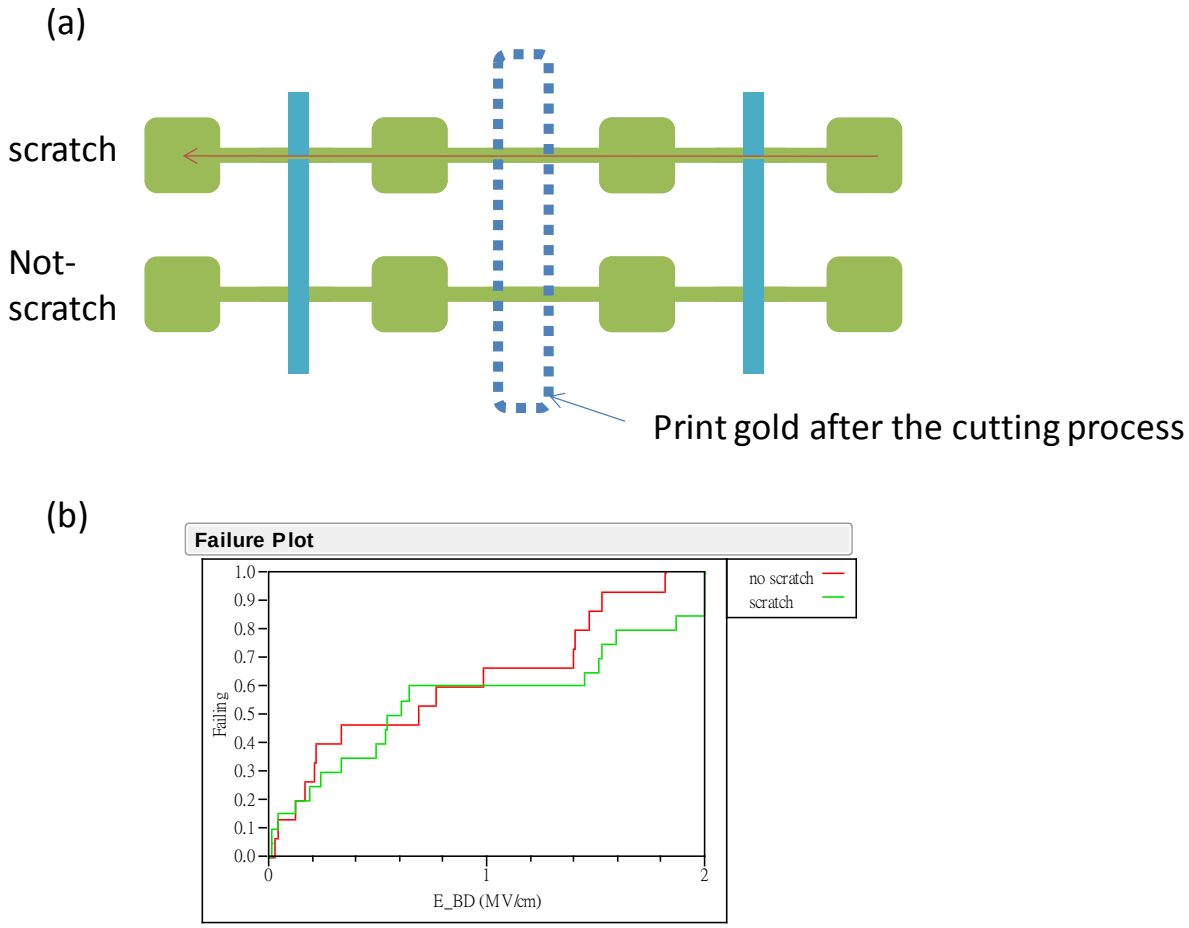

Figure 5.17 (a) The pattern used for testing the impact of the mechanical splitting on the PVP. (b) Cumulative failure plot of the capacitor with or without the splitting process

To further verify whether the mechanical splitting could deteriorate the PVP breakdown, capacitors with and without the splitting on the PVP surface were fabricated. Figure 5.17(a) shows the pattern for this test. Horizontal PND gate lines were first printed, followed by a spin-coat of PVP. Vertical gold lines were then printed on the first and third column. Mechanical splitting was then performed on the first row. The vertical lines on the first row were then inspected to confirm a successful split. The split indicates that the same force was applied on all three columns in the first row, where the second row was completely intact. A vertical gold line was finally printed on the middle column to cover the PVP. Then, the breakdown of the capacitors with or without the splitting on PVP were characterized. Figure 5.17(b) shows the cumulative breakdown extracted from the measurement of 16 capacitors. The breakdown was determined at the electric field at which an abrupt increase of the current was observed. The results show a similar cumulative curve with or without the splitting process. This indicates that the impact of the mechanical splitting on the PVP breakdown is not significant. Therefore, the technique can then be used to demonstrate a sub-micron printed transistor.

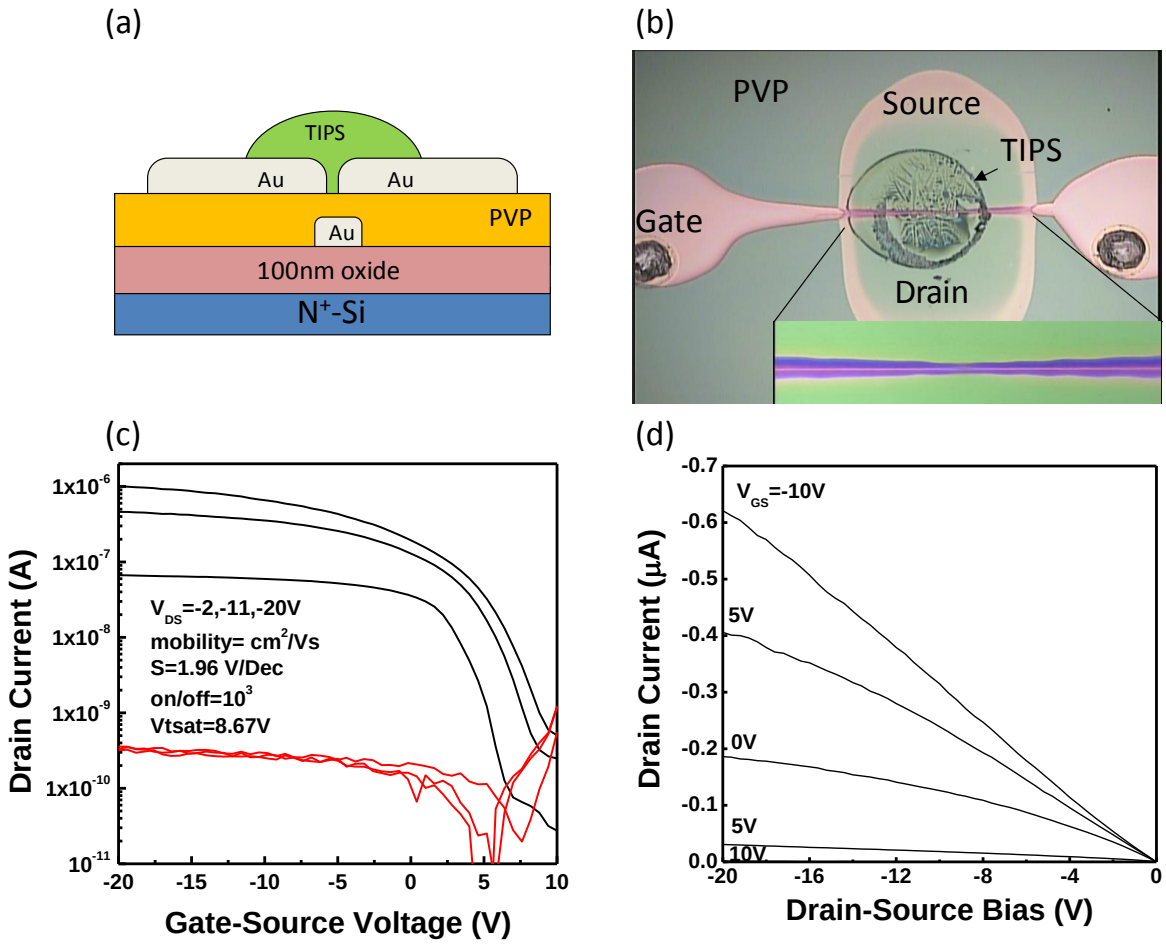

Figure 5.18 (a) Cross-sectional structure and (b) optical micrograph of the sub-micron printed transistor. (c) Transfer and (d) output characteristics of the printed transistor.

The transistor process started with the PND gate lines and the spin-coated PVP (110 nm), similarly to the first two steps of the capacitors. A vertical line was then printed on PVP across the gate line. Due to the coffee-ring effect, the printed gold on the PVP was too thin in the middle. Therefore, three layers of gold were printed to achieve a conductive line. After a wait-time of 30 minutes, the channel was then created by mechanically splitting the printed gold line, with the probe tip, mechanically aligned to the gate. The split gold line becomes two closely-spaced S/D electrodes, as shown in the inset of Figure 5.18(b). After the sintering step of the S/D, 1 wt% of TIPS pentacene dissolved in anisole was then printed on the channel. Five 80 pL drops of the TIPS pentacene were printed. The cross-sectional structure and the optical micrograph are shown in Figure 5.18(a) and (b) respectively. A channel length of 600 nm was achieved. Figure 5.18(c) and (d) shows the transfer and output characteristics respectively. Low gate leakage indicates that the PVP was not impacted by the splitting process, matching the testing done previously. Short channel effect was not observed despite the channel length of merely 600 nm. This is due a thin TIPS pentacene layer on the channel, made possible by inkjet printing a small volume. Therefore, sub-threshold slope and on/off ratio was significantly improved comparing to the 2.75 μm transistor. Note that the output characteristic shows S/D series resistance limiting current at V_G=-10V, due to the relatively thin S/D electrode printed.

Finally, due to the non-uniform coverage of the TIPS pentacene on the channel, the channel width was difficult to extract. As a result, the mobility of this transistor could not be determined precisely. However, based on the turn-on current, the mobility is believed to be around 0.001 cm^2/Vs. The speed of the transistor was unfortunately difficult to measure, due to the use of an oxidized silicon substrate. The silicon substrate results in a large parasitic capacitance that can significantly degrade the speed.

5.5.2. Self-aligned splitting

To achieve an even smaller channel length, a self-aligned technique reported by previous work was used [7]. Continuing from the source side self-aligned printing, the entire surface was treated by PFDT. This modified the source electrodes to become highly hydrophobic. 20 minutes of treatment was chosen as the optimum to achieve a surface contrast between the source electrode and PVP. The drain drop was then inkjet printed onto the source edge and it rolled-off to self-align to the source as illustrated in Figure 5.19(a). The drain drop completely conforms to the edge of the source edge as clearly seen in Figure 5.19(b). A high yield of 95% was achieved by verifying the electrical isolation between the S/D from 215 devices. The AFM image in Figure 5.19(c) shows a 200 nm gap between the S/D, with some noticeable residue. The printed drain was then sintered at 185℃ for 30mins.

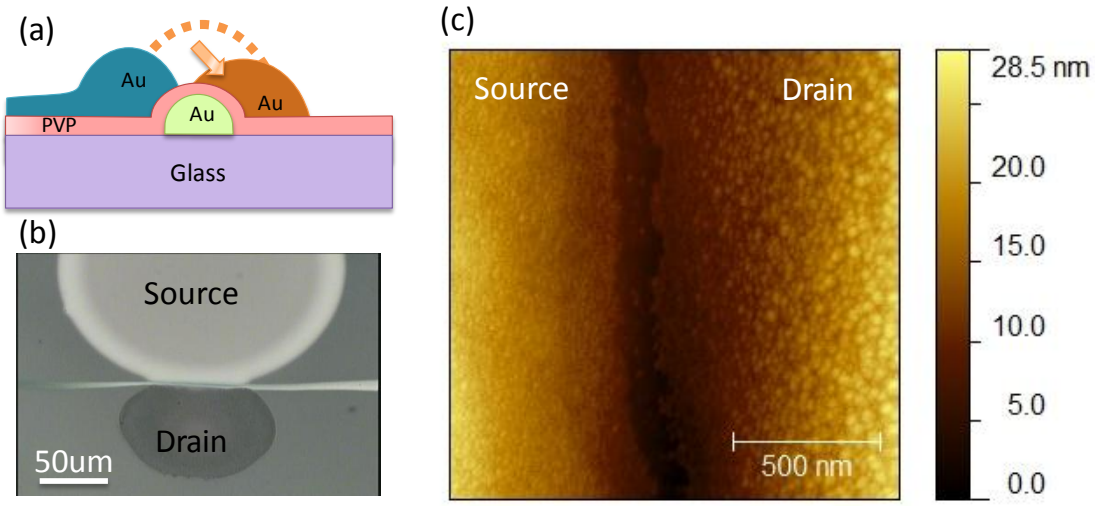

Figure 5.19 (a) Schematic diagram illustrating the self-alignment process of the printed drain (b) Optical micrograph showing the printed drain self-alignment to the source (c) AFM image showing the gap of 180 nm between the printed source and drain.

TIPS CFP was then inkjet printed on the channel to form a semiconductor layer. The printing parameters of TIPS CFP are identical to those in Chap. 4. The transistors were then characterized in air. Figure 5.20(a) and (b) show the transfer and output characteristics of the printed transistor. Channel width and length are 65 µm and 200nm respectively. The low gate leakage current indicates the PVP quality remained excellent after the S/D and semiconductor processing. Significant short channel effects including low on/off and unsaturated output curves were observed. Additionally, the transfer curve showed a punch-through-like leakage current at high drain bias, indicating a sub-channel surface conduction. As previously discussed, the dielectric

thickness of 110 nm is no longer below αL (α=0.2-0.5), therefore the severe short channel effect was expected. A thinner gate dielectric is required to enhance the electrostatic gate-control.

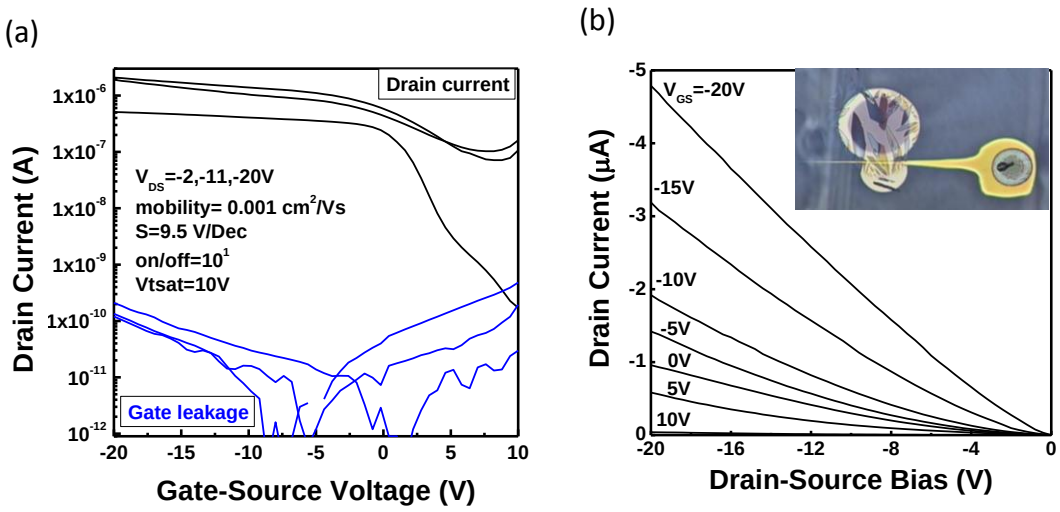

Figure 5.20 (a) Transfer characteristics of the printed transistor (b) Output characteristics of the printed transistor. Inset shows an optical micrograph of the printed transistor. Channel length and width are 200 nm and 65 μm respectively. PVP thickness is 110 nm.

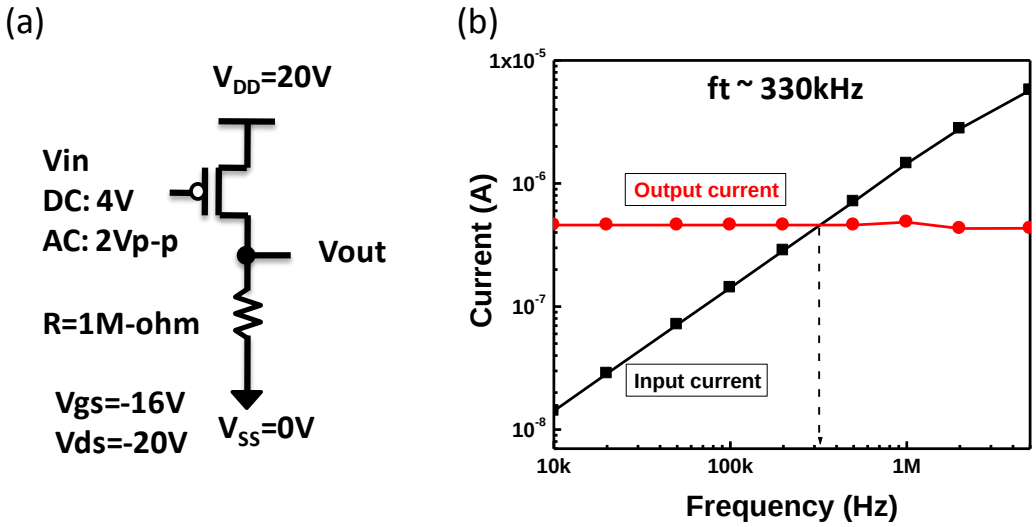

Figure 5.21 (a) The circuit setup of the cut-off frequency measurement. (b) Cut-off frequency of the printed transistors showing the speed of 330 kHz.

The speed of the transistor was then measured using a similar setup to the one introduced previously. A V_{GS}=-16V was used to bias the transistor at the maximum g_m. A cut-off frequency of 330 kHz was measured. Although further scaling has achieved a 200 nm channel length, the mobility was significantly lower than in the case of the previous devices with L=2.75 μm. As a result, the cut-off frequency becomes lower. First, of course, the gate dielectric was not appropriately scaled, as discussed above, resulting in low transverse fields. Additionally, the degraded mobility of the sub-micron channel could imply that the TIPS system might have some

unknown fundamental limits, as no study in the literature to date has demonstrated high mobility results in the sub-micron channel length range.

5.6. Summary

We have successfully developed and demonstrated highly-scaled printed organic transistors. By using a highly-scaled printed gate lines and a novel self-aligned S/D process, we have realized transistors that can operate at over 1 MHz. To our knowledge, the frequency performance demonstrated herein represents the highest operating frequency reported to date for printed organic transistors.

The mechanism of the self-alignment was investigated using an inductive method. Various physical and chemical factors were excluded. The encapsulants on the nanoparticles were determined to be the crucial component in achieving the self-alignment.

Finally, downscaling to sub-micron channel length was investigated, and initial results in this regime were reported as well, with successful demonstration of functional, albeit non-optimal transistors. Appropriate scaling of the gate stack and detailed studies on semiconductor material properties in this length regime are warranted.

5.7. References

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Chapter 6 Conclusions and Future Work

6.1. Conclusions

In this thesis, we have successfully developed an inkjet printed organic transistor process that self-aligns the source and drain to the gate without any lithography steps. Using this technique, we have overcome the registration limit of printed electronics and scaled down the gate-to-S/D overlap from 20 µm to 0.47 µm. All inkjet-printed transistors and inverters with minimum parasitic capacitances and a channel length of 50 µm were demonstrated. A switching speed of 2 kHz was obtained. Further scaling was then achieved using a novel print-and-drag technique to create highly-scaled gate lines. The process parameters were studied in order to optimize the line printing. All printed transistors and inverters with a channel length of 14 µm were then demonstrated. The switching speed was improved to 66 kHz by scaling. The limitation of the PND lines was then characterized and discussed. Scaling of the printed pads and nanoparticle size are required to achieve conductive 2 µm gate lines. A novel self-aligned printing was then introduced to successfully align to the highly-scaled 2.75 µm gate lines. Transistors with channel length of 2.75 µm were then demonstrated, showing a cut-off frequency of 1.6 MHz. The channel length was then aggressively scaled down to 600 nm by using a mechanical-splitting technique. The self-aligned printing technique was also used to achieve a channel length of 200 nm. Figure 6.1(a) summarizes the performance of the printed transistors versus the various channel length achieved in this thesis. While the horizontal dimension was successfully scaled down by novel printing techniques, the mobility degrades when scaling into the sub-micron region. As a result, the highest speed was obtained with a channel length of 2.75 µm. Figure 1(b) shows the enhancement of the speed over last three years. A significant improvement in speed was achieved, despite the use of relatively low-mobility materials. Further improvements are likely possible by using more advanced organic semiconductor materials that have now become commercially available.

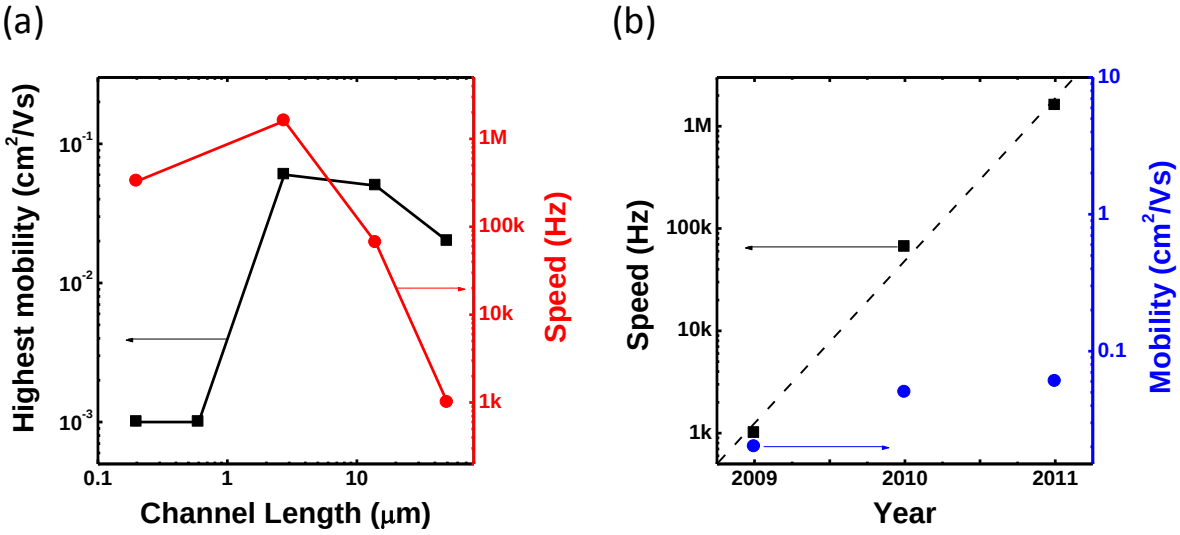

Figure 6.1 (a) Highest mobility and speed as a function of channel length (b) Speed and mobility improvement over the last three years.

To conclude, the techniques developed in this thesis have provided a pathway to study highly-scaled all-printed transistors. Short channel device physics specifically for printed transistors can now be studied by using these methods to produce highly scaled devices. Moreover, the self-aligned techniques developed in this thesis are not only limited to inkjet, but can also be applied to other roll-printing processes such as gravure. With the breakthrough in printing resolution, we believe the transistor speed can be improved over the 13.56 MHz range in the near future. This will open up a range of new applications in RFID, smart packages, and other novel applications for low-cost flexible electronics.

6.2. Future work

The transistors demonstrated in this thesis, although showing high switching speed, require further optimization. In particular, vertical scaling, including the thinning of dielectric and semiconductor layers, is required in the future to obtain better gate electrostatic control. The on/off ratio and sub-threshold slope are expected to be improved if appropriate vertical scaling is incorporated. On the other hand, mobility can potentially be improved by simply switching the material to more recently-developed higher-performance semiconducting polymers. Moreover, in a short channel transistor with bottom contact S/D, the impact of contact resistance needs to be characterized and optimized.

The self-alignment mechanisms introduced herein needs to be studied further to verify the proposed mechanism. We have currently concluded that the encapsulant of the silver and gold nanoparticles is a major contributor to the PVP surface energy difference. A follow-up experiment can be done to verify the hypothesis: The diffusion of the nanoparticles can be characterized by using Secondary Ion Mass Spectrometry (SIMS) measurement. If the profile of sulfur or nitrogen (typically used to attach the encapsulant to the metal nanoparticles) can be observed in the PVP layer, direct evidence of nanoparticle diffusion can be obtained. It is important to note that nitrogen also exists in the crosslinker of PVP; therefore, the PVP samples without the addition of crosslinker are required for SIMS measurement. Unfortunately, the absence of the crosslinker can perturb the system, e.g. a different diffusion profile can be obtained, as the interaction between the crosslinker and the encapsulant can be crucial. This complicates the analysis if nitrogen was used in the encapsulant for the metallic nanoparticles. However, if sulfur is detected in the profile, the analysis can be less complicated. Should the profile show an appearance of sulfur on the PVP surface, the surface energy difference can be concluded to be caused by the direct interaction between encapsulants and inks. On the other hand, if sulfur is only detected inside the PVP, then the surface energy difference can be caused by the encapsulant-induced chemical change of PVP surfaces. The latter case would then require an analysis to detect the surface chemical composition of PVP. To conclude, various unknown components exist in this system, causing the analysis to be difficult and ambiguous. Therefore, a bottom-up approach in achieving the self-alignment is highly recommended in the future, where the system is completely understood. An example of developing a bottom-up self-alignment would be to use an in-house-synthesized nanoparticle to print the gate electrodes, followed by a coating of PVP and a printing of S/D using the identical nanoparticle inks used in gates. By varying the encapsulant in the nanoparticles, e.g. various carbon numbers in the alkane chain or variety of atoms used in either end of the encapsulant, the correlation between the surface energy difference and the type of the encapsulant can be fully studied.

To continue, with the high speed transistors achieved, printed circuit such as frequency divider can be potentially demonstrated to divide down 13.56 MHz signal, where circuit techniques can be utilized to achieve a frequency division above cut-off frequency of transistors. High speed CMOS circuit can be potentially printed by applying the newly developed N-type organic semiconductor, with the S/D-semiconductor interface optimized.

To sum, more studies and demonstrations can be potentially done. The novel concept demonstrated in this work can inspire creativity in propelling the realization of all-printed circuit applications.

Appendix A Organic Transistor compact modeling

A.1. Introduction

In this appendix, a unified analytical compact model for organic thin film transistors (OTFTs) with short channel effect is developed to precisely describe the transistor behavior in circuit simulators such as HSPICE. Analytical model of OTFTs were proposed and studied in previous papers. M. A. Alam et al. and Horowitz et al. have numerically calculated the sub-threshold and above threshold characteristic of alpha-sexithienyl (α-6T) transistors [1-2]. Their reports help understanding the relation between the trap distribution and the current characteristics. However, their models require numerical computation, and are therefore not suitable for SPICE simulations. L. Torsi et al. have reported a short channel analytical OTFTs model for evaporated α-6T OTFTs and showed good fitting results down to channel length of 1.5 μm [3]. However, their model adopts a piece-wise field effect mobility, i.e. a constant mobility at low lateral field, and a power-law mobility at high field (>10^5 V/cm). This discontinuity could cause divergence in SPICE simulation. Therefore, a channel-length-scalable compact model optimized for circuit simulator is developed in this work. Various semi-physical based equations have been implemented into the model, including gate-bias dependent mobility, trap-assist leakage current and drain induced grain boundary lowering effects.

Spin-coated pentacene OTFTs were fabricated to obtain the experimental I-V characteristics of the OTFTs with channel length from 18 μm to 1.5 μm. The developed model was used to fit the transistors characteristics with one set of parameters. The model shows a good agreement with the experimental data, attesting to the precision and the scalability of the model

A.2. Experimental

The OTFTs were fabricated on heavily-doped N+ silicon wafers with 100 nm thermal-oxide. The N+ wafer and the thermal oxide were used as the gate and insulator respectively. Evaporated golds were used for source and drain electrodes. Gold has a high work function to form ohmic contacts with the HOMO (highest occupied molecular orbital) level of pentacene. Patterning of the gold source and drain was done by a lift-off process. HMDS was then treated on the oxide to obtain a hydrophobic channel surface in improving the packing of pentacene layer. Finally, the baseline pentacene precursor dissolved in chloroform with a concentration of 5 wt.% was spin-coated to form a semiconductor layer. Upon spinning, the precursor was annealed (~170℃) in a nitrogen (10ppm oxygen) atmosphere to create crystalline pentacene. The device structure is shown in Figure A.1. The pentacene was then patterned by mechanically scribing the periphery of the source and drain electrodes to isolate between devices. The channel length and width of OTFTs were measured by a high resolution microscope. The I-V characteristics of the OTFTs were measured by an Agilent 4156C semiconductor parameter analyzer.

A.3. Analytical model of organic transistors

Figure A.1 shows the equivalent circuit used to model an OTFT. The current source represents the channel current, which will be described using one unified equation. Since the equivalent circuit is symmetric, components on the source side will be introduced as follows: A resistor in series with the current source represents the contact resistance and the contact barrier.

The capacitance between gate and source is described using one fixed capacitor and one gate-bias dependent capacitor. Each circuit component will be discussed in individual sections.

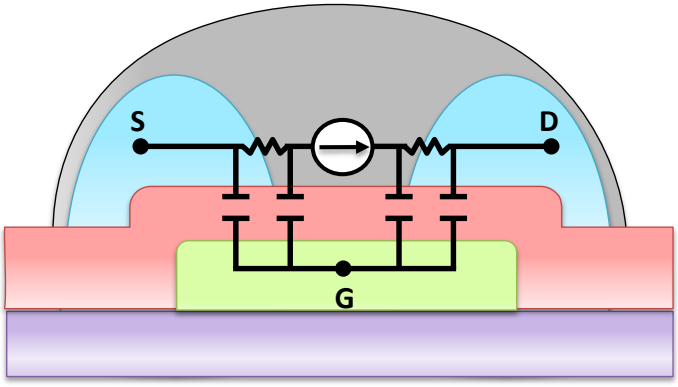

Figure A.1 Equivalent circuit of a bottom-gate and bottom contact OTFT.

A.3.1. Current equation

Unlike metal-oxide semiconductor field-effect-transistors (MOSFET), OTFTs operate in accumulation mode, due to the low carrier concentration and the abundant trap states between LUMO (lowest unoccupied molecular orbital) and HOMO level. Although OTFTs exhibit different transport mechanism than MOSFET, the current characteristic at high gate bias still obeys the square-law model. A conventional square-law model divides the transistor current into linear and saturation regimes. However, to improve the convergence in SPICE simulation, the current characteristic is written in one equation:

$$I_{ds} = \frac{W}{L}\mu_{eff} \cdot C_{ox}\left(V_{gte} - \frac{V_{dse}}{2}\right)\cdot V_{dse} \qquad (1)$$

where W, L are channel width and length, and C_{ox} is the insulator capacitance per unit area. μ_{eff} is the effective mobility, which will be discussed in the following section.

A.3.2. Effective mobility

From the square-law current equation, the mobility should be modified to account for the trap-filling effects in OTFTs. A gate-bias dependent mobility was then introduced to describe the trap states being filled gradually as the Fermi level approaching HOMO level of organic semiconductors. According to variable range hopping (VRH) [4] and multiple trap and release (MTR) [5-6], the mobility should exhibit a power-law relationship to the gate-bias. Therefore the effective mobility is modeled by combining a constant mobility μ_o and a power-law mobility:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \frac{1}{K \cdot V_{gte}^{\ \gamma}} \qquad (2)$$

where K and γ are fitting parameters. This equation mathematically represents an asymptote to a

constant mobility μ_o from the power-law mobility as shown in the inset of Figure A.2. With the effective mobility, the current equation shows a square-law behavior under high gate bias, and a power-law relation at low gate bias and sub-threshold regimes as shown in Figure A.2.

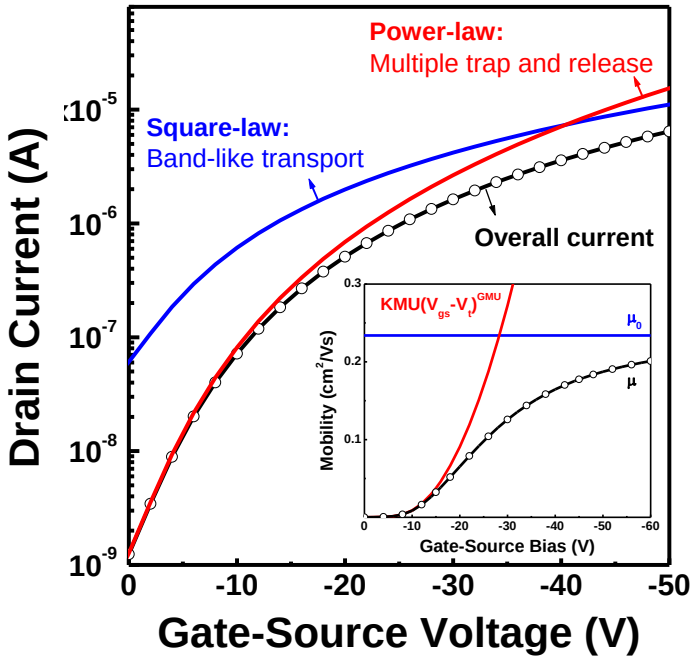

Figure A.2 Drain current as a function of gate-source voltage showing a transition from square-law to power-law dependence.

A.3.3. Smoothing function

Two smoothing functions are used to describe a continuous transition between different I-V regimes. V_{gte} is a function that smooths the transition between sub-threshold to above-threshold, where VMIN and DELTA are fitting parameters that change the shape of the curve as illustrated in Figure A.3(a). V_{dse} smooths the transition between linear to saturation regimes, where SAT and M are fitting parameters as illustrated in Figure A.3(b).

$$V_{gt} = V_{gs} - V_T \tag{3}$$

$$V_{gte} = \frac{VMIN}{2}\left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1\right)^2}\right] \tag{4}$$

$$V_{dsato} = SAT \cdot V_{gte} \tag{5}$$

$$V_{dse} = \frac{V_{ds}}{\left(1 + \left(\frac{V_{ds}}{V_{dsato}}\right)^M\right)^{\frac{1}{M}}} \tag{6}$$

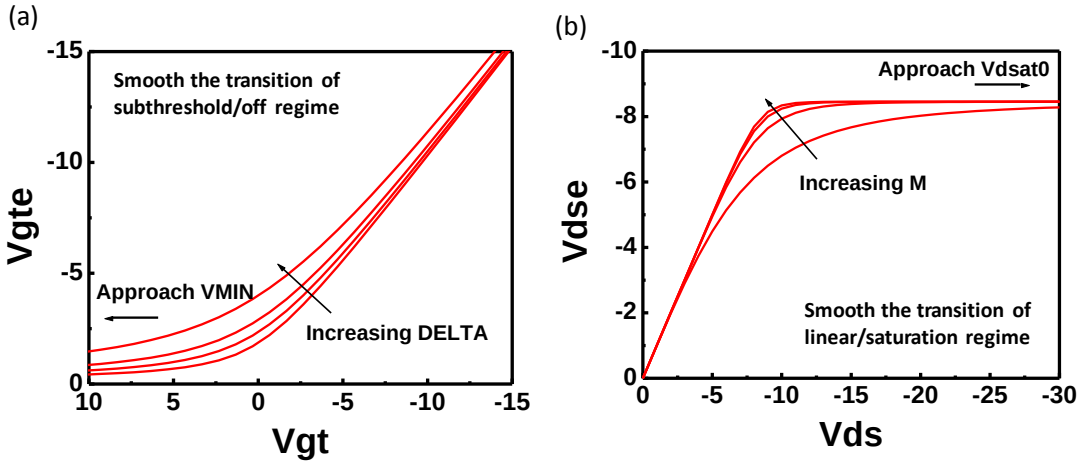

Figure A.3 (a) Vgte as a function of Vgt (b) Vdse as a function of Vds

A.3.4. Leakage current

The fabricated OTFTs show a channel leakage current with V_{gs} biasing below threshold voltage. The phenomenon is similar to gate-induced-drain-leakage (GIDL) observed in short channel MOSFET [7]. Moreover, low temperature poly silicon (LTPS) TFT exhibits a similar leakage characteristic, resulted from the thermionic field-emission of carriers through the grain-boundary trap states [8]. Here, channel leakage current of OTFTs is modeled as a simplified version of that in LTPS TFT as:

$$I_{leak} = \frac{W}{L} \cdot IOL \cdot \exp\left(\frac{V_{gs}}{VGSL}\right) \cdot \exp\left(\frac{-V_{ds}}{VDSL}\right) \qquad (7)$$

where the W/L term empirically accounts for the geometric dependence on the leakage current. IOL, VGSL, and VDSL are fitting parameters. The exponential dependence of the gate and drain bias represents the change of barrier heights of the thermionic emission and tunneling.

A.3.5. Series resistance and contact barrier

As shown in Eq. (8), the series resistance is modeled using a constant parameter R_{SERIES}. The contact barrier is empirically modeled using an exponential dependence on a barrier height – φ_b, divided by thermal voltage V_{th}. The exponential term is then divided by V_{ds} to describe a minimum impact of the contact barrier at a high drain bias as shown in Eq. (9). The total resistance R_S is then plugged into Eq. 11 to represent voltage drops at both source and drain sides. A modified current equation is then derived to account for the series resistance and contact barrier as shown in Eq. (11). Figure A.4 shows a representative output characteristic exhibiting a severe contact barrier. The bird-beak-like curves at low drain bias are well described by the developed model.

$$R_s = R_{SERIES} + R_B \tag{8}$$

$$R_B = \frac{\exp(\frac{\varphi_b}{V_{th}})}{V_{ds}} \tag{9}$$

$$I_{ds} = \frac{W}{L}\mu_{eff} \cdot C_{ox}\left(V_{gte} - \frac{V_{dse}}{2}\right) \cdot V_{dse} = G_{ch} \cdot V_{dse} \tag{10}$$

$$I_{ds} = G_{ch} \cdot \left(V_{dse} - 2 \cdot I_{ds} R_s\right) \Rightarrow I_{ds} = \frac{G_{ch} \cdot V_{dse}}{1 + 2 \cdot R_s \cdot G_{ch}} \tag{11}$$

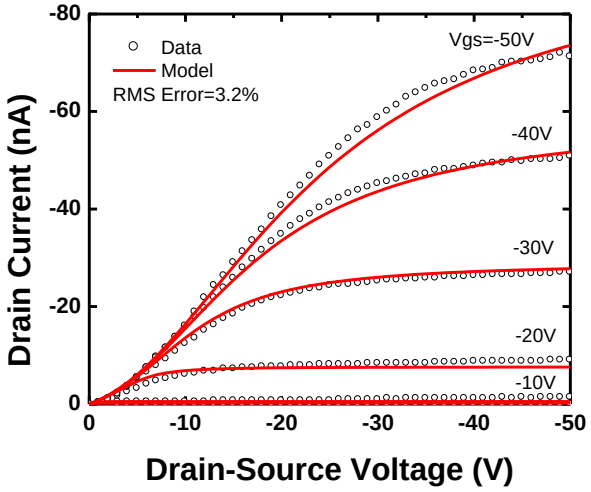

Figure A.4 Output characteristic of an OTFT with significant contact barrier. The model is in good agreement with the experimental data.

A.3.6. Capacitance

The capacitor components consist of a fixed overlap capacitor and a gate-bias dependent channel capacitor. Equation (14) shows the channel capacitance as a function of gate bias. Mathematically similar to the effective mobility, the equation indicates an asymptote to the value of $C_{ox}WL$, where the channel capacitance at the low gate-bias is described by a power-law. Figure A.5 shows the model fits correctly to an experimental data measured using a 75 kHz small signal. Note that the channel capacitance model is independent to the frequency, meaning the capacitance value would be inaccurate when operating at high frequency (>MHz), where a reduction of the capacitance was observed in our measurement. The frequency dependence on the capacitance model can be further developed in the future to precisely simulate the OTFT operating over MHz range. Equation (12) and (13) describe the capacitance partition between source and drain with respect to the linear-saturation transition. C_{gdc} and C_{gsc} both become half of C_{gc} at linear region due to a uniform distribution of the channel carriers. Under saturation region, C_{gsc} becomes two thirds of C_{gc}, while C_{gdc} becomes zero due to a carrier pinch-off near the drain side.

$$C_{gdc} = \frac{2}{3} C_{gc} \left[1 - \left(\frac{V_{dsato}}{2V_{dsato} - V_{dse}} \right)^2 \right] \quad (12)$$

$$C_{gsc} = \frac{2}{3} C_{gc} \left[1 - \left(\frac{V_{dsato} - V_{dse}}{2V_{dsato} - V_{dse}} \right)^2 \right] \quad (13)$$

$$\frac{1}{C_{gc}} = \frac{1}{C_{ch}} + \frac{1}{C_{ch} \cdot (V_{gte})^{\gamma}} \quad (14)$$

$$C_{ch} = C_{ox} \cdot WL \quad (15)$$

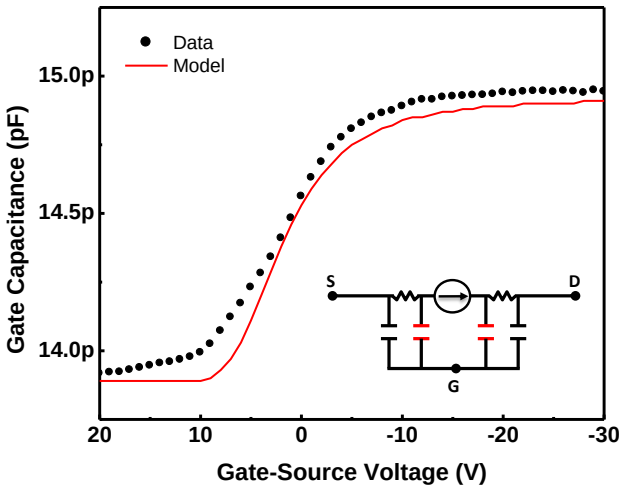

Figure A.5 Experimental data (dots) and model fitting (lines) results of the channel capacitance. Inset highlights the capacitance described by the model.

A.4. Short channel effect – V_T roll-off

A V_T roll-off equation is also included in the developed model. Unlike conventional MOSFETs which exhibit short channel effect at deep sub-micron scale, OTFTs show a V_T roll-off below 10 μm. V_T roll-off occurs when the lateral field is comparable to the vertical field in short channel devices, in which the V_T becomes a function of both V_{GS} and V_{DS}, resulting in the V_T reduction due to the drain bias. The drain-bias dependent can be explained as a drain induced grain barrier height lowering (DIGBL) due to the lateral field [9]. The grain barrier height decreases with the lateral field and causes an increase of drain current, which is equivalent to a reduction of V_T. DIGBL has been used to successfully model the V_T roll-off in LTPS TFTs. Therefore, in this work, V_T roll-off in OTFTs is modeled similar to LTPS TFTs, where the V_T is a function of channel length and drain bias [10]:

$$V_T = V_{T0} + \frac{\alpha V_{ds}{}^2 + \beta}{L} \qquad (16)$$

α and β are fitting parameters accounting for drain-bias dependent and the scaling of channel length respectively. Figure A.6 shows the V_T roll-off in our fabricated OTFTs, where a reduction of V_T (the value increases for p-type OTFTs) is clearly seen with L below 10 μm. Note that the V_T was extracted from the linear region using the conventional extrapolation method at the maximum transconductance (g_m). The model shows a good agreement with the extracted V_T, indicating the roll-off model used in LTPS TFTs can be applied to the pentacene OTFTs. This can be explained by the fact that pentacene forms a poly crystalline structure with sub-micron grain size similar to LTPS system [11].

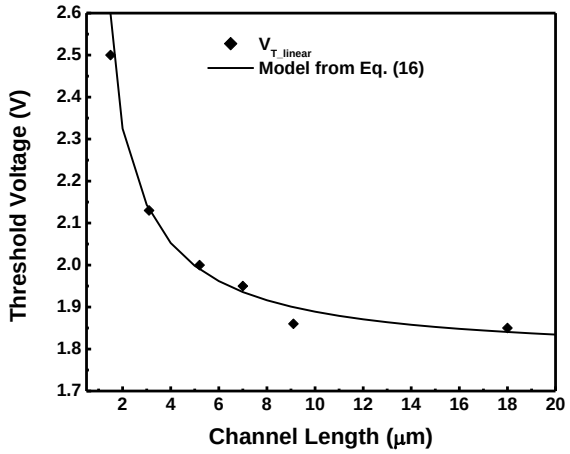

Figure A.6 Linear threshold voltage extracted from the power-law model (dots) and the model fitting results (lines) as a function of channel length.

A.5. Fitting results

The complete DC analytical model is equal to the sum of the channel current and the leakage current (Eq. (1) and (7) respectively). The equations are written in verilog-A language and plugged into Agilent IC-CAP software for fitting-parameters extractions and optimizations. The initial value for μ_0 was extracted from the slope of $\sqrt{I_{Dsat}}$ vs. V_G curve at a drain-source bias of -20 V. Figure A.7(a) and (b) show the experimental data and model fitting results of OTFTs with dimension of W/L=378/18 μm, and the parameters extracted are listed in Table I. The model shows an excellent fitting result except a noticeable discrepancy on the maximum current between Figure A.7(a) and (b), which is believed to be caused by the bias stress during the measurement [12].

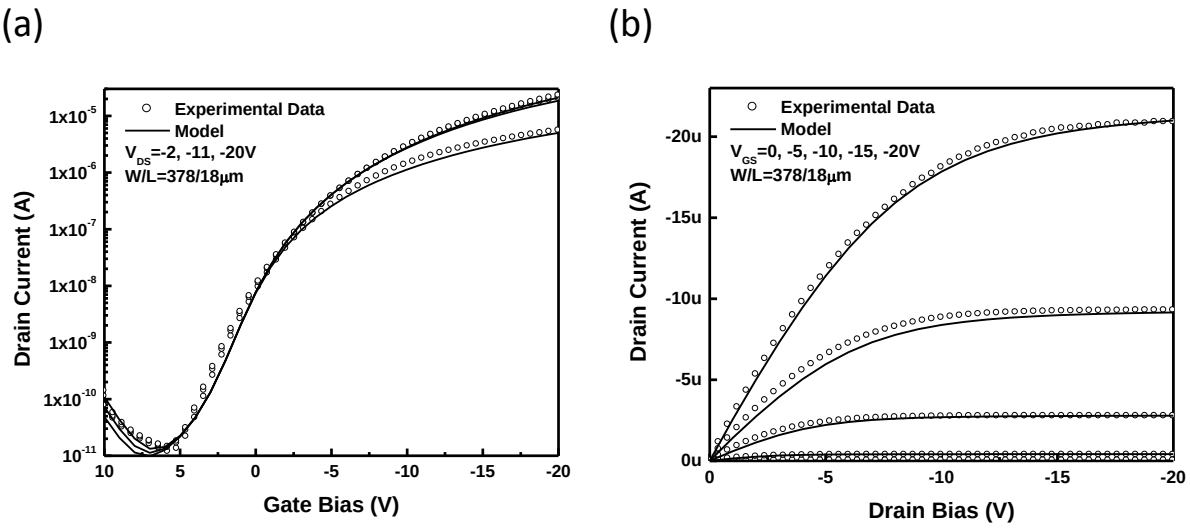

Figure A.7 Experimental data (dots) and model fitting (lines) results of the (a) transfer and (b) output characteristics of a pentacene OTFT with W/L=378/18μm.

Parameters	*Value*	*Units*
V_T	1.86	V
γ	1.8	-
K	9.6×10^{-4}	cm^2/Vs
μ_0	0.49	cm^2/Vs
IOL	-8.9×10^{-17}	A
VGSL	1	V
VDSL	21.45	V
M	3.175	-

Parameters	*Value*	*Units*
VMIN	-0.141	-
DELTA	19.06	-
SAT	0.5	-
PHIB	$4.441e^{-10}$	V
RSERIES	8.358×10^{7}	Ω
V_{T0}	1.78	V
α	4.3×10^{-3}	μm/V
β	1.09	μmV

Table A.1 Extracted model parameter values

A.6. Scalability of the model

By using the long channel parameters extracted in Table A.1, the scalability of the model is examined. Figure A.8 shows the model fitting results of OTFTs with 9, 5 and 1.5 μm channel length. The model demonstrates an excellent agreement with the experimental data by using the same set of parameters with W/L changing as scaling down.

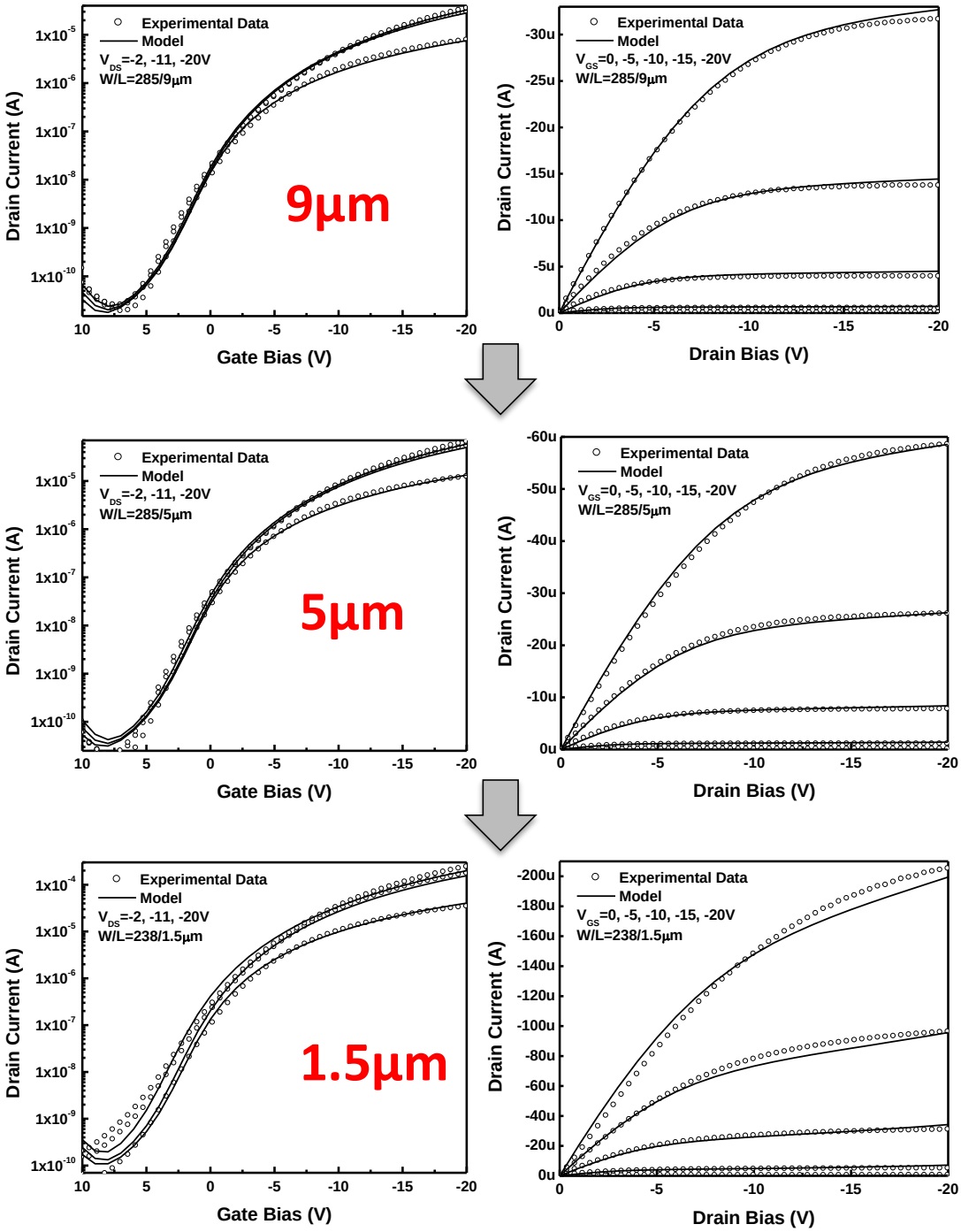

Figure A.8 Experimental data (dots) and model fitting (lines) results of both transfer and output characteristics from channel length of 9 um to 1.5 um.

A.7. Conclusions

An analytical model of OTFTs with short channel effects was developed. By introducing the gate-dependent mobility, trap-assist leakage current, and V_T dependence on DIGBL, the model has successfully fitted the experimental data from 18μm to1.5μm channel length. Furthermore, the model exhibits continuous transitions between the leakage, sub-threshold and above-threshold regimes, making it suitable for SPICE simulation.

A.8. References

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Appendix B Solution shearing

A solution shearing method was originally developed by Becerril, et al. to deposit solution-based organic semiconductors [1–3], in which the direction of crystal growth can be controlled to induce large grains, resulting in high mobility. Unlike spin coating and dip coating processes, the solution shearing method requires less volume of the semiconductor solution. This is beneficial in reducing the material cost. Moreover, the process involved a movement of two parallel plates, which is expected to be compatible with roll-to-roll processing. Fig. B.1(a) illustrates the solution shearing process, where a top plate with a non-sticking coating is used to shear the semiconductor solution on the preheated bottom plate. The top plate translates in parallel to the bottom plate, exposing an evaporating front that produces a seeding film with multiple crystal grains. The crystal then nucleates from the seed and propagates along the direction of the shearing. With the optimized temperature, shearing rate and semiconductor concentration, a highly crystallized film can be deposited over a large area.

A shearing apparatus was setup in our lab in order to produce high quality organic semiconductor film. The setup is described as follows: A hot plate was used as the bottom substrate. A silicon wafer with an ultra-hydrophobic CYTOP (Asahi Glass) coating was used as the top plate. The gap between the top plate and the sample (glass substrate) was created by a spacer consisting of a glass substrate (identical to the sample) and a Kapton tape, resulting in a gap of 125 µm. The top plate was then attached to an aluminum holder to form a module, as illustrated in Fig. B.1(b). A syringe pump (New Era Pump NE300) was used to push the top plate holder at a programmable velocity, as shown in Fig. B.1(c).

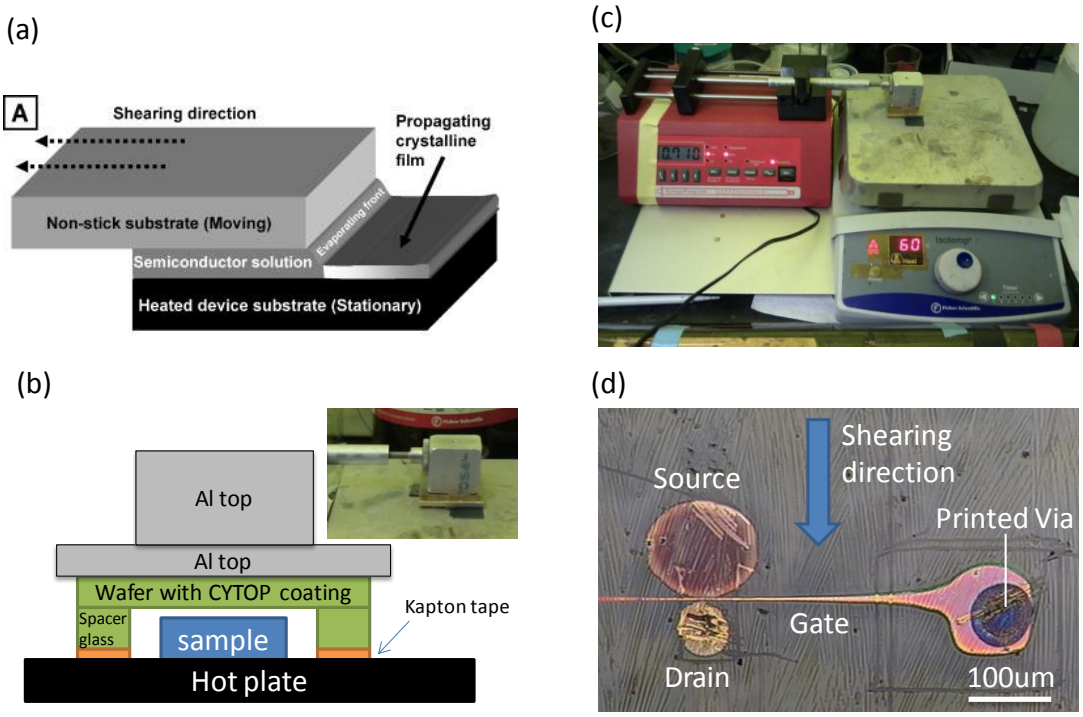

Figure B.1 (a) Schematic illustration of solution shearing method (b) Schematic illustration of the top plate module (c) Photograph of our solution shearing setup (d) Optical micrograph showing the TIPS pentacene layer deposited by the solution shearing method.

As indicated from the original solution shearing work, higher concentrations or temperatures can result in thicker films and amorphous precipitates. On the other hand, lower semiconductor concentration can result in low substrate coverage. Additionally, faster shearing rates can lead to a thinner film with reduced average crystallite size. Given these constraints, the solution shearing process was optimized using a relatively high temperature (half of the solvent boiling point) and a high shearing rate. 50 µL of 1 wt% triisoprophylsilylethynyl (TIPS) pentacene dissolved in toluene was drop-cast onto the sample substrate (2.5 cm × 2.5 cm) with the temperature preheated to 60℃. The top plate module was used to cover the sample immediately after the drop-casting and translated with a velocity of 520 µm/s. After the sample fully exposed from the top plate, the sample remained on the hotplate for a 10-minute drying step. The deposited TIPS pentacene was then isolated using probe tips for the subsequent transistor measurement.

Figure B.2(a) shows the cross-sectional structure of the testing transistors. Spin-coated PVP and inkjetted Harima gold S/D electrodes were used. TIPS pentacene was deposited using the solution shearing method with a shearing direction from top to bottom, as shown in the optical micrograph of the transistor (Figure B.2(b)). The transfer and output characteristics are shown in Fig. B.2(c) and (d) respectively. A highest mobility of 0.5 cm^2/Vs was achieved, surpassing the spin-coating and inkjet printing results obtained in this work.

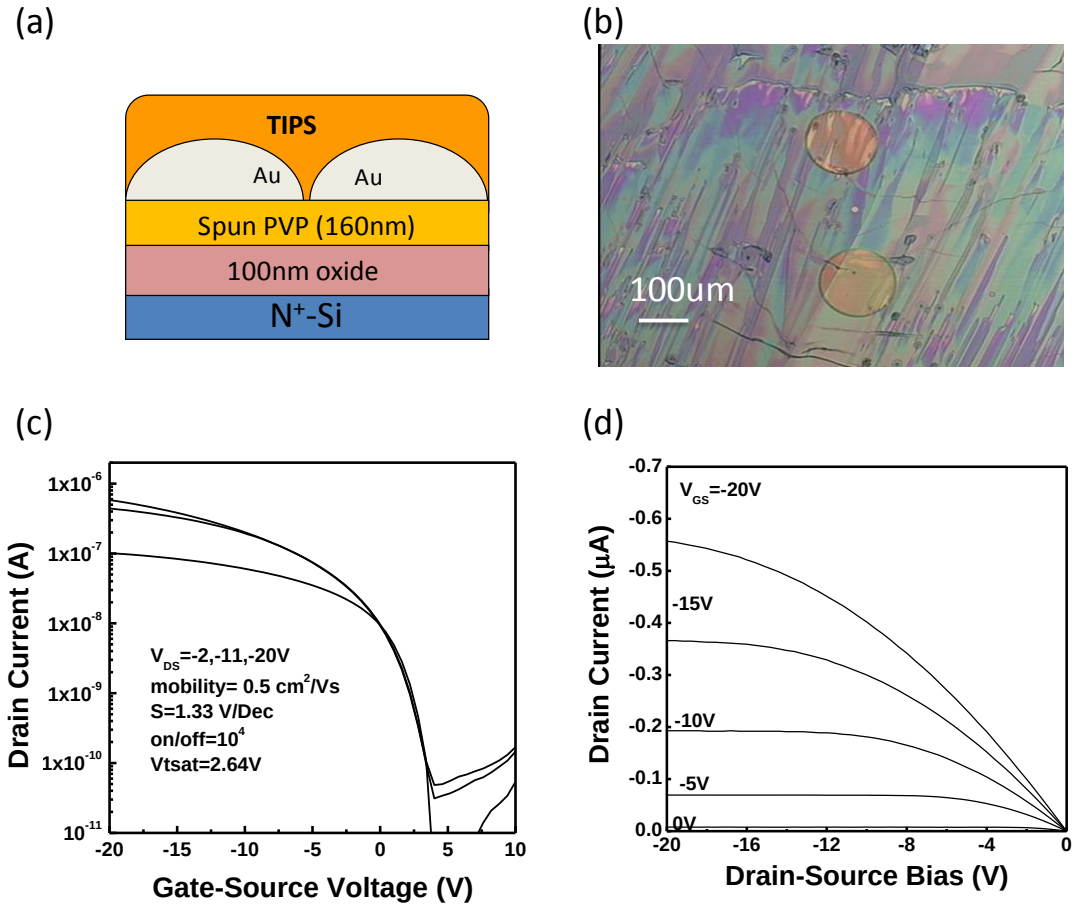

Figure B.2 (a) Cross-sectional structure of the testing transistor. (b) Optical micrograph of the transistor. (c) Transfer and (d) output characteristics of the transistor. The transistor has a channel length of 185 µm.

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