Solution-Processed Inorganic Electronics

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by

Teymur T. Bakhishev

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Committee in charge:

Professor Vivek Subramanian, Chair

Professor Ali Javey

Professor Oscar D. Dubon

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Abstract

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The field of low-cost and solution-processed electronics has experienced a steady increase in research interest over the past two decades. Fueled by continuous advances in materials development and deposition techniques, low-cost, printable electronics are approaching reality. However, a number of advances remain to be accomplished in order to enable some key, sought after applications, such as displays and RFID tags. In particular, to realize such systems, it will be necessary to facilitate the development of a number of underlying electronic devices, including conductors, transistors, and memory technologies. These particular devices are the focus of this work.

This work is focused on transparent thin film transistors (TFTs) and conductors for flexible displays and memories for printed RFID tags. TFTs and conductors are based on ink-jet printed reduced graphene oxide (rGO). Conditions for achieving good printed features, such as jetting dynamics, ink formulation, and printing temperature control are examined. Effects of these conditions, as well as various annealing schemes, on electrical performance are presented. Physical properties of printed films are investigated by atomic force microscopy (AFM) and X-ray photoemission spectroscopy (XPS). Resulting devices exhibit drive currents up to 1 μA, current ON/OFF ratios of up to 10, and field effect mobilities of up to 0.018cm^2/V-s. Presented drive currents and mobilities are sufficient to drive a basic display pixel; however, larger ON/OFF ratios are generally required. Potential solutions to achieving higher ON/OFF ratios, such as use of nano-ribbon graphene inks or dual gate structures, are proposed.

Memory presented in this work is based on filamentary switching in a silver/zinc oxide/gold (Ag/ZnO/Au) stack. There, diffusing Ag ions can reversibly form conducting paths through the ZnO electrolyte, thereby accomplishing data storage by changing the resistive state of the cell. A fully solution-processed cell is presented along with control cells based on evaporated metal contacts. Overall, good memory characteristics are observed: long retention time, cycling endurance of over 2000 cycles, good memory window, and minimum programming time of 200 ns. Filament growth dynamics are examined via potentiostatic, potentiodynamic, and temperature measurements. With the exception of a high temperature ZnO annealing step (350°C), these memories are fully-printable and plastic-compatible. Possible solutions for achieving low-temperature ZnO are presented, such as plasma treatments of deposited films and alternative sol-gel deposition techniques. With the incorporation of plastic-compatible electrolyte, this memory technology presents a promising candidate for printed electronics.

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First and foremost, I would like to thank my parents, Lisa and Tofik. This thesis belongs to them at least as much as it does to me. Their continuous support and encouragement made my education possible. I would also like to thank my sister, Delya, for her moral support and relentless attempts at trying to take an interest in my work. My parents have sacrificed so much to bring us here and give our family a better life and for that I will be forever grateful.

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1 Introduction: Solution-processed electronics

The pace of advancements in the field of electronics in recent years has been historically unparalleled and will likely continue to accelerate, particularly in the area of personal and mobile computing. Such progress can be attributed to improvements throughout the entire hierarchy of the field, starting from novel and improved materials all the way to innovative circuits and systems design. Furthermore, the emergence of novel processing techniques has introduced a possibility of drastically reducing the cost of personal electronics and allowing further expansion of the market. Once considered futuristic, products like foldable displays or e-papers and smart e-clothing may not be far away, and that in turn would allow a more ubiquitous integration of information technology into everyday life.

The cost of any electronic gadget is a complicated assortment of factors; however, some of the key components include the cost of the substrate used and the cost of processing (lithography, vacuum, thermal, etc.). Reducing the cost of these components may drastically affect the overall cost of the product. Consider a silicon wafer generally used in standard electronics processing: depending on the size and purity it may cost up to several dollars per square inch. In contrast, a plastic substrate, such as PET or PEN, may cost as low as single cents per square inch. However, said substrates will impose processing temperature restrictions due to plastic deterioration (150C and 200C for PET and PEN, respectively). This restriction on temperature may limit materials compatibility, but it also steers the processing away from potentially costly high-temperature processing steps.

Solution processing of electronic materials has been a research interest for quite a while as a path to ubiquitous electronics. In particular, printing techniques such as ink-jet and gravure are promising candidates for replacement of traditional lithography and deposition techniques. Currently, electronics fabrication consists of multiple deposition, lithography, and etch steps which are costly individually and overall due to the subtractive nature (whereby a blanket film is deposited and parts of it are removed to create a pattern). Printing, on the other hand, provides an additive process where material is only deposited where required, which reduces the net waste and material consumption. This therefore replaces both a deposition step (which may include vacuum and high-temperature), as well as a subsequent lithographical patterning step.

Printing in the context of electronics, whether ink-jet, gravure, or otherwise, generally involves deposition of functional inks in certain patterns to serve a specific purpose. The inks can be of metallic, semiconducting, or insulating nature, thereby covering all the necessary components of semiconductor manufacturing. A multitude of materials have been developed as candidates for such inks including organic insulators, polymer semiconductors and conductors, inorganic nanoparticles, as well as inorganic carbon solutions. Additionally, printing techniques are compatible with roll-to-roll continuous processing which increases throughput and decreases costs. A schematic representation of a basic additive process via ink-

jet printing can be seen in Figure 1.1, where different materials are deposited sequentially to form a device. Printing has been demonstrated as a possible fabrication route for thin film transistors, solar cells, light emitting diodes, sensors, and memory devices. Additionally, there are prototypes of entire electronic systems, such as RFID tags and displays.

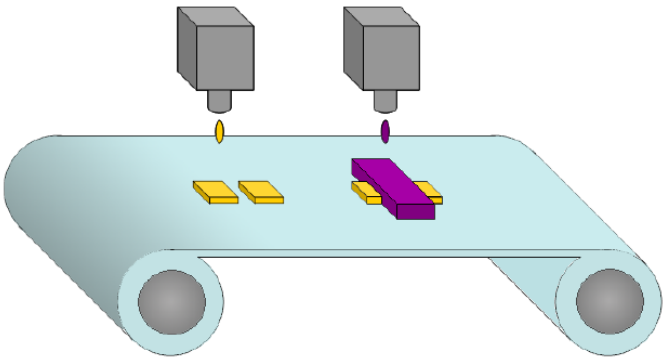

Figure 1.1. Ink-jet Printing Process.

1.1 Applications

Applications with the potential to utilize solution fabrication routes that garner the most attention are displays and RFID tags. The decrease in the cost of displays has been a key contributor to the expansion of personal media and communication electronics. An interactive display lies at the heart of almost any mobile computing device, such as a smartphone or a tablet. These have been getting smaller and thinner with each successive generation. One of the anticipated next steps in display development is the introduction of flexible displays. Currently displays are manufactured on glass and employ conventional processing techniques (lithography, vacuum, and high temperature steps). However, introduction of flexible technology would require flexible substrates, such as plastics. These substrates would, in turn, enable incorporation of roll-to-roll manufacturing which is compatible with solution-processing techniques. Additionally, a significant decrease in manufacturing cost of displays may allow incorporation into brand new markets, such as smart, interactive packaging and clothing.

Similar to displays, RFID tags and other mobile data and media interface devices are poised to break into the market on an unprecedented scale. An RFID tag could potentially replace a bar code for certain situations (such as checkout counters). It can contain significantly more information about the product than a bar code and requires less human interaction in handling, as the information stored can be read over a larger distance and has no line-of-sight requirements. Such RFID schemes have already been implemented by a wide range of industries to track package shipping, livestock, freight, and card key access. However, at present, tags are too expensive to penetrate more cost sensitive markets such as bar code replacement for supermarkets. Fabrication of RFID tags and displays via solution processing and printing techniques holds the promise of reducing production costs and allowing implementation on a wider scale.

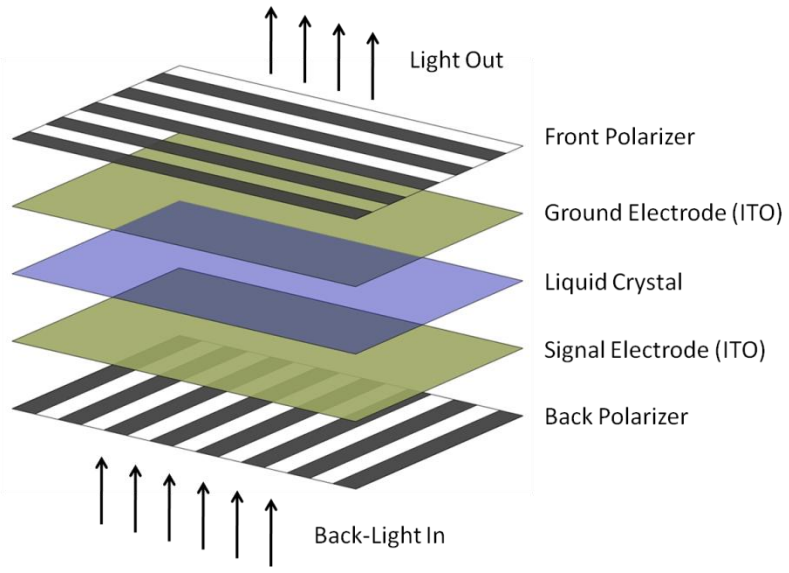

Figure 1.2. Schematic of a basic LC display.

1.1.1 LCD

Most current LCD applications employ an active matrix addressing scheme, where a control transistor is implemented for each pixel to enable switching. In this chapter, "LCD" will generally refer to AMLCD, unless otherwise specified. Let us examine the operation of a basic LCD display. A display consists of a large array of pixels/cells that can be individually selected to allow or prevent light passing through the cell, thereby producing a bright or dark pixel, respectively. A basic schematic of an LCD is presented in Figure 1.2. Generally, a display consists of a backlight source, a polarizing filter, a liquid crystal (LC) cell, and a second polarizing filter orthogonal to the first. An LC cell consists of a layer of liquid crystals sandwiched between two transparent electrodes, usually indium tin oxide (ITO). Application of voltage to the electrodes can force a change in alignment of the LC and the polarization of the light passing through. If the polarization of the light matches the polarizing filter on the outside of the cell, light is allowed to pass through, hence creating a bright pixel. If the induced LC alignment is such that light polarization does not line up with the filter, no light passes and a dark pixel is produced. A cell is addressed by properly biasing a control thin film transistor (TFT) attached to the cell, which in turn sets up an electric field across the LC electrodes which forces the liquid crystals into either transparent or opaque alignment. Figure 1.3a shows a schematic of a pixel array. Addressing happens by biasing appropriate gate and signal bus-lines.

Select TFTs and electrodes are key components of LCD circuitry. Proper selection and optimization of these will directly affect display performance and, thus, must be considered carefully. Parts of this work will address fabrication and characterization of transparent TFTs and electrodes. Benefits of their integration in an LCD will be discussed in this section. Figure 1.4(a) shows a cross section schematic of an LCD pixel. It can be seen that light only passes through the transparent ITO area, whereas some portion of the total screen area is blocked by the interconnect wiring and the control TFT. Such TFTs are generally manufactured from amorphous or poly-crystalline silicon (Si) and are not good transmitters of light. The blocked

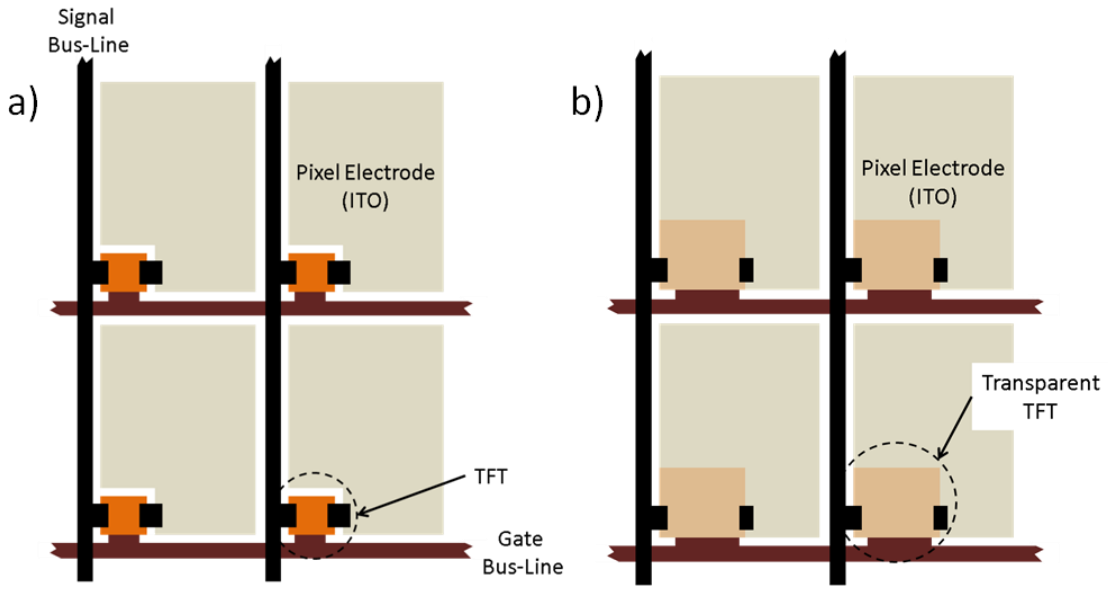

Figure 1.3. (a) Schematic of standard LCD pixel array, (b) Schematic of a pixel array with transparent TFTs.

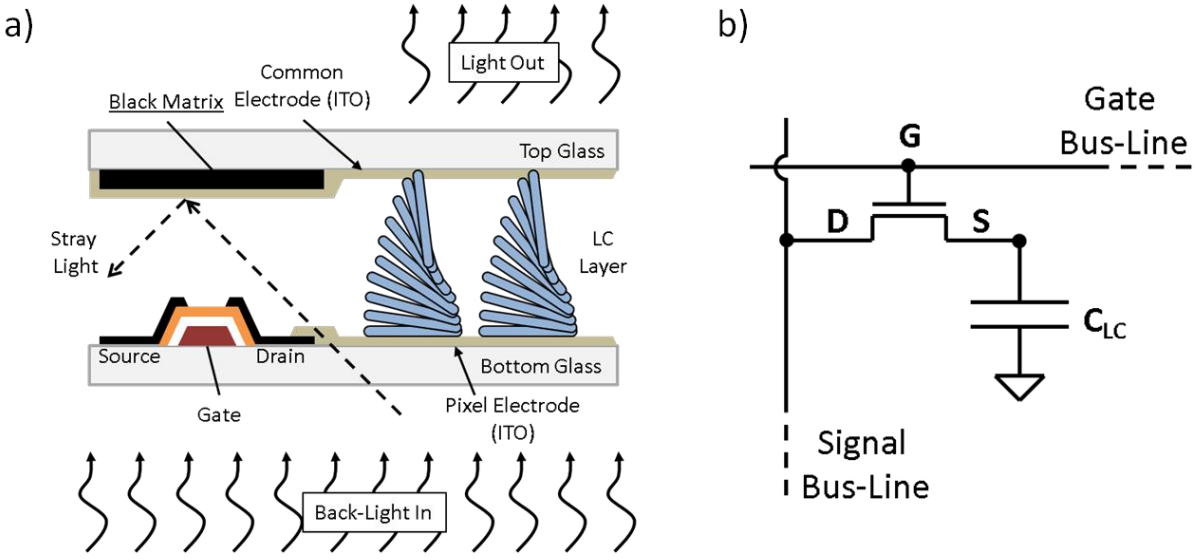

Figure 1.4. (a) Cross section schematic of an LCD pixel, (b) Circuit diagram of a pixel.

light does not contribute to the display signal which has a negative effect on overall brightness and contrast ratio. The relation of useful to wasted light is often called Aperture Ratio and is calculated as follows:

$$A = \frac{transmissive\ \ area\ of\ a\ pixel}{total\ area\ of\ a\ pixel} * 100\%$$

The aperture ratio is a critical parameter determining performance of an LCD display and a ratio close to one is desired. It can be seen that decreasing the size of the control TFT will

increase the transmissive area of the pixel and improve aperture ratio (Figure 1.3a). However, care should be taken in properly sizing the control device. The function of the TFT is to pass current and effectively charge the ITO/LC/ITO capacitor (C_{LC}), as demonstrated in Figure 1.4b. Size of the TFT directly affects the RC delay of the overall cell, which in turn determines the switching speed of the display. A TFT that is too small would not be able to source enough current, hence resulting in a slow switching display. Conversely, a large TFT would allow faster switching, but would simultaneously degrade the aperture ratio. So a tradeoff between speed and picture quality has to be considered when designing such cells. However, a significant improvement in performance can be obtained if the control TFT is manufactured from a transparent material. Such a design would significantly relax the inherent tradeoffs associated with optimizing the aperture ratio, as the size of the active area of the TFT would not contribute towards the portion of the light that is wasted. Figure 1.3b demonstrates this principle. It can be seen that the overlapping transparent TFT would allow a larger part of an individual pixel to transmit light, hence improving aperture ratio. It should be noted that the transparent TFT was deliberately scaled to appear larger than its conventional counterpart with the purpose of alluding to two points: first, currently proposed replacement TFT materials are not quite ready to compete with conventional technology, particularly in drive current. As such, these devices may have to be larger in size to produce equivalent current sufficient for appropriate switching speed. The second point, however, is to demonstrate that a transparent control device can occupy a large portion of the pixel with potentially negligible degradation in optical performance.

Consider a control TFT in a standard LCD application. Operation of such device can be approximately modeled with a standard square-law drive current formula, given by:

$$I_{D,Sat} = \frac{W}{2L}\mu_{Sat}\, C_{OX}(V_G - V_T)^2$$

Generally drive current on the order of 1 µA is required to drive a cell[1]. Given currently available state-of-the-art printing techniques, a 10 µm gate length can be achieved. Assuming a *W/L* value of 100, which is reasonable for a transistor spanning the entire pixel, an overdrive voltage of 5 V, and oxide thickness of 100 nm, mobility requirements can be calculated. This results in mobility of 0.015 cm^2/Vs. This value is achievable with current printing technologies. Current LCD applications generally utilize amorphous silicon (α-Si) TFT which produce mobilities of about 1 cm^2/Vs, and thus can be sized much smaller. It should be noted that the *W/L* ratio used in the calculation would essentially span the whole pixel width; however, as mentioned before, given TFT transparency optical, performance would not be degraded. Such metrics and performance comparisons will be examined in more detail in the following chapters.

Several materials have been examined in recent years as potential candidates for transparent TFTs including semiconducting polymers, various metal oxides (such as Zn, In and their doped and alloy variants), and graphene. Graphene, a two dimensional form of inorganic carbon, has become a heavily researched material because of its interesting and unique characteristics both as a conductor and a semiconductor. Through chemical processing it can be oxidized and form graphene oxide (GO) which forms stable suspensions in water, which can

subsequently be printed or otherwise solution deposited. Once on a substrate, GO can be reduced back to graphene and regain most of its electronic properties by thermo-chemical processes below 100°C. Both metallic and semiconducting variants of graphene can be deposited from the same starting solution by controlling deposition thickness and post-deposition processing. Graphene's compatibility with low-cost solution processing could make it well suited for low-cost and flexible electronics. Parts of his work will focus on graphene and its properties and the possibility of incorporation into flexible/transparent electronics.

Optical characteristics of an LCD display can be improved further by introducing transparent conductors and interconnects in conjunction with transparent TFTs. Figure 1.4a shows a cross section of a basic LCD cell. It demonstrates how stray light can penetrate through parts of the back plane which are not controlled by a specific cell and introduce light leakage, which degrades optical metrics such as contrast ratio and color fidelity. Light leakage can occur in multiple locations on the back plane: between pixel electrodes and bus lines, around the edges of control TFTs, interconnects, etc. To ameliorate light leakage a Black Matrix (BM) layer is introduced on the top plane. It is a patterned layer of opaque material which covers the areas where light leakage may occur, thereby preventing unwanted light from escaping. As a consequence of the addition of the BM a larger portion of the overall area is wasted by not transmitting light signal, hence the aperture ratio is decreased as well as brightness. However, if the signal bus lines and the interconnects can be replaced with transparent materials, alternative multi-planar cell architectures maybe applied. In such a case the bus lines along with control TFTs could be "folded" underneath the pixel electrode and a larger portion of the cell could transmit light. This may drastically reduce or eliminate the need for the BM layer, improve aperture ratio, brightness and other critical optical characteristics.

Let us consider the effects of line resistance on charging an LCD cell. In "turned on" state, Figure 4(b) can be simplified as an RC charging circuit, presented in Figure 1.5. The charging time of the LC cell, represented as effective capacitance, C_{LC}, can be expressed by the following equation:

$$V_{LC} = V_S(1 - e^{-t/R_{TOT}\, C_{LC}})$$

where R_{TOT} is total combined resistance of the signal line (R_{LINE}) and the control TFT (R_{TFT}), and V_S is the signal voltage. Alternatively, the equation can be rewritten to solve for time:

$$t = -R_{TOT}\, C_{LC} \ln(1 - \frac{V_{LC}}{V_S})$$

For a large cell array, the contribution from the line resistance can get quite large. For simplicity, it is assumed to be equal to R_{TFT}. Currently, sputtered metal is used for signal lines with low resistivities on the order of 10^{-7} Ω-m, and widths on the order of 10 µm. As discussed earlier, the width has to be minimized to maximize aperture ratio. However, if the width restriction is relaxed to 100 µm or, maximally, to the width of a pixel, charging time will be improved by approximately 50% or more. Alternatively, a lower resistivity material can be used and still maintain appropriate charging time. Thus, a transparent conductor can be utilized as

signal line material with resistivities of 10 – 100 times greater than sputtered metal and still achieve proper switching characteristics.

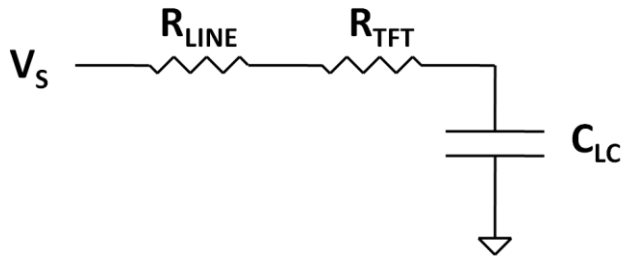

Figure 1.5. A simplified RC circuit representation of a charging LCD cell.

Another key component of an LCD cell is the ITO electrode itself. It has to fulfill two important requirements: first, it has to be highly transparent and cause minimum attenuation of the light. Second, it has to be conductive enough as to not degrade the RC delay of a cell. In the scope of currently available display technology, ITO has performed quite well; however, there are some potential problems with it going forward. One key problem is the rising cost of indium. With the rising demand of indium for the ever growing display market and its increased use in conductive pastes and solders, coupled with the shortage in production, the price of indium has been rising steadily over recent years. This not only causes general concern for the display market, but is particularly detrimental to efforts of incorporating ITO into low-cost electronics. Furthermore, in order to achieve required conductivities, ITO contact film thickness needs to exceed 100 nm. In that thickness range, ITO becomes brittle and unstable while bent, which introduces yet another barrier to its incorporation into flexible, low-cost electronics. The final, and perhaps most important, problem with ITO in regards to low-cost electronics is the fact that currently there is no good way of deposition that is compatible with low-cost routes. Sol-gel processes exist which require temperatures in excess of 500C which eliminates compatibility with inexpensive substrates; whereas room temperature sputtering techniques would still require post deposition patterning involving lithography and subtractive etching. Therefore, an alternative transparent conductor is required for integration with a fully solution-processed flow. Graphene is yet again a promising candidate for this role. In its metallic state, graphene has been shown to be an excellent material for both large area transparent electrodes as well as contacts for both organics TFTs and OLEDs. This work will demonstrate the compatibility of graphene with solution processing and will discuss the characteristics of conductors obtained with such techniques.

1.1.2 RFID

RFID tags and other “smart” devices are expected to allow on-the-go data interactions and such devices will all inevitably require some capacity for memory storage. Let us examine the basic operation of an RFID system as demonstrated in Figure 1.6.

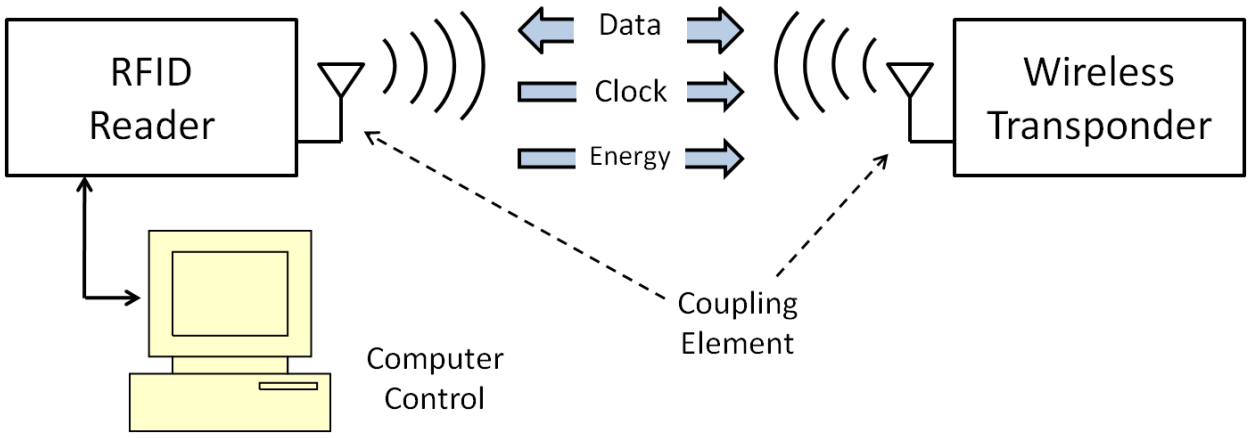

Figure 1.6. Diagram of an RFID system.

Generally the system consists of a reader and a transponder (or tag), which could be coupled magnetically or electromagnetically via an antenna. A reader produces a signal which, once coupled to the tag, provides both data and energy to power the electrically passive transponder. The tag then sends a signal with a unique identifier back to the reader to be interpreted. A reader system may consist of a single or multiple computers capable of various levels of data processing. As such the reader has no constraints on power, speed, and, to a large extent, cost since it is usually a singular part of a large implementation. Conversely, the cost of a tag plays a more significant role since any given RFID implementation may include hundreds or thousands of tags. Figure 1.7 demonstrates operation of a basic RFID tag. The signal from the reader is coupled through an antenna consisting of an inductor which is coupled to a capacitor to produce a resonant circuit. The signal produced by the antenna is then rectified and used to power the tag. The original signal could also be used as a clock for onboard logic. The clock frequency may be stepped down to be compatible with the logic elements. The logic portion of the tag generally consists of a nonvolatile memory array and output shift registers. Logic output is then fed back to the antenna and transmitted to the reader.

There are a large number of academic and industrial groups that have done extensive research on solution-processing techniques for RFID incorporation. To date, a large portion of the work has been dedicated to printable organic transistors[2-4] and passive components[5,6]. In fact, full tags have been demonstrated based on organic transistor logic[7-10]. Additionally, Jung et. al. have recently demonstrated a fully roll-to-roll printed tag[11]. However, none of these demonstrations had incorporated a printed programmable memory. So far, memory has been achieved by a secondary attached chip, hardwiring the circuitry, or post-fabrication physical alteration, such as mechanical or laser ablation. Mattis has achieved a potentially printable memory architecture based on an organic diode/antifuse stack[12]; however, this is a write-once design and it has not been demonstrated via solution-processing. It is clear that printed memory technology is necessary for a successful implementation of a low-cost, solution-processed RFID tag.

Currently two types of memory are used for conventional RFID tags without batteries: read-only and read/write. Read only memory is achieved by “writing” the data directly during

the manufacturing process, or by using a laser to "burn" data onto a configurable part of the chip after manufacturing. Read-only memory is generally used for price-sensitive applications, where the cost of a read/write memory is prohibitive. To achieve write and erase functionality, EEPROM is generally used. Storage capacity varies between single bytes to tens of kilobytes. EEPROM usually consists of a flash-like transistor design which will be described in more detail in Chapter *4*. To program this device, voltages around 20 V are necessary. Since an RFID tag is usually supplied with 3 V – 5 V from the coupling antenna, a charge pump is required to achieve proper programming. This is a very long and energetically expensive process which requires up to tens of milliseconds and hundreds of microjoules. A faster, lower power technology is desired.

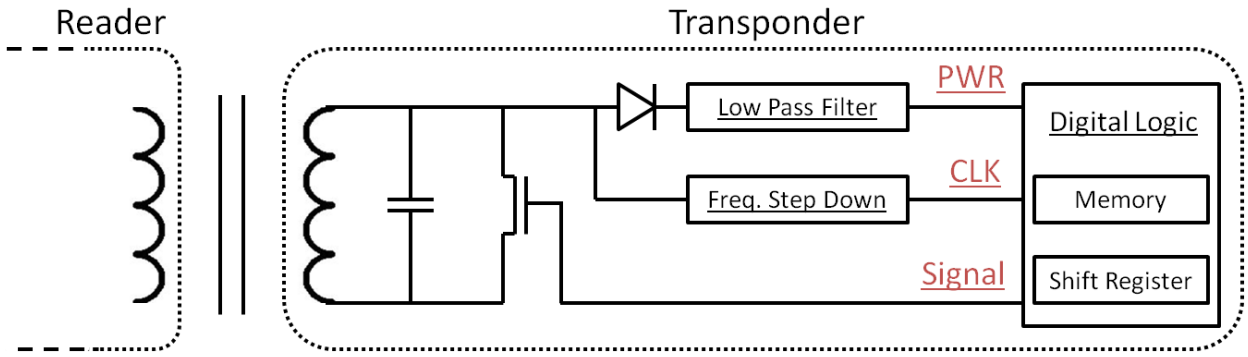

Figure 1.7. Schematic of a basic RFID tag.

A few solutions have been proposed for printed memories including ferromagnetic devices and flash-like organic transistors; however, none have shown significant potential for long term, full scale integration. Resistive random access memory (RRAM) variants based on metallic filament formation through a dielectric have shown some promise as a candidate for low-cost implementation. Such memories usually operate on the principle of metal ion (usually silver or copper) diffusion through various dielectrics (often metal oxides or sulfides). Parts of this thesis will demonstrate RRAMs based on silver (Ag) filament formation through a zinc oxide (ZnO) dielectric in an Ag/ZnO/Au cell, which can be fully solution-processed. Various properties of this system will be investigated for potential implementation into low-cost RFID tags.

1.2 Organization

This thesis is organized in the following manner:

Chapter *2* will introduce graphene as a potential material for solution-processed TFTs. Graphene's unique electronic properties will be discussed. It will be compared to other transparent semiconducting materials in the context of printed electronics. Ink-jet printed graphene TFTs based on graphene oxide will be presented; fabrication and processing techniques as well as resulting device characteristics will be discussed.

Chapter *3* will discuss ink-jet printed graphene conductors. Other solution-processed conductors will be introduced and compared to printed graphene. Effects of various fabrication and processing steps on the electronic properties of conductive lines will be examined.

Chapter *4* will introduce resistive random access memory (RRAM) and its principle of operation based on zinc oxide (ZnO) nanoparticle films. Various solution-processed memories will be discussed and compared. Data on electric properties, endurance, retention, and temperature effects will be presented.

Chapter *5* will provide conclusions and potential future research related to the topics covered.

2 Graphene Thin Film Transistors

2.1 TFT Background

A transistor is the most important element in electronics. It responsible for performing crucial tasks in both digital and analog circuits such as signal processing and logic functions. In LCDs, it serves a critical role of controlling individual pixels, as discussed earlier. Most conventional integrated circuits (ICs) are produced from single crystal silicon transistors. However, applications that demand substrates other than standard silicon often require deposition of all the materials necessary to form transistors, usually in form of thin films. An LCD is a perfect example of this, where a glass substrate is used to allow light transmission. A thin film transistor (TFT) is then "grown" on top by sequentially depositing patterned thin films. Currently this field is dominated by amorphous silicon (a-Si) TFTs; consequently, this is the technology against which all novel approaches, including printed transistors, are compared.

Any novel TFT will have to be compared based on metrics such as field effect mobility (μ), drive current, off current, on/off ratio, threshold voltage (V_T), and subthreshold slope (SS). Depending on any given application some of these parameters may become more important that others, which in turn may guide materials and processing selection. For example, a low-cost flexible display may require select transistors with a large on/off ratio to allow large array implementation, whereas drive current requirements may be relaxed if switching speed is not critical.

The structures generally used for fabrication of standard TFTs and printed TFTs are quite similar. Those can be gated from either top or bottom, and also have the source and drain (S/D) contacts on either top or bottom (Some examples are presented in Figure 2.1). It should be noted that the structure with a highly conductive bottom substrate as a gate is not practical for real life applications; however, it is very useful for lab prototyping printed transistors, especially for investigating semiconducting (SC) materials and S/D interactions. Usually such substrates consist of thermally oxidized, highly doped silicon.

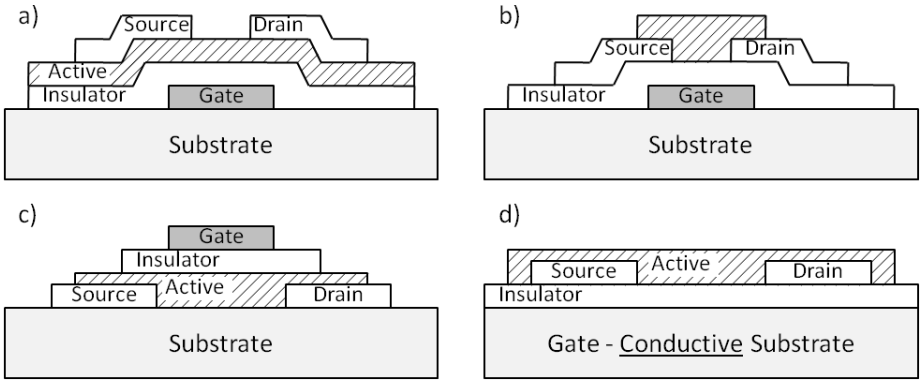

Figure 2.1. Some TFT structure types.

Depending on the particular desired structure, the fabrication process flow of a printed TFT can proceed in various ways. An example of one such flow is given in Figure 2.2. This is a bottom-gate structure as presented in Figure 2.1(b). First, a gate line is printed, usually from metallic ink such as gold (Au) or silver (Ag), but other options are possible. Second, an insulator layer is deposited. Some of the often used insulator materials are organic polymer dielectrics, such as poly-vinylalcohol (PVA)[13], poly-vinylphenol (PVP)[14]; however, a multitude of other materials are currently being researched for this purpose[15]. Third, S/D contacts are printed. Again, these could be metallic in nature or a conducting polymer, such poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS)[16]. Finally, a semiconducting, or "active", material is deposited to bridge the S/D contacts. A variety of semiconductor materials have emerged as potential candidates to fill the role of a printable active material including polymers[14,16] , inorganic nanoparticles[17] or sol-gels[18], and inorganic carbon systems[19] and no clear frontrunner has been identified yet.

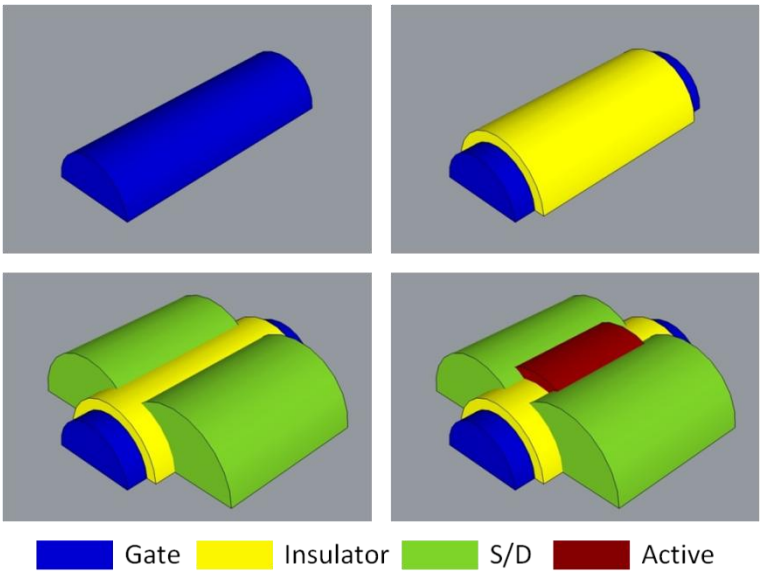

Figure 2.2. A schematic of a sample printed TFT process flow.

The process, as described, may sound simple enough; however, the complexity of the overall system and the individual component interactions cannot be overstated. The gate lines, for example, cannot be too thin to ensure good conductivity; yet depositing lines of appreciable thickness may lead to surface roughness or cracking. This, in turn, may cause problems with the dielectric layer facilitating pinholes in the insulator or spikes through it, resulting in degraded or unusable devices. The dielectric layer has to be smooth and conformal in order to ensure electrical isolation between the gate and active material. It also has to be chemically favorable to the active material to prevent causing disorder at the insulator-semiconductor interface which will likely result in decreased performance[20]. The S/D contacts have to be energetically matched with the semiconductor to ensure proper carrier injection and transport. This is a commonly encountered problem between metallic contacts and organic semiconductors, which is sometimes overcome by introducing a secondary organic (mono)layer to the metal/SC interface to improve carrier injection. All of the mentioned examples barely scrape the tip of an

iceberg represented by the enormous amount of complexity associated with incorporating different, often dissimilar, materials to produce a transistor.

2.1.1 TFT Modeling and Parameter Extraction

In order to properly compare different TFT technologies, it is important to have a meaningful metrics of evaluation. Generally, device characteristics such as mobility, drive current, on/off ratio, threshold voltage (V_T), and subthreshold slope (SS) are used for this purpose. Thin film transistors often operate in accumulation mode due to a large number of trap sites associated with impurities and defects in the semiconductor. These imperfections in the active layer cause additional energy states, in particular in the band gap of the material, which act like traps. Consequently, it is often hard or impossible to invert the semiconductor, which limits the operation range to accumulation. However, overall operation is quite similar to ideal transistors, where cut-off, linear, and saturation regimes are clearly present. This enables simple modeling of TFTs with basic square law equations and extraction of operational metrics, such as mobility, threshold voltage, and subthreshold slope. The linear and saturation square law equations are as follows:

$$I_{D,Lin} = \frac{W}{L}\mu_{lin} C_{OX} (V_G - V_T - \frac{V_{DS}}{2})V_{DS}$$

$$I_{D,Sat} = \frac{W}{2L}\mu_{Sat} C_{OX} (V_G - V_T)^2$$

It is, however, difficult to predict the threshold voltage due to non-idealities and gradual turn on characteristics. It is often more appropriate to extract the transconductance given by:

$$g_{m,Lin} = \frac{dI_{D,Lin}}{dV_G} = \frac{W}{L}\mu_{lin} C_{OX} V_{DS}$$

$$g_{m,Sat} = \frac{dI_{D,Sat}}{dV_G} = \frac{W}{L}\mu_{Sat} C_{OX} (V_G - V_T)$$

then extract mobility by combining the equations. Mobility is quite often gate dependent, which is due to gradual filling of the trap states as a function of transverse electric field.

2.2 Active Materials

The most actively researched aspect of printed TFTs has been the active material. As previously mentioned, there are multiple material systems that have shown promise as candidates for solution-processed semiconductors.

2.2.1 Organic SCs

Organic semiconductors were some of the earliest materials widely investigated for printed applications, and are still heavily researched. Original work was done on poly-thiophene[21], and a good portion of the exploration since dealt with thiophene[22] or pentacene[23] derivatives. Figure 2.3 shows some of the more commonly used semiconductors for organic thin film transistors (OTFT). The basic building block of an organic semiconductor is a conjugated system with sp^2 hybridized carbon-carbon bonds. This bond scheme allows

delocalization of electrons which can effectively become (partially) free carriers[24]. Each molecule or unit of a polymer acts as a site with associated delocalized electrons. An organic film can then be represented as an assembly of such sites and individual delocalized carriers can hop from one site to another, thereby resulting in electrical conductivity.

Although certain properties, such as solvent compatibility and low processing temperatures, make some organic semiconductors attractive for solution processing, these polymers are generally not without significant disadvantages. Organic SCs are often very sensitive to oxygen and moisture, where prolonged, or even minor, exposure can cause significant degradation. Consequently, special care is required while processing these materials, which is usually done in an inert environment such as a glovebox. Furthermore, to ensure reasonable lifetime, OTFTs need to be heavily encapsulated to prevent atmospheric exposure. There have been, however, continuous advancements in the field of organic chemistry that have allowed organic SC performance to approach that of a-Si. Recently, poly(2,5-bis(3-alkythiophen-2-yl)thieno[3,2-b]thiophene has been developed, which exhibits significant improvements in oxygen stability and approaches performance of a-Si in mobility (up to 0.6 cm^2/Vs)[25].

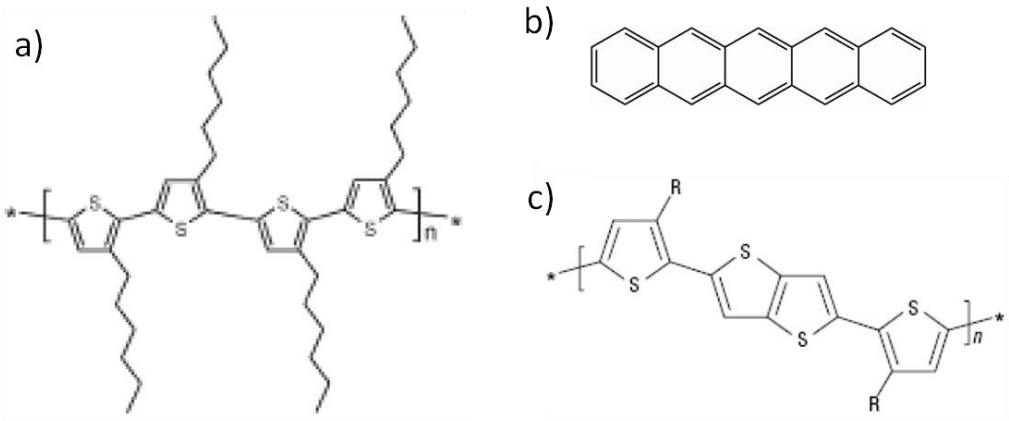

Figure 2.3. Some common organic semiconductors: a) poly-3(hexylthiophene) (P3HT), b) pentacene, and c) poly(2,5-bis(3-alkythiophen-2-yl)thieno[3,2-b]thiophene (pBTTT).

2.2.2 Metal Oxide (Chalcogenide) SCs

Metal oxide (MO) binary systems have been investigated as semiconductors for quite a while; in fact, ZnO and its ternary derivatives deposited by sputtering are heavily researched material systems for use in transparent TFTs[26,27]. However, it wasn't until fairly recently that solution processable metal oxide semiconductors started to emerge as candidates for printed electronics[28,29]. The following section will focus on ZnO processing; however, the techniques discussed here are generally applicable to a number of similar systems, such as aluminum-doped zinc oxide (ZnO:Al), indium zinc oxide (IZO), gallium zinc oxide (GaZnO), and combinations thereof.

There are two major solution routes towards depositing ZnO: nanoparticle inks[30] and sol-gel[18]. Nanoparticle inks consist of particles in the range of 1-10 nm dissolved in a solvent,

possibly with other additives to increase solubility, stability, etc. Nanoparticles can be passivated or encapsulated with a surfactant to prevent agglomeration. (A more detailed description will also be included in Chapter 4 as it deals more directly with ZnO nanoparticles). After deposition, particles can be annealed and sintered into continuous films. This technique often requires anneal temperatures of up to 400°C for oxides, whereas some sulfide based films have been shown to become electrically active as low as 200°C[31].

In a sol-gel process a precursor is deposited on a substrate first and then converted to form the final product. The precursor is generally a salt of the metal of interest, such as acetate or nitrate, dissolved in a solvent. Again, additives could be introduced to either improve solubility or promote subsequent chemical conversion. For example, ammonium hydroxide can be added to a zinc salt solution. Sol-gel processes often require temperature up to 600°C - 700°C; however, there has been work recently where ZnO TFTs were demonstrated via a sol-gel process at 150°C. In that work, devices deposited by spin-casting exhibited mobilities of ~2 cm^2/Vs, although it is unclear from the publication whether transfer to ink-jet printing is likely.

2.3 Graphene

2.3.1 History

Graphene has become one of the most researched materials since its initial recent demonstration in 2004 by Geim and Novoselov[32]. Graphene is a truly two-dimensional form of carbon where individual atoms are arranged in a hexagonal, "honeycomb" pattern (Figure 2.4). When stacked together these sheets form graphite. The theoretical concept of a 2-D material has been around for over 60 years[33]; however, it was widely assumed that such structure could not exist physically due to thermodynamic instability. It was believed that thermal energy at any appreciable temperature would induce enough fluctuation of the lattice to preclude sustainability of the film and cause it to segregate into islands or decompose[34]. It was not until 2004 that the first demonstration of graphene was achieved with a rather unconventional method. The method involved separating layers from bulk graphite by physically peeling them away with adhesive tape and transferring onto a silicon dioxide (SiO_2) substrate[32,35]. This has since been referred to as the "scotch tape method", or more formally as micro-mechanical cleavage. The great advantage of this particular technique as compared to previous similar attempt is the ability to distinguish the thickness of a resulting film based on the color it forms when deposited on SiO_2. Utilizing interference effects, the color of the graphene film can be carefully matched to the thickness, down to single layer, by using an optical microscope. Thus, films could be rapidly examined without the need of vacuum or electron microscopy and areas of interest (i.e. few layer graphene) could be identified for further testing. With significant fine-tuning and careful implementation, the "scotch tape" method can provide single layer films tens of micrometers in size. While sufficient for materials research and preliminary investigations, this method is not usable for real scale manufacturing. Other deposition methods will be discussed later in this chapter.

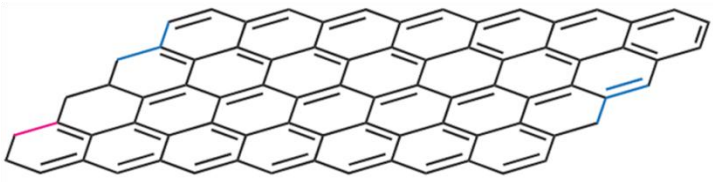

Figure 2.4. Graphene Lattice.

2.3.2 The Magic of Graphene

Graphene's unique structure results in a number of fascinating properties otherwise largely unattainable in bulk materials. Single- and double-layer graphene is a zero-bandgap semiconductor, although a gap can be induced in certain instances, which will be discussed later. Beyond three layers, the electronic structure of graphene become significantly more complicated and structures with 10 or more layers effectively act as thin films of graphite[36]. In a graphene sheet, carbon atoms are sp^2 hybridized allowing delocalization of electrons within the π orbitals which act as free carriers. In fact, charge carriers in graphene acts as massless Dirac fermions and have been shown to reach mobilities of up to 15,000 cm^2/Vs at room temperature[37,38]. Additionally, chirality is observed between electrons and holes and the charge carriers can be tuned from one type to another continuously in the presence of ambipolar electric field. Figure 2.5 demonstrates this principle, where resistivity of a single layer graphene is modulated continuously in both positive and negative bias direction. This will result in (close to) ambipolar transistor characteristics in most cases. The insets show the energy spectra, which are conical at energies below ±1 eV, and the shift in the Fermi level associated with positive and negative V_G. The linear nature of the low-energy band structure gives rise to massless carriers[39].

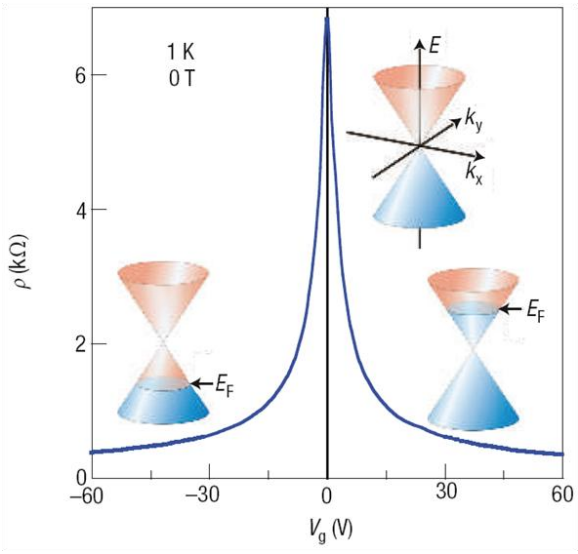

Figure 2.5. Ambipolar electric field effect in single-layer graphene. Insets show conical E-k spectra indicating Fermi energy level at positive, neutral, and negative V_G[34].

2.3.3 Opening the Bandgap

With all its great properties, graphene would likely see little integration into transistors as a gap-less semiconductor. There are, however, ways of inducing (or sometimes forcing) a bandgap in a graphene layer. Perhaps the most elegant and clean way is to utilize the inherent properties of bilayer graphene. It acts similarly to its single layer counterpart, maintaining electron-hole chirality (although the carriers are no longer massless with $m \approx 0.05m_0$) and high mobility. However, it has been shown that upon application of transverse electric field a bandgap can be introduced[40,41]. In its pristine form, bilayer graphene is inversion symmetric AB-stacked and is a zero-gap semiconductor. However, breaking the inversion symmetry introduces a non-zero bandgap, which is precisely the effect of applied electric field. Figure 2.6 shows a schematic representation of the electronic bands separating. Resulting bandgap is a function of applied field and can be up to 300 meV in magnitude. It should be noted, however, that producing this effect requires a double-gate transistor design (Figure 2.6(d)). While quite interesting and useful for material properties investigations, a double-gate design may be prohibitively complicated for full scale, industrial implementation.

Altering the geometry of a single-layer graphene sheet can also create a bandgap. Most notably, sheets patterned into ribbons with widths of several nanometers have been demonstrated to have a gap. In this case the lattice can no longer be approximated as semi-infinite and a large number of edge states are introduced[42,43]. Subsequently, devices made

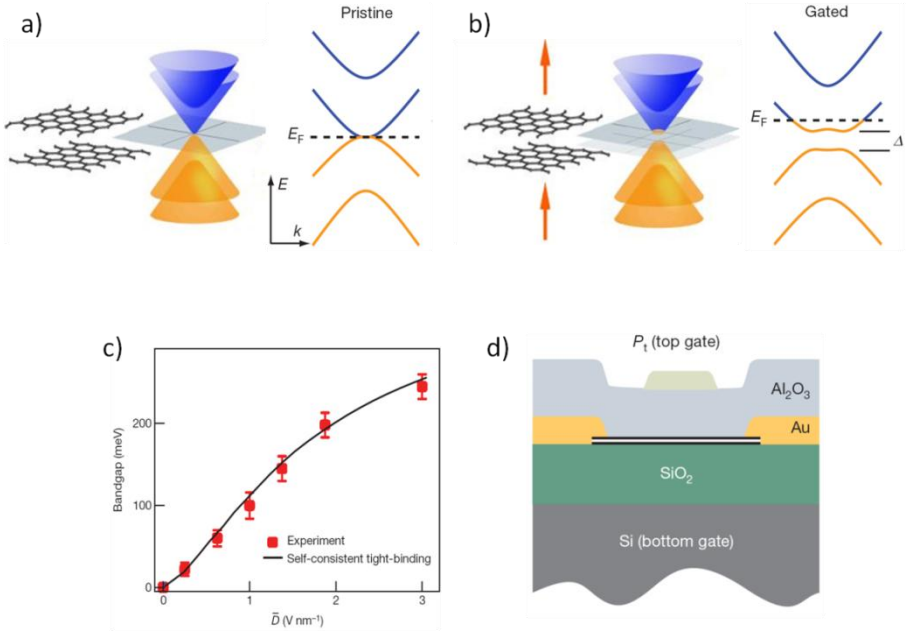

Figure 2.6. a) Electronic structure of pristine graphene, showing zero bandgap. b) Field induced band gap opening. c) Band gap as a function of transverse electric field. d) Cross section schematic of a dual gated graphene transistor[40].

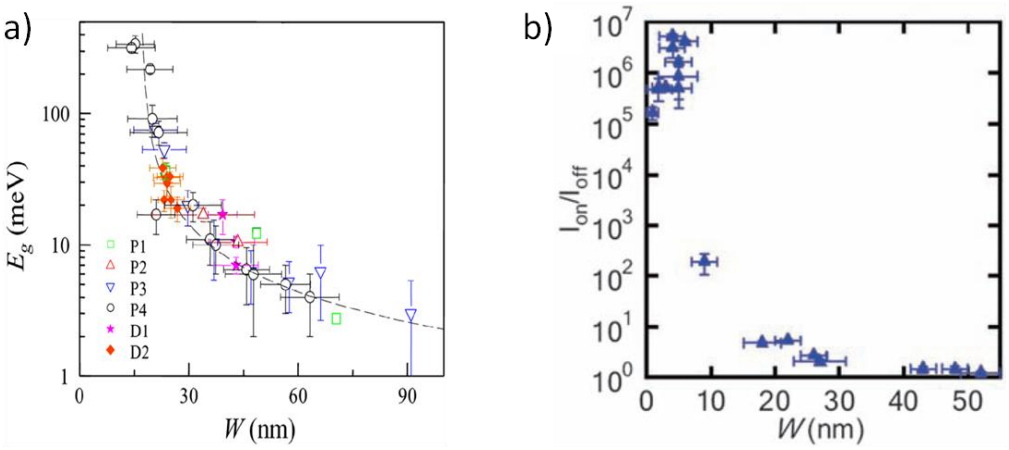

Figure 2.7. a) Band gap as a function of ribbon width. b) ION/IOFF ratio as a function of ribbon width.

out of such ribbons appear more like standard transistors and demonstrate significant on/off ratios. Figure 2.7 shows the bandgap of various nanoribbons and the on/off ratio of resulting devices. It can be seen that a gap of several hundred meV can exist in the narrower samples. By comparing parts (a) and (b) of Figure 2.7, it can be seen that the on/off ratio correlates strongly to the bandgap, as expected.

One can alter not only the physical geometry of graphene but also its electronic geometry. This can be accomplished by introducing graphene to a substrate with a precisely matched lattice which acts as an inversely symmetric layer. It has been shown that growing graphene on a silicon carbide (SiC) wafer can induce a bandgap of up to 260 meV[44]. Figure 2.8(a) shows a schematic representation of a graphene layer on a SiC substrate, and demonstrates the difference of potentials on corresponding sublattices. The effect on the induced gap deteriorates quickly with increasing thickness of the film, and disappears entirely after four layers (Figure 2.8(b)). As expected, thicker films act more like bulk graphite and the intricacies of substrate interactions are lost.

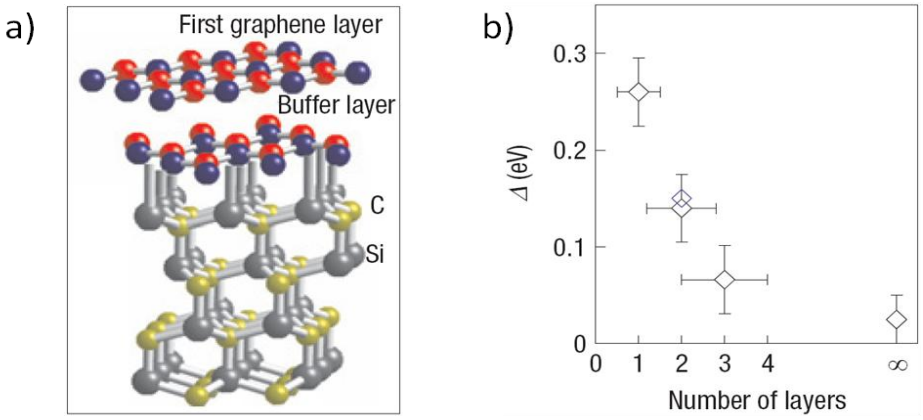

Figure 2.8. a) Schematic diagram of graphene of SiC showing interface induced different potentials on the sublattices. b) Band gap as a function of number of layers[44].

Perhaps the least elegant, and yet most simplistic, way of inducing an effective gap in the energy spectrum of graphene is via chemical alteration, in particular oxidation. Graphene oxide (GO) is an insulator with a bandgap of approximately 2.1 eV[45]. The oxidation causes sp^3 hybridization of the carbon atoms, thereby reducing the number of free carriers present in an sp^2 hybridized lattice. GO possesses many interesting properties which could be utilized in fabrication of solution-processed electronics. These will be introduced in detail later in this chapter. However, for the purposes of current discussion, it is important to note that the bandgap of GO is strongly dependant on the extent of oxidation where a strongly oxidized sample shows a large gap, whereas a pristine graphene sample is a zero-gap material. The gap can be continuously altered based on the level of oxidation[46,47]. When incorporated into a FET, as expected, the resulting devices behave like insulators for strongly oxidized samples and conductors for the pristine ones. Figure 2.9(a) shows the evolution of extracted bandgap based on extent of oxidation. Figure 2.9(b) shows I-V characteristics of TFTs made from graphene oxide reduced back to graphene form to varying extent. It can be seen that the most oxidized samples exhibit the highest on/off ratio at the expense of drive current.

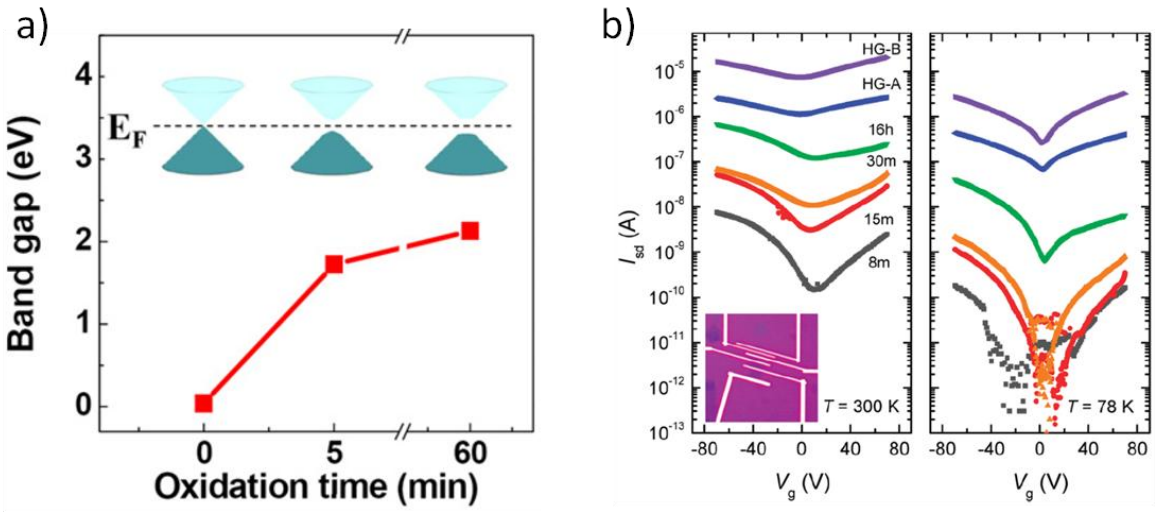

Figure 2.9. a) Band gap as a function of graphene oxidation time. b) I_D-V_G characteristics for reduced graphene oxide samples at various times. HG-A/B are samples reduced in aqueous solution of hydrazine. 8m, 15m, 30m, and 16h are samples reduced with hydrazine vapor for amount of time indicated by the label.

2.4 Graphene Oxide

Graphene can be oxidized to form GO, which possesses a number of interesting properties that make it pertinent to solution-processed electronics. During oxidation some bonds of a graphene sheet break to form bonds with oxide and other carbon functional groups[48,49]. The various functional groups make an individual sheet very hydrophilic and easily soluble in water (and other polar solvents). Once solubilized, material can be deposited via several techniques such as spin-coating, ink-jet printing, spraying, and others.

2.4.1 Fabrication

Separating graphene into individual sheets is commonly achieved by chemical exfoliation, where strong oxidizing agents are used to yield GO. Currently, the exact structure of GO is undetermined, although it is clear that in the oxidized form some of the aromatic rings of the graphene lattice are broken up and decorated with alcohols, epoxides, carboxylic, and other functional groups. This "functionalization" of individual sheets serves two important purposes: one, it breaks up the Van der Waals forces holding the sheets together; and two, it makes the sheets strongly hydrophilic and soluble in water and other polar solvents.

The first demonstration of GO synthesis was performed in 1859[50] by treating graphitic powder with nitric acid and potassium chlorate. However, the most popular route of producing GO is commonly referred to as "Hummers' method", introduced in 1958 by Hummers and Offeman[51]. The process involves mixing graphite powder with sodium nitrate ($NaNO_3$) and subsequent addition of sulfuric acid (H_2SO_4). The solution is then cooled to 0°C to control reaction rate and vigorously stirred. Potassium permanganate ($KMnO_4$) is then added to complete the mixture. The solution temperature is allowed to increase to ≈ 35C and the reaction proceeds for a desired amount of time. At the end of reaction time, the final GO product is extracted by washing. Figure 2.10(a) shows a schematic of graphene in its pristine and oxidized forms.

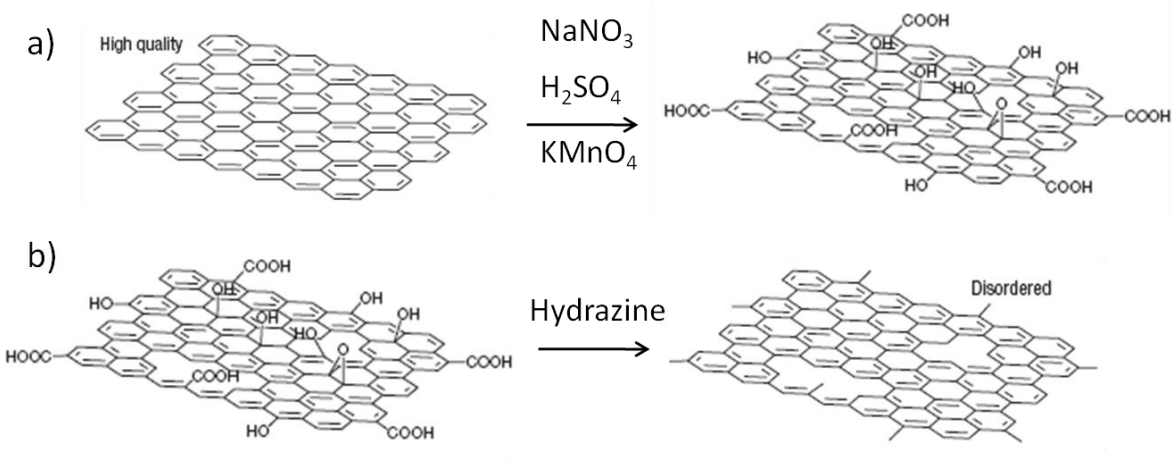

Figure 2.10. a) Graphene lattice before and after oxidation via Hummers method. b) Representation of the graphene oxide lattice and its reduced form.

2.4.2 Reduction

While graphene oxide could be an interesting material in itself, in the context of printed electronics, its most intriguing property is the ability to be converted back to graphene form via chemical reduction. Once converted, reduced graphene oxide (rGO) regains many of the electronic properties that make graphene so attractive, such as low resistivity ($1x10^{-4}$ Ω-cm)[52] and high mobility (365 cm^2/V-s for holes)[53].

Several pathways have been demonstrated for reduction of GO including thermal annealing both in inert atmospheres (vacuum, nitrogen, argon)[48,49,54] and chemically active ambients (hydrogen, forming gas, hydrazine)[47,55,56] and chemical reduction[57]. One of the

most widely used methods, and most promising for ink-jet printing, is reduction in hydrazine (N_2H_4) vapor. Hydrazine is a very strong reducing agent and requires very little thermal assistance (as low as 80°C) to convert GO, which is important for plastic substrate compatibility.

Hydrazine annealing can be performed in various ways. The simplest one is to place a GO sample into a heated enclosure (such as a covered beaker) which also separately contains liquid hydrazine. The atmosphere in the beaker will become saturated with hydrazine vapor which will react with GO and reduce it. Although simple and often utilized, this method is not very precise in temperature control and vapor exposure extent. A more reliable method of introducing hydrazine vapor is through a bubbler system, where an inert gas (N_2 or Ar) is bubbled through a volume of hydrazine solution. The resulting gas mixture with chemical vapor is sourced into a heated chamber containing the samples to be reduced. This method is advantageous as it provides better temperature control through a furnace-like chamber and more precise chemical exposure through gas flow control. Figure 2.11 demonstrates a schematic of a bubbler.

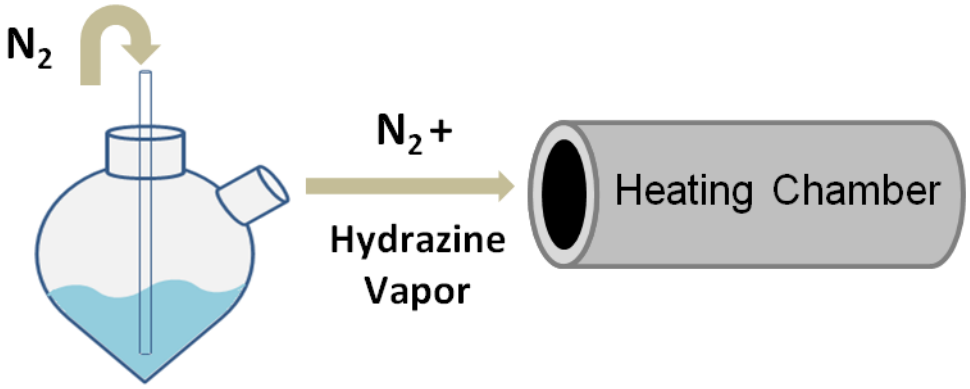

Figure 2.11. Hydrazine bubbler. N2 is bubbled through hydrazine solution and directed into a heated chamber.

It should be noted that the reduction process is not a perfect reversal of the oxidation process. Although a large portion of the oxidizing groups is removed, some are inevitably left over and the resulting rGO lattice is imperfect. Figure 2.10(b) shows a schematic of a sheet of rGO. Clearly, the imperfections in the lattice will have detrimental effects on electrical characteristics, such as mobility. Furthermore, remaining chemical impurities will result in sp^3 hybridization of carbon atoms which reduces the number of delocalized carriers and disrupts their transport through an sp^2 network, reducing conductivity and mobility. Figure 2.12 shows representative electrical behavior as a function of anneal conditions. Part (a) demonstrates conductivity as a function of reaction time in hydrazine at 80°C; it can be seen that the effects saturate after approximately 2 hours of exposure. Part (c) demonstrates the atomic percentage of different carbon bonds as a function of anneal temperature in UHV (identified by XPS) as well as the percentage of sp^2 bonds and total oxygen content (inset). It can be seen that the atomic percentage of desired C-C bonds, and associated sp^2 hybridization, saturates at approximately 80%. This suggests that complete reversal to graphene is not achieved.

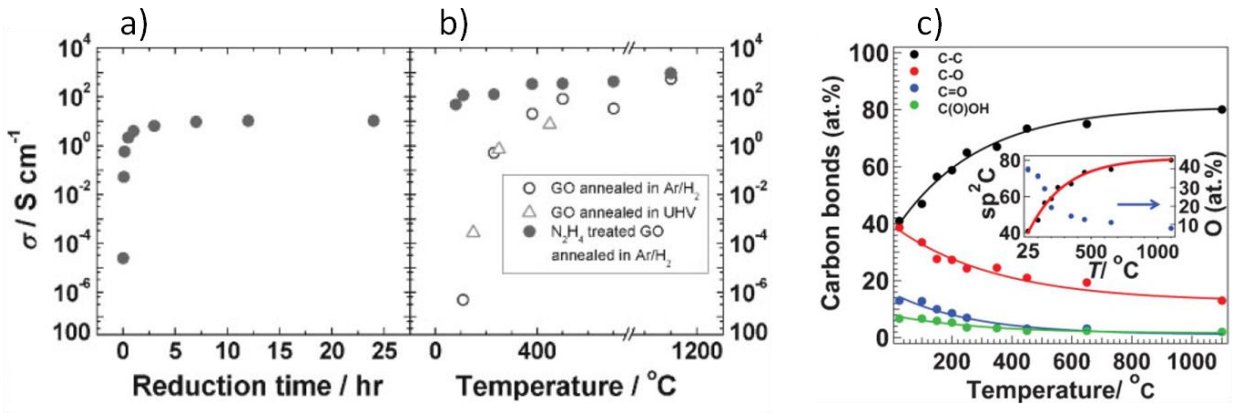

Figure 2.12. Conductivity as a function of (a) reduction time and (b) reduction temperature of GO. c) Concentration of various carbon bonds as a function of anneal temperature.

2.4.3 GO Deposition Methods

A number of methods have been demonstrated for depositing solutions of graphene oxide. One of the more direct ways to deposit any material in solution on a flat surface is spin-coating[58]. It has proven invaluable in the development of many solution-processable materials as a quick and effective means for materials prototyping. Generally spin-coating consists of pouring a solution onto a wafer/substrate and spinning the substrate at desired rotation rate (usually on the order of 500 – 5000 RPM). Solution properties, such as viscosity and mass loading, along with the spin speed determine the final thickness of the resulting film. Spin-coating of GO solutions has been demonstrated before for both electronic and nano-mechanical devices. Although conceptually simple, is not ideally suited for purely aqueous solutions as the surface tension of the drying water will cause formation of small beads and result in a non-uniform films. To remedy this effect, ethanol, or a similar solvent, could be added to reduce net surface tension and allow for more uniform drying.

One of the earlier methods used for obtaining film of GO with controllable thickness was filtration[59,60]. It has been previously used for deposition of carbon nanotubes[61]. A solution containing a controlled concentration of GO flakes would be passed through a filter which would catch the flakes on the surface of the membrane. The filter/GO assembly is subsequently placed onto a substrate (GO face down) and the membrane is removed via dissolution. By controlling the amount and the concentration of the solution used it is possible to produce films of thicknesses down to single monolayers. Although this method is claimed to produce high-yield films, there is an obvious processing complication involving the transfer and dissolution of the filter membrane.

Techniques such as Langmuir-Blodgett deposition[62], templating[63], and spraying[64] have also been shown to produce GO films with varying degree of success. Some of these and previously mentioned methods promise compatibility with low-cost manufacturing; however, none of those are well suited for true large area integration due to issues with large area coverage uniformity and thickness control. Coverage uniformity is critical for device yield while thickness control is essential for electrical properties of graphene, as discussed earlier.

Furthermore, all of these techniques deposit blanket films thereby necessitating post-deposition patterning to achieve proper designs for most electronic applications. Patterning is usually achieved through conventional lithography or stamping techniques. For lithographic patterning, electron-beam (e-beam) techniques can locate an area of graphene favorable for TFT measurements and expose appropriate areas for electrode deposition. Stamping techniques often utilize polydimethylsiloxane (PDMS) or hybrid structures consisting of silicon, glass, and plastic for transferring graphene films which have been deposited on a temporary dummy substrate, hence introducing an extra step to the fabrication process. While these methods have proven valuable for basic investigations of graphene properties, their low throughput (e-beam) and poor registration control over large area (PDMS) make such techniques poorly suited for low-cost, large-area integration.

2.5 Ink-Jet Printed rGO TFTs

Ink-jet printing promises distinct advantages over the previously mentioned solution-processing compatible deposition methods. Firstly, it is ideally suited for low-cost manufacturing due to its all additive, low-waste process. Blanket deposition methods are inherently wasteful as they deposit material everywhere, which subsequently requires removal of some or most of the material to create the desired pattern. In contrast, ink-jet printing is capable of depositing material only where necessary. Furthermore, with simple adjustment of the print program, it is possible to deposit various amounts of material in different locations on the substrate, thereby achieving different film thicknesses. This is useful both for rapid prototyping and, potentially, for manufacturing. None of the blanket deposition techniques offer such flexibility. Additionally, the pattering step itself (usually requiring photolithography) adds additional cost to the fabrication process. Ink-jet printing is also capable of producing uniform micron-sized patterns over large areas and a wide variety of substrates. It can be implemented into roll-to-roll processes for fast throughput manufacturing.

In this section, fabrication and characterization of ink-jet printed rGO TFTs will be presented and their properties will be discussed. For active material prototyping purposes, devices presented here were printed on back-gated SiO_2 substrates. Effects of jetting conditions, substrate temperature, and anneal conditions on device performance will be examined. By controlling printing conditions, uniform films of rGO are achieved. Devices exhibit drive currents up to 1 μA, current ON/OFF ratios of up to 10, and field effect mobilities of up to $0.018 cm^2/V\text{-}s$.

2.5.1 Device Fabrication

2.5.1.1 *Print Ink Optimization*

It is often erroneously assumed that “solution” is synonymous with “ink”. Unfortunately for the printing community that is rarely the case; a material in solution does not always make an optimal ink compatible with jetting. One of the biggest problems plaguing pattern formation via liquid drop deposition is a “coffee ring” effect, first described by Deegan[65]. He showed that non-uniform drying on the surface of a drop leads to an excess of solute at the edge. Figure 2.13(a) demonstrates this principle. Left side shows the evaporation patterns in a freshly deposited drop. On the edges, evaporation proceeds faster as compared to the center. This

causes flow from the bulk of the drop to the edges. As drying proceeds, more solute is transferred to the edges (right side of Figure 2.13(a)). At the completion of the drying process, most of the material ends up on the periphery of the printed feature. Figure 2.13(b) shows a representative cross section of printed drop exhibiting strong coffee ring effect. Clearly, substrate temperature will have an effect on drying rate and dynamics, and increasing temperature is expected to increase convective flow. In fact, it has been shown that increasing temperature can result in a more pronounced coffee ring[66].

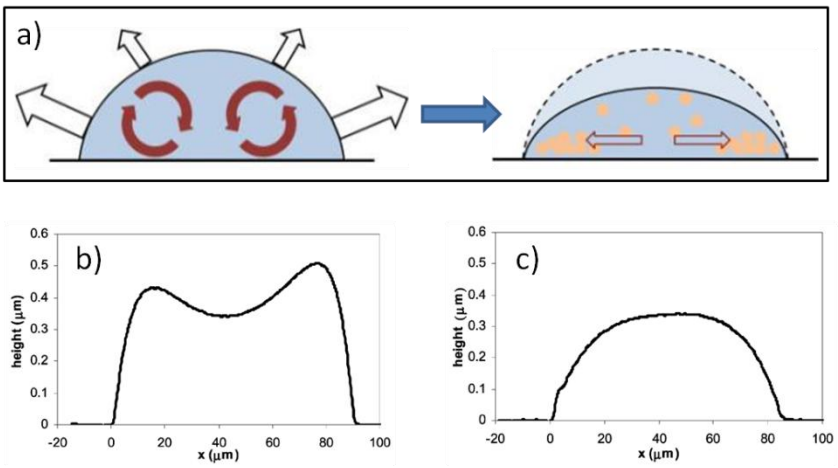

Figure 2.13. a) Schematic of an evaporating liquid drop demonstrating non-uniform drying and resulting convective flow. b) A cross section of a dried drop showing strong CF effect, and c) cross section of a drop without CR effect.

To ameliorate the coffee ring problem a dual solvent system can be introduced. It has been shown that by combining two solvents dissimilar in volatility and surface tension more uniform drops can be obtained. Multi-solvent systems can be used to increase a surface tension enhanced flow inside a drying drop[67,68]. This is often referred to as "Marangoni effect"

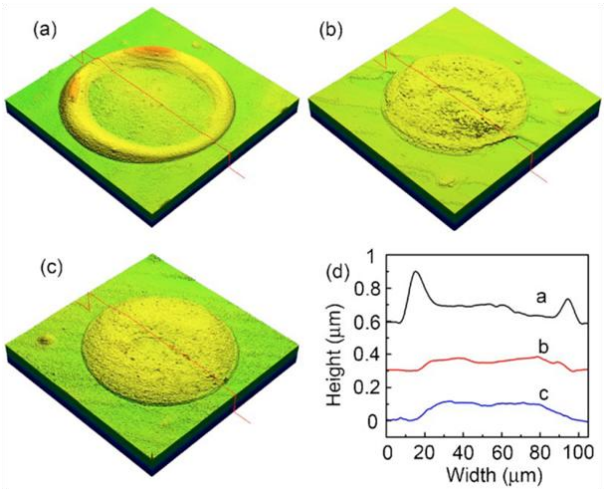

Figure 2.14. Top view images of aqueous silver nanoparticle solution drops with (a) 0, (b) 16, and (c) 32 wt% EG. d) Corresponding cross section profiles[68].

which states that mass transfer will occur in a liquid from an area with low surface tension to an area with high surface tension. It has been shows that addition of ethylene glycol (EG) to water eliminates the formation of a coffee ring (Figure 2.14). The proposed mechanism is as follows: in a freshly deposited liquid drop evaporation proceeds faster at the edges, which creates an excess of EG at the edges as it evaporates slower due to higher boiling point. This in turn generates a surface tension gradient in the drop due to a difference in surface tension of EG and water (γ = 48 mN/m and 72 mN/m, respectively). Thus, an inward Marangoni flow is induced carrying solute from the edge towards the center of the drop (i.e. low to high surface tension). In the case of water/EG system, this induced Marangoni flow is sufficiently large to offset the convective flow generally responsible for the coffee ring effect.

2.5.1.2 *Experimental Setup and Sample Preparation*

GO flake solutions were prepared via the Hummers method which was described earlier. After oxidation, the GO slurry was ultrasonicated, centrifuged for cleaning, and suspended in water. The loading of the final solution was approximately 0.3 mg/ml of GO flakes in water. The ink was filtered through a 5 µm Nylon filter before printing to remove agglomerated particles and prevent clogging of the print head.

Bottom-gate structures were used for printing and testing. A heavily doped n++ substrate served as the conductive gate and a 100 nm of thermally grown SiO_2 layer served as the gate insulator (as illustrated in Figure 2.1). Both top and bottom contacts structures were used. Bottom contacts consisted of a chrome/gold (Cr/Au) stack of 2.5/50 nm deposited by thermal evaporation. These were defined by standard lithographic step followed by liftoff. Top contacts consisted of printed silver inks annealed at 150 °C in air. GO inks were deposited at various substrate temperatures and drop conditions. After deposition, GO films were subjected to a two step anneal process. An initial "pre-anneal" step was performed in a N_2 ambient at temperatures of 150°C – 250°C to drive off excess solvent and EG. The second step was performed in a hydrazine bubbler chamber (as described earlier) to reduce GO at temperatures of 80°C – 150°C. Figure 2.15 shows optical micrographs of devices with printed and evaporated S/D contacts. The slight variations in the rGO film morphology and the dissimilarity with the SiO_2 substrate result in a variation of the surface energy experienced by the printed silver lines. Consequently, the lines exhibit line edge non-uniformity.

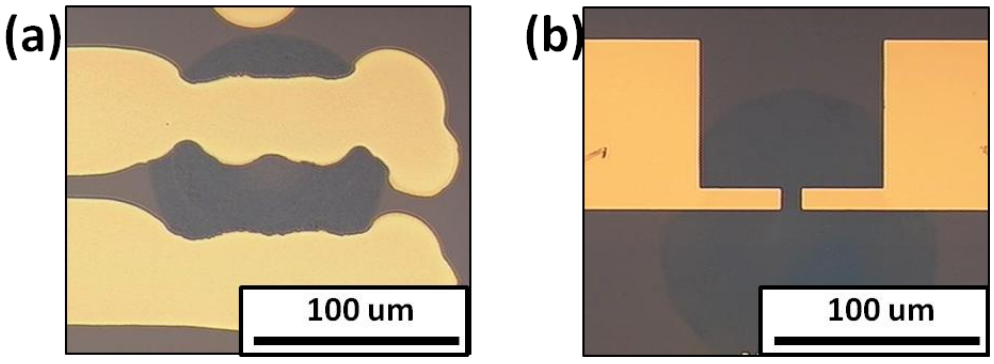

Figure 2.15. Optical micrographs of rGO devices with (a) printed Ag top contacts and (b) evaporated Au bottom contacts.

GO inks were printed with a custom-built ink-jet printer. The printer consists of a substrate holder with lateral and rotational movement (accuracy of approximately 1μm). Ink delivery is performed via a piezoelectric actuated print head manufactured by Microfab Inc. with nominal nozzle size of 60 μm and drop volume of 100 pL. The ink is stored in a pressure controlled reservoir and fed to the head via a Teflon tube. Commercially available CCI-300 silver particle ink from Cabot Corporation was used for silver top S/D contacts structures. Metallic ink was printed with a Dimatix DMP 2800 printer. Cr/Au contacts were deposited in a standard thermal evaporator at base pressure of approximately 2e-6 torr.

Electrical measurements were performed with an Agilent 4155/6 parameter analyzer. Atomic force microscopy (AFM) measurements were taken with a Veeco Dimension 3100.

2.5.2 Results and Discussion

2.5.2.1 *Print Conditions*

As described earlier, ink composition and substrate temperature play a critical role in determining the final print feature morphology and it is important to optimize both to achieve desired film quality. Three types of inks were evaluated: pure water, water + ethanol, water + EG. As expected, pure water resulted in a pronounced build up of material at the edges, likely due to induced convective flows. Addition of ethanol also resulted in undesirable drop profiles, most likely due to an additional outward Marangoni flow. Ethanol has lower boiling point and surface tension than water (T_b = 78°C and γ = 22.4 mN/m). As a result, the edge of a drying drop will evaporate ethanol faster and result in an excess of water. The water rich region will have higher surface tension and induce an outward Marangoni flow, thus enhancing the undesired transfer of solute to the edge.

Addition of EG and proper control of temperature was found to give the best results with GO flake inks. Combination of 4 – 5% EG with water produces the desired inward Marangoni flow to counteract the outward convective flow. Figure 2.16 shows optical micrographs of dried drops printed at various temperatures and drop counts. Multi-drop features were printed immediately, i.e. no drying time was implemented in between individual drop depositions. It can be seen that substrate temperature of 40°C produces the most uniform films. At 25°C, coffee rings are clearly present and become more pronounced with increasing drop count. At 50°C, material agglomeration occurs in the middle likely due to the fact that inward Marangoni flow becomes more pronounced at higher temperature.

The thickness of the graphene film or, more precisely, the number of individual layers plays a dramatic effect on its electronic properties. As shown in Figure 2.8(b), the bandgap approaches zero as the number of layers is increased past three. To achieve semiconducting behavior, it is important to maintain close-to-single-layer films. Going past three layers will result in a more “metallic” behavior of the film. Consequently, TFTs produced from semiconducting films are likely to show better device characteristics than the metallic films. Figure 2.17 shows AFM images of the features obtained at various print conditions. Part (a) shows an edge of a multi-drop feature printed at substrate temperature of 25°C. It can be seen that the height of the coffee ring is approximately 7.1 nm which corresponds to 7 layers of rGO

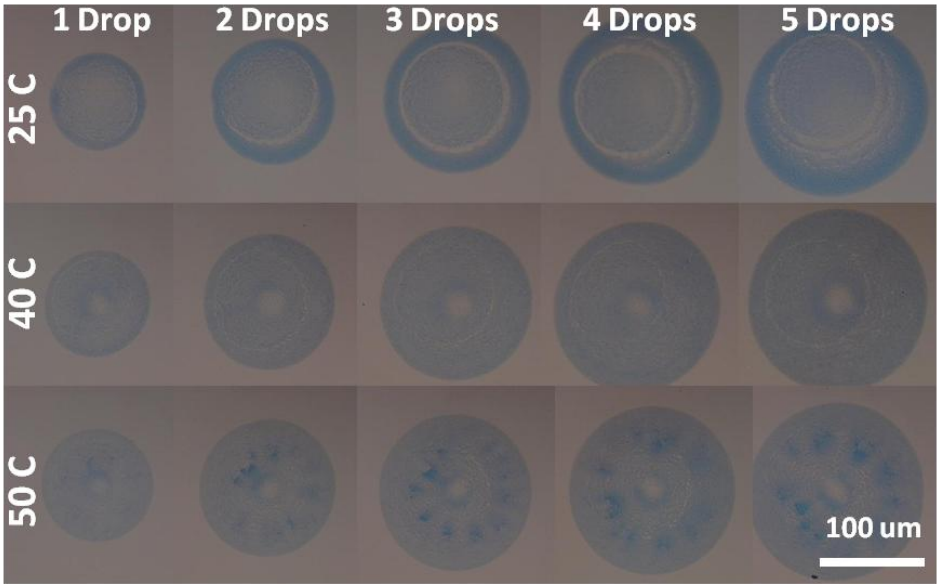

Figure 2.16. Optical micrographs of GO inks printed at various temperatures and drop counts.

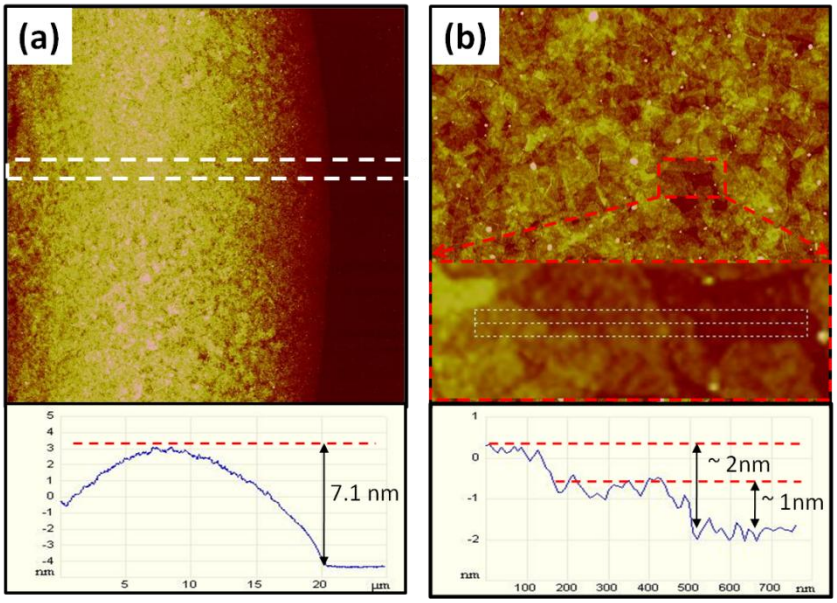

Figure 2.17. (a) AFM micrograph of the edge of a printed feature resulting in a "metallic" device, showing a relatively thick, multi-layer graphene. (b) AFM micrograph of a printed feature resulting in a "semiconducting" device, showing near single-layer film structure.

(it has been shown that a single layer of rGO is approximately 1 nm, depending on the fabrication/reduction process[55,69]). This type of morphology is expected to result in a more metallic behavior. Figure 2.17(b) shows and AFM image of a feature printed at 40°C. It can be seen that the film consists of 1- to 3-layer rGO, which should result in a more semiconducting behavior and allow much better gate control in a TFT structure. Cross-sectional AFM analysis shows that thickness of an individual sheet is approximately 1 nm.

2.5.2.2 *Device Characteristics*

TFT device characteristics corresponding to various print conditions were examined. Figure 2.18 shows representative I-V curves for a metallic (5 drops, 25°C) and a semiconducting (3 drops, 40°C) device. After GO deposition, devices were annealed at 200°C in N_2 and 90°C in hydrazine for 1 hour each. Subsequently, silver S/D contacts were printed and annealed in air at 150°C for 1 hour. It can be seen that a "thick" device (Figure 2.18(a)), with a pronounced coffee ring effect, exhibits more metallic behavior. It has higher drive current of 0.98 µA and lower ON/OFF ratio of 1.63 (ON/OFF ratio is defined as maximum to minimum I_{DS} measured at V_G = 5V and 0V, respectively). In contrast, a more semiconducting device (Figure 2.18(b)) exhibits a higher ON/OFF ratio of 5.2 at the expense, of lower drive current of 0.26 µA.

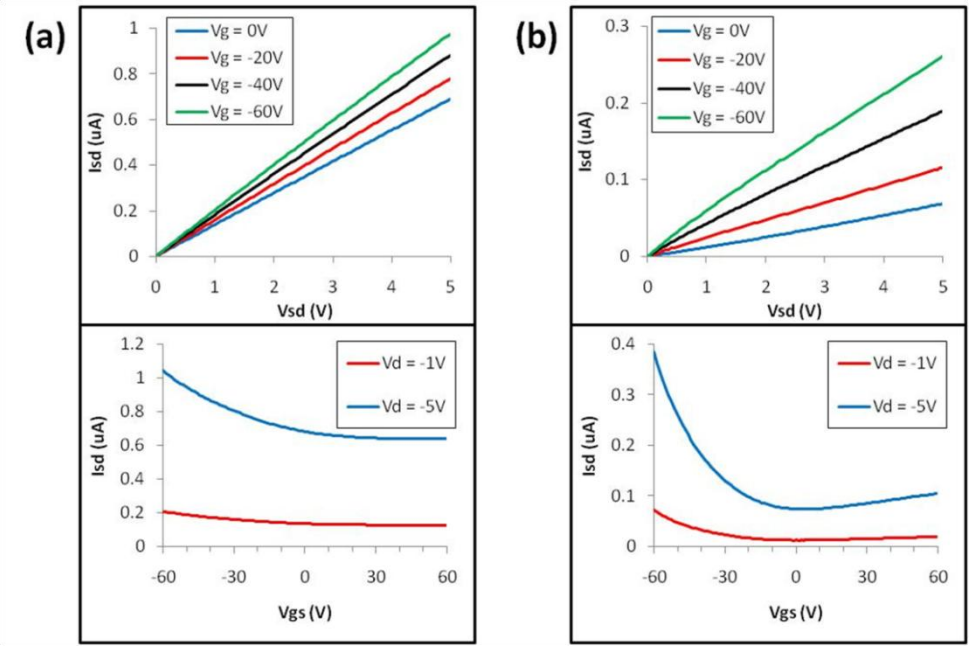

Figure 2.18. I-V characteristics for (a) metallic and (b) semiconducting device.

Mobility of these devices was calculated using the extracted transconductance with a square-law approximation (as detailed earlier). Extracted values for linear mobility are 0.018cm^2/V-s and 0.015cm^2/V-s for the metallic and semiconducting devices, respectively. Seemingly, film thickness has a minor-to-negligible effect on mobility. Mobility values obtained in this work are lower than reported by some groups working with rGO. This is likely due to two factors: first, the GO flakes that were used in this work are on the order of 1 µm or less, whereas the publications that quote significantly higher mobilities often utilize much larger flake sizes (up to 25 µm). Consequently, charge conduction happens through many more flake-to-flake interfaces, or effective "grain boundaries". Second, and perhaps more important, is the fact that all other works utilize lithographically patterned S/D contacts located close enough to span a single or very few sheet of rGO, which dramatically improves transport characteristics. Thus, there appears to be room for improvement with the presented ink-jet printed TFT devices. Although it is unclear whether advanced printing processes will ever be created to effectively reach S/D separations similar to lithographically patterned versions, there is

definitely room for improving ink formulations to incorporate larger sheet of GO and increase drive currents.

Previous analysis clearly demonstrates that device characteristics depend strongly on the printed feature morphology. The effects of print conditions were studied in more detail. Data was collected on 5 – 10 devices for each point. Figure 2.19(a,b) shows the effects of drop count and substrate temperature on drive current (I_{ON}) and ON/OFF ratio. As the number of drops increases, the thickness of the film increases which in turn increases I_{ON} while decreasing the ON/OFF ratio. This is consistent with the assumption that the increase in thickness will make the films more metallic, which would result in more conductive layer (higher I_{ON}) and degradation of gate control (lower ON/OFF ratio). It can also be seen that the ON/OFF ratio is least affected for features obtained at 25°C, because even at 1 drop the metallic multi-layer coffee ring (Figure 2.16) dominates the conduction. As a consequence, in 25°C prints, increasing drop count and thickness results in higher drive current while the ON/OFF ratio remains almost constant. In contrast, films printed at 40°C and 50°C show a sharp decline on ON/OFF ratio as the drop count increases from 1 to 2 as the film morphology likely transitions from close-to-single to multiple layers. Deposition of more than 2 drops results in a monotonic decline of ON/OFF ratio. Figure 2.19(c) demonstrates the relationship between I_{ON} and ON/OFF ratio for devices printed at various conditions. As expected, there is a strong inverse correlation between drive current and effectiveness of gate control. To verify the robustness of the process I-V characteristics of several devices fabricated at the same print condition were compared. Figure 2.19(d) shows I_D-V_G characteristics of devices printed with two drops at 40°C. It can be seen that the electrical response is quite similar.

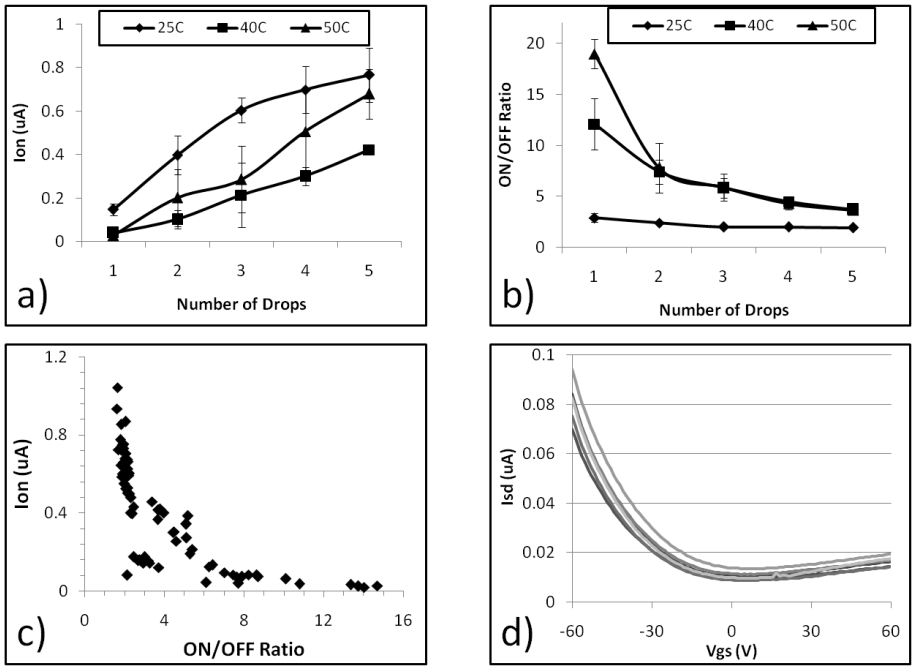

Figure 2.19. a) I_{ON} as a function of number of drops, b) ON/OFF ratio as a function of drop count, c) I_{ON} distribution vs. ON/OFF ratio, and d) I_D-V_G curves of multiple devices printed as a given condition.

2.5.2.3 *Anneal Effects*

Annealing conditions used in GO reduction play an important role in the resulting device characteristics. In this work effects of two types of anneals at various times and temperatures were examined. To simplify the fabrication process, devices used in this experiment were manufactured on evaporated S/D contacts consisting of a Cr/Au stack. Data was collected on two sets of devices: one set was used to test the effects of N_2 anneals and the other for hydrazine. Hydrazine treatment consisted of a two-step anneal process, where the initial 60 minute N_2 anneal was performed to remove excess solvent and EG, and was followed by the hydrazine anneal. Each set was annealed at a specified temperature and electrical data was collected at 10, 20, 40, and 80 minute marks. Subsequently, data was normalized to the initial value obtained at the 10 minute mark.

Figure 2.20 (a and b) shows normalized drive current and ON/OFF ratio as a function of time for samples annealed in N_2 at 200°C. It can be seen that the ON/OFF ratio increases initially and saturates after 20 minutes. This increase can be attributed to an improvement in drive current as a consequence of the thermal treatment. Drive current continues to increase with time, which is likely due to continuous conversion of GO towards graphene. Furthermore, the lack of saturation suggests incomplete conversion after 80 minutes.

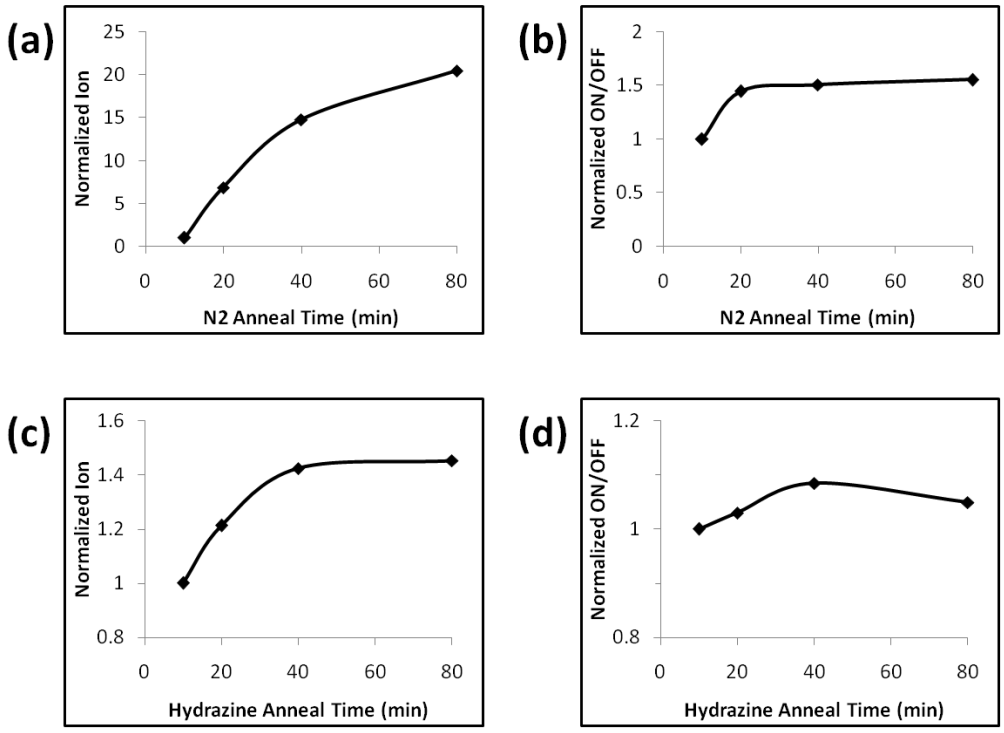

Figure 2.20. (a) Normalized I_{ON} and (b) ON/OFF ratio vs. N_2 anneal time at 200°C. (c) Normalized I_{ON} and (d) ON/OFF ratio vs. hydrazine anneal time at 150ºC.

Figure 2.20(c and d) demonstrates normalized drive current and ON/OFF ratio as a function of time for samples annealed in hydrazine at 150°C. ON/OFF ratio seems largely unaffected by the hydrazine treatment, which is likely related to the first step in the treatment

of the hydrazine annealed samples (a pre-anneal at 200°C in N_2). During that step, ON/OFF is saturated as suggested in Figure 2.20(b). In contrast, drive current increases by 45% after and saturates after 40 minutes of hydrazine exposure suggesting a limit to the reduction process at the given temperature.

2.5.2.4 *Viability of rGO TFTs*

Although rGO devices presented here hold a promise of fully solution-processed transparent TFTs, several issues still need to be resolved, in particular with respect to LCD incorporation. Although drive currents and mobilities achieved are sufficient to drive a basic liquid crystal cell, a higher ON/OFF ratio is required to successfully operate a large pixel array. An array with a large number of pixel rows (over 100) requires select transistors with ON/OFF ratio of over 10^5[1]. Currently, basic rGO transistors, including the ones discussed in this work, are incapable of achieving such current ratios.

It may be possible to improve ON/OFF ratios of printed rGO transistors by modifying the ink or the device structure to realize lower leakage current. A dual-gate device structure could be implemented to decrease leakage current. As discussed earlier, applying a high transverse electric field can induce a bandgap widening in dual-gated bilayer graphene devices. Such a device could be fabricated by modifying the printing process presented in Figure 2.2 to include an additional top dielectric and gate contact. This, of course, would add processing steps and complexity to the fabrication flow. Furthermore, this would only be effective with bilayer films, whereas printed films achieved so far consist of areas with 1 – 3 layer graphene. Consequently, in order to maximally utilize the dual-gate structure, printing of rGO should be further optimized to achieve bilayer films.

Alternatively, if an ink containing primarily graphene nanoribbons could be produced, it could be used to fabricate printed devices with much higher ON/OFF ratios. As discussed earlier, the bandgap and, consequently, the current ratio of a graphene ribbon is inversely proportional to its width. Li et. al. were able to produce such solutions, which consisted mostly of graphene nanoribbons, via a combination of chemical and mechanical (sonication) routes[43]. They have also examined devices made of single nanoribbons which exhibited high current ratios; however, these were achieved with S/D contacts lithographically defined in predetermined locations of interest. In contrast, printing a nanoribbon ink would likely form films with randomly oriented ribbons, where some may span the entire channel length, while most of the channel would consist of a network of ribbons. This would likely result in a decrease in current density, as compared to a device with a single ribbon bridging the channel, as conduction will be dominated by inter-ribbon transport. However, it should nonetheless result in high effective channel bandgap and an improved ON/OFF ratio.

2.6 Summary

Ink-jet printed reduced graphene oxide transistors were demonstrated. Ink-jet provides a consistent deposition technique compatible with large-area, high-throughput integration and capable of good control of deposited film thickness and morphology. Devices were manufactured with printed Ag and evaporated Cr/Au contacts, and showed well-behaved characteristics. Manufactured devices exhibited mobility on the order of $2x10^{-2}$ $cm^2/V\text{-}s$, and

ON/OFF ratios of up to 10. Deposited GO films were reduced at 200°C in N_2 or 90°C – 150°C in hydrazine. Anneal tests showed that hydrazine treatment was required for maximum reduction of GO at the investigated temperatures. Low temperatures required to convert oxidized graphene into rGO, make this material well suited for plastic-compatible, low-cost manufacturing.

3 Graphene Conductors

Although often overlooked in "state-of-the-art" and "the future of electronics" discussions, conductors are an integral component of electronics. Transistors are generally assumed to be the heart of modern technology; however, it is possible to have a wide range of functional electronics without a single transistor but not without conductors. Conductors serve a number of critical roles from transistor-to-transistor interconnects, to discrete IC components on a circuit board, to board input/output (I/O) contacts to the outside world. They are necessary and often influential in determining performance of a given component. A perfect example of that is a solution-processed TFT, where even the best structure with the best semiconductor must still be matched to the proper source/drain conductor to achieve good performance.

To become successful outside of the purely academic realm, a fully solution-processed fabrication flow needs to incorporate a variety conductor components including connections within TFTs, connections between devices, and connections to the outside of the package. Individual components may necessitate different requirements and it is important to identify the various constraints in order to achieve the desired final product.

3.1 Applications and Requirements

3.1.1 LCD Electrodes

LCD displays have steadily become more and more widespread in our society almost to the point of ubiquity. An LCD display seems to decorate even the most benign of electronic gadgets (e.g. a toothbrush). As discussed in the introduction chapter, an LCD display pixel consists of multiple components; various conductor components associated with it will be discussed here. Perhaps the most important from operational standpoint and demanding from material properties standpoint is the pixel electrode of a cell. In a conventional LCD, two properties for pixel electrode material are of particular importance: high transparency and low resistivity. A flexible display adds a further restriction of being robust to a certain amount of bending and stretching.

Currently, indium tin oxide (ITO) is the dominant material used for pixel electrodes in LCD displays. Liquid crystal (LC) material is sandwiched between two planes of ITO electrodes which control the electric field across the switching layer. This ITO/LC/ITO sandwich can be thought of and modeled as a capacitor which needs to be charged and discharged to achieve the restructuring of LC molecule backbones and switching of the pixel. Inherent to this capacitor is the resistance of the contact electrodes which have to be included in RC delay considerations when estimating the total delay time. Currently ITO electrodes on the order of 100nm – 200nm are used with resistivities on the order of $1x10^{-5}\Omega$-m and transparency in up to 90%[70].

Although ITO has been the workhorse of the display technology, there are a number of issues which may prevent it from widespread use in flexible electronics. From an economic

perspective, ITO is becoming a problem due to a shortage in supply of indium which resulted in an increase in prices over recent years[71]. While conventional LCD industries have been able to absorb this so far, it may become a significant problem for low-cost printed electronics. Additionally the costs associated with the conventional deposition and lithographic patterning of ITO will also be prohibitive. Furthermore, ITO has been shown to inject indium and oxygen ions into the active media, thereby decreasing voltage response performance over time[72].

In addition to cost implications, ITO has technical barriers preventing it from integration in flexible electronics; in particular, its poor stability during bending. Robustness of ITO on plastic substrates such as PET has been studied before[73]. Figure 3.1 shows the effects of strain as a result of bend tests on ITO films of approximately 100 nm thick. It can be seen that significant degradation occurs at strains over 1%, with thicker films being more brittle and less resistant to flexing[74]. Furthermore, ITO films are not very robust against repetitive bending. In test comparing polymer (such as PEDOT) to ITO coatings, polymers showed negligible degradation in conductivity, whereas ITO films showed significant increases in resistance or complete line failure after 100 – 300 cycles[75]. Clearly conductors with high modulus of elasticity, such as TCOs and most of the metals currently used in LCD production (Cr, Ta), have to be replaced with alternate materials with low modulus of elasticity (such as Ti or Al). Alternatively, a material strongly resistant to strain degradation could be used. Graphene promises to be such a material; it has been shown to significantly outperform ITO is strain tests on plastic substrates[76]. Figure 3.2 shows the effects of strain applied by bending on the change in resistance of graphene films. It can be seen that the electronic effects on graphene films are negligible compared to effects on ITO. Additionally, graphene can exhibit low resistivity of 10^{-7} Ω-m – 10^{-6} Ω-m and high transparency of over 90%.

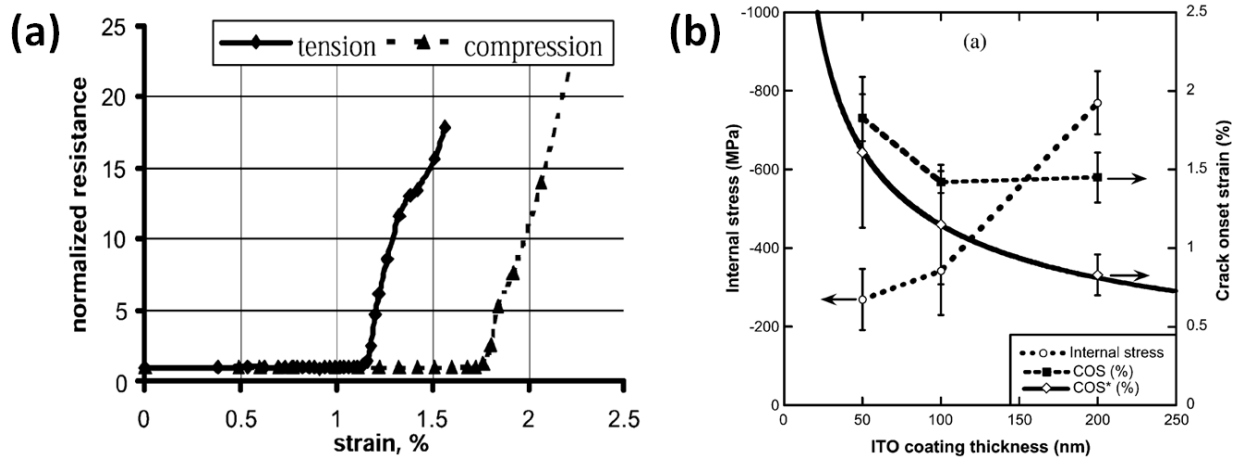

Figure 3.1. a) Resistance of ITO coatings as a function strain under tension and compression, b) Internal stress and crack onset strain as a function of ITO thickness.

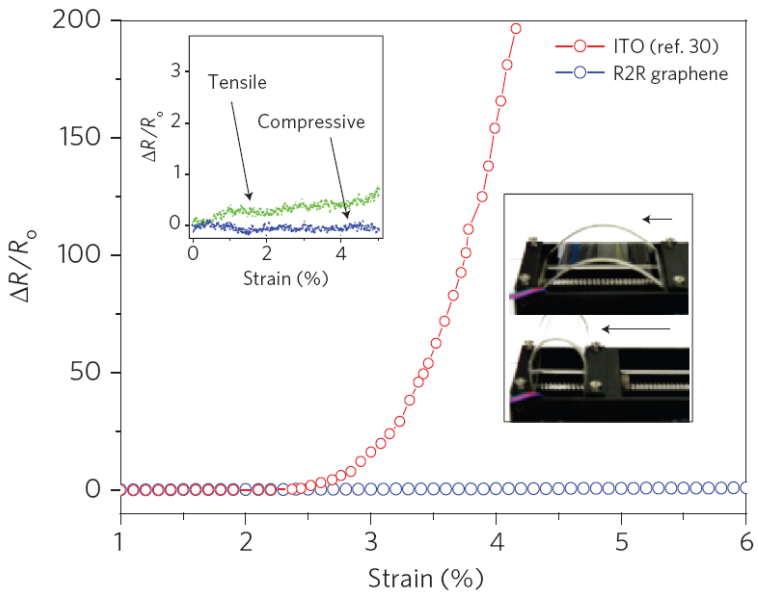

Figure 3.2. Change in resistance as a function of strain for graphene and ITO films on a plastic substrate.

3.1.2 Interconnects

Interconnects account for a significant amount of metal used in electronics, from low level contacts that bridge individual transistors, to medium level interconnects that link system level blocks such as logic or memory, to circuit board level contacts that connect multiple chips.

Circuit boards have been used in electronic devices such as radios well before transistors entered the scene. Nowadays they are ubiquitous in electronics and comprise the backbone of most devices holding together discrete IC components. Generally a printed circuit board (PCB) comprise of multiple layers of metal separated by a dielectric[77]. Each layer is patterned in a desired way to implement appropriate contact schemes and is connected to other layers through via contacts. Patterning usually happens via a mask-and-etch process of a laminated or electroplated blanket film. As such, this is a subtractive and inherently wasteful process. Copper is generally used as the metal because of low resistivity, while epoxy filled fiberglass is used as the dielectric. With the constant increase in miniaturization individual IC components have also become smaller and I/O connection schemes denser. As such demands on metal line pitch and thickness in a circuit board have also increased and are becoming a concern for a very cost-sensitive industry.

This is particularly pertinent to flexible circuit boards, where a delicate balance between flexibility and electronic performance is critical. Flexible circuit boards are found in a number of applications including connection between rigid boards in multi-dimensional packaging, connections to moving parts, and connections in tight spaces such as a digital camera. These boards can be quite complicated and capable of holding discrete components. The requirements for flexible boards are similar to those of regular PCB with the additional demand that materials used are capable of withstanding large numbers of bend cycles. The construction of a flexible circuit board is largely similar to that of a regular PCB, where patterned layers of

metal are separated by a dielectric; however, special caution needs to be taken to assure that none of the components are too brittle. For metals this usually means selecting metals with a lower young's modulus (such as aluminum). Additionally, a more robust encapsulation layer is required to prevent moisture and oxygen penetration into board as that would lead to a degradation in conductivity. All of these requirements place additional costs to the fabrication process. Incorporating a low-cost printing process could reduce the costs of metal deposition and patterning.

On a lower level, interconnects play a critical role of serving as the contacts to the semiconductor of an individual transistor as well as contacts between transistors and other elements. On a transistor level, contacts have to be selected appropriately to ensure suitable match to the semiconductor. This applies both to energetically, where the work function of the metal makes an ohmic contact, and from a physical materials compatibility perspective, where the metal-semiconductor interface has to have a low defect count in order to avoid Fermi level pinning and excessive recombination. In conventional silicon this is easily achieved by using highly-doped Si as initial metallic contact. This ensures proper band alignment and good physical contact. (The highly-doped region is then contacted with a metallic via through a silicide). In printed TFTs this is a much harder task as all the individual components are dissimilar (for example, a common case of gold electrodes on an organic semiconductor). Thus, the search for the properly matching materials becomes even more important and complicated. The rest of the chapter will deal in more detail with the topics discussed in this section and discuss reduced graphene oxide (rGO) as a candidate conductor for the applications of interest.

3.2 Conductive Inks

To incorporate a fully solution-processed fabrication flow into any of the applications discussed, deposition of conductive inks is clearly necessary. Various approaches have been tried towards achieving such inks and a number of candidates emerged based on the following concepts: conducting polymers, metal nanoparticles, metal flakes, organo-metallics, and inorganic carbon.

Electrically active organic compounds have been known to exist since the 1950s. The discovery of a range of conducting and semiconducting polymers is largely responsible for the popularization of printed electronics. With the advent of electrically active polymers that could be dissolved in common solvents and deposited in solution to create a functional film, solution-processed electronics became a more realistic possibility. Generally organic compounds are insulators; however, in the case of conjugated molecules with alternating single and multiple bonds, delocalized electrons will exist. These delocalized electrons are responsible for high electrical conductivity in such systems. Conjugated systems are most often semiconducting, but can be made more metallic by introducing oxygen doping, which removes electrons and creates an excess of holes. These organic semiconductors are often p-type, hence increasing hole concentrations results in an increase of conductivity.

Some of the most commonly used organic conductors are based on poly(ethylenedioxythiophene) doped with polystyrenesulphonate (PEDOT:PSS)[16], polyacetylene[78], and polyaniline[79]. These polymers have a wide range of both industrial

and academic uses such as coatings in antistatic packaging, transparent conductors in some packaging applications, hole transport layers for organic diodes and solar cells, and contacts to organic semiconductor devices. Unlike polymers in general, conducting molecules are usually more difficult to dissolve in common organic solvents due to their salt-like nature, thus making it harder to incorporate into a printable ink. Furthermore, their electronic properties can be affected greatly by introduction of moisture and oxygen as those can affect the oxidative state of a molecule and in turn the carrier concentration. Thus organic conductors have seen a fairly limited integration into areas of electronics where consistent performance is critical.

Some of the most widely used metallic inks for device research in academia consist of metal nanoparticles. Such inks are capable of providing highly conductive films at fairly low, plastic-compatible temperatures. They utilize the fact that melting temperature of a particle is significantly suppressed with decreasing size. Figure 3.3 shows results from some of the earliest work done on investigating gold nanoparticle melting temperatures[80]. It can be seen that below 50 nm melting temperature of a particle drops dramatically.

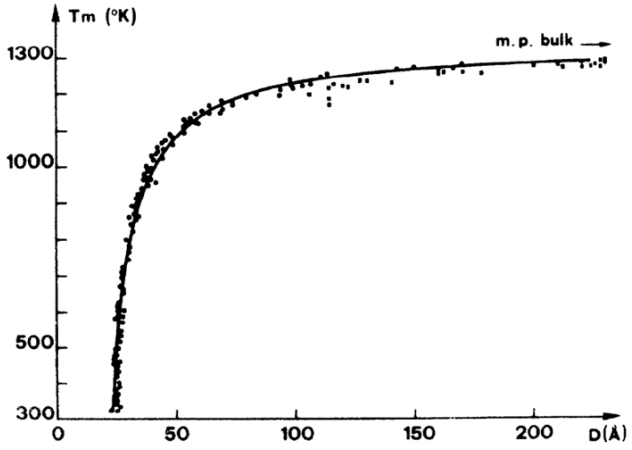

Figure 3.3. Melting temperature of gold nanoparticles as a function of particle size.

Nanoparticle inks often consist of individual particles encapsulated with a surfactant and dissolved in an organic solvent or, in some cases, water. The surfactant can serve several purposes: prevent particle agglomeration, prevent particle chemical reactions such as oxidation, and increase solubility in a given solvent. After deposition, the inks can be thermally treated and converted to continuous films of mostly elemental metal. In a well engineered ink, several processes take place: evaporation of the solvent, de-encapsulation and volatilization of the surfactant, and sintering of the nanoparticles into a film. Depending on ink formulation, these processes are driven to various levels of completion. For example, not all the encapsulant material is necessarily removed during the sintering process, which may result in an imperfect contact between particles. However, overall metallic inks are well capable of producing conductivities of over 50% of bulk at plastic compatible temperatures[81].

A wide range of nanoparticle inks have been developed and a number of those can be obtained commercially. Silver has become the metal of choice for ink-jet development since it is significantly cheaper than gold and it is more stable that copper and aluminum. Although silver

does form an oxide easily, it does not result in a significant degradation in conductivity since the oxide itself is conducting, which is not the case with copper. A large number of synthetic pathways have been developed to achieve silver inks including silver ion reduction, reverse micelles reduction, and thermal decomposition in organic solvents. These methods can produce a wide variety of particle shapes and sizes. Some of these have been formulated into inks with mass loadings of up to 80% and a broad range of ink viscosities which could be utilized in printing techniques such as ink-jet, screen, and gravure.

Nanoparticle inks are a good candidate for wide range integration in solution-processed fabrication since they form stable, high-performance films, multiple material systems are available which allows appropriate work-function matching to desired semiconductors, and they can be processed at plastic compatible temperatures. However, these systems may have issues with colloidal stability over long periods, which have negative impacts on printability, final film roughness due to particle agglomeration or crystallization, and the likelihood of material mismatch with semiconducting materials which may result in imperfect contact behavior. Additionally, metal particle films are not transparent, which makes them less desirable for some display applications.

A more direct (if not less elegant) pathway towards metallic inks is metal powder. Such inks are usually formulated by simply combining powders of a metal with a solvent/polymer mixture to achieve a slurry of desired consistency. The simplicity of this process, especially compared to potentially complicated synthetic pathways for metal nanoparticles or organic conductors, makes this type of ink very cost competitive. Consequently, metal powder based slurries are most often used in the industry as metal inks. These inks produce films of fairly large particles (on the order of 10s μm to 100s μm) which have enough contact to neighboring particles to create effective electron conduction paths. As a result, no thermal treatment is required to initiate a conversion into a conducting film. The films are usually annealed only to drive off excess solvent and, sometimes, to harden the polymer/binder to ensure mechanical stability. Thus, these types of inks are quite useful in applications where thermal budget is critical. However, the large size of the powder particles is also detrimental to film roughness which will be strongly affected by the size of individual particles.

Another method of achieving a metallic film is through the use of organometallic precursors. These are compounds which contain a carbon structure with bonds to metal atoms. These can be combined in solution with other mild reacting agents and additives and deposited via standard solution-processing techniques. Such pathways have been developed for a wide variety of materials including silver, gold, platinum, and others. In general, such inks consist of an organometallic compound, one or multiple reacting agents responsible for the decomposition and conversion of the compound, and various additives which could be used to control reaction rate and film morphology. After deposition, an annealing step is used to initiate the reaction and decompose the organometallic compound into elemental metal. These inks are attractive due to their straightforward formulation and good achievable conductivities. However, resulting films are often chemically impure which may cause deterioration of adjacent materials. Additionally, organometallic inks are usually of low viscosity and mass loading, which results in films which are too thin or mechanically unstable.

All of the metallic inks discussed so far fit well in certain applications but not others, and it seems all of them have been utilized for some purpose or another. However, none of these are ideally suited for a solution-processed display application. An ideal ink would be capable of producing transparent films with high conductivity, and would also be easy to produce and print. Inks based on graphene oxide (GO) flakes could meet these requirements. This chapter will discuss the merits of rGO films achieved with such inks and present data on ink-jet printed rGO conductors.

3.3 Graphene Conductors

3.3.1 Properties of graphene conductors

Graphene possesses a multitude of fascinating properties which were discussed in the previous chapter and some of those properties make graphene and its derivatives very attractive to transparent and flexible electronics. Properties like transparency, low resistance, chemical stability, mechanical strength, and good interface characteristics with organic electronic materials. Since the first "scotch-tape" deposition method has been demonstrated, researches have managed to fabricate graphene and its derivatives in a variety of ways. It has also been incorporated into a variety of devices related to the fields of flexible and transparent electronics. Devices such as liquid crystal cells, organic light emitting diodes (OLEDs), dye-sensitized solar cells, as well as organic and inorganic TFTs as both a S/D electrode and active material.

ITO currently dominates as the conductor of choice for most transparent electronics applications; however, as described earlier in this chapter, alternative materials are being sought after due to ITOs cost and incompatibility with flexible substrates as a result if its brittleness and poor bend cycling stability. In contrast graphene shows excellent bend and strain stability, as well as good electrical and optical characteristics required for display applications. Graphene resistivities down to 10^{-6} Ω-m with transmittance of over 90% have been shown. Native sheet resistance of graphene is on the order of 6 kΩ, which is one conductivity quantum per species of charge carriers)[82]. It can be reduced to 50 Ω with artificial doping while maintaining high transmittance. Several research groups have investigated transparency of graphene films deposited by a variety of methods. Figure 3.4 demonstrates absorption and transmittance of such films obtained through a scotch-tape and chemical vapor deposition (CVD) methods. It can be seen that a single layer of graphene absorbs about 2%, which is significantly lower than that of ITO (15-18%[83]). As expected, there is an inverse relationship between the number of layers and sheet resistance. Resistance of approximately 100 Ω/□ is achieved at a thickness of 4 layers which corresponds to transmittance of 90%. Although large LCD applications require lower sheet resistance values (approximately 20 Ω/□), these characteristics should be sufficient for use as a transparent conductor in a flexible display application[84].

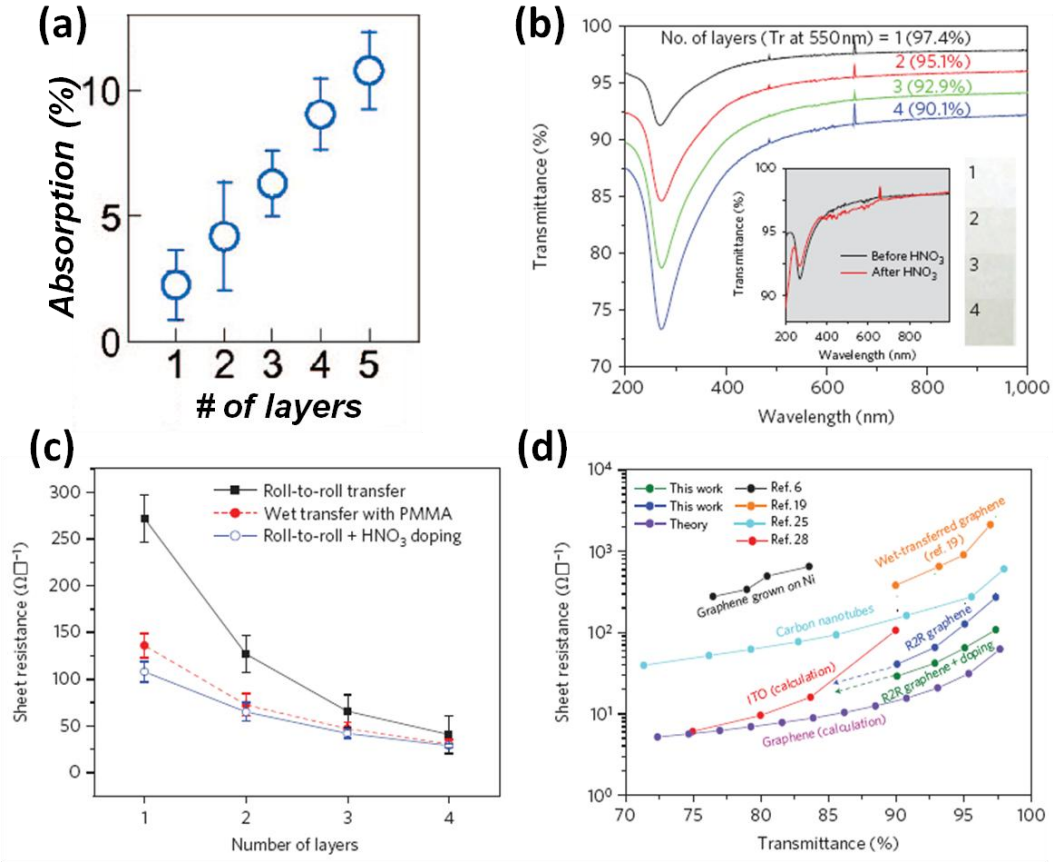

Figure 3.4. a) Light absorption of suspended graphene of different thicknesses. b) Transmittance spectra of graphene films. c) Sheet resistance of graphene films as a function of thickness. d) Sheet resistance vs. transmittance for various graphene films.[76,82]

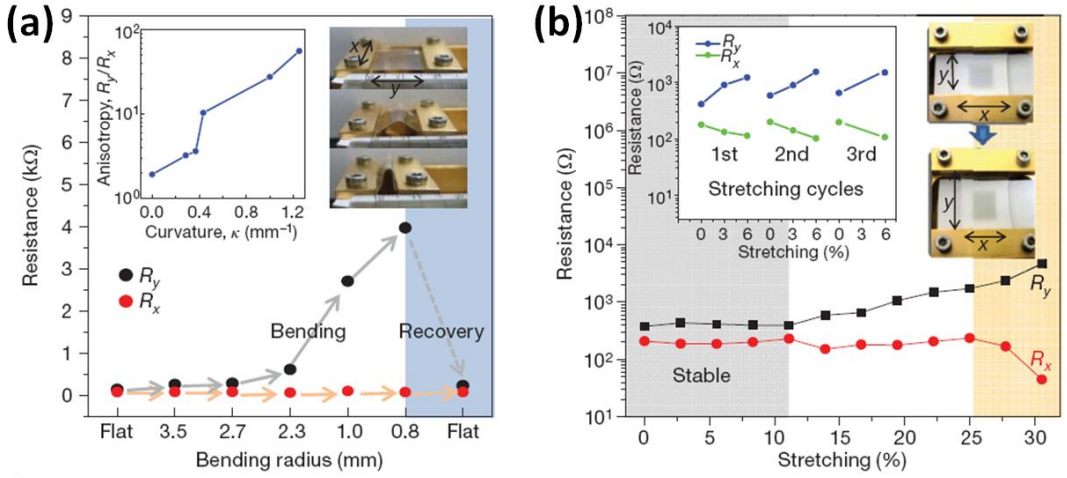

Figure 3.5. a) Resistance as a function of bending radius of graphene on PET. b) Resistance of graphene films deposited on prestrained substrates as a function of stretching %.[85]

Response to stretching and bending plays a critical role in selection of a proper conductor for a flexible application. Figure 3.5 demonstrates resistance response of graphene films as a function of bending[85]. These films were grown by CVD on nickel substrates and transferred onto plastic sheets. It can be seen that resistances vary little with bending radius up to 2.3 mm, which corresponds to strain of approximately 6.5%. Furthermore, resistance recovers fully even after bending to a radius of 0.8 mm (representative of approximately 18% strain). Generally, graphene has been shown to be stable at strain levels of up to 6%. However, if deposited on a pre-strained substrate, upon relaxation of which ripples in the film develop, such films can be stretched up to 11% without degradation in resistance as demonstrated in Figure 3.5(b). This level of mechanical robustness far exceeds that of conventional ITO.

3.3.2 Incorporation of Graphene Conductors

Liquid crystal cells based on graphene contacts have, in fact, been demonstrated with graphene as a replacement to ITO[82]. Figure 3.6(a) shows a schematic of a graphene LC cell. In an LC cell, the electrode is generally covered with a polymer layer which is rubbed after deposition to create alignment groves for LC molecules to conform to. In these samples polyvinyl alcohol (PVA), which is a standard alignment layer, was used. PVA induces n-type doping in pure graphene sheets, and, in this particular sample, it resulted in a drop of graphene sheet resistance down to 400 Ω, while still maintaining transparency of about 98%. Figure 3.6(b-e) shows transmittance response at varying applied bias (8 Vrms – 100 Vrms). The contrast ratio, as defined by maximum to minimum transmission, is approximately 100:1 under white light illumination, which demonstrates the potential graphene for this type of application.

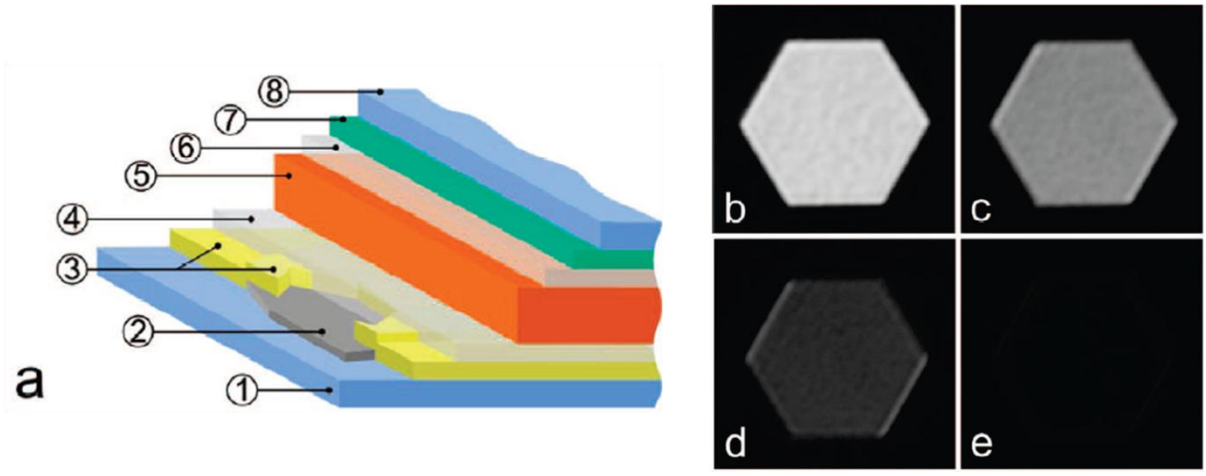

Figure 3.6. a) A schematic of the liquid crystal cell: 1) glass; 2) graphene; 3) Au/Cr contacts to graphene; 4) PVA alignment layer; 5) LC material; 6) PVA alignment layer; 7) ITO; 8) glass. Parts (b-e) optical micrographs showing light transmission at cell voltages of 8 Vrms, 13 Vrms, 22 Vrms, 100 Vrms, respectively[82].

A number of demonstrations have also been made of graphene as a contact for organic semiconductors in both diode (OLED and solar cell)[86,87] and transistor structures[88,89]. In addition to optical and mechanical properties described earlier, graphene has a work-function on the order of 4.6 eV – 4.9 eV. This is similar to gold work-function, a common metal contact

for organic TFTs, and usually matches well with the highest occupied molecular orbital (HOMO) of many p-type organic semiconductors, thus lowering the Schottky barrier[88]. Wu et. al. have fabricated OLED structures with solution-processed rGO as a conductor and compared those to conventional ITO devices for control[90]. Figure 3.7 shows the electrical and optical response of rGO based cells compared to ITO. It can be seen that ITO performs better at current densities greater than 10 mA/cm^2. This is attributed to a relatively high sheet resistance of rGO films achieved in this study (approximately 800 Ω/□) and an associated parasitic voltage drop at high current. Figure 3.7(b) shows external quantum and luminous power efficiencies; again, rGO based devices have similar characteristics to those fabricated on ITO. The authors believe that optimizing the rGO deposition and annealing methods can further improve the overall performance of such cells.

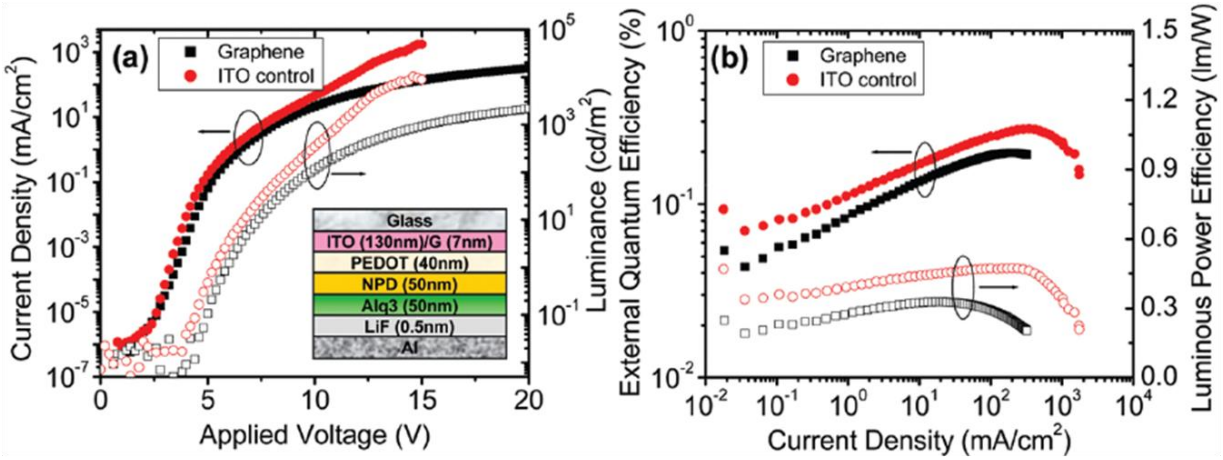

Figure 3.7. a) Current density and luminance as a function of applied voltage of an OLED on graphene and ITO. b) External quantum efficiency and luminous power efficiency as a function of current density for graphene and ITO based OLED[90].

Incorporation of graphene contacts into TFT structures has been shown to improve device characteristics significantly. Semiconductor/contact interface plays a very important role on overall device performance, particularly with decreasing channel lengths. The nature of a contact/organic interface is complicated. The inherent dissimilarity of the materials can cause a disorder of the semiconductor near the contact or induce unfavorable dipoles at the interface. This could be detrimental to carrier injection and transport properties. To ameliorate this problem a variety of techniques have been used such as introducing organic monolayers to the contact[91] or coating it with an organic conductor like PEDOT:PSS[92]. However, low conductivity of organic conductors may introduce unfavorable parasitic resistance. Lee et. al. have demonstrated significant improvements in an OTFT by incorporating a solution-processed rGO contact interface layer[93]. Figure 3.8(a,b) shows I_D-V_D characteristics of a base device with Au contacts and device with a hybrid (rGO/Au) contact. It can be seen that the rGO layer improves drive current by almost a factor of 5. Furthermore, a decrease in the S/D barrier is observed in the hybrid contact device. An improvement in effective mobility can also be observed (Figure 3.8(c,d)). The hybrid contact improves mobility by a factor of 3.

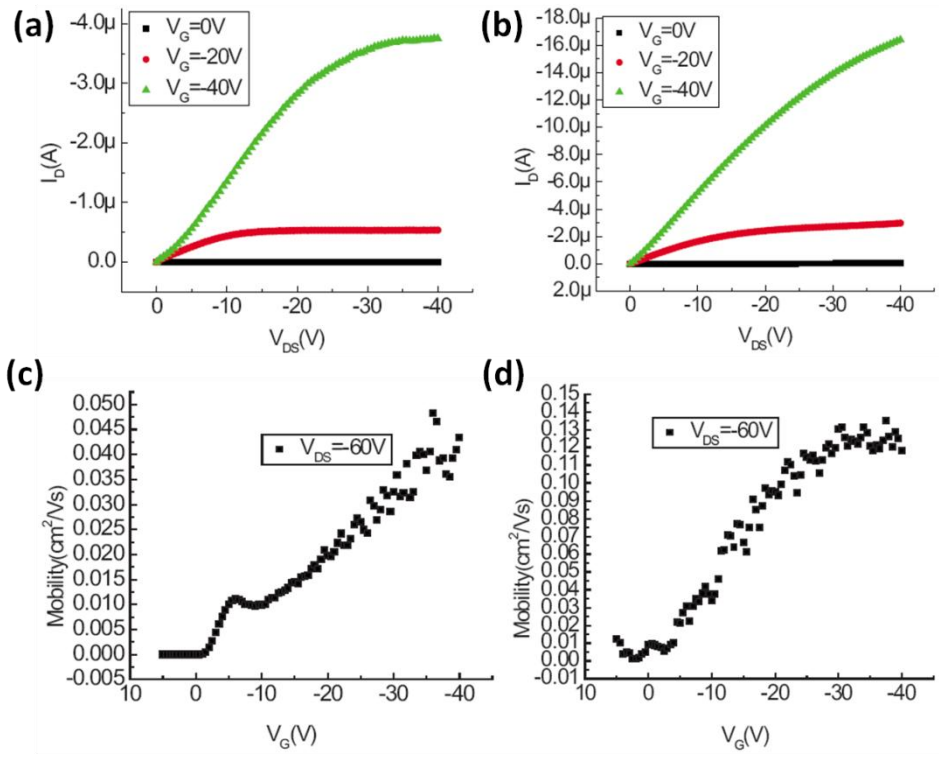

Figure 3.8. I_D-V_D characteristics of a device with (a) pure Au contacts and (b) rGO-coated Au contacts. Mobility as a function of V_G for (a) pure Au contacts and (b) rGO-coated Au contacts[93].

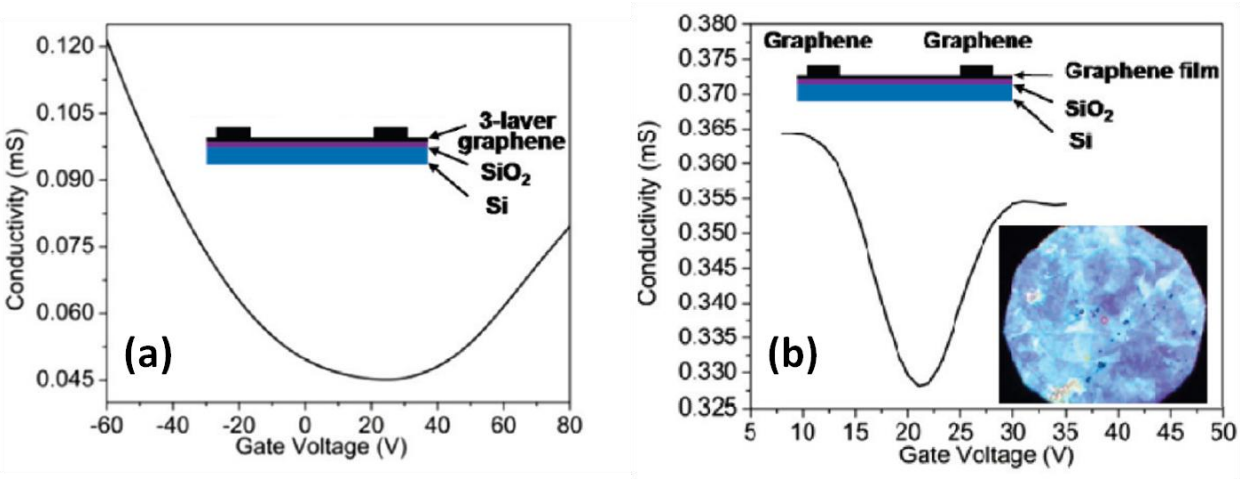

Figure 3.9. a) Transfer characteristics of a tri-layer rGO TFT. b) Transfer characteristics of a tri-layer rGO TFT with rGO contacts[94].

Perhaps, one of the more exciting applications for graphene conductors in the context of printed electronics is as an S/D contact in an all-graphene TFT. As discussed earlier, by controlling the thickness of deposited graphene films, their electronic properties can be tailored towards either semiconducting or conducting. This could be easily achieved via ink-jet printing.

Wang et. al. have fabricated an "all-graphene" device based on solution processed rGO[94]. Figure 3.9 shows conductivity as a function of gate voltage for a control device with gold S/D contacts and an full-rGO device, both with 3-layer graphene active region. It can be seen that conductivity is improved with rGO contacts and the extracted mobility increases from 51 cm^2/Vs and 92 cm^2/Vs to 281 cm^2/Vs and 365 cm^2/Vs for electrons and holes, respectively. This is attributed to a reduction of contact resistance and injection barrier due to interfacial π-π interactions of at the contact/semiconductor interface. This demonstrates the great potential of rGO as a solution-processed material for TFT applications. However, lithographic techniques coupled with high temperature anneals (1000°C) were used in this work to fabricate devices.

All the examples of graphene incorporation into various applications discussed so far attest to the material's potential as candidate for flexible, transparent, and solution-processed electronics. However, a fully printed, plastic-compatible device is yet to be demonstrated. Generally post deposition patterning techniques (lithography and etching) and large anneal temperatures are used. Clearly a printable, plastic-compatible conductor is desired to allow graphene incorporation into low-cost flexible electronics. The rest of this chapter will discuss fabrication and characterization of ink-jet printed rGO conductors.

3.4 Fabrication

3.4.1 Printing Conditions Optimization

Unlike active material in a TFT which usually can be (and should be) confined to a small area, conductors have to span larger areas and carry electrical signal throughout a given system via long lines. Printing lines present challenges in addition to those associated with printing drops, as discussed in the previous chapter. All the problems related to coffee ring (CR) formation, surface tension related morphology imperfections still apply. In fact, solutions for dealing with CR have been sought after since the inception of the printed electronics field. It has essentially the same effect on lines as it does on single drops, where the solute is pushed to the edge of the line and the center of the line is left empty. Figure 3.10 shows a top view of a line with and without pronounced CR effect[68]. As expected, the more uniform line exhibits significantly lower resistivity. Some of the earlier attempts to solve this problem involved printing at high temperatures such that each drop dries immediately after landing before the subsequent drop lands. This results in a "coin stack" morphology, where adjacent coffee rings are offset and stacked on top of one another. Figure 3.10(c) demonstrates a top view of a resulting line[81]. It can be seen that the coverage is more uniform and conduction through the bulk can easily proceed in such a line; however, this type of morphology is far from perfect. The stacking introduces excessive roughness which is undesirable, especially for multi-layer structures as it may result in localized fields and spikes through a dielectric. In general, smooth and uniform lines are desired. Fortunately, solutions used to mitigate the CR problem in drops also apply to printed lines. Dual-solvent systems of mixed boiling point and surface tension could be used to induce a favorable Marangoni flow and result in a more uniform line (as in Figure 3.10(b)).

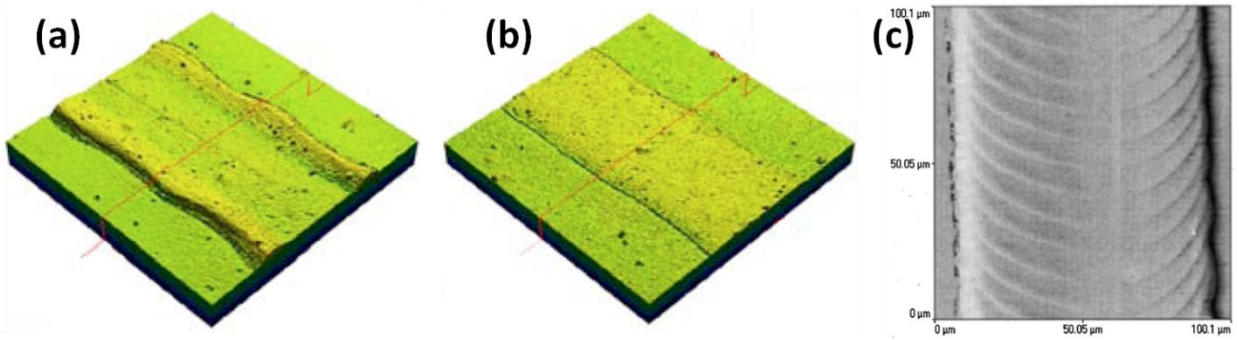

Figure 3.10. Top view of lines printed with aqueous Ag inks with (a) 0% and (b) 32% EG. (c) Printed Au line with "coin stack" morphology[68,81].

In addition to the coffee ring problem, line formation is sensitive to the solvent surface tension and line pinning effects. A long line of liquid represents a higher energy state than a drop or sphere. Thus liquids with high surface tension, such as water, are often unstable in a line configuration and tend to separate into individual beads. Figure 3.11 shows an image of the line right after printing and one after allowing the solvent to relax and bead up. Clearly, this renders the printed feature unusable as a conductor. This effect is particularly problematic in ink/substrate interactions where contact line pinning effect is weak.

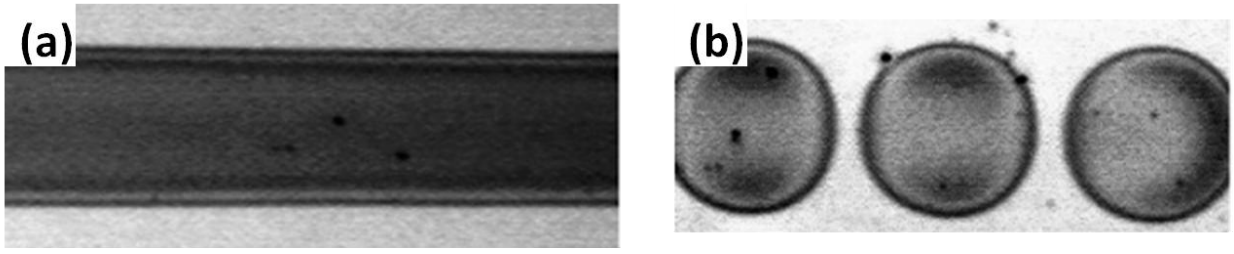

Figure 3.11. Optical micrographs of (a) as-printed line before drying and (b) beads resulting from line separation.

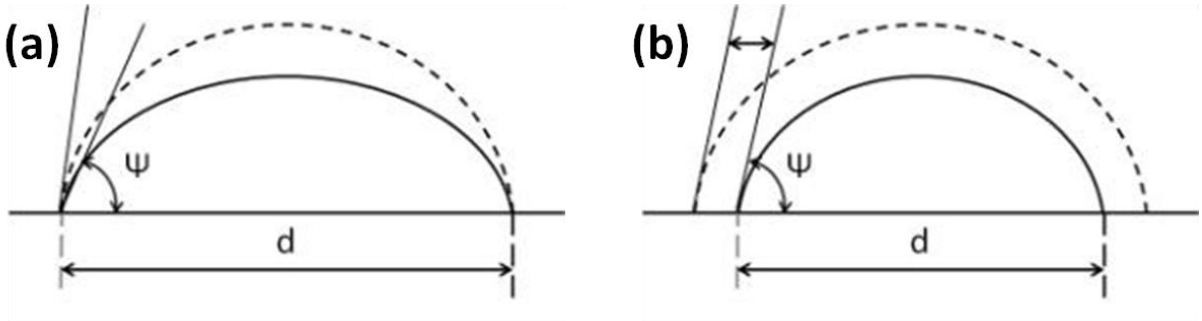

Figure 3.12. Drying dynamics of a line (a) with and (b) without a pinned contact line.

Contact line pinning describes the phenomenon where the edge of a deposited liquid is fixed after deposition and throughout the drying process. Pinned systems differ greatly from the non-pinned ones both in drying process dynamics and resulting feature morphology. Figure

3.12(a) shows a schematic of the drying process in a pinned drop. After deposition, the diameter, *d*, is fixed, thus the contact angle, *ω*, decreases as the volume decreases through solvent evaporation. In contrast, a non-pinned drop maintains the original contact angle while the diameter decreases during evaporation. The exact origin of contact line pinning is yet unclear, but it is thought to be related to some, or all, of the following: surface/solvent chemical attraction, surface roughness, ink mass loading, and chemical or physical impurities[95-97]. Irrespective of its origin, line pinning may have a dramatic effect on final drop/line morphology. A non-pinned system may move all the solute to the center as the solvent recedes resulting in poor coverage. Often complete or partial pinning is desired to ensure a smooth and uniform line. Additionally, contact line pinning may mitigate the effects of surface tension by preventing the beading process.

Pure water inks printed on smooth, clean surfaces such as SiO_2 are particularly problematic from the standpoint of surface tension and contact line pinning. The most direct approach to resolving the surface tension problem is to introduce a co-solvent with a lower surface tension. Common solvents like ethanol and methanol have been used to improve the surface roughness of solution-deposited graphene films before[98]. Additionally, several pathways to induce line pinning have been suggested in the literature; these include: surfactant addition, surface roughening, and increasing ink loading. For the purposes of this work, surface roughening is undesired as it is generally detrimental in electronic applications, where as mass loading was largely limited by the solubility of GO flakes in water. As the last option, addition of several surfactants commonly used for ink formulations was tried, including Triton, Tween, and ethylene glycol butyl ether (EGBE). Unfortunately, none of these induced sufficient contact line pinning to result in smooth continuous lines. Consequently, even with a reduction of surface tension, the complete lack of line pinning prevented proper line formation at room or moderate temperatures. Therefore, for the purposes of first stage investigation, high substrate temperature (90°C – 110°C) was used to cause immediate drying of the drops and prevent line separation. Inks containing 5% of ethylene glycol (EG) were investigated as well. It should be noted that, although very useful for initial exploration, high temperature printing is generally not desirable. Consequently, a better engineered ink would likely be required for real process integration.

3.4.2 Experimental Setup and Sample Preparation

Same GO flake inks were used as described in Section *2.5.1.2*. Samples were printed on test silicon wafers with 100 nm of thermally grown SiO_2. Four point measurements were performed in two ways: one, by using direct probe to the printed rGO lines. Two, by first printing Ag contacts over the rGO lines. After deposition, GO lines were subjected to either N_2 anneals in a glove box, or hydrazine anneals in a custom bubbler (as described in Section *2.4.2*). Anneal temperatures were 200°C – 350°C for N_2 and 80°C – 150°C for hydrazine.

Cabot CCI-300 inks were used for Ag contacts. Printing of GO inks an Ag inks was as described in Section *2.5.1.2*. Electrical measurements were performed with an Agilent 4155/6 parameter analyzer. Atomic force microscopy (AFM) measurements were taken with a Veeco

Dimension 3100. XPS measurements were performed on a PHI VersaProbe Scanning XPS Microprobe.

3.4.3 Substrate Temperature and Print Frequency Control

Both substrate temperature and drop print frequency affect the drying characteristics and adjacent drop interactions. As substrate temperature increases, the solvent evaporation increases hence allowing the printed feature less time to flow and restructure itself. Similarly, increasing the time between consecutive drops allows a drop to dry more completely before the next one arrives, thus minimizing chances of redissolving and reflow. Since water was used as the primary solvent in this work, substrate print temperatures of 90°C – 110°C were selected around boiling point of water. Inks containing EG were printed at temperatures of 100°C – 130°C. Print frequency was controlled indirectly by introducing artificial wait times between successive drops of 0 ms, 30 ms, and 50 ms, which would correspond to print frequencies of approximately 30 Hz, 20 Hz, and 12 Hz, respectively, depending on line drop spacing (ds).

Figure 3.13 shows a set of lines printed at the substrate temperature of 90°C with varying drop spacing. It can be seen that ds = 5 µm gives a fairly dense line; however, coffee rings are clearly present and line edges are thicker than the center. Going to ds = 30 µm the lines get less dense, the coverage is incomplete, and the individual drops become more identifiable. Clearly, a spacing of 5 µm produces the most desirable line in terms of coverage. Figure 3.14 shows lines printed at various temperatures for drop spacings of 5 µm and 10 µm. It can be seen that at higher temperature (110°C) the jetting can become unstable, as evidenced by irregular patterns in the line. This effect is less visible at 5 µm spacing as the line is denser. Overall, adjusting the wait time and frequency seemed to play little role on line quality directly but did affect jetting stability. The drops were least stable at a wait value of 0 ms and became much more stable once a wait time of 30 ms or 50 ms was introduced.

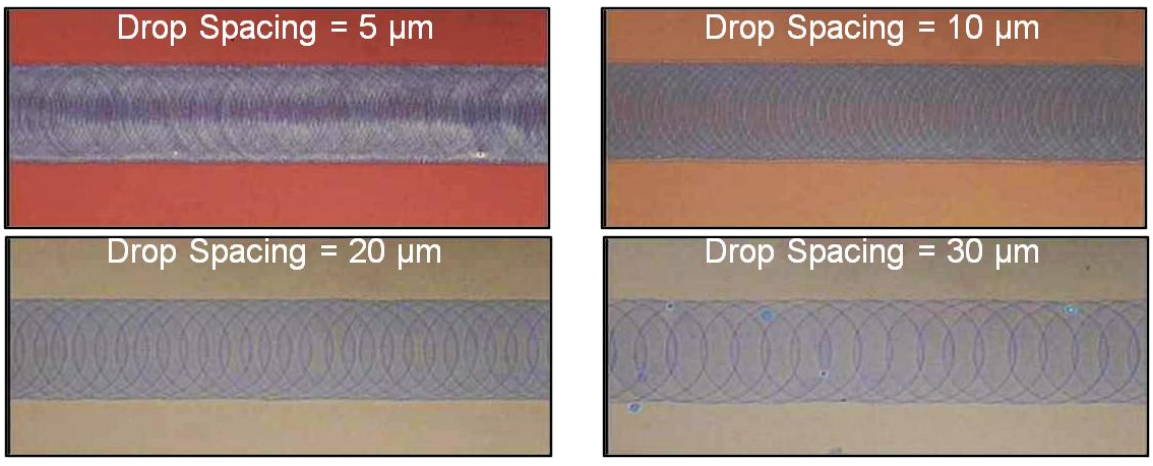

Figure 3.13. Optical micrographs of rGO lines printed at 90°C with drop spacings of 5 µm, 10 µm, 20 µm, and 30 µm.

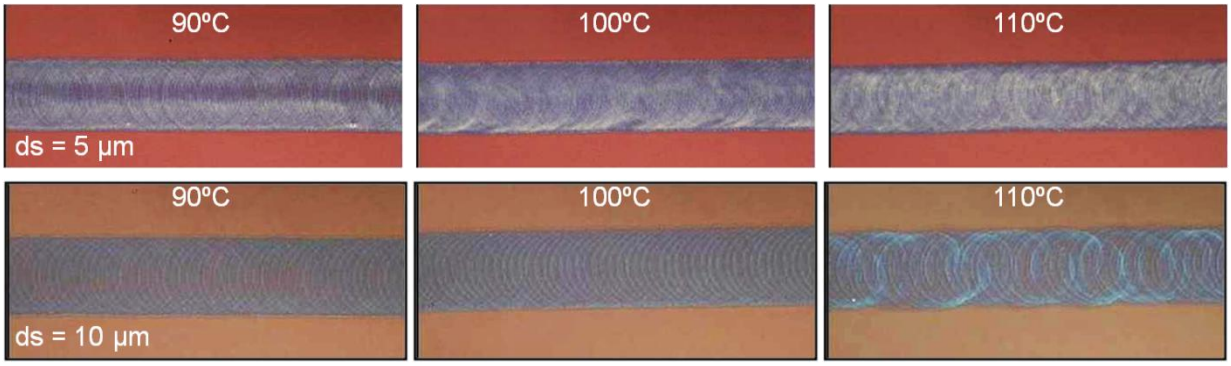

Figure 3.14. Optical micrographs of lines printed at 90°C, 100°C, and 110°C with drop spacings of 5 µm and 10 µm.

To investigate the effects on surface roughness atomic force microscopy (AFM) was used. Figure 3.15 shows AFM micrographs of lines printed at 90°C, 100°C, and 110°C. The extracted RMS roughness of the films was 3.1 nm, 3.6 nm, and 3.8 nm, respectively. The bright areas aligned into (semi)continuous lines represent agglomeration at the edges of individual drops. It can be seen that the edge lines are more continuous at higher temperatures. This is likely due to the following mechanism: as the drying proceeds, convective flows carry the solvent along with GO flakes to the edge. Towards the end of the drying process, most of the volume accumulates at the edge; however, due to the high surface tension of water, the edge line breaks into small beads and forms discrete agglomerates. At lower temperatures this surface tension related agglomeration has time to proceed, whereas at higher temperatures the solvent evaporates too fast for the beading process to happen. Hence, at 110°C the edge lines are more pronounced and continuous. Figure 3.16 shows AFM micrographs of lines printed at varying drop spacing at 90°C. It can be seen that the edge line agglomerations follow the periodicity of associated drop spacing parameter, thus verifying the reasoning of their occurrence.

The effects of substrate temperature and jetting frequency were also investigated on inks containing 5% of EG. As discussed earlier, EG can be used in conjunction with water to reduce the coffee ring problem. Figure 3.17 shows optical micrographs of water/EG ink lines printed at 100°C – 130°C. It can be seen that at lower temperatures the lines are discontinuous and heavy material agglomeration is present. In contrast, higher temperature prints are significantly more uniform. This is likely due to large boiling point difference between water and EG. At about 100°C water evaporates almost instantaneously while some EG remains. When the subsequent drop arrives, it mixes with the previous one forming a concentrated EG/flake slurry. At this temperature EG has enough time to reflow and cause agglomeration. At 130°C, on the other hand, EG evaporates fast enough that each drop dries before the next one arrives, hence preventing re-dissolution and agglomeration. This effect can be further investigated by decreasing jetting frequency and allowing more drying time between successive drops. Figure 3.18 demonstrates the effects of wait time on resulting line morphology printed at 100°C. It can be seen that introducing longer drying time for individual drops results in a much more uniform line.

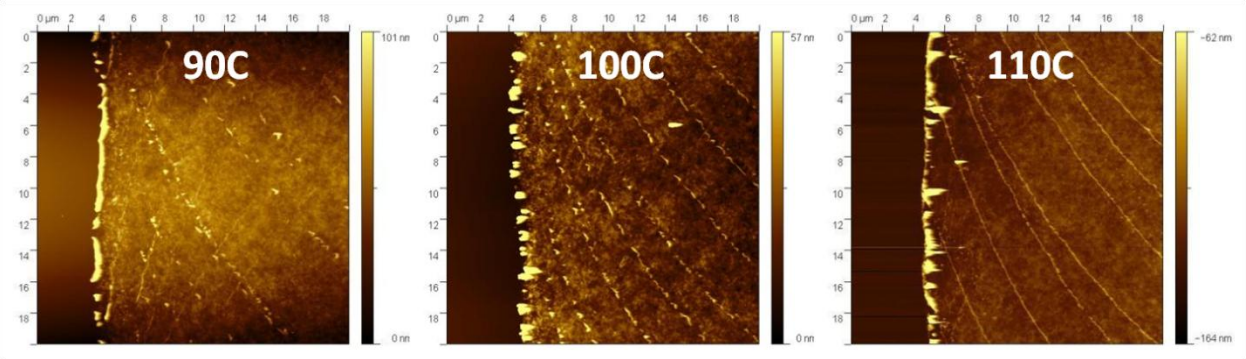

Figure 3.15. Temperature evolution. AFM micrographs of lines printed at 90°C, 100°C, and 110°C with drop spacing of 5 µm and wait time of 30 ms.

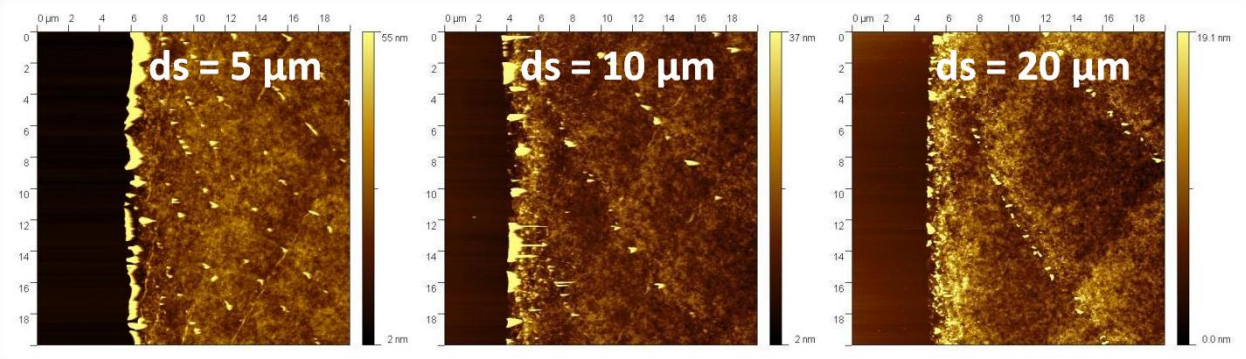

Figure 3.16. Drop spacing evolution. AFM micrographs of lines printed with ds of 5 µm, 10 µm, and 20 µm (temperature 90°C, wait time 30 ms).

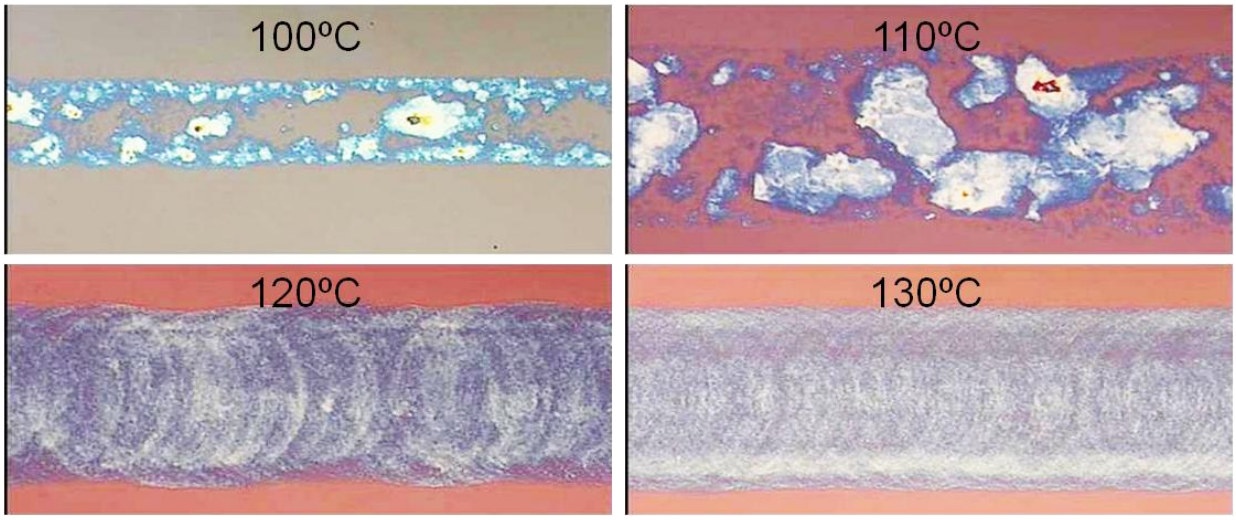

Figure 3.17. Temperature evolution of inks with EG. Optical micrographs of lines printed at 100°C – 130°C. (ds = 5 µm, wait = 0 ms)

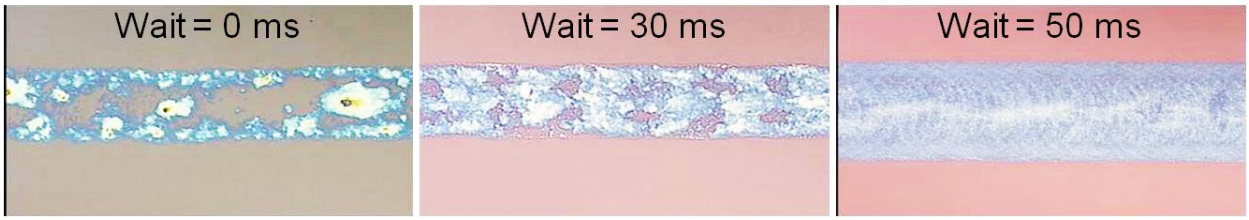

Figure 3.18. Wait time evolution. Optical micrographs of lines printed with w = 0 ms, 30 ms, and 50 ms. (ds = 5 µm, temperature = 100°C).

To examine surface roughness and material agglomeration two techniques were used: dark field optical imaging and AFM. Dark field imaging is sensitive to out of plane features which, in the scope of the present discussion, refer to large agglomerations on the surface of printed lines. In dark field view, these will show as bright spots which will allow quick estimation for the amount of large aggregates. Figure 3.19 shows dark field optical micrographs of lines printed with EG at varying substrate temperatures (ds = 5 µm, wait = 50 ms). Lower temperature prints have noticeable agglomeration at the edges, as evidenced by bright spots. Above 120°C bright spots largely disappear signifying a lack of large agglomerates. To verify edge smoothness, AFM measurements were performed on samples printed at 120°C and 130°C (Figure 3.20) When compared to AFM images from lines printed with pure water as, it can be seen that addition of EG suppresses agglomeration and results in significantly lower amount of aggregates at line edges.

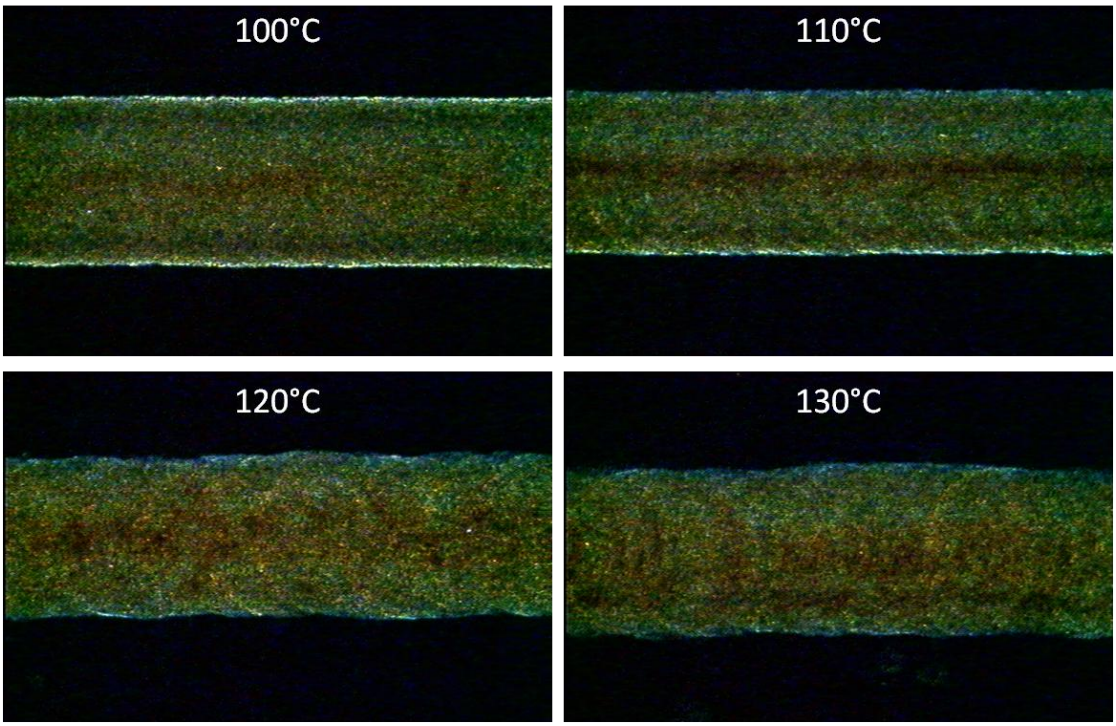

Figure 3.19. Dark field micrographs of lines printed at 100°C – 130°C.

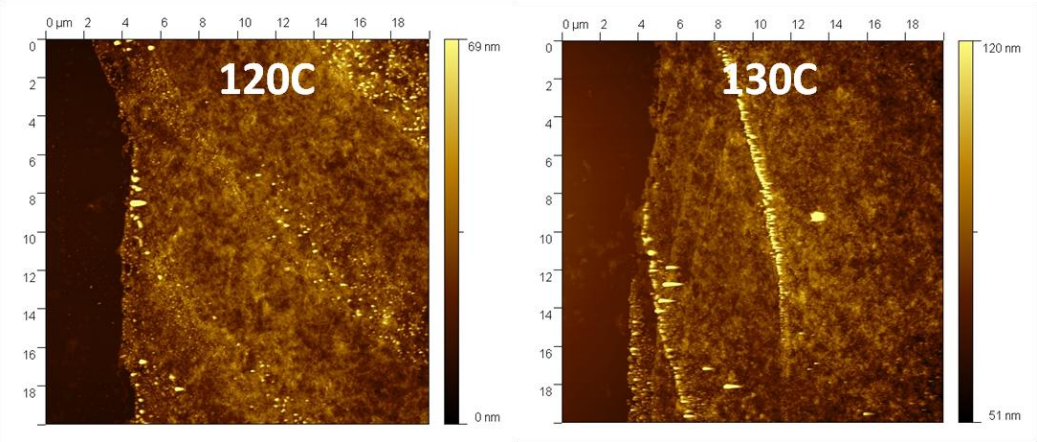

Figure 3.20. AFM micrographs of GO lines printed with EG at 120°C and 130°C.

3.5 Anneal Effects

Annealing effects were examined on lines printed with pure water inks. Two thermal treatment methods were used to reduce graphene oxide and produce rGO: N_2 and hydrazine. Data was taken on two sample sets with approximately 10 devices per data point. For better comparison, resistance values were normalized to the value at first measurement. Figure 3.21 shows normalized resistance as a function of temperature and time for N_2 (a,b) and hydrazine (c,d). Temperature measurements were performed for 60 minutes at each point, while time measurements were performed at 200°C and 90°C for N_2 and hydrazine, respectively. It can be seen that N_2 anneal proceeds continuously with temperature up to 350°C without saturation. This is expected, as maximum reduction of GO in inert gasses has been shown to happen only at much higher temperatures[55]. N_2 anneal at 200°C shows that resistance saturates after about 100 minutes, indicating a limit to reduction at this temperature. Hydrazine anneal appears more effective in the reduction process. After 20 minutes of anneal at 90°C (Figure 3.21(d)), the resistance is close to its final value. Examining the temperature effects, it can be seen that there is a large decrease going from 80°C to 90°C with a slow subsequent decrease. Generally, hydrazine anneals achieve resistivities of almost an order of magnitude lower than N_2. Resistivities achieved in this study were on the order of $5x10^{-4}$ Ω-m, which is higher than the best reported for rGO ($1x10^{-4}$ Ω-m), but are similar to those of solution processed ITO ($2x10^{-4}$ Ω-m).

To examine the effects of annealing on the chemical composition of the films, X-ray photoemission spectroscopy (XPS) was performed. This is a powerful technique that can provide elemental composition of a material along with the chemical state and binding characteristics of its individual components. XPS works by bombarding a sample with X-rays and measuring the energy of the emitted electrons. Given the energy of the incoming photons and other machine related factors, binding energy of the escaping electrons can be calculated. The binding energy of emitted electrons can be used to identify source elements. Furthermore, the exact binding energy of an electron in a given configuration may also depend on the chemical state of the element of interest. In particular, various carbon bonds (C-C, C=O, C-OH, etc.) have

unique binding energies of the 1s electrons, which can be revealed with a high resolution XPS analysis.

Figure 3.22 shows XPS spectra of carbon C1s binding energies for samples annealed in N_2 and hydrazine at various temperatures compared to as-deposited films. At room temperature both C-C and C-O are clearly present, represented by their relative intensity of the associated peaks. The C-O bonds does not diminish with N_2 heat treatment until 200°C, which correlates well to the fact that significant conductivity occurs in samples annealed at 200°C and above. In contrast, hydrazine exposure reduces the C-O peak significantly after 80°C, again demonstrating the effectiveness of hydrazine as a reducing agent for graphene oxide. Clearly, such low temperatures would be easily maintained within the bounds of plastic-compatibility.

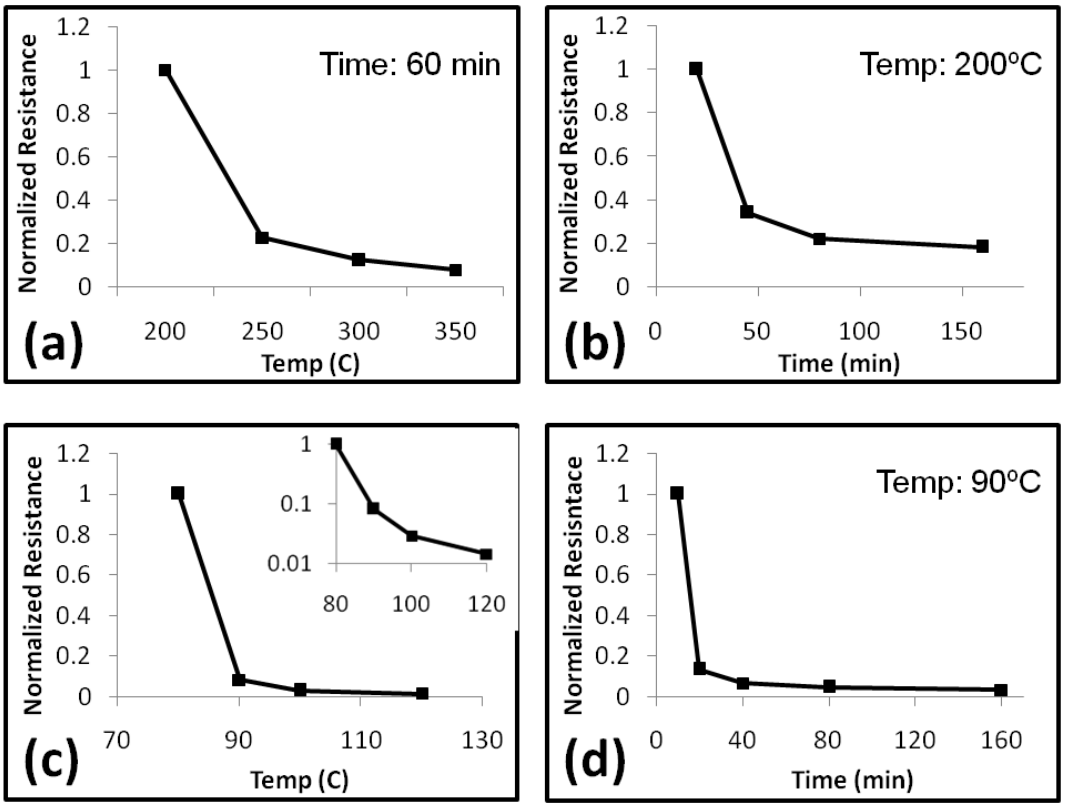

Figure 3.21. Normalized resistance as a function of N_2 anneal (a) temperature and (b) time, as well as hydrazine anneal (c) temperature and (d) time.

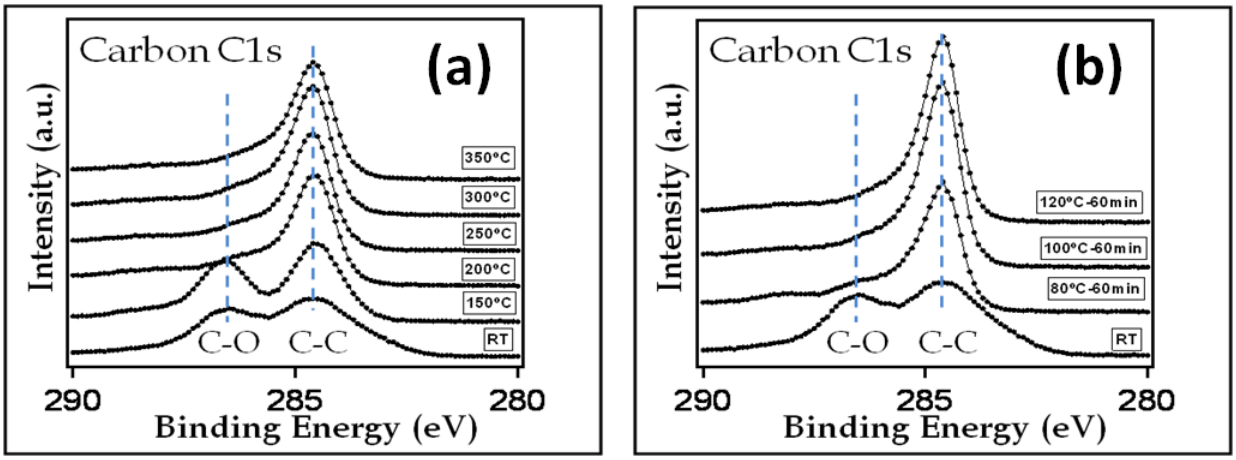

Figure 3.22. Carbon C1s XPS spectrum evolution at varying temperature for rGO lines annealed in (a) N_2 and (b) hydrazine.

3.6 Discussion

Resistivities achieved with printed rGO conductors in this work are higher than state-of-the-art ITO coatings currently used in large scale LCD applications. These require sheet resistances on the order of 20 Ω/□. Resistivity of printed lines presented here would result in sheet resistances on the order of 10^3 Ω/□ with film thickness of 100 nm. However, current ITO coatings are not compatible with flexible substrates. Thus, printed rGO should be compared against other technologies proposed as contacts for flexible and low-cost electronics, such as organic conductors, solution-processed TCOs, and other rGO based conductors. In that case, conductive films presented here match or approach the resistivities published, as discussed earlier.

Resistivity of rGO films could be improved by formulating inks to include larger GO flakes. Wang et. al. have modified the Hummers method to produce stable solutions with GO sheets of up to 25 µm[53]. Smaller sheets have a larger relative concentration of edge states and broken aromatic bonds, which decreases the number of delocalized carriers. Furthermore, films consisting of smaller flakes have a greater amount of sheet-to-sheet contacts, which act as effective grain boundaries. It is likely that electron conductivity in these systems is limited by transport between individual sheets. Therefore, formulating inks with larger GO flakes would improve overall conductivity. In the films presented here, GO flakes on the order of 0.5 µm – 1 µm were used. Assuming that conductivity is limited by sheet defects and inter-sheet boundaries, increasing the printed flake size to 25 µm should increase conductivity by a factor of 10 – 20. This, in turn, will decrease sheet resistance to the 10^2 Ω/□ range, which approaches viability for small display applications.

Additionally, even with the resistivities achieved here, printed rGO conductors can be utilized as interface layers for TFT S/D contacts. As discussed earlier, performance of a TFT with rGO active material can be improved greatly by incorporating rGO contacts. This works by improving the physical and electronic interface between the contact and the semiconductor. TFT printing flow presented in Figure 2.2 can be easily modified to incorporate metallic rGO

over the S/D contacts. No extra ink formulation is necessary, as the same solution used for the active layer can be used here. Assuming transistor width of 100 µm, rGO layer thickness of 10 nm, channel-contact interface thickness of 2 nm, and taking the achieved resistivity of $5x10^{-4}$ Ω-m, the effective series ohmic resistance of the interface layer can be calculated to be 25 Ω. This is negligible compared to channel and other parasitic resistances. However, incorporation of such interface layers has been shown to improve effective TFT mobility by a factor of 2 – 5. Thus, integration of rGO as a contact layer should improve electrical characteristics of TFTs presented in Chapter 2 by producing an all-graphene transistor.

3.7 Summary

Ink-jet printed conductive lines were demonstrated based on pure water and water/ethylene glycol inks. Lines were printed at elevated substrate temperatures to overcome issues of feature splitting and lack of contact line pinning. Addition of EG decreased the coffee ring effect and resulted in smoother line edges. These lines can be deposited and processed at plastic-compatible temperatures and, thus, have potential for printed and flexible electronics. Resistivities of $5x10^{-4}$ Ω-m were achieved. We believe with ink optimization, such as increasing flake size, lower values can be achieved. Although, it is already competitive with plastic-compatible solution processed ITO and PEDOT:PSS for transparent applications.

4 Zinc Oxide RRAM

The ability to store information is critical to any "smart" electronic application including those where solution-processed, low-cost electronics are most likely to become relevant. Applications such as RFID tags, displays and smart cards all require some capability for non-volatile memory (NVM) in order to perform their intended functions. In fact, constant scaling of both size and cost of memory is a key contributor to the relentless growth of mobile electronics. Although, a number of NVM technologies are available, flash memory has by far become the largest contributor to the field of personal entertainment and mobile communications.

While there is a push for a replacement for flash technology in conventional electronics, the field of printed electronics, on the other hand, has been struggling to identify a clear frontrunner for any stable and implementable memory technology. A printed NVM would have to conform to the same processing requirement as all the other components, namely solution-processability and plastic temperature compatibility. This implies that proper inks have to be available for all the individual components and processing temperatures have to be kept under 200°C. In this chapter, various memory implementations will be discussed and resistive random access memory (RRAM) based on metallic filament formation will be presented as a candidate for an all-printed storage medium.

4.1 Flash Memory Background

As mentioned earlier, flash currently dominates the non-volatile memory market. It is based on a floating gate transistor design as demonstrated in Figure 4.1. General fabrication principles of these devices are very similar to those of standard CMOS processing. Flash FETs are fabricated on single-crystal silicon substrates and are usually NMOS in order to utilize high mobility of electrons as compared to holes. This results in lower effective channel resistances, higher currents, and faster switching speeds. A flash transistor is schematically similar to a regular MOSFET with one major difference: the secondary "floating" gate. The floating gate is isolated from the signal gate (or word line) by an inter-poly dielectric (IPD) and from the channel of the device by a tunnel dielectric/oxide (TOX). Data is stored via the accumulation of electrons in the floating gate layer. Stored electrons act as an effective threshold voltage (V_T) regulator. These electrons are introduced into the channel by turning the transistor "ON" and are injected into the floating gate via Fowler-Nordheim (FN) tunneling or hot carrier injection. Once stored, the negative charge induces a positive V_T shift. The state of the device can then be determined by biasing the gate just above the nominal V_T and examining the current output. An erase event can be achieved by biasing the control gate in the opposite direction and forcing the stored electrons to tunnel back into the bulk.

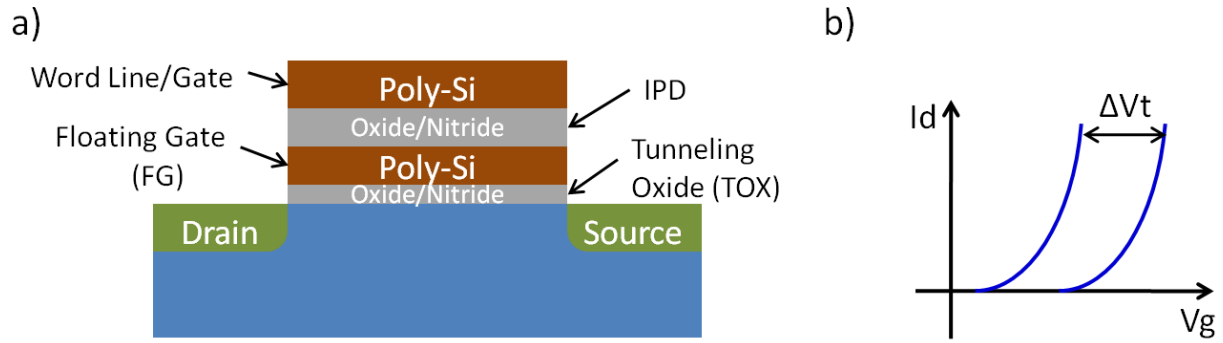

Figure 4.1. a) Cross section schematic of a Floating Gate Flash transistor. b) I_D-V_G of a Flash transistor demonstrating a V_T shift due to stored charge.

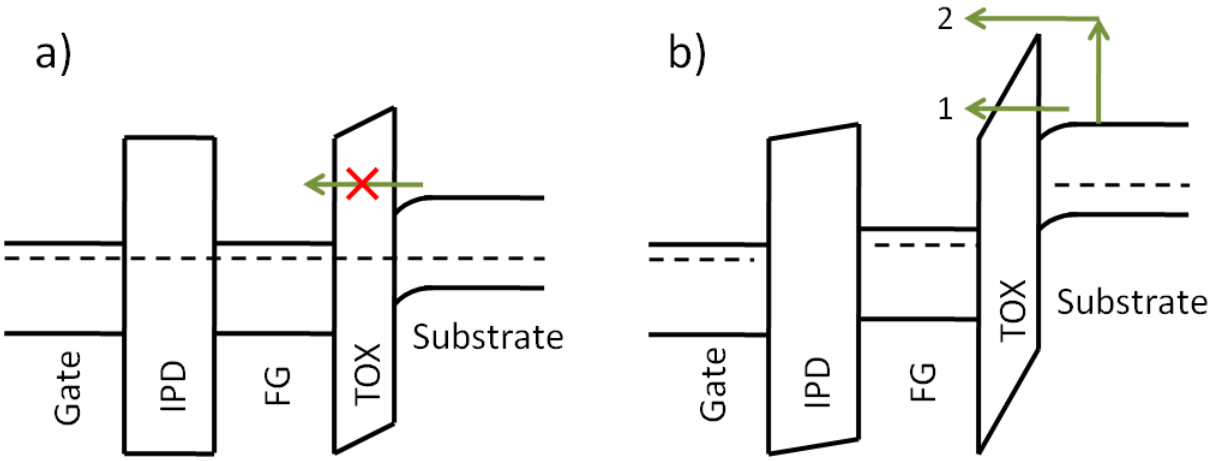

Figure 4.2. Band diagrams through the gate stack of a Flash transistor at a) equilibrium and b) positive control gate bias. Two tunneling processes are demonstrated: 1) Fowler-Nordheim tunneling, 2) hot carrier injection.

Figure 4.2 shows representative band diagrams of a device in equilibrium and under programming bias. Under equilibrium conditions or small positive control gate bias, electrons in the channel do not have enough energy to tunnel through or hop over the TOX barrier. However, when sufficient positive bias is applied to the control gate, electrons can transport via FN tunneling. Alternatively, under sufficient V_{DS} bias, a carrier may gain enough energy to hop over the TOX; this is often referred to as hot carrier injection (HCI). FN tunneling and HCI are denoted in Figure 4.2(b) as mechanisms 1 and 2, respectively.

Two major design architectures of flash memory exist: NAND and NOR. These are named because of the circuit similarity to the respective logic gate designs. Figure 4.3 demonstrates schematic circuit representations of the two architectures. NAND is implemented as a pull-down string of transistors. All the transistors in a string are connected sequentially drain-to-source via the diffusion region and no independent S/D connection is necessary. This results in a fairly compact $4F^2$ architecture, where F is the minimum feature size for a given technology[99,100]. This results in relatively high density; however, individual device isolation is

impossible and accessing data requires routing signal through the whole bit string. This, in turn, results in slower random access speeds and lower data integrity.

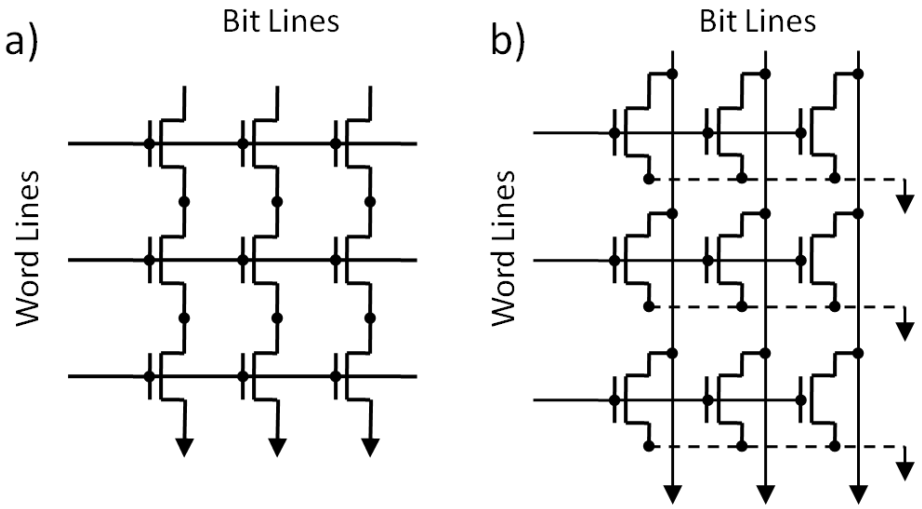

Figure 4.3. A circuit schematic for two types of Flash implementation: a) NAND and b) NOR.

To program a cell in a NAND array a "high" voltage is applied to the primary word line (WL), while the other WLs are turned "ON" to some minimal required programming voltage. Applying proper voltage to the desired bit line (BL) activates the transistor string. Current flows through all the transistors; however, only the WL of interest is biased high enough to induce FN tunneling and program the device. To read the device, BL bias is applied, a nominal "ON" voltage is again applied to all the WLs, and the voltage on the WL of interest is swept to determine the point where the whole string turns on. Comparing that voltage to the nominal V_T allows determination of the cell state. FN programming requires fairly low energy (as compared to HCI), which, combined with high density, makes NAND very attractive for low-cost, low-power applications.

NOR architecture is also implemented as a pull-down circuit; however, just like its logic equivalent, each device has a dedicated BL and ground (GND). This allows direct access to each cell for reliable read and write operations. The dedicated GND contact requires an additional $4F^2$ area, thus bringing total cell area to $8F^2$. NOR flash is programmed by direct application of voltage to the desired WL and BL. High current and electric field at the source edge allows HCI to proceed. HCI requires significantly more current than FN tunneling programming and results in increased power consumption. Higher power, coupled with a larger area requirement, makes NOR flash less desirable for mass market consumer memory products; however, it's faster speed and greater reliability still necessitate its use in certain applications.

Several parameters of a flash device are important to realize if an attempt to transfer the technology into solution-processed electronics is to be made. Perhaps the most important is the tunnel oxide. TOX has to be thin enough to allow efficient tunneling to the FG. If it is too thick, band bending will be insufficient to allow FN tunneling, while the injected hot-carriers may get trapped in the dielectric itself instead of the FG. On the other hand, if it is made too

thin, excessive leakage from the storage area to the substrate will degrade retention and reliability, perhaps to the level of inoperability. Additionally, the thickness of the IPD is limited in relation to TOX through the gate coupling ratio (GCR), which is the ratio of IPD capacitance to total gate capacitance. This ratio has to be kept high to ensure that a sufficient portion of the total gate voltage is dropped across TOX. GCR has to be over 0.6 for modern devices[99]. To keep this ratio high C_{IPD} has to be kept high, which implies a thin dielectric. However, just like TOX, it cannot be too thin to prevent tunneling across the IPD. In addition to the being properly scaled, the dielectrics and their interfaces have to be of sufficient quality to minimize interface and bulk traps, as those would assist in retention loss.

4.2 Solution Processed Memory Background

4.2.1 Organic Flash

Given the demands described, one can quickly recognize the issues that would arise in attempting a solution-processed flash device, particularly related to dielectric stability and reliability. Nonetheless, flash-type NVM has been demonstrated based on organic TFTs. These are usually based on either a full FG[101,102] or a nanoparticle FG[103,104] where individual particles serve as charge trap centers. Figure 4.4(a) shows a schematic cross-section of a device with gold nanoparticles embedded in an organic polymer to serve as a floating gate. In this case the tunneling and the inter-gate dielectrics were on the order of 5 nm – 10 nm. Although flash-like behavior was achieved in this work, and others similar to it, it is hard to distinguish the true effects of the FG from those of trapping due to the defects in the dielectric itself. Additionally, retention time of these devices is on the order of 100s of seconds (Figure 4.4(b)). This is likely due to the poor insulating property of the dielectric as well as low charge trap lifetime.

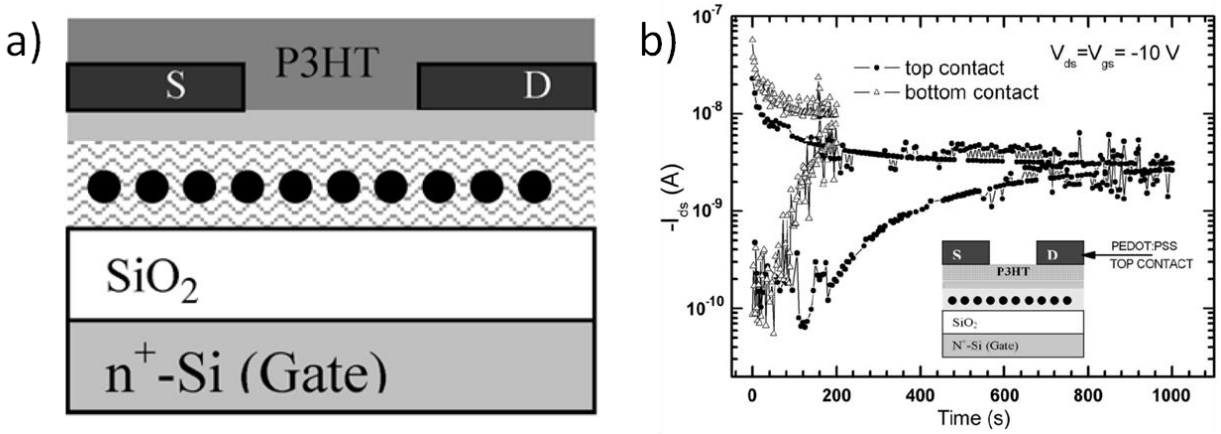

Figure 4.4. a) Cross section schematic of an organic Flash-like transistor based on gold nanocrystals embedded in the gate dielectric. b) Data retention characteristics[103].

In an attempt to improve memory characteristics, Sekitani et. al. have demonstrated organic flash devices with dielectrics of aluminum oxide (AlO_X) and a self assembled monolayer (SAM)[101]. Figure 4.5(a) shows a schematic representation of the device. Both the control and the floating gates are made of thermally evaporated Al. To form the dielectric, the Al gate is first exposed to oxygen plasma to form an oxide of approximately 4 nm; subsequently an

organic SAM of about 2 nm is deposited in solution. This is done for both IPD and TOX equivalents. Active material (pentacene) and Au contacts are deposited on top of the gate stack. The researches claim that the improvement in interface and trap qualities of the AlO_X/SAM dielectric would result in improved memory performance. Figure 4.5(b and c) show the I-V response of the devices before and after programming as well as time evolution of the storage states. It can be seen that I-V characteristics are representative of a strong V_T shift. However, data retention seems to degrade after about 1000 seconds and collapses completely after 10^4 seconds. This is most likely due to the leakage through the dielectric or recombination at the interface, as the Al FG should be able to hold charge significantly longer than that.

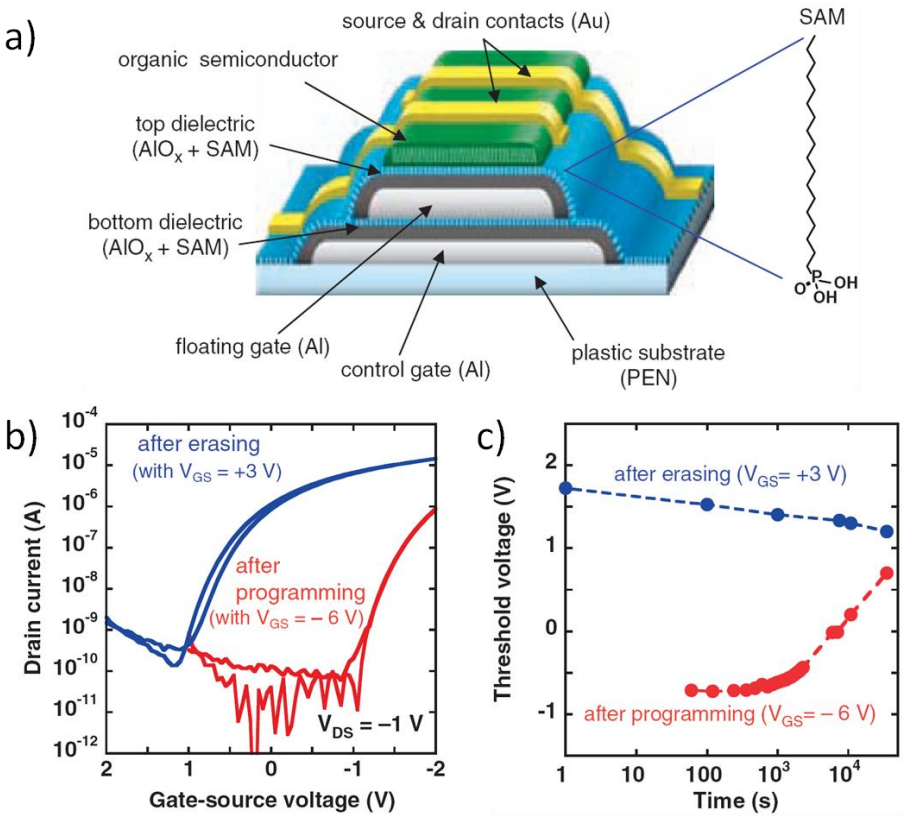

Figure 4.5. a) Cross section schematic of the floating gate transistor based on AlO_X and SAM dielectric. b) I_D-V_G characteristics demonstrating a V_T shift after programming. c) Data retention characteristics.

Although interesting from an academic perspective, the flash-like devices based on organic materials described here are hardly promising in terms of full integration. Furthermore, none have been shows to be fully printable and achieving any reasonable performance always requires some level of traditional processing. Achieving the tight geometrical and electrical characteristics required for successful flash-like implementation may never be feasible through solution-processing.

4.2.2 Ferroelectric Memory

Perhaps the closest technology to being implemented into a fully solution-processed flow is ferroelectric based memory (FeRAM)[105-107]. In these devices a ferroelectric material is used as the gate dielectric. Such materials can be reversibly electrically polarized by an external field. This results in remnant polarization perceived externally as charge on the surface of the dielectric (units of C/m^2), which, in turn, acts as an effective V_T control for the transistor. Thus applying a sufficient gate bias can polarize the dielectric in either positive or negative direction, thereby inducing an appropriate shift in device characteristics. Most of the literature focuses on poly(vinylidene fluoride/trifluoroethylene) (P(VDF-TrFE)) as the ferroelectric dielectric of choice. It can be solution-deposited and annealed at a plastic compatible temperature of 140°C. Figure 4.6 shows a solution-processed FeRAM device based on P(VDF-TrFE) as the storage element along with the associated electrical characteristics. Device architecture is that of a standard bottom-gate, top-contact design with a dielectric thickness of 300 nm. It can be seen that device can be programmed by polarizing the dielectric at approximately ±60 V. I-V curves show a strong response of V_T.

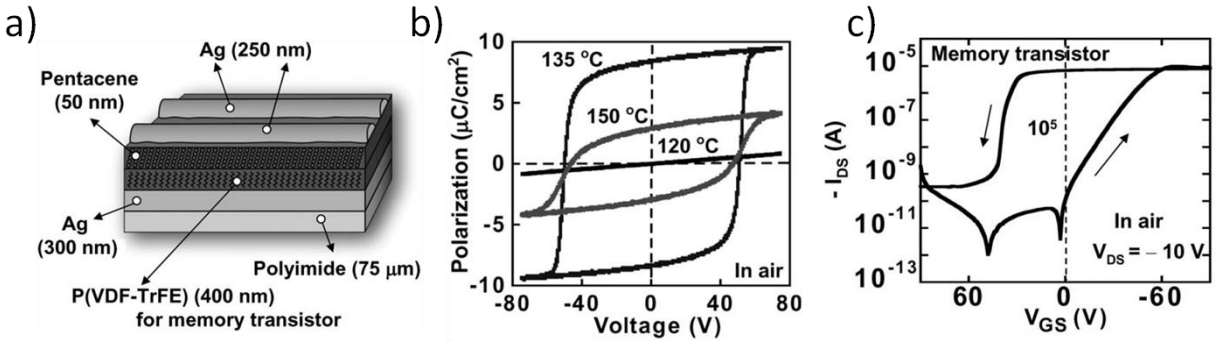

Figure 4.6. a) Schematic of a FeRAM transistor, b) polarization curves of P(VDF-TrFE) annealed at different temperatures, c) I_D-V_G characteristics demonstrating a V_T shift after programming[105].

FeRAM is a very interesting technology for low-cost electronics and it has been demonstrated through a fully solution-processed, plastic compatible fabrication process. However, there are a number of issues that still need to be addressed. As described earlier fairly large program/erase voltages are necessary to induce proper polarization in a ferroelectric film at the thicknesses demonstrated in the literature. These voltages can be scaled lower with decreasing the gate dielectric thickness; however, that will result in smaller remnant polarization charge and, consequently, a smaller V_T shift and programming margin. To date, only devices with fairly thick dielectric (over 100 nm) have been shown via solution-processing. Another negative consequence of a thick film is increased programming time, as it takes longer to align the dipoles within a domain. Usually programming times on the order of milliseconds are necessary. Additionally, organic FeRAM devices generally suffer from high temperature instability due to the fairly low Curie temperature of the ferroelectric materials used. Curie temperature is the point at which the polarized domains relax, hence losing stored data (140°C – 180°C for PVDF based polymers). This type of relaxation is also responsible for

relatively low retention times at elevated temperatures. In fact, Naber et. al.[108]have been the only authors to demonstrate retention even at room temperature on the order of several days.

Clearly, a more stable and reliable memory technology is desired for printed electronics. Currently, a significant percentage of the publications on organic or printable memory utilize an inherent hysteresis of the system as a storage mechanism. The line between random trapping in the various organic layers and true memory effect (be it flash or ferroelectric) is sometimes blurred.

4.3 Resistive Memory Background

Resistive random access memory (RRAM) has been one of the frontrunners in an effort to locate a suitable successor for flash. However, RRAM could also be promising for printed electronics as well, mostly due to its architectural simplicity, low operating voltages, low switching power, and, critically, its potential compatibility with solution-processable materials. The low operational voltage and power make it particularly attractive to mobile, low power applications such as printed RFID tags, while its scalability is also important for conventional CMOS integration. RRAMs a generally implemented as a two terminal device that changes resistance, and thus storage state, based on applied bias. A schematic of a typical RRAM device is shown in Figure 4.7. It consists of a solid electrolyte stacked between two electrodes, either both inert or one inert and one reactive. This, next to a conductive line, is likely the simplest type of device structure one can find in an electronic circuit. Along with its simplicity, the general scaling restrictions of RRAM are also relaxed compared to TFT based memories, in particular as related to tunneling oxide dimensions. As will be discussed later, the electrolyte layers can be made thick to ensure good yield and yet, with proper programming, result in low voltage operation and fast switching.

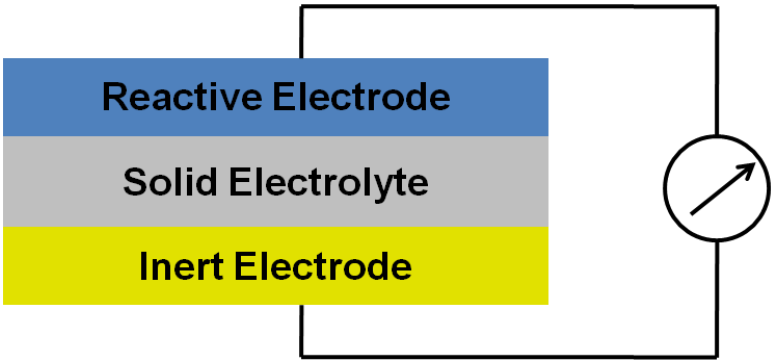

Figure 4.7. Cross section of a basic Resistive Random Access Memory cell.

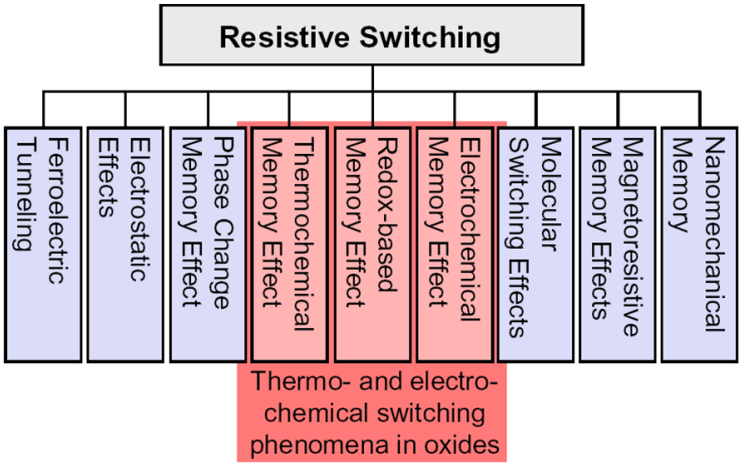

Figure 4.8. Classification of resistive switching effects.

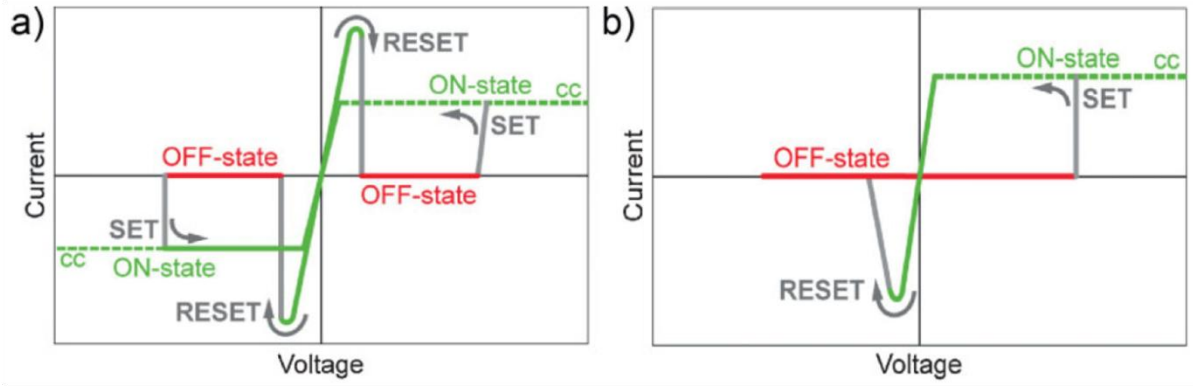

Figure 4.9. Basic operation schemes for RRAM: a) unipolar and b) bipolar.

A number of different types of RRAM exist based on different switching mechanisms. These can be generally classified into nine categories, as demonstrated in Figure 4.8[109]. This section will discuss the subset where switching is based on filamentary formation via the following mechanisms: electrochemical metallization (ECM), valence change mechanism (VCM), and thermo-chemical mechanism (TCM)[110]. These may exhibit either unipolar or bipolar switching as demonstrated in Figure 4.9. Generally, the SET or program event is associated with a switch from high-to-low resistive state, where as a RESET or erase event with a low-to-high resistive state. Unipolar devices show I-V response symmetric around V = 0 V and can be programmed and erased at the same bias polarity. Bipolar devices show asymmetric characteristics, where program and erase events happen at opposite polarities.

4.3.1 Electrochemical Mechanism Switching

RRAM based on Electrochemical Mechanism (ECM) utilizes controlled formation and dissolution of metallic filaments. This is the type of memory that will be discussed in this chapter. A representative schematic of a cell is demonstrated in Figure 4.10. A cell consists of three layers: a reactive electrode, a solid electrolyte, and an inert electrode. The reactive electrode serves as the ion source for forming filaments. The electrolyte is an ionic conductor;

ideally a material which will allow diffusion of the reactive electrode ions while limiting electronic conductivity. The inert electrode is a high work-function material like gold, platinum, or tungsten. (Tungsten has been particularly popular due to its CMOS compatibility.)

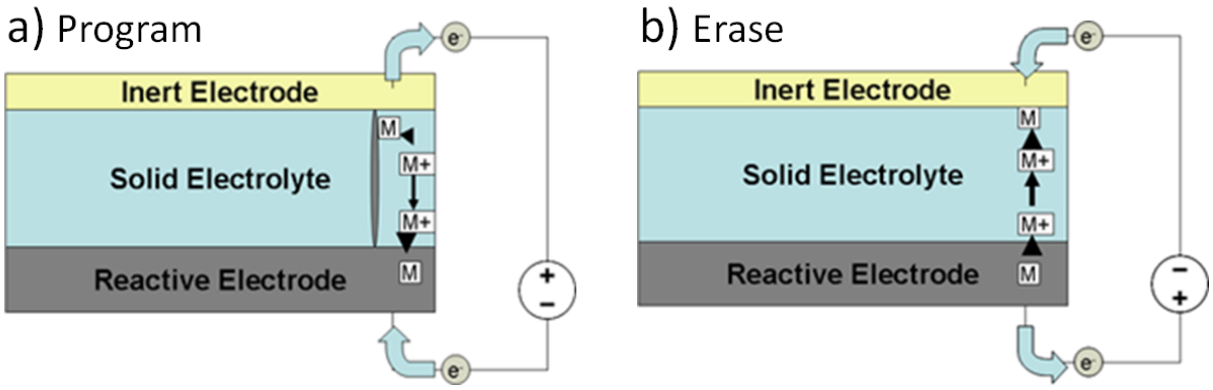

Figure 4.10. Schematic representation of ECM cell operation: a) program, b) erase.

Filament formation proceeds in three steps. First, upon application of a positive bias to the reactive electrode, metal ions at the surface of the reactive electrode oxidize forming positively charged cations. Second, the formed cations migrate under the applied electric field through the electrolyte to the inert electrode. Finally, cations arriving at the inert electrode will reduce to elemental metal and crystallize on the cathode surface. At the onset of this process, the reduction and crystallization sites are random; however, after initial island formation, electric field will be localized to thinner areas of the electrolyte and promote local filament growth. As this growth proceeds, the filament will reach the inert electrode and form a conductive path, thus converting the cell from a high to low resistive state and accomplishing the SET event. The RESET event works in the opposite manner. Application of negative bias to the reactive electrode forces the oxidation and dissolution of the atoms in the filament. The metal ions are driven back to the reactive electrode and, once the filament is no longer continuous, cell resistance transitions from low to high. It is not required for the filament to dissolve completely in order to RESET successfully; the filament only needs to be "broken" to induce a high resistive state. Upon breaking of the filament, the erase process stops and most of the filament remains. Consequently, after the first cycle, programming steps need to only bridge the gap in the filament. Hence, both programming time and required bias decreases with increased cycling until a certain stable value. The initial programming step is often referred to as a forming step. This type of behavior is representative of all the switching mechanisms described in this section.

Pan has created a kinetic Monte Carlo (KMC) model to simulate the formation and dissolution of filaments[111]. The KCM method considers individual particles in the system and the energies associated with various transition processes. A schematic of a representative system is demonstrated in Figure 4.11(a). Several possible processes for atomic transitions are presented and numbered as follows: (1) oxidation at adatom site, (2) oxidation at step site, (3) oxidation at hole site, (4) reduction at adatom site, (5) reduction at step site, (6) reduction at hole site, (7) adsorption, (8) desorption, (9) bulk diffusion, (10) surface diffusion. The only

process considered in the bulk of the electrolyte is ionic diffusion. The electrolyte is assumed to be a pure ionic conductor. The rest of the processes occur at the electrodes. An atom may start at one of three anode sites: hole, step, or adatom. Then it is allowed to either oxidize or maintain current state. Once oxidized, an atom is allowed to diffuse across the surface or desorb from the surface. A desorbed ion may either re-adsorb onto the surface or diffuse through the bulk of the electrolyte. Without external bias, bulk diffusion is isotropic. If an atom successfully reaches the cathode, it can adsorb and reduce by following the steps described for the anode in reverse. Each of the described transitions has an associated activation energy and rate. The relative energies govern the extent of individual transition probabilities. Application of external bias modifies these transition rates. As a consequence, anisotropic bulk diffusion is induced and oxidation versus reduction is favored at the opposite electrodes.

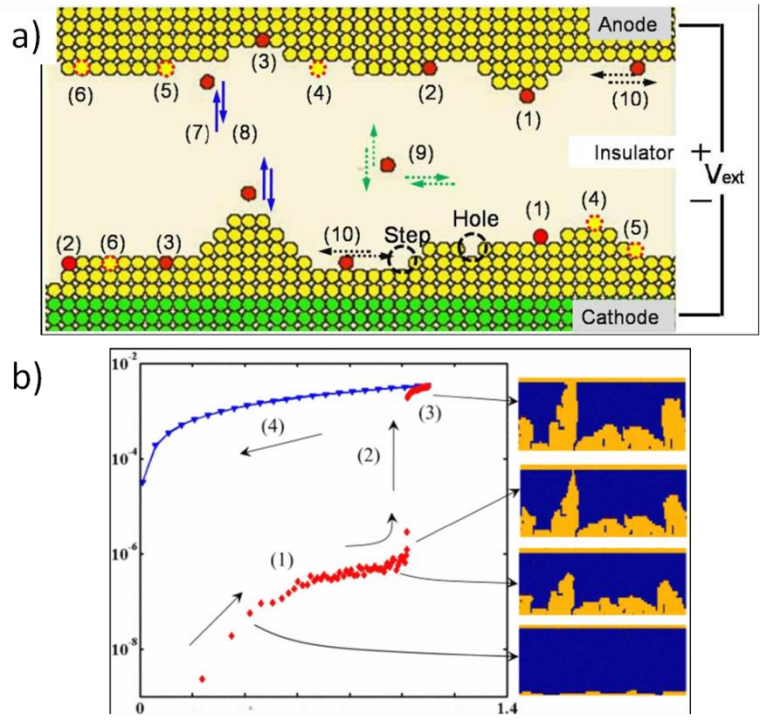

Figure 4.11. a) Processes involved in ECM switching as used in the KCM model. b) Simulation results showing the I-V response and cell cross section for filament formation.

Using this framework, filament formation and cell switching can be modeled. Figure 4.11(b) demonstrates I-V characteristics of a simulated programming event along with a cross section of the resulting filament. It is interesting to note that towards the end of the filament formation process, a thin portion forms quickly to complete the circuit. The conductivity of the filament is still high enough to induce a sufficient voltage drop across the top part. This results in overgrowth of the filament and decrease of cell resistance (denoted as process (3)), which is often referred to as filament "ripening".

Material selection is very important in ECM based cell design. Perhaps the easiest part is the inert electrode. As mentioned earlier, a metal with a high work-function that will not be easily oxidized is desired. In the scope of printed electronics, gold is the primary candidate for

this role. A variety of stable, well behaved, and easily handled gold inks exist and have been used in the field for long time. The reactive electrode has to have the opposite properties; it has to be oxidizable and be a fast diffuser in ionic form. Generally, silver and copper are used for this role in conventional manufacturing. For the purposes of printed-electronics, silver could be used as it is also easily available in well-behaved ink form. The electrolyte, as mentioned before, has to allow diffusion reactive material ions; however, the diffusivity and the solubility of said ions cannot be too large as that would make the formed filaments less stable and negatively affect data retention. In this work, ZnO is used as the electrolyte. Along with other transition metal oxides, it has been researched for use in conventionally fabricated RRAM. Its solution processability makes ZnO attractive for a printed RRAM implementation.

4.3.2 Valence Change Mechanism Switching

The switching mechanism in valence change devices is schematically similar to that of ECM, except here charged vacancies migrate through the electrolyte instead of ions. Transition metal oxides are often used as electrolytes for such systems (e.g. TiO_2, ZnO, NiO, Ta_2O_5, etc), where oxygen vacancies are the migrating species of interest. It should be noted that some of these oxides can operate under different switching mechanism depending on contacts used which could result in either bipolar or unipolar characteristics. ECM proceeds as follows: upon biasing the electrodes (one as anode and one as cathode), an electric field forms across the electrolyte. Oxygen vacancies (positively charged) in the electrolyte are pushed by the electric field towards the cathode where they accumulate. Excess of vacancies increases local conductivity thereby increasing local electric field, similar to metal ion formation. As vacancy migration/diffusion proceeds, the vacancy-rich, high conductivity region grows towards the anode. Once the anode is reached, the cell becomes conductive and the SET operation is achieved. RESET, similarly to ECM, is achieved by reversing polarity, where the reversed electric field causes the dissolution and back-diffusion of oxygen vacancies.

Generally, ECM based RRAM exhibit bipolar switching characteristics representative of filament formation and dissolution under opposing bias conditions. Such filaments have been verified in by AFM and TEM studies in TiO_2 based cells[112]. Filamentary conduction can also be deduced from area dependency of state resistance. Namely, in the OFF state, resistance is strongly dependent on cell area, which is expected of a metal/insulator/metal (MIM) structure. However, in the ON state, resistance is almost independent of cell area, suggesting localized conduction, as would be the case given a single filament per cell.

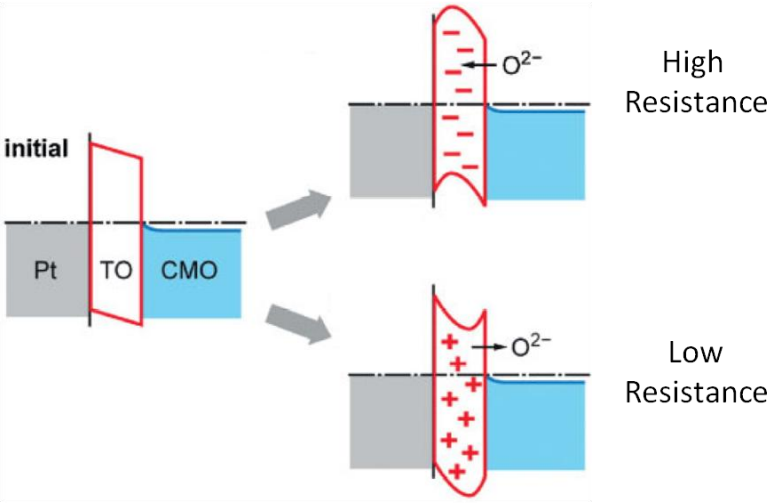

Figure 4.12. Potential barrier for a high resistance and low resistance cell. [113]

In addition to filamentary switching, ECM can also exhibit areal switching. In this case, instead of forming a filament all the way across the electrolyte, oxygen vacancies accumulate at the interface and modulate the injection barrier from the contact into the electrolyte[110]. Such devices may require a dual-layer electrolyte structure: a thin tunnel oxide (TO) and a thicker conducting metal oxide (CMO). The CMO is a mixed (ionic and electronic) conductor which is capable of providing oxygen vacancies. The TO is an interfacial layer capable of absorbing an excess of said vacancies. Figure 4.12 shows a schematic representation of a high and low resistance states[113]. To induce a high resistance state, oxygen vacancies from CMO are driven into the TO area thereby increasing the injection barrier from the contact. Conversely, a low resistance state is achieve by driving the oxygen vacancies out of the TO area and lowering the injection barrier. This type of system exhibits cell area dependence for both ON and OFF state resistance, suggesting areal, as opposed to filamentary, switching behavior.

4.3.3 Thermo-Chemical Mechanism Switching

Thermo-chemical mechanism (TCM) switching uses partial dielectric breakdown and joule heating in the electrolyte to accomplish state storage. This is in contrast to ECM and VCM which utilize ionic transport trough the electrolyte. In TCM several phenomena can account for conductance change. Biasing the electrodes induces a high electric field and some current flow through the dielectric. This can cause the oxide to decompose by either vacancy migration or joule heating. Current most likely begins to flow through grain boundary defects. With significant current increase, joule heating causes thermal expansion of current percolation region. This proceeds until sufficient melting of the electrode or decomposition of the oxide creates a conducting path. The initial programming step, forming, usually requires higher bias and longer time. During programming, current compliance is generally set to a low value to ensure that joule heating does not immediately destroy the filament. To erase a cell, a smaller voltage is applied without limiting current compliance. Since the cell is highly conductive, higher current flows at lower voltages which, without current limiting, results in excessive joule heating and burns or dissolves the conducting path.

Figure 4.13 demonstrates representative I-V switching characteristics for a representative TCM cell consisting of a Pt/NiO/Pt cells[114]. TCM cells are generally unipolar due to the symmetry of the cell and the nature of the switching mechanism. Following the initial forming step, subsequent programming steps require significantly lower voltage. This is likely due to existence of a partially formed conductive path which remains from the initial forming.

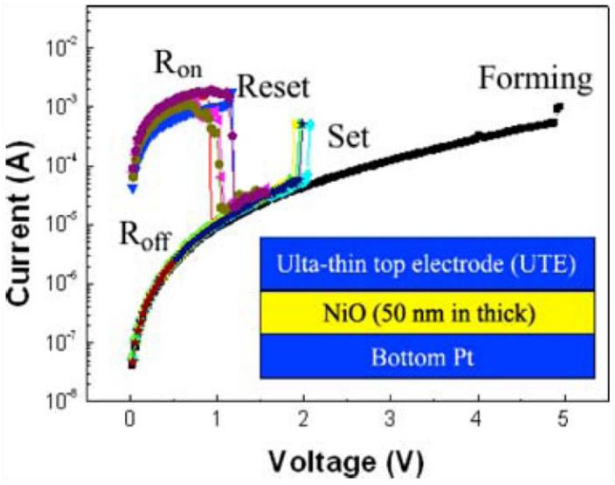

Figure 4.13. Unipolar switching characteristics of a TCM cell (Pt/NiO/Pt)[114].

This chapter will focus on RRAM based on an Ag/ZnO/Au cell. It exhibits bipolar, filamentary switching via diffusion of Ag^+ ions through ZnO electrolyte. Although multiple phenomena could be present within the ZnO layer, ECM is believed to be the primary switching mechanism, for which evidence will be presented.

4.3.4 RRAM Circuit Architectures

As discussed earlier, the simplicity of a two-terminal MIM structure is beneficial from manufacturing perspective. Additionally, read, write, and erase events are fairly straight forward. Sensing can happen by simply applying a small sense voltage (Vsense) to the appropriate bit line (BL) and word line (WL) and measuring resulting current. The sensing window in an RRAM cell is defined by the ratio of the resistance in the ON state to that of the OFF state (R_{ON}/R_{OFF}). This ratio will set the limit on a maximum array size that a particular RRAM technology type can accommodate. If the ratio is low, testing a cell may result in a false positive if the leakage paths across adjacent cells are significant. Furthermore, even with an extreme R_{ON}/R_{OFF} ratio, a simple cross bar array is not sufficient for a simple MIM-type memory cell due to secondary conduction paths. Consider an array presented in Figure 4.14(a). Assume a cell at location BL2-WL1 is to be tested, while cells colored in red are programmed (low resistance). If a sense signal is applied to BL2 and WL1, a parasitic current as shown by the dotted arrows will flow and result in a false reading of low resistance. Thus, a simple cross bar array without appropriate use of steering elements to control current flow is not suitable for direct RRAM integration.

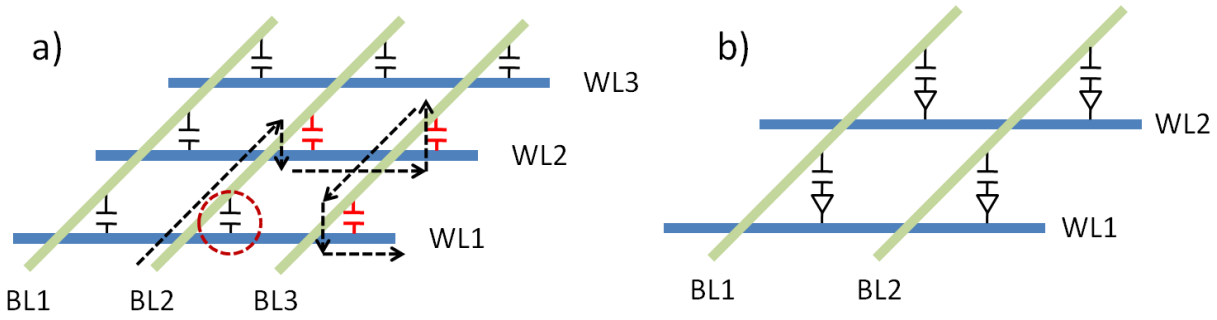

Figure 4.14. a) An array of RRAM cells illustrating a false read leakage path. b) An array with diode steering elements.

Steering elements are often implemented in cross bar arrays to eliminate parasitic conduction paths. One of the most direct ways of accomplishing this effect is by incorporating a diode in series with the MIM structure. Figure 4.14(b) demonstrates such a structure. If the cell in position 1-1 was to be tested, a leakage path across adjacent cells would be prevented by reverse biased diodes. This type of structure has been used successfully in memory structures like antifuse arrays[12]. However, use of a diode as a steering element is only useful for unipolar devices where both the SET and RESET events are performed under the same bias polarity. A more complicated steering element is necessary for RRAM devices with bipolar switching characteristics.

To accommodate bipolar switching devices, solutions involving a Zener diode or a TFT as a steering device could be implemented. Transistors are regularly used as select devices in cross bar array applications (e.g. DRAM). Figure 4.15 shows a schematic representation of such a system. A transistor is activated by biasing the proper BL and WL thereby passing current to the RRAM cell. In this manner, both positive and negative bias can be applied to the cell. Incorporating a transistor in series with a MIM structure has two major drawbacks: processing complexity and increased area. A diode steering element could be, and generally is, stacked on top of the memory cell itself. This could be as simple as incorporating one extra layer into the

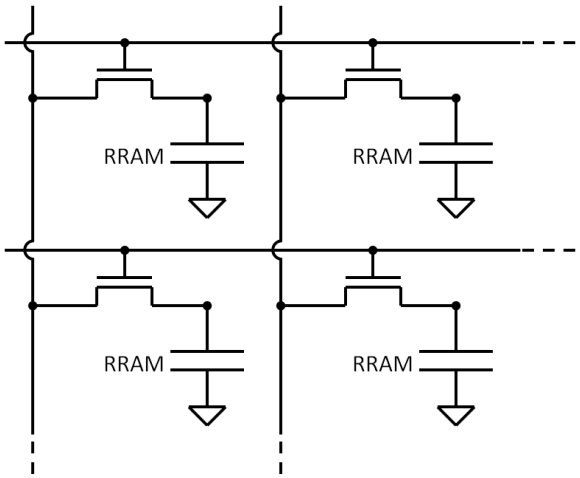

Figure 4.15. An RRAM array with transistor steering elements.

cell to form a rectifying contact. This is both straightforward and potentially free of area penalty. In contrast, incorporating a transistor will certainly require more layers, S/D interconnects, increase in processing steps, and an area penalty.

Despite the drawback of incorporating a transistor as a steering element, for the field of printed electronics, this may be acceptable due to two critical reasons: first, no other memory technology has been clearly shown as implementable with printing. As such, an increase in manufacturing complexity may well be tolerated to achieve a fully solution-processed memory. Second, the field is not yet concerned with scaling and density in way conventional semiconductor manufacturing is. Consequently, even with a non-maximally packed circuit structure, an implementable technology would be beneficial. Therefore, bipolar RRAM is an interesting candidate for printed memory, provided a fully solution-processed flow can be achieved. This chapter will demonstrate and examine such a memory cell consisting of an Ag/ZnO/Au stack.

4.3.5 Sputtered Ag/ZnO/Pt

The structure proposed in this chapter for an all-printed memory is quite similar to what has already been demonstrated via conventional routes. Yang et. al. have fabricated a Ag/ZnO/Pt cell at room temperature via sputtering[115]. Additionally, they have imaged what appear to be Ag conductive bridges responsible for switching. Manganese (Mn) doping was used in that work to decrease ZnO conductivity and increase the memory window (i.e. R_{ON}/R_{OFF} ratio). Figure 4.16 shows a schematic of the fabricated cells. Pt, ZnO:Mn, and Ag were deposited sequentially by RF magnetron sputtering. The cell shows bipolar switching characteristics with program and erase voltages of approximately ±2 V. The manufactured cells were cycled up to 100 times, showed R_{ON}/R_{OFF} ratios of up to 10^7, and good data retention for several months. The cells could be programmed with voltage pulses at a minimum pulse width of 5 ns. All of these specifications are very promising for plastic compatible implementation, if such a cell could be achieved with a solution-processed fabrication flow.

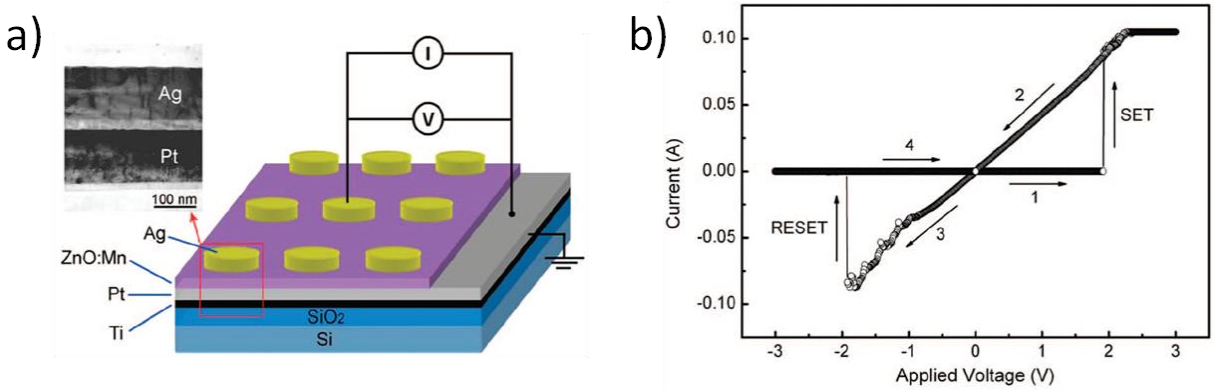

Figure 4.16. a) Schematic representation of fabricated RRAM devices. b) I-V curves showing bipolar switching characteristics.

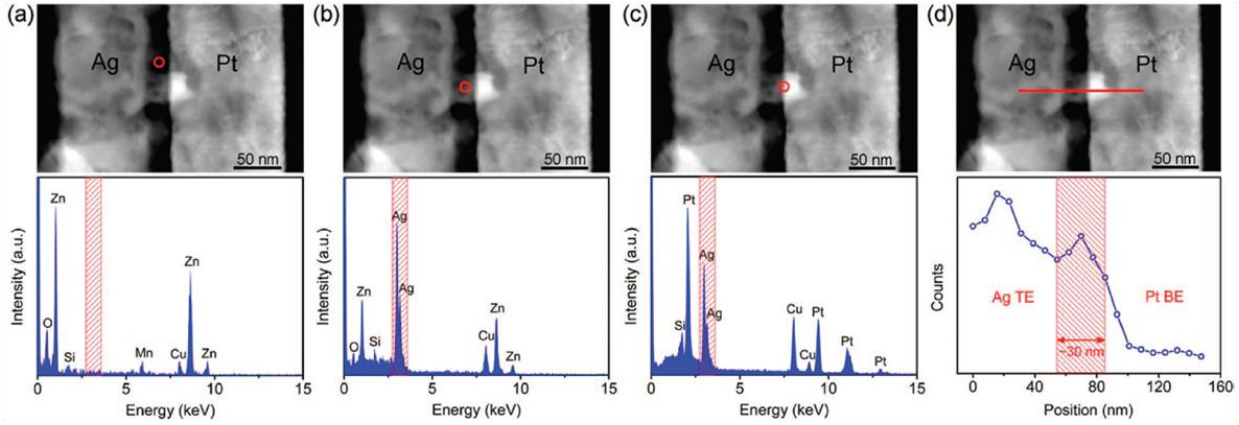

Figure 4.17. STEM Z-contrast image (top panels) and EDX analysis (bottom panels) of an RRAM cell cross section showing a silver conductive filament.

Figure 4.17 shows scanning transmission electron microscopy (STEM) images of cell cross-sections in the ON state with corresponding energy dispersive X-ray (EDX) data for points of interest. EDX analysis indicates that the conductive bridge spanning the two electrodes does, in fact, consist mostly of Ag. This strongly supports the filamentary switching theory by Ag ion diffusion through ZnO electrolyte.

The demonstration of this system is significant as it is very close to being entirely printable. As mentioned before, silver is common metal used in ink-jet inks for printing of conductive lines. Additionally, several paths have been demonstrated for solution-processable ZnO[18,30,116]. For the inert electrode, gold is proposed in place of platinum. Just like silver, gold based inks have been widely researched for as printed conductor candidates. Thus, a fully printed memory cell is possible.

4.4 Fabrication and Materials Characterization

A variety of cells structures were examined in this work with different extents of incorporation of solution-processing and printing. Initial, proof-of-concept cells were fabricated with evaporated Au and Ag electrodes, while final, fully printed cells were also examined. Commercially available inks were used for Ag and Au electrodes. ZnO inks were custom-synthesized. This section will discuss fabrication details related to materials and cell structures.

4.4.1 ZnO

4.4.1.1 *Synthesis*

Nanoparticles of ZnO were used as the primary ink component. Synthetic route similar to that used by our group previously was used for ZnO nanoparticles[30]. Approximately 1.17 g of zinc acetate (ZnAc) dihydrate was mixed in 175 ml of 2-propanol and allowed to dissolve at 50°C on a stir place. Then 0.34 g of sodium hydroxide (NaOH) dissolved in 175 ml of 2-propanol was added to the zinc source and allowed to react at 50°C for 10 minutes. At that point, 0.1 ml of dodecanethiol was added to the solution and the solution continued to stir for an additional 10 minutes. The solution was then dried in a rotoevaporator to remove the solvent. A

separatory funnel was then used to separate encapsulated nanoparticles from salts and other reaction byproducts. This resulted in a non-polar solution of nanoparticles which were again dried and collected.

The reaction of ZnAc with NaOH results in precipitation of material which consists of a combination of zinc hydroxide (ZnOH) and zinc oxide, depending on the conditions. The added thiol binds to the surface of precipitating material and serves three primary purposes. First, it encapsulates the growing particles thereby stopping the reaction and limiting the size of the final particles. Second, once encapsulated, it prevents interaction and agglomeration of nanoparticles. Agglomeration is undesired as it leads to large precipitates. Third, it makes the particles soluble in common organic solvents and available for solution deposition routes. Consequently, the size of the particles is dependent on the reaction time allowed before addition of the thiol and on relative concentration of the thiol to the reactants. Resulting nanoparticles are similar to those reported earlier and are approximately 3 nm in diameter (Figure 4.18).

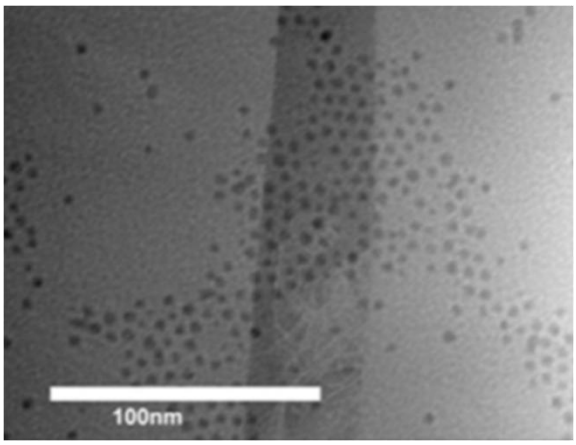

Figure 4.18. TEM micrograph of fabricated ZnO nanoparticles[30].

4.4.1.2 *Characterization*

Effects of thermal treatments on fabricated nanoparticles and films were investigated. Heat treatments were used to remove excess solvent and encapsulant, promote particle binding and sintering, and attempt to convert the ZnOH portion of the material into ZnO. Figure 4.19 shows thermogravimetric analysis and differential scanning calorimetry (TGA/DSC) response of the fabricated particle powders. Examining the TGA response, a slow decrease in mass is seen until about 260°C which is likely due to desorption of solvent and moisture. At that point, a large drop in mass is observed, which is representative of desorption and volatilization of the thiol encapsulant. DSC curves show multiple exothermic and endothermic peaks. Again, the peak around the decrease in the TGA data is likely related to desorption of the encapsulant. It is believed that some of the endothermic peaks above 350°C are likely related to film crystallization and sintering. Currently, further investigation is needed to completely identify the various peaks.

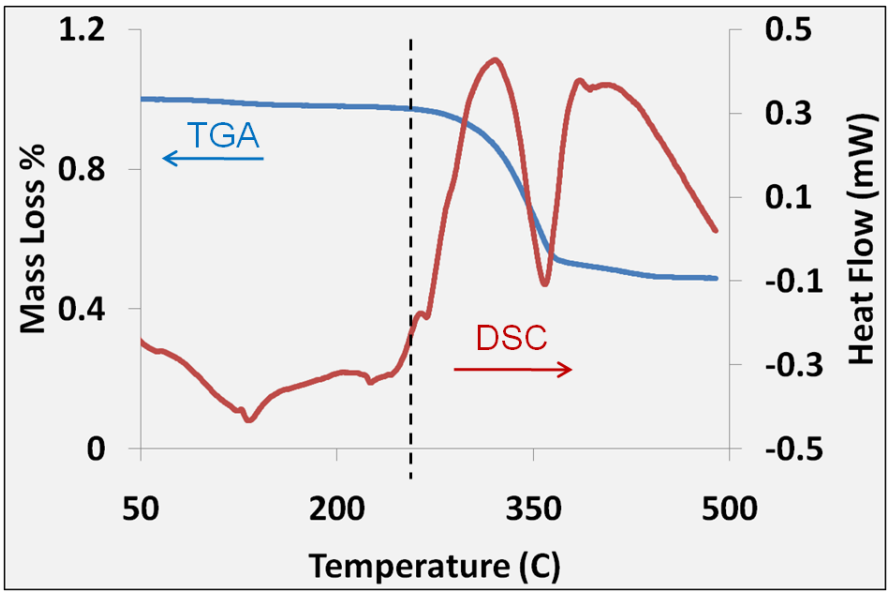

Figure 4.19. TGA/DSC curves showing mass loss and heat flow of ZnO nanoparticles.

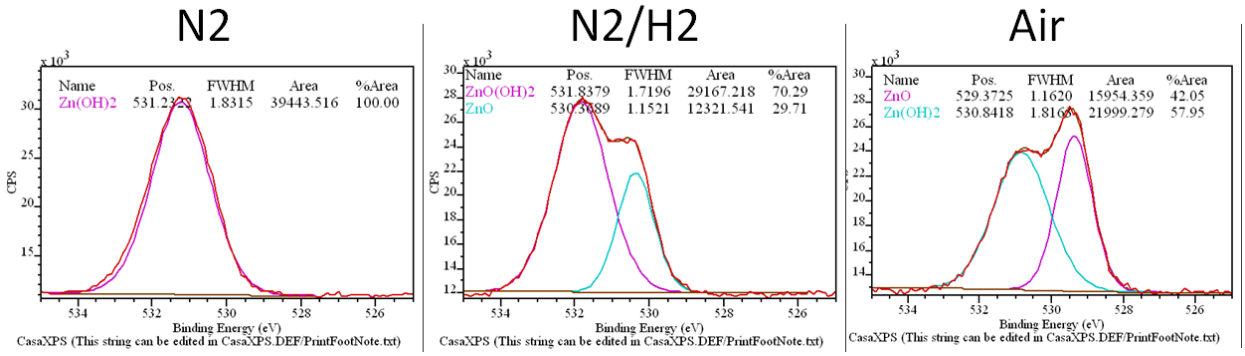

Figure 4.20. XPS binding energies of the oxygen 1s2 peak for samples annealed in N_2, N_2/H_2, and Ar.

Effects on the ZnO films of thermal treatments under varying ambients were examined. Annealing ambient may have a strong effect on the native resistivity of a ZnO film. This, in turn, affects the resistance of a memory cell in the OFF state. Hence, a film sintering condition which provides the highest resistivity would be beneficial for improving the memory window (R_{ON}/R_{OFF} ratio). Three ambients were selected to examine potential chemical interactions during the annealing step: Air, N2, and forming gas (N_2/H_2). Air was used as oxygen containing ambient to promote the conversion from ZnOH to ZnO. N_2 was used as an inert option to isolate temperature effects. Finally, forming gas was used to examine the effects of potential grain boundary passivation by hydrogen. All samples were prepared at 350°C. XPS data was obtained to investigate the concentration of ZnO vs ZnOH. In this case, the 1s2 peak of the oxygen spectra is observed at approximately 531 eV for the oxide bond and 532 eV for the hydroxide bond[117]. Thus, XPS can be utilized to examine the relative concentrations of Zn binding to O and OH groups.

Figure 4.20 shows XPS spectra for the binding energies of the oxygen 1s2 peak. High energy examination of this peak indicates the relative concentration of Zn-O and Zn-OH bonds, which appear at approximately 530 eV and 531 eV, respectively. It can be seen that a pure N_2 anneal results in a negligible amount of ZnO. In contrast, forming gas anneal results in close to 30% Zn-O bonds, while anneal in air achieves the highest conversion with 42% ZnO. However, within the boundaries of the cell structures that were tested, the different anneals provided no significant change in either R_{ON} or R_{OFF}. The consistency in R_{ON} is expected as the conduction happens through a formed metallic filament. The lack of response of R_{OFF} resistance to oxide/hydroxide stoichiometry suggests that conduction in the OFF state is likely through the boundaries of the highly nano-structured film as opposed to the bulk of the particles.

4.4.2 Cell Fabrication

Several flows were implemented for cell and array fabrication based on the extent of incorporation of solution-processed steps. All cells consisted of gold bottom electrode (BE), ZnO electrolyte, and silver top electrode (TE). Figure 4.21 shows a schematic of a generic cell fabrication flow. Original cells consisted of evaporated metal for both TE and BE. A printed TE was then implemented and tested. Subsequently, and all-printed electrode cell was made. ZnO was generally deposited by spin-coating for simplicity; however, an ink-jet printed system was also investigated. Spin-coating solution consisted of 3 wt% - 5 wt% solution of ZnO nanoparticles in chloroform. Spin speeds varied between 2000 RPM – 5000 RPM. Printing inks consisted of 6 wt% of ZnO nanoparticles in butylbenzene. Both types of solutions were subjected to vortex mixing and mild ultrasonication to achieve maximum solubility. Solutions were filtered before deposition to remove large agglomerates.

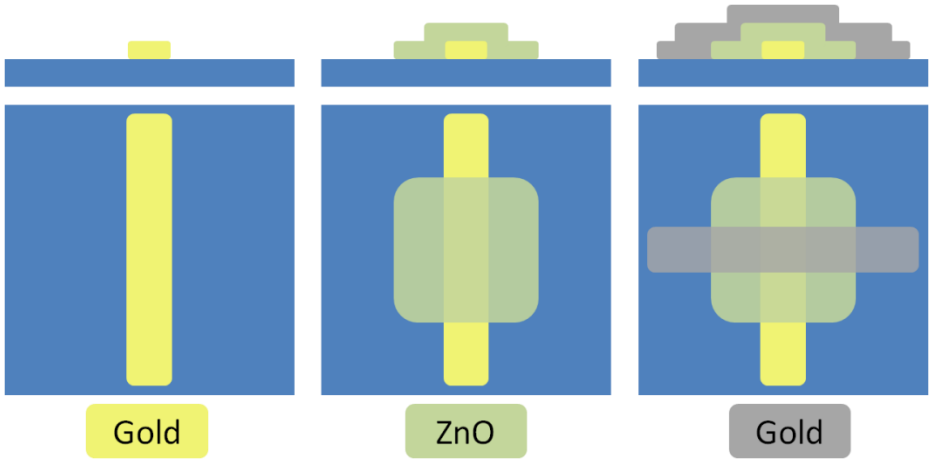

Figure 4.21. Schematic representation of a generic cell fabrication flow.

Gold was always deposited first, as the BE, due advantages in terms of to thermal and chemical stability during the ZnO film annealing process (up to 400°C). Thermally evaporated gold was used as-deposited. Printed gold lines were annealed at 250°C in air for 30 minutes. ZnO films, whether spin-cast or printed, were annealed at 200°C – 350°C in a custom furnace in various ambients. Silver TEs were either thermally evaporated and used as-deposited, or were printed and annealed at 200°C for 30 minutes.

4.4.3 Ink-Jet Printing

Printing of the gold lines was straightforward as the commercial ink is well-behaved both during printing and line drying. Printing conditions for ZnO had to be optimized for proper jetting, drying, and substrate interactions. In a process similar to that described in Section *2.5.1*, substrate temperature of 60°C – 80°C was determined to be optimal for feature morphology. Overall, the ZnO/butylbenzene solution jetted well and resulted in smooth films. Figure 4.22 shows AFM micrographs of annealed ZnO deposited on blank SiO_2 and on top of a gold line, as well as an AFM of a clean gold line. ZnO films deposited on blank SiO_2 are very smooth and uniform. The extracted RMS roughness is on the order of 4.2 nm. In contrast, films on top of gold lines exhibit large, discrete aggregates. This may be due to enhanced crystallization on top of gold the crystalline sites of which may serve as seeds. Alternatively, thiol, which is used as the encapsulant, is likely to have strong interactions with the gold and may cause agglomeration. The exact origin is yet to be determined; however, this behavior did not seem to affect device yield. The aggregates are not features of the gold itself, as evidenced by Figure 4.22(c).

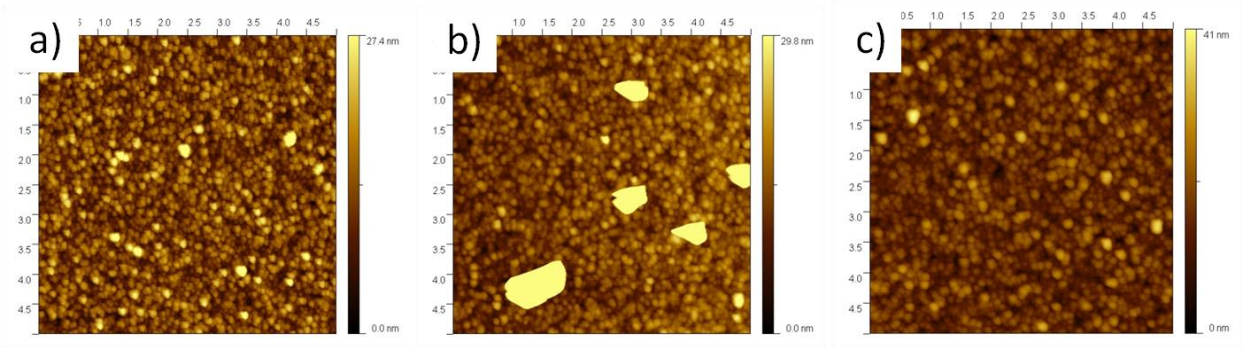

Figure 4.22. AFM micrographs of a) ZnO film on blank SiO_2, b) ZnO film on top of a gold line, c) clean gold line.

Printing of the silver lines was the most challenging as it had to be continuous across multiple surfaces and boundaries. Figure 4.23(a) shows a result of printing a silver line across a circular ZnO feature over a gold line. Two negative effects are clearly present: first, the splitting of the Ag line over Au; second, the splitting of the lines at the ZnO boundary and Ag ink migration to the exterior. The interplay of several effects is responsible for this behavior. Even after annealing, ZnO still has some encapsulant and organic contaminants bound to the surface. These make the surface somewhat hydrophobic and cause a high contact angle for an aqueous Ag ink. Thus, the ink beads off of the ZnO surface and onto a more favorable, hydrophilic, SiO_2 surface. Additionally, high curvature of the surface both at the ZnO boundary and around the Au line causes a high energy state for the liquid Ag line. To reach a lower energy state, the line splits. This effect has been observed in printed lines before[118]. To circumvent this problem, a spot feature was printed for the TE instead of a line, as demonstrated in Figure 4.23(b). This, of course, was implemented as temporary solution in order to proceed with investigation of cell RRAM properties. In order to achieve a real integrated array, lines and contacts would have to be printed across these and other features. The ZnO surface energy problem may be fixed by exposure to UV light or plasma to remove the organic contaminants and make the surface more

hydrophilic. Alternative ink formulations or surface modifications may also have to be employed. For the purposes of this work, a spot contact was sufficient.

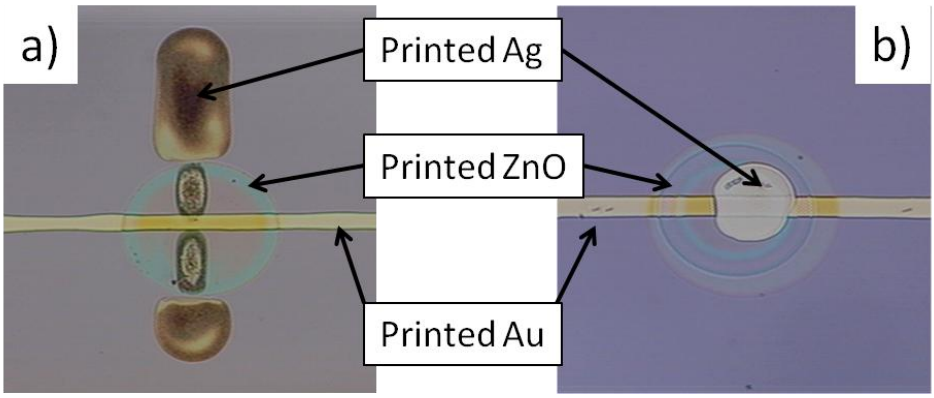

Figure 4.23. a) A silver line printed across a Au/ZnO stack, b) A silver spot printed in the middle of a An/ZnO stack.

4.4.4 Experimental Setup and Sample Preparation

All samples were printed on SiO_2 thermally grown on test Si wafers. Reactants for ZnO synthesis were purchased from Sigma Aldrich and used as-received. Solutions for ZnO deposition were prepared as described in Section *4.4.1*. Standard gold/silver contacts were deposited by thermal evaporation in a custom evaporator. For printing, CCI-300 silver ink from Cabot Corporation and NPG-J gold ink from Harima Chemicals were used. These were printed in a Dimatix DMP 2800 printer. All anneals were performed in air, unless otherwise specified.

Electrical measurements were performed with an Agilent 4155/6 parameter analyzer. Pulse measurements down to µs range were performed with an Agilent 41501B pulse generator unit attached to the parameter analyzer. Measurements of switching time below 5 µs were performed using a function generator to apply a pulse of desired width. Subsequently, a parameter analyzer was used to measure resulting resistance. Atomic force microscopy (AFM) measurements were taken with a Veeco Dimension 3100. XPS measurements were performed on a PHI VersaProbe Scanning XPS Microprobe.

4.5 Results and Discussion

This section will describe and discuss characteristics of various fabricated RRAM cells. Overall, good memory characteristics were achieved: cycling endurance of over 2000, indefinite data retention at room temperature, robust resistance to disturb voltage signals, and minimum programming time of 200 ns.

4.5.1 Electrode Study

Three electrode schemes were investigated: all-evaporated, evaporated Au BE with printed Ag TE, and all-printed. All-evaporated contacts were used as reference devices for simplicity and stability. Spin-cast ZnO films annealed in air at 350°C were used for all three sample types. Devices with evaporated Au BE were generally well-behaved and exhibited bipolar switching characteristics, as expected. Figure 4.24 shows representative I-V curves for a

switching cell with linear and logarithmic scales. The cell starts in an OFF state. As the voltage is swept positive, a critical bias is reached (about 0.5 V) and the filament forms. At that point the cell switches to the ON state (low resistivity). Upon sweeping the bias negative, a critical voltage is reached (about -1.4 V) to promote filament oxidation and dissolution. At that point the cell switches back to the OFF state. The process can then be repeated for further write/erase events.

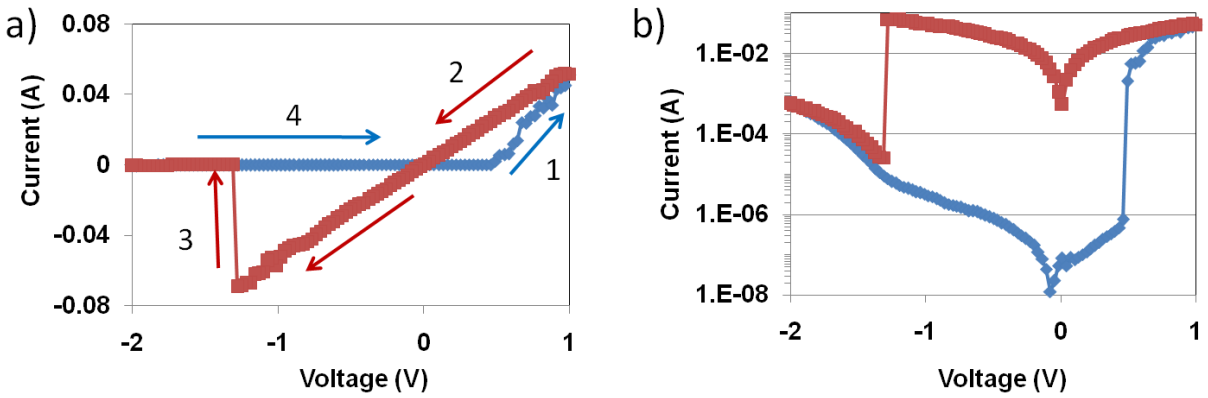

Figure 4.24. I-V characteristics of a cell with all-evaporated contacts showing bipolar switching behavior. a) linear and b) logarithmic scale.

This data was obtained by sweeping the voltage in the direction required for program/erase. Such graphs are helpful in determining cell characteristics such as switching voltages, current conduction characteristics, and filament overgrowth. However, in real applications, switching is achieved by voltage pulsing. This requires significantly less time and energy. The effects of pulse characteristics on cell behavior will be discussed later. The number of times this write/erase process can be repeated is generally referred to as cycling endurance. Unless otherwise specified, pulsing schemes in this work were implemented similar to flash memory, where a continuous pulse-test loop is used until the test returns desired state. To program, a high voltage pulse ("write pulse") is applied in an attempt to form a filament. A small voltage pulse ("test pulse") is then applied to measure cell resistance. If the measured resistance is LOW, then the programming sequence stops, and the program moves on to the erase sequence. Otherwise, the write pulse voltage is increased by a predetermined increment and the process is repeated until the desired R_{ON} is reached. To erase the cell (towards R_{OFF}), the same process is used with opposite bias. Here, the voltages required to program and erase are referred to as ProgV and EraseV, respectively. All the data, such as resulting resistances, program/erase voltages, and number of cycles required is recorded and stored for future examination. The starting voltages for program and erase pulse are generally set lower than expected necessary values to ensure that a minimum voltage required for the switch is used.

Figure 4.25 shows the evolution of voltage and resistance as a function of cycling for an all-evaporated electrode cell. The sample shows good endurance for almost 1300 cycles maintaining a memory window of over 10^2. Generally, all-evaporated electrode samples showed endurance of several hundred cycles, with a few passing the 1000 mark. Figure 4.25(c-

e) shows histogram of program and erase voltages and the correlation between the two. It can be seen that filaments formed under higher voltages require a higher voltage to erase. This can likely be attributed to the overgrowth mechanism, as discussed in Section *4.3.1*. The median ProgV and EraseV are ±0.6 V, which is significantly lower than the voltages required for either flash or FeRAM implementations.

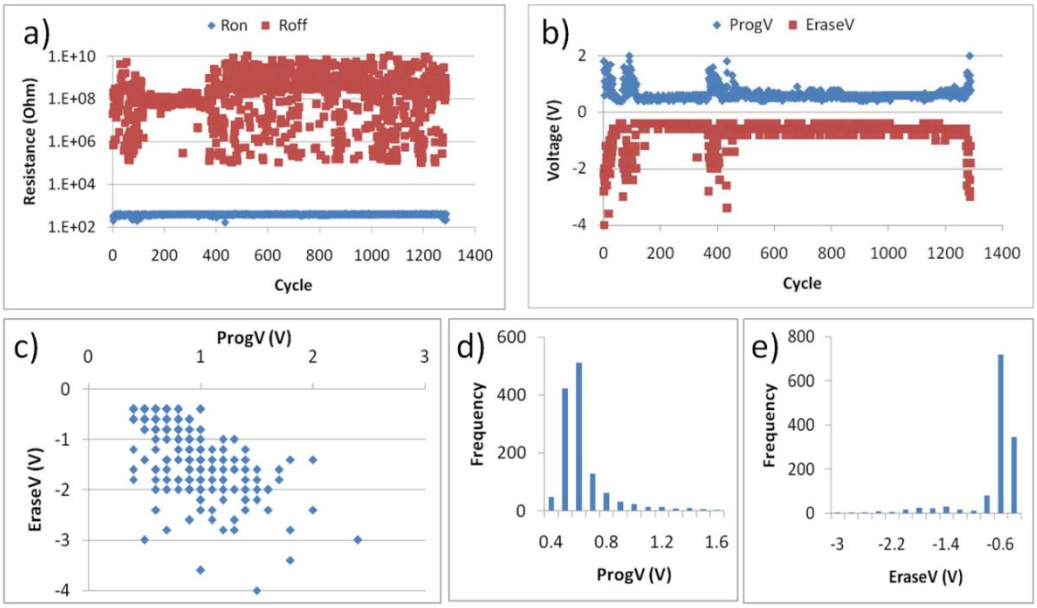

Figure 4.25. Cycling characteristics showing a) R_{ON}, R_{OFF} and b) ProgV, EraseV evolution for a cell with all-evaporated contacts. c) Erase voltage as a function of program voltage. Histograms displaying the spread of d) program and e) erase voltage.

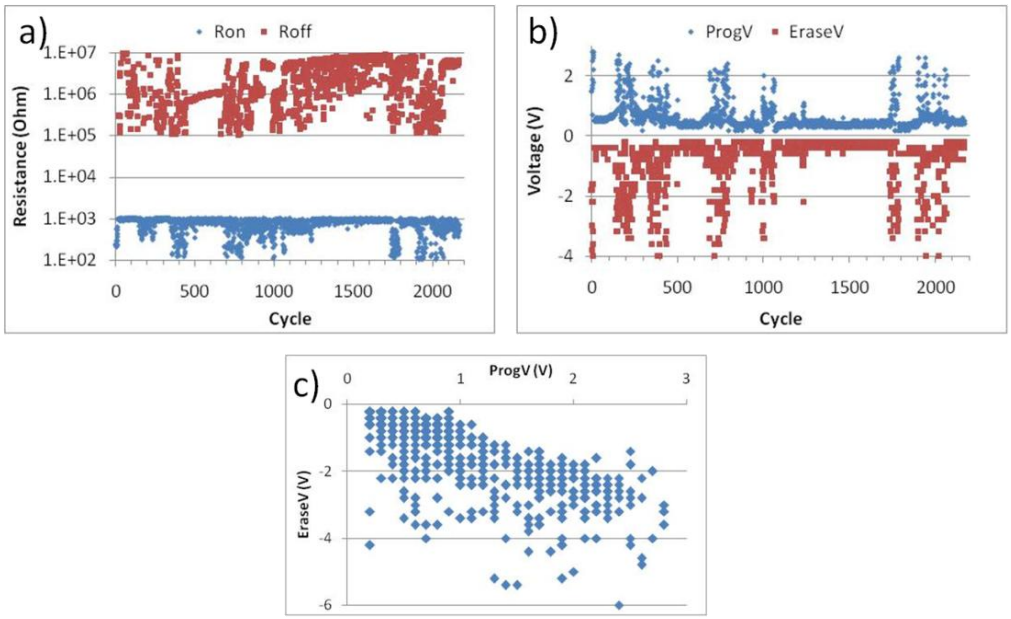

Figure 4.26. Cycling characteristics showing a) R_{ON}, R_{OFF} and b) ProgV, EraseV evolution for a cell with hybrid contacts. c) Erase voltage as a function of program voltage.

Figure 4.26 shows cycling data for a hybrid electrode cell with evaporated Au and printed Ag. It can be seen that the cell again performs well. It can be cycled over 2200 cycles with a minimum memory window of over 10^2. Average program and erase voltages are on the order of ±(0.4V – 0.6 V). Additionally, there is strong ProgV to EraseV correlation, similar to the all-evaporated case. This suggests that there is little difference between the operation of the evaporated and printed Ag electrodes.

Incorporation of printed Au BE proved to be a more challenging. Initial attempts of using Au lines printed and annealed to manufacturer specifications (250°C in air) resulted in "write once, read multiple" (or WORM) type behavior. That is, cells could be programmed but not erased. In fact, application of negative voltage to the Ag TE also resulted in a HIGH to LOW transition of cell resistance. Figure 4.27 demonstrates I-V characteristics of multiple WORM cells under positive and negative sweeps. Each curve represents a fresh cell. Both positive and negative bias results in similar program-type events. Since the Au BE is the only change in this system, this behavior is attributed to it. It may be due to an excess of organic contaminants remaining on the surface of the printed Au lines after deposition. Such contaminants may prevent the electron transfer from the cathode (Au) to the migrating Ag^+ ion, which is necessary for ion reduction and filament formation. In this case, no filament will be formed and dielectric breakdown will occur once critical electric field is reached in the electrolyte. The relative magnitudes of positive and negative breakdown voltages support this theory. Gold has higher work-function than silver (approximately 5.2 eV and 4.6 eV, respectively). They both form Schottky contacts to ZnO (electron affinity of about 4.2 eV[119]). However, gold electrode creates a higher barrier and, thus, higher native electric field. Consequently, to achieve critical electric field, a lower negative bias is required on the Au electrode than on the Ag electrode.

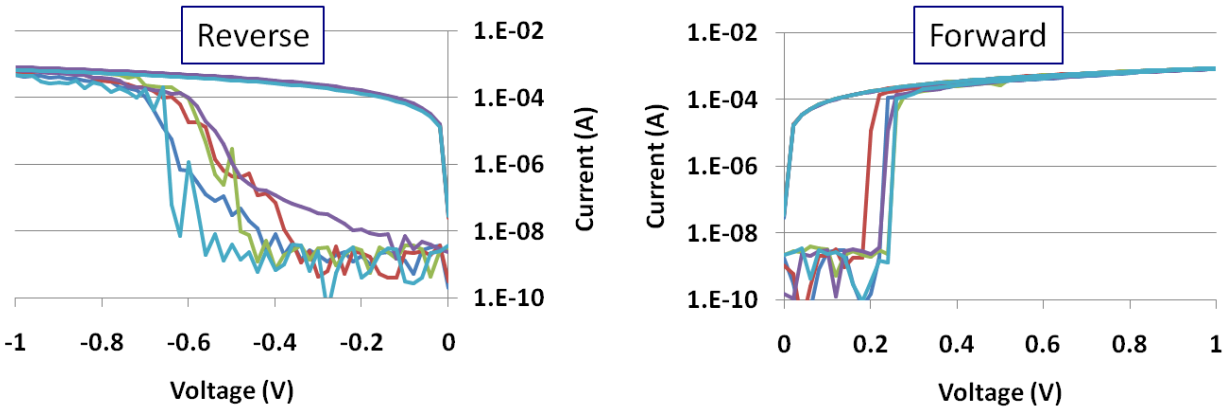

Figure 4.27. I-V curves showing WORM-type programming under forward and reverse bias.

To investigate the source of WORM behavior further, surface modifications were performed on the printed Au lines in an attempt to remove the organic contaminants. Three different schemes were implemented: ultraviolet ozone (UVO) clean, chemical (methanol) clean, heat treatment. UVO cleaning is a common technique for organic removal and surface modification. Additionally, methanol has been shown to remove nanoparticle encapsulants.

However, in this case, neither improved RRAM cell behavior and resulted in similar write-once cells as described previously.

Thermal treatment, in contrast, resulted in cells which could be cycled repeatedly, similar to the ones with evaporated Au BE. It consisted of one hour anneal at 350°C in air. This temperature was selected since this value is used for ZnO film anneals. Figure 4.28 shows I-V characteristics for cells with thermally treated Au BE. Some cells exhibited standard bipolar characteristics where application of negative bias to the Ag TE resulted in cell erase (as demonstrated in part (a)). However, some cells also exhibited an erase-and-reprogram behavior, as demonstrated in Figure 4.28(b). Fortunately, the "reprogram" part occurs at higher voltage than is necessary to erase. This can be avoided during real pulse programming, where the voltage sweep is stopped as soon as the OFF transition occurs. Figure 4.29 shows cycling data for cells with thermally treated Au BE. The sample show good endurance up to 300 cycles maintaining a minimum memory window of over 10^6. The memory window is significantly improved over the all-evaporated electrode samples; the exact origin of this improvement is unclear currently and requires further investigation. Program and erase voltages were approximately 1 V and -6 V, respectively. On average, these samples demonstrated endurance on the order of 100 – 200 cycles.

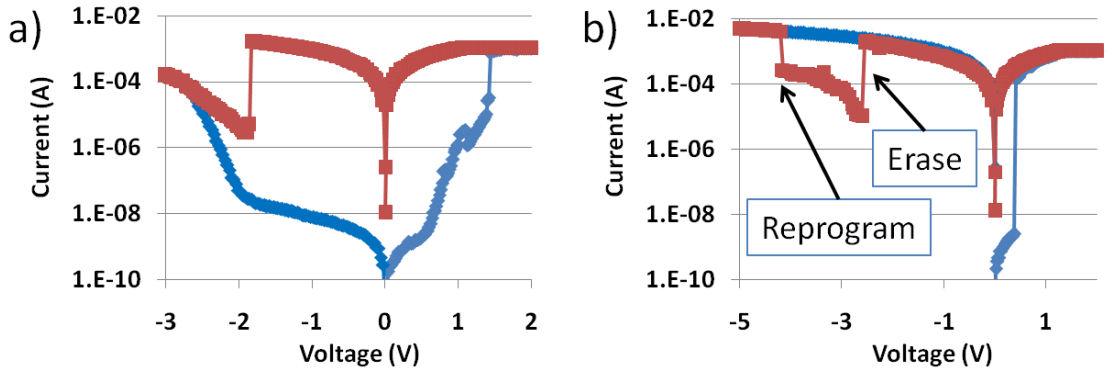

Figure 4.28. I-V characteristics of a cell with all-printed contacts showing a) bipolar switching behavior and b) bipolar switching behavior with a reprogram event.

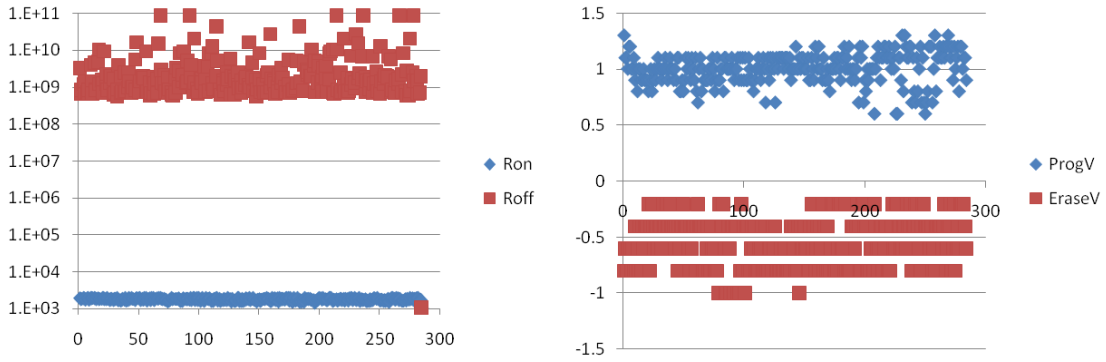

Figure 4.29. Cycling characteristics showing a) R_{ON}, R_{OFF} and b) ProgV, EraseV evolution for a cell with all-printed contacts.

Thermal treatment of 350°C is clearly not ideal for plastic-compatible fabrication. In the future, in order to avoid high temperature "cleaning" of the Au electrodes, a more aggressive low temperature process may be implemented. One such clean may involve oxygen or inert plasma; plasma cleaning techniques for removing organic contamination are widely used[120]. Alternatively, a different ink formulation could be used for the inert bottom contact. Shorter chain alkanethiols have been shown to dissociate from printed gold nanoparticles at temperatures as low as 120°C.

4.5.2 ProgV/EraseV Characteristics

As discussed in Section *4.3.1*, erasing of the cell does not completely dissolve the conducting filament. Consequently, voltage required to program a cycled cell is significantly lower than voltage required for a fresh cell. Figure 4.30(a) shows I-V curves of consecutive programming sweeps on a given cell. It can be seen that with increasing cycle count, voltage required to program the cell steadily decreases. Additionally, the native resistance of the cell decreases by about 10^3 after initial programming, as demonstrated by an increase in current at low bias. Both these effects are consistent with the theory of partial filament dissolution. Figure 4.30(b) shows ProgV and EraseV evolution through ten cycles averaged over several cells. A large decrease in magnitude occurs over the first 3 cycles and then the values saturate as the cycle count increases.

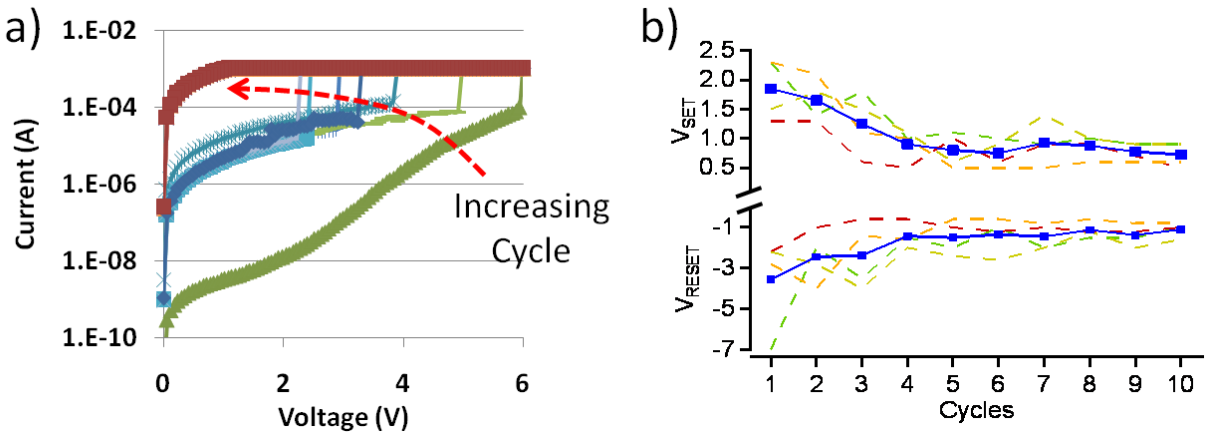

Figure 4.30. a) I-V curves for successive programming cycles showing a decrease in ProgV. b) ProgV and EraseV evolution as a function of cycles averaged over several cells.

The interaction between program/erase pulse width (PW) and switching voltage was investigated. To avoid voltage drift effects, PW value was selected at random within predefined boundaries before each program/erase event. Programming then proceeded as described earlier, where progressively higher voltage pulses were applied until the cell switched. The resulting program/erase voltages were then compared to the PW of individual cycles. EraseV seemed to have little correlation with erase PW. In contrast, ProgV has a strong inverse correlation to programming PW. Figure 4.31 demonstrates the relationship between programming PW and voltage. This relationship is anticipated, as programming at lower

voltages is expected to take longer; thus, allowing a longer PW may provide enough time to complete filament growth at lower voltages.

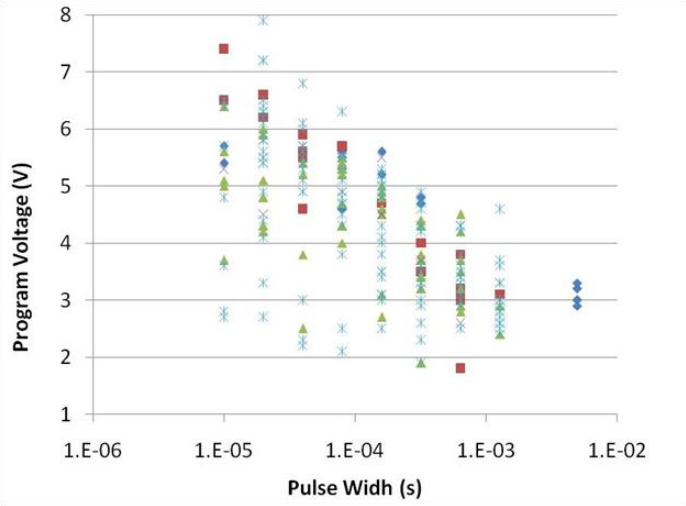

Figure 4.31. Programming voltage as a function of applied pulse width.

More detailed studies of programming time dependence on applied voltage will be presented in later sections. However, it is important to emphasize the tradeoffs between programming voltage and time in the context of application requirements. The logarithmic dependence of voltage on time indicates that a small increase in voltage can dramatically reduce the time required for programming. This could be beneficial for applications where programming time is important. Alternatively, mobile applications with low voltage requirements which do not need high speed switching, could benefit from reduced bias operation at the expense of programming speed.

4.5.3 Data Retention and Voltage Disturb Effects

One of the key metrics of any non-volatile memory is the extent of its non-volatility. This is often characterized by data retention in an idle cell or by robustness to random voltage spikes in the system, usually referred to as disturb signals. In the case of filamentary RRAM, the most likely reason for loss of data retention is undesired dissolution of the filament. This could happen in systems where the formed conductive filament is excessively narrow or the diffusivity of the reactive metal in the electrolyte medium is very large. In both cases, unintentional dissolution of the filament renders the memory ineffective. Disturb signals in a memory array most often happen due to capacitive coupling to adjacent electrodes and cells. A large signal on one line may induce a smaller voltage spike on neighboring lines. The individual voltage spikes may be too small to induce noticeable effects on a cell, but overtime these could add up to erase a cell. It is important to understand such effects on any given memory technology.

Both retention and disturb dynamics of fabricated cells were examined. The following measurements were performed on all-evaporated electrode cells. Figure 4.32(a) shows representative retention data for the cells tested. Resistance determination was made by

introducing a 50 mV pulse with 50 ms width to the cell and measuring resulting current (similar to the "test pulse" during cycling). Very little deterioration of R_{ON} and R_{OFF} is present at 10^4 seconds. A memory window of over 10^4 is observed throughout. Effects of higher magnitude pulse tests are presented in Figure 4.32(b). It can be seen that resistance percent change is very small. This is not surprising since positive bias is used to program the cell and is not expected to negatively affect the filament.

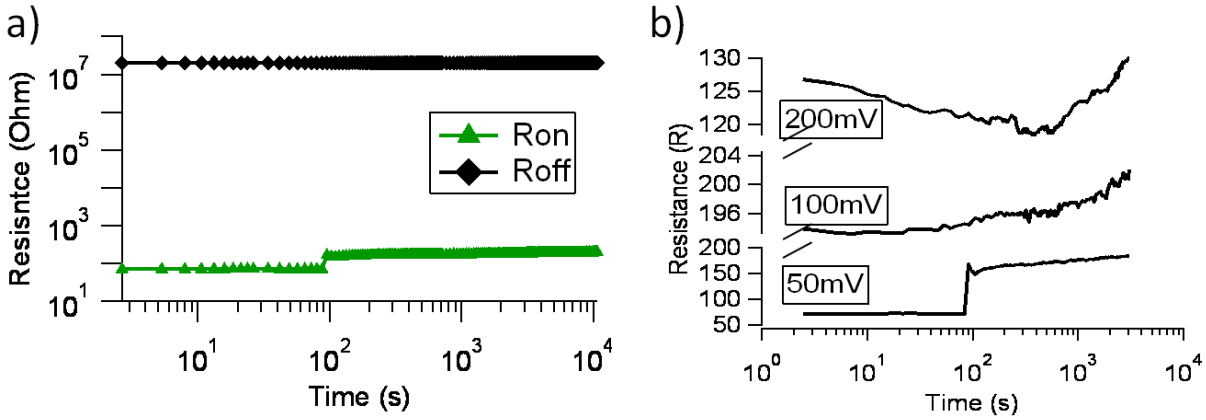

Figure 4.32. a) R_{ON} and R_{OFF} as a function of time. b) R_{ON} as a function of time with different read pulse voltages.

Effect of negative disturb pulsing is demonstrated in Figure 4.33. Widths of these pulses were 50 ms. It can be seen that pulses of magnitude up to of 140 mV have little effect on cell R_{ON} even with repetitive application of 1500 times. However, once -160 mV is applied, cell resistance starts to steadily increase with each pulse. After approximately 700 pulses R_{ON} is deteriorated out of specified boundaries. This implies that cell filaments are fairly stable, considering the erase voltage for an average cell is on the order of 0.5 V – 1 V. This means that a large number of voltage spikes on the order of 15% – 30% are required to erase a cell accidentally.

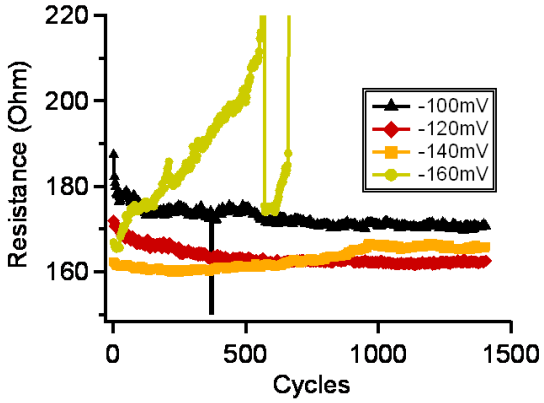

Figure 4.33. R_{ON} as a function of disturb pulsing cycles at different pulse voltages.

4.5.4 Cell Size Effects

As mentioned earlier, RRAMs exhibiting filamentary switching have a weak or negligible dependence on cell area in the ON state and a linear dependence in the OFF state. This is in contrast to RRAMs exhibiting areal switching, such as injection barrier modulated systems. In the OFF state, conduction proceeds through the entirety of the insulating area, as would be expected of a MIM structure. Conversely, the ON state of a filamentary RRAM cell is determined by a single, localized conduction path. As such, areal dependence of R_{ON} is very weak. It should be noted that the strong correlation between R_{OFF} and cell area is most relevant in fresh cells. In a cycled cell, OFF state conduction is still partially localized by the remainder of the filaments created by previous programming steps.

Effect of cell area on cell resistance was investigated. Measurements were taken on hybrid evaporated Au/printed Ag cells. Cell size was variation was achieved by controlling the number of contiguous lines printed for a given sample. This could be easily achieved "on the fly" by modifying the printing program input, which demonstrates the merits of ink-jet printing as a materials prototyping tool. Figure 4.34 demonstrates dependence of R_{ON} and R_{OFF} on fabricated cell area averaged over multiple samples. A strong correlation to R_{OFF} is clearly present, while R_{ON} shows little to no correlation. This is yet another indicator of filamentary switching in RRAM fabricated in this work.

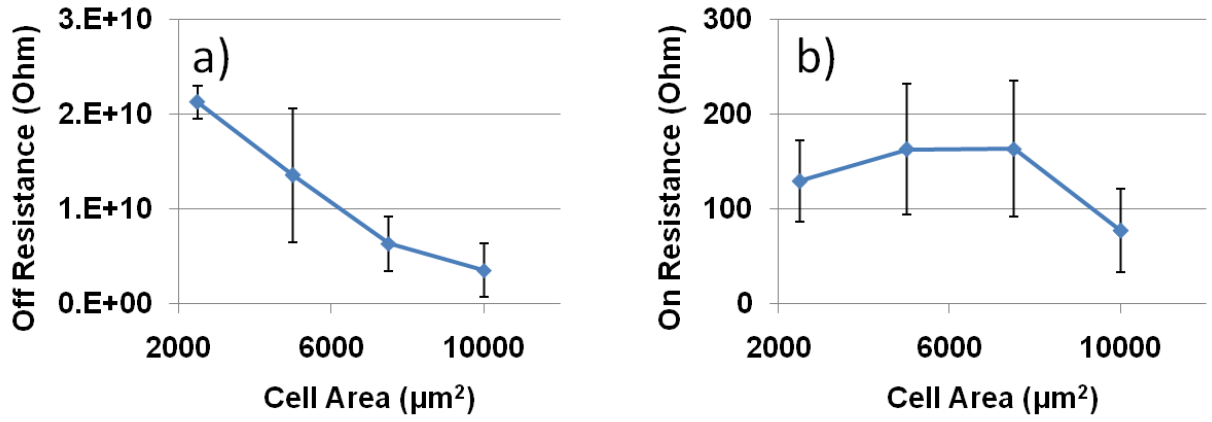

Figure 4.34. R_{ON} and R_{OFF} as a function of cell size.

4.5.5 Low Temperature Fabrication

Generally, high temperature is required for device fabrication involving ZnO due the material's high melting point. Transistors fabricated with ZnO nanoparticles or sol-gel often have to be annealed at 400°C or above. This is necessary to maximize particle sintering and improve grain size and interactions. In contrast, an RRAM cell does not require a fully-sintered film with large grains. In fact, an electronically poor film may be beneficial if it provides a higher native resistance, which will result in a higher R_{OFF} and, thus, improve the memory window. A set of low temperature cells was fabricated with the hybrid evaporated/printed electrode structure and a spin-cast ZnO film. Unlike the previously described samples, the ZnO film was subjected to a 200°C anneal, which is compatible with some plastic substrates.

Figure 4.35 shows representative I-V curves for a sample annealed at 200°C.These cells exhibit reasonable bipolar behavior; however, the overall stability is poor. Some cells exhibit WORM-type behavior and the best samples can only be cycled about 10 times. The exact reasons for poor reliability and endurance are unclear at this point. Even at 350°C the ZnO films are not expected to undergo large amount of crystallization, so grain size is likely not the reason for undesired behavior. Clearly, a large portion of organic contaminants still remain within the film at 200°C, as suggested by TGA data in Figure 4.19. It is possible that excess organic material negatively affects the ionic conduction and electrode reaction dynamics. In fact, the encapsulant used in ZnO fabrication (an alkanethiol) is also often used as an encapsulant for gold and silver. It is feasible that excess thiol in the electrolyte film binds to and passivates the silver ions, thereby preventing filament material diffusion. Thiols may also interact with the gold electrode in ways similar to those described in Section *4.5.1*. Perhaps, pathways described there for dealing with excess organic material (such as O_2 plasma) could be used to remove contaminants from the ZnO film.

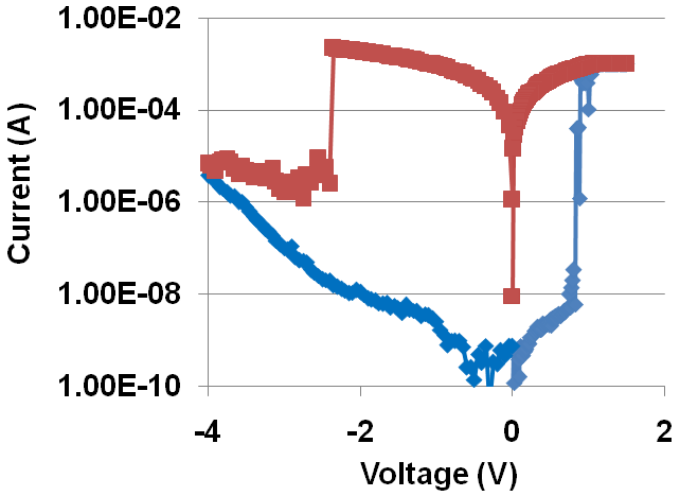

Figure 4.35. I-V characteristics of a cell with ZnO annealed at 200°C.

4.5.6 Switching and Filament Growth Dynamics

Further insight into the filament growth process can be obtained by examining RRAM cell switching behavior during potentiostatic and potentiodynamic biasing, as well as switching under different temperatures.

4.5.6.1 *Potentiodynamic Measurements*

Potentiodynamic measurements consist of sweeping voltage across the cell at constant rate. Such measurements could be directly correlated to the filament crystallization and growth dynamics at the electrode interface. As mentioned earlier, filament formation consists of three main processes: anodic oxidation and dissolution, ion diffusion through the electrolyte, and cathodic reduction and crystallization. The last process is often estimated to be the rate limiting step of a SET process in an electrochemical metallization (ECM) cell[121]. The first process, anodic dissolution, is expected to be fast because no crystallization overpotential is involved. Additionally, no concentration overpotential is expected at the anode/electrolyte interface, as

reactive ion are exposed to high electric field and expected to migrate rapidly. The second process, ion diffusion, is also expected to be fast because of large long-range disorder in amorphous oxide systems in general, and in nano-crystalline ZnO in particular[122,123]. Thus, cathodic electrocrystallization is left as the likely rate-limiting process of the SET process.

Given the cathode interaction of the diffused ions, the resulting filament growth current density can be described by the Butler-Volmer (BV) equation[110]:

$$i = i_0 \left[\exp\left(\frac{\alpha z e \eta}{kT}\right) - \exp\left(-\frac{(1-\alpha) z e \eta}{kT}\right)\right] \quad (1)$$

where i_0 is the exchange current density, α is the cathodic charge transfer coefficient, ze represents number of electronic charges, and η is electrochemical overpotential. For high cathodic overpotential ($\eta \gg kT/ze$), the BV equation can be rewritten as:

$$\ln i = \frac{\alpha z e}{kT}\eta + \ln i_0 \quad (2)$$

Additionally, the charge needed for 1D growth of a filament given a potentiodynamic voltage sweep can be described as:

$$Q_{SET} = \int_0^{V_{SET}} \frac{I_f}{v} dV = \int_0^{V_{SET}} \frac{i\pi r_f^2}{v} dV \quad (3)$$

where V_{SET} is the switch-on voltage, I_f is the growth current of the filament, i is the electrodeposition current density, and r_f is the filament radius. Combining equations (2) and (3), the following expression for switching voltage (V_{SET}) as a function of sweep rate can be obtained:

$$V_{SET} = \frac{kT}{\alpha z e} \ln v + \frac{kT}{\alpha z e} \ln \frac{Q_{SET} \alpha z e}{i_o \pi r_f^2 kT} \quad (4)$$

where v (=dV/dt) is the voltage sweep rate. Using this equation, temperature dependencies and cathodic charge interactions can be investigated.

In this work, sweep rates of 0.005 V/s to 10 V/s were examined. Figure 4.36 shows the set voltage (V_{SET}) as a function of sweep rate (v). As predicted by equation (4), there is a logarithmic relationship between v and V_{SET}. From, the slope of the line fitted to the exponential portion of the graph, a value of ≈ 0.02 can be extracted for α. V_{SET} reaches a lower limit at rates below 10 mV/s. This apparent threshold voltage may be due to some combination of minimum overpotential required for Ag crystallization at the inert electrode and overpotential required for Ag oxidation at the anode. The lower saturation of V_{SET} suggests that filament growth proceeds faster than the rate of voltage change. That is, once the threshold of about 4.3 V is reached, filament growth rate is independent of sweep rates below 10 mV/s.

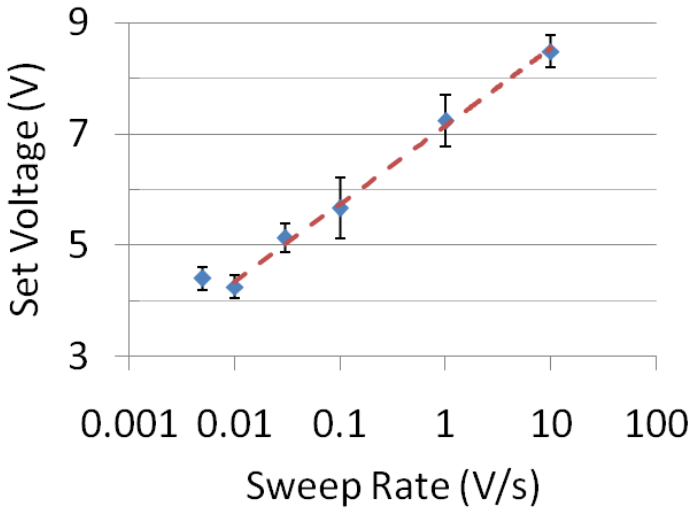

Figure 4.36. Set voltage as a function of sweep rate.

Additionally, equation (4) suggests that V_{SET} should be dependent on electrolyte thickness as longer filaments would be required for thicker films. Longer filaments would, in turn, require more ions to diffuse, which necessitates larger Q_{SET}. This, in fact, has been shown experimentally for the initial set process (forming)[124]. However, after the initial forming step, V_{SET} is largely independent of fabricated electrolyte thickness. This can be attributed to the remnant filament phenomenon, where subsequent programming only needs to bridge a small distance within the broken filament.

This type of set voltage response to the change in sweep rate is another indicator of filamentary switching, and it has been observed experimentally[121] and in simulation[125]. The extracted charge transfer coefficient can be used as one of the simulation parameters of the system, as it represents the chemical reaction rate at the electrodes. The minimum threshold for V_{SET} should also be considered as it represents the lowest voltage that the system has to be capable of producing in order to achieve successful programming.

4.5.6.2 *Potentiostatic Measurements*

Potentiostatic measurements consist of applying a voltage step to a cell and measuring the time required for switching. Combined with temperature variation, these measurements could also be used to investigate cell switching dynamics. Here, voltage steps of 2.5 V – 5.5 V were used. Time was measured until a predetermined low resistance was reached. Measurements were performed on fresh, unprogrammed cells. This means that the observed switching times represent the forming process, as described earlier, and account for filament growth across the entire thickness of the electrolyte. The processes involved in filament formation (as described in previous section) could have an exponential relationship to the applied electric field. Thus, an exponential relationship is expected between switching time (t_{SW}) and voltage (V_{SW}), and can be generally expressed as:

$$t_{SW} \propto e^{-\beta V_{SW}} \qquad (5)$$

where β is a fitting parameter proportional to the charge transfer coefficient (α) used in the BV equation[126].

Figure 4.37 demonstrated the relationship between switching time and voltage for cells programmed at various temperatures. As expected an exponential relationship can be observed. However, the responses at 27°C and 47°C appear to have two distinct regions of operation at low and high V_{SW}. This is likely an indication of different rate limiting processes being dominant at different biases. Furthermore, β at high bias appears to be roughly double that of low bias. This type of behavior has been previously observed with Ag_2S atomic switch RRAM[126]. The authors postulated that at higher electric fields, filament growth is limited by the ionic diffusion, whereas at lower fields, growth is limited by the electrochemical reaction at the electrodes. This is a plausible, with the assumption that diffusion is a weaker function of potential than the cathodic reaction[127,128].

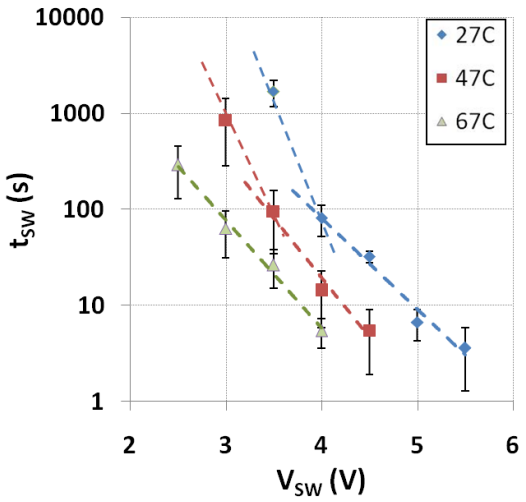

Figure 4.37. Switching time as a function of applied voltage.

Additionally, Figure 4.37 does not show a dual region response at 67°C. Both diffusion and electrode reactions have an exponential dependence on temperature. However, if the activation energies are different, as they most likely are, one of the factors may become significantly larger than the other within the voltage ranges examined in this study. This could result in a single region behavior, as is exhibited at 67°C. Given the similarity of the slope of the high temperature line to the high field regimes of the low temperature lines, high temperature switching is likely diffusion limited.

It should be noted that further investigation into the exact dynamics of cell switching would be beneficial for understanding ECM RRAM. To date, most theories (including the ones presented in this section) attempt at deconvoluting the multitude of processes that go on in these cells by selecting certain aspects of certain experimental results. However, no direct experimental observations of the individual processes have been presented. This is not surprising given their inherent interdependencies, where all the processes involved in filament formation and dissolution are directly dependent on applied voltage and temperature.

Given the observed relationship between switching voltage and time, a potential operational tradeoff can be observed (similar to the one described in Section *4.5.2*. As mentioned at the beginning of this section, switching times in Figure 4.37 represent forming voltages of fresh cells, which are significantly larger than the voltages required to program cycled cells. Thus, fresh cells can be "burned in" at low voltages over longer times prior to product distribution. Subsequently, these memories can be programmed with lower time and bias requirements during real product operation.

4.5.6.3 *Temperature Measurements*

The relationship between temperature and cell switching dynamics was also investigated. As discussed in the previous section, varying temperature during cell operation can elucidate some of the interactions of the processes active during switching. Effects of temperature on switching voltage (under potentiodynamic conditions) and switching time (under potentiostatic conditions) were examined. Figure 4.38 shows the V_{SET} as s function of temperature. Equation (4) shows both linear and logarithmic temperature components when calculating voltage, hence a sublinear relationship is expected. This matches the response presented. As expected, V_{SET} decreases continuously with increasing temperature. This is likely related to both faster electrode reaction and ionic diffusion.

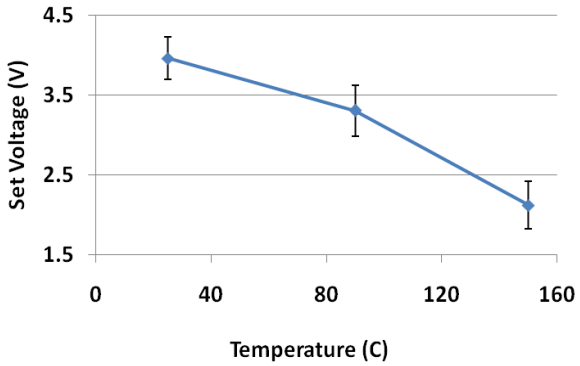

Figure 4.38. Set voltage as a function of temperature.

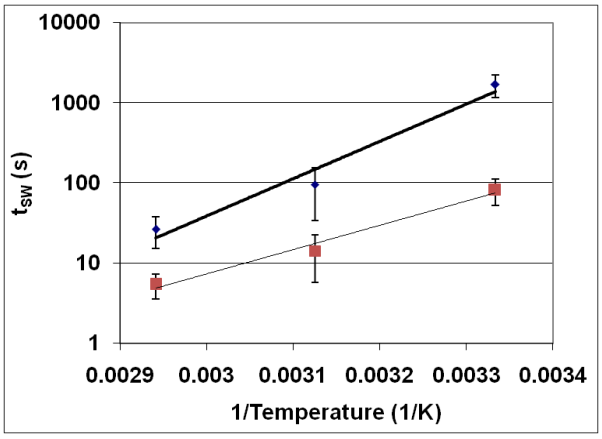

Figure 4.39. Switching time as a function of inverse temperature (1/T).

Figure 4.39 shows switching time as a function of inverse temperature (1/T) under potentiostatic conditions at 3.5 V and 4 V. Exponential relationship is expected for t_{SW} and can be generally described as[126]:

$$t_{SW} \propto e^{E_a/kT} \quad (6)$$

where E_a is the activation energy representative of an Arrhenius temperature response. As anticipated, switching time decreases with increasing temperature. Activation energies were extracted to be 0.92 eV and 0.6 eV for biases of 3.5 V and 4 V, respectively. These are similar to those obtained with Ag_2S switches (0.58 eV – 1.32 eV). These similarities suggest that reaction and diffusion rates responsible for filament formation within the Ag/ZnO/Au stack examined here are likely similar to Ag ion diffusion and reaction rates given an Ag_2S electrolyte.

4.6 Summary

Solution processed RRAM cells were fabricated. These cell exhibited good memory characteristics, such as cycling endurance of over 2200, perfect data retention for the maximum measured time of 10^4 seconds, minimum programming time of 200 ns, and good stability under voltage disturb testing. To achieve good memory behavior, 350°C anneals of ZnO films were necessary. A 200°C cell was fabricated and exhibited memory characteristics; however, overall endurance and reliability was poor. To achieve a fully solution-processed cell a thermal "cleaning" step (also 350°C) of the printed gold electrode was required.

Effects of cycling and pulse width variation on programming characteristics were examined. Both programming and erase voltage decreased with initial cycling, which is attributed to the remnant filament effect. Programming voltage also showed a strong correlation to the voltage pulse width. R_{ON}, unlike R_{OFF}, showed a dependence on cell area, which supports the filamentary switching mechanism. Filament growth dynamics were investigated with potentiostatic, potentiodynamic, and temperature measurements. These suggested that two limiting regimes (diffusion and electrode reaction) may exist at different programming conditions.

Overall, these results suggest that Ag/ZnO/Au based RRAM cells could be a promising candidate for low-cost, solution-processed electronics. The biggest factor that currently precludes its implementation is the high temperatures (350°C) required for ZnO film treatment. This problem may be solved by going to alternative ZnO deposition routes. Recently, low temperature sol-gel routes have been demonstrated which could replace the nanoparticle flow used in this work [28,129]. Of course, future investigation is necessary to verify compatibility of these processes with an all-printed flow.

5 Conclusions and Future Outlook

In this work, solution-processable transistors, conductors, and memories were investigated as possible candidates for printed and transparent electronics. Just like any emerging technology, printed electronics need to outperform the existing technologies in a given field in the aspect of cost or performance to see successful implementation. Alternatively, an emerging technology may enable an entirely new market which was infeasible or impractical previously. In the case of printed electronics, both scenarios may apply. For example, RFID has been an established technology for several decades and has seen wide spread implementation. However, despite the potential advantages and a large engineering effort, RFID has not been able to reach the ubiquity level of conventional barcodes. In this particular market, solution-processed electronics may be able to compete based on cost by reducing the fabrication expenses of a tag. In contrast to RFID, the push towards flexible electronics is a fairly recent one, particularly on the scale of personal and mobile applications. In this case, there are no established technologies. Consequently, development of printing and solution-processing techniques has been closely related to developments in flexible electronics. Any electronic application will consist of an ensemble of discrete components, such as passive elements, conductors, transistors, memory, and display elements. This chapter will summarize the results obtained in this work related to some of these components.

Transistors and conductors investigated in this work were based on reduced graphene oxide (rGO) and could be fabricated at temperatures as low 80°C, which is compatible with low-cost plastic substrates. A key enabler of solution processing is the availability of solutions which can be transformed into desired materials. However, in the context of deposition, such as printing, extra effort is often required to achieve desired features. As discussed in Sections *2.5.1* and *3.4*, control over precise ink formulation, jetting conditions, and printing temperatures was required to realize good feature uniformity and morphology. By controlling the printing conditions and film thickness, both metallic and semiconducting rGO films could be achieved. This could be beneficial for two reasons: first, it simplifies the manufacturing process by allowing multiple parts of a device to be printed with a single ink, thereby eliminating processing steps. Second, it allows incorporation of graphene into S/D contacts, which has shown to increase performance of devices based on both organic and inorganic active materials.

In Chapter 2, printed TFTs were presented and exhibited drive currents of up to 1µA, ON/OFF ratios of up to 10, and mobilities of 0.015cm^2/V-s. Although the achieved drive current and mobility could be sufficient to drive a basic display cell, a significantly larger ON/OFF ratio would be required to drive a large pixel array, as discussed in Section *2.5.2.4*. Currently, ON/OFF ratios of over 10^3 have only been achieved with graphene nanoribbons or dual-gate structures. Both are possible with printing techniques; however, new graphene inks or TFT structures have to be developed. Additionally, the inks used here could be improved to incorporate larger GO flakes. The inks used had flakes on the order of 0.5 µm – 1µm. In the literature, solutions of GO sheets with sizes up to 25µm have been reported. Increasing average

sheet size should improve drive currents significantly by reducing inter-flake transport, which act as effective grain boundaries.

In Chapter 3, printed conductors were presented and exhibited resistivities on the order of $5x10^{-4}$ Ω-m. This would result in a sheet resistance of $5x10^{3}$ Ω/□ at a thickness of 100 nm. This is significantly larger than the sheet resistance of ITO films currently used in LCD manufacturing; however, current ITO films are not compatible with flexible substrates, as discussed earlier. Consequently, fabrication on such substrates has focused on organic conductors or solution-processed TCOs and rGO, which exhibit resistivities similar to those achieved in this work. Furthermore, similar to the effects on TFT drive currents, improving the inks by incorporating larger GO sheets will improve the resistivities of rGO conductors.

Having demonstrated fabrication of rGO as an active material and a conductor, the next logical step is to combine the discrete components into an all-graphene transistor. This is likely to improve overall performance of printed rGO TFTs as it has been shown with other graphene transistors. Additionally, performance could be improved by increasing the size of GO sheets used for ink formulation. Finally, the ON/OFF ratio of these rGO devices needs to be addressed. As discussed earlier, formulating inks with graphene ribbons or dual-gate TFT architectures could result in a reduction of leakage current and improvement of the ON/OFF ratio. Combining these improvements would result in a printed rGO technology which could be sufficient for flexible, transparent electronics.

Moving on to a different aspect necessary for smart, solution-processed electronics, Chapter 4 presented a fully-printed RRAM memory based on filamentary switching in an Ag/ZnO/Au stack. Currently, no clear frontrunner exists in the search for printed read/write memory. The system presented here has been shown in the literature to perform well when fabricated using conventional techniques. Furthermore, solution routes exist for all the components of the stack; hence making this a promising candidate for printed electronics. Here, several device variations were presented with all-printed, all-evaporated, and hybrid printed/evaporated electrodes. In order to achieve a fully-printed cell, Au bottom electrodes had to be thermally treated to remove excess organic contaminants remaining after film annealing. The system showed good memory characteristics: good endurance over 2000 cycles, memory window of up to 10^{5}, long data retention times, good stability to voltage disturb signals, and minimum programming time of 200 ns.

“Low-temperature” cells with ZnO films processed at 200°C were demonstrated and exhibited desired bipolar switching behavior; however, these were unstable and had poor yield and memory characteristics. In order to achieve stable, well-behaved cells, a ZnO anneal of 350°C in air was necessary. This removes excess solvent, encapsulant, and other organic contaminants from the films which would otherwise prevent proper filament growth. The use of such high temperatures is clearly undesirable, as it precludes the use of low-cost plastic substrates and makes this technology less competitive. This problem may be overcome by implementing additional film processing techniques to remove these contaminants. This could be achieved by exposing the films to inert or active plasma or ultra violet ozone cleaning, both of which have been shown to remove organic contaminants. Alternatively, a different ink

formulation may be used which does not require such high processing temperatures, such as recently developed, plastic-compatible ZnO sol-gels. Unlike transistor applications, for which ZnO sol-gels are generally developed, an RRAM stack does not necessarily require large crystalline size and good grain boundary interfaces. This could allow for further decrease of standard ZnO sol-gel processing temperatures for RRAM implementation. Additionally, the high temperature heat treatment of Au electrodes may be avoided by similar cleaning techniques or alternative ink formulations. Decreasing processing temperatures or Au and ZnO films would allow incorporation of this technology into an all-printed, low-cost fabrication flow.

Clearly, quite a lot remains to be done for the field of printed electronics to become a reality. Consequently, there is ample opportunity for research and improvement. This work has presented some solution-processed components which could prove useful for all-printed, low-cost applications in the future.

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