Improving CMOS Speed and Switching Power with Air-gap Structures

Jemin Park

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2011-84
http://www.eecs.berkeley.edu/Pubs/TechRpts/2011/EECS-2011-84.html

July 21, 2011

Copyright © 2011, by the author(s).
All rights reserved.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission.

Improving CMOS Speed and Switching Power with Air-Gap Structures

By

Je Min Park

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Chenming Hu
Professor Tsu-Jae King Liu
Professor Eugene E. Haller

Fall 2011

Improving CMOS Speed and Switching Power with Air-Gap Structures

Copyright © 2011

by

Je Min Park

Abstract

Improving CMOS Speed and Switching Power with Air-Gap Structures

By

Je Min Park

Doctor of Philosophy in Engineering – Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Chenming Hu, Chair

Scaling transistors is good for speed but scaling interconnect degrades it due to resistances and parasitic capacitances. Scaling of supply voltage V_{DD} has significantly slowed down since the 130 nm node. As a result, integrated circuit (IC) power consumption has been on the rapid rise. Crosstalk noise problem has been also increased as scaling. Reducing capacitance is an excellent solution for these problems; the circuit delay, power consumption, and crosstalk noise. The future transistor and interconnect with lower capacitance should be considered to overcome these problems. An air-gap structure can be attractive solution for both transistor and interconnect. Novel air-gap structures are proposed in this research. In the transistors, the conventional spacer structure is replaced with air-gap spacer structure. This new structure leads for the fringing capacitance to be decreased much. Therefore, the speed and power consumption can be improved. This structure can be compatible with both the conventional gate-first and gate-last process. Other designs involve use of self-aligned contact or linear contact processes to achieve a much more effect. The low-k spacer transistor which is included this air-gap spacer transistor degrades the current performance. Thus, the air-gap spacer technology is very helpful to the high performance devices but it is not much helpful to the low stand-by power devices. The corner spacer transistor with high-k inner spacer and low-k outer spacer is proposed to overcome the degradation of current performance. The high-k material can improve the current performance and the low-k material can improve the capacitance. In the interconnects, the proposed novel air-gap interconnects are compatible with both the subtractive etch interconnect and dual damascene interconnect. These air-gap structures can improve not only the effective dielectric constant but also crosstalk noise problem.

To my wife for her devoted love and support,
to my daughters for their affording great pleasure to me,
and to my mother for her unbounded love and prayer.

Contents

Table of Contents ii

List of Figures vi

List of Tables x

Acknowledgements xi

Table of Contents

Chapter 1: The Needs for Vacuum Gap Structures 1

1.1 Scaling down is no longer the absolute solution for improving circuit speed 1
1.2 CMOS Power density has increased with scaling transistors 2
1.3 Crosstalk noise is also a big problem 4
1.4 A possible solution 4
1.5 Research outline 5
1.6 References 5

Chapter 2: Vacuum Spacer Transistors ……..6

2.1 Introduction 6
2.2 Historical Background 8
2.3 Process Integration 9
2.3.1 A vacuum spacer transistor with conventional contact process 9
2.3.1.1 The comparison structures with simulation ....………………………………….9
2.3.1.2 Structure and Process Concept ……………………………………………...…9

2.3.2 A vacuum spacer transistor with SAC process 11
2.3.2.1 The comparison structures with simulation 11
2.3.2.2 Structure and Process Concept 11
2.3.2.3 Self-aligned contact Technology 12
2.4 Analytical Frameworks 13
2.4.1 Gate Capacitances 13
2.4.2 NMOSFETs and PMOSFETs of simulations 15
2.4.3 Miller Effect 16
2.4.4 3D Mixed Mode Simulations 17
2.5 Simulation Results 18
2.5.1 A vacuum spacer transistor with conventional contact process simulations 18
2.5.2 A vacuum spacer transistor with SAC process simulations 21
2.6 Summary 24
2.7 References 25

Chapter 3: Vacuum Spacer Transistors with Gate Last Process 28

3.1 Introduction 28
3.2 Process Integration 29
3.2.1 Vacuum spacer transistors of high performance and low standby power devices 29
3.2.1.1 The comparison structures with simulation 29
3.2.1.2 Structure and Process Concept 31
3.2.2 A vacuum spacer transistor with gate last and SAC process 32
3.2.2.1 The comparison structures by simulation 32
3.2.2.2 Structure and Process Concept 34
3.2.3 A vacuum spacer transistor with gate last and linear contact process 35
3.3 Simulation Results 35
3.3.1 Vacuum spacer transistors of high performance and low standby power devices 35
3.3.2 A vacuum spacer transistor with gate last and SAC process 39
3.3.3 A vacuum spacer transistor with gate last and linear contact process 43
3.4 Reasonable Expectation 46
3.5 Summary 49
3.6 References 50

Chapter 4: Corner Spacer Transistor 52

4.1 Introduction 52
4.2 Historical Background 53
4.3 Process Integration 54
4.3.1 The comparison structures by simulation 54
4.3.2 Structure and Process Concept 55
4.4 Simulation Results 56
4.4.1 A corner spacer transistor in high performance devices 56
4.4.1.1 A simple corner spacer transistor with silicon nitride and oxide ……..………57
4.4.1.2 Corner spacer transistors with other materials ………..…………………....61
4.4.2 A corner spacer transistor in low stand-by power devices 65
4.4.2.1 A simple corner spacer transistor with silicon nitride and oxide ……..………65
4.4.2.2 Corner spacer transistors with other materials ………..…………………....69
4.5 Summary 72
4.6 References 72

Chapter 5: Vacuum-Gap Interconnect 74

5.1 Introduction 74
5.2 Historical Background 76
5.2.1 Vacuum gap integration in aluminum interconnect 76
5.2.2 Vacuum gap integration in copper interconnect 77
5.3 Process Integration 77
5.3.1 A subtractive etch interconnect with vacuum-sheath structure 78
5.3.1.1 The comparison structures with simulation ......……………………..………78
5.3.1.2 Structure and Process Concept ………..…………………………………....79
5.3.2 A dual damascene interconnect with vacuum-corridor structure 80
5.3.2.1 The comparison structures with simulation ......……………………..………80
5.3.2.2 Structure and Process Concept ………..…………………………………....81
5.4 Modeling for Simulation 83
5.4.1 General Modeling for Interconnect 83
5.4.2 Capacitance Definitions of RAPHAEL Default Database 84
5.5 Simulation Results 85

5.5.1 A subtractive etch interconnect with vacuum-sheath simulation 85
5.5.1.1 Simulation implementation ……………….......…………………….....………85
5.5.1.2 Simulation Results ……………………..……………………………………....87
5.5.2 A dual damascene interconnect with vacuum-corridor simulation 91
5.5.2.1 Simulation implementation ……………….......…………………….....………91
5.5.2.2 Simulation Results ……………………..……………………………………....92
5.6 Reasonable Expectation 96
5.7 Summary 98
5.8 References 99

Chapter 6: Conclusions 101

6.1 Summary of Work 101
6.2 Future Directions 102

List of Figures

1.1 Gate delay and interconnect delay with scaling transistor 1

1.2 Doping concentration and junction depth 2

1.3 The trend of V_{DS} and V_{TH} with each generation 3

1.4 The active and passive power densities 3

1.5 a The illustrated mutual capacitance 4

1.5 b Worst case interconnect delay due to crosstalk 4

2.1 The trend of vertical scaling down 7

2.2 a Vertical view of Togo's air-gap transistor 8

2.2 b Comparison of each capacitance 8

2.3 The final structures of NMOSFETs using TSUPREM4 10

2.4 The proposed process flows for a vacuum spacer transistor 10

2.5 NMOSFETs constructed with 3D simulator 11

2.6 The proposed process flow of the novel vacuum spacer transistor with SAC process 12

2.7 a The layout and vertical view of conventional contact process 13

2.7 b The layout and vertical view of SAC process 13

2.8 MOS capacitance parameters 14

2.9 Simulation Procedures 15

2.10 Gate capacitances and switching energy 16

2.11 The Miller capacitances 16

2.12 a 3D NMOSFET structure 17

2.12 b 3D PMOSFET structure 17

2.13 The schematic of 4 stages of inverter structures 17

2.14 Simulated I_{DS}-V_{GS} characteristics 18

2.15 The gate capacitances of oxide and vacuum spacers 19

2.16 The total gate charge of oxide and vacuum spacers 19

2.17 The mixed-mode simulation of inverter delay 20

2.18 a Simulated I_{DS}-V_{GS} characteristics of three types of NMOSFETs 21

2.18 b Simulated I_{DS}-V_{GS} characteristics of three types of PMOSFETs 21

2.19 a The gate capacitances of 5 different types of spacers and contacts 22

2.19 b The gate charge of 5 different types of spacers and contacts 22

2.20 The mixed-mode simulation of 5 types of inverters 22
2.21 a The layout of Intel 45nm SRAM cell 24
2.21 b The imaginary layout of SRAM cell with SAC process 24

3.1 The final structures of NMOSFETs using Sentaurus 30
3.2 A proposed process flow of the vacuum spacer transistor with gate last process 31
3.3 3D NMOSFETs with SAC process from 65nm to 20nm of gate length 32
3.4 The proposed process flow of the novel vacuum spacer transistor 33
3.5 NMOSFETs constructed with 3D simulator 34
3.6 The simulated I_{DS}-V_{GS} characteristics of NMOSFETs 36
3.7 a The 3D mixed-mode simulation results for high performance device 37
3.7 b The 3D mixed-mode simulation results for low standby power device 37
3.8 a The comparison of switching charges between oxide and vacuum spacer 38
3.8 b The comparison of switching energies between oxide and vacuum spacer 38
3.9 The simulated I_{DS}-V_{GS} characteristics of MOSFETs with different gate lengths 40
3.10 The 3D mixed-mode simulation results at 45nm gate length 41
3.11 The simulated delay time results with different gate lengths 41
3.12 The simulated switching charge results with different gate lengths 42
3.13 The simulated switching energy results with different gate lengths 42
3.14 The simulated I_{DS}-V_{GS} characteristics of the 4 types of NMOSFETs 44
3.15 The mixed-mode simulation results of the 4 stage inverter chains (Fan-out = 1) 44
3.16 Simulated inverter delay and the switching energies at three V_{DD} 45
3.17 The proposed process flow of the novel vacuum spacer transistor with gate last and raised S/D and linear contact processes 47
3.18 The proposed process flow of the novel vacuum spacer transistor with FinFET and linear contact processes 48

4.1 a Vertical view of Jaegoo's dual spacer transistor 53
4.1 b Vertical view of Jun-Wei's dual spacer transistor with metal gate process 53
4.1 c Vertical view of Chun-Jen's sidewall spacer transistor 53
4.2 The final structures of NMOSFETs using Sentaurus simulator 54
4.3 The proposed process flows for a corner spacer transistor 55
4.4 The proposed process flows for a corner spacer with vacuum outer spacer transistor 56

4.5 The simulated I_{DS}-V_{GS} characteristics of the oxide spacer transistor in high performance device 57
4.6 Simulated on and off current of all the different spacer widths and heights in high performance device 58
4.7 a Electric potential contour plot of transistor with 16nm all silicon nitride spacer 59
4.7 b Electric potential contour plot of transistor with 9nm silicon nitride spacer 59
4.7 c The electric potential at the semiconductor/dielectric interfaces of the two transistors 59
4.8 Simulated gate capacitance and CV/I of all the different spacer widths and heights in high performance device 60
4.9 The 3D mixed-mode simulation results of the different spacer widths and heights in high performance device 61
4.10 Simulated on and off current of all the different spacer materials in high performance device 62
4.11 Simulated gate capacitances of all the different spacer materials in high performance device 63
4.12 The 3D mixed-mode simulation results of the different spacer materials in high performance device 64
4.13 The simulated I_{DS}-V_{GS} characteristics of the oxide spacer transistor in low stand-by power device 66
4.14 Simulated on and off current of all the different spacer widths and heights in low stand-by power device 66
4.15 Simulated gate capacitances of all the different spacer widths and heights in low stand-by power device 67
4.16 The 3D mixed-mode simulation results of the different spacer widths and heights in low stand-by power device 68
4.17 Simulated on and off current of all the different spacer materials in low stand-by power device 69
4.18 Simulated gate capacitances of all the different spacer materials in low stand-by power device 70
4.19 The 3D mixed-mode simulation results of the different spacer materials in low stand-by power device 71

5.1a Vacuum gap integration profile using non-conformal CVD process in aluminum interconnect 76
5.1 b Vacuum gap integration profile using sacrificial material in aluminum interconnect 76
5.2 a Vacuum gap integration profile using non-conformal CVD process in copper interconnect 77
5.2 b Vacuum gap integration profile using sacrificial material in copper interconnect 77

5.3 Comparison between the suggested vacuum-gap interconnect and conventional subtractive etch interconnect structures 78

5.4 3D rendering of the proposed air-sheath interconnect structure 78

5.5 The proposed process flow of the vacuum-sheath interconnect 79

5.6 Comparison between the suggested vacuum-corridor interconnect and conventional dual damascene interconnect structures 80

5.7 3D rendering of the proposed vacuum-corridor interconnect structure 81

5.8 The proposed process flow of making the dielectric support beams 81

5.9 The proposed process flow of the dual damascene interconnect with vacuum-corridor structure 82

5.10 Interconnect parameters for accurate 3D field solver simulation 84

5.11 The represented interconnect capacitances 84

5.12 The simulation structure of vacuum sheath interconnect using RAPHAEL simulator 86

5.13 Total and mutual capacitances *vs.* different vacuum gap widths 87

5.14 Total and mutual capacitances *vs.* different metal widths 89

5.15 Total and mutual capacitances *vs.* different IMD thicknesses 90

5.16 Relative delay *vs.* different metal thicknesses 90

5.17 The simulation structure of vacuum corridor dual damascene interconnect using RAPHAEL simulator 92

5.18 Total capacitances *vs.* each metal layer 93

5.19 Total and mutual capacitances *vs.* vacuum percentages 93

5.20 Total and mutual capacitances *vs.* different metal widths 94

5.21 Total and mutual capacitances *vs.* different IMD thicknesses 95

5.22 RC delay *vs.* different metal thicknesses 96

5.23 The effective dielectric constants *vs.* beam dielectric constants and vacuum percentages 98

6.1 Vertical view of bit line and storage node contact in DRAM cell 102

6.2 Vertical view of NAND flash cell structure 103

List of Tables

2.1 The equations of six capacitances 14

2.2 The characteristics of oxide and vacuum spacers 20

2.3 The characteristics of transistors and inverters 23

3.1 ITRS specifications and simulation parameters 30

3.2 Several key parameters at each generation 33

3.3 The characteristics of transistors and inverters between oxide and vacuum spacers 39

3.4 Characteristics of transistors and inverters between conventional SAC and SAC with vacuum spacer structures 43

3.5 Comparison of four different transistors 46

5.1 ITRS 2008 specifications for interconnect and the assumptions for the simulation in aluminum interconnect 86

5.2 ITRS 2008 specifications for interconnect and the assumptions for the simulation in dual damascene copper interconnect 91

5.3 Characteristics summary of vacuum sheath interconnect 97

5.4 Characteristics summary of vacuum corridor interconnect 97

Acknowledgements

Firstly, I would like to thank my research advisor Professor Chenming Hu. His sincere and expert advice led me to find the interesting research topic and keep going to the right way of the research. His unwavering interest in my work have encouraged for me to do my Ph. D. study and research. I have become a better engineer and scholar as result of his ungrudging concern. I would also like to thank Professor Tsu-Jae King Liu for being a member of my committee and for all her advice and feedback. Professor King has been a wonderful source of help with regards to fabrication challenges in Microlab for all device group students. I would like to thank Professor Eugene E. Haller for being a member of my dissertation committee and helping to review my thesis.

I am heartily thankful to my wife, Jeong Hyun Kim for supporting and encouraging me to pursue my Ph.D. degree. Without my wife's encouragement, I would not have finished the degree. I really thank my lovely daughters, Hyein Park and Hyewon Park, for adjusting well to life in America. My mother has prayed to God for my study and health. I really appreciate it.

I would like to acknowledge SAMSUNG, one of the leading semiconductor companies in the world, for funding and supporting me.

Lastly, I would like to thank device group, one of the smartest and friendliest collaborative research groups in the world. I consider it a privilege to be a device group alumnus. I want to thank, in particular, Kanghoon Jeon and Changhwan Shin for being my closest friends. We entered the same year and have been through the worst of times and best of times in graduate school together. They have always been willing help me and more than happy to answer my questions even when I bother him too much. I would also like to thank Jaeseok Jeon, Sunghwan Kim, Pratik Patel, and Anupama Bowonder for their help to my fabrication works. I will miss playing tennis on Wednesday nights. Finally, I had a wonderful time with all my friends in this great school, University of California, Berkeley.

Chapter 1

The Needs for Vacuum Gap Structures

1.1 Scaling down is no longer the absolute solution for improving circuit speed

All the modern digital logic devices consist of two major elements: transistors and metal lines for interconnecting them. Scaling the transistor size improves the on-current and reduces the switching time and hence the logic delay. However, this scaling increases the resistance and capacitance of the metal lines, and therefore the overall interconnect delay is increased. Hence, scaling improves the logic delay but degrades the interconnection delay as shown in Figure 1.1.

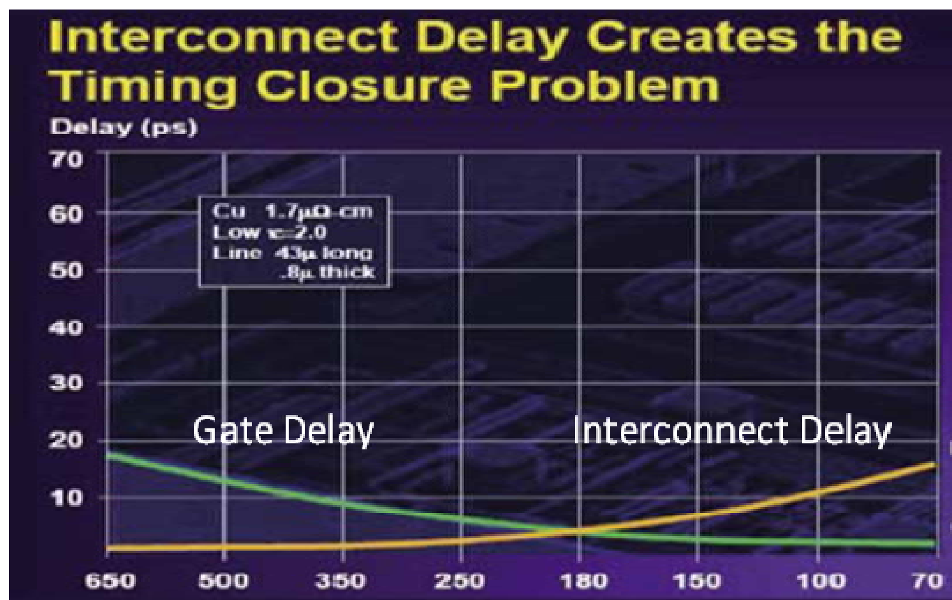


Figure 1.1: The gate delay is reduced but the interconnect delay is increased as scaling the transistor size. [1.1]

Furthermore, scaling transistors is more and more difficult. Scaling gate oxide is hard to be achieved due to gate leakage current and scaling the gate length is also hard to be demonstrated because of short channel effect (SCE). And scaling source/drain contact induces high contact resistance which drops the voltage a lot so that current is degraded. Junction depths have not scaled at previous historical trends due to inability to increase active dopant concentrations as shown in Figure 1.2. This makes SCE improvements extremely difficult and limits threshold voltage scaling. Thus, the circuit speed cannot be improved much with scaling transistors. Therefore, scaling is no longer the absolute solution for the circuit speed due to the interconnect delay and the difficulty of scaling transistors. In order to improve the circuit speed, reducing capacitance is more and more important.

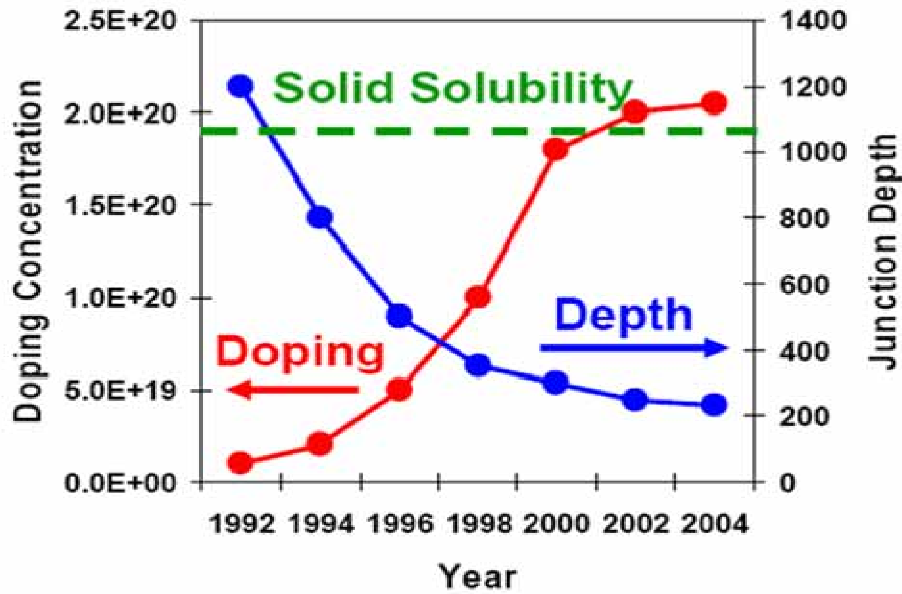


Figure 1.2: The doping concentration cannot be increased due to the solid solubility so that junction depth is hard to be reduced. [1.2]

1.2 CMOS Power density has increased with scaling transistors

Figure 1.3 shows that the trends of the power-supply voltage (V_{DD}) and the threshold voltage (V_{TH}) with each generation. In order to scale V_{DD} at the same drive current (I_{ON}), V_{TH} should be reduced as following Eq. (1.1). However, decreasing V_{TH} increases the off-current exponentially. Thus, V_{TH} cannot be scaled down aggressively as shown in Figure 1.3. From this reason, scaling V_{DD} is extremely difficult as the technology node gets small.

$$I_{ON} \propto (V_{DD} - V_{TH})^{\alpha}, \text{ where } \alpha = 1\text{-}2 \quad (1.1)$$

Reducing V_{DD} is the most effective solution of power consumption in circuit devices. However, CMOS power density has increased with transistor scaling since V_{DD} has not been scaled down in proportion to the transistor channel length. The active and passive powers are closely related by capacitance and V_{DD} which are defined as Eq. (1.2). Figure 1.4 shows that

active and passive power densities are increased by 1.3 times /generation and 3 times /generation, respectively. This power crisis will become more severe with increasing device density. Thus, reducing capacitance is a good solution to reduce power consumption.

$$P_{ACTIVE} \propto CV_{DD}^2, P_{PASSIVE} \propto V_{DD} \tag{1.2}$$

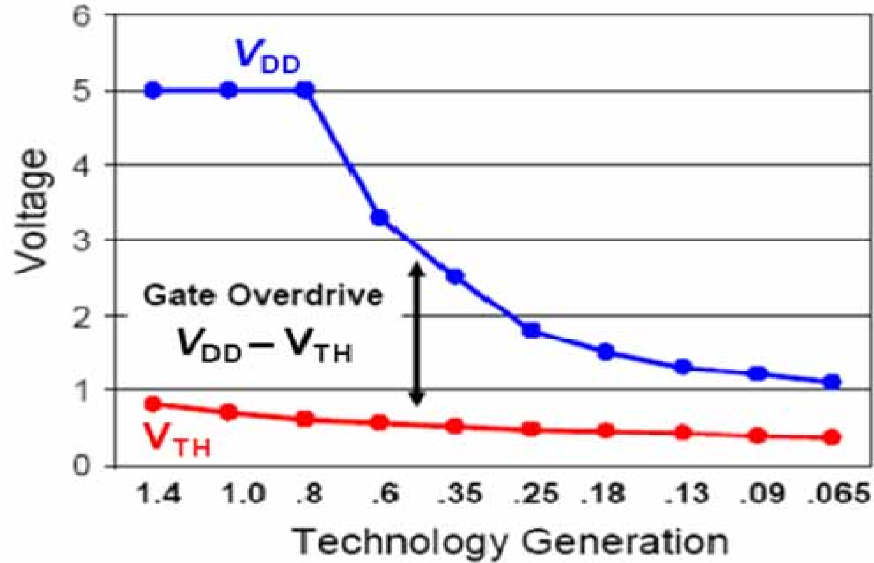


Figure 1.3: The trends of V_{DD} and V_{TH} with each generation. [1.2]

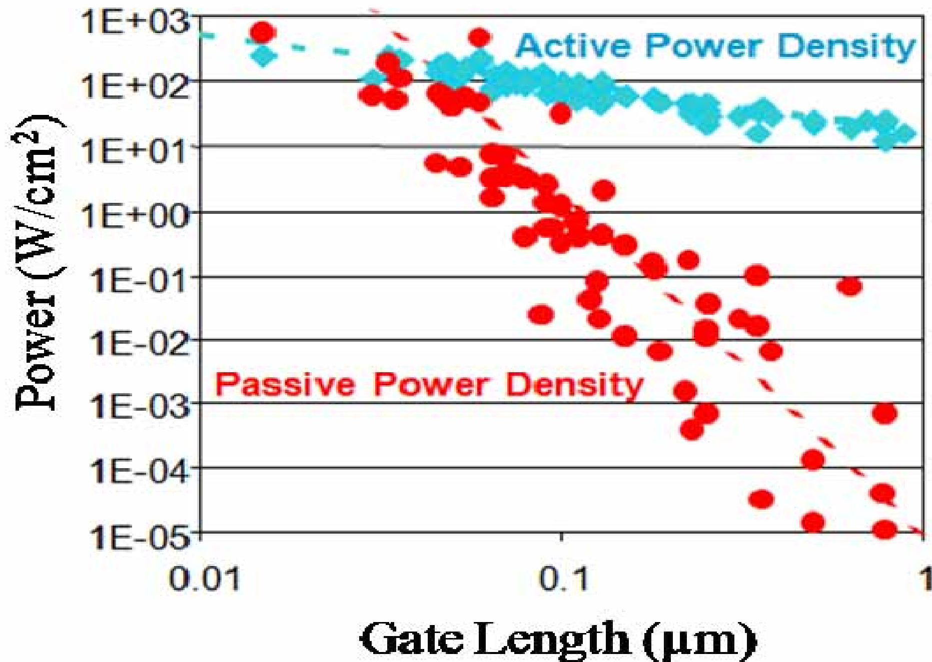
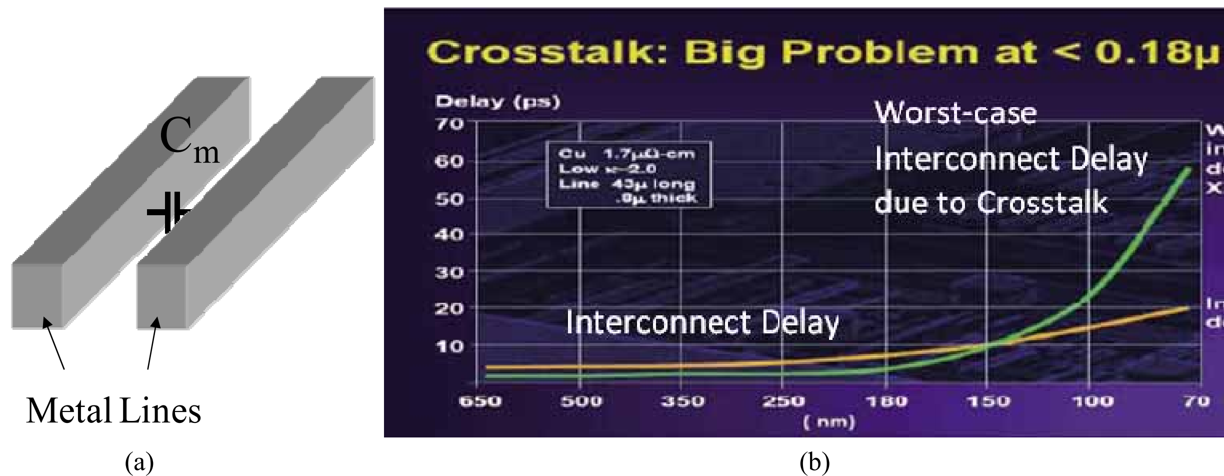


Figure 1.4: The active and passive power densities are increased as the gate length is decreased. [1.3]

1.3 Crosstalk noise is also a big problem

Crosstalk noise is defined as an undesired coupling from one circuit node to another. This noise is closely related the mutual capacitance which is the capacitance between the parallel metal lines as shown in Eq. (1.3). Figure 1.5 (a) illustrates mutual capacitance. As the technology node gets smaller, this crosstalk noise is extremely difficult to solve. James Meindl, director of the Microelectronics Research Center at the Georgia Institute of Technology, said that the tyranny of interconnects is threatening the timing, power, and cost of next-generation chips. For an example, interconnect switching energy is five times that of MOSFET switching energy at 100nm technology but the interconnect energy becomes 30 times greater at 35nm technology [1.4]. Jay McDougal said that signal integrity was really an order of magnitude worse as shown in Figure 1.5 (b) [1.5]. Therefore, crosstalk noise is also a big problem with scaling down. Reducing capacitance is also very helpful to decrease crosstalk noises.

$$\text{CROSSTALK NOISE} \propto C_{MUTUAL} \tag{1.3}$$



(a) (b)

Figure 1.5: (a) Mutual capacitance is defined by figure . (b) Crosstalk noise becomes a big problem as the technology node gets smaller. [1.1]

1.4 A possible solution

Reducing capacitance is good for speed, power, and crosstalk noise from Section 1.1, 1.2, and 1.3. A lot of research about decreasing capacitance has been studied. Finding low-k material is one option. However, most of low-k materials have porous structure so that the poor structural stability induces reliability problem.

Another option is the combination of conventional material and vacuum. Vacuum is the lowest dielectric material but it cannot be demonstrated by itself. There were lots of patents and papers about this vacuum gap structure. However, most of the research have been focused on interconnect capacitance. The fringing capacitance of transistor is increased at the small gate

length device. Therefore, the vacuum gap structure of transistor will be an attractive structure to overcome delay, power consumption, and crosstalk noise.

1.5 Research outline

The overall focus of this research is to study novel device structures for the purpose of improving complementary metal-oxide semiconductor (CMOS) speed and power consumption. The scaling of CMOS technology has been the driving force for technology advancements in the semiconductor industry over the last few decades. Speed and power are the most important parameters in scaling CMOS devices. These two parameters are closely related to each other. Increasing current is good for speed but this higher current consumes a lot of energy and power. Decreasing drain voltage (V_{DD}) leads low power consumption but it makes on-current slower and speed will be decreased. Reducing the device capacitance will be an increasingly important way to enhance the device speed and switching energy and power as the technology node is getting smaller and smaller.

The scope of this work is limited to simulation works of both transistors and interconnects. Chapter 2 reviews the general vacuum spacer transistor which is compared to the conventional spacer transistor. And self-aligned contact (SAC) process with vacuum spacer transistor is proposed for reducing capacitance as well as chip area. In Chapter 3, we propose the gate last process with vacuum gap spacer in both high performance and low stand-by power devices. The linear contact process will be used at the small feature size to overcome the contact resistance. Vacuum spacer transistor with linear contact process becomes more beneficial. In Chapter 4, corner spacer transistor is proposed. A small portion of high-k corner spacer improves the on-current and a large portion of low-k outer spacer decreases the capacitance. Chapter 5 introduces novel subtractive etch interconnect and dual damascene interconnect with vacuum gap structures. Chapter 6 summarizes all the works and shows considerable future directions.

1.6 References

[1.1] Zvi Or-Bach, “Paradigm Shift in ASIC Technology: In-Standard Metal, Out-Standard Cell”, eASIC, March 9, 2006. [online] Available:
http://camars.kaist.ac.kr/~maeng/cs310/micro04/papers/Paradigm_Shift_in_ASIC_Technology.pdf

[1.2] Paul Packan, “Device and Circuit Interactions”, International Electron Devices Meeting 2007, Short Course.

[1.3] B. Meyerson, IBM, semico Conf., Januaruy 2004, Taiwan.

[1.4] James Meindl, “Beyond Moore’s Law: The Interconnect Era”, a keynote speech at the International Symposium on Physical Design (ISPD), April 2004

[1.5] Planet Analog, June 24, 2004, “Bad signals interfere with 90-nm designs”, By Richard Goering. [online] Available:
http://www.planetanalog.com/showArticle.jhtml?articleID=19202088

Chapter 2

Vacuum Spacer Transistors

2.1 Introduction

Speed and power consumption are the most important considerations for developing new transistors. These two parameters are closely related to each other. Increasing on current and decreasing total capacitance should be extremely helpful to develop a high performance transistor. However, higher on current consumes a lot of power. Decreasing V_{DD} leads to low power consumption but it makes on current lower and speed will be decreased. Thus, designers focus on only one parameter, either speed or power. Higher on current and lower total capacitance are important in high performance technology and V_{DD} scaling and low on and off current are essential in low power technology.

Capacitance reduction is remarkably useful to both speed and power. As the technology node gets smaller, starting material, gate stack, well/channel doping profile, extension junction, and contact to source/drain (S/D) process have been changed [2.1]. Thus, capacitance has been increased sharply.

In starting material and gate stack aspects, the end of planar bulk complementary metal-oxide-semiconductor (CMOS) is becoming visible within the next several years. As a consequence, new technologies that use planar fully depleted silicon on insulator (FDSOI) devices [2.2] and dual- or multi-gate devices [2.3] [2.4] either in a planar or vertical geometry because of the robustness of short channel effect (SCE) [2.5]. The capacitance of these structures is much increased since junction/diffusion and fringing capacitances are increased [2.6]. Moreover, a new gate dielectric material having a higher dielectric constant than SiO_2 is needed due to improving device performance and reducing gate leakage current so that the capacitance is much increased [2.7].

In well/channel and extension junction doping profiles aspects, scaled devices are expected to have very shallow well/channel and extension junction doping profile [2.8] with highly

activated junctions [2.9] because of SCE. The capacitances of these scaled devices are also increased since gate channel, overlap, and junction/diffusion capacitances are increased. Furthermore, super steep retrograded body doping [2.10] and halo doping make the capacitance worse.

The contact to S/D process makes the capacitance worse. Raised S/D process due to improving resistance increases the capacitance between gate and contact is increased [2.11]. According to the general scaling theory [2.12], the height of gate stack should be reduced with scaling gate length. However, the height of gate stack is hard to be reduced due to the gate resistance problem in real fabrication. There are some gate profiles with several generations from 170nm to 45nm as shown in Figure 2.1[2.13] [2.14] [2.15] [2.16]. The gate profiles have been changed from square to high aspect ratio of rectangular. Thus, this higher aspect ratio gate profile makes the gate-to-contact capacitance worse.

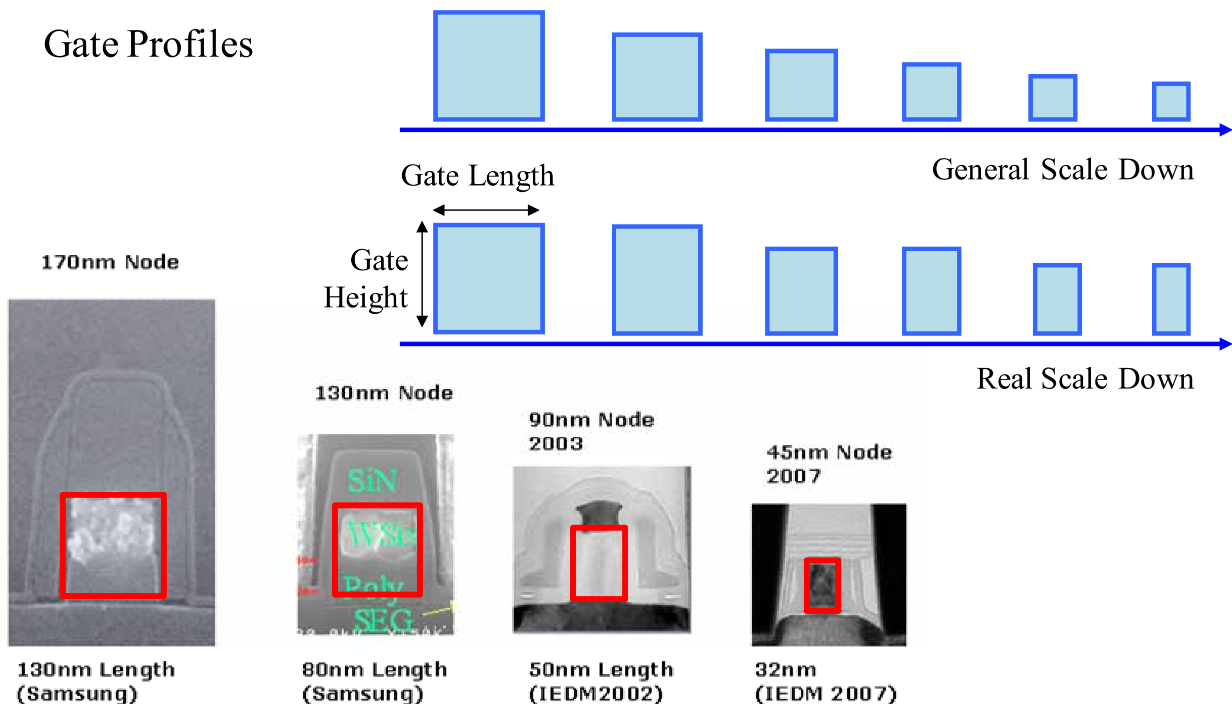


Figure 2.1: Vertical scale down of gate stack is difficult because of gate resistance problem. There is big difference between general scale down theory and real scale down in fabrication.

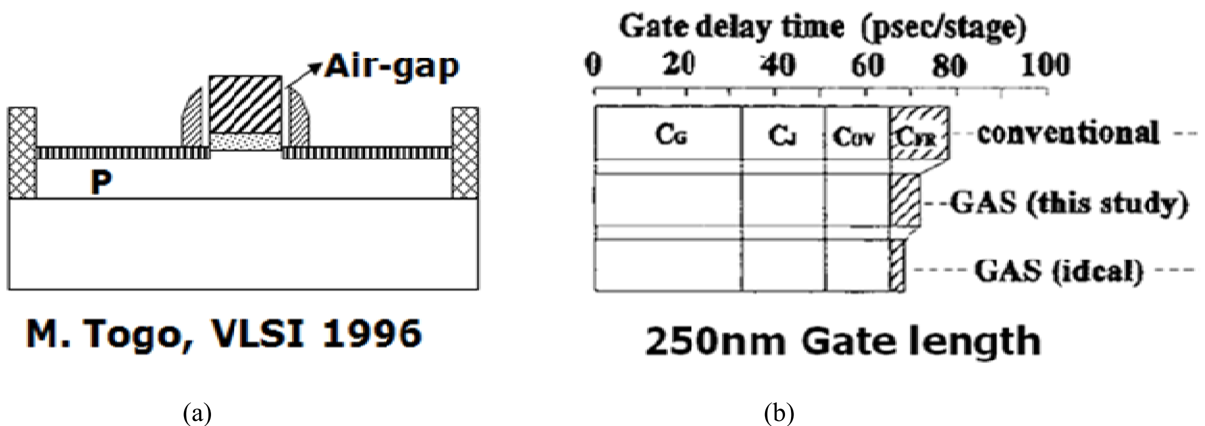
Decreasing capacitance always leads to higher speed and lower power consumption. Research on decreasing capacitance continues mostly in the field of device implementations, as it is the preferred technology for both speed and power. Capacitance consists of three factors, dielectric constant, area and distance. As we have to scale all the size, area and distance is fixed with design rule. The only changeable parameter is dielectric constant.

In order to reduce dielectric constant, low dielectric constant (k) material is used for inter layer dielectric (ILD) [2.17]. Another approach is to replace ILD with vacuum (air) gap since the associated ILD k value is very low even if only small portions of ILD are changed to vacuum gaps. Different vacuum gap integration approaches are being developed to fabricate novel MOSFETs. All approaches can be classified into one of three categories: (1) vacuum gap

replaces spacer material (2) vacuum gap is located between gate and contact (3) vacuum gap is located near contact. Each of these methods has benefits and trade-offs. Among these approaches, the technology that vacuum gap replaces gate spacer material is more useful since gate spacer materials usually have been silicon oxide (k=3.9) or silicon nitride (k=7.9). Vacuum spacer can effectively reduce the fringing capacitance and is particularly useful when combined with high-k gate dielectric.

2.2 Historical Background

An air gap technology was introduced in several papers and patents. For 0.25μm air spacer transistors, Togo reported only 6% inverter speed improvement as shown in Figure 2.2 [2.18]. In this process, he did not consider gate-to-contact capacitance because contacts were located in far away from gate. Thus, fringing capacitance portion is very small. Moreover, the air gap size is only 15nm at 250nm gate length. Even thought the improvement of air gap was very small, it effectively reduced the gate fringe capacitance without degrading electrical characteristics or reliability. Pocket implantation using air gap technology was proposed to reduce the junction capacitance compared to that of conventional pocket implantation. Yin reported an air-spacer process for raised source/drain for ultrathin-body SOI MOSFET [2.19]. The air spacer can effectively reduce the fringing capacitance and is particularly useful when combined with high-k gate dielectric. Compared to those with an oxide spacer, the speed of device with high-k dielectric gate can be improved as much as 23% using an air spacer, which is simulated by two-dimensional simulator. However, these processes of air spacer were very complicated. The reason is top sealing process is very difficult. An unconformable material should be needed. The air gap size was also smaller than what we initially designed because the initial air gap was decreased by top sealing material.



(a) (b)

Figure 2.2: (a) Vertical view of Togo's air-gap transistor. (15nm of air-gap at 250nm of gate length) (b) Comparison of each capacitance. (C_G: gate capacitance, C_J: junction capacitance, C_{OV}: overlap capacitance, C_{FR}: fringing capacitance)

At very small gate lengths, the gate-to-contact/plug capacitance becomes the dominant capacitance component in the transistor because of higher aspect ratio of gate profile and raised S/D process. This capacitance is even larger in dense memory devices because self-aligned contact (SAC) technology places the contact plug closer to the gate and the spacer material is silicon nitride having nearly twice the k of SiO_2. Giving up the SAC technology will of course improve the gate capacitance but the sacrifice in density would be unacceptable. It will be critical to reduce the gate to SAC capacitance in order to reduce the device, bit-line, and world-line capacitances for better speed and power.

Two types of vacuum spacer technologies are proposed. One is for Non-SAC and the other is for SAC processes. These two processes are very simple and do not need unconformable material. Especially, a novel vacuum spacer transistor with SAC process that does not sacrifice the SAC density reduces the gate capacitance, power, and delay to levels even lower than conventional non-SAC transistor. With this combination of density and performance, vacuum spacer transistor with SAC process could be attractive to not only Dynamic Random Access Memory (DRAM), but also Static Random Access Memory (SRAM), embedded SRAM, and perhaps even other applications.

2.3 Process Integration

We propose two different types of vacuum spacer transistor. One is a conventional gate first transistor with vacuum spacers which is used for logic devices or peripheral circuits. Usually, these transistors have silicon oxide or silicon nitride spacers. The other is a vacuum spacer transistor with SAC process which is used for high density memory devices or cell transistors. SAC process needs silicon nitride hard mask and spacers so that gate capacitance is much increased due to high k material such as silicon nitride.

2.3.1 A vacuum spacer transistor with conventional contact process

2.3.1.1 The comparison structures with simulation

Two different types of transistors with non-SAC process using a commercial process simulator [2.20] are compared as shown in Figure 2.3. Besides the vacuum spacer MOSFET, we simulated MOSFETs with silicon oxide spacer as the one of the conventional MOSFET. The vacuum spacer is only 10nm thick. Except for the spacer design, the three types of transistors have identical design parameters such as S/D and channel doping, T_{OX}, and L_{GATE}.

2.3.1.2 Structure and Process Concept

The proposed process flow for the vacuum spacer technology is illustrated in Figure 2.4. Channel implant is formed and gate oxidation is grown. Gate material and mask oxide are deposited, sequentially. Mask oxide and gate material and gate oxide are patterned. A thin oxide liner is deposited to protect the gate structure. Sidewall oxidation can be used for this thin liner.

Sacrificial gate spacer, which may be silicon nitride or porous silicon and S/D are formed in Figure 2.4 (a). Silicon nitride and porous silicon can be easily removed by hot phosphoric acid [2.21] and a dilute hydroxide solution as low as 1% [2.22]. After ILD deposition, oxide chemical mechanical polishing (CMP) is carried out until the top of the sacrificial spacer is exposed as shown in Figure 2.4 (b), (c). In Figure 2.4 (d), wet-etching has selectively removed the sacrificial spacers to create the air gaps. Because the top openings of the air gaps are smaller than the bottom of the air gaps, they can be easily sealed during non-conformal ILD2 deposition as shown in Figure 2.4 (e). The width of the vacuum pockets is easily controlled by changing the thickness of the sacrificial spacer.

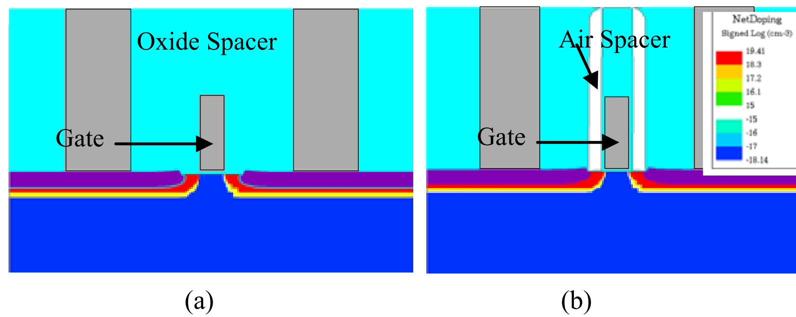


Figure 2.3: The final structures of NMOSFETs using TSUPREM4. T_{POLY} = 600Å, L_{GATE} = 20nm, contact size = 50nm, gate to contact distance = 50nm. Nitride/oxide spacer = 12nm, vacuum spacer = 10nm of air + 2nm of oxide. (a) Conventional structures with oxide spacers (c) Vacuum spacer structure

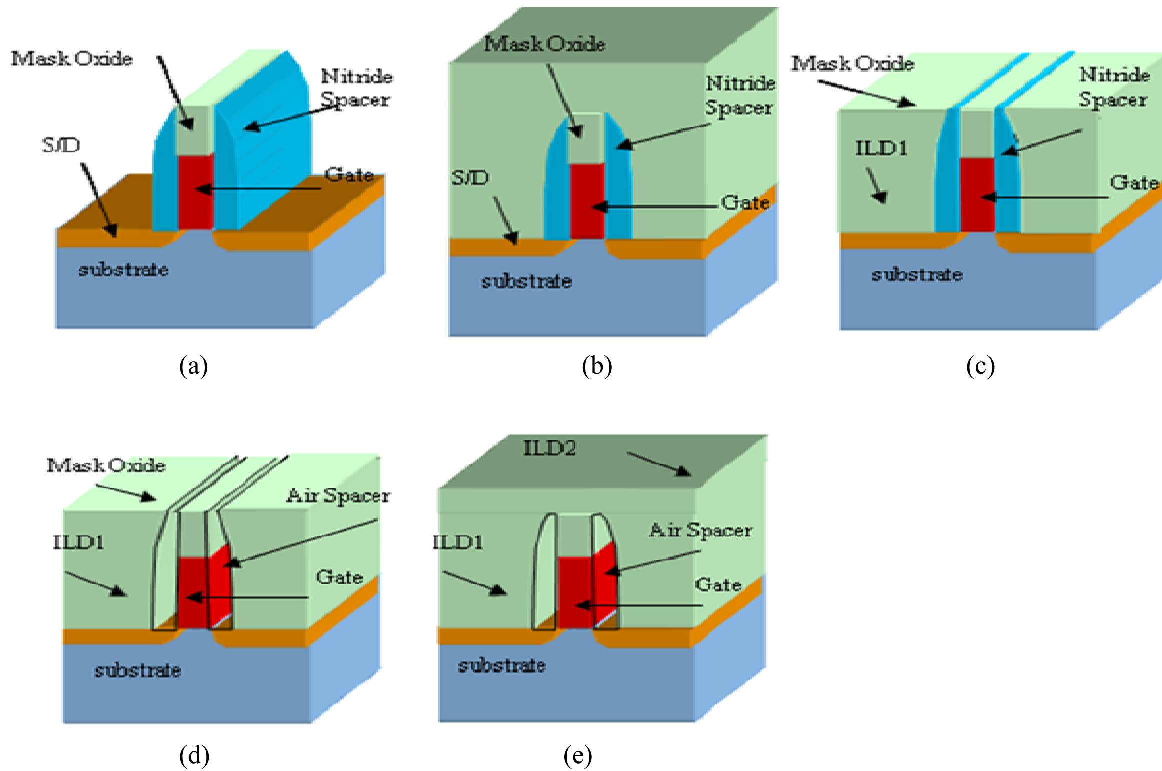


Figure 2.4: The proposed process flows for a vacuum spacer transistor with conventional contact process. (a) After source/drain formation (b) ILD deposition (c) After CMP (d) Sacrificial spacer removal (e) ILD2 deposition

2.3.2 A vacuum spacer transistor with SAC process

2.3.2.1 The comparison structures with simulation

3D Computer simulations were performed. First we constructed the transistors using 2D TSUPREM-4 [2.20]. From that, we constructed 3D structures with contacts using the Sentaurus structure editor [2.23]. We compared three devices: conventional non-SAC device in Figure 2.5 (a), conventional SAC device in Figure 2.5 (b), and the novel vacuum spacer transistor with SAC process in Figure 2.5 (c). Except for the spacer and contact, the three transistors have identical design parameters such as S/D and channel doping, T_{OX}, and L_{GATE}. In the case of the non-SAC device, the space between gate and contact is 30nm.

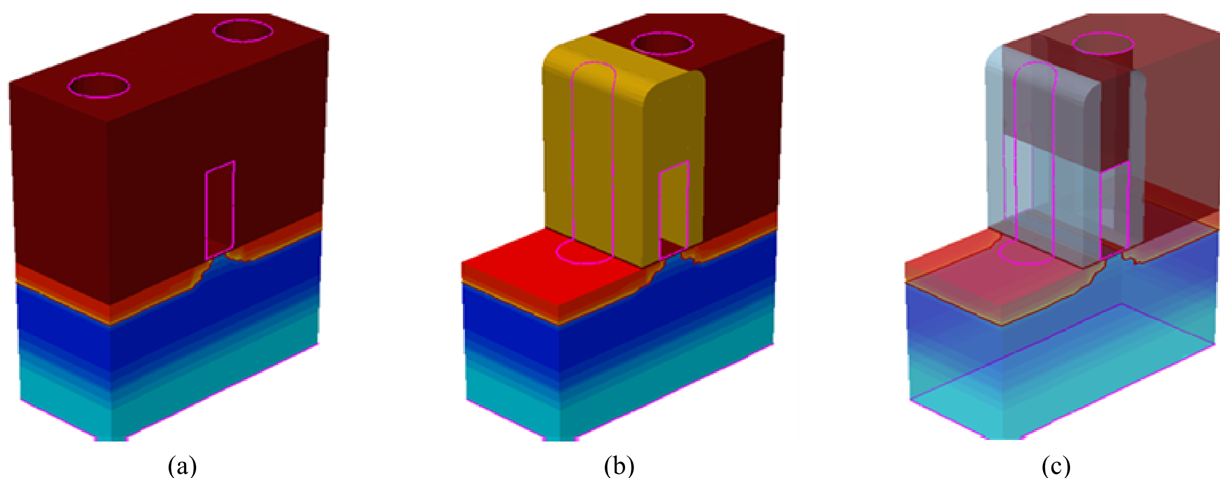


Figure 2.5: NMOSFETs constructed with 3D simulator. In (b) (c) part of ILD is removed to show the outlines of SAC. L_{GATE} = 20nm, nitride/oxide/vacuum spacer thickness = 12nm. (a) Silicon oxide spacer with conventional contact process (b) Silicon nitride spacer with SAC process (c) Vacuum spacer with SAC process

2.3.2.2 Structure and Process Concept

The proposed vacuum spacer process flow is as follows. In Figure 2.6 (a), channel implant is formed and gate oxidation is grown. Gate material, mask oxide and mask nitride are deposited, sequentially. Mask nitride, mask oxide, gate material and gate oxide are patterned. A thin oxide liner is deposited to protect the gate structure. Silicon nitride spacer and S/D are formed, ILD is deposited, and oxide CMP carried out. Figure 2.6 (b) shows that SAC has been formed by high-selectivity contact hole etch and contact plug filling. The contact plug is formed before making the vacuum spacer. Excess plug material over the surface is not shown. Figure 2.6 (c) shows the novel results of using CMP to expose the top of the mask nitride and selective etch of the nitride mask/spacer without etching the oxide to create a vacuum gap. The etch chemistry can be hot phosphoric acid. Generally, the ratio of nitride and oxide etch rates is 100:1. The contact height is 120nm. If the etch target is 200nm considering over etch, 2nm of oxide will be removed. Thus 4nm sidewall oxidation can protect the gate stack. A very thin oxide liner is deposited

underneath the nitride spacer to protect the gate dielectric from this etch step. The plug material should be resistant to the etchant, for example poly-silicon that is used in today's SAC processes, or be protected by thin etch-resistant spacer. Figure 2.6 (d) shows non-conformal ILD2 deposition has sealed the top openings and completed the making of the vacuum spacers.

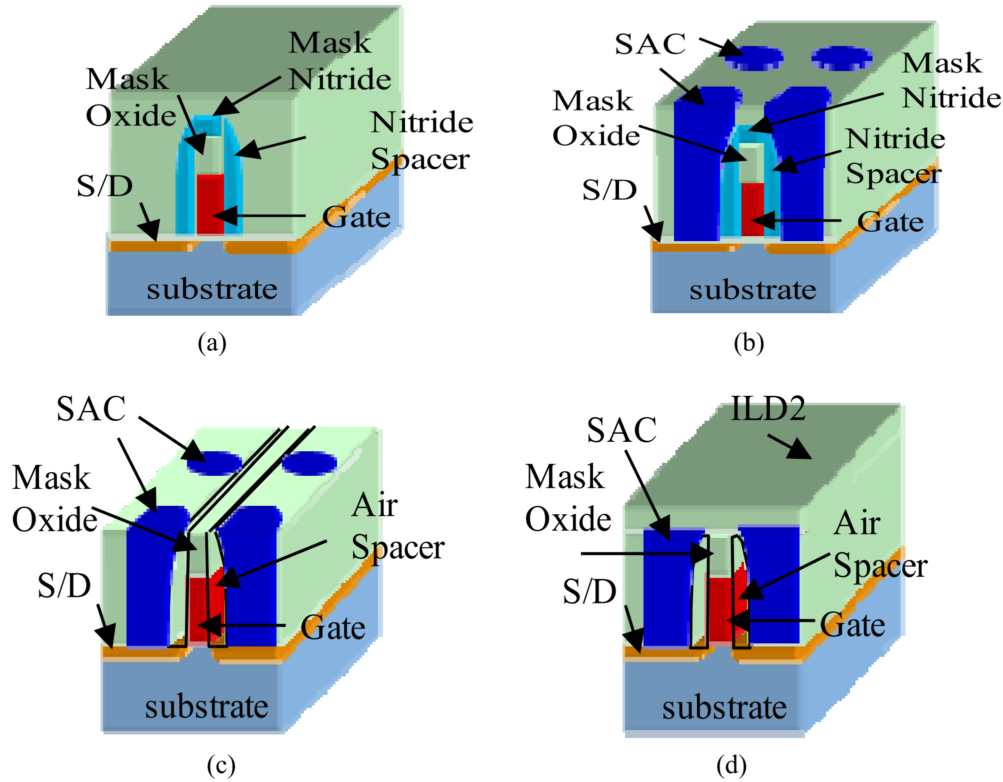
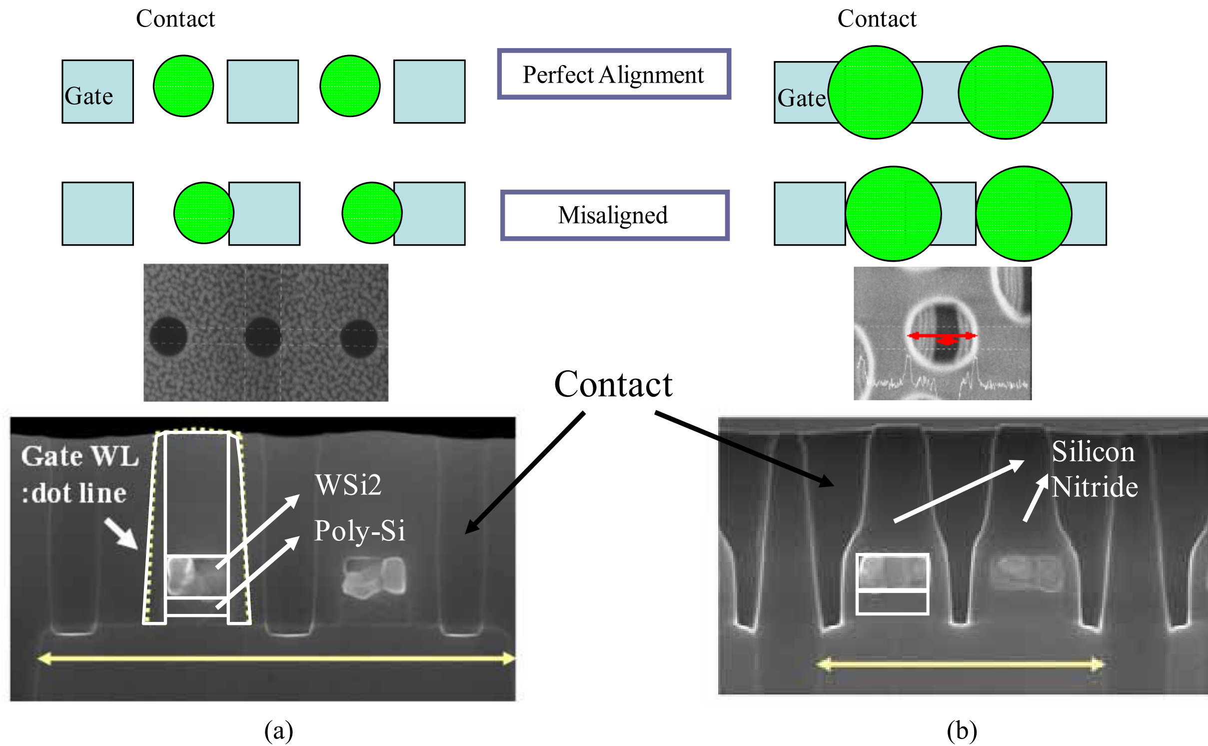


Figure 2.6: The proposed process flow of the novel vacuum spacer transistor with SAC process. (a) After ILD deposition (b) SAC and contact plug formation (c) CMP and silicon nitride removal (d) ILD2 deposition

2.3.2.3 Self-aligned contact Technology

Contact to the S/D of MOSFETs is necessary to incorporate them into functioning circuits. Contact will normally be made through an overlying layer of dielectric. If the contact holes are misaligned with respect to the gate, a short will result. The problem is depicted schematically in Figure 2.7 (a). In order to avoid this problem lithographically, we need to impose design rules keeping the contact holes at least a couple of alignment standard deviations from the gate edges; this forces the circuit layout to be bigger than strictly necessary as shown in Figure 2.7 (b). Covering the gate with an insulating layer does not help by itself, because the oxide layer will be etched away during the contact etch, but the gate is exposed before the contact etch is done so that high selectivity is needed. The silicon nitride protects the gate insulation: no contact to the gate is made despite the patterned hole overlying the gate edge [2.24]. Thus, the spacing between the gates can be decreased because the bottom area of SAC is same as the area of conventional contact technology as shown in the top view of Figure 2.7. These SAC technology cannot be

used in most devices in spite of reducing the layout size because of high capacitance due to higher dielectric k of silicon nitride which is needed for high selectivity etching process. Thus, high density memory such as DRAM uses this SAC technology. Figure 2.7 shows that silicon oxide gate mask and spacer are used in conventional contact process and silicon nitride gate mask and spacer are used in SAC process.



(a) (b)

Figure 2.7: (a) conventional contact process of layout, top view of contacts, and vertical view of contacts, respectively. (b) SAC process of layout, top view of contacts, and vertical view of contacts, respectively.

2.4 Analytical Frameworks

2.4.1 Gate Capacitances

Generally, we use capacitance model parameters with all MOSFET model statements. Model charge storage is used by fixed and nonlinear gate capacitances and junction capacitances. Gate-to-drain, gate-to-source, and gate-to-bulk overlap capacitances are represented by three fixed-capacitance parameters: CGDO, CGSO, and CGBO. The algorithm used for calculating nonlinear, voltage-dependent MOS gate capacitance depends on the value of model parameter CAPOP. In MOS capacitances, Cij determines the current transferred out of node i from a voltage change on node j. The arrows, representing direction of influence, point from node j to node i. These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance as shown in Figure 2.8. Six capacitances are reported in the operating point printout as shown in Table 2.1.

Besides these capacitances, there are other capacitances which are called fringing and gate-to-contact capacitances. As the technology node gets small, these parasitic capacitances are more and more important since these parasitic capacitances are increased up to other capacitances. It is very hard to reduce gate channel, overlap, and junction capacitances because all the parameters such as V_{DD}, I_{ON}, I_{OFF}, and T_{OX} are fixed. Thus minimizing parasitic capacitance is a key issue for realizing high-speed and low-power technologies.

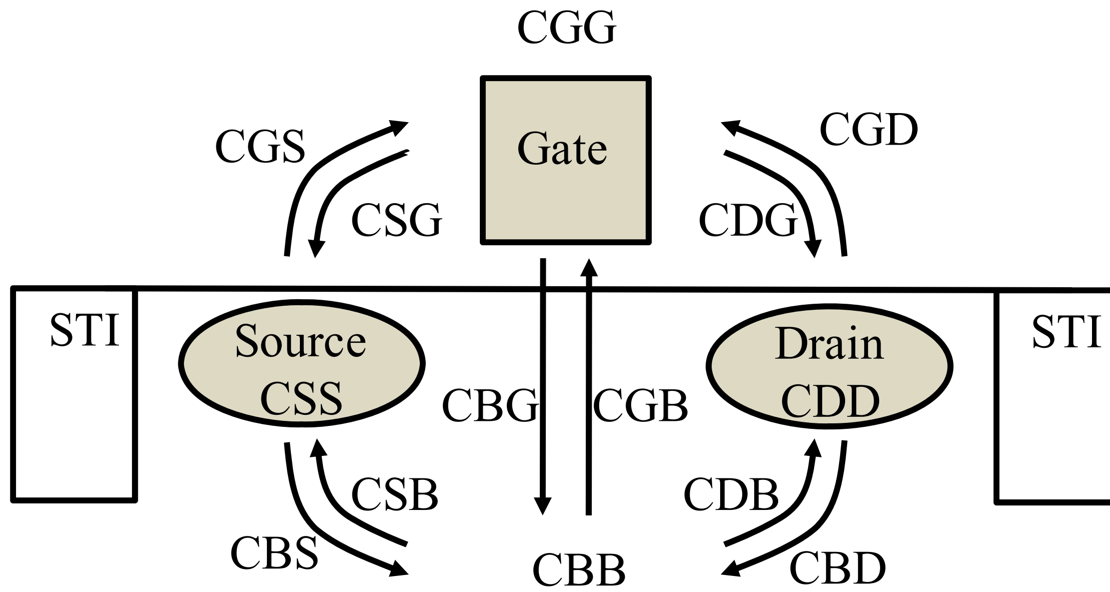


Figure 2.8: MOS capacitance parameters

Cdtot	$\frac{dQ_D}{dV_D}$	**Cgd + Cdb**		**Cbtot**	$\frac{dB}{dV_B}$	**Cgb + Csd + Cdb**
Cgtot	$\frac{dQ_G}{dV_G}$	**Cgs + Cgd + Cgb**		**Cgs**	$-\frac{dQ_G}{dV_S}$	**Cgs**
Cstot	$\frac{dQ_S}{dV_S}$	**Cgs + Csb**		**Cgd**	$-\frac{dQ_G}{dV_D}$	**Cgd**

Table 2.1: Six capacitances are represented by differential charge over voltage.

2.4.2 NMOSFETs and PMOSFETs of simulations

In order to make a 3D transistor, 2D process simulator (Tsuprem4) was used to make a 2D transistor [2.20]. After that, 2D device simulator (Medici) was used to extract I_{DS}-V_{GS} characteristics [2.25]. The parameters such as T_{OX} and L_{GATE} are followed by ITRS specifications [2.1]. Other parameters such as T_{GATE}, spacer width, the distance between gate and contact, and contact size are our options. We changed retrograded body, channel, S/D, and extension of S/D doping profiles to make the same characteristics of ITRS specification. From those, we made a 3D transistor with the same doping profiles of 2D transistor and real shape contacts using 3D structure editor (Sentaurus) [2.23]. The I_{DS}-V_{GS} characteristics of this 3D transistor are the same as those of 2D transistor. These simulation procedures are illustrated in Figure 2.9. From this 3D transistor, we extracted gate capacitance as shown in Figure 2.10. And the area below the capacitance line is gate charge which can be calculated using equation (2.1).

$$\text{Switching Charge} = \int I_{GATE} \cdot dt = \int C \cdot dV/dt \cdot dt = \int C \cdot dv \quad (2.1)$$

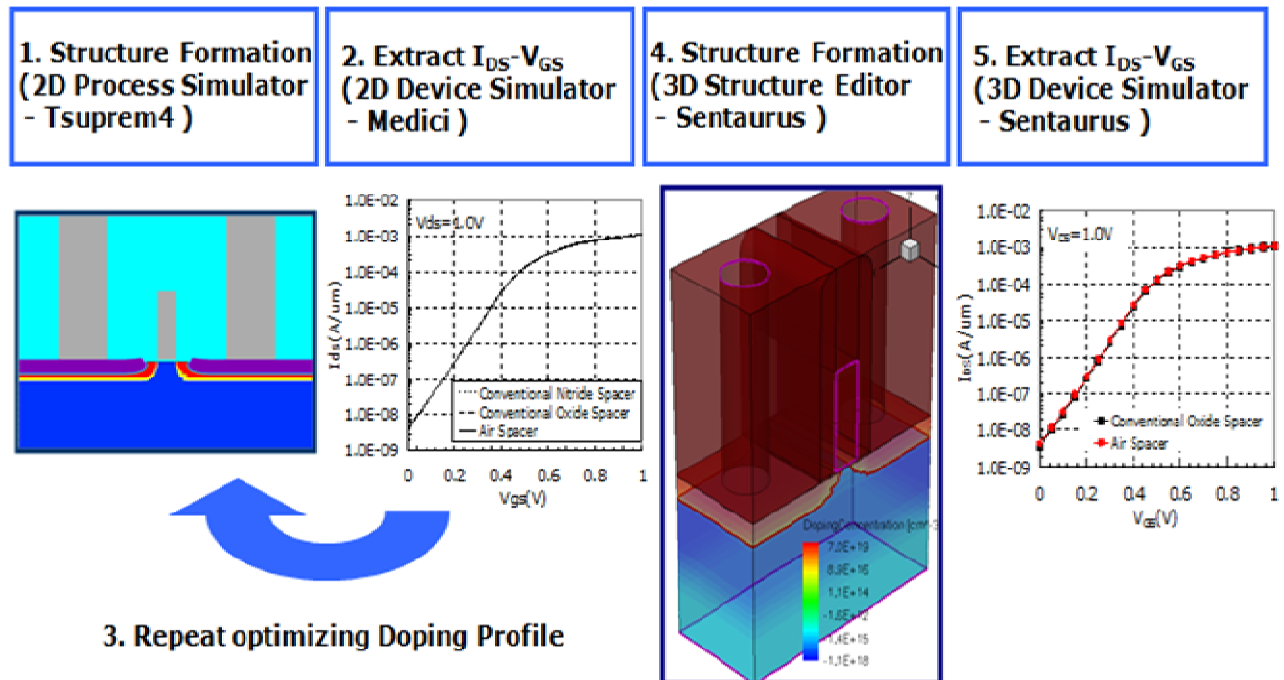


Figure 2.9: Simulation Procedures (1) Making 2D transistor using Tsuprem4 (2) Extracting I_{DS}-V_{GS} characteristics using Medici (3) Repeating (1) and (2) to optimize doping profiles (4) Making 3D transistor with contacts using Sentaurus (5) Extracting I_{DS}-V_{GS} characteristics using Sentaurus

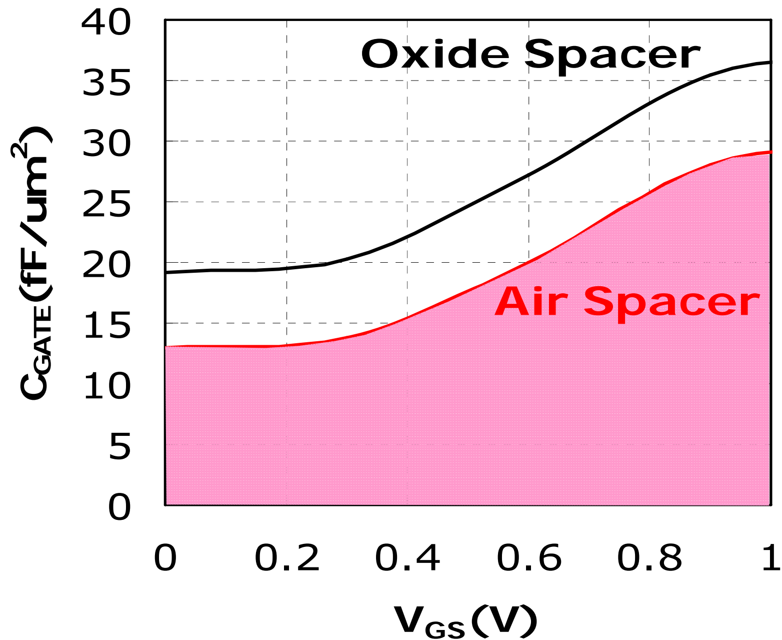


Figure 2.10: Gate capacitances are extracted. The shadow area is gate switching charge. Black and red lines are the capacitances of oxide and vacuum spacer. (V_{DS}=0V)

2.4.3 Miller Effect

A capacitor experiencing identical but opposite voltage swing at both terminals can be replaced by a capacitor to ground, whose value is two times the original value. During a low-high or high-low transition, the terminals of the gate-drain capacitor are moving in opposite direction as shown in Figure 2.11. In this study, it is very important to extract how much delay time is changed by this Miller Effect. Especially, the fringing capacitance of SAC process is bigger than that of non-SAC process. Thus, the Miller capacitance is one of the most important parasitic capacitances.

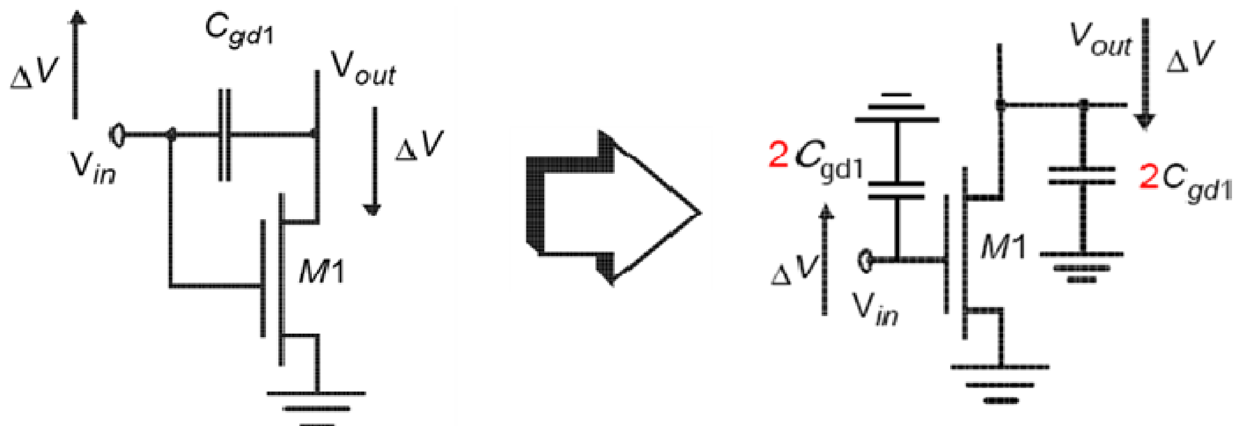


Figure 2.11: The Miller effect accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the capacitance between the input and output terminals.

2.4.4 3D Mixed Mode Simulations

In order to extract inverter delay, we made a PMOSFET which has the same geometries of the NMOSFET except the channel width which is twice of that of NMOSFET and doping types and profiles as shown in Figure 2.12. And we made 4 stages of inverters to simulate the inverter delay with considering Miller effect. Fan-out is a measure of the ability of a logic gate output, implemented electronically, to drive a number of inputs of other logic gates of the same type. The fan-out of this simulation is 1. The inverter delay is defined by the average of the pull-up and pull-down delays of the 2nd stages of inverters measured at 50% V_{DD}. Inverter switching energy can be calculated using equation (2.2). I_{DD} is the current of PMOSFET which is illustrated in Figure 2.13.

$$\text{Switching Energy} = V_{DD}\int I_{DD}\cdot dt \qquad (2.2)$$

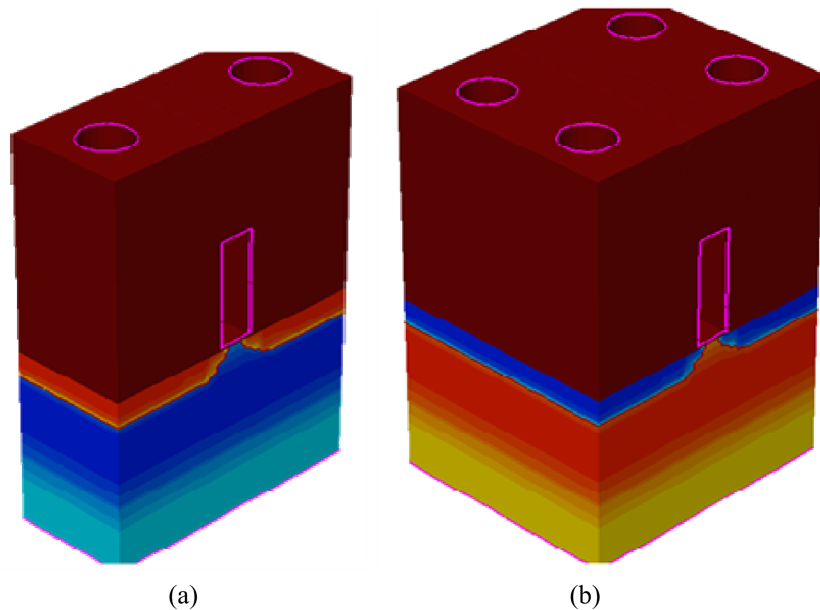


Figure 2.12: 3D structure of transistors. (a) 3D NMOSFET structure.
(b) 3D PMOSFET structure. Channel width is twice of that of NMOSFET.

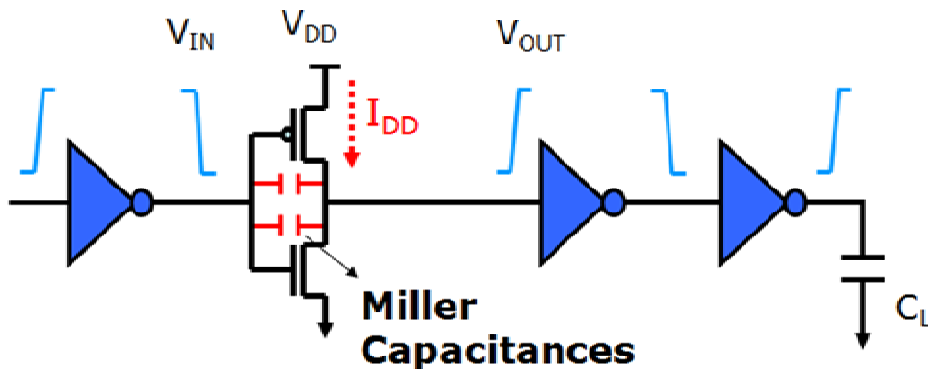


Figure 2.13: The schematic of 4 stages of inverter structures.

2.5 Simulation Results

2.5.1 A vacuum spacer transistor with conventional contact process simulations

Computer simulations with 2D TSUPREM-4 and MEDICI were performed [2.20] [2.25]. In order to suppress the short channel effect, retrograde body doping was used. The first high doping (2e18/cm3) and the second low doping (1e17/cm3) epitaxial layers are 500 Å and 210 Å respectively. The gate oxide thickness is 1.5nm. The gate poly-Si is 600 Å thick and the distance between gate and contact is 50nm. There are conventional oxide spacer transistor and novel vacuum spacer transistor. The I_{DS}-V_{GS} characteristics of the two different types of transistors are substantially the same as shown in figure 2.14.

Figure 2.15 presents the gate (input) capacitances. Two curves are shown for each transistor: V_{DS}=50mV and V_{DS}=1V. At low V_{GS}, before the channel is strongly turned on, the oxide spacer transistor has about twice the gate capacitance as the vacuum spacer transistor. This agrees well with simple estimates: the 10nm vacuum spacer in Figure 2.3 (b) roughly reduces the gate-plug capacitance by two and the gate to S/D diffusion fringing capacitance by more than two. At $V_{GS}>V_T$, we see the additional gate to channel capacitance, which is only a fraction of the gate to plug/diffusion capacitances. Gate charge, Q_{GATE}, shown in Figure 2.16 is the charge required to raise V_{GS}. It can be seen (by extrapolating the low V_{GS} line) that 77% of Q_{GATE} at V_{GS} =1V in the oxide spacer device is due to the gate to plug/diffusion capacitance. Q_{GATE} is lower in vacuum spacer transistor by 39% than oxide spacer transistor.

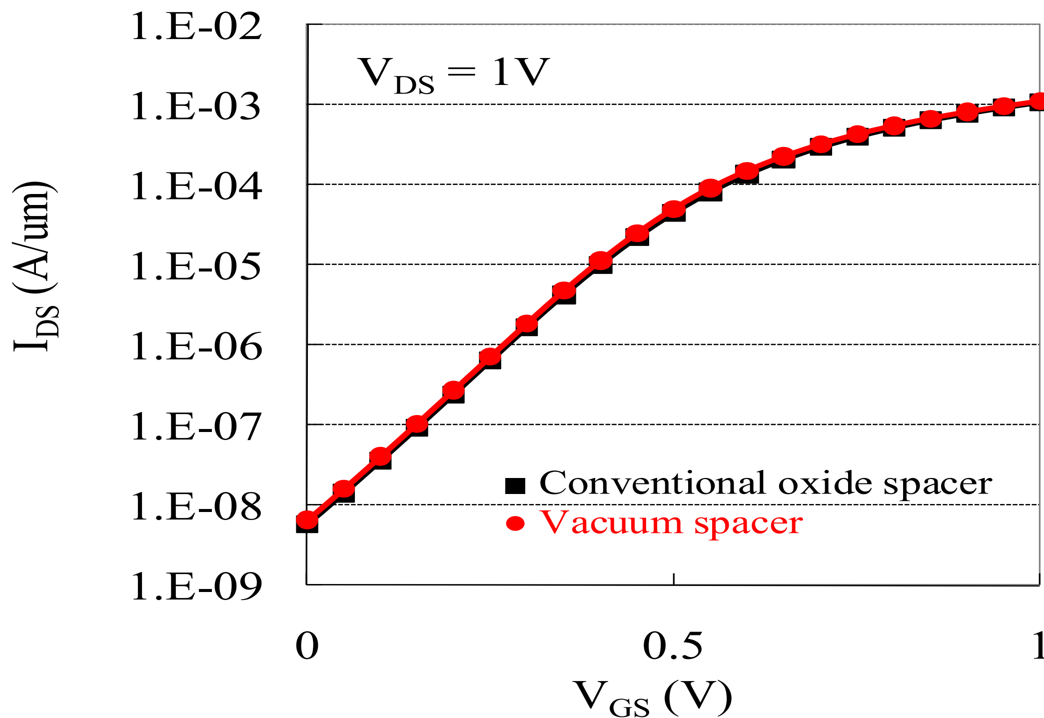


Figure 2.14: Simulated I_{DS}-V_{GS} characteristics of the three structures show identical results.

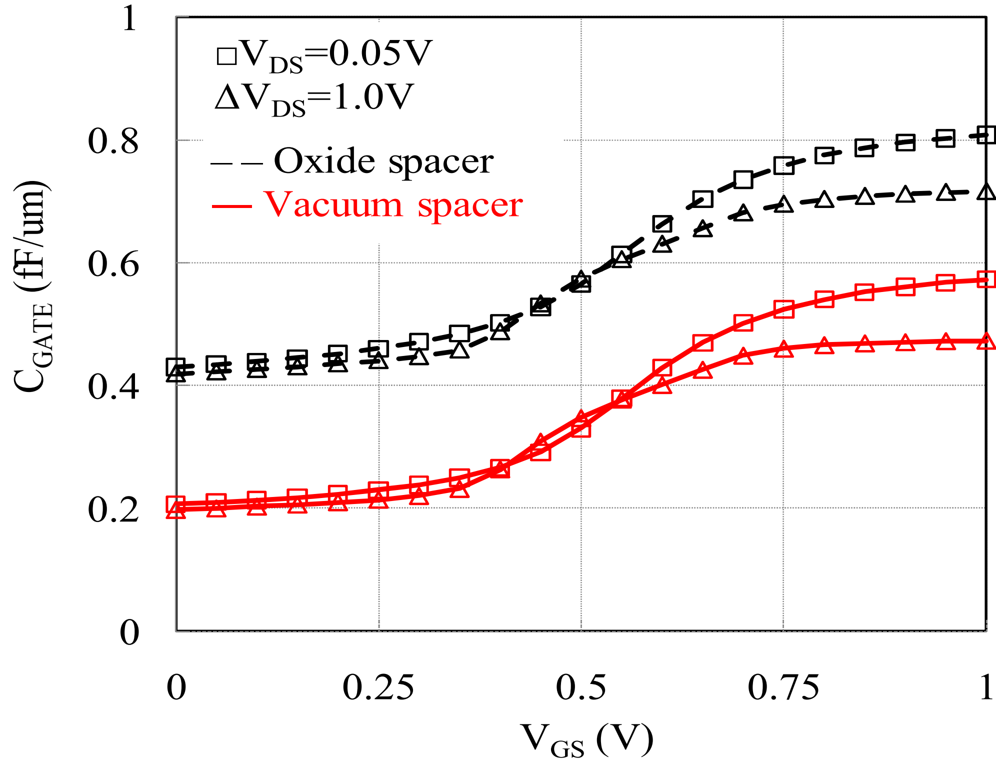


Figure 2.15: The gate capacitances are compared. Vacuum spacer shows the lower capacitance than oxide spacer.

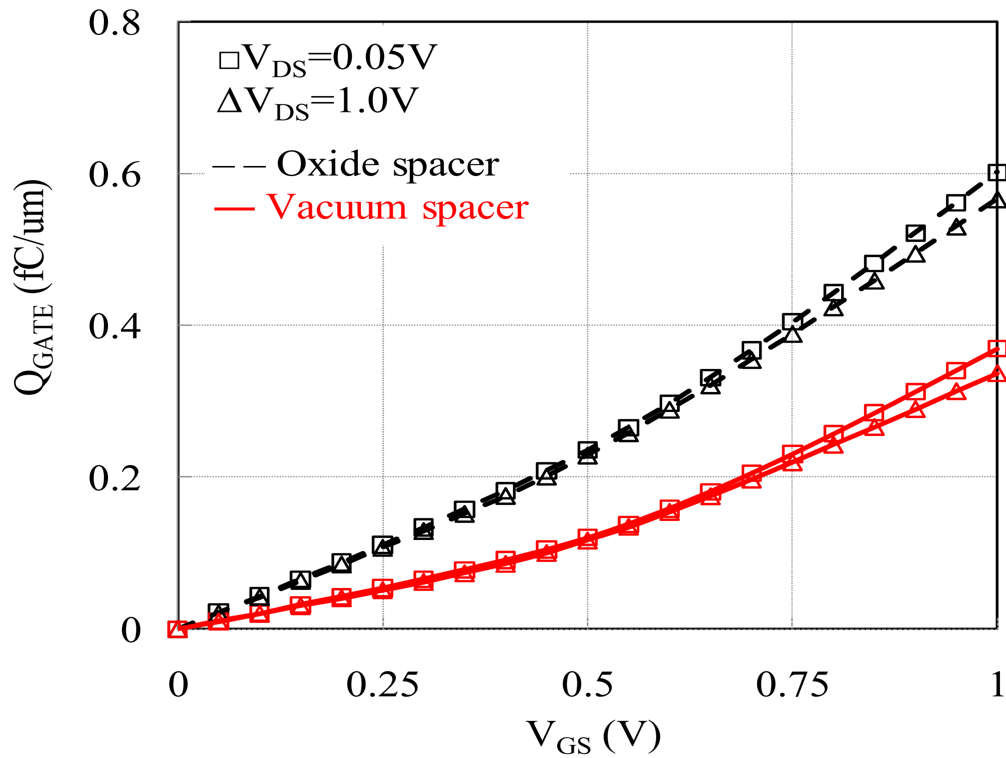


Figure 2.16: The total gate charge of vacuum spacer structure is decreased about 39% compared with oxide spacer.

The inverter in Figure 2.17 was simulated by mixed-mode simulation using MEDICI [2.25]. The inverter delay of the vacuum spacer inverter is 30% smaller than the oxide spacer inverters. This delay is calculated by the average of rising and falling time. All characteristics of transistor and inverter are shown in Table 2.2. The interesting results are shown in the last three rows of Table 2.2. Incidentally, comparing the last two rows leads to the conclusion that the junction-capacitance contribution to the switching charge/energy is 32% of the gate-capacitance contribution in the oxide spacer cases and 56% in the vacuum spacer case.

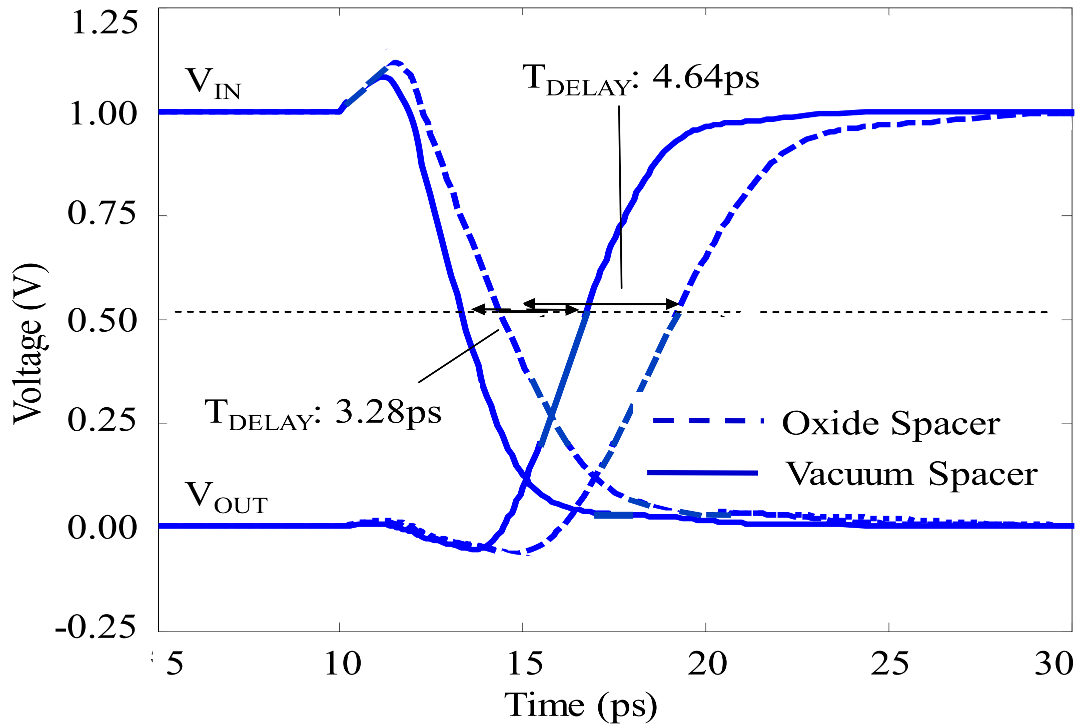


Figure 2.17: The mixed-mode simulation of inverter delay. The delay of vacuum spacer is decreased by 30% compared with that of oxide spacer.

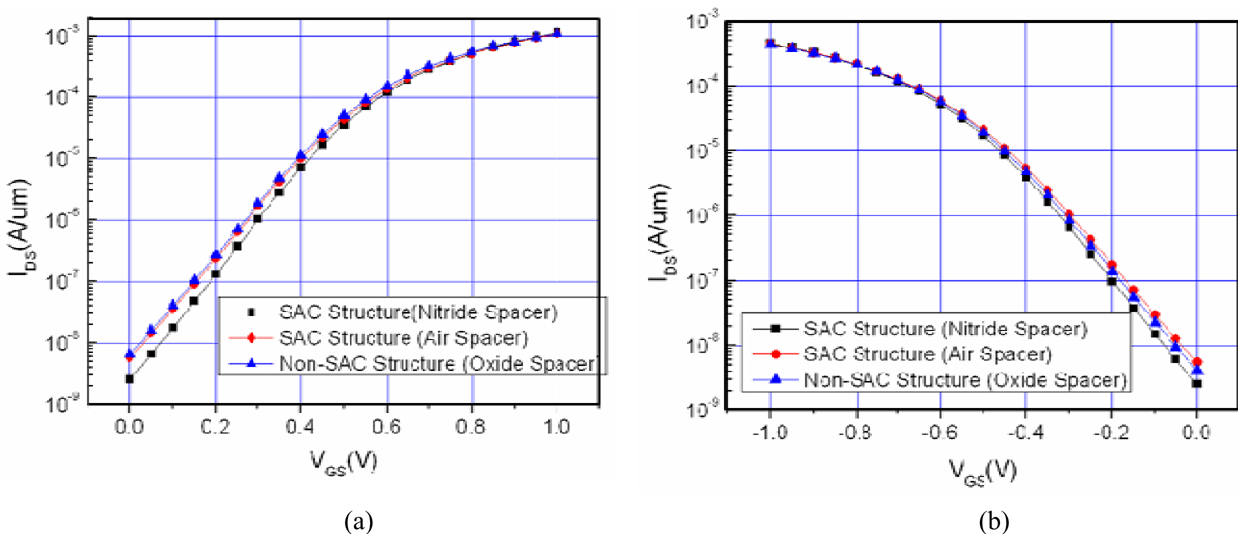
	Oxide Spacer	Vacuum Spacer
ION (mA/um)	1.06	1.06
IOFF (nA/um)	3.6	4.23
Max Q_{GATE} (Coul/um)	6.01e-16	3.69e-16
Inverter Delay (ps)	4.64	3.28
Inverter switching energy (fJ)	2.98	2.01
Gate switching charge (fC)	2.3	1.3

Table 2.2: The characteristics of oxide spacer transistors and inverters are compared with those of vacuum spacer transistors and inverters. The vacuum spacer inverter is better in speed and power.

2.5.2 A vacuum spacer transistor with SAC process simulations

The characteristics of transistors and inverters are simulated with Sentaurus 3D device simulator [2.23]. In order to suppress the short channel effect, retrograde body doping is created with a 500 Å 2e18/cm^3 doped region and a 210 Å 1e16/cm^3 doped epitaxial layer at the surface. Gate oxide thickness is 1.5nm. The gate length is 20nm and the height is 600 Å. The contact size is 30nm and the height of the contact is 121.5nm; the aspect ratio of the contact is 4. The thickness of all three types of spacer is 12nm. In the case of the non-SAC device, the spacing between gate and contact is 30nm. The three PMOSFETs are the same as the NMOSFETs except for the dopants employed in the simulations.

Figure 2.18 shows that the I_{DS}-V_{GS} characteristics of the three transistors are little changed by the spacer/contact designs. They employ the same channel and S/D dopants profiles to keep the comparison simple. The general understanding is that the higher permittivity the spacer material has, the greater control the gate fringing field has over the channel edge (hence the lower I_{OFF} is). Thus I_{OFF} (nitride spacer) is lower than that of other structures. However, even the vacuum spacer structure has a thin oxide liner (spacer) therefore I_{OFF} difference between vacuum and oxide spacer should be very small and is probably determined by the differences in automatic grid generation.

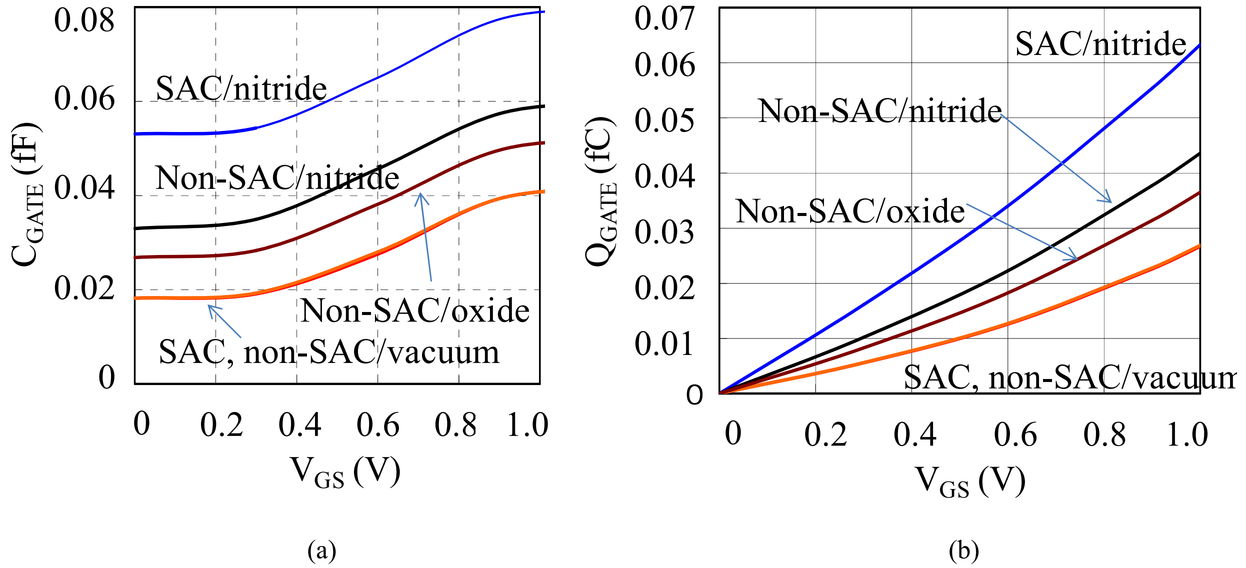


(a) (b)

Figure 2.18: Simulated I_{DS}-V_{GS} characteristics of the three types of MOSFETs are similar (V_{DS} = 1V). (a) NMOS (b) PMOS

3D simulation is quite different to 2D simulation because of real contact shape. Thus, in order to compare all devices, we made 5 transistors: non-SAC with nitride spacer, non-SAC with oxide spacer, non-SAC with vacuum spacer, SAC with nitride spacer, and SAC with vacuum spacer. Figure 2.19 presents the gate (input) capacitances and gate charge. The gate capacitance and charge of SAC process are much higher than those of other structures due to small distance between gate and contact and high k of silicon nitride material. However, if we apply vacuum spacer technology in this SAC process, the capacitance and charge can be reduced to the same level of vacuum spacer with non-SAC process. The reason of difference between Figure 2.15,

2.16 and 2.17 is the gate channel width difference. In 2D simulation, gate channel width is fixed at 1µm. However, in 3D simulation, we can change the geometries. Our devices are all 70nm gate channel width.



(a) (b)

Figure 2.19: The gate capacitances (a) and gate charge (b) are compared. Vacuum spacer with SAC process has only 46% of capacitance and 52% of charge compared to nitride spacer with SAC process.

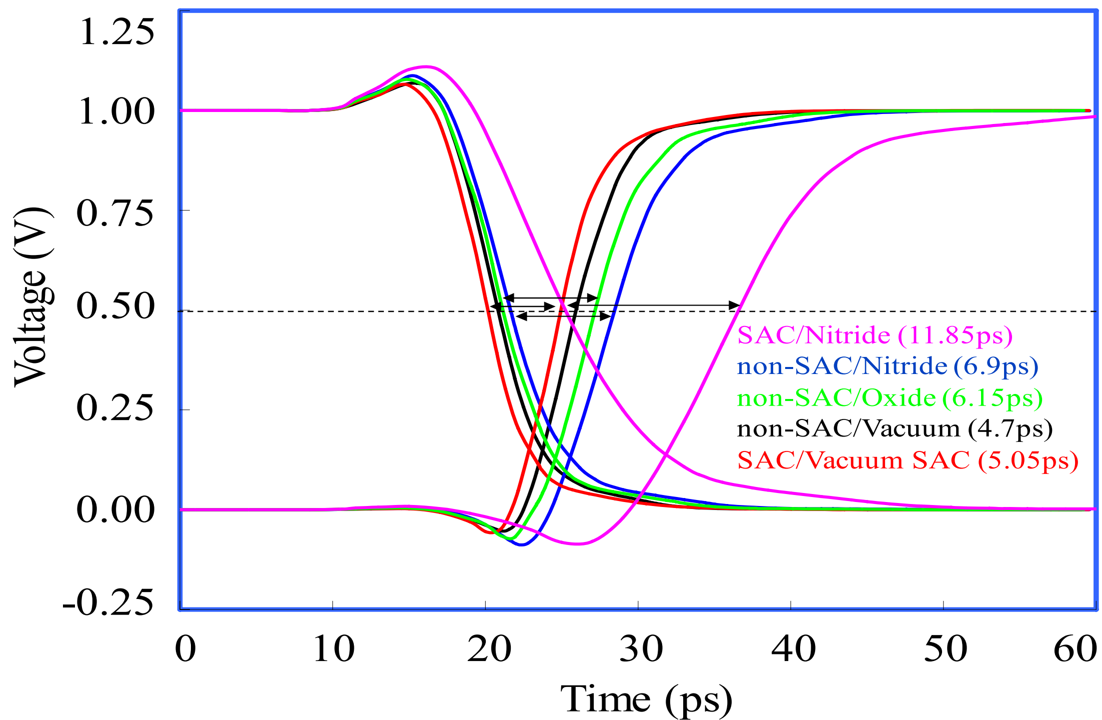


Figure 2.20: Mixed-mode simulation shows that the delay of the SAC/vacuum spacer inverter is 57% and 18% smaller than SAC/nitride spacer and non-SAC/oxide spacer inverters.

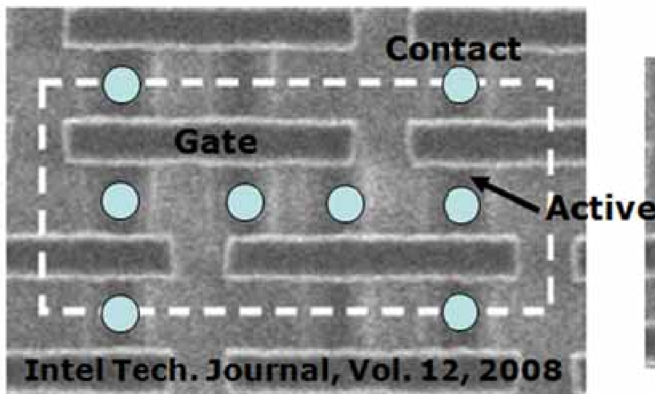
Figure 2.20 shows inverter delay that was simulated with 3D mixed–mode simulator. The NMOSFETs have 70nm channel width and the PMOSFETs, 140nm channel width. The conventional non-SAC with oxide spacer have 22% longer delay than the SAC with vacuum spacer; the conventional SAC with nitride spacer, 135%. Similar benefits were observed for SAC with vacuum spacer transistor in terms of switching energy as shown in Table 2.3. The reason of different time delay in non-SAC with oxide spacer inverter between 2D and 3D simulation is that 2D structure has line type contact thus the resistance is small. However, 3D structure has circular contact so the resistance is high.

	Non-SAC Oxide Spacer	SAC Nitride Spacer	SAC Vacuum Spacer
NMOS ION/IOFF (A/μm)	1.06e-3 / 5.55e-9	1.13e-3 / 2.56e-9	1.08e-3 / 6.14e-9
PMOS ION/IOFF (A/μm)	4.32e-4 / 4.03e-9	4.51e-4 / 2.53e-9	4.40e-4 / 5.50e-9
Inverter Delay (ps)	6.15	11.85	5.05
Delay relative to SAC with vacuum spacer	1	1.93	0.82
Switching Energy relative to non-SAC with oxide spacer	1	1.85	0.78
Area relative to non-SAC process	1	0.7	0.7

Table 2.3: Characteristics of transistors and inverters between a conventional non-SAC with oxide spacer and SAC with nitride and vacuum spacer. The SAC with vacuum spacer inverter is better in speed and power.

Figure 2.21 illustrates the density advantage of SAC devices over non-SAC devices. Generally, most memory except DRAM does not use SAC process because of higher parasitic capacitance and longer delay. However, this vacuum spacer technology has about 18% shorter delay time than non-SAC with oxide spacer technology. This is a huge advantage in future memory. If SRAM or other memory devices use this SAC with vacuum spacer, the area can be reduced about 35%, furthermore the delay time is shorter. Figure 2.21 (a) shows that Intel 45nm SRAM cell layout. If design rule is F, cell width and height are 10F and 5F, respectively, so that the cell area is $50F^2$. Figure 2.21 (b) shows the imaginary SRAM cell layout with SAC process. Cell width and height are 10F and 3.5F, respectively, at the same design rule F. The cell area of this imaginary cell layout is $35F^2$.

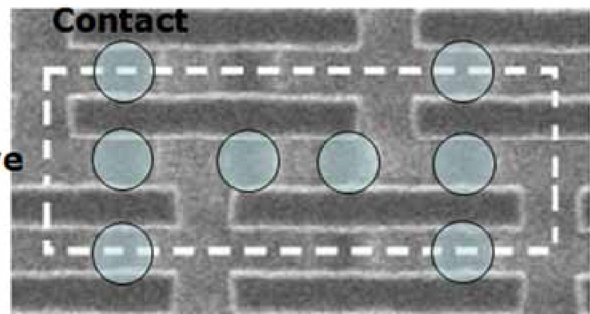
Intel 45nm SRAM Cell



Design Rule : F
Cell Width : 10F
Cell Height : 5F
Cell Area : $50F^2$

(a)

Imaginary Design using SAC



Design Rule : F
Cell Width : 10F
Cell Height : 3.5F
Cell Area : $35F^2$

(b)

Figure 2.21: Area comparison of non-SAC and SAC MOSFET and SRAM. (a) The layout of Intel 45nm SRAM cell. (b) The imaginary layout of SRAM cell with SAC process.

2.6 Summary

In a 20nm-gate MOSFET with oxide spacer, 77% of the gate charge is due to the gate to plug/diffusion capacitances. Reducing these capacitances will be an increasingly important way to improve the device speed and switching energy/power at 20nm and beyond. Unlike the enhancement of I_{ON}, reduction of capacitance can reduce the transistor switching energy significantly in addition to the delay. Compared to a vacuum spacer inverter, a conventional pure-oxide-spacer inverter has 41% longer delay and 48% larger switching energy (power consumption) than the vacuum spacer inverter. These benefits of the vacuum spacer technology are very significant and can justify the cost of the additional mask-less steps of removing the sacrificial spacers and sealing the vacuum spacer top openings during ILD deposition.

High density memories employ the SAC technology that requires the use of nitride spacers. This significantly raises the gate to plug/diffusion capacitance and increases the delay and switching energy by about 93% and 85%. A novel SAC with vacuum spacer device can preserve the 35% area benefit of SAC device while reducing the delay and power by about 18% and 22% respectively, to levels even better than the non-SAC conventional device. It also reduces the bit-line and word-line capacitances. The result is increased DRAM and SRAM speed, reduced power, and reduced chip size.

Furthermore, the delay of vacuum spacer will be much decreased compared the delay of reference oxide spacer at the same gate length as the design rule is decreased. Thus, this vacuum spacer technology is promising key technology for 20nm generation and beyond.

2.7 References

[2.1] International Technology Roadmap for Semiconductors for Interconnect, 2007

[2.2] Z. Krivokapic, W. Maszara, F. Arasnia, E. Paton, Y. Kim, L. Washington, E. Zhao, J. Chan, J. Zhang, A.Marathe, and M.R. Lin, "High performance 25 nm FDSOI devices with extremely thin silicon channel", VLSI Symposium, pp.131-132, June 2003

[2.3] S. Venkatesan, G.W. Neudeck, and R.F. Pierret, "Dual-gate operation and volume inversion in n-channel SOI MOSFET's", Electron Device Letters, Volume 13, Issue 1, pp.44-46, January 1992

[2.4] F. McGrath, C. Varmazis, C. Kermarrec, and R. Pratt, "Novel high performance SPDT power switches using multi-gate FET's", Microwave Symposium Digest, pp.839-842, June 1991

[2.5] K.K. Young, "Short-channel effect in fully depleted SOI MOSFETs", Transactions on Electron Devices, Volume 36, Issue 2, pp.399-402, February 1989

[2.6] Ge Lixin, F. Gamiz, G.O. Workman, and S. Veeraraghavan, " On the gate capacitance limits of nanoscale DG and FD SOI MOSFETs", Transaction on Electron Devices, Volume 53, Issue 4, pp.753-758, April 2006

[2.7] E.P. Gusev, D.A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P.C. Jamison, D.A. Neumayer, M. Copel, M.A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L.-A. Ragnarsson, P. Ronsheim, K. Rim, R.J. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin high-K gate stacks for advanced CMOS devices", IEDM Technical Digest, pp.20.1.1-20.1.4, December 2001

[2.8] S. B. Felch, Z. Fang, B. -W. Koo, R. B. Liebert, S. R. Walther and D. Hacker, "Plasma doping for the fabrication of ultra-shallow junctions", Surface and Coatings Technology, Volume 156, Issues 1-3, pp.229-236, July 2002

[2.9] Seong-Dong Kim, Cheol-Min Park, and J.C.S. Woo, "Advanced source/drain engineering for box-shaped ultrashallow junction formation using laser annealing and pre-amorphization implantation in sub-100-nm SOI", Transaction on Electron Devices, Volume 49, Issue 10, pp.1748-1754, October 2002

[2.10] Sun-Jay Chang, Chun-Yen Chang, Coming Chen, Tien-Sheng Chao, Yao-Jen Lee, and Tiao-Yuan Huang, "high-performance and high-reliability 80-nm gate-length DTMOS with indium super steep retrograde channel", Transaction on Electron Devices, Volume 47, Issue 12, pp.2379-2384, December 2000

[2.11] L. Chang, Yang-kyu Choi, D. Ha, P. Ranade, Shiying Xiong, J. Bokor, Chenming Hu, and T.J. King, "Extremely scaled silicon nano-CMOS devices", Proceedingd of the IEEE, Volume 91, Issue 11, pp.1860-1873, November 2003

[2.12] G. Baccarani, M.R. Wordeman, R.H. Dennard, "Generalized scaling theory and its application to a ¼ micrometer MOSFET design", Transaction on Electron Devices, Volume 31, Issue 4, pp.452-462, April 1984

[2.13] Daewon Ha, Dongwon Shin, Gwan-Hyeob Koh, Jaegu Lee, Sanghyun Lee, Yong-Seok Ahn, Hongsik Jeong, Taeyoung Chung, and Kinam Kim, “A cost effective embedded DRAM integration for high density memory and high performance logic using 0.15um technology node and beyond”, Transactions on Electron Devices, Volume 47, Issue 7, pp.1499-1506, July 2000

[2.14] Hong Kyu Hwang, Y.S. Hwang, D.S. Hwang, J.M. Park, M.H. Jo, D.H. Kim, N.J. Kang, J.Y. Kim, M.Y. Jeong, S.E. Kim, B.J. Park, Y.M. Choi, I.B. Chung, D.I. Kim, J.W. Lee, H.J. Kim, H.S. Kim, Y.J. Park, and Kinam Kim, “A Novel Bit Line Contact Process using Co-Silicide on SEG for 70nm and beyond”, Journal of the Korean Physics Society, Volume 44, Number 1, January 2004

[2.15] S. Thompson, N. Anand, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, J. Bielefeld, R. Bigwood, J. Brandenburg, M. Buehler, S. Cea, V. Chikarmane, C. Choi, R. Frankovic, T. Ghani, G. Glass, W. Han, T. Hoffmann, M. Hussein, P. Jacob, A. Jain, C. Jan, S. Joshi, C. Kenyon, J. Klaus, S. Klopcic, J. Luce, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, P. Nguyen, H. Pearson, T. Sandford, R. Schweinfurth, R. Shaheed, S. Sivakumar, M. Taylor, B. Tufts, C. Wallace, P. Wang, C. Weber, and M. Bohr, “A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 μm2 SRAM cell”, International Electron Devices Meeting (IEDM), pp.61-64, December 2002

[2.16] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. Mclntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging”, International Electron Devices Meeting (IEDM), pp.247-250, December 2007

[2.17] Y. Taur, C.H. Wann, and D.J. Frank, “25 nm CMOS design considerations”, International Electron Devices Meeting (IEDM), pp.789-792, December 1998

[2.18] M. Togo, A. Tanabe, A. Furukawa, K. Tokunaga, and T. Hashimoto, “A gate-side air-gap structure (GAS) to reduce the parasitic capacitance in MOSFETs”, Symposium on VLSI Technology Digest, pp.38-39, June 1996

[2.19] Yin Chunshan, P.C.H. Chan, and M. Chan, “An Air Spacer Technology for Improving Short-Channel Immunity of MOSFETs With Raised Source/Drain and High-k Gate Dielectric”, Electron Device Letter, Volume 26, No 5, pp.323-325, May 2005

[2.20] TSUPREM4 User Manual, Synopsys, Mountain View, CA

[2.21] W. van Gelder and V. E. Hauser, “The Etching of Silicon Nitride in Phosphoric Acid with Silicon Dioxide as a Mask”, Journal of the Electrochemical Society, Volume 114, Issue 8, pp. 869-872, 1967

[2.22] T.E. Bell, P.T.J. Gennissen, D. DeMunter and M. Kuhl, “Porous silicon as a sacrificial material”, Journal of Micromechanics and Microengineering, Volume 6, Issue 4, pp.361-369, 1996

[2.23] SENTAURUS User Manual, Synopsys, Mountain View, CA

[2.24] J. Kim, C.W. Chu, C.J. Kang, W.S. Han, and J.T. Moon, "Exposed area ratio dependent etching in a submicron self-aligned contact etching", Journal of Vacuum Science, Volume 20, Issue 5, pp.2065-2070, September 2002

[2.25] MEDICI User Manual, Synopsys, Mountain View, CA

.

Chapter 3

Vacuum Spacer Transistors with Gate Last Process

3.1 Introduction

Speed and power are more and more important parameters as the technology node is getting smaller and smaller. Reducing capacitance is remarkably useful for these two aspects. So lots of vacuum gap technologies were introduced in several papers and patents. Togo reported 6% inverter speed improvement at 0.25um gate length [3.1]. Jemin reported 30% inverter speed and 33% switching energy improvements at 20nm gate length [3.2]. The on current of vacuum spacer transistor is slightly decreased compared to the oxide spacer or silicon nitride spacer transistors. The general understanding is that the higher permittivity the spacer material has, the greater control the gate fringing field has over the channel edge (hence the higher I_{ON} is) [3.2]. It is very difficult to meet the specifications both high on-current and low off-current. Thus, ITRS reported to several directions which are high performance, low standby power, and low operating power technologies [3.3].

Metal gate and high dielectric constant (high-k) gate insulator will allow MOSFET gate length scaling to very small sizes. However, metal-gate/ high-k stack is easily degraded by high temperature processes such as the S/D activation annealing. The gate last process is attractive in this regards and has been put into production [3.4] [3.5]. Even without using metal-gate and/or high-k dielectric, the gate-last technology provides scaling benefits. In dense memory technologies, SAC is widely used for cell size reduction. However, SAC technology places the contact plug closer to the gate and the spacer material is silicon nitride having a large dielectric constant. The gate to contact-plug capacitance can be the largest contributor to the bit-line and word-line capacitances in scaled technologies with serious consequences to speed and power. It will be critical to reduce the gate to SAC capacitance. Using the gate-first process technology, a SAC with nitride spacer MOSFET has 134% longer delay and 138% higher switching energy than a SAC with vacuum spacer MOSFET [3.6].

As the transistor size gets smaller, the contact resistance becomes a serious problem due to small contact area. In order to reduce the contact resistance, line-shaped contacts (linear contacts) have been introduced to replace the long popular circular contacts. Intel reported that the linear contact technology lowered the contact resistance by >50% [3.7]. However, linear contact technology increases the gate-to-contact capacitance relative to the conventional circular contact technology. At 20nm gate length, there is more gate capacitance from the gate to contact (contact-plug and source/drain diffusion) than to body and channel [3.2]. At very small gate lengths, the gate-to-contact capacitance becomes a critical factor in device optimization.

Vacuum spacer technologies can be applied to these technologies: high performance devices, low standby power devices, gate last process, SAC process, and linear contact process. Firstly, a vacuum spacer transistor is compared with a conventional oxide spacer transistor in both high performance and low standby power technologies. Secondly, we propose a novel vacuum spacer gate last transistor that does not sacrifice the SAC density and reduces the gate capacitance, power, and delay to levels much lower than with the conventional SAC transistor with nitride spacers. With this combination of density and performance, vacuum spacer SAC transistor could be attractive to not only DRAM, but also SRAM, embedded SRAM, and perhaps even other applications. And finally, four different transistor structures, oxide spacer transistors with circular contact and linear contact and vacuum spacer transistors with circular and linear contact, are compared.

3.2 Process Integration

3.2.1 Vacuum spacer transistors of high performance and low standby power devices

3.2.1.1 The comparison structures with simulation

In order to meet the ITRS specifications, we use super steep retrograde body doping profile and mobility increasing technology. All the geometries of the transistors are followed by ITRS 2009 specifications [3.3]. Table 3.1 shows that 16nm gate length high performance device and 22nm gate length low standby power device. The gate height, spacer thickness, contact size, and the distance between gate and contact are fixed for this simulation in Table 3.1.

3D computer simulation was used to build these transistors [3.9]. Figure 3.1 (a) shows that the simulation structures of high performance NMOSFETs with 16nm gate length and figure 3.1 (b) shows that the structures of low standby power NMOSFETs with 22nm gate length. The PMOSFETs have the same structures as the NMOSFETs except for the dopants.

	High performance	Low standby power
Gate length	16nm	22nm
VDD	0.78V	0.95V
GOX	0.5nm	1.0nm
Gate height	54nm	60nm
Spacer thickness	14nm	18nm
Contact size	24nm	30nm
The distance between gate and contact	20nm	24nm

Table 3.1: ITRS specifications and simulation parameters for high performance and low standby power devices.

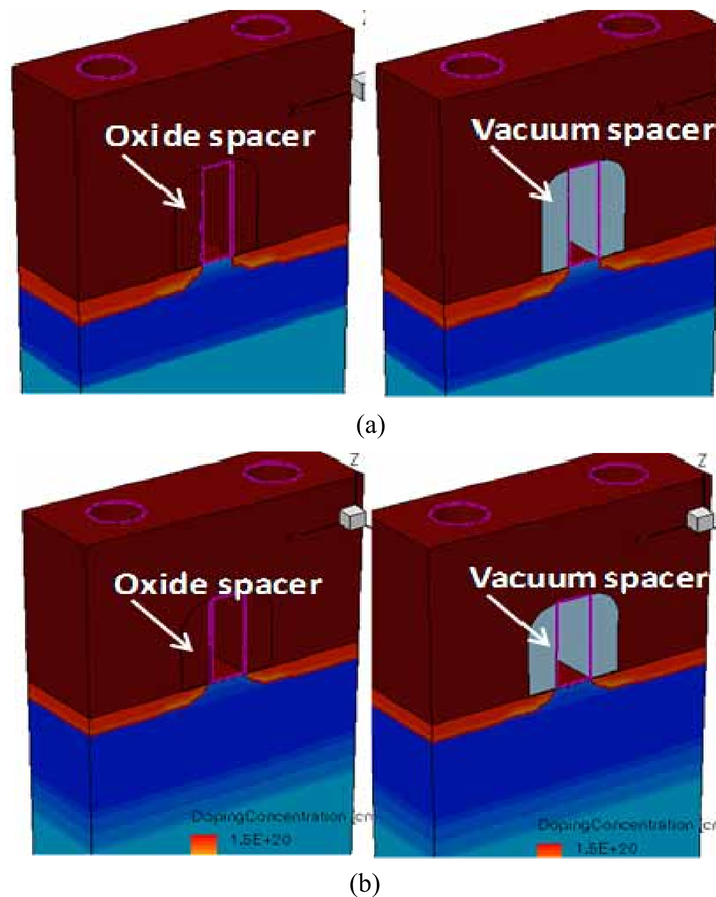


Figure 3.1: The final structures of NMOSFETs using Sentaurus.
(a) High performance NMOSFETs. T_{POLY} = 540Å, L_{GATE} = 16nm, contact size = 24nm, gate to contact distance = 20nm.
(b) Low standby power NMOSFETs. T_{POLY} = 600Å, L_{GATE} = 22nm, contact size = 30nm, gate to contact distance = 24nm

3.2.1.2 Structure and Process Concept

The proposed vacuum spacer gate last process flow is as follows. Figure 3.2 (a) shows that the sacrificial gate is patterned and source, drain and nitride spacer are formed as shown in Figure 3.2 (b). A very thin oxide liner (not shown) is deposited underneath the nitride spacer to protect the gate dielectric. ILD is deposited and oxide CMP carried out as shown in Figure 3.2 (c). Figure 3.2 (d) shows that after the sacrificial gate is removed, gate dielectric is deposited and the gate material is deposited and metal CMP carried out (or etch-back process). Figure 3.2 (e) shows that ILD is etched back some amount to expose the nitride spacer which is a sacrificial material. After that, the selective etch of the nitride spacer without damaging the gate dielectric to create a vacuum gap as shown in Figure 3.2 (f). Figure 3.2 (g) shows that non-conformal ILD2 deposition has sealed the top openings and sealed the vacuum spacers. And then the conventional contact process is followed. In this process, there are only 2 additional processes to make vacuum spacers: ILD etch back process and removing the nitride spacers. This process needs 2 different sacrificial materials, one is for sacrificial gate and the other is for sacrificial spacers. SiGe has higher selectivity over silicon oxide (300:1) [3.8]. Thus, our sacrificial gate is SiGe and sacrificial spacer is silicon nitride.

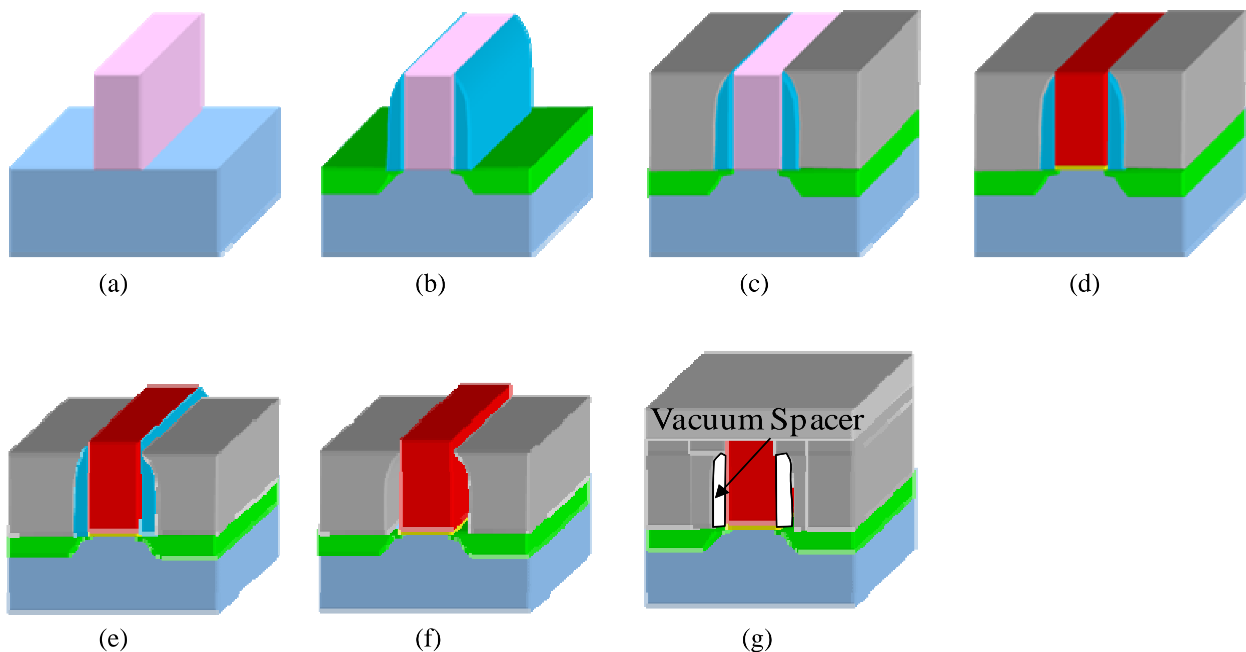


Figure 3.2: A proposed process flow of the vacuum spacer transistor with gate last process. (a) After gate sacrificial material is deposited, gate photolithography carries out. Sacrificial gate is etched using reactive ion etch (RIE) process. (b) Shallow S/D, sacrificial spacer, and deep S/D are formed, sequentially. (c) After ILD is deposited, oxide CMP carried out to expose top of the sacrificial gate. (d) After removing sacrificial gate material, gate oxide and real gate material are deposited, sequentially. And then metal CMP carried out to pattern the real gate. (e) ILD is etched back to expose top of the sacrificial spacer. (f) Sacrificial spacers are removed. (g) Non-conformal ILD is deposited to seal the vacuum gaps.

3.2.2 A vacuum spacer transistor with gate last and SAC process

3.2.2.1 The comparison of structures by simulation

3D structures with SAC are constructed using the Sentaurus structure editor [3.9]. We compare two devices: SAC devices with vacuum spacers and silicon nitride spacers. In order to study the effect of scaling on the benefits of the vacuum spacer, we also compare 65, 45, 32 and 20nm gate length structures as shown in Figure 3.3. In each generation, two transistors having identical design parameters such as S/D and channel doping, equivalent oxide thickness, and L_{GATE}. Retrograde body doping is created with a 500 Å, 2e18/cm3 doped region and a 210 Å, 1e16/cm3 doped epitaxial layer to suppress the short channel effect at 20nm gate length. We optimized the doping profiles at each generation. We assume the thickness of the gate is 600 Å at all generations. Some other parameters of each generation are shown in Table 3.2. The PMOSFETs have same structures as the NMOSFETs except for the dopants.

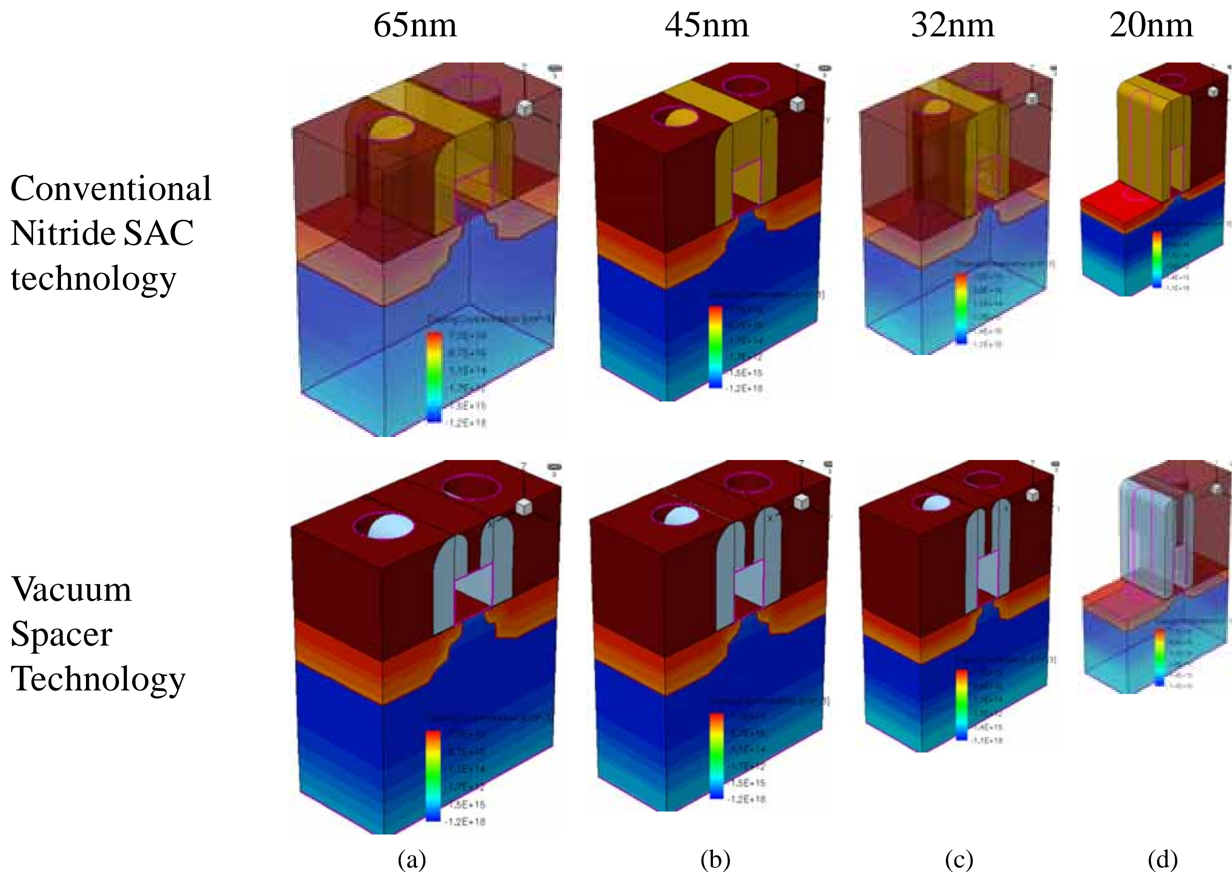


Figure 3.3: NMOSFETs with SAC process which is constructed with 3D simulator. Every generation has different parameters such as gate length, gate oxide thickness, spacer thickness, and V_{DD}. Nitride and vacuum spacer transistor at (a) 65nm, (b) 45nm, (c) 32nm, and (d) 20nm. ILD is removed to show the SAC process at 20nm gate length.

Gate Length	65nm	45nm	32nm	20nm
ILD and Gate Thickness	ILD 60nm / GATE 60nm			
Spacer Thickness	35nm	27nm	18nm	12nm
Contact Size	70nm	50nm	40nm	30nm
G_{OX}	1.3nm	1.2nm	1.1nm	1nm
V_{DD}	1.2V	1.1V	1V	1V

Table 3.2: Several key parameters at each generation.

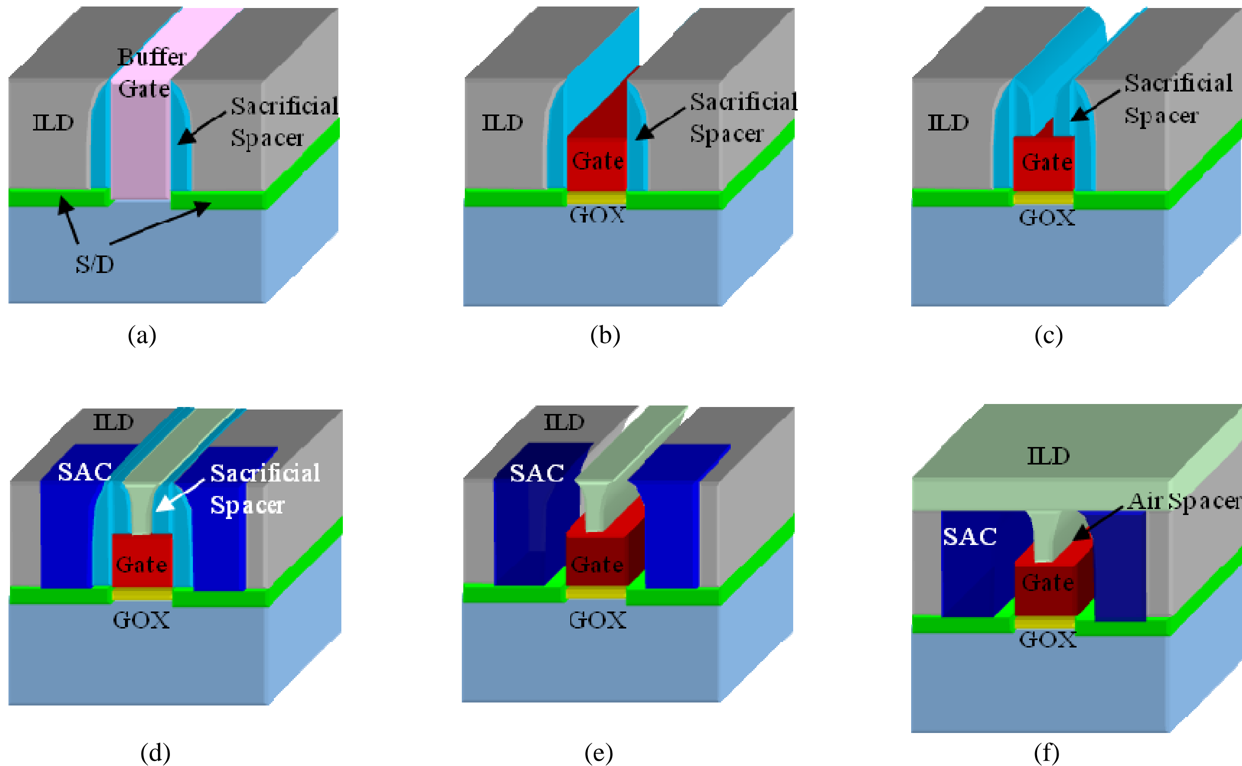


Figure 3.4: The proposed process flow of the novel vacuum spacer transistor with gate last and SAC processes. (a) After gate sacrificial material is deposited, the gate is etched using reactive ion etch (RIE) process. Shallow S/D, sacrificial spacer, and deep S/D are formed, sequentially. And then ILD is deposited and CMP carried out to expose top of the sacrificial gate. (b) After removing sacrificial gate material, gate oxide and real gate material are deposited, sequentially. And then gate material is etched back. (c) Another sacrificial spacers are formed. (d) After ILD is deposited, CMP carried out. In order to make SAC, contact holes are etched using high- selectivity etching. After contact material is deposited, CMP carries out to expose top of the sacrificial spacer. (e) Sacrificial spacers are removed. (f) Non-conformal ILD is deposited to seal the vacuum gaps.

3.2.2.2 Structure and Process Concept

The proposed vacuum spacer gate last process flow is as follows. Figure 3.4 (a) shows that the sacrificial gate is patterned and source, drain and nitride spacer (sacrificial spacer) are formed. A very thin oxide liner (not shown) is deposited underneath the nitride spacer to protect the gate dielectric. ILD is deposited and oxide CMP carried out. Figure 3.4 (b) shows that after the sacrificial gate is removed, gate oxide and gate material are deposited, sequentially. And then the gate material is etched back. Figure 3.4 (c) shows that another nitride spacer is formed on top of the gate to increase the vacuum spacer size. Figure 3.4 (d) shows that after ILD is deposited, oxide CMP carried out. After that, SAC is formed by high-selectivity contact hole etch and contact plug filling. A novel step of CMP to expose the top of the nitride spacer is performed. Figure 3.4 (e) shows the selective etch of the nitride spacer without damaging the gate dielectric to create vacuum gaps. Figure 3.4 (f) shows that non-conformal ILD2 deposition has sealed the top openings and sealed the air spacers.

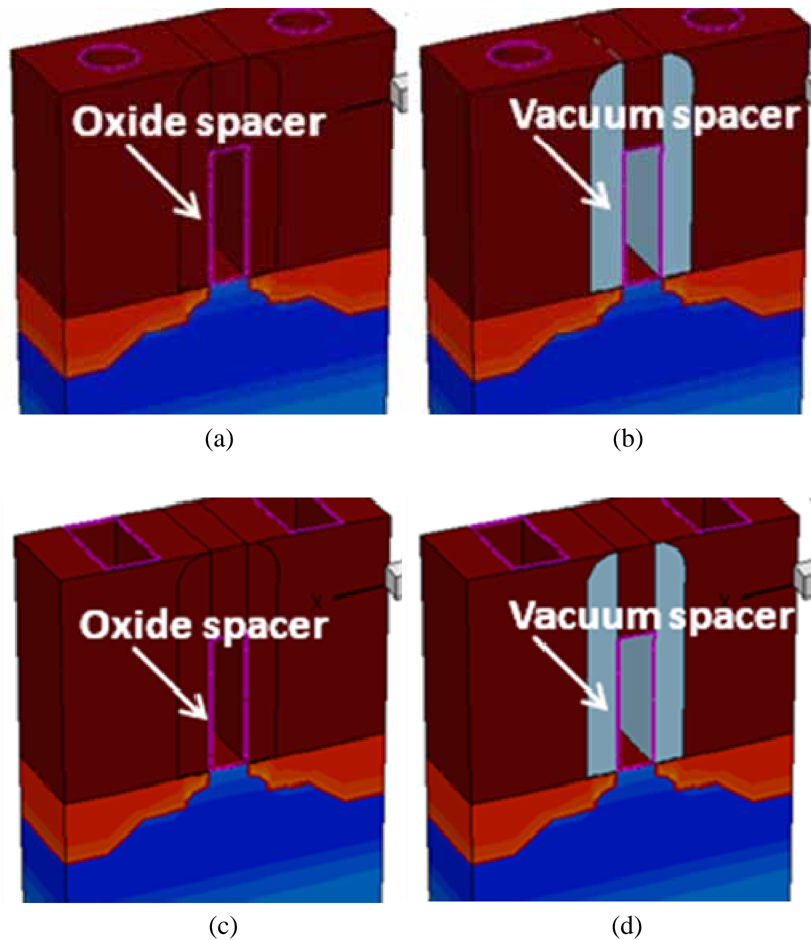


Figure 3.5: NMOSFETs are constructed with 3D simulator. LGATE=14nm. (a) Oxide spacer transistor with circular contact. (b) Vacuum spacer transistor with linear contact (c) Oxide spacer transistor with linear contact (d) Vacuum spacer transistor with linear contact

3.2.3 A vacuum spacer transistor with gate last and linear contact process

A process of fabricating the vacuum spacers was previously described for circular-contact transistors as shown in Figure 3.2. 3D computer simulations were employed in this study. 3D contact structures with circular and linear contacts are made by the Sentaurus structure editor [3.9]. We compared four devices: conventional oxide spacer transistors with circular and linear contacts shown in Figure 3.5 (a) and (b), and vacuum spacer transistors with circular and linear contacts in Figure 3.5 (c) and (d).

Except for the spacer material and contact shape, these four transistors have identical design parameters such as S/D and channel doping, gate oxide thickness, and gate length. Gate equivalent oxide thickness (EOT) and the gate length are 0.45nm and 14nm, respectively in accordance with International Technology Roadmap for Semiconductors (ITRS) 2009 [3.3]. The height of the gate is 52nm. The contact diameter/width is 20nm and the height of the contact is 86nm. The aspect ratio of the contact is 4.3. The thickness of the spacer and the distance between gate and contact are 12nm and 18nm, respectively. The PMOSFETs are identical to the NMOSFETs except for the dopants employed in the simulations.

3.3 Simulation Results

3.3.1 Vacuum spacer transistors of high performance and low standby power devices

The characteristics of transistors and inverters are simulated with Sentaurus 3D device simulator [3.9]. Figure 3.6 shows that I_{DS}-V_{GS} characteristics of both 16nm high performance NMOSFET and 22nm low standby power NMOSFET. Figure 3.6 (a) shows that the on-current is 1.7mA/um (ITRS: 1.7mA/um) and the off-current is below 10nA/um (ITRS: <100nA/um). The difference of on-current is only 3.4% between oxide spacer and vacuum spacer. However, the difference of on-current in low standby power devices is 14.2% as shown in Figure 3.6 (b). The on-current of oxide and vacuum spacers is 0.749mA/um (ITRS: 0.506mA/um) and 0.649mA/um and the off-current is below 30pA/um (ITRS: < 50pA/um), respectively. The general understanding is that the high performance transistors have S/D overlapped profile and thicker S/D extension region so that the on-current degrade of the poor controllability of gate channel edge due to the lower permittivity of the spacer material is no problem. However, in the low standby power devices, the structures have S/D underlapped profile and shallow S/D extension region so that there is a big on-current difference.

The delay time of vacuum spacer structure is decreased about 6.6% compared to oxide spacer structure in high performance device as shown in Figure 3.7 (a). However, the delay time of vacuum spacer structure is increased about 10% compared to oxide spacer structure in low standby power device because the on-current degradation is much bigger than the reduction of gate capacitance due to using vacuum spacer as shown in Figure 3.7 (b).

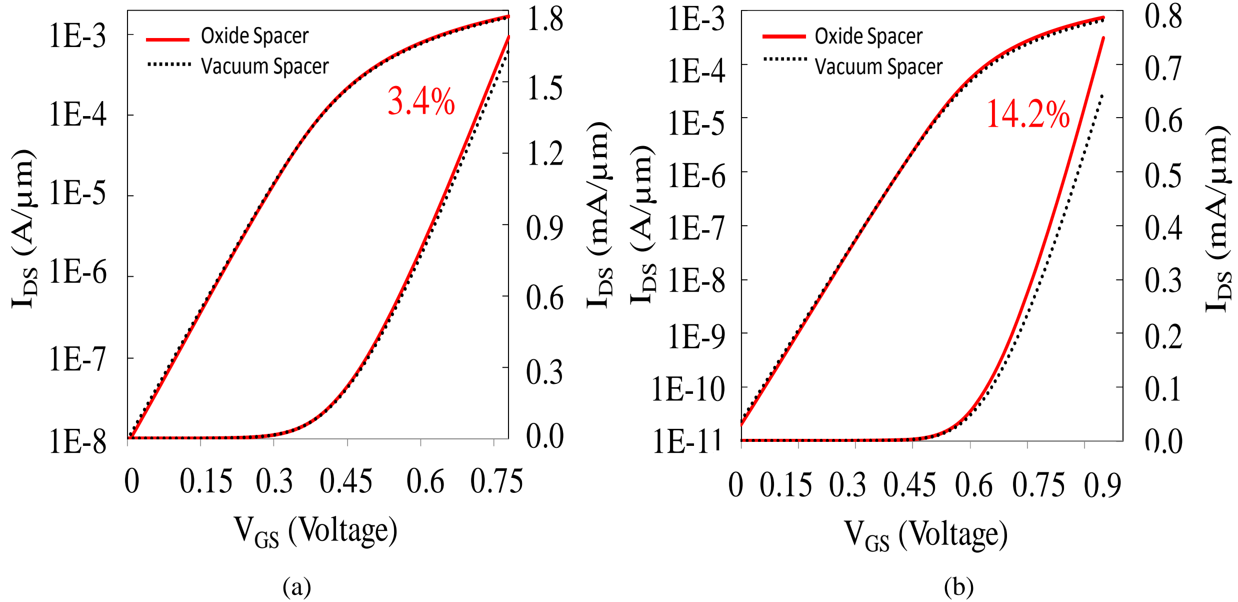
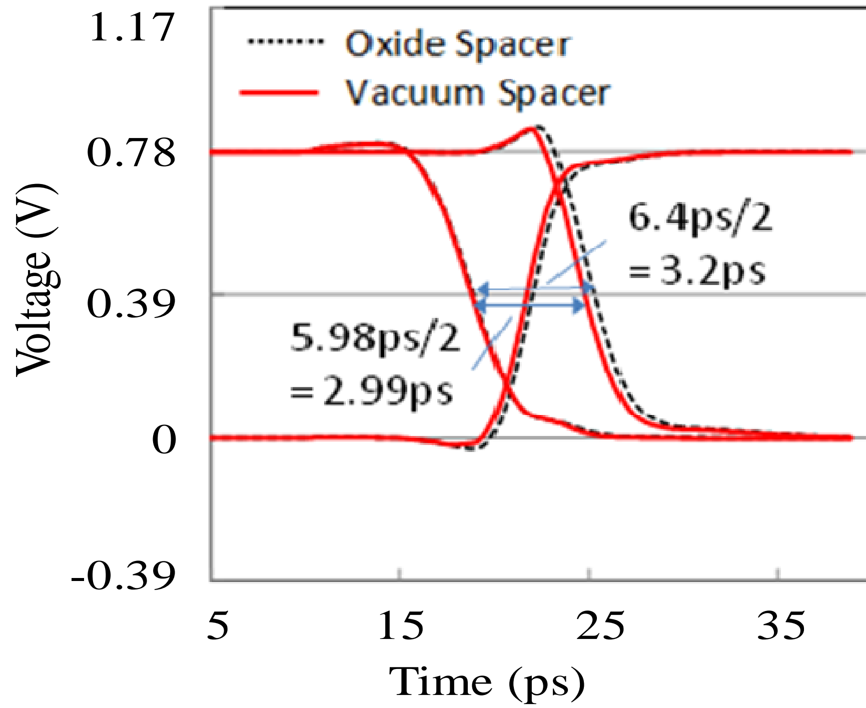


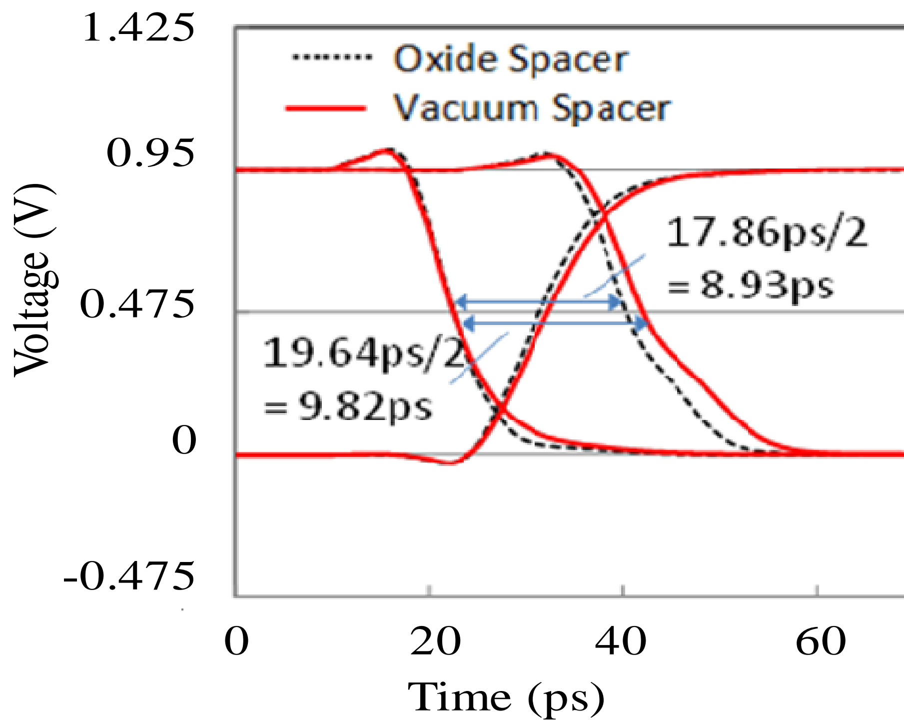
Figure 3.6: The simulated I_{DS}-V_{GS} characteristics of NMOSFETs (a) 16nm gate length in high performance device. (V_{DS}=0.78V) (b) 22nm gate length in low standby power device. (V_{DS}=0.95V)

Figure 3.8 (a) shows the calculated switching charge per area. The switching charges of vacuum spacer structures in the high performance and low standby power devices are decreased by 15.6% and 10.1%, respectively, compared to those of oxide spacer structures. Figure 3.8 (b) shows the calculated switching energy per area. The switching energies of vacuum spacer structures are also smaller than those of oxide spacer structure. The energies of vacuum spacer structure of high performance and low standby power devices are decreased by 19.1% and 9.3%, respectively.

All characteristics of transistors and inverters are shown in Table 3.3. The vacuum spacer technology is a promising solution for very small gate length devices for speed, switching charge, switching energy, and power consumption aspects. However, in the very shallow junction device, the degradation of on-current due to small controllability of gate channel edge should be considered when the vacuum spacer technology is used.

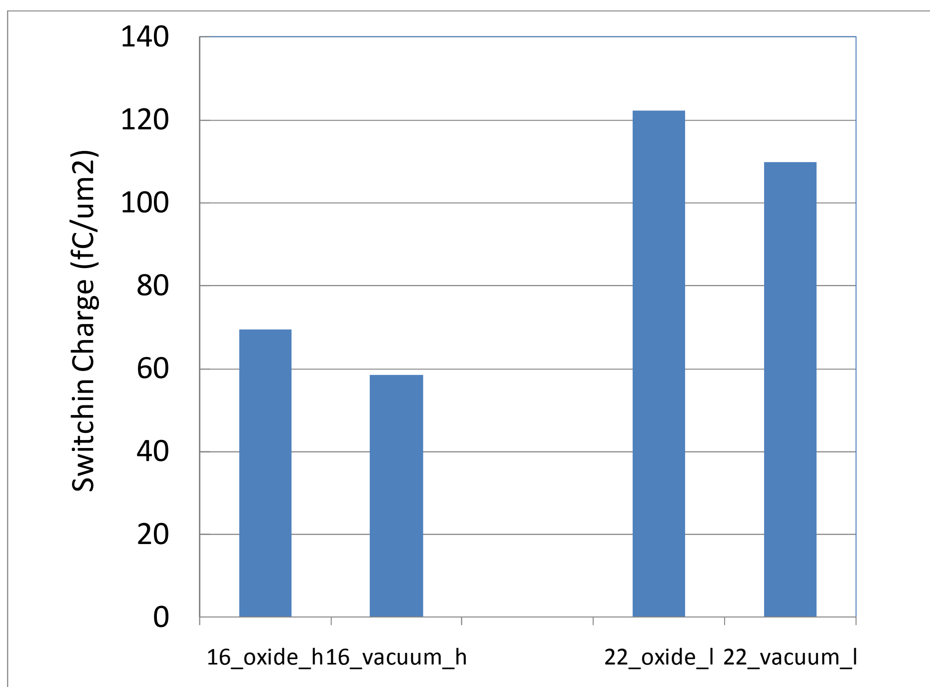


(a)

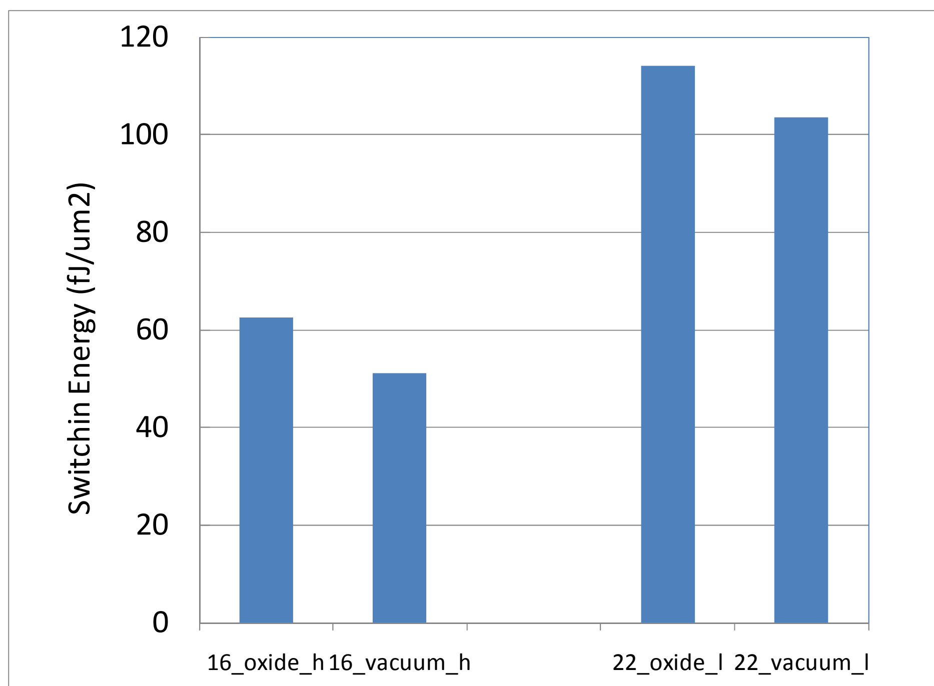


(b)

Figure 3.7: The 3D mixed-mode simulation results (a) the vacuum spacer transistor is faster than the oxide spacer in high performance device. (b) the vacuum spacer is slower than the oxide spacer in low standby power device.



(a)



(b)

Figure 3.8: (a) Switching charges are compared between oxide and vacuum spacer structures in both high performance and low standby power devices. (b) Switching energies are compared between oxide and vacuum spacer structures in both high performance and low standby power devices.

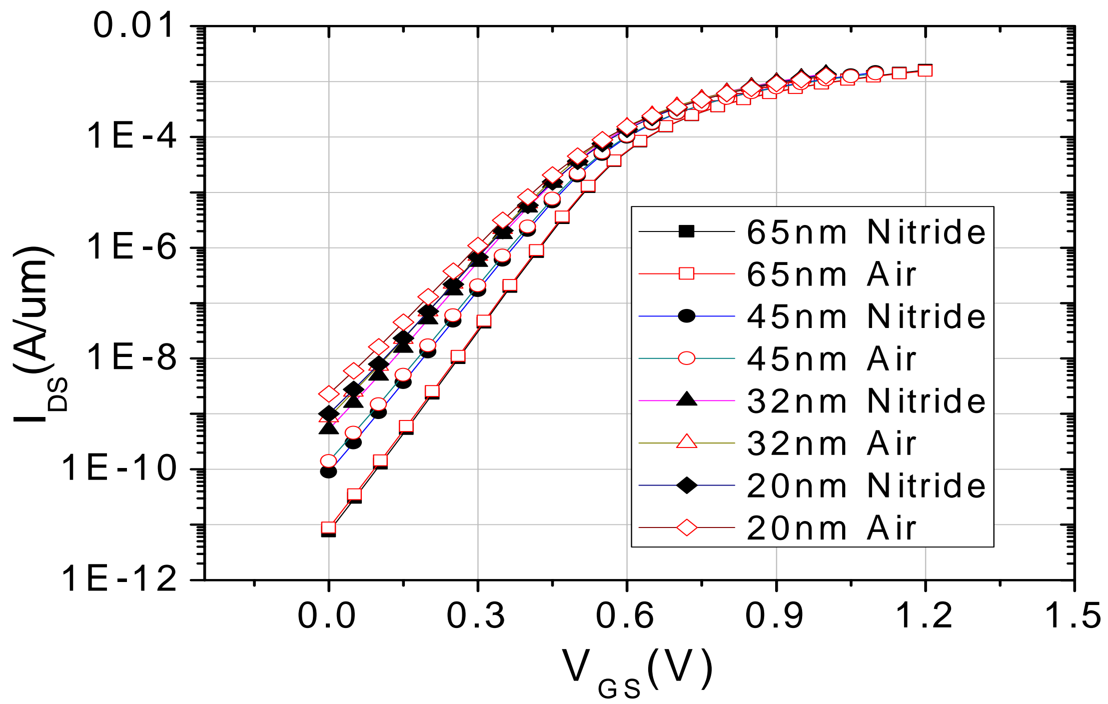
	High performance		Low standby power	
Gate spacer	Vacuum	Oxide	Vacuum	Oxide
NMOS I_{ON}/I_{OFF} (A/um)	1.63m 9.42n	1.69m 8.4n	0.649m 23.1p	0.749m 19.9p
PMOS I_{ON}/I_{OFF} (A/um)	0.834m 13.1n	0.854m 10.7n	0.359m 55.7p	0.376m 48.1p
Inverter Delay (ps)	2.99	3.2	9.82	8.93
Switching Charge (fC/um^2)	58.6	69.4	110	122
Switching Energy (fJ/um^2)	51.2	62.5	104	114

Table 3.3: Comparison between vacuum spacer and oxide spacer structures at both 16nm high performance and 22nm low standby power devices.

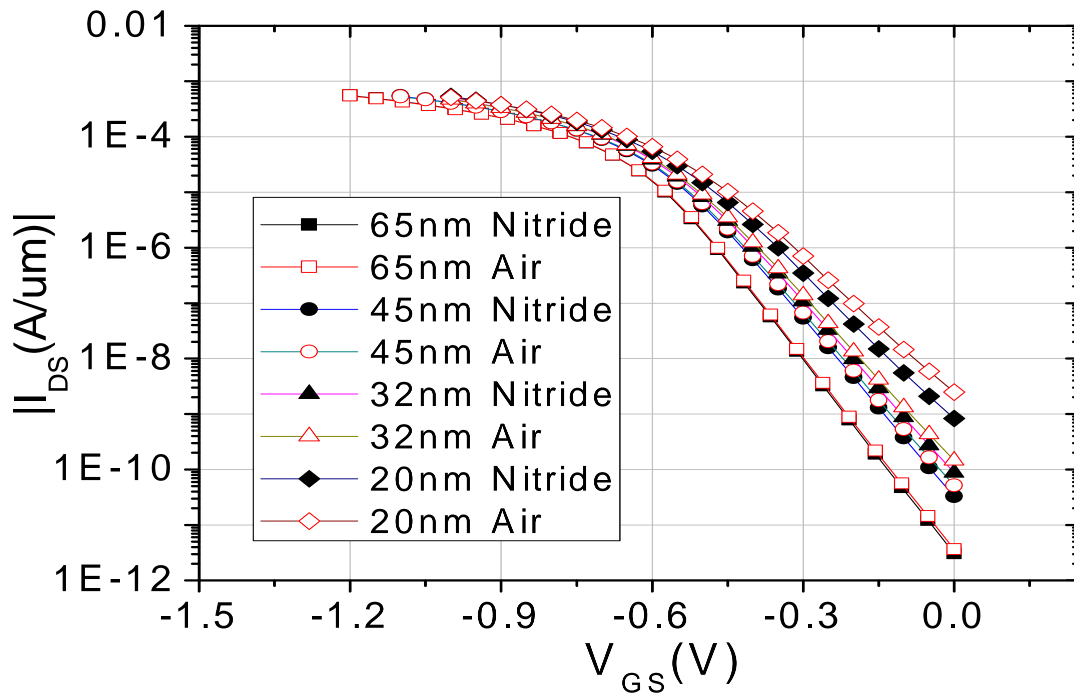
3.3.2 A vacuum spacer transistor with gate last and SAC process

The characteristics of transistors and inverters are simulated with Sentaurus 3D device simulator [3.9]. Figure 3.9 shows that the I_{DS}-V_{GS} characteristics of the two transistors are little changed by the spacer/contact designs at each generation. Generally, on-current is increased as the gate length is decreased. However, in this simulation, on-current is decreased as the gate length is decreased because V_{DD} is also decreased as technology node gets small. The differences of the NMOS off-current between vacuum and nitride spacers at the gate length 65nm, 45nm, 32nm, and 20nm are 18%, 55%, 64%, and 125%, respectively. The general understanding is that the higher permittivity the spacer material has, the greater control the gate fringing field has over the channel edge (hence the lower I_{OFF} is). Thus I_{OFF} (nitride spacer) is lower than that of vacuum spacer. As the gate length is decreased, the portion of this controllability of the gate fringing field is much increased so that the differences are increased.

Figure 3.10 shows the delay time of vacuum spacer structure is decreased about 25% compared to nitride spacer structure at 45nm gate length (V_{DD} = 1.1V). Generally, the delay time is decreased as the gate length is decreased. However, figure 3.11 shows that delay time is increased since the portion of gate capacitance is increased due to the SAC technology. Thus, the benefit of vacuum spacer over nitride spacer is more and more significant as the gate length is decreased.



(a)



(b)

Figure 3.9: Simulated I_{DS}-V_{GS} characteristics of the MOSFETs are basically the same. (V_{DS} = 1.2, 1.1, 1.0, and 1.0V at 65, 45, 32, and 20nm, respectively). (a) NMOS (b) PMOS

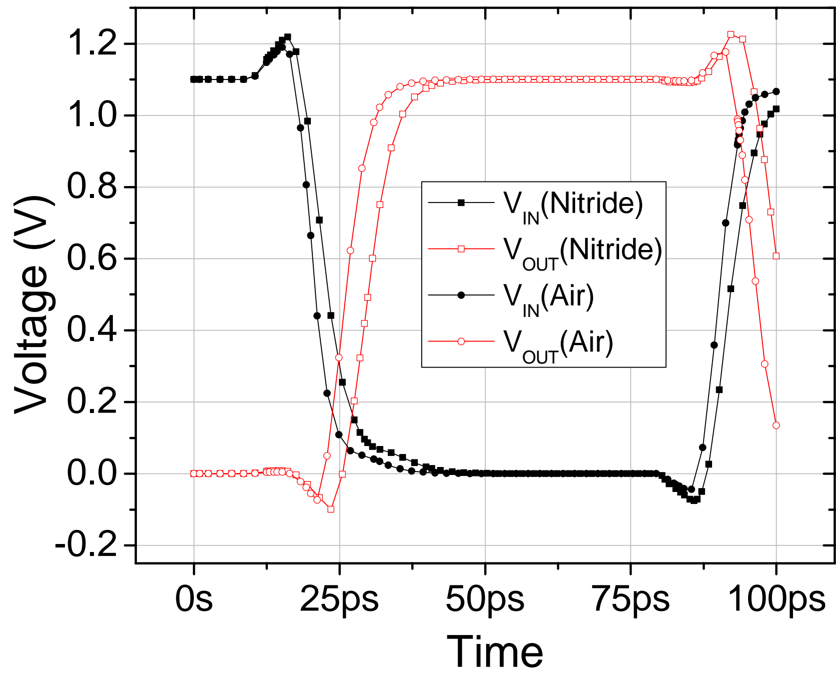


Figure 3.10: The 3D mixed-mode simulation results at 45nm gate length. (tPLH_vacuum =5.7ps, tPLH_nitride = 7.6ps, tPHL_vacuum = 5.9ps, tPHL_nitride = 7.9ps, tP = (tPHL + tPLH)/2, tP_vacuum = 5.8ps, tP_nitride = 7.75ps). The delay of vacuum spacer is decreased by 25% compared with nitride spacer.

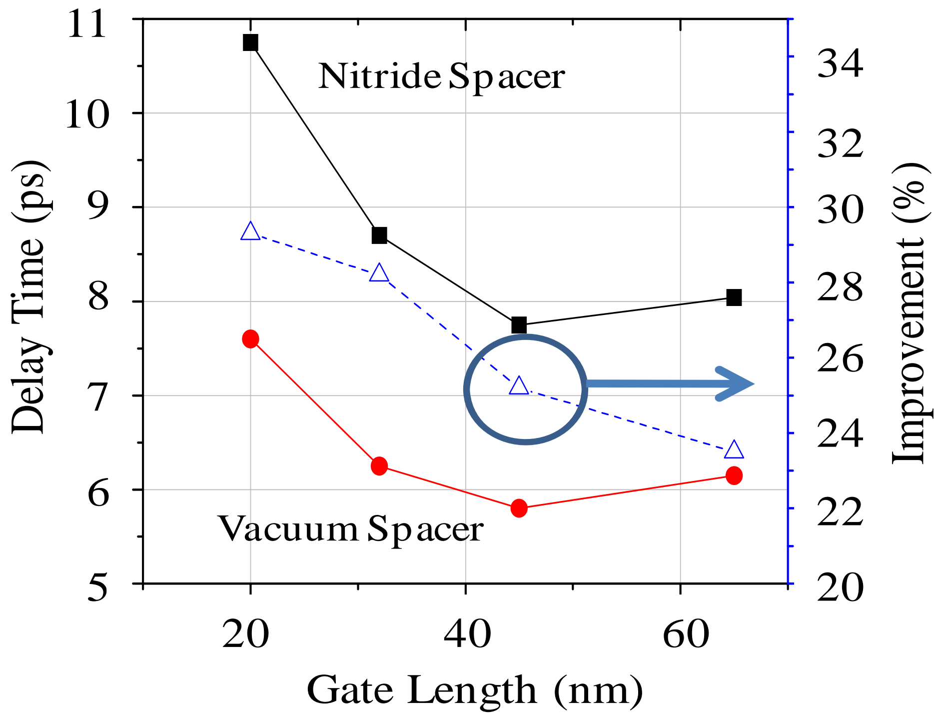


Figure 3.11: The Delay time is increased as the gate length is decreased.

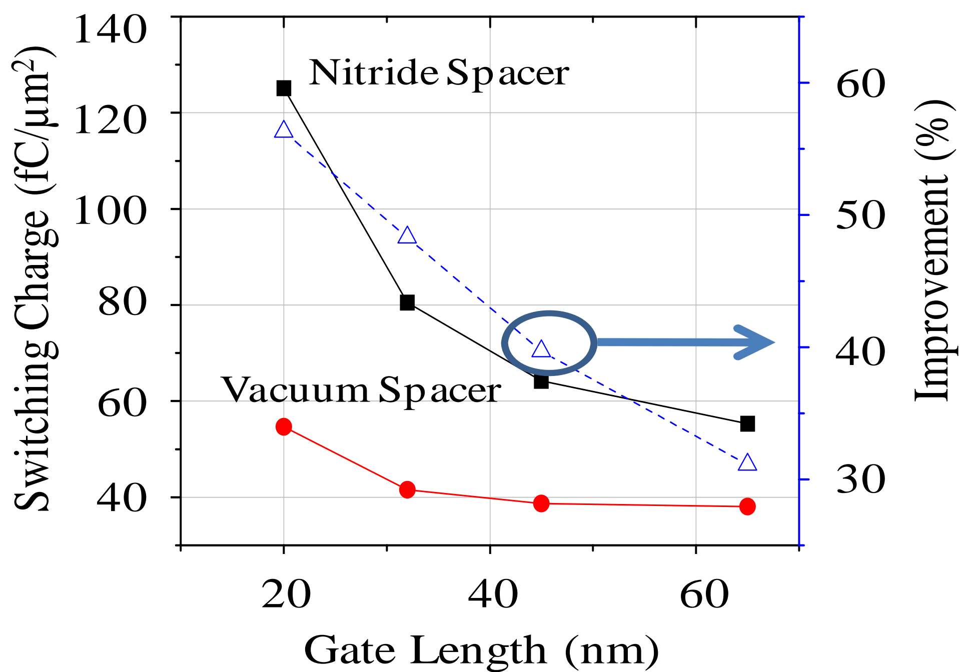


Figure 3.12: Switching charge is compared between nitride and vacuum spacer structures.

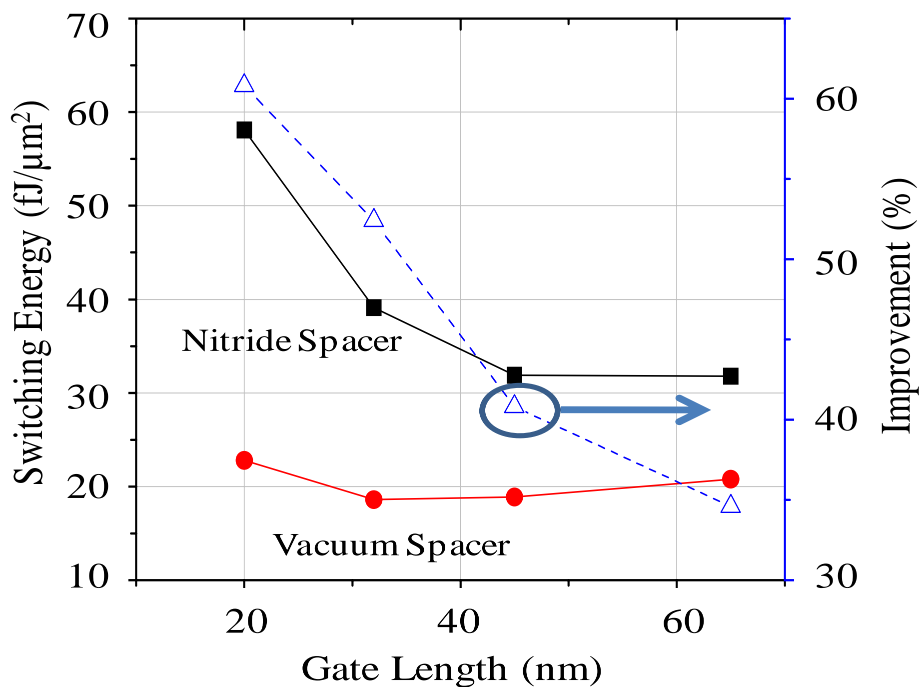


Figure 3.13: The benefit of switching energy using vacuum spacer is much increased below 30nm of gate length.

Figure 3.12 shows that switching charge per area is increased as the gate length is decreased. The switching charge of vacuum spacer at 20nm is smaller than that of nitride spacer at 65nm. The improvement of switching charge using vacuum spacer is from 35% to 57% as the gate length is scaled from 65nm to 20nm. Figure 3.13 shows that switching energy per area is also increased when the gate length is reduced. In nitride spacer technology, the switching energy is changed from 32fJ/um^2 to 58fJ/um^2 as the gate length is changed from 65nm to 20nm. In vacuum spacer technology, the change of switching energy is only 4fJ from 65nm to 20nm gate length. This vacuum spacer technology is more and more important to lower not only delay time but also power consumption as the technology node is getting smaller and smaller. The summary of all data is shown in Table 3.4. The characteristics of vacuum spacer are excellent over all generations, especially at smaller size.

Gate Length	65nm		45nm		32nm		20nm	
Spacer Type	Si3N4	Air	Si3N4	Air	Si3N4	Air	Si3N4	Air
NMOS I_{ON} (A/um) NMOS I_{OFF} (A/um)	1.61m 7.44p	1.56m 8.76p	1.46m 90.1p	1.40m 0.14n	1.39m 0.53n	1.32m 0.87n	1.35m 1.01n	1.26m 2.28n
PMOS I_{ON} (A/um) PMOS I_{OFF} (A/um)	0.56m 3.07p	0.55m 3.64p	0.54m 32.6p	0.53m 51.3p	0.48m 87.5p	0.47m 0.15n	0.53m 0.83n	0.51m 2.49n
Delay (ps)	8.04	6.15	7.75	5.8	8.7	6.25	10.75	7.6
Switching Charge (C/um^2)	55.3f	38.1f	64.2f	38.7f	80.5f	41.6f	125.1f	54.7f
Switching Energy (J/um^2)	31.8f	20.8f	31.9f	18.9f	39.1f	18.6f	58.1f	22.8f

Table 3.4: Characteristics of transistors and inverters between a conventional SAC with nitride spacer and SAC with vacuum spacer. The SAC with vacuum spacer inverter is better in speed and power.

3.3.3 A vacuum spacer transistor with gate last and linear contact process

The characteristics of transistors and inverters are simulated with Sentaurus 3D device simulator [3.9]. Figure 3.14 shows the I_{DS}-V_{GS} characteristics of the four transistors. The off currents are basically the same but the on currents of the linear contact devices are increased by about 10% compared to the circular contact devices due to low contact resistance. The on currents of vacuum spacer devices are decreased by about 6% compared to the oxide spacer devices. A higher permittivity spacer material allows the gate to better reduce the S/D resistance through its fringing field, hence the higher I_{ON}.

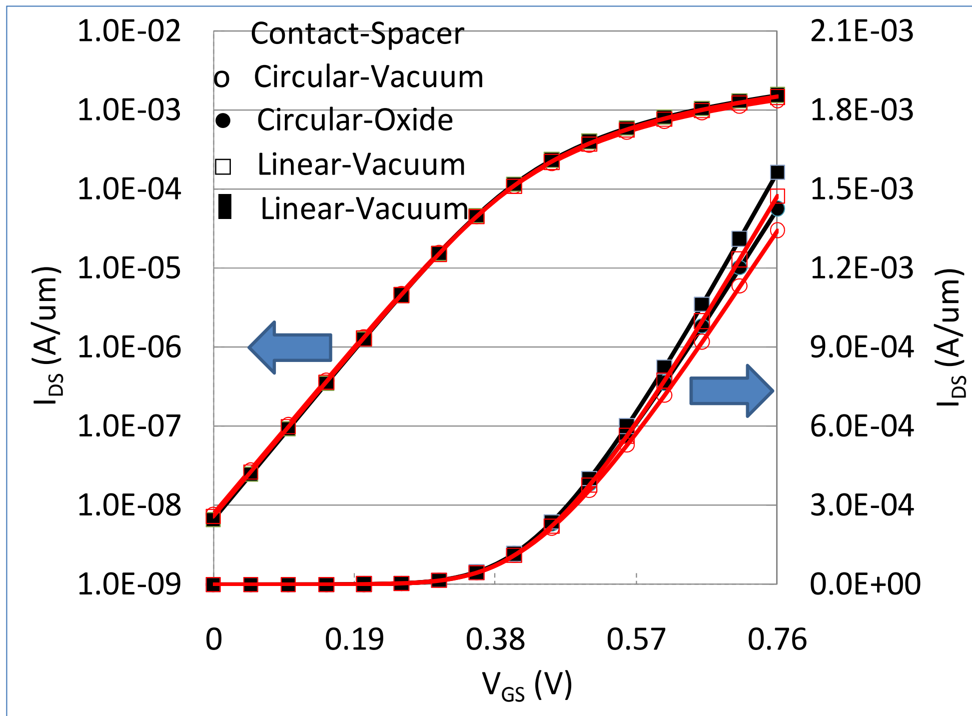


Figure 3.14: Simulated I_{DS}-V_{GS} characteristics of the four types of NMOSFETs (V_{DD} = 0.76V, V_{DS} = 0.76V). Linear contacts increase I_{ON} by about 10% over circular contact. Vacuum spacers decrease I_{ON} by about 6% relative to oxide spacer.

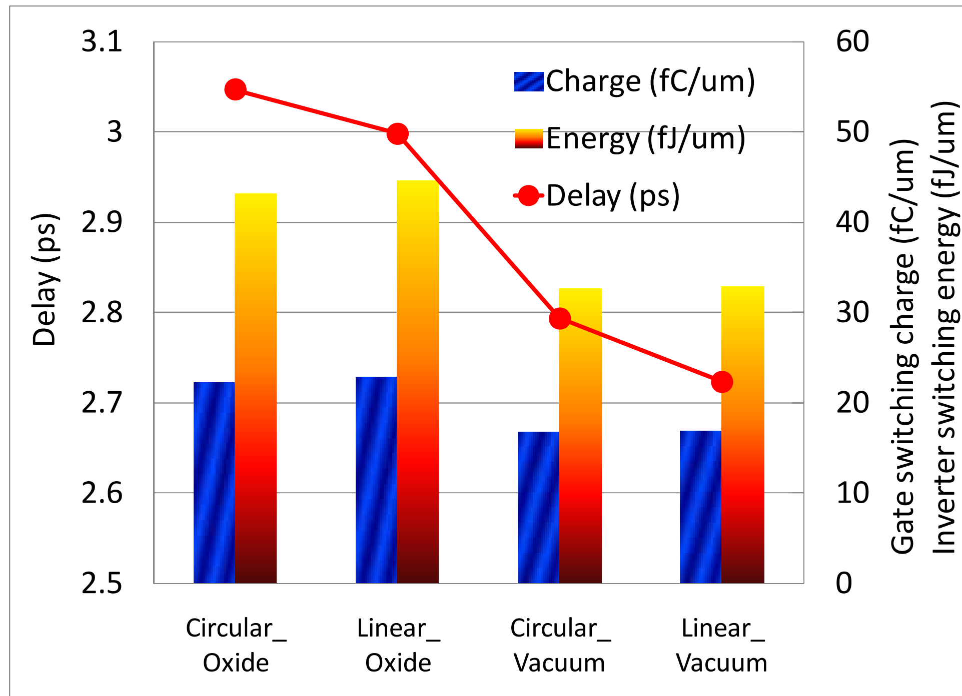


Figure 3.15: Mixed-mode simulation of the 4 stage inverter chains (Fan-out = 1). The delay of linear contact is faster than that of circular contact. The vacuum spacer technology significantly reduces the inverter delay, gate switching charge, and inverter switching energy relative to oxide spacer technology.

Figure 3.15 shows the 4 stage inverter chains simulated with 3D mixed–mode simulator. Inverters using the linear contact transistor are faster than those using the conventional circular contact transistor. However, the improvement is only about 2% even though the on current of the linear contact is increased by about 10% compared to the circular contact. The reason is that the gate-to-contact capacitance of the linear contact is larger than that of the circular contact transistors. With vacuum spacer technology, the delay time is reduced by about 10% in Figure 3.15 (even though the on-current of the vacuum spacer transistor is degraded by about 6% as shown in Figure 3.15). The gate switching charge and the switching energy are calculated. The vacuum spacer technology decreases the gate switching charge by 25% compared to the oxide spacer technology. It also decreases the inverter switching energy by 24%.

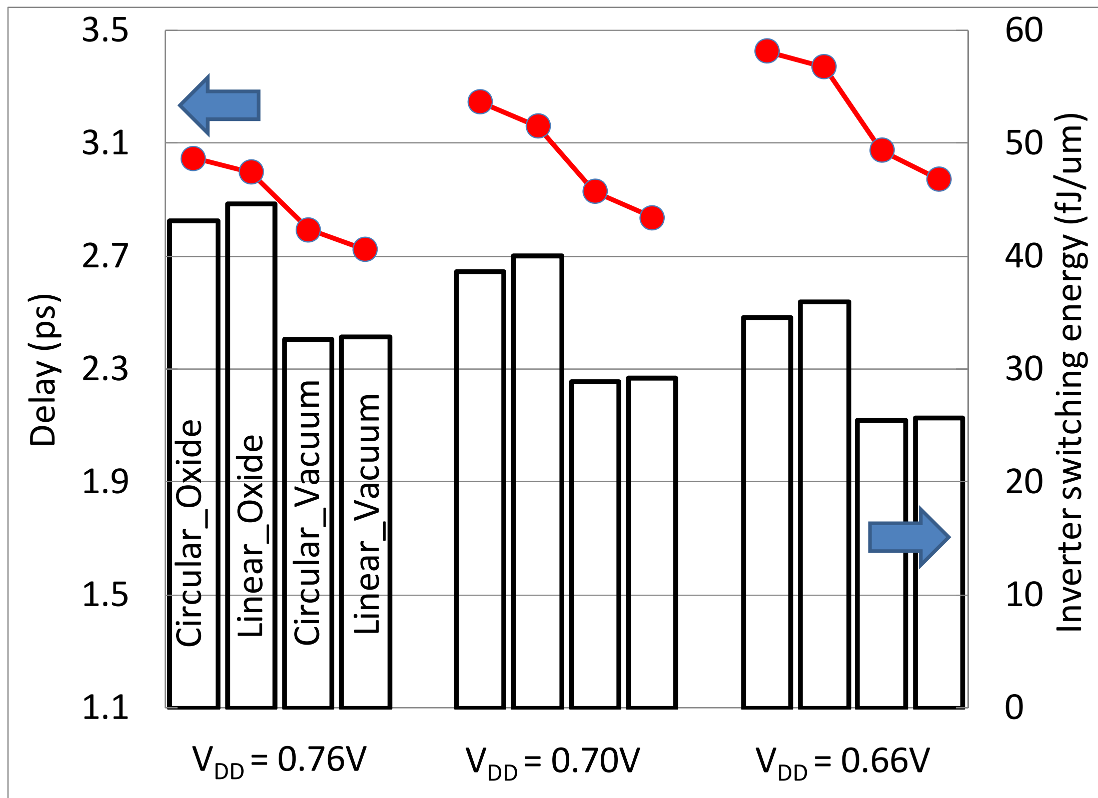


Figure 3.16: Simulated inverter delay and the switching energy at three V_{DD} (0.76V, 0.70V, 0.66V)

Figure 3.16 shows the effect of V_{DD} on inverter delay and switching energy. The vacuum spacer technology has an even greater switching energy advantage than the oxide spacer technology if the two are operated at the same speed. Vacuum spacer inverter with linear contact at 0.66V has the same delay as the oxide spacer inverter with linear contact at 0.76V. At these constant speed conditions, the vacuum and oxide spacer inverters have the switching energy of 25.4 and 44.6 fJ/um, respectively. The switching energy improvement is 43%. Some key characteristics of these four transistors and inverters are shown in Table 3.5.

	Oxide Spacer		Vacuum Spacer	
Contact	Circular	Linear	Circular	Linear
NMOS (A/um) I_{ON} / I_{OFF}	1.43m 7.23n	1.56m 6.59n	1.35m 7.92n	1.47m 7.25n
PMOS (A/um) I_{ON} / I_{OFF}	0.703m 16.1n	0.84m 16.3n	0.684m 17.6n	0.815m 17.9n
Inverter Delay (ps) (V_{DD} = 0.76V) (V_{DD} = 0.66V)	3.047 3.426	2.998 3.37	2.794 3.075	2.723 2.971 (9.1%↑)
Switching Energy (fJ/um) (V_{DD} = 0.76V) (V_{DD} = 0.66V)	43.2 34.6	44.6 35.9	32.6 25.4	32.9 25.7 (22%↓)

Table 3.5: Comparison of four different transistors. The vacuum spacer transistor with linear contact excels in speed and energy.

3.4 Reasonable Expectation

With scaling of planar bulk MOSFETs, the channel doping will need to be increased to undesirably high levels in order to gain adequate control of short-channel effects and to set the threshold voltage properly. Another challenge for highly scaled MOSFETs is reducing the parasitic series S/D resistance to tolerable values with very shallow source and drain junction depth. Due to the challenges with scaling planar bulk MOSFETs, advanced devices such as ultra-thin body fully depleted SOI MOSFETs and multiple-gate, particularly double-gate (DG) MOSFETs (e.g., FinFETs) are expected to be eventually implemented.

However, the parasitic capacitances of these processes are much increased. Even if current characteristics are improved by these processes, the performance such as speed and power consumption is not improved much because of this increased capacitance. Our vacuum spacer technology can be used in these processes to reduce parasitic capacitance. For example, two proposed processes are illustrated in Figure 3.17 and 3.18. Figure 3.17 shows that a vacuum spacer process can be compatible with SOI or raised S/D structures. This structure is very similar to SAC with vacuum spacer process. Thus, the simulation results were described in Chapter 2.5.2, a SAC with vacuum spacer and gate first processes and Chapter 3.2.2, a SAC with vacuum spacer and gate last processes. Figure 3.18 shows another vacuum spacer process that can be used for FinFET process. FinFET process has larger parasitic capacitance than MOSFET process. Thus, the effect of the vacuum spacer will be better than general MOSFET structure.

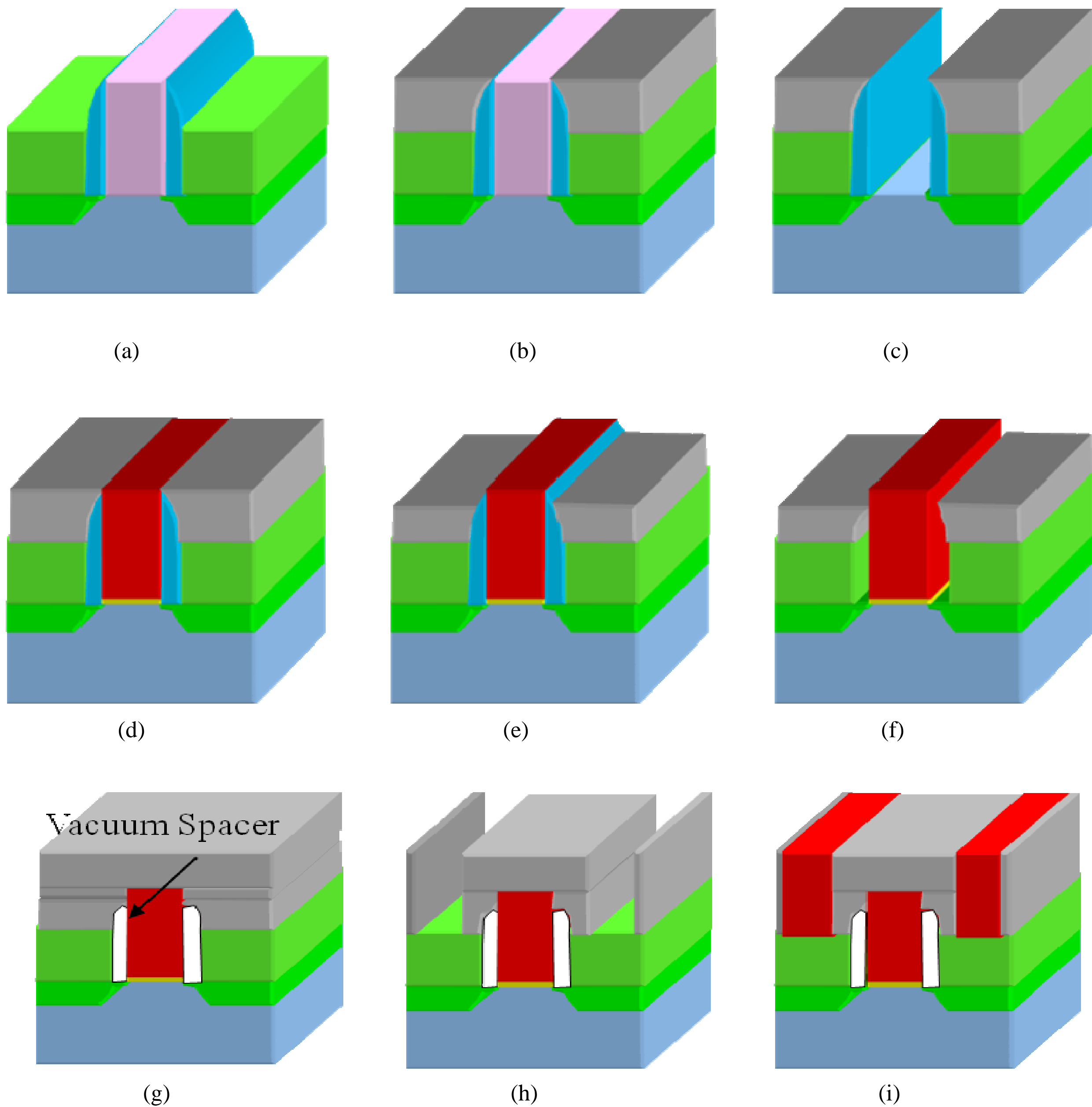


Figure 3.17: The proposed process flow of the novel vacuum spacer transistor with gate last and raised S/D and linear contact processes. (a) After gate sacrificial material is deposited, the gate is etched using reactive ion etch (RIE) process. Shallow S/D, sacrificial spacer, and deep S/D are formed, sequentially. And then raised S/D is formed. (Silicide process is optional process.) (b) After ILD is deposited, CMP carried out to expose top of the sacrificial gate. (c)-(d) After removing sacrificial gate material, gate oxide and real gate material are deposited, sequentially. And then gate material is etched back. (e) ILD is recessed to expose top of the sacrificial spacer. (f) Removing the sacrificial spacer. (g) Non-conformal ILD is deposited to seal the vacuum gaps. (h) After linear contact photo is done, ILD is etched using RIE etching process to connect the raised S/D region. (i) Contact material is deposited and recessed to fill the contact plug.

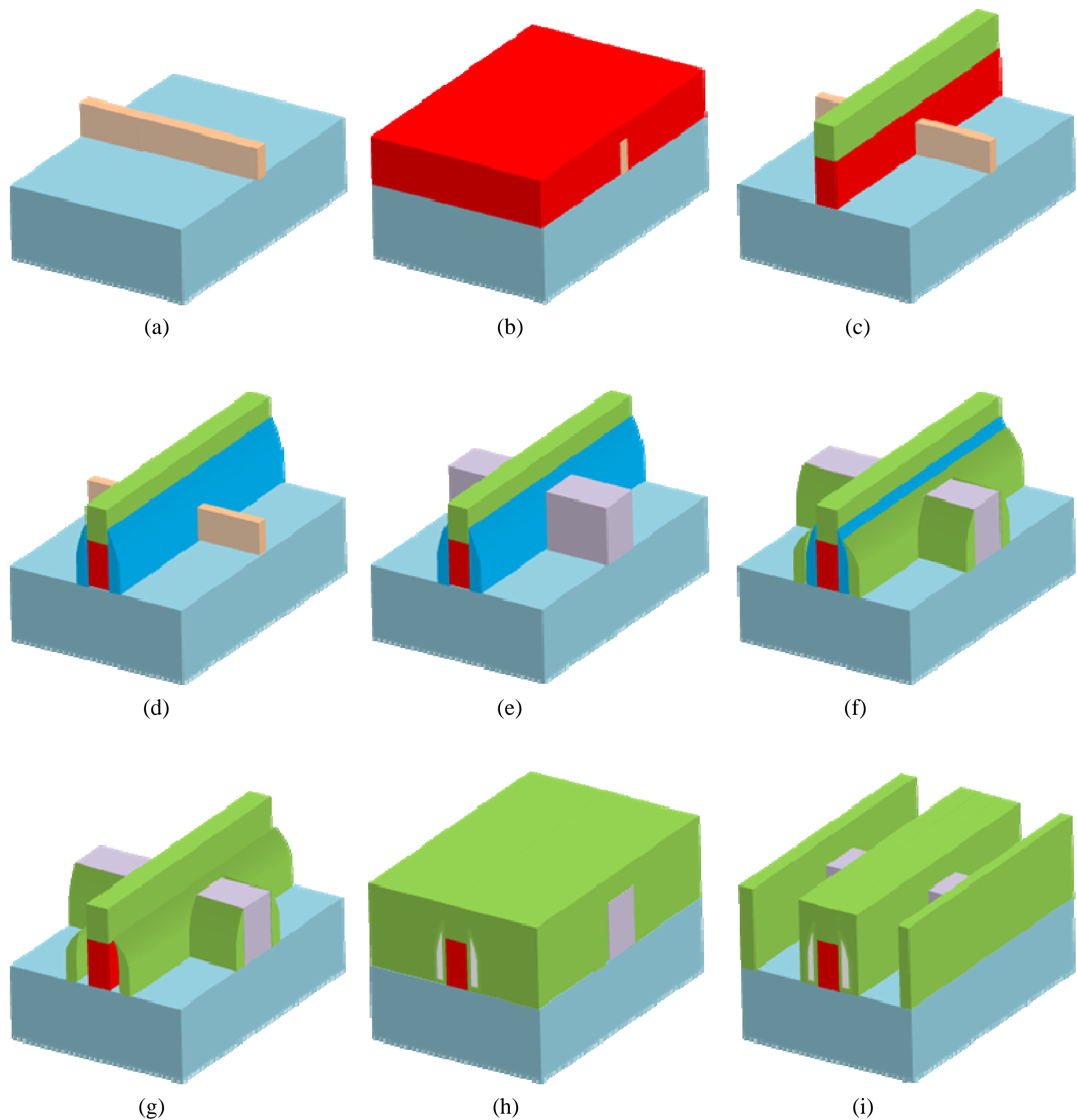


Figure 3.18: The proposed process flow of the novel vacuum spacer transistor with FINFET and linear contact processes. (a) Silicon is etched on SOI wafer to make a fin. (b) Gate oxide and gate material are deposited, sequentially. And then CMP carried out. (c) After gate hard mask is deposited, the gate mask and gate material are etched, sequentially. (d) Sacrificial spacers are formed. In this process, the sacrificial spacers are formed only at the gate sides not at the fin side using controlling over etch time. (e) Raised S/D is formed. (f) Oxide spacers are formed to expose the top of the sacrificial spacer. (g) Sacrificial spacers are removed. (h) After non-conformal ILD is deposited to seal the vacuum gaps, CMP carried out. (i) After linear contact photo is done, ILD is etched using RIE etching process to connect the raised S/D region. After that, contact material is deposited to fill the contact plug which is not shown in this figure for simplicity.

The proposed vacuum spacer with raised S/D process flow is as follows. Figure 3.17 (a) shows that the sacrificial gate is patterned and source, drain and nitride spacer (sacrificial spacer) are formed. A very thin oxide liner (not shown) is deposited underneath the nitride spacer to protect the gate dielectric. After that, raised S/D is formed to reduce S/D resistance. Figure 3.17 (b) shows that ILD is deposited and oxide CMP carried out to expose top of the sacrificial gate. Figure 3.17 (c) shows that the sacrificial gate is removed. After gate oxide and gate material are deposited, sequentially. And then the gate material is etched back as shown in Figure 3.17 (d). Figure 3.17 (e) shows that ILD is etched back to expose top of the nitride spacer. Figure 3.17 (f) shows the selective etch of the nitride spacer without damaging the gate dielectric to create vacuum gaps. Non-conformal ILD deposition has sealed the top openings and sealed the vacuum spacers as shown in Figure 3.17 (g). Figure 3.17 (h) and (i) show linear contact process. This contact process can be changed easily to conventional circular contact process using change the contact mask.

Another proposed vacuum spacer with FinFET process flow is as follows. Figure 3.18 (a) shows that silicon fin is etched on the SOI wafer. And then gate oxide and gate material are deposited, sequentially. CMP carried out to planarize the surface as shown in Figure 3.18 (b). After gate mask is deposited, gate mask and gate material are etched, sequentially as shown in Figure 3.18 (c). Figure 3.18 (d) shows that sacrificial (nitride) spacers are formed. A very thin oxide liner (not shown) is deposited underneath the nitride spacer to protect the gate dielectric. The fin height can be controlled by over etch time. Gate height is much taller than fin height. Thus, sacrificial spacers are formed at only gate sides not fin sides. Figure 3.18 (e) shows that raised S/D is formed to reduce the S/D resistance. Figure 3.18 (f) shows that oxide spacers are formed to expose top of the nitride spacers. Oxide spacer height can be controlled by over etch time. Figure 3.18 (g) shows the selective etch of the nitride spacer without damaging the gate dielectric to create vacuum gaps. Figure 3.18 (h) shows that non-conformal ILD deposition has sealed the top openings and sealed the vacuum spacers. Figure 3.18 (i) shows linear contact process.

3.5 Summary

In high performance device case, the vacuum spacer technology will be a promising solution in the speed, switching charge, switching energy, and power aspects because reducing the device capacitance will be an increasingly important way to improve the performances. In low standby power device case, the degradation of on-current should be carefully considered when the low-k spacer material is used. The partial spacer technology which the high-k material is located near surface and low-k material is located in the top of the high-k spacer will be very helpful to this low standby power device which is described in chapter 4.

Reducing the device capacitance will be an increasingly important way to improve the device speed and switching energy/power at smaller gate length. High density memories employ the SAC technology that requires the use of nitride spacer which significantly raises the delay and switching power. A novel SAC gate last vacuum spacer structure that yields small size, high speed and low switching energy is proposed. Compared to a vacuum spacer technology, a conventional nitride spacer transistor would have 41% longer delay and 129% larger switching

charge and 155% larger switching energy at 20nm gate length. These benefits are more and more significant for smaller dense memories.

Reducing contact resistance is an increasingly important approach to improving the device speed. Linear contact technology was recently introduced into production to increase the on current but it also increases the gate-to-contact capacitance. Vacuum spacer is a concept recently proposed for the conventional circular contact MOSFETs. Vacuum spacer is particularly attractive for future linear contact device, which has larger gate to contact capacitive coupling. Mixed-mode simulation shows that the delay of linear contact inverter can be improved with vacuum spacer technology by 10%. More significantly, the inverter switching energy (power consumption) can be reduced by about 25% using vacuum spacer technology at the fixed VDD=0.76V. The power consumption of vacuum spacer with linear contact inverter can be decreased by 43% at the same speed relative to circular-contact oxide spacer inverter. This is almost a factor of two improvement in switching energy.

3.6 References

[3.1] M. Togo, A. Tanabe, A. Furukawa, K. Tokunaga, and T. Hashimoto, "A Gate-side Air-gap Structure(GAS) to Reduce the Parasitic Capacitance in MOSFETs", Symposium on VLSI technology Digest, pp.38-39, 1996

[3.2] Jemin Park and Chenming Hu, "Air Spacer MOSFET Technology for 20nm Node and Beyond", ICSICT, pp.53-56, China, October 2008

[3.3] International Technology Roadmap for Semiconductors for Interconnect, 2009

[3.4] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. Mclntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging", International Electron Devices Meeting, pp.247-250, December 2007

[3.5] S. Mayuzumi, J. Wang, S. Yamakawa, Y. Tateshita, T. Hirano, M. Nakata, S. Yamaguchi, Y. Yamamoto, Y. Miyanami, I. Oshiyama, K. Tanaka, K. Tai, K. Ogawa, K. Kugimiya, Y. Nagahama, Y. Hagimoto, R. Yamamoto, S. Kanda, K. Nagano, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, S. Kadomura, and N. Nagashima, "Extreme High-Performance n- and p-MOSFETs Boosted by Dual-Metal/High-k Gate Damascene Process using Top-Cut Dual Stress Liners on (100) Substrates", International Electron Devices Meeting, pp.293-296, December 2007

[3.6] Jemin Park and Chenming Hu, "Air-Spacer MOSFET with Self-Aligned Contact for Future Dense Memories", IEEE Electron Device Letters, volume 30, issue 12, pp. 1368-1370, 2009

[3.7] Chris Auth, Mark Buehler, Annalisa Cappellani, Chi-hing Choi, Gary Ding, Weimin Han, Subhash Joshi, Brian Mcintyre, Matt Prince, Pushkar Ranade, Justin Sandford, and Christopher

Thomas, “45nm High-k+ Metal Gate Strain-Enhanced Transistors”, Intel Technology Journal, pp.77-85, June 2008

[3.8] KIM Sung-Min, OH Chang-Woo, CHOE Jeong-Dong, LEE Chang-Sub, and PARK Dong-Gun, “A study on selective Si0.8Ge0.2 etch using polysilicon etchant diluted by H2O for three-dimensional Si structure application”, Proceedings – Electrochemical Society, Volume 5, pp.81-86, 2003

[3.9] SENTAURUS User Manual, Synopsys, Mountain View, CA

.

Chapter 4

Corner Spacer Transistor

4.1 Introduction

Lowering the capacitance is increasingly important for improving not only speed but also power dissipation. Over 70% of the gate switching charge can be due to the gate to contact-plug and gate to source/drain (S/D) diffusion capacitances which is described in Chapter 2. In order to reduce these capacitance components without increasing the gate to contact distance, the material between gate and contact-plug should be a relatively low dielectric (low-k) material. However, the degradation of on and off current occurs.

In Chapter 2, the off current of nitride spacer transistor is lower than that of oxide or vacuum spacer transistors. The general understanding is that the higher permittivity the spacer material has, the greater control the gate fringing field has over the channel edge (hence the lower I_{OFF} is). And the on current of nitride spacer transistor is higher than that of oxide or vacuum spacer transistors. It is known that high-k spacer increases the on-state current [4.1]. A higher permittivity spacer material allows the gate to better reduce the S/D resistance through its fringing field, hence the higher I_{ON}.

In Chapter 3, the high performance transistors have S/D overlapped profile and relatively thicker S/D extension region so that the on-current degradation of the controllability of gate channel edge due to the lower permittivity of the spacer material is not so much. However, in the low standby power devices, the structures have S/D underlapped profile and shallow S/D extension region so that there is big on-current degradation.

This degradation is more and more severe beyond the 18nm high performance technology node and 22nm low stand-by power technology node because the shallow junction region plays a greater role. Even though the low-k spacer can achieve low gate capacitance, it decreases on current so that the speed is not much improved, if at all.

A novel corner spacer technology is introduced in this Chapter. The small highly localized high-k spacers are present only at the gate-S/D edges where they are needed to improve on-

current and off-current. The larger low-k spacer reduces the gate capacitance for improved speed and energy consumption. The high-k spacer material may be silicon nitride or HfO_2 and the low-k material may be silicon oxide or even vacuum.

4.2 Historical Background

At the long channel transistor technology node, there was no need for gate spacers. However, as the gate length is scaled, lightly doped drain (LDD) technology [4.2] was needed to improve short channel effect (SCE) or hot carrier effect. Gate spacer was needed to make LDD structure. After gate patterning, gate spacer formation is followed by shallow ion implantation (IIP). After that, deep S/D is formed by deep IIP. The gate spacer material is usually SiO_2.

As the gate length is more scaled, the gate spacer size is different to the LDD location and doping profile. In DRAM technology, dual spacer technology was introduced in order to reduce cell junction leakage current and use SAC technology. Dual spacer structure is that thin SiO_2 spacer is located besides gate pattern and thick Si_3N_4 spacer is outside the SiO_2 spacer. The merit of gate dual spacer process is less silicon consumption in the cell array. For the conventional process, severe silicon recess occurs because the silicon surface is exposed twice to etching environments during Si_3N_4 spacer formation and SAC etching processes [4.3]. This dual-sidewall spacer technology was used in metal gate process [4.4].

However, this dual spacer technology increases the gate capacitance because of higher-k of silicon nitride spacer. Figure 4.1 (a) shows that thin oxide and thick silicon nitride dual spacer transistor and Figure 4.1 (b) shows that this dual spacer technology could be applied to metal gate process. Thus, high density memory such as DRAM uses this dual spacer technology because this memory is important to the cell density and leakage current, not to the speed. In high speed device, this technology could not be used due to high gate capacitance.

Figure 4.1 (c) shows a different type of dual spacer technology. This offset spacer configuration and width can effectively increase the on-state driving current and reduce the off-state leakage current off due to the high vertical fringing electric field effect arising from the side capacitor comprising of gate spacer extension structure.

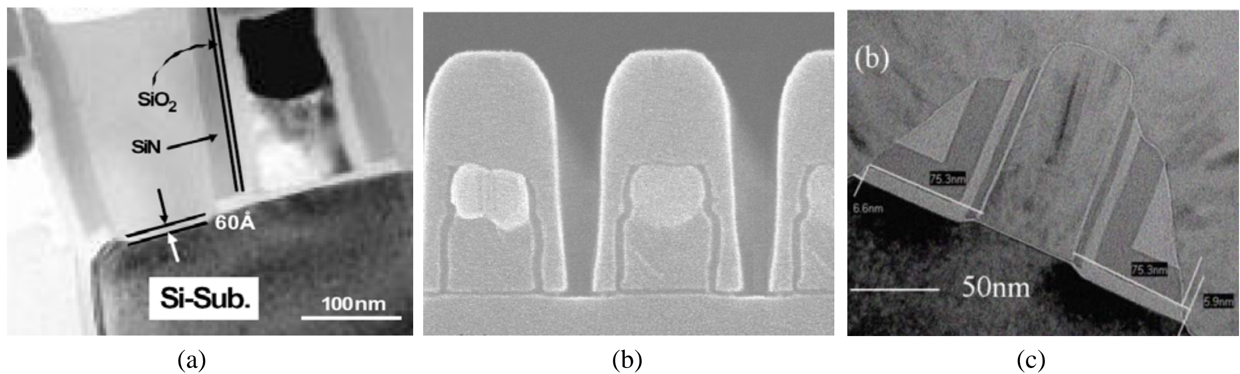


Figure 4.1: (a) Vertical view of Jaegoo's dual spacer transistor [4.3]. (6nm of SiO_2 spacer and 30nm of Si_3N_4 spacer) (b) Vertical view of Jun-Wei's dual spacer transistor with metal gate process [4.4]. Thin oxide layer covered all gate structure and thick silicon nitride covered the all gate structure and thin oxide layer. (c) Vertical view of Chun-Jen's sidewall spacer transistor [4.5].

4.3 Process Integration

4.3.1 The comparison of structures by simulation

L_{GATE}, V_{DD}, and G_{OX} follow the projections of the International Technology Roadmap for Semiconductor (ITRS) 2009 (18nm, 0.84V, and 0.55nm, respectively) [4.6]. Firstly, we made a reference transistor with conventional oxide spacers whose size is 16nm of width and 58nm of height. Except for the spacer material, all other transistors have identical design parameters such as S/D and channel doping, gate oxide thickness, and gate length. After that, corner spacer width is changed from 3nm to 16nm (full width) and corner spacer height is changed from 3nm to 58nm (full gate height). Figure 4.2 shows that some examples of different types of spacers.

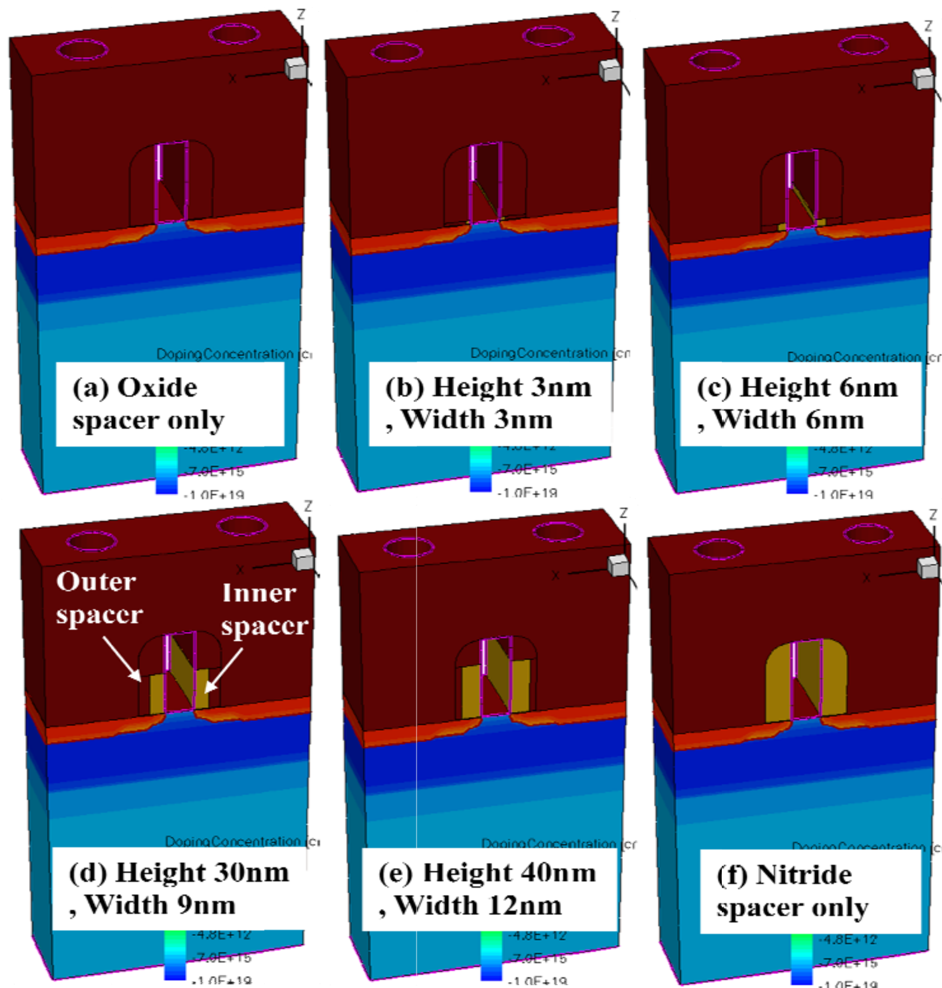


Figure 4.2: The final structures of NMOSFETs using SENTAURUS. T_{POLY} = 580Å, L_{GATE} = 18nm, contact size = 28nm, gate to contact distance = 22nm. Nitride/oxide spacer = 16nm.

4.3.2 Structure and Process Concept

The proposed general corner spacer transistor process flow is as follows. Figure 4.3 (a) shows that after gate oxidation, gate material is deposited. After gate photolithography, gate material is patterned. Sidewall is slightly oxidized. And shallow ion implantation (IIP) is carried out as shown in Figure 4.3 (b). After that, high-k corner spacer is formed as shown in Figure 4.3 (c). The width of this corner spacer is controlled by the deposition thickness of the inner spacer. The height of the corner spacer could be controlled by over etch time. Figure 4.3 (d) shows that low-k outer spacers are formed. And deep IIP is carried out to form deep S/D. After that, ILD is deposited and conventional contact process is done.

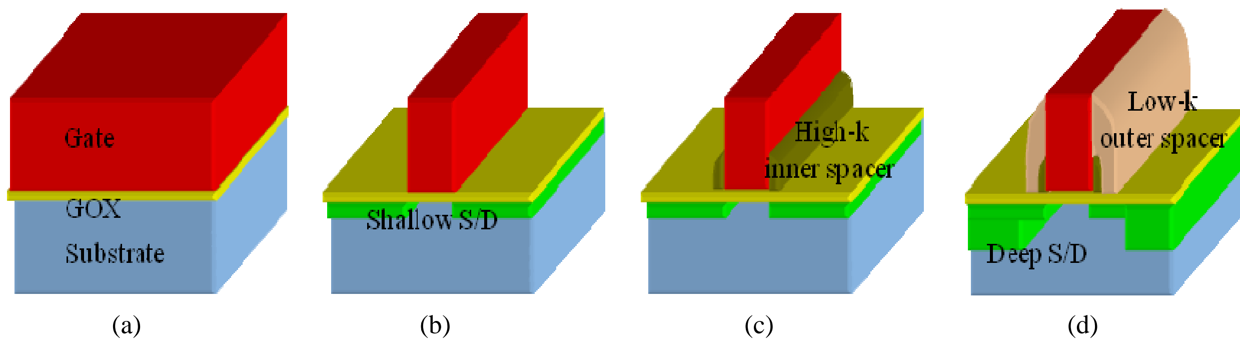


Figure 4.3: The proposed process flows for a corner spacer transistor. The corner spacer is higher-k material and the outer spacer is lower-k material. (a) Gate oxide and gate material are deposited, sequentially. (b) After gate material is etched, shallow IIP is done to form shallow S/D (c) High-k inner spacer material is deposited and etched-back. The height of the corner spacer (inner spacer) could be controlled by over etch time. (d) Low-k outer spacer material is deposited and etched-back to form the outer spacer.

Another proposed process flow for the corner spacer transistor with replacing the outer spacer with vacuum spacer is illustrated in Figure 4.4. Figure 4.4 (a) shows that the process is the same as the process of Figure 4.3 (a)-(c). Thin oxide is deposited in order to protect the gate material and high-k inner spacers. Figure 4.4 (b) shows that sacrificial spacer is formed. Sacrificial material may be silicon nitride and porous silicon which can be easily removed by hot phosphoric acid and a dilute hydroxide solution as low as 1% as illustrated in Chapter 2. Figure 4.4 (c) shows that ILD is deposited and etched back in order to planarize the surface and expose the top of the gate material. Figure 4.4 (d) shows that ILD is etched back a little bit to expose the top of the sacrificial spacer. Figure 4.4 (e) shows that wet-etching has selectively removed the sacrificial spacers to create the vacuum gaps. Because the top openings of the vacuum gaps are smaller than the bottom of the vacuum gaps, they can be easily sealed during non-conformal ILD2 deposition as shown in Figure 4.4 (f). The width of the vacuum pockets is easily controlled by changing the thickness of the sacrificial spacer. After that, conventional contact process is followed.

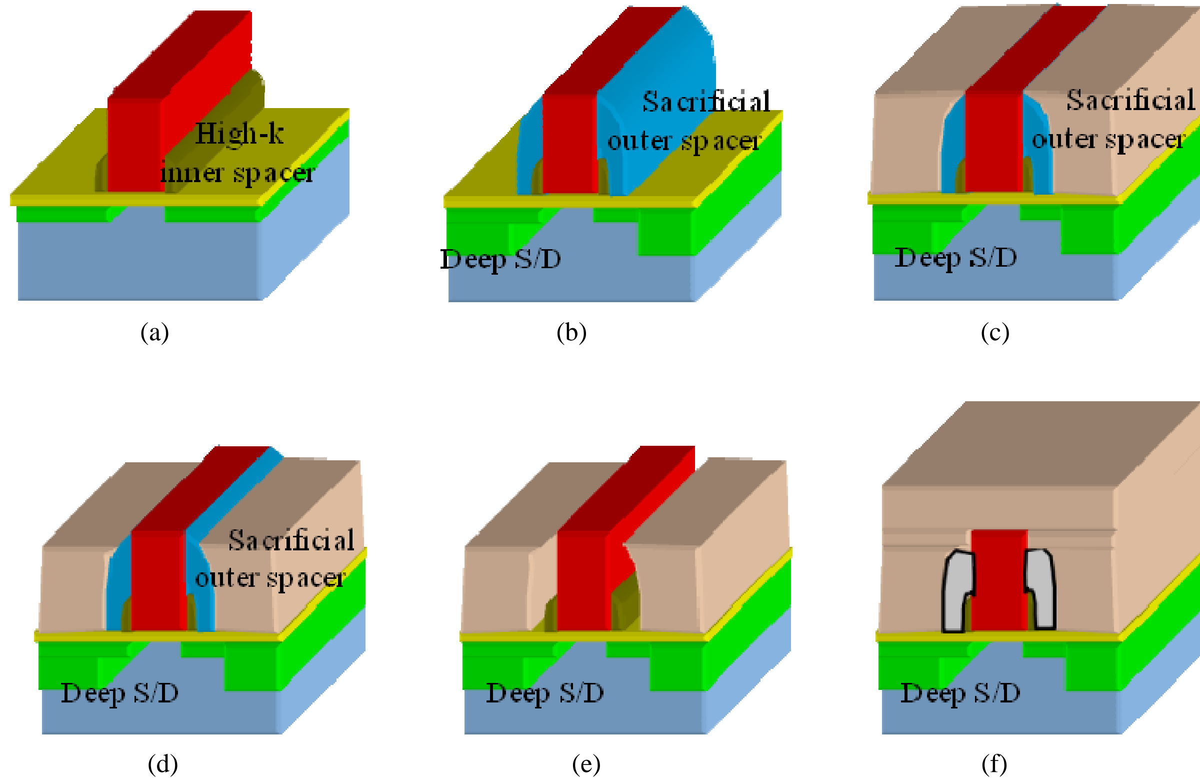


Figure 4.4: The proposed process flows for a corner spacer with vacuum outer spacer transistor. (a) All the process flow are the same as Figure 4.3 (a)-(c). After high-k corner spacer is formed, thin oxide is deposited to protect the gate material and the corner spacer. The thin oxide is not shown in this figure. (b) Sacrificial outer spacer material (silicon nitride) is deposited and etched-back to form the outer spacer. Deep S/D is formed by deep IIP. (c) After ILD is deposited, oxide CMP is carried out to expose the top of the gate material. (d) ILD is etched back to expose the top of the sacrificial spacer. (e) The sacrificial spacers are removed. (f) Non-conformal ILD2 is deposited to seal the vacuum gaps.

4.4 Simulation Results

4.4.1 A corner spacer transistor in high performance devices

The doping profile of high performance device is much different than that of low stand-by power device. The corner spacer effect is also different with this doping profile difference. Firstly, we made a reference transistor with oxide spacers only. The parameters of this transistor are followed by the high performance devices of ITRS 2009 [4.6]. And then, high-k inner spacer and low-k outer spacer are changed. The combinations of these spacers are here: (Si_3N_4 and SiO_2), (HfO_2 and SiO_2), (HfO_2 and Si_3N_4), (SiO_2 and vacuum), (Si_3N_4 and vacuum), and (HfO_2 and vacuum). In order to analyze these phenomenon easily, the corner spacer whose inner and outer spacers are Si_3N_4 and SiO_2, respectively, is analyzed, firstly.

4.4.1.1 A simple corner spacer transistor with silicon nitride and oxide

The electrical characteristics of transistors are simulated with Sentaurus 3D device simulator [4.7]. Figure 4.5 shows that the I_{DS}-V_{GS} characteristics of the oxide spacer (control) device meet the ITRS 2009 specifications. The on-current is 1.58mA/µm (ITRS: 1.58mA/µm) and the off-current is below 20nA/µm (ITRS: <100nA/µm). The corner spacer transistors are made by inserting corner spacers of varying size to this transistor. Except for the corner spacer size, all transistors have identical design parameters such as S/D and channel doping as the control device. The PMOSFETs have the same structures as the NMOSFETs except for the dopant types.

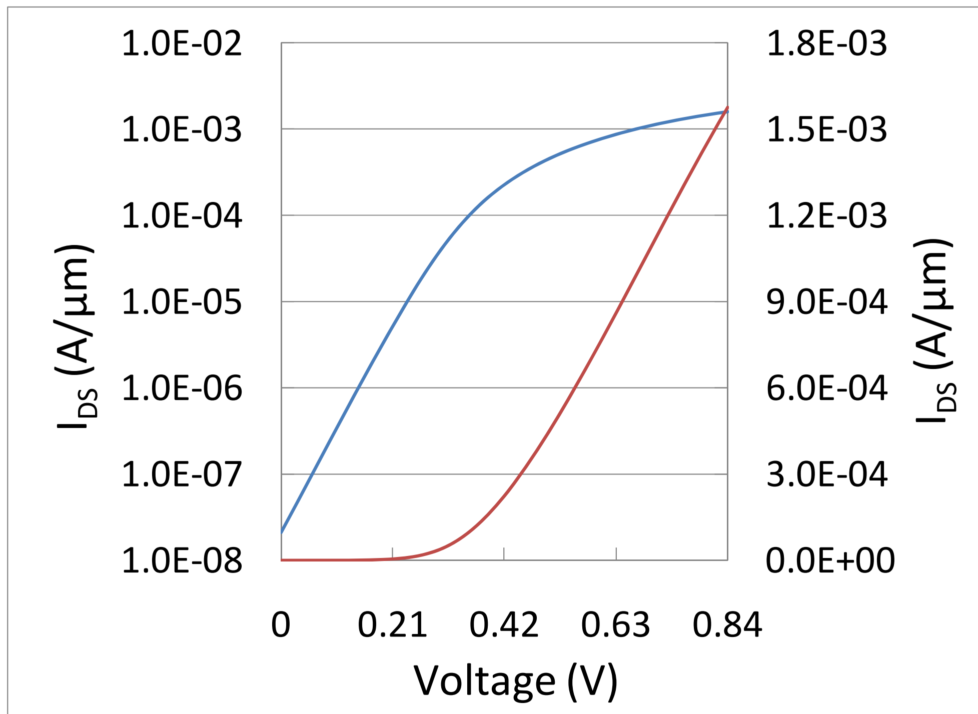


Figure 4.5: Simulated I_{DS}-V_{GS} characteristics of the control transistor (oxide spacer only) in high performance devices (V_{DS} = 0.84V, V_{DD}=0.84V, L_{GATE}=18nm)

The corner high-k material is Si_3N_4 (k=7.9) and the outer low-k material is SiO_2 (k=3.9). The conventional transistor with oxide spacer only is compared with the corner spacers and nitride spacer transistors. The total outer spacer size is fixed at 16nm width and 58nm height. The corner spacer widths varies from 0nm (oxide spacer), 3, 6, 9, 12, 15, and 16nm and the heights varies from 3nm to 58nm.

Figure 4.6 shows the on-current of the nitride spacer transistor is larger than oxide spacer transistor, also as expected, because of the stronger control of gate over the channel-S/D edge region. The on-current of the nitride spacer transistor is increased by 3.8% compared to that of the oxide spacer transistor. Surprisingly, the on-current of the corner spacer transistors, even with a modest width, is just as high as or even higher than that of the totally nitride spacer transistor. In the same corner spacer height, the on-current of 9nm corner spacer width is higher than that of 16nm corner spacer width. We have found that the critical location in the shallow S/D that

requires good gate coupling is the gate edge region, where the doping concentration is lower and the current density is higher (being adjacent to the thin inversion layer) than the rest of the S/D region. A narrow high-k corner spacer increases the gate coupling (the gate-induced vertical electric field) in this critical region over the case of a full-width nitride spacer.

The off-current of the nitride spacer transistor is reduced by 7.7% compared to that of the oxide spacer transistor. The higher permittivity of the spacer material makes the gate fringing field over the channel edge much controllable so that it makes the off-current lower. The optimum corner spacer width is 6nm for off-current aspect.

Figure 4.7 shows the vertical field in the critical corner region of a 9nm corner spacer transistor is higher than that of full width transistor as shown in Figure 4.7 (a) and (b). The corner spacer heights are all 6nm. This yields a lower resistance in the corner spacer transistor than the full-width corner spacer transistor. Figure 4.7 (c) shows that the lower resistance at the gate edge of the source leads to a lower IR drop between x=-0.015um and x=-0.01um. Thus, the resistance of source side of 9nm width of the corner spacer is smaller than that of 16nm width (full width) of the corner spacer so that the current of the 9nm width is higher than that of 16nm width.

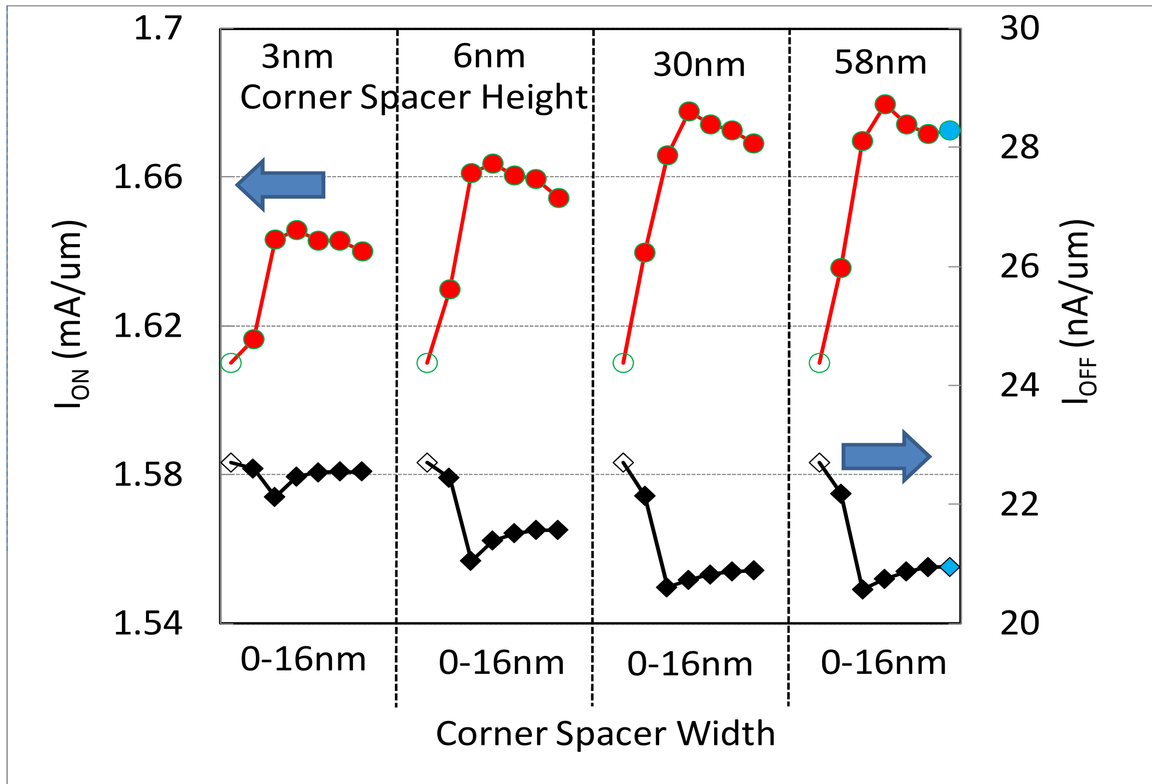
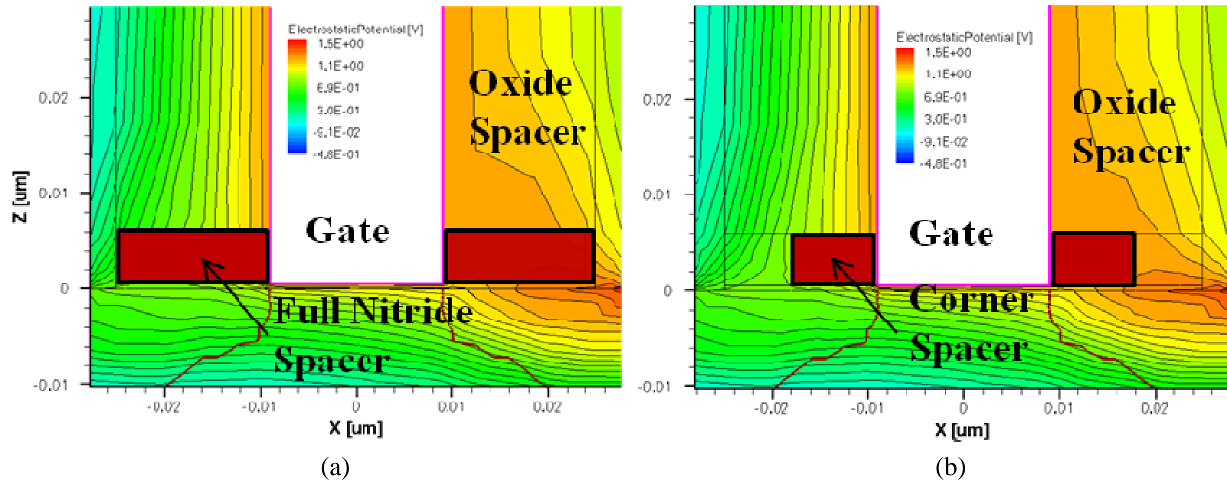
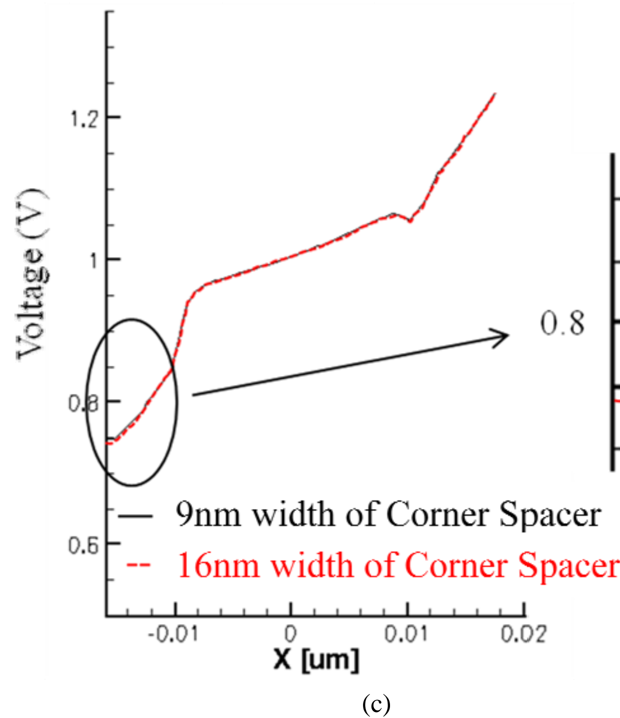


Figure 4.6: Simulated on and off-current of all the splits. X axis is the width of corner spacer from 0 to 16nm. 0nm indicates all oxide spacer and 16nm indicates the full width of the outer spacer width. Blank and blue symbols represent oxide spacer only and nitride spacer only, respectively. The corner spacer heights are separated by 4 regions: (3nm, 6nm, 30nm, and 58nm).



(a) (b)



(c)

Figure 4.7: The comparison of the electric potential in two transistors. (a) Contour plot of transistor with 16nm all nitride spacer. (b) Contour plot of transistor with 9nm nitride corner spacer. (c) The electric potential at the semiconductor/dielectric interfaces of the two transistors.

Figure 4.8 shows the gate capacitance (at V_{DS}=0V) increases as the corner spacer width or height increases as expected. The gate capacitance of 16nm corner spacer width are increased by 0.7%, 2.2%, 6.5%, and 9.5% compared to that of 0nm corner spacer width (oxide spacer only) at each corner spacer height: (3nm, 6nm, 30nm, and 58nm, respectively). The gate capacitance increases much more than on-current with increasing spacer width. Even though the on-current of nitride spacer is higher than that of oxide spacer, the delay which is simply calculated (CV/I) is longer since the higher gate capacitance. However, this simple calculation is not accurate because it is not the real inverter delay.

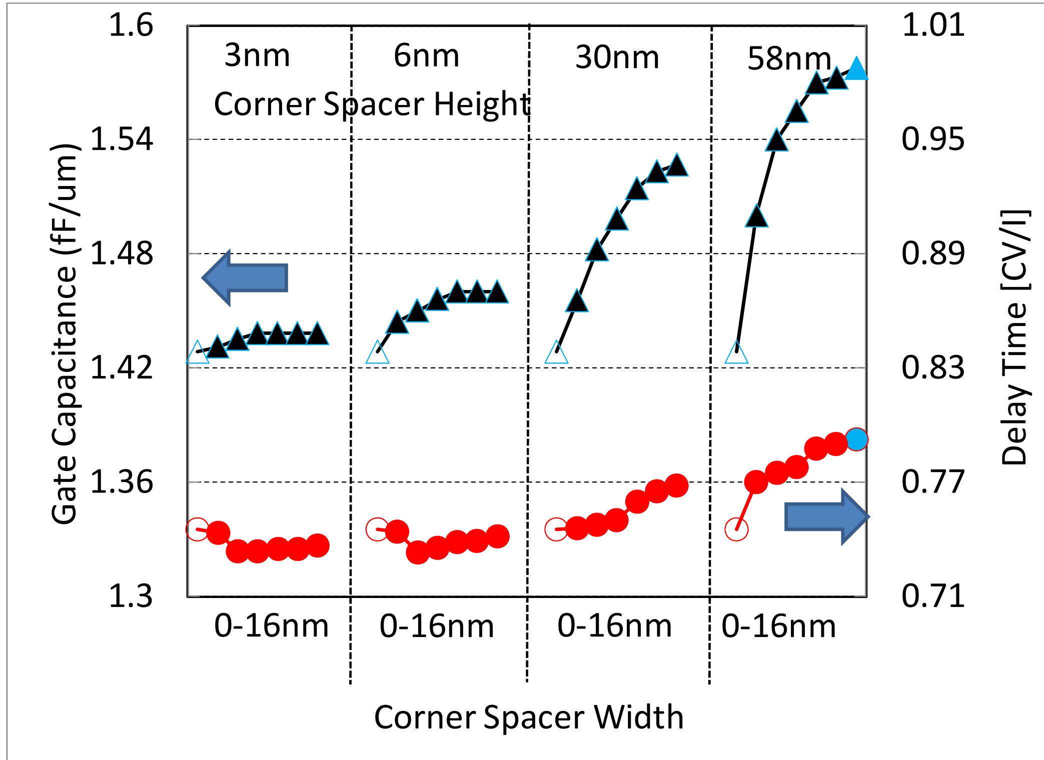


Figure 4.8: Simulated gate capacitance and CV/I of all the splits. X axis is the width of corner spacer from 0 to 16nm. 0nm indicates all oxide spacer and 16nm indicates the full width of the outer spacer width. Blank and blue symbols represent oxide spacer only and nitride spacer only, respectively. The corner spacer heights are separated by 4 regions (3nm, 6nm, 30nm, and 58nm).

In order to compare the device performance, 3D mixed-mode simulation is used to extract the accurate delay time. A four stage inverter is simulated with 3D Sentaurus simulator at V_{DD}=0.84V. The NMOSFETs have 56nm channel width and the PMOSFETs, 112nm channel width. The inverter delay is defined as the average of the pull-up and pull-down delays measured from V_{IN}=0.42V and V_{OUT}=0.42V. Even though the highest on-current is for 9nm width of corner spacer, 6nm width of corner spacer inverter is faster than 9nm width of corner spacer in the 4 stage inverter delay simulation because of the gate capacitance of both NMOSFET and PMOSFET. In Figure 4.9, solid triangle, square, and circle represent oxide spacer only, nitride spacer only, and corner spacer, respectively. Red and black represent delay time and inverter switching energy, respectively. 58nm column shows conventional dual spacer structure which has 6nm width nitride spacer with full height and 10nm width oxide spacer with full height. The delay of the corner spacer inverter with 6nm width and 6nm height is improved by 9% and 18% compared with that of oxide and nitride spacer inverters, respectively as shown in Figure 4.9. The inverter switching energy of the nitride spacer and the oxide spacer are increased by 30% and 13%, respectively compared to that of the optimal corner spacer inverter.

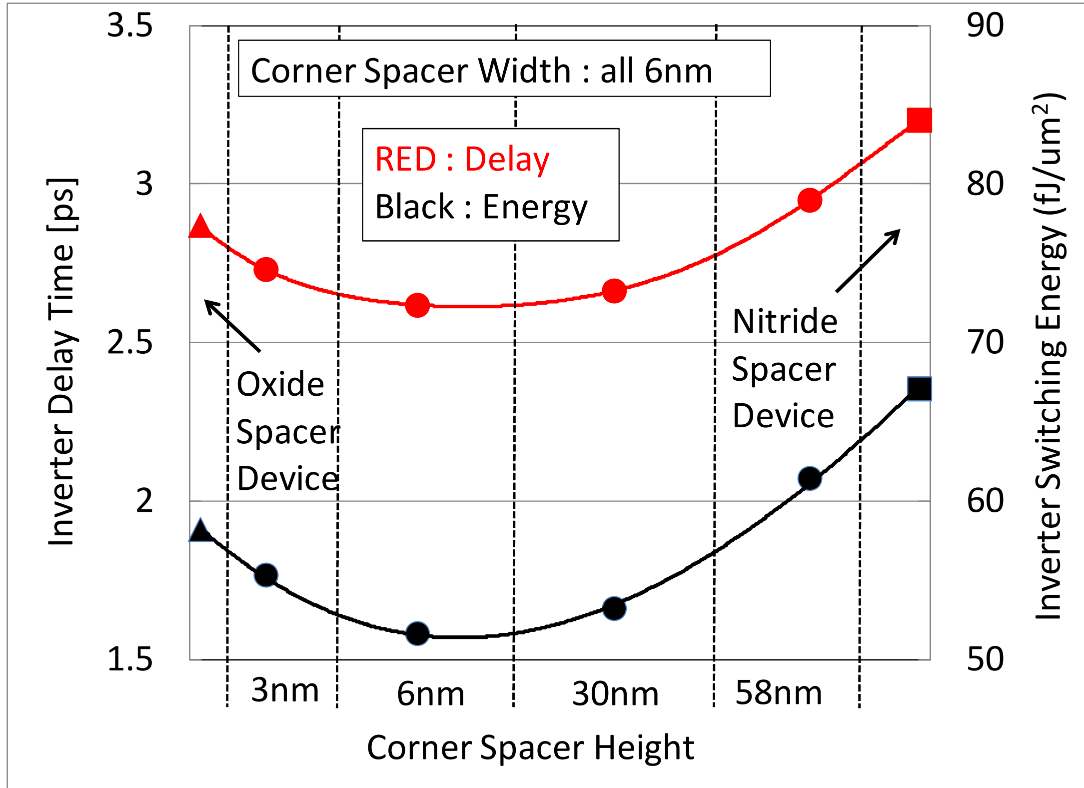


Figure 4.9: The 3D mixed-mode simulation results show the corner spacer device is faster than oxide spacer or nitride spacer devices or oxide/nitride double spacers of the same height.

4.4.1.2 Corner spacer transistors with other materials

High-k inner spacer and low-k outer spacer are changed. The combinations of these spacers are here: (Si_3N_4 and SiO_2), (HfO_2 and SiO_2), (HfO_2 and Si_3N_4), (SiO_2 and vacuum), (Si_3N_4 and vacuum), and (HfO_2 and vacuum). In Figure 4.10, the on-current is increased with increasing corner spacer width and height. The on-current of vacuum, oxide, nitride, and hafnium oxide spacer transistor are 1.53mA/μm, 1.61mA/μm, 1.67mA/μm, and 1.77mA/μm, respectively. Vacuum spacer transistor has low on-current but hafnium oxide spacer transistor has high on-current. In the combination of HfO_2 and vacuum spacers, only 3nm width and height corner spacer transistor has higher on-current than that of nitride spacer only transistor. The on-current is increased by 10% compared to that of vacuum spacer transistor. In the combination of HfO_2 and oxide spacers, small portion of corner spacer transistor has higher on-current than that of nitride spacer only transistor.

The off-current of vacuum, oxide, nitride, and hafnium oxide spacer transistor are 25nA/μm, 22.7nA/μm, 20.9nA/μm, and 17.7nA/μm, respectively. Vacuum spacer transistor has high off-current but hafnium oxide spacer transistor has low off-current. The small portion (3nm width and 3nm height of hafnium oxide) of corner spacer transistor can decrease the off-current by 19% compared to that of vacuum spacer transistor.

In all the combination of inner and outer spacers, 9nm width of corner spacer transistor has higher on-current compared to other spacer widths at the same height of corner spacer but 6nm width of corner spacer transistor has lower off-current compared to other spacer with the same height of corner spacer.

Figure 4.11 shows the gate capacitance (at V_{DS}=0V) of all the splits. The capacitances increase as the corner spacer width or height increases as expected. The capacitances of vacuum, oxide, nitride, and hafnium spacer transistors are 1.268fF/μm, 1.428fF/μm, 1.575fF/μm, and 1.964fF/μm, respectively. The capacitance of the oxide, nitride, and hafnium oxide spacer transistors are increased by 12.6%, 24.2%, and 54.9%, respectively, compared to that of vacuum spacer transistor. When the portion of the corner spacer is increased, the on-current of the transistor is increased but the capacitances are also increased. Thus, the delay of each transistor is very complicated to be calculated.

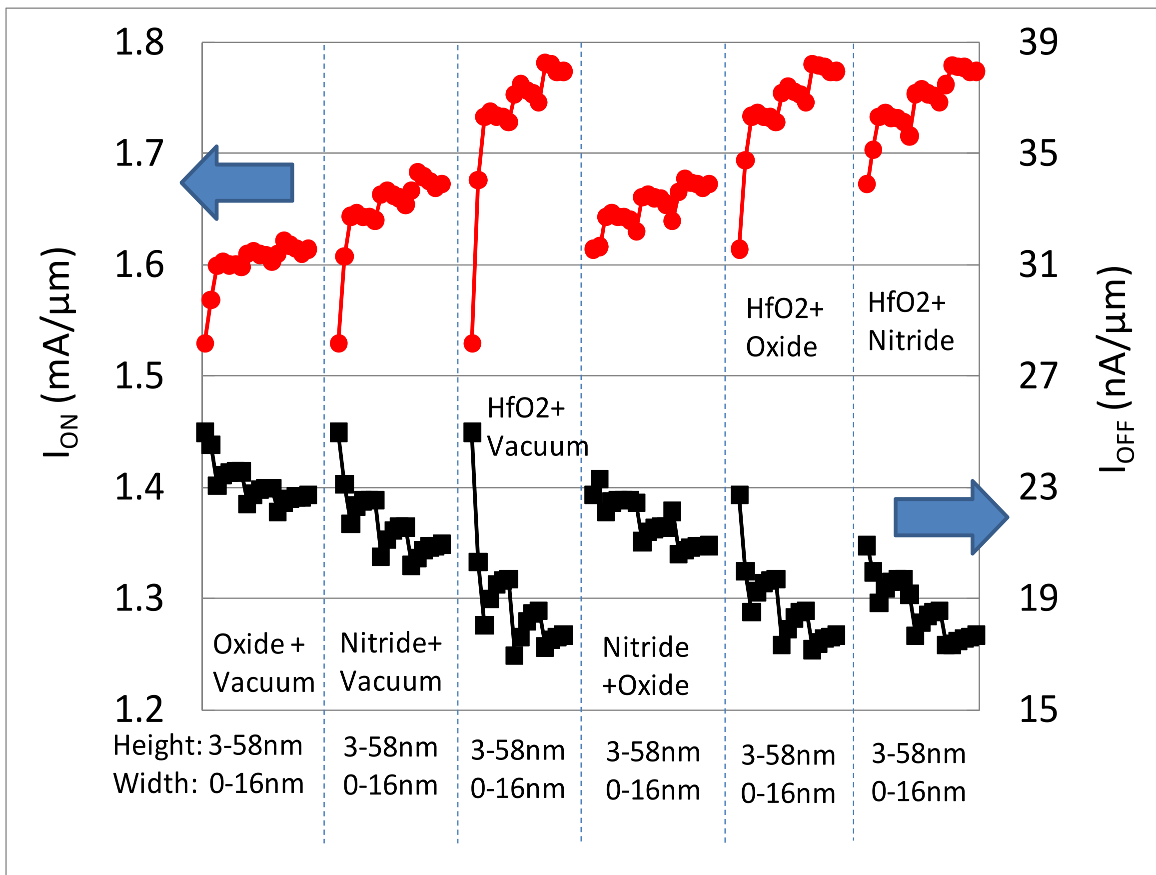


Figure 4.10: Simulated on and off-current of all the splits. There are six combinations of corner spacers. The column of the nitride and oxide is the same as Figure 4.6. X axis are the width of corner spacer from 0 to 16nm and the height of corner spacer from 3 to 58nm. The left side of the each column represents lower dielectric spacer only and the right side of the column indicates higher dielectric spacer only.

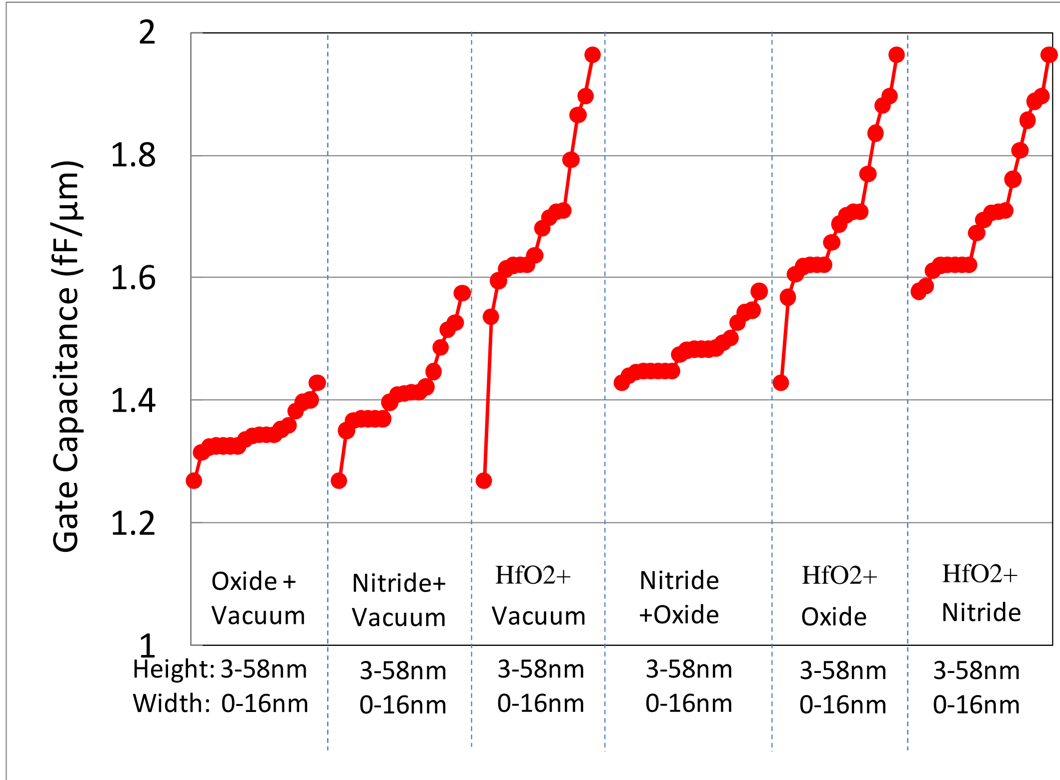


Figure 4.11: Simulated gate capacitances of all the splits. X axis is the width of corner spacer from 0 to 16nm and the height from 3 to 58nm. The left side of the each column represents lower dielectric spacer only and the right side of the column indicates higher dielectric spacer only.

In order to compare the device performance, 3D mixed-mode simulation is used to extract the accurate delay time and inverter switching energy. A four stage inverter is simulated with 3D Sentaurus simulator at V_{DD}=0.84V. All the simulation parameters except material are exactly same as the parameters of Figure 4.9.

In the speed aspect, the delay times of vacuum, oxide, nitride, and hafnium oxide spacers are 2.71ps, 2.87ps, 3.23ps, and 3.86ps, respectively as shown in Figure 4.12. Even if on-current of hafnium oxide spacer is higher than those of other spacers, vacuum spacer inverter is faster than other spacer inverters due to gate capacitances. If the difference of the dielectric constants between corner spacer material and outer spacer material is bigger, the effect of the corner spacer is smaller because the gate capacitance is much increased compared to the improvement of on-current. The interesting results are here. The combination of silicon oxide and silicon nitride can be improved as much as the combination of vacuum and oxide (or nitride). Since vacuum corner spacer process is extremely difficult, the corner spacer with silicon oxide and nitride can be an attractive solution in order to enhance the speed.

In inverter switching energy aspect, the energy of vacuum, oxide, nitride, and hafnium oxide spacers are 48.6fJ, 58.2fJ, 67.1fJ, and 90.3fJ, respectively. When the dielectric constant is increased, the energy is also increased. The corner spacer inverter can be helpful to decrease the energy. However, the energy of vacuum spacer is the lowest energy of all the splits.

In high performance devices, we have some options to improve the performances. If we want to improve power consumption, the vacuum spacer may be an excellent solution. If we want fast

switching speed, we can choose the corner spacer structure. When we consider both high speed and low power consumption, we may choose the vacuum spacer transistor or the corner spacer transistor whose materials are vacuum and silicon oxide.

.

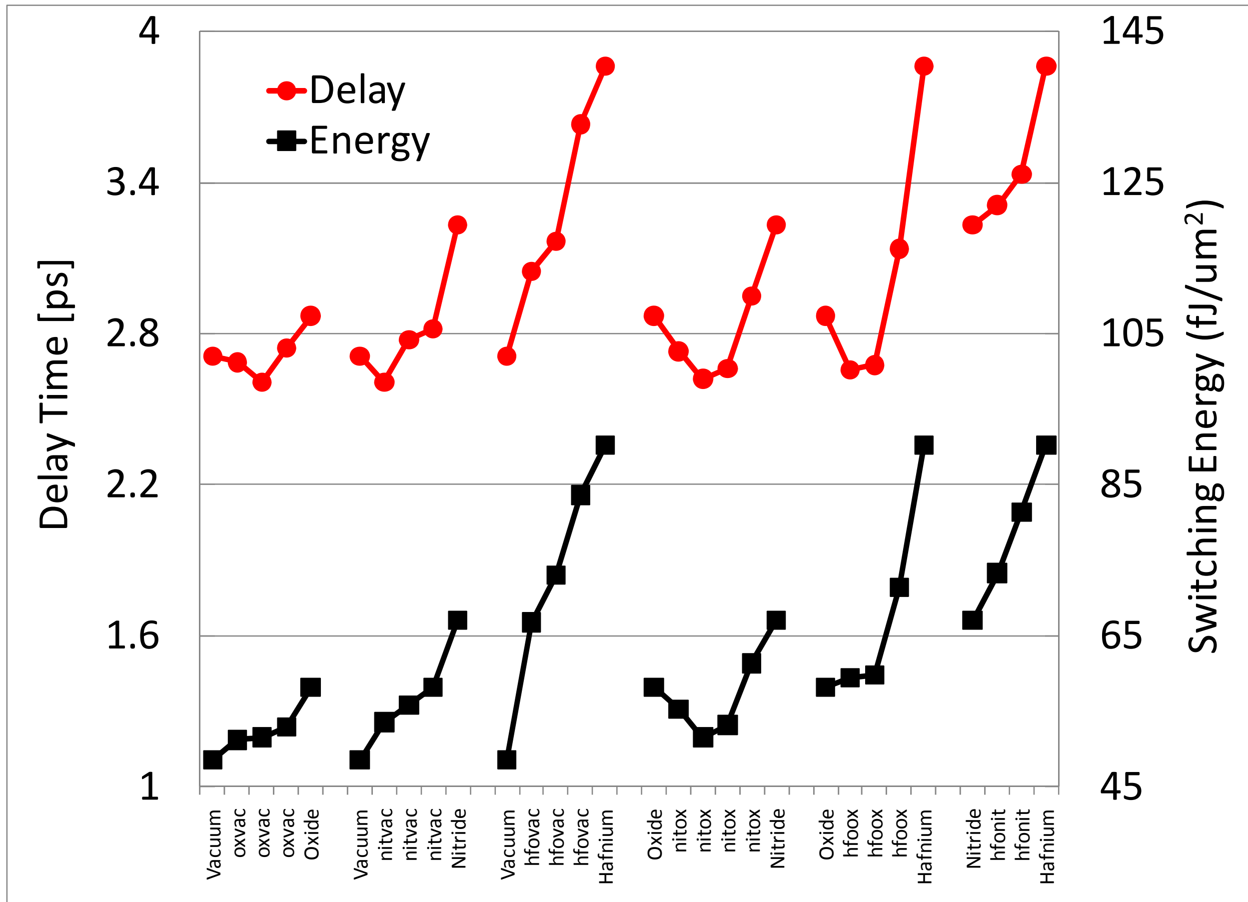


Figure 4.12: The 3D mixed-mode simulation results of all the splits. There are six combinations of corner spacers. Vacuum, oxide, nitride, and hafnium represent conventional spacer structure whose material is changed. Other notations are all corner spacer structures. For example, oxvac means corner spacer material is silicon oxide and outer spacer material is vacuum.

4.4.2 A corner spacer transistor for low stand-by power devices

The corner spacer effect in low stand-by power device is supposed to be much higher than that in high performance device because of the underlapped S/D profiles and very thin S/D thickness. We can increase the on-current more easily using the vertical field of the spacer materials. Thus, we made a reference transistor with oxide spacers only. The parameters of this transistor follow the low stand-by power devices of ITRS 2009 [4.6]. And then, high-k inner spacer and low-k outer spacer are changed. The combinations of these spacers are here: (Si_3N_4 and SiO_2), (HfO_2 and SiO_2), (HfO_2 and Si_3N_4), (SiO_2 and vacuum), (Si_3N_4 and vacuum), and (HfO_2 and vacuum). In order to analyze these phenomenon easily, the corner spacer whose inner and outer spacers are Si_3N_4 and SiO_2, respectively, is analyzed, firstly. The sequences of the low stand-by power devices are exactly same as those of the high performance devices.

4.4.2.1 A simple corner spacer transistor with silicon nitride and oxide

The electrical characteristics of transistors are simulated with Sentaurus 3D device simulator [4.7]. Figure 4.13 shows that the I_{DS}-V_{GS} characteristics of the oxide spacer (control) device meet the ITRS 2009 specifications. The on-current is 605µA/µm (ITRS: 600µA/µm) and the off-current is below 12.8pA/µm (ITRS: <50pA/µm). The corner spacer transistors are made by inserting corner spacers of varying size to this transistor. Except for the corner spacer size, all transistors have identical design parameters such as S/D and channel doping as the control device. The PMOSFETs have the same structures as the NMOSFETs except for the dopant types.

The corner high-k material is Si_3N_4 (k=7.9) and the outer low-k material is SiO_2 (k=3.9). The conventional transistor with oxide spacer only is compared with the corner spacers and nitride spacer transistors. The total outer spacer size is fixed at 16nm width and 58nm height. The corner spacer widths varies from 0nm (oxide spacer), 3, 6, 9, 12, 15, and 16nm and the heights varies from 3nm to 58nm.

Figure 4.14 shows the on-current of the nitride spacer transistor is larger than oxide spacer transistor, the same as for the high performance device. The on-current of the nitride spacer transistor is increased by 11% compared to that of the oxide spacer transistor. However, the improvement of the high performance device is only 3.8%. In the same corner spacer height, the on-current of 9nm corner spacer width is higher than that of 16nm corner spacer width. A narrow high-k corner spacer increases the gate coupling (the gate-induced vertical electric field) in this critical region over the case of a full-width nitride spacer which is the same as in high performance devices. But the improvement of corner spacer transistor of low stand-by power device is much higher than that of high performance device because of the underlapped and very thin S/D profiles.

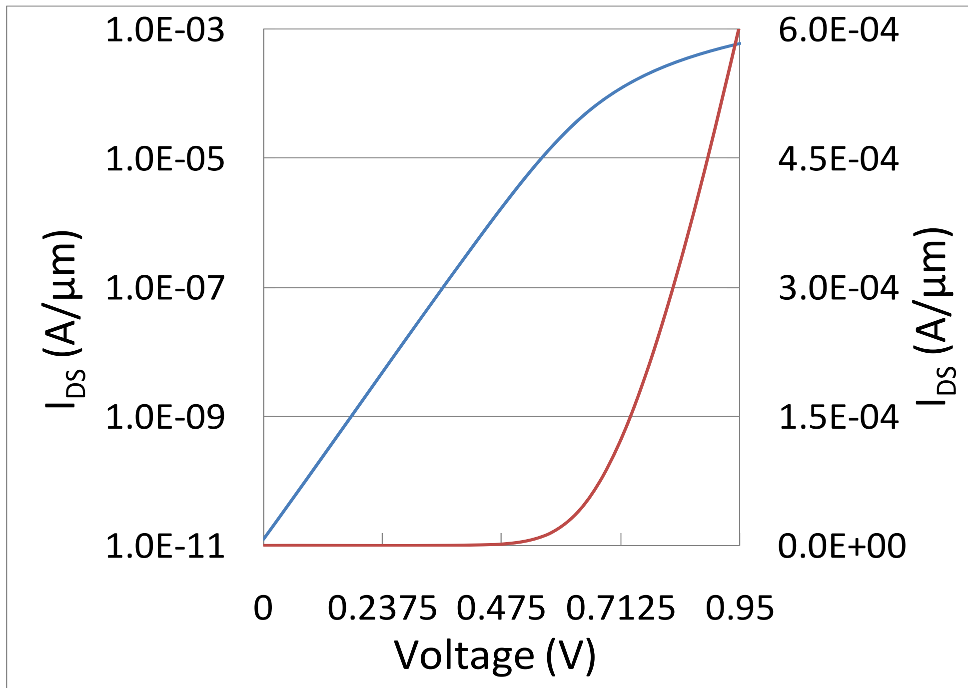


Figure 4.13: Simulated I_{DS}-V_{GS} characteristics of the control transistor (oxide spacer only) in low stand-by power devices. (V_{DS} = 0.95V, V_{DD}=0.95V, L_{GATE}=18nm)

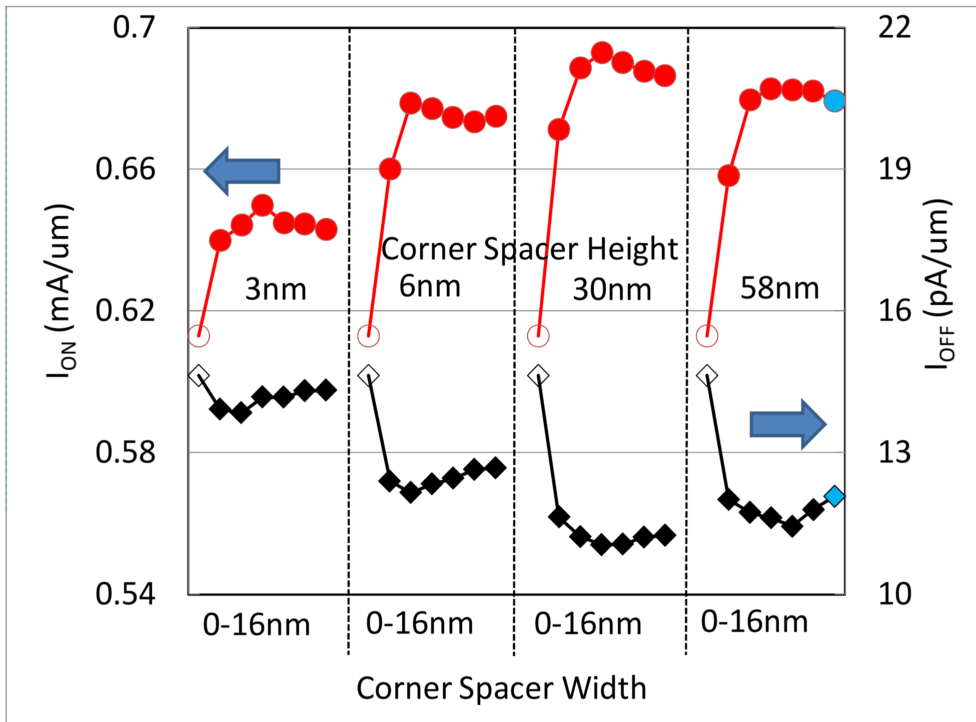


Figure 4.14: Simulated on and off-current of all the splits. X axis is the width of corner spacer from 0 to 16nm. 0nm indicates all oxide spacer and 16nm indicates the full width of the outer spacer width. Blank and blue symbols represent oxide spacer only and nitride spacer only, respectively. The corner spacer heights are separated by 4 regions: (3nm, 6nm, 30nm, and 58nm).

The off-current of the nitride spacer transistor is reduced by 17.4% compared to that of the oxide spacer transistor. However, the improvement of the high performance device is only 7.7%. The static power consumption of the oxide spacer transistor is calculated by $V_{DD}I_{LEAK}$ (0.95Vx14.6pA/μm = 13.9pW/μm). When V_{DD} can be reduced at the same on-current of the oxide spacer transistor, the static power consumption of the corner spacer transistor (6nm of width and height) is 0.924Vx12.15pA/μm = 11.23pW/μm. The power can be decreased by 19.2%. When the work function is shifted, the off current of this corner spacer transistor is 6.79pA/μm at the same on-current of the oxide spacer transistor. The power is 0.95Vx6.79pA/μm = 6.44pW/μm. The power can be reduced by 53.7%. For the only static power aspect, the change of the work function is more useful, however, for the both static and dynamic power aspects, the reduction of V_{DD} is more useful.

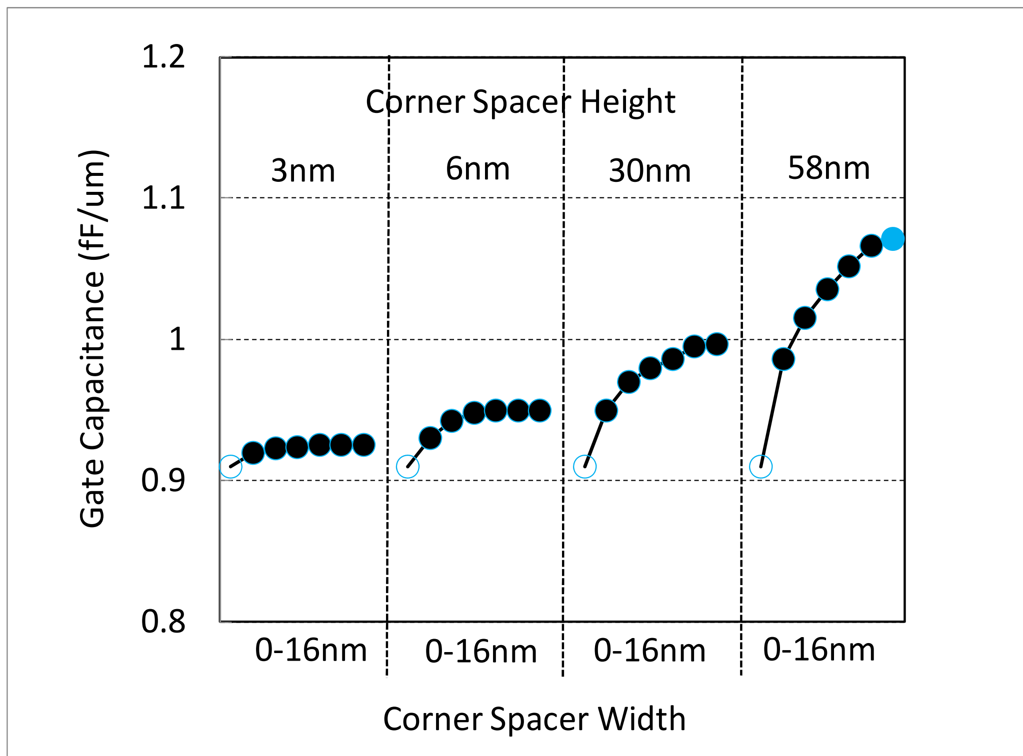


Figure 4.15: Simulated gate capacitance of all the splits. X axis is the width of corner spacer from 0 to 16nm. 0nm indicates all oxide spacer and 16nm indicates the full width of the outer spacer width. Blank and blue symbols represent oxide spacer only and nitride spacer only, respectively.

Figure 4.15 shows the gate capacitance (at V_{DS}=0V) increases as the corner spacer width or height increases as expected. The gate capacitance of 16nm corner spacer width are increased by 2%, 6.9%, 18.6%, and 27.6% compared to that of 0nm corner spacer width (oxide spacer only) at each corner spacer height: (3nm, 6nm, 30nm, and 58nm, respectively). The effect of increasing the gate capacitance in the low stand-by power device is much higher than that in the high performance device.

In order to compare the device performance, 3D mixed-mode simulation is used to extract the accurate delay time. A four stage inverter is simulated with 3D Sentaurus simulator at

V_{DD}=0.95V. The NMOSFETs have 56nm channel width and the PMOSFETs, 112nm channel width. The inverter delay is defined as the average of the pull-up and pull-down delays measured from V_{IN}=0.475V and V_{OUT}=0.475V. Figure 4.16 shows the delay and switching power of the oxide, nitride, and some corner spacer transistors. In the low stand-by power device, the oxide spacer transistor has low on-current and low gate capacitance but the nitride spacer transistor has high on-current and high gate capacitance, thus the delays are almost the same. The delay time of the corner spacer transistor with 6nm of height is improved by 15% compared to that of the oxide spacer transistor. In the high performance devices, the effect of the corner spacer transistor is only 10% for the speed aspect. The inverter switching energy of the corner spacer transistor with 3nm of height is improved by 7% compared to that of the oxide spacer transistor. In the high performance devices, the best performance can be achieved at 6nm width of the corner spacer. However, the best performance in the low stand-by power devices can be achieved at 3nm, 6nm of corner spacer width.

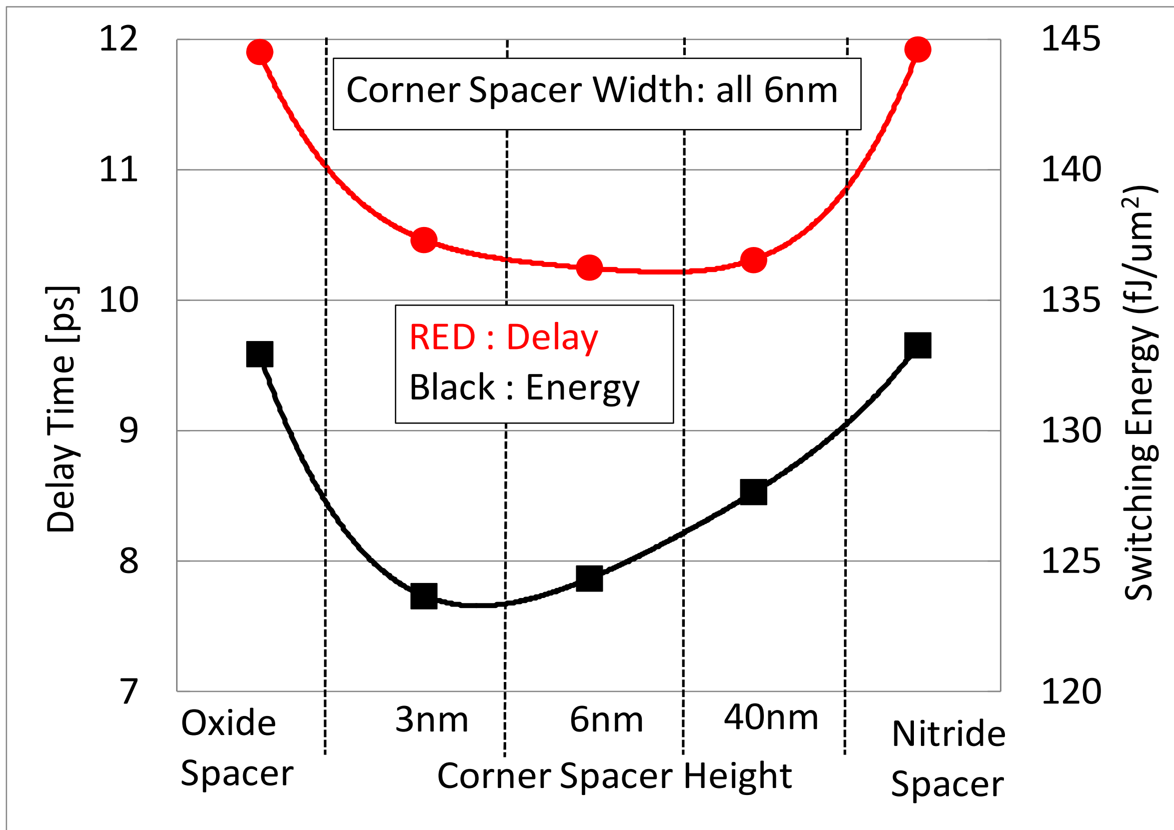


Figure 4.16: The 3D mixed-mode simulation results show the corner spacer device is faster than oxide spacer or nitride spacer devices.

4.4.2.2 Corner spacer transistors with other materials

High-k inner spacer and low-k outer spacer are changed. The combinations of these spacers are here: (Si_3N_4 and SiO_2), (HfO_2 and SiO_2), (HfO_2 and Si_3N_4), (SiO_2 and vacuum), (Si_3N_4 and vacuum), and (HfO_2 and vacuum). In Figure 4.17, the on-current is increased with increasing corner spacer width and height. The on-current of vacuum, oxide, nitride, and hafnium oxide spacer transistor are 0.5mA/μm, 0.613mA/μm, 0.679mA/μm, and 0.797mA/μm, respectively. Vacuum spacer transistor has low on-current but hafnium oxide spacer transistor has high on-current. In the combination of hafnium oxide and vacuum spacers, only 3nm width and height corner spacer transistor has higher on-current than that of nitride spacer only transistor. The on-current is increased by 40% compared to that of vacuum spacer transistor. In the combination of hafnium oxide and oxide spacers, small portion of corner spacer transistor has higher on-current than that of nitride spacer only transistor.

The off-current of vacuum, oxide, nitride, and hafnium oxide spacer transistor are 16.1pA/μm, 14.6pA/μm, 12.1pA/μm, and 7.33pA/μm, respectively. Vacuum spacer transistor has high off-current but hafnium oxide spacer transistor has low off-current. The small portion (3nm width and 3nm height) of corner spacer transistor with hafnium oxide and vacuum can decrease the off-current by 34% compared to that of vacuum spacer transistor.

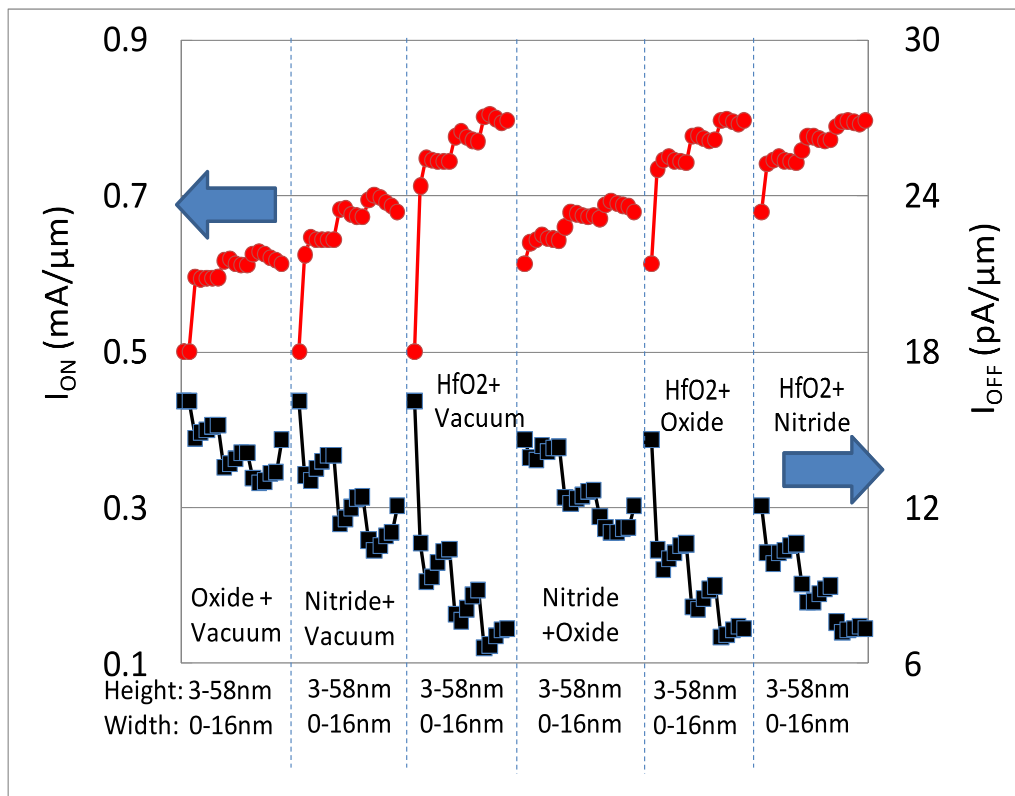


Figure 4.17: Simulated on and off-current of all the splits. There are six combinations of corner spacers. The column of the nitride and oxide is the same as Figure 4.14. X axis are the width of corner spacer from 0 to 16nm and the height of corner spacer from 3 to 58nm. The left side of the each column represents lower dielectric spacer only and the right side of the column indicates higher dielectric spacer only.

In all the combination of inner and outer spacers, 3-9nm widths of corner spacer transistor has higher on-current compared to other spacer widths at the same height of corner spacer but 3-9nm widths of corner spacer transistor has lower off-current compared to other spacer with at the same height of corner spacer.

Figure 4.18 shows the gate capacitance (at V_{DS}=0V) of all the splits. The capacitances increase as the corner spacer width or height increases as expected. The capacitances of vacuum, oxide, nitride, and hafnium oxide spacer transistors are 0.786fF/μm, 0.91fF/μm, 1.07fF/μm, and 1.375fF/μm, respectively. The capacitance of the oxide, nitride, and hafnium oxide spacer transistors are increased by 28.5%, 51.1%, and 74.9%, respectively, compared to that of vacuum spacer transistor. However, the gate capacitance of low stand-by power device is much lower than that of the high performance device because of thicker gate oxide thickness. And the change of the gate capacitance with increasing the portion of corner spacer is much higher than that of high performance device.

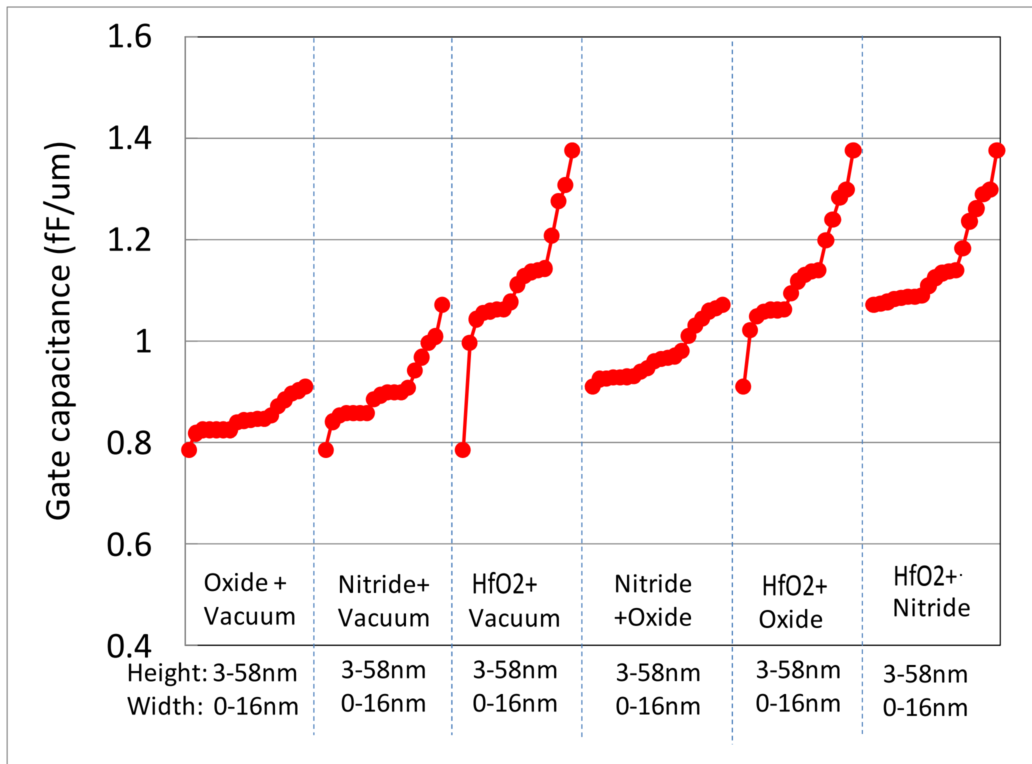


Figure 4.18: Simulated gate capacitances of all the splits. X axis is the width of corner spacer from 0 to 16nm and the height from 3 to 58nm. The left side of the each column represents lower dielectric spacer only and the right side of the column indicates higher dielectric spacer only.

In order to compare the device performance, 3D mixed-mode simulation is used to extract the accurate delay time and inverter switching energy. A four stage inverter is simulated with 3D Sentaurus simulator at V_{DD}=0.95V. All the simulation parameters except material are exactly same as the parameters of Figure 4.16.

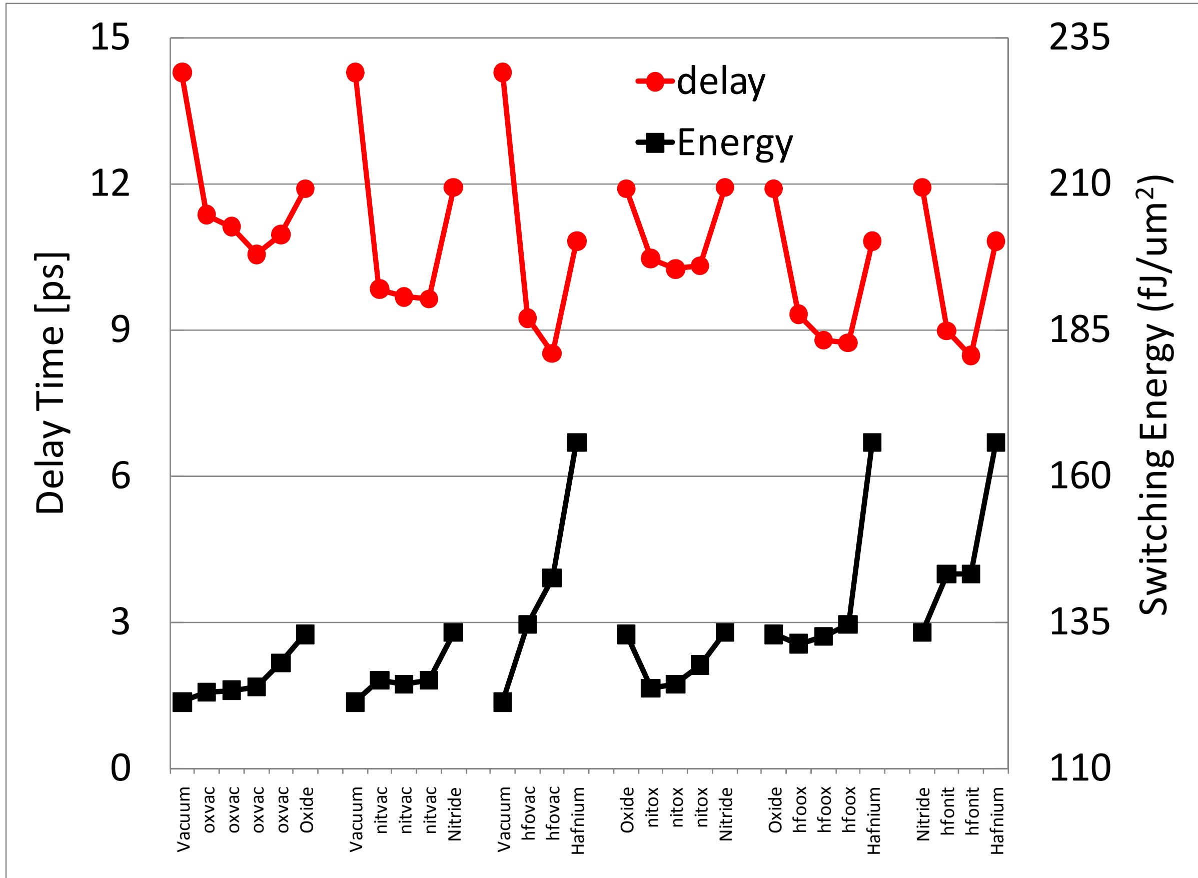


Figure 4.19: The 3D mixed-mode simulation results of all the splits. There are six combinations of corner spacers. Vacuum, oxide, nitride, and hafnium represent conventional spacer structure whose material is changed. Other notations are all corner spacer structures. For example, oxvac means corner spacer material is silicon oxide and outer spacer material is vacuum.

In the speed aspect, the delay times of vacuum, oxide, nitride, and hafnium oxide spacers are 14.28ps, 11.90ps, 11.92ps, and 10.82ps, respectively as shown in Figure 4.19. In low stand-by power devices, vacuum spacer inverter is slower than other spacer inverters. The results are totally different from the results in high performance devices. The reasons are that the improvement of on-current is much higher than the degradation of increasing capacitance. However, the corner spacer devices are faster than conventional spacer devices. The corner spacer inverters with the combination of hafnium oxide/vacuum, hafnium oxide/oxide, and hafnium oxide/nitride are faster than other corner spacer inverters and other conventional spacer inverters.

In inverter switching energy aspect, the energy of vacuum, oxide, nitride, and hafnium oxide spacers are 121.33fJ, 132.94fJ, 133.27fJ, and 165.67fJ, respectively. When the dielectric constant is increased, the energy is also increased. The corner spacer inverter can be helpful to decrease the energy but not much. However, the energy of vacuum spacer is the lowest energy of all the splits.

In low stand-by power devices, we also have some options to improve the performances. If we want to improve power consumption, the vacuum spacer may be an excellent solution just same as the results in high performance devices. If we want fast switching speed, we can choose

the corner spacer structure. When we consider both high speed and low power consumption, we may choose the corner spacer transistor whose materials are vacuum and silicon nitride.

4.5 Summary

In high performance device case, the high-k spacer material increases gate capacitance much more than on-current. Thus, vacuum spacer device is the best option for speed aspect. However, the corner spacer device is faster than this vacuum spacer device due to increasing on-current and almost same gate capacitance. For speed aspect, the corner spacer can be the best option but this corner spacer device has a little bit larger power consumption. For power consumption aspect, the vacuum spacer device is a good solution. If we consider both speed and power, the corner spacer or conventional spacer device with vacuum spacer are attractive solutions. As speed is more important in this high performance device, the best structure is the corner spacer device with combination of vacuum and silicon oxide. The speed of this device is improved by 4%, 10%, 20%, and 32% compared to conventional spacer devices with vacuum, silicon oxide, silicon nitride, and hafnium oxide, respectively. The switching energy of this device is increased by 6% compared to the vacuum spacer device. However, except vacuum spacer, this energy is improved by 12%, 24%, and 43% compared to silicon oxide, silicon nitride, and hafnium oxide, respectively.

In low stand-by power device case, the high-k spacer material increases on-current much more than gate capacitance. Therefore, vacuum spacer device is slower than other high-k spacer devices. But the corner spacer device is also helpful. For speed aspect, the corner spacer can be the best option but this corner spacer device has high power consumption. For power consumption aspect, the vacuum spacer device is a good solution. But in this case, the speed is too slow. If we consider both speed and power, the corner spacer is an attractive solution. As power is more important in this low stand-by power device, the best option is the corner spacer device with combination of vacuum and silicon nitride. The speed of this device is improved by 33%, 19%, 19%, and 11% compared to conventional spacer devices with vacuum, silicon oxide, silicon nitride, and hafnium oxide, respectively. The switching energy of this device is increased by 2% compared to the vacuum spacer device. However, except vacuum spacer, this energy is improved by 7%, 7%, and 25% compared to silicon oxide, silicon nitride, and hafnium oxide, respectively. Furthermore, we can reduce V_{DD} in this case because the speed improvement is 33%. Thus, this corner spacer device can be achieved much lower power consumption than vacuum spacer device using decreasing V_{DD}. If V_{DD} is scaled, the static power can be decreased as well as the dynamic power.

4.6 References

[4.1] Sung-il Chang, Hyunjin Lee, Jongho Lee, and Hyungcheol Shin, " Effects of S/D non-overlap and high-κ dielectrics on nano CMOS design", Semiconductor Device Research Symposium, pp.661-664, USA, July. 2001.

[4.2] P.N. Andharea, R.K. Nahara, N.M. Devashrayeea, S. Chandraa and W.S. Khoklea, “Development and performance characterization of the lightly doped drain MOS transistor”, Microelectronics Reliability, Volume 30, Issue 4, pp.681-690, 1990

[4.3] Jaegoo Lee, Changhyun Cho, Juyong Lee, Sooho Shin, Jinwoo Lee, Donghwa Kwak, Kyuhyun Lee, Byunghyug Roh, Taeyoung Chung, and Kinam Kim, “Highly Extendible Memory Cell Architecture for Reliable Data Retention Time for 0.10μ m Technology Node and beyond”, European Solid-State Device Research Conference, pp.571-574, 2002.

[4.4] Jun-Wei Gong, Yeh-Chang Fang, Ta-Yung Wang, Jia-Rui Hu, Chung-I Chang, Tings Wang, Shih-Jung Lee, J. Opsal, L. Nicolaides, “Thickness and Topography of Dielectric Dual-Sidewall Spacers on Metal Gate of DRAM Extracted by Spectroscopic Ellipsometry”, Advanced Semiconductor Manufacturing Conference, pp.272-277, June 2007.

[4.5] Chun-Jen Weng, “Optimization of sub-100nm transistor gate sidewall spacer process for high-performance applications”, Electron Devices and Solid-State Circuits, pp.50-53, December 2009

[4.6] International Technology Roadmap for Semiconductors for Interconnect, 2009

[4.7] SENTAURUS User Manual, Synopsys, Mountain View, CA

Chapter 5

Vacuum-Gap Interconnect

5.1 Introduction

Interconnects are metal wires that connect two or more points in a circuit. In older technologies, the distance between adjacent wires were much larger than metal-oxide-semiconductor (MOS) transistor dimension and the lengths that these metal wires had to travel were relatively short. As a results, interconnect resistance and capacitance were not very large nor comparable to those of active devices such as MOS transistors. The only considerable parameter was reliability problem.

As the technology node gets smaller, the distance between adjacent wires are very close to MOS transistor dimension. Moreover, the thickness of metal wires is hard to be reduced due to resistance problem so that high aspect ratio metal and via occur. Interconnect resistance and capacitance can no longer be considered trivial. New chemical vapor deposition (CVD), physical vapor deposition (PVD), electrochemical deposition (ECD) techniques and metal planarization techniques using chemical mechanical polishing (CMP) as well as novel low dielectric constant (k) materials which have high structural stability and gap filling ability are required for the improved density and performance.

In conventional subtractive etch interconnect (aluminum metallization), aluminum reflow technique for enhanced step coverage into high aspect ratio contacts or vias and the subsequent introduction of CVD tungsten fill/etch-back to form contact/via plugs are needed for providing reliable metal fill of the high aspect ratio contact and via which are followed by lithographic scaling. Dielectric CMP technique is also required to improve the fidelity of high-resolution lithography by providing a more planar surface for imaging as depth of focus decreased with improved resolution. Planar dielectric surfaces also enhanced process margin and yield, since less over-etch was required to clear metal filaments in forming tungsten plugs and aluminum leads. However, aluminum has been used widely in the past and is still used since it has low resistivity, excellent adhesion to dielectric and ease of deposition. Aluminum can be etched using

dry etching technique and make ohmic contacts to silicon but problem with shallow junctions and does not contaminate silicon [5.1].

Aluminum has serious reliability problems. Electromigration is due to electron wind induced diffusion of aluminum through grain boundaries [5.2]. Electromigration induced hillocks which make short circuits and voids which make open circuits. Adding copper to aluminum which decreases its self diffusivity and using materials with higher activation energy are good solutions to increase resistance to electromigration [5.3]. Reducing grain boundary diffusion and stress are also helpful [5.4] [5.5]. Bamboo structure and layered structure reduce grain boundary diffusion [5.6] [5.7].

Although aluminum is still the most predominant interconnect material, there are serious resistance and reliability problems at small feature size. Copper is one of the excellent solutions. It has higher electromigration resistance and lower resistivity compared to aluminum [5.8]. However, copper metallization has some problems. Copper atoms ionize, penetrate into the dielectric, and then accumulate in the dielectric as copper space charge so that there is fast diffusion of copper into dielectric. And copper has poor adhesion to dielectric and poor oxidation/corrosion resistance. Diffusion barrier and passivation are needed in order to overcome these problems. Furthermore, copper is hard to be etched by conventional dry etching technique. Thus damascene process is required. While current copper damascene processes utilize PVD Ta-based barriers and Cu nucleation layers, continued scaling of feature size requires development of other materials and nucleation layer deposition solutions. Continuous improvement of tools and chemistries will extend electrochemically deposited (ECD) Cu to the end of the forecasted roadmap but small, high A/R features necessitate the simultaneous development and subsequent selection of alternative filling techniques. A thin barrier is also needed to maintain the effective conductor resistivity in these features.

Lowering dielectric constant (k) of insulator is also important to reduce interconnect capacitance. Reducing capacitance has a lot of significant benefits of reducing cross-talk noise, delay and power consumption. Fluorine doped silicon dioxide (κ = 3.7) was introduced at 180 nm, however insulating materials with κ = 2.7–3.0 were not widely used until 90 nm [1]. The reliability and yield issues associated with integration of these materials with damascene copper processing proved to be more challenging than expected. The integration of porous low-κ materials is expected to be even more challenging due to low structural stability and reliability issue.

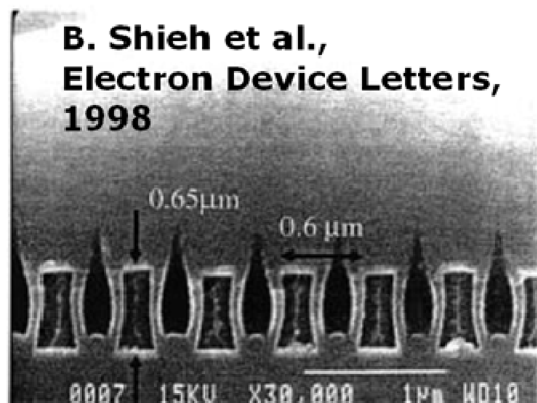
Since the associated inter metal dielectric (IMD) k value is close to 1, vacuum (air) gap appears as the ultimate hybrid architecture leading to dramatic interline capacitance reduction and very low effective κ values. Different air gap integration approaches are being developed to fabricate multi-level interconnects. All approaches can be classified into one of two categories: (1) partial or complete material removal between metal lines followed by non-conformal CVD deposition and (2) damascene integration of metal lines in a sacrificial material which can be selectively removed through a dielectric cap. Each of these methods has benefits and trade-offs.

5.2 Historical Background

5.2.1 Vacuum gap integration in aluminum interconnect

Most vacuum gap integration techniques were already investigated in the 1990's and use either: (1) non-conformal CVD process (2) sacrificial materials. In the aluminum era, IMD had to gap-fill the spaces between the metal lines. Vacuum gaps were unintentionally formed at the narrowest pitches. These vacuum gaps were undesired because their uncontrolled formation could lead to metal voids or electrical shorts during subsequent via formation. However, these vacuum gaps by non-conformal CVD became attractive due to the scale down of interconnect and high interline capacitance. Shieh reported a 40% reduction in capacitance at 0.3µm metal width [5.9]. The vacuum gaps of non-uniform size and shape were made by non-conformal CVD process as shown in Figure 5.1 (a). The vacuum gaps are located between same level metals so that there reduce interconnect capacitance between wires. Heat is carried mostly by vias. This vacuum gap structure has high electromigration resistance because of stress relaxation allowed by free space.

Another approach was the use of sacrificial layer. After formation of the aluminum lines, sacrificial materials are deposited and planarized. After IMD is deposited, the sacrificial materials can be decomposed and vacuum gaps are formed. These sacrificial materials may be photo resist or carbon [5.10]. A drawback is the dependence of material properties. Vacuum gap collapse occurs at wide spaces of more than 4µm. However, there was no problem at the narrow space where low capacitance is very important. Anand reported a process uses O_2 gas diffused through a thin bridge layer (SiO_2) to react with the underlying carbon layer at 450ºC as shown in Figure 5. 1 (b) [5.11].



(a)

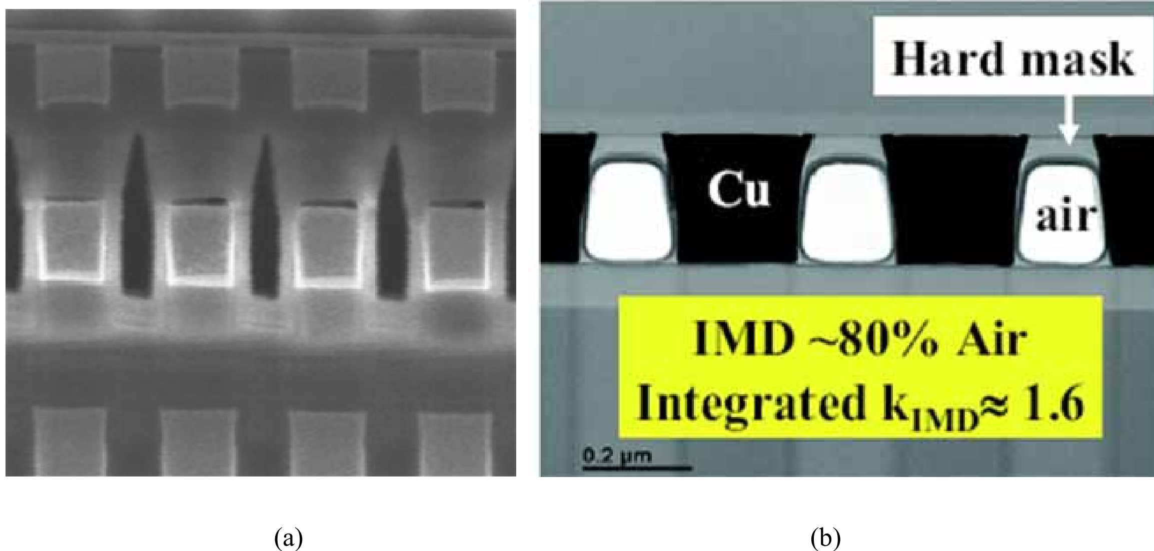
(b)

Figure 5.1: Some vacuum gap integration profiles in aluminum interconnect (a) using non-conformal CVD process (b) using sacrificial materials

5.2.2 Vacuum gap integration in copper interconnect

Copper cannot be easily etched anisotropically; the integration is done using damascene technology. The vacuum gap integration techniques in copper interconnect are almost same as those of aluminum interconnect. A vacuum gap interconnect using non-conformal CVD process flow is that after damascene process, the surrounding dielectric needs to be removed before applying the non-conformal CVD process to form the vacuum gaps. Gosseta reported a process using conventional dry etching technique to remove the surrounding dielectric at 0.14 μm [5.12]. Figure 5.2 (a) shows that vacuum gap profile in copper damascene interconnect looks like that in aluminum interconnect.

Another way is to use the sacrificial materials. Daamen reported vacuum gap interconnect scheme using the copper dual damascene process [5.8]. He used the sacrificial material as thermal degradable polymers (TDP) which is composed at 400°C easily. Figure 5.2 (b) shows that vacuum gap is located between two same level metals. Carbon CVD is one of the good sacrificial materials [5.10].



(a) (b)

Figure 5.2: Some vacuum gap integration profiles in copper interconnect (a) using non-conformal CVD process (b) using sacrificial materials

5.3 Process Integration

As the technology node gets smaller, the conventional subtractive etch interconnect should be changed to the copper damascene interconnect due to better electro-migration resistance, low metal resistivity, and IMD gap-fill problem. However, the conventional subtractive etch interconnect process is still used for dense memory products such as dynamic random access memory (DRAM) or static random access memory (SRAM) or NAND and NOR flash memory. Thus, two types of interconnect with vacuum-gap structures are suggested. One is for the subtractive etch interconnect process for dense memories and the other is for the dual damascene interconnect process for high speed devices.

5.3.1 A subtractive etch interconnect with vacuum-sheath structure

5.3.1.1 The comparison of structures by simulation

We propose a novel vacuum sheath structure for subtractive metal etch process suitable for dense memory products. This proposed interconnect structure places every metal line inside a vacuum corridor. We compared the capacitances of the interconnect structures with and without the vacuum sheaths from 175nm to 20nm feature sizes by simulation as shown in Figure 5.3. C_M, C_O, and C_F represent mutual capacitance, overlap capacitance, and fringing capacitance, respectively.

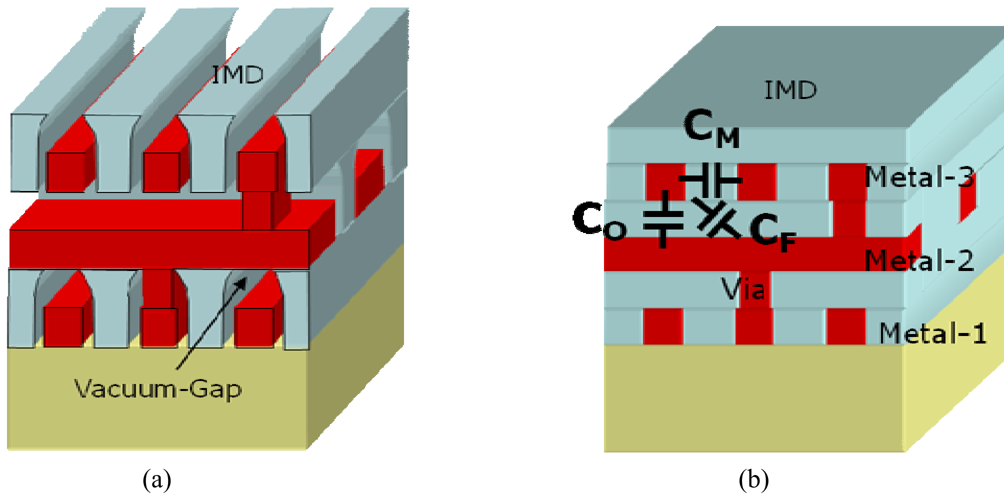


Figure 5.3: Comparison between the suggested vacuum-gap interconnect and conventional subtractive etch interconnect. (a) Every metal lines and Vias are surrounded by vacuum-gap (b) Every metal lines and Vias are surrounded by IMD.

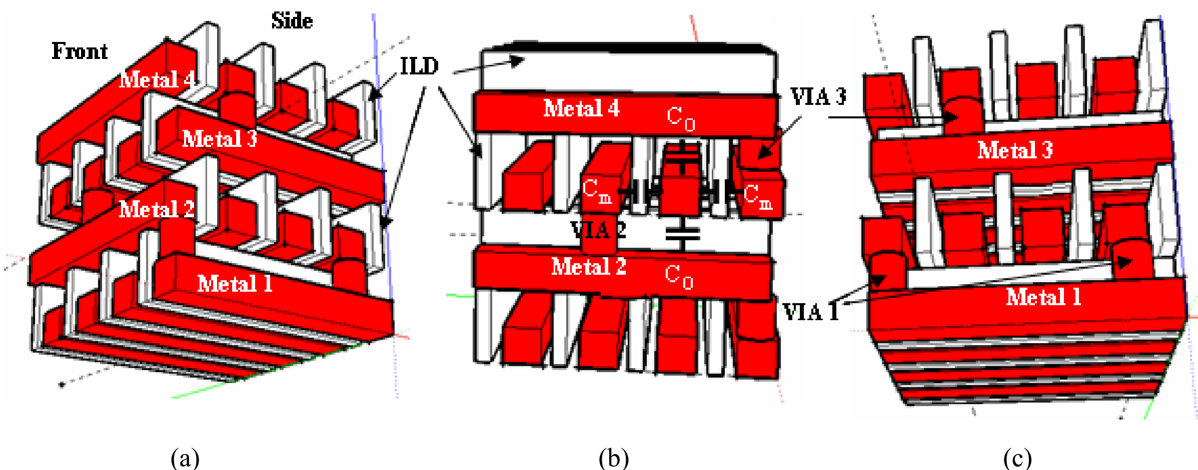


Figure 5.4: 3D rendering of the proposed air-sheath interconnect structure. (a) Tilted view of a block of the interconnect structure (b) Front view of the structure (c) Side view of the structure

5.3.1.2 Structure and Process Concept

Figure 5.4 shows three views of the same block of the proposed interconnect and Vias structure. Figure 5.4 (a) shows that the metal lines are supported by a 3-dimensinal system of beams or walls. Figure 5.4 (b) shows the front view of the tunnels that house the metal-3 lines. Figure 5.4 (c) shows the tunnels that house the metal-2 lines. All the metal lines are completely enveloped by vacuum sheaths on the sides and over the top as well as on the bottom wherever they cross over metal lines. The Vias are surrounded by vacuum sheaths, too.

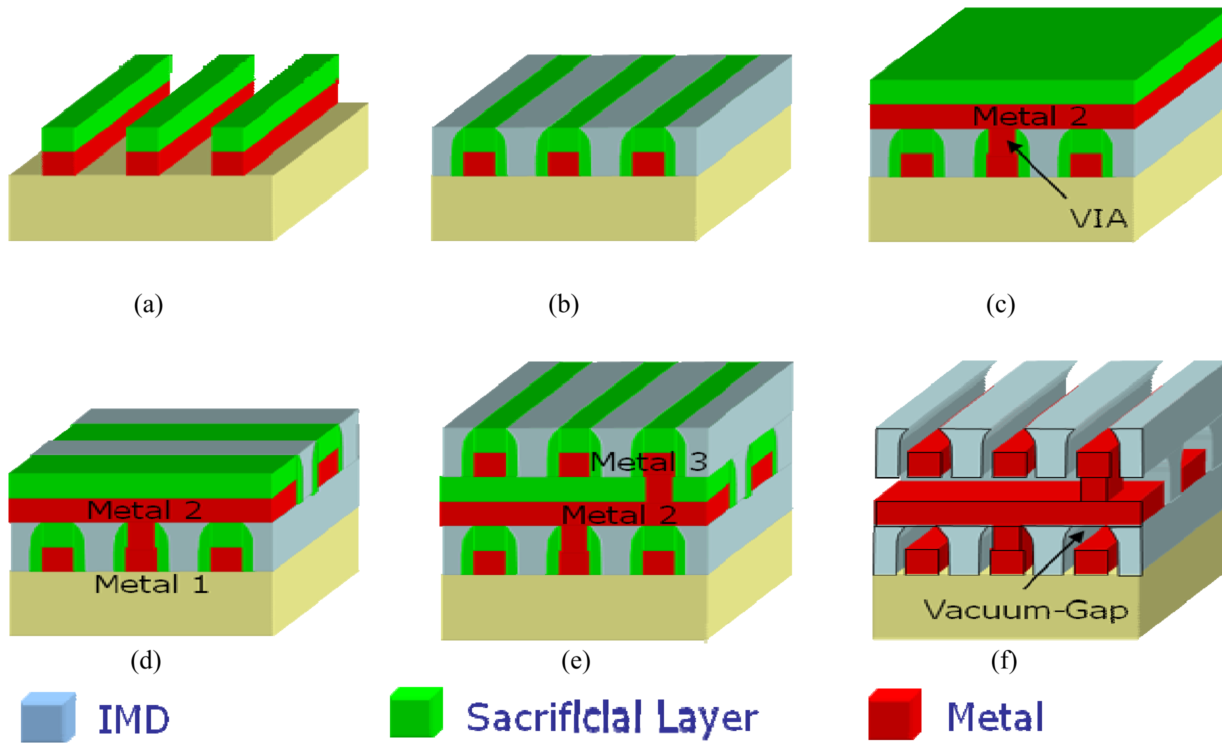


Figure 5.5: A proposed process flow of the vacuum-sheath interconnects. (a) After Metal-1 material and sacrificial layer are deposited sequentially, Metal-1 photolithography carries out. Sacrificial layer and Metal-1 are etched sequentially using reactive ion etch (RIE) process. (b) Sacrificial spacer is formed and IMD is deposited and dielectric CMP is carried out. (c) After Vias photolithography, all the Via holes are etched and barrier metal is deposited. The barrier metal and Tungsten (W) are filled and polished using metal CMP process. Barrier metal is not shown in this figure for simplicity. Metal-2 and another sacrificial material are deposited sequentially. (d) After Metal-2 lithography, sacrificial layer and Metal-2 are etched. And then sacrificial spacer is formed and IMD is deposited and polished just like Figure 5.5 (b) processes. (e) Metal-3 process is the same as Metal-2 process (repeat Figure 5.5 (c) and (d) processes). (f) All the sacrificial layers and spacers are connected to each other so that the material can be removed. And final IMD is deposited to seal the vacuum-gaps which is not shown in this Figure for simplicity.

Figure 5.5 illustrates the proposed process flow. Figure 5.5 (a) shows the same structure of the conventional subtractive Metal-1 etch structure except replacing oxide hard mask with sacrificial material [5.13]. The etched lines of metal-1 topped with a sacrificial layer such as carbon oxide. One key requirement for the sacrificial layer material is the ease of removal. In

Figure 5.5 (b), two sacrificial spacers between one metal line are connected to one sacrificial layer which is located at the top of the each metal line. Figure 5.5 (c) and (d) processes are the same as the conventional Metal-2 process except replacing oxide hard mask with sacrificial layer and having sacrificial spacers. All the sacrificial spacers and layers are connected to other sacrificial spacers and layers. In Figure 5.5 (e), After Metal-3 process, the sacrificial layers on the top of the Metal-3 lines are exposed. In Figure 5.5 (f), all sacrificial spacers and layers are removed by an etching process such as carbon oxide or TDP. And a top non-conformal dielectric is deposited to seal the arch shaped vacuum pocket.

The proposed process is easily compatible with conventional process. The additional steps are only forming sacrificial spacer and removing it. All the techniques to prevent electromigration can be used in this vacuum-sheath interconnect structure.

5.3.2 A dual damascene interconnect with vacuum-corridor structure

5.3.2.1 The comparison structures with simulation

We propose a novel vacuum-gap structure for dual damascene metal process. This proposed interconnect structure places every metal line inside a vacuum-corridor. We compared the capacitances of the interconnect structures with and without the vacuum-corridor from 59nm to 20nm feature sizes through simulation as shown in Figure 5.6.

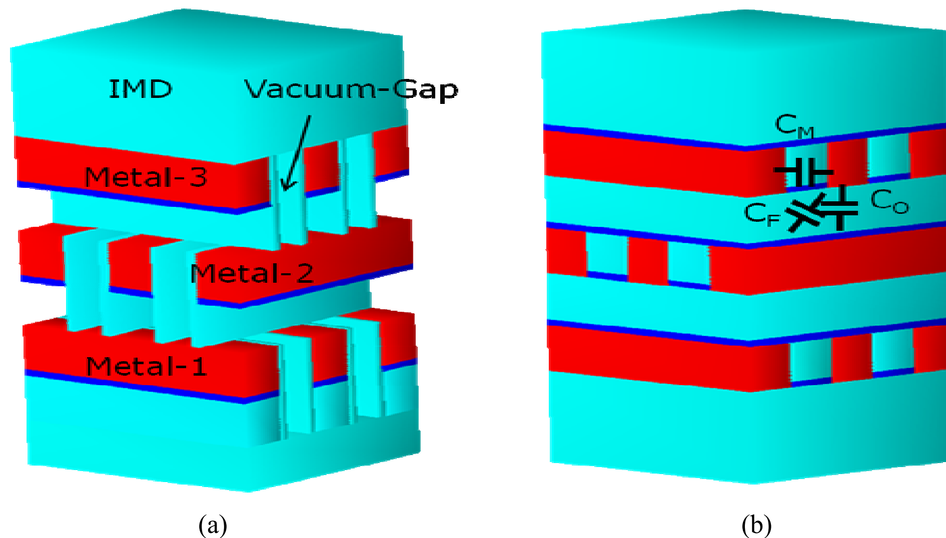


Figure 5.6: Comparison between the suggested vacuum-corridor interconnect structure and conventional dual damascene interconnect structure. (a) Every metal line has two support oxide beams and is surrounded by vacuum-gap (b) Every metal line is surrounded by IMD

5.3.2.2 Structure and Process Concept

Figure 5.7 shows three views of the same block of the proposed interconnect and via structure. Figure 5.7 (a) shows that each metal line is supported by a 3-dimensinal system of two dielectric support beams. Figure 5.7 (b) shows that every metal line is surrounded by vacuum corridor except two support beams. Figure 5.7 (c) shows all the support beams are connected to both upper support beams and lower support beams. Vacuum exists on every metal cross over point and between the metals. The Vias are also surrounded by vacuum corridor. Figure 5.8 shows the detailed process flow of the dielectric support beams. This process puts the support beams under every metal lines so that the metal lines are solidly built with the support beams.

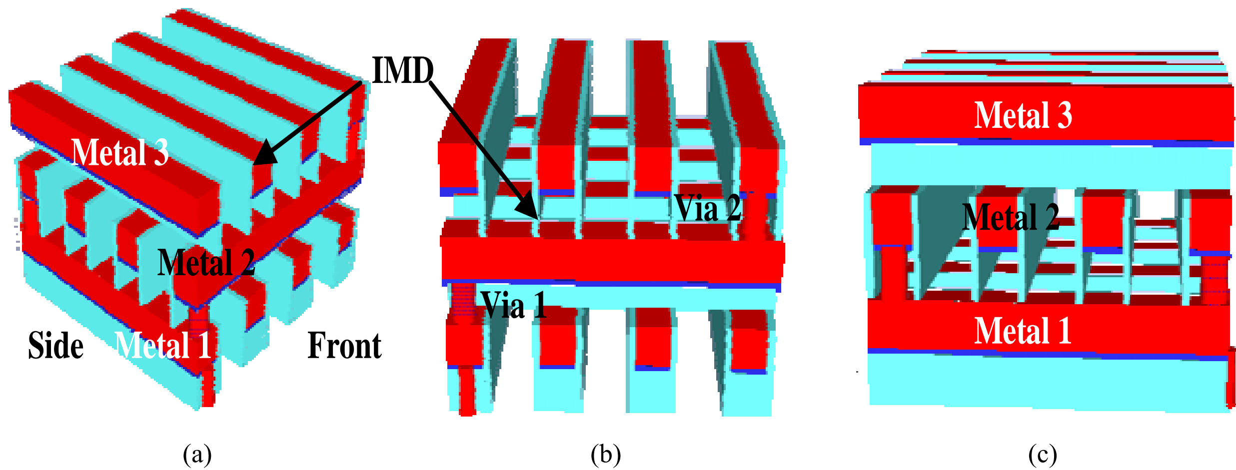


Figure 5.7: 3D rendering of the proposed vacuum-corridor interconnect structure. (a) Tilted view of a block of the interconnect structure (b) Front view of the structure (c) Side view of the structure

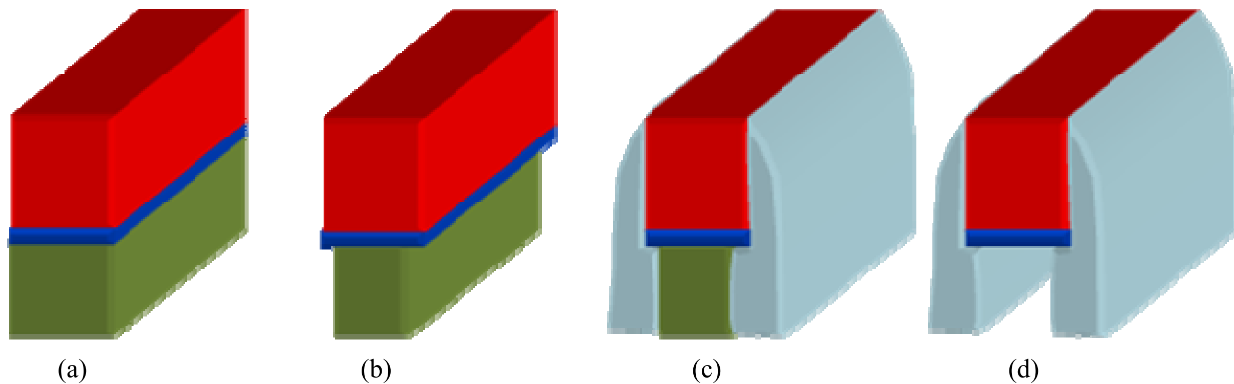


Figure 5.8: 3D process flow shows how to make the dielectric support beams. (a) After etching process (b) Cleaning process etches the dielectric under the metal (c) Spacer formation (d) After removing the dielectric, two support beams can support one metal line tightly

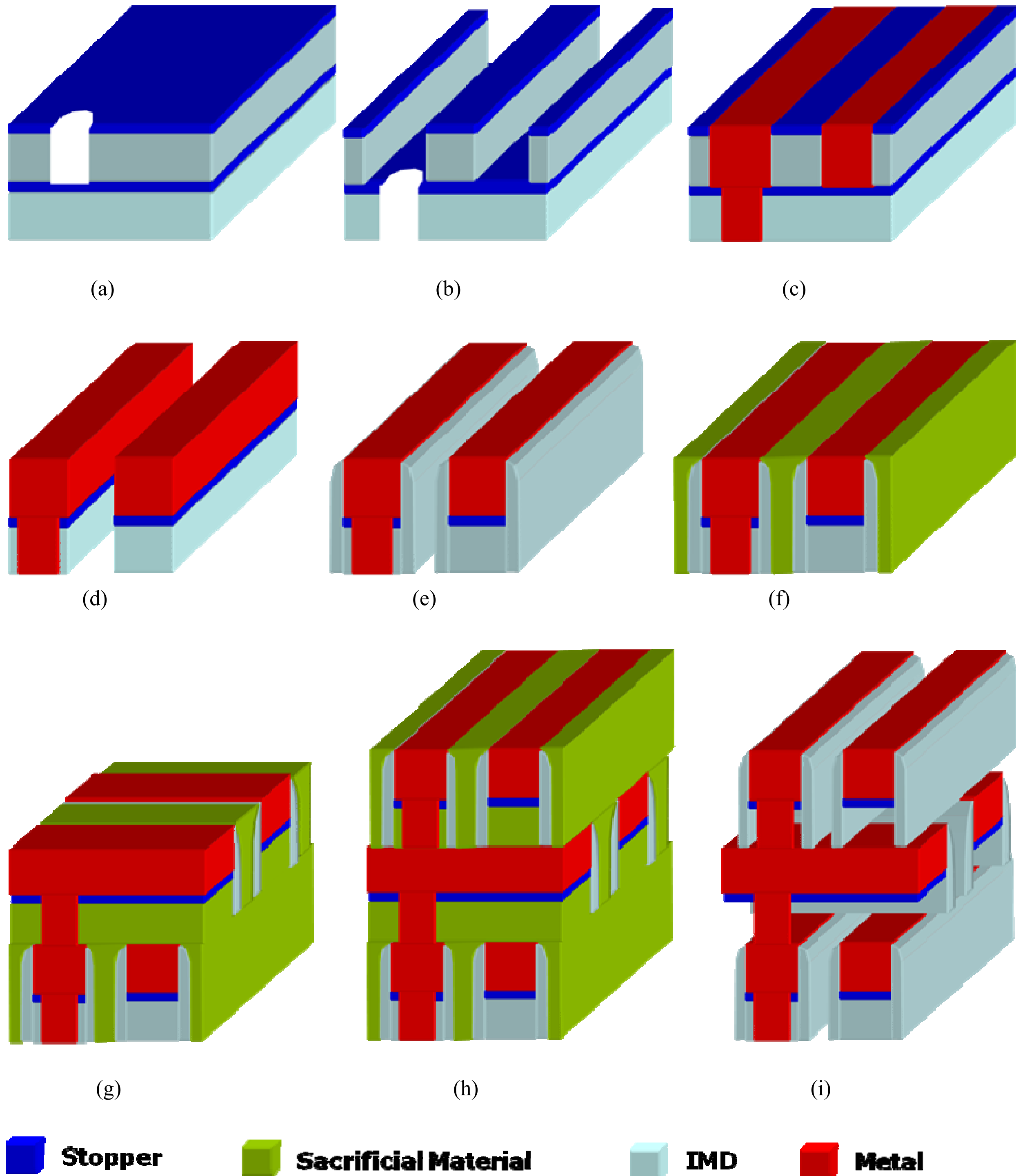


Figure 5.9: A proposed process flow of the dual damascene interconnect with vacuum-corridor structure. (a)-(c) The same process as the conventional dual damascene process (d) Selective etching the stopper nitride and IMD (e) Dielectric spacer is formed (the detailed process flow showed in Figure) (f) Sacrificial material is deposited and polished (g) Metal-2 process is same as the Metal-1 process except the material under the Metal-2 layers is changed by sacrificial material (h) Metal-3 process is exactly same as Metal-2 process (i) All the sacrificial layers are connected to each other so that the material can be removed. And final IMD is deposited to seal the vacuum-gaps which is not shown in this Figure for simplicity.

Figure 5.9 illustrates the proposed process flow. Figure 5.9 (a) - (c) processes are same as the conventional dual damascene process [5.14]. The barrier metal and the alumina capped oxidation-free structure that has been proven to protect Cu from oxidation is not shown in these figures for simplicity [5.15]. In Figure 5.9 (d), the stopper nitride and IMD are etched by selective etching process. Copper would not be etched. Figure 5.9 (e) shows that oxide spacers are formed. These solid dielectric beams are supported by each metal line. In Figure 5.9 (f), the sacrificial layers are deposited and chemical mechanical polishing (CMP) is carried out. In Figure 5.9 (g) - (h), the Metal-2 and Metal-3 processes have been completed by repeating the processes shown in Figures 5.9 (a) through 5.9 (f). The only different point is that the dielectric material under the metals is replaced with the sacrificial material since all the sacrificial material should be connected to other sacrificial material. However, the dielectric material under Metal-1 layers cannot be connected to other sacrificial layers so that that material under Metal-1 layers is same as the conventional material. In Figure 5.9 (i), all sacrificial layers are removed and a top non-conformal dielectric is deposited to seal the vacuum-corridor. Carbon chemical vapor deposited (CVD) oxide can be used as the sacrificial layer. One key requirement for the sacrificial layer material is the ease of removal.

5.4 Modeling for Simulation

5.4.1 General Modeling for Interconnect

Simulation-based approaches tended to rely on 3-D Maxwell equations (5.1 - 5.4) solvers to provide the most realistic results. The field solvers require a full specification of the interconnect structure. If the capacitance between two metal plates was to be simulated, the width, length, and height of each plate must be specified. In addition, the IMD thickness and dielectric constants for the insulator between the two plates as well as above the top plate need to be specified as shown in Figure 5.10. After all interconnect parameters have been specified, the 3-D field solver can be used to simulate the capacitance for various interconnect patterns and geometries. The total number of possible patterns and combinations is near infinite. The results of 3-D field solver are then stored in a database for latter use by a design tool. Design tools will try to match the patterns in the design to those within the database. If a match is found, it simply uses its capacitance value. Raphael 3D simulator is used for these simulations [5.16] [5.17].

Faraday's law: $$\nabla \times \overline{E} = - (\partial \overline{B}) / \partial t \quad (5.1)$$

Ampere's law: $$\nabla \times \overline{H} = - (\partial \overline{D}) / \partial t + \overline{J} \quad (5.2)$$

Gauss' law: $$\nabla \cdot \overline{B} = 0 \quad (5.3)$$

$$\nabla \cdot \overline{D} = \rho \quad (5.4)$$

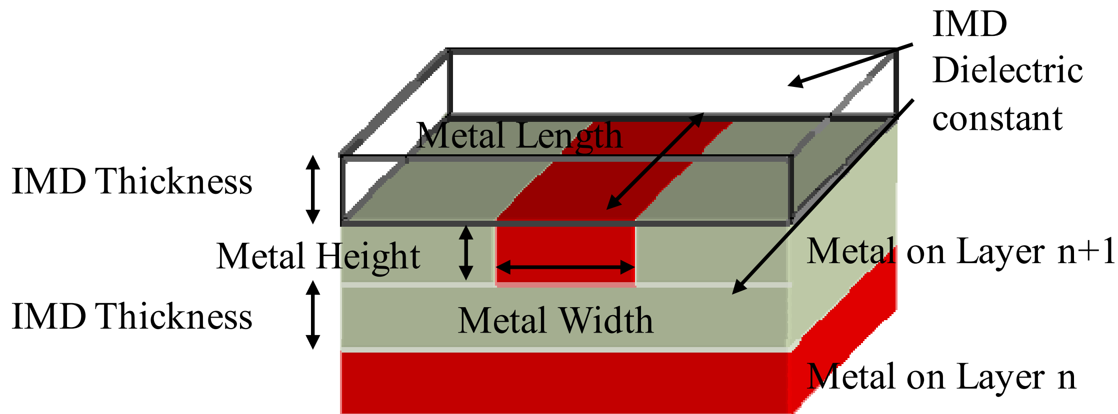


Figure 5.10: Interconnect parameters must be specified for accurate 3-D field solver simulations.

1.6.2 Capacitance Definitions of RAPHAEL Default Database

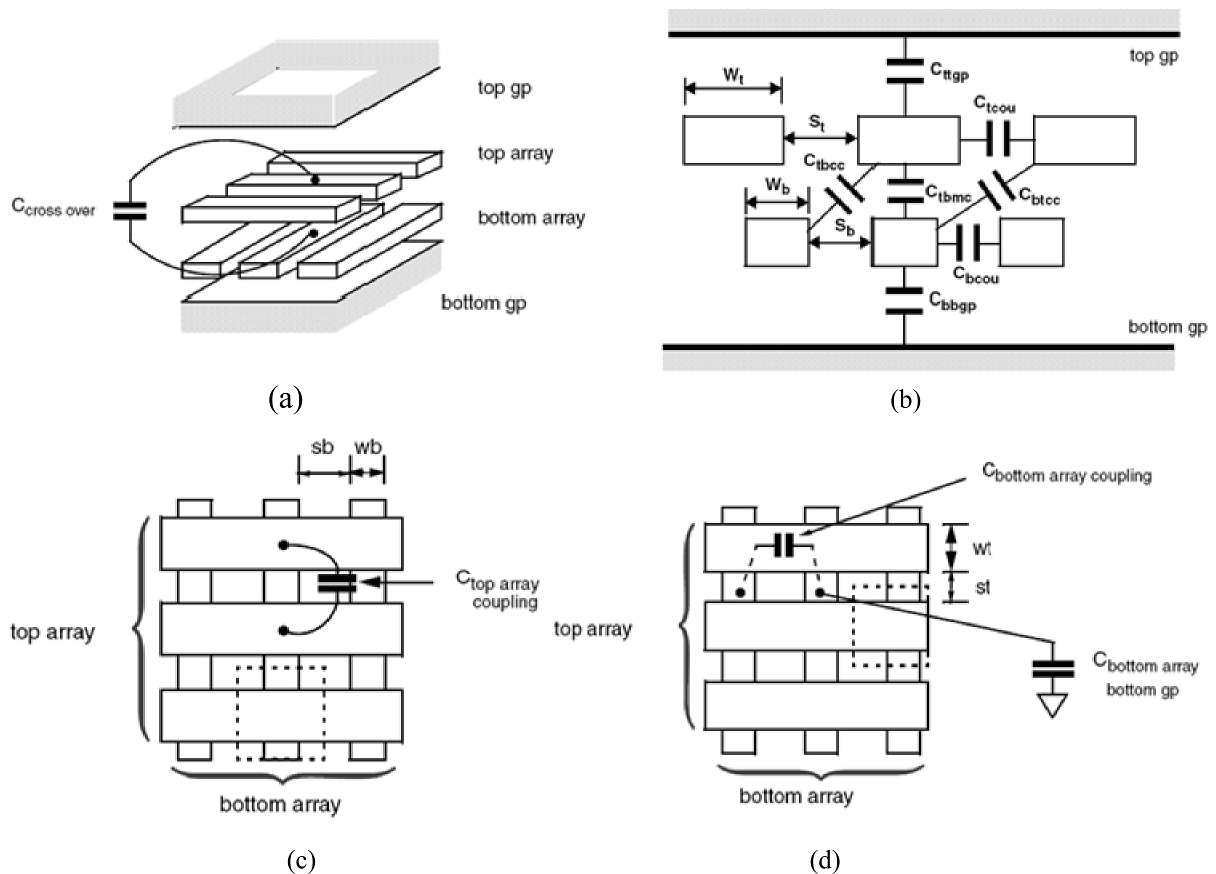


Figure 5.11: (a), (c) and (d) Capacitance terms for "array crossover between ground planes" generic structure. (b) Capacitance terms for "two parallel arrays between two ground planes" generic structure.

There are two ground planes, top ground plane (top gp), bottom ground plane (bottom gp) as shown in Figure 5.11 (a). In bottom array, metal width and space represent wb and sb, respectively as shown in Figure 5.11 (c). Metal width and space in top array shows wt and st, respectively as shown in Figure 5.11 (d). C_{ttot} is the total capacitance for a trace in the top array to all other electrodes in the dashed box in Figure 5.11 (c). C_{ttgp} is the capacitance for a trace in the top array to top ground plane in the dashed box in Figure 5.11 (c). C_{btot} is the total capacitance for a trace in the bottom array to all other electrodes in the dashed box in Figure 5.11 (d). Array coupling capacitance is the capacitance between same level metals. Top and bottom array coupling capacitance show C_{tcou} and C_{bcou}, respectively in Figure 5.11 (b). There are some overlap capacitances: capacitance of bottom center conductor to bottom ground plane (C_{bbgp}), capacitance of top center conductor to bottom center conductor (C_{tbmc}), capacitance of top center conductor to top ground plane (C_{ttgp}). There are two cross coupling capacitances: cross coupling capacitance between top center and bottom left conductors (C_{tbcc}), cross coupling capacitance between bottom center and top right conductors (C_{btcc}).

5.5 Simulation Results

5.5.1 A subtractive etch interconnect with vacuum-sheath simulation

5.5.1.1 Simulation implementation

3D Computer simulations were performed. The structure generated in the Raphael simulator [5.16] [5.17] is shown in Figure 5.12. Each metal is almost surrounded by Vacuum. This structure is totally different to previous vacuum gap interconnect which has vacuum gap only between the same level metals. C_M is the mutual capacitance between two parallel metal lines which is the same as coupling capacitance. It is a key determinant of the cross talk noise [5.18]. C_O and C_F are the overlap and fringing capacitances (cross coupling capacitance), respectively. The total capacitance, the sum of C_M, C_O, and C_F is the C_{TOT} in the RC delay of interconnect. Table 5.1 shows the 2008 International Technology Roadmap for Semiconductors (ITRS) projections for interconnection [1]. ITRS shows the aspect ratio of metal so that metal thickness will be calculated. We assume that the IMD thickness is twice the metal thickness. These values are used in the simulations. We assume that the support beams of the vacuum-sheath structure have a dielectric constant of 3.3. The effective dielectric constants in Table 5.1 are used in the simulation of the ITRS capacitance requirement. Below 40nm metal width, the ITRS required effective dielectric constant decrease rapidly as shown in Table 5.1. However, ITRS states that the manufacturing solutions for these under 2.9 effective dielectric constants are not known [5.1]. The proposed vacuum-sheath interconnect structure is a potential solution.

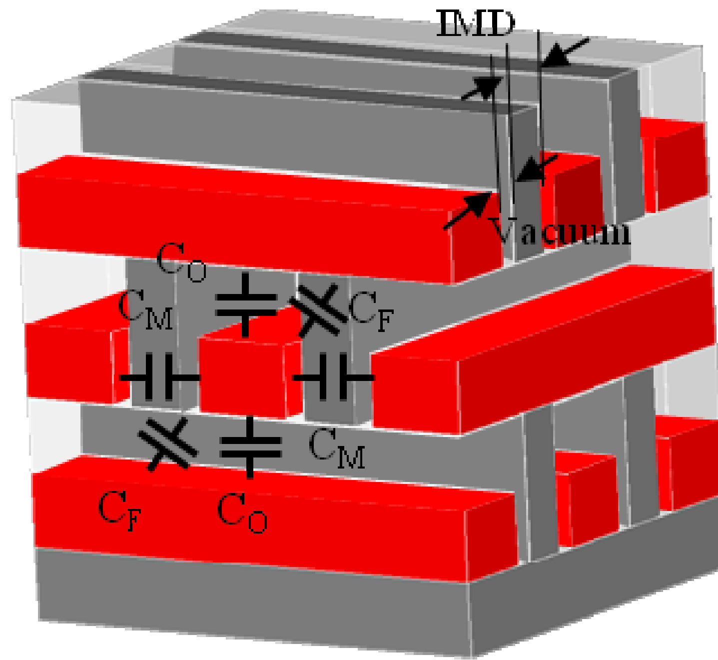


Figure 5.12: The simulation structure of vacuum sheath interconnect using RAPHAEL simulator.

ITRS 2008 Specifications							
Metal1 Width	175nm	122nm	90nm	59nm	40nm	28nm	20nm
Metal1 Space	175nm	122nm	90nm	59nm	40nm	28nm	20nm
Metal1 A/R	1.6	1.6	1.7	1.8	1.8	1.9	2.0
Metal1 Thick	2800Å	1952Å	1530Å	1062Å	720Å	532Å	400Å
Effective Dielectric Constant(k)	2.9~3.3	2.9~3.3	2.9~3.3	2.9~3.3	2.6~2.9	2.4~2.8	2.1~2.5
The Assumption for the simulation							
IMD Thick	5600Å	3904Å	3060Å	2124Å	1440Å	1064Å	800Å
Dielectric constant	3.3	3.3	3.3	3.3	3.0	2.7	2.4

Table 5.1: ITRS 2008 specifications for interconnect and the assumptions for the simulation.

5.5.1.2 Simulation Results

There are two interconnect structures: vacuum sheath interconnect and conventional interconnect as shown in Figure 5.3. Our simulation structure has 9 metals: 3 of metal-1, 3 of metal-2 and 3 of metal-3. Among these metal lines, the capacitance of the center of metal-2 line is higher than that of other metal lines because of fringing capacitance. So this capacitance is used for our simulation.

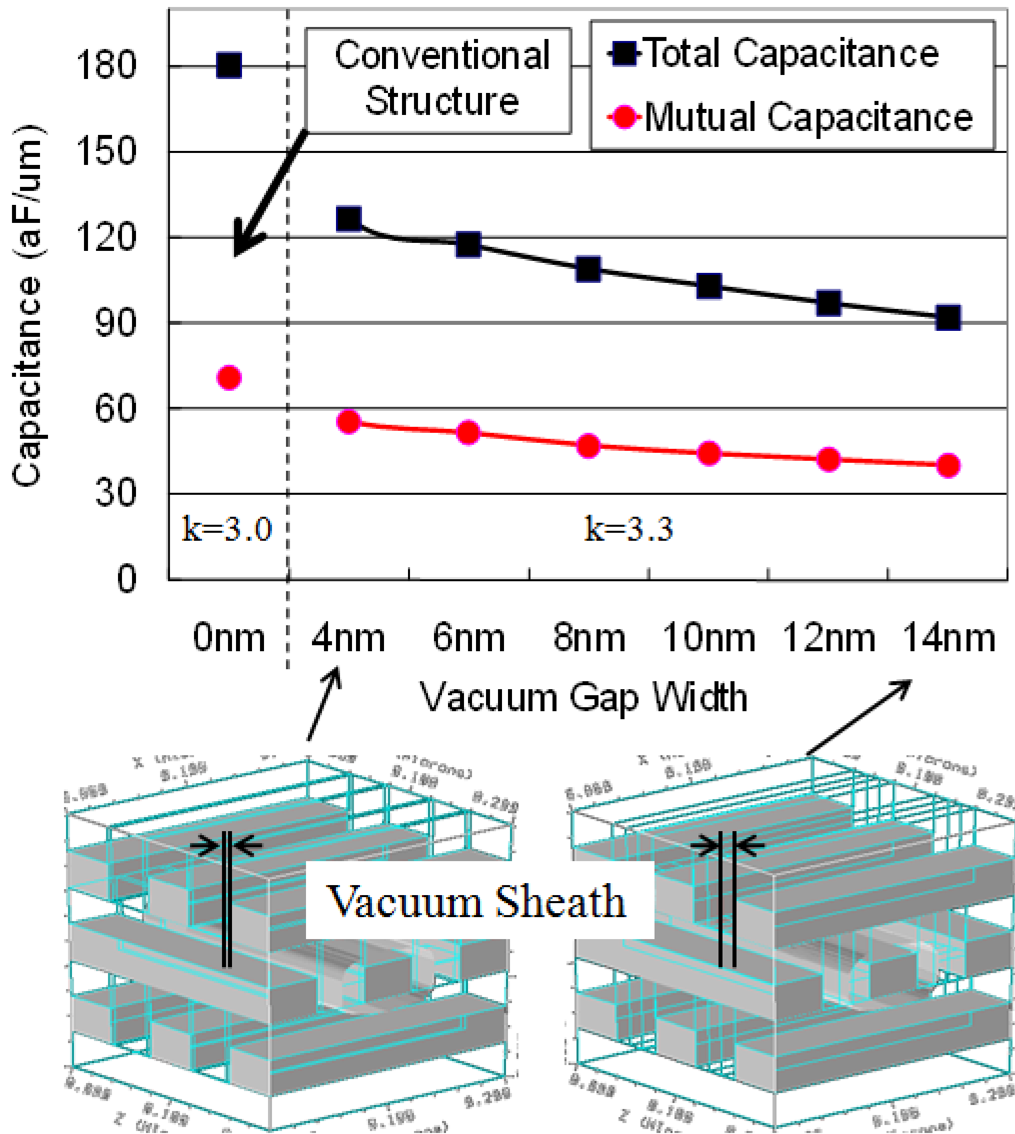
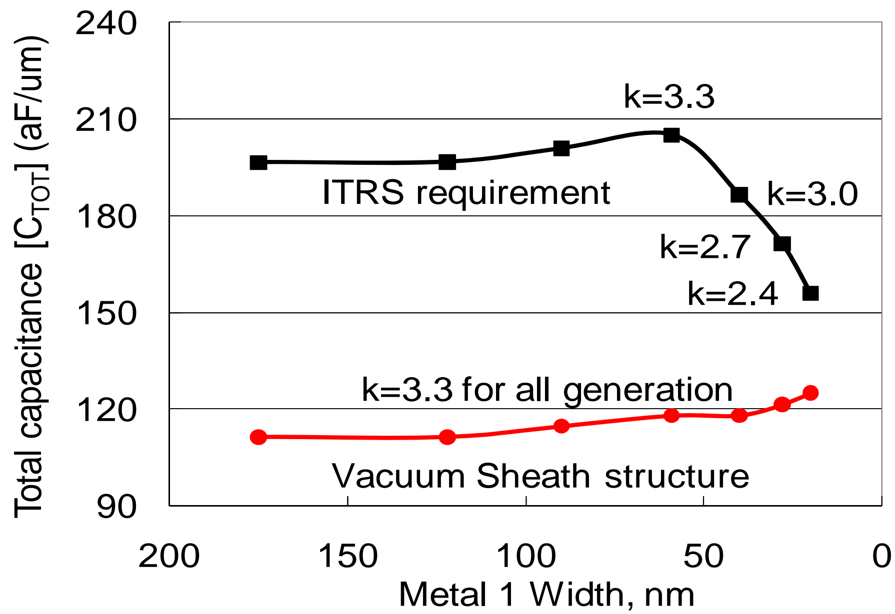


Figure 5.13: Total and mutual capacitances are decreased as vacuum gap width is increased. Total capacitance of only 4nm vacuum gap width with higher k (k=3.3) is much less than that of conventional structure with lower k (k=3.0). Metal width is 40nm.

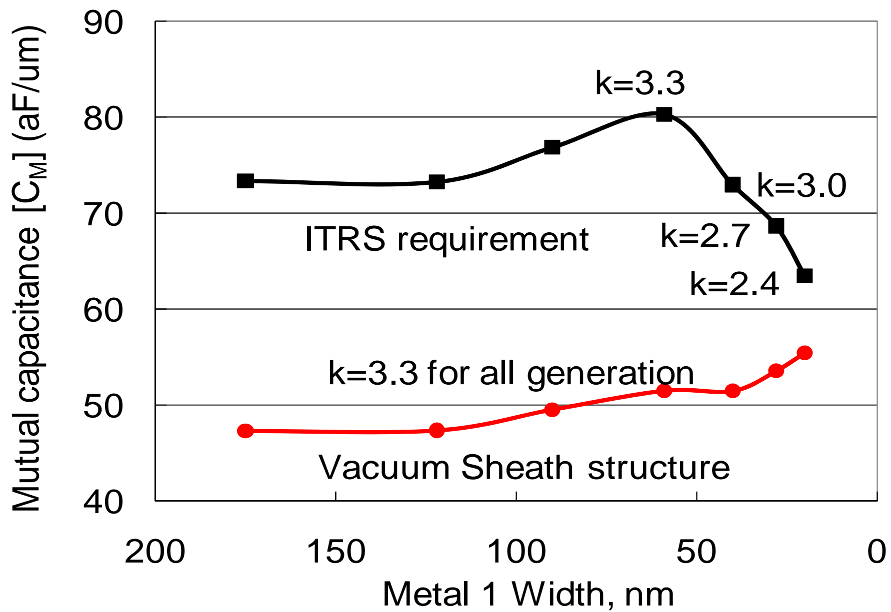
The total and mutual capacitances of the center of metal-2 lines are extracted. All the specific parameters of each generation are followed by Table 5.1 in conventional structure. Vacuum sheath structure has the same geometry as the conventional structure except vacuum sheath parts. Metal space is divided into two vacuum gaps of equal width and one support dielectric beam. A thicker vacuum gap width leads to lower support dielectric beam width at the fixed metal space. Figure 5.13 shows total and mutual capacitances of several vacuum gap widths. X axis represents vacuum gap width from 0nm to 14nm at 40nm metal width and space. Conventional structure is 0nm vacuum width with dielectric constant is 3.0 which are followed by Table 5.1. The dielectric constant of the support beam dielectric is 3.3. The dielectric (k=3.3) is known to high structural stability. The vacuum gap width is defined as one vacuum gap width. For example, 10nm vacuum gap width means that two 10nm vacuum gap widths and 20nm support beam. Even if 4nm vacuum gap width is used in this simulation, total and mutual capacitances of vacuum sheath structure are lower than that of conventional structure (ITRS requirements) by 30% and 22%, respectively. 14nm vacuum gap width leads to 50% lower total capacitance. A thicker vacuum gap width leads to lower capacitance but lower structural stability. Thus, only 8nm vacuum gap width is chosen to other simulations. 8nm is only 20% of the 40nm metal space. So 20% vacuum width is used for all generations. For example, if metal space is 28nm, the space consists of two 5.6nm vacuum gap widths (20%) and 16.8nm support beam width (60%).

Figure 5.14 shows total and mutual capacitances at each generation. All the specific parameters are followed by Table 5.1 (ITRS specifications). From 175nm to 59nm of metal widths, the total and mutual capacitances of vacuum sheath structure are reduced by 44% and 36%, respectively compared to those of conventional structure. From 40nm to 20nm of metal widths, dielectric constant of IMD should be reduced from 3.0 to 2.4 according to ITRS specifications. However, there is no solutions below effective k = 2.9. The total and mutual capacitances of vacuum sheath structure is slightly increased with scaling due to using the same dielectric support beam (k=3.3). Those capacitances of vacuum sheath structure are much lower than those of conventional structure even if a solution is found for implementing k=2.4. Total and mutual capacitances can be reduced by 20% and 13% at 20nm of metal width compared to those of conventional structure (k=2.6). That means current dielectric technique can be extended to below 20nm technology using vacuum sheath interconnect with high dielectric material (k=3.3).

Process variation is also important part of the interconnect process. Figure 5.15 shows IMD variations. All the simulation of Figure 5.13 and 5.14 assume that IMD thickness is twice the metal thickness. However, there are some variations in real process. Relative IMD thickness means IMD thickness over twice the metal thickness. For example, if relative IMD thickness is 0.5, IMD thickness is half of the metal thickness and if it is 2, the thickness is 4 times thicker than the metal thickness. The structures of figure 5.15 (a) and (b) show the structures of relative IMD thickness is 0.5 and 2, respectively. As the IMD thickness is increased, total capacitance is decreased but mutual capacitance is increased. It is notable that both the total and mutual capacitances of the vacuum sheath structure are less sensitive to the IMD thickness than those of the conventional structure. Even if IMD thickness is changed a lot, the effects of the vacuum sheath interconnect are still same. Total and mutual capacitances can be reduced by 45% and 34%, respectively at 40nm of metal width.

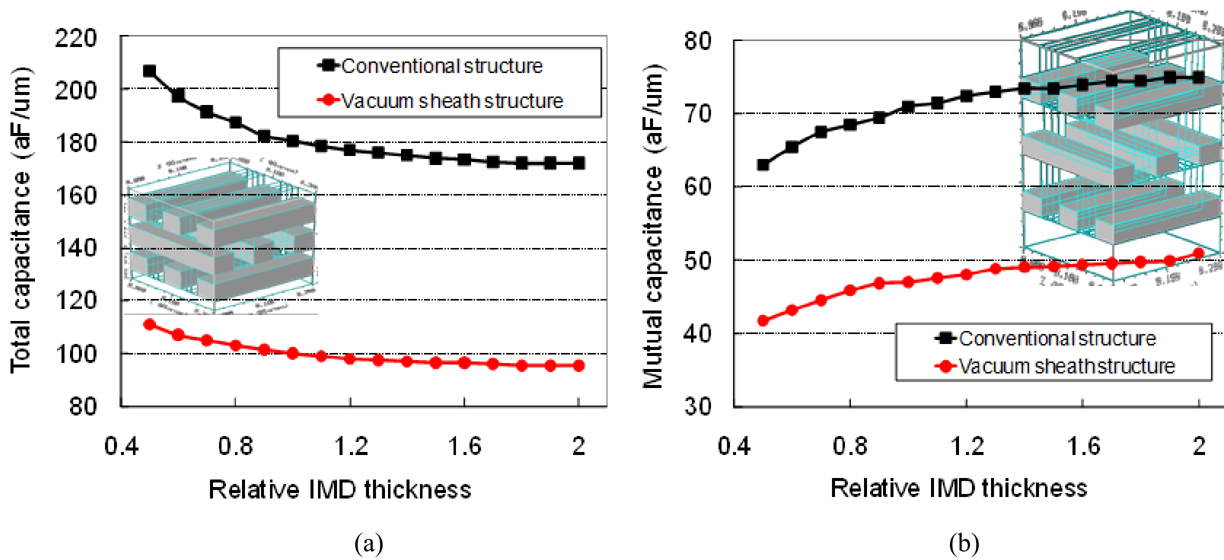


(a)



(b)

Figure 5.14: Total (a) and mutual (b) capacitances should be increased as metal width is decreased without scaling dielectric constant.. Total and mutual capacitances of vacuum sheath interconnect using conventional dielectric (k=3.3) are still lower than those of conventional interconnect using ultra low dielectric (k=2.4).



(a) (b)

Figure 5.15: (a) Total capacitance (speed) is decreased as the thicker IMD. (b) Mutual capacitance (cross-talk noise) is increased as the thicker IMD. Metal width is 40nm

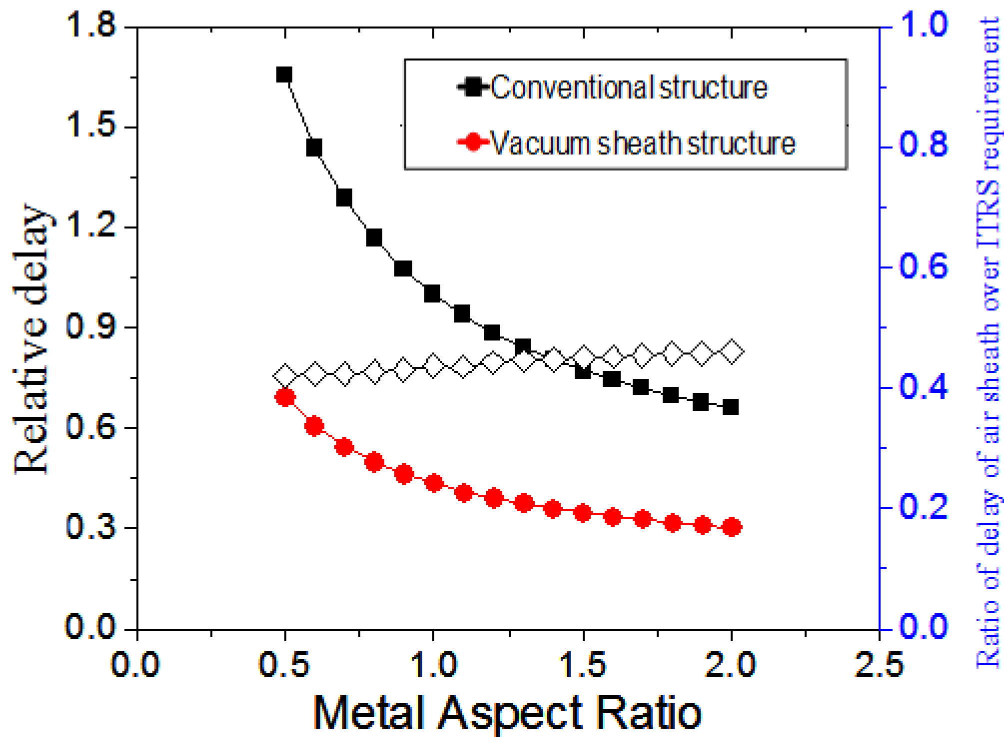


Figure 5.16: Relative delay is decreased as metal thickness is increased. Metal width and space are 40nm

Figure 5.16 shows the Relative interconnect RC delay time versus the metal aspect ratio. Metal width and space are 40nm. If the ratio is higher (taller metal height), the delay is smaller due to reducing metal resistance but the vacuum sheath interconnect scheme always has approximately 45% of the delay of the conventional interconnect scheme.

5.5.2 A dual damascene interconnect with vacuum-corridor simulation

5.5.2.1 Simulation implementation

Table 5.2 shows the 2007 International Technology Roadmap for Semiconductors (ITRS) projections for interconnection [5.19]. We assume that the thickness of stopper nitride is shown in Table 5.2 and IMD thickness is twice the metal thickness. Although ITRS shows effective k, we assume it to be the dielectric constant of IMD material as shown in Table 5.2. These values are used in the simulations of the conventional interconnect scheme. We also assume that the support beams of the vacuum-corridor structure have a dielectric constant of 2.9.

There are some differences between conventional dual-damascene structure and vacuum-corridor structure as shown in Figure 5.6. Conventional structure has two nitride stoppers in each metal line. However, vacuum-corridor has only one nitride stopper in each metal line because the nitride stopper is etched as shown in Figure 5.9 (d). 3D Computer simulations were performed. The structure generated in the Raphael simulator is shown in Figure 5.17 [5.16] [5.17].

2007 ITRS specifications				
Metal Width / Space	59 / 59nm	40 / 40nm	28 / 28nm	20 / 20nm
Metal A/R	1.8	1.8	1.9	2.0
Assumption for simulation				
Metal Thickness	1062Å	720Å	532Å	400Å
Stopper Nitride Thickness	10nm	10nm	5nm	5nm
IMD Thickness (Metal + Via Thickness)	2124Å	1440Å	1064Å	800Å
Dielectric Constant (k) for conventional structure	2.9	2.7	2.5	2.3
Dielectric Constant (k) for Vacuum-Corridor	2.9	2.9	2.9	2.9

Table 5.2: ITRS 2007 specifications for interconnect and the assumptions for the simulation.

Below 40nm metal width, the effective dielectric constant should be less than 2.9 according to ITRS. However, ITRS states that the manufacturing solutions for the under 2.9 effective dielectric constant are not known [5.19]. The proposed vacuum-corridor interconnect structure is a potential solution. In the conventional dual-damascene structure, we should use an IMD whose dielectric constant is 2.25 to meet effective k=2.9 because of high dielectric constant of nitride stopper material. For simplicity, we use some different dielectric constant at each generation as shown in Table 5.2.

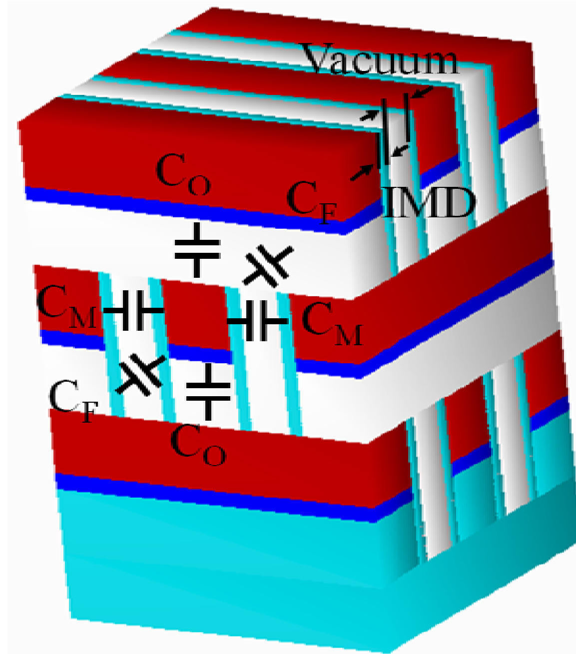


Figure 5.17: The simulation structure of vacuum corridor dual damascene interconnect using Raphael simulator.

5.5.2.2 Simulation Results

Simulation shows that even if the k of the support beam dielectric remains at 2.9, the capacitance of the vacuum-corridor structure is significantly less than that of the conventional structure at 40nm metal width as shown in Figure 5.18. X axis represents each metal line of the simulation structure as shown in Figure 5.17. "M1B" means the center metal-1 line. The total capacitance of the M2B metal line is higher than that of other lines due to fringing capacitance in conventional dual damascene structure. However, the capacitance of M3B metal line is higher than that of other lines in vacuum corridor structure. The reason is that the capacitance between top ground plane and M3B is much higher than that of conventional structure because the dielectric constant of vacuum corridor structure is much smaller so that area effect is more critical than dielectric effect in this simulation structure. Generally, the capacitance of M2B is the much higher than that of other metal lines. So this capacitance is used for our simulation. The capacitance can be reduced by 56% compared to that of conventional dual damascene structure.

The total and mutual capacitances of the M2B line are extracted. All the specific parameters of each generation are followed by Table 5.2 in conventional structure. Vacuum corridor structure has the same geometry as the conventional structure except vacuum corridor parts. Metal space is divided into one vacuum gap and two support dielectric beam of equal width. A thicker vacuum gap width leads to lower support dielectric beam width at the fixed metal space. Figure 5.19 shows total and mutual capacitances of several vacuum gap widths. X axis represents vacuum gap percentage from 20% (8nm) to 80% (32nm) at 40nm metal width and space. The dielectric constant of the support beam dielectric is 2.9. A thicker vacuum gap width leads to lower capacitance but lower structural stability. Thus, 60% (24nm) of vacuum gap width is

chosen to other simulations. Total and mutual capacitances with vacuum gap (= 24nm) can be decreased by 53% and 55%, respectively compared to those of conventional structure.

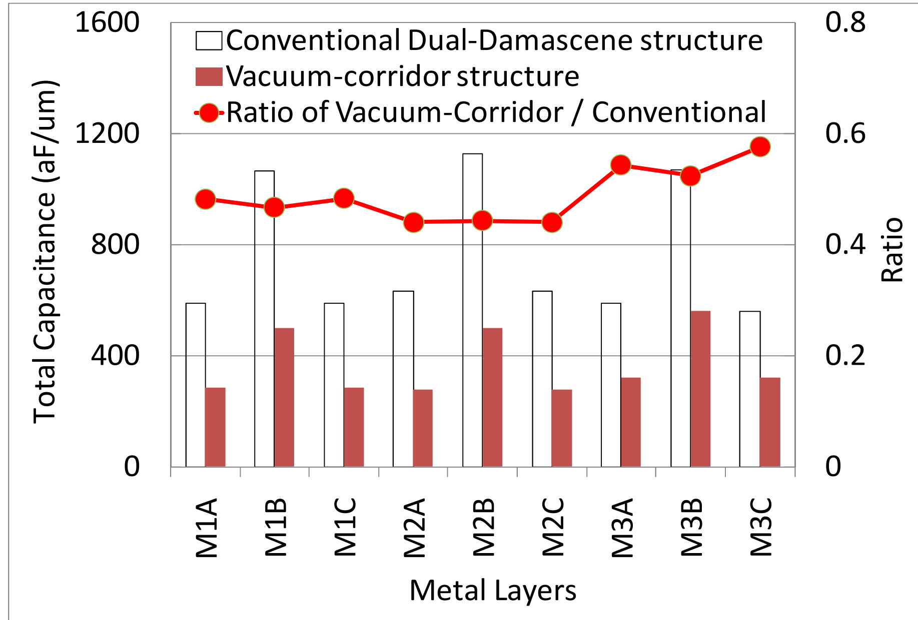


Figure 5.18: Total capacitance versus each metal layer. The ratio is the total capacitance of vacuum-corridor over that of conventional dual damascene structure. Metal width = 40nm

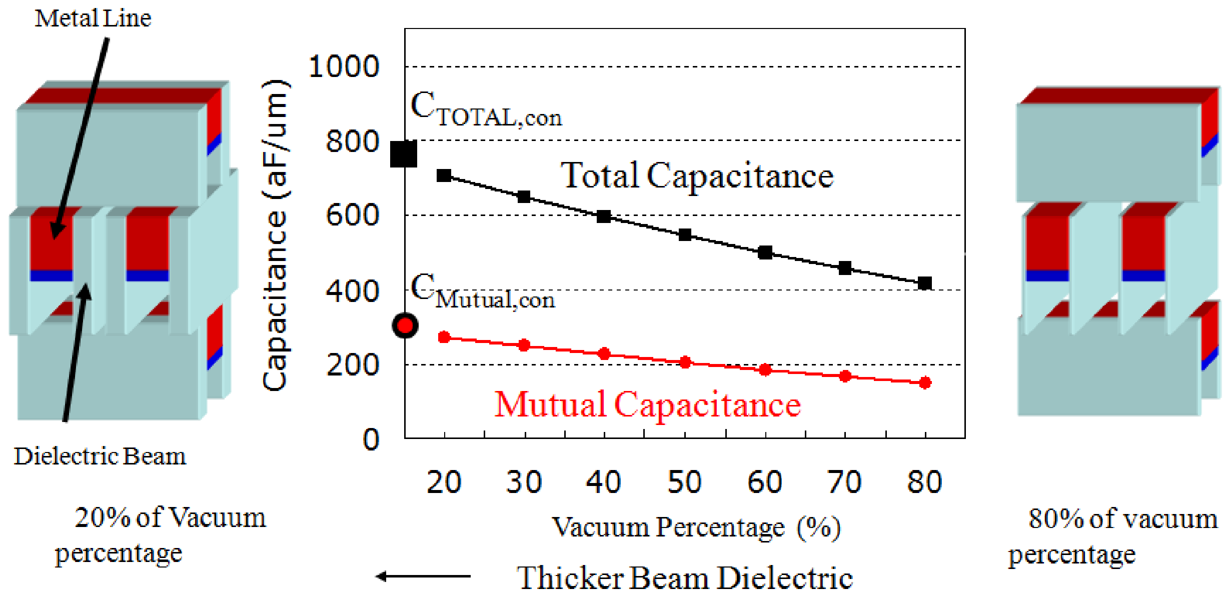
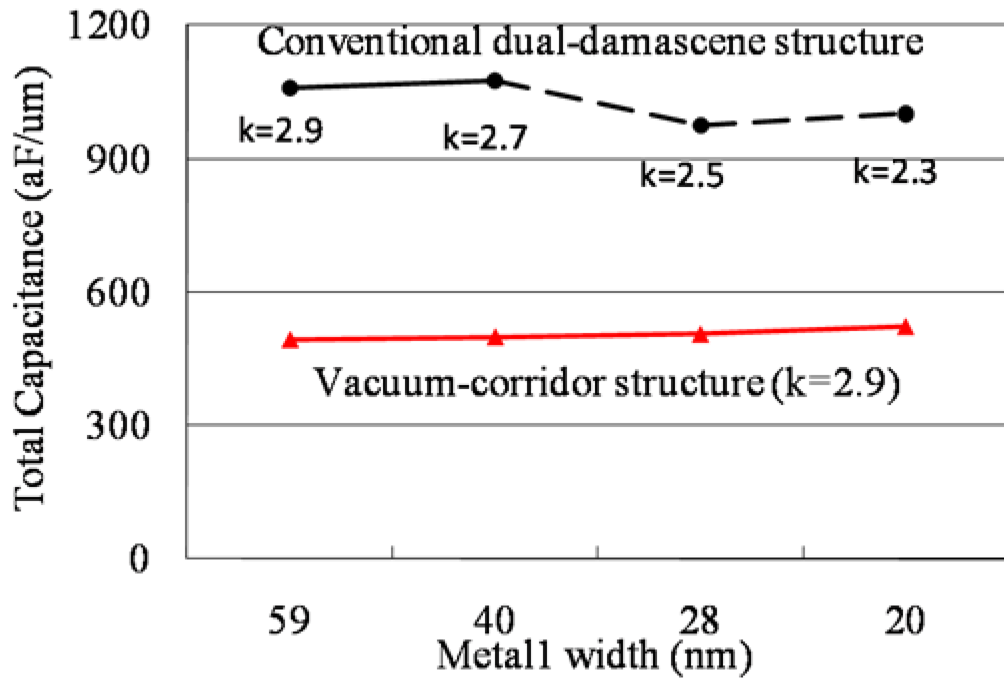
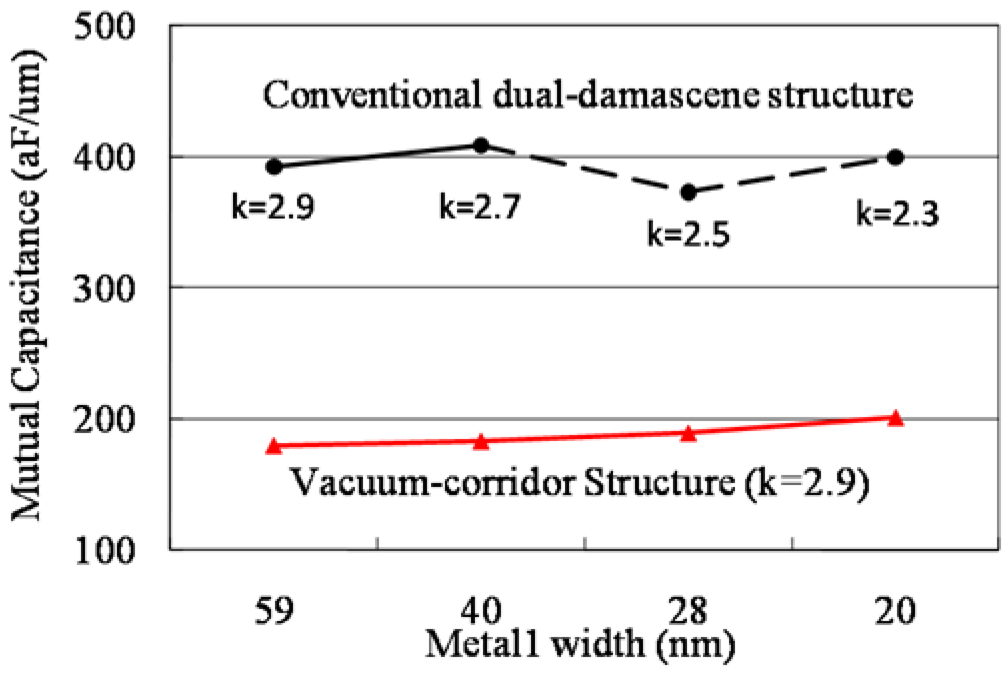


Figure 5.19: Total and mutual capacitances are decreased as vacuum gap width is increased. Total capacitance of only 20% of vacuum gap width (8nm) with higher k (k=2.9) is much less than that of conventional structure with lower k (k=2.7). Metal width is 40nm.



(a)



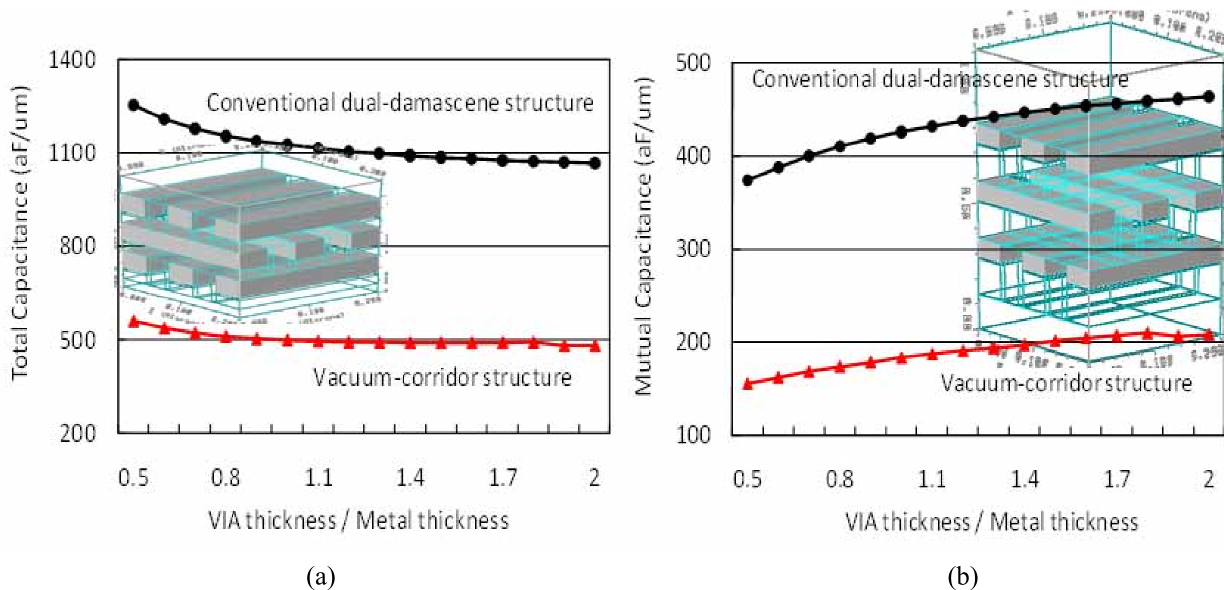
(b)

Figure 5.20: Total (a) and mutual (b) capacitances should be increased as metal width is decreased without scaling dielectric constant. Total and mutual capacitances of vacuum corridor interconnect using conventional dielectric (k=2.9) are still lower than those of conventional interconnect using ultra low dielectric (k=2.3).

Figure 5.20 shows total and mutual capacitances at each generation. All the specific parameters are followed by Table 5.2 (ITRS specifications). From 59nm to 20nm of metal widths, dielectric constant of IMD should be reduced from 2.9 to 2.3 according to ITRS specifications. However, there is no solutions below effective k = 2.9. The total and mutual capacitances of vacuum corridor structure is slightly increased with scaling due to using the same dielectric support beam (k=2.9). At 20nm metal width, both the total capacitance and the mutual capacitance of the vacuum-corridor structure (with IMD k=2.9) are superior to those of the conventional structure even if a solution is found for implementing oxide k=2.3. Total and mutual capacitances can be reduced by 48% and 50% at 20nm of metal width compared to those of conventional structure (k=2.3). That means current dielectric technique can be extended to below 10nm technology using vacuum sheath interconnect with high dielectric material (k=2.9).

All the simulation of Figure 5.18, 5.19 and 5.20 assume that via height is the same as the metal thickness. If via over metal thickness is 0.5, the height of via is half of the metal thickness and if it is 2, the height of via is twice of the metal thickness. The structures of figure 5.21 (a) and (b) show the structure of via over metal thickness is 0.5 and 2, respectively. As the height of via is increased, total capacitance is decreased but mutual capacitance is increased. It is notable that both the total and mutual capacitances of the vacuum corridor structure are less sensitive to the via height than those of the conventional structure. Even if the height of via is changed a lot, the effects of the vacuum corridor interconnect are still same. Total and mutual capacitances can be reduced by 56% and 57%, respectively at 40nm of metal width.

Figure 5.22 shows the RC delay time versus the metal thickness. Metal width and space are 40nm. If the metal thickness is higher, the delay is smaller due to reducing metal resistance but the vacuum corridor interconnect scheme always has approximately 47% of the delay of the conventional interconnect scheme.



(a) (b)

Figure 5.21: (a) Total capacitance (speed) is decreased as the thicker IMD. (b) Mutual capacitance (cross-talk noise) is increased as the thicker IMD. Metal width is 40nm

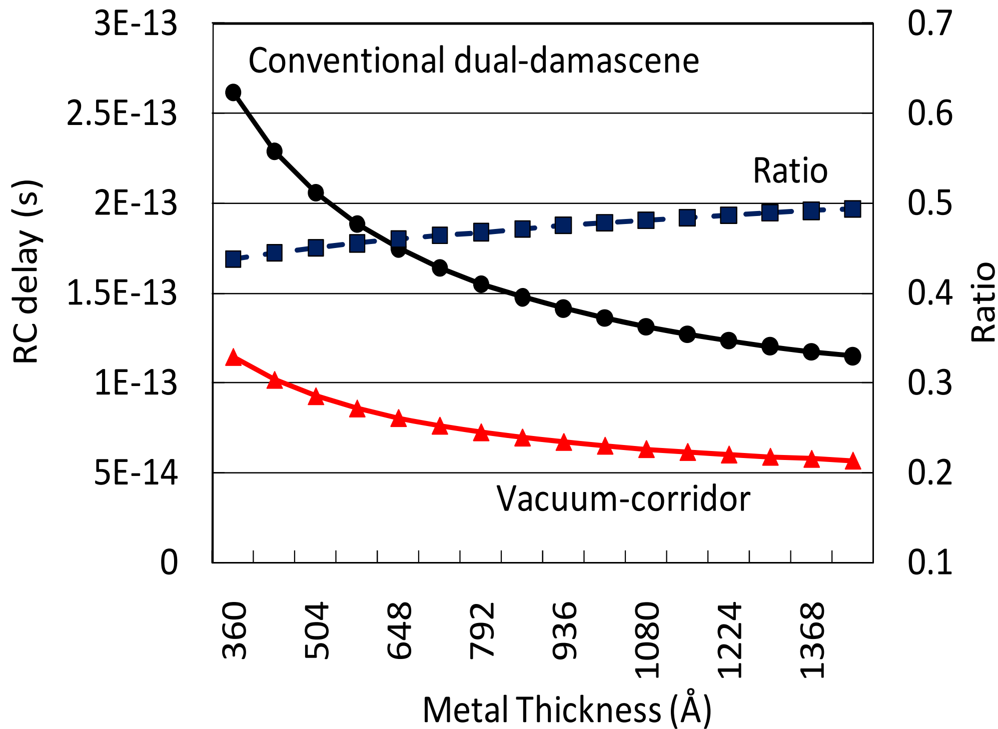


Figure 5.22: RC delay is decreased as metal thickness is increased. Metal width and space are 40nm.

5.6 Reasonable Expectation

According to all the simulations, table 5.3 shows the effective dielectric constant of the vacuum sheath interconnect can be reduced to 1.9 and 1.76 using support beam having 3.3 and 2.9 dielectric constant, respectively, for a 40% vacuum gap design (two of 20% vacuum gaps) in the subtractive etch interconnect. ITRS reported there were no solutions below effective k = 2.9 so that total and mutual capacitance would be much increased as metal width is decreased below 40nm. However, the proposed vacuum sheath interconnect scheme is extendable to 14nm of metal width without requiring a dielectric technology with k < 2.9.

Table 5.4 shows the effective dielectric constant of the vacuum corridor interconnect can be reduced to 1.65 and 1.49 using support having 2.9 and 2.25 dielectric constant, respectively, for a 60% vacuum gap design in the dual damascene interconnect. ITRS reported the bulk dielectric constant should be reduced to below 1.74 to meet the requirements of 40nm metal width. At 20nm metal width generation, we should use dielectric constant of IMD=1.35 because we have to meet ITRS specs (effective dielectric constant=2.3). It will be extremely difficult for developing ultra low dielectric constant. However, this novel vacuum corridor structure makes the effective dielectric constant much lower even if we use present dielectric constant material. The proposed vacuum corridor dual damascene interconnect is extendable to 11nm of metal width without requiring a dielectric technology with k<2.9.

	Metal Width	175nm	122nm	90nm	59nm	40nm	28nm	20nm
ITRS specification	Metal Space	175nm	122nm	90nm	59nm	40nm	28nm	20nm
	Metal A/R	1.6	1.6	1.7	1.8	1.8	1.9	2.0
	Metal Thickness (Å)	2800	1952	1530	1062	720	532	400
	Effective k	2.9~3.3	2.9~3.3	2.9~3.3	2.9~3.3	<u>2.6~2.9</u>	<u>2.4~2.8</u>	<u>2.1~2.5</u>
Assumption	IMD Thickness (Å)	5600	3904	3060	2124	1440	1064	800
Simulation Results (Vacuum sheath)	Effective k (k_{IMD} : 3.3)	.	.	1.88	1.9	1.9	1.91	1.92
	Effective k (k_{IMD} : 2.9)	.	.	1.74	1.75	1.76	1.77	1.78

Table 5.3: Effective dielectric constant of vacuum sheath interconnects with 40% vacuum gaps designs for the subtractive etch interconnect.

Metal Width (nm)	59	40	28	20
ITRS bulk dielectric k	2.25	<u>**1.74**</u>	<u>**1.81**</u>	<u>**1.35**</u>
ITRS effective dielectric k	2.9	2.7	2.5	2.3
The effective k of Vacuum-corridor structure (beam k: 2.9)	1.62	1.66	1.62	1.65
The effective k of Vacuum-corridor structure (beam k: 2.25)	1.47	1.50	1.47	1.49

Table 5.4: Effective dielectric constant of vacuum corridor interconnects with 60% vacuum gaps design for the dual damascene interconnect.

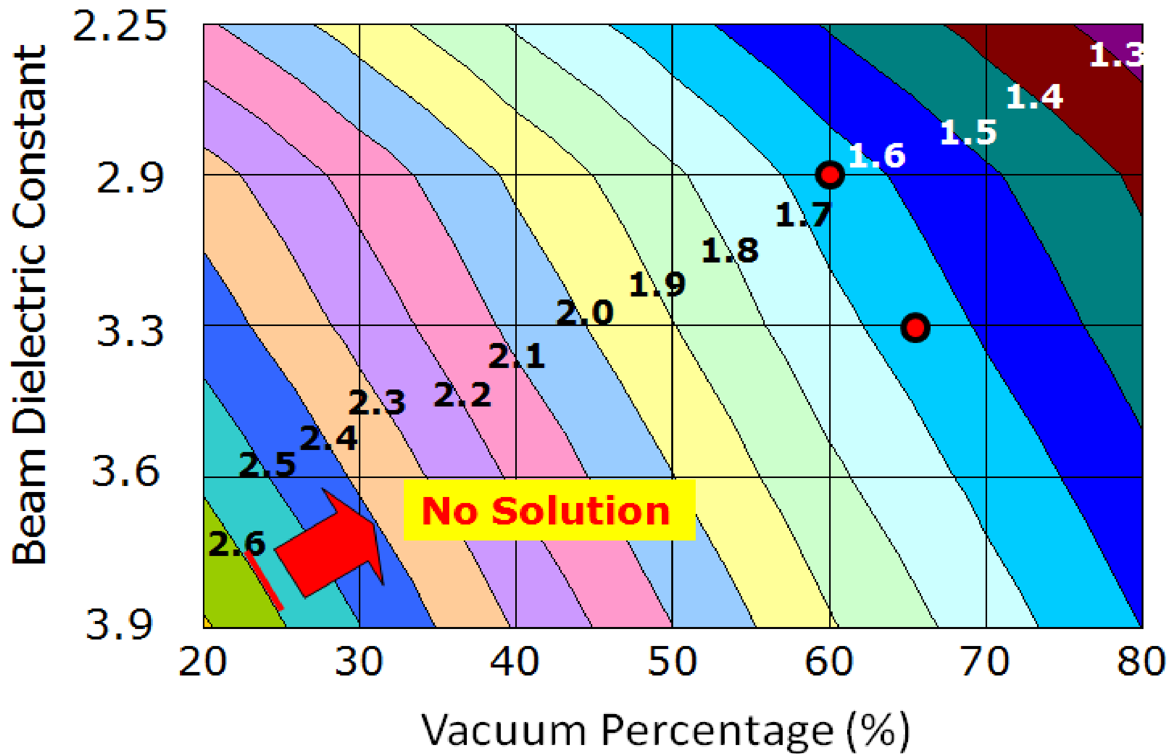


Figure 5.23: The effective dielectric constants are indicated with vacuum gap percentage and beam dielectric constant. Metal width and space are 40nm.

At 40nm metal width, there are lots of solutions to achieve lower effective dielectric constant. Y axis shows the conventional dielectric technology and X axis shows vacuum percentage. If the effective dielectric constant 1.65 is required, 60% vacuum gap design and 2.9 beam dielectric are needed or 65% vacuum gap design and 3.3 beam dielectric are required which are shown in Figure 5.23 (two dots). For example, if the effective dielectric constant 2.0 is required, we can make it with 5 different beam dielectric constants: beam dielectric constants 3.9, 3.6, 3.3, 2.9, 2.25 are required vacuum percentage 55%, 50%, 45%, 38%, 27%, respectively.

5.7 Summary

Reducing the interconnection capacitance will be an increasingly important way to improve the circuit speed, switching energy/power, cross-talk noise and electromigration reliability. As the technology node gets smaller, the subtractive etch interconnect should be changed to the dual damascene copper interconnect. However, dense memory which has only 3 or 4 metal lines still uses the subtractive etch interconnect. Thus, we proposed two novel interconnect structures with vacuum gaps.

A novel subtractive etch interconnect with vacuum (air) gaps structure is proposed [5.20]. Every metal line is surrounded by a vacuum sheath on all sides and supported on the bottom by a series of solid dielectric beams. The vias are also surrounded by vacuum sheaths. Computer simulation shows that the total capacitance of this interconnect scheme is reduced by about 45%

and the RC delay is decreased about 55%. The effective dielectric constant can be reduced to about 1.78 using existing dielectric with k=2.9.

Another novel dual damascene copper interconnect with vacuum gaps structure is proposed [5.21]. Every metal line which has two support beams is surrounded by vacuum corridor. The vacuum corridor structure has not only lower effective capacitance but also higher stability of structure. Raphael simulation shows that the total capacitance is reduced by about 56% and the RC delay is decreased about 53%. The effective dielectric constant can be reduced to about 1.65 using existing dielectric with k=2.9. The proposed vacuum corridor scheme is easily extended to 11nm of metal width without requiring a dielectric technology with k = 2.9.

Heat dissipation problem of these vacuum gap structures is not critical since all the dielectric beams are connected to each other and metal lines are contacted the dielectric beam material. This dielectric beam material is not porous material with low thermal conductivity but conventional material with relatively high thermal conductivity [5.22]. And the thermal conductivity of vacuum gap with helium (0.142W/(m·k)) is six times higher than that of air (0.024 W/(m·k)) [5.23]. Electromigration reliability of vacuum (air) gap structure is better than that of the conventional structure because of stress relaxation [5.24].

5.8 References

[5.1] International Technology Roadmap for Semiconductors for Interconnect, 2008

[5.2] Jens Lienig, "introduction to electromigration-aware physical design", Proceedings of the 2006 international symposium on Physical design, 2006

[5.3] D. James, T. Watanabe, K. Yamada, "EFFECTS OF METHODS OF ADDING COPPER ON THE STRENGTH OF SINTERED ALUMINUM COPPER ALLOYS", INT J POWDER METALL. Vol. 4, no. 3, pp. 37-47. July 1968

[5.4] S. Vaidya, A.K. Sinha, "Effect of Texture and Grain Structure on Electromigration in Al-0.5%Cu Thin Films", Thin Solid Films, Volume 75, No. 3, pp.253-260, 1981

[5.5] Young-Chang Joo and Carl V. Thompson, "Electromigration-induced transgranular failure mechanisms in single-crystal aluminum interconnects", Journal of Applied Physics, Volume 81, Issue 9, 1997

[5.6] E. Arzt and W.D. Nix, "A model for the effect of line width and mechanical strength on electromigration failure of interconnects with "near-bamboo" grain structures", Journal of Materials Research, Volume 6, Issue 4, 1991

[5.7] Onoda, Hiroshi; Kageyama, Makiko; Hashimoto, Keiichi, "Al-Si crystallographic-orientation transition in Al-Si/TiN layered structures and electromigration performance as interconnects", Journal of Applied Physics, Volume 77, No. 2, pp.885-892, 1995

[5.8] A.V. Vairagar, S.G. Mhaisalkar, and Ahila Krishnamoorthy, "Electromigration behavior of dual-damascene Cu interconnects—Structure, width, and length dependences", Microelectronics Reliability, Volume 44, Issue 5, pp.747-754, May 2004

[5.9] B. Shieh, K. C. Saraswat, J. P. McVittie, S. List, S. Nag, M. Islamraja, and R. H. Havemann, "Air-Gap Formation During IMD Deposition to Lower Interconnect Capacitance", IEEE Electron Device Letters, VOL. 19, NO.1, January 1998

[5.10] R. Daamen, P.H.L. Bancken, V.H. Nguyen, A. Humbert, G.J.A.M. Verheijden, R.J.O.M. Hoofman, “The evolution of multi-level air gap integration towards 32nm node interconnects”, Microelectronic Engineering, Volume 84, pp.2177-2183, 2007

[5.11] M. B. Anand, Masaki Yamada, and Hideki Shibata, “Use of Gas as Low-k Interlayer Dielectric in LSI’s: Demonstration of Feasibility”, IEEE Transactions on Electron Devices, VOL. 44, NO. 11, November 1997

[5.12] L.G. Gosseta, A. Farcyb, J. de Pontcharrac, Ph. Lyanc, R. Daamend, G.J.A.M. Verheijdend, V. Arnalb, F. Gaillardc, D. Bouchuc, P.H.L. Banckend, T. Vandeweyerd, J. Michelond, V. Nguyen Hoangd, R.J.O.M. Hoofmand and J. Torresb, “Advanced Cu interconnects using air gaps”, Microelectronic Engineering, Volume 82, pp.321-332, December 2005

[5.13] Jonathan Faltermeier, Andreas Knorr, Robert Talevi, Heidi Gundlach, Kaushik Arun Kumar, Gregory G. Peterson, Alain E. Kaloyeros, John J. Sullivan, and James Loan, “Integrated plasma-promoted chemical vapor deposition route to aluminum interconnect and plug technologies for emerging computer chip metallization”, Journal of Vacuum Science & Technology, Volume 15, Issue 5, 1997

[5.14] Sailesh M. Merchant, Seung H. Kang, Mahesh Sanganeria, Bart van Schravendijk and Tom Mountsier, “Copper interconnects for semiconductor devices”, JOM Journal of the Minerals, Metals and Materials Society, Volume 53, Number 6, pp.43-48, 2001

[5.15] Chung-Hui Chen, Yean-Kuen Fang, Chun-Sheng Lin, Chih-Wei Yang, Jang-Cheng Hsieh, “A novel multi-level interconnect scheme with air as low K inter-metal dielectric for ultradeep submicron application”, Solid-State Electronics 45 (2001) pp.199-203

[5.16] RAPHAEL Interconnect Analysis Program Reference Manual, Synopsys, Mountain View, CA, September 2007

[5.17] RAPHAEL Interconnect Analysis Program Tutorial, Synopsys, Mountain View, CA, December 2006

[5.18] Masao Takahashi, Masanori Hashimoto, Hidetoshi Onodera, “Crosstalk Noise Estimation for Generic RC Trees”, 2001 IEEE International Conference on Computer Design (ICCD'01), September 2001

[5.19] International Technology Roadmap for Semiconductors for Interconnect, 2007

[5.20] Jemin Park and Chenming Hu, "Vacuum-Sheath Interconnect Structure for Dense Memory", Electronics Letters, Volume 45, Issue 25, pp.1294-1296, 3 December 2009

[5.21] Jemin Park and Chenming Hu, "An Air-Corridor Interconnect Structure", VLSI MULTILEVEL INTERCONNECTION CONFERENCEVMIC, pp.229-234, Fremont CA, October 2008

[5.22] Chuan Hu, Michael Morgen, Paul S. Ho, Anurag Jain, William N. Gill, Joel L. Plawsky, and Peter C. Wayner, “Thermal conductivity study of porous low-k dielectric materials”, Applied Physics Letters, Volume 77, Issue 1, 2000

[5.23] F.G. Keyes, “THERMAL CONDUCTIVITY OF GASES”, Transactions of the American Society of Mechanical Engineers, Volume 76, 1954

[5.24] Young-Bae Park and In-Su Jeonb, “Mechanical stress evolution in metal interconnects for various line aspect ratios and passivation dielectrics”, Microelectronic Engineering, Volume 69, Issue 1, pp.26-36, August 2003

Chapter 6

Conclusions

6.1 Summary of Work

This work has focused on improving CMOS speed and power with reducing capacitance. Vacuum gap structure is a good option to decrease capacitance without researching new low-k materials which have poor structure stability. This technology can be used for both FEOL and BEOL process.

In Chapter 2, novel vacuum spacer transistors were simulated using 2D and 3D process and device simulator. We proposed two types of vacuum spacer transistors: Vacuum spacer transistors in the gate first process with non-SAC and SAC processes. The gate capacitances were derived from analytical framework and Miller effect is shortly reviewed to use in 3D mixed-mode simulations. Even if the on current of vacuum spacer transistor was slightly lower than that of conventional spacer transistor, the speed and power consumption were much improved due to reducing the gate capacitance. The effect of vacuum spacer with SAC process was improved a lot because of lower k and short distance between gate and contacts. Surprisingly, the performance of the vacuum spacer with SAC process transistor was much higher than that of the conventional oxide spacer with non-SAC transistor for speed, power, and area aspects.

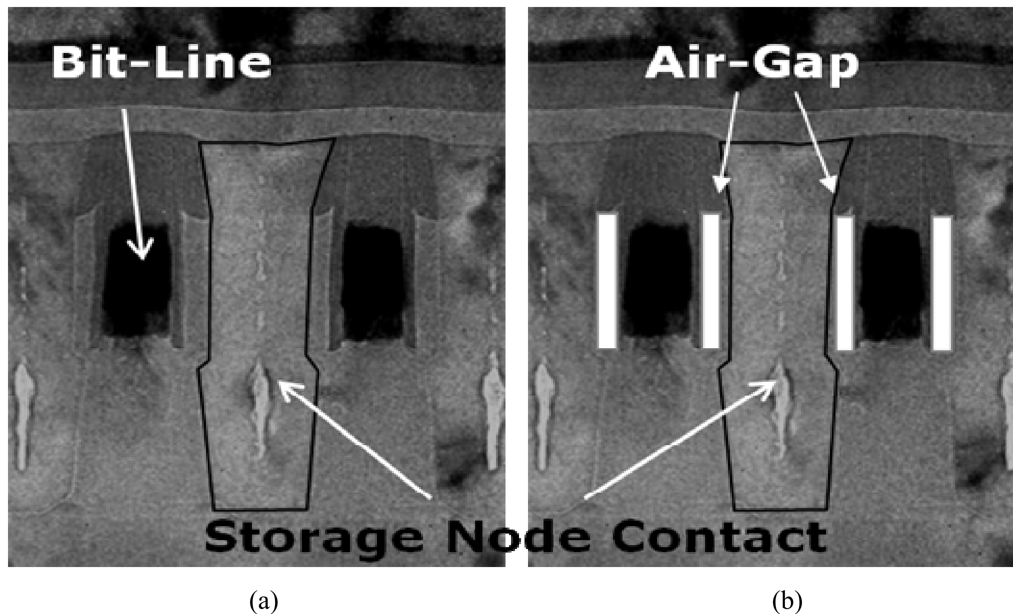
In Chapter 3, this vacuum spacer technology can be also used in gate last process or linear contact process. The linear contact process has been used to reduce the contact resistance but the capacitance between gate and contacts was increased due to increasing the area so that the speed was not improved much as we had expected. Thus, vacuum spacer is particularly attractive for future linear contact devices which has larger gate to contact capacitive coupling. In high performance devices, the effect of the vacuum spacer was also attractive for the speed and power. However, in low stand-by power devices, the degradation of on current should be carefully considered when the low-k spacer material is used. And this technology can be used for the raised S/D or FinFET processes which have a higher capacitance between gate and contacts.

In Chapter 4, we proposed a novel corner spacer transistor which a small portion of high-k inner spacer material can improve the on and off current and a large portion of low-k outer spacer material can reduce the gate capacitance. The corner spacer transistor in high performance devices was improved for both speed and power. Especially, the effect of the corner spacer was much improved in low stand-by power device since this transistor have S/D underlapped profile and shallow S/D extension region.

In Chapter 5, we proposed novel vacuum gaps processes of both the subtractive etch interconnect and the dual damascene interconnect. Reducing the interconnection capacitance will be an increasingly important way to improve the circuit speed, switching energy/power, cross-talk noise and electromigration reliability. Vacuum gap interconnect was more attractive than low-k material interconnect because of high structural stability and lower effective dielectric constant.

6.2 Future Directions

It is the firm belief of this researcher that the vacuum spacer transistor and the vacuum gap interconnect can and will be experimentally demonstrated. Some novel processes will be needed to demonstrate this technology easily. Firstly, the below 16nm photolithography process is needed because the effect of the vacuum spacer transistor is more and more attractive below 16nm gate length. Secondly, a new sacrificial material is also needed to remove more easily. Thirdly, new sealing materials and process conditions to make larger air-gap is developed.



(a) (b)

Figure 6.1: Vertical view of bit line and storage node contact in DRAM cell structure. (a) An example of low-k material is located between bit-line and contact. (b) An imaginary vertical view of air gap.

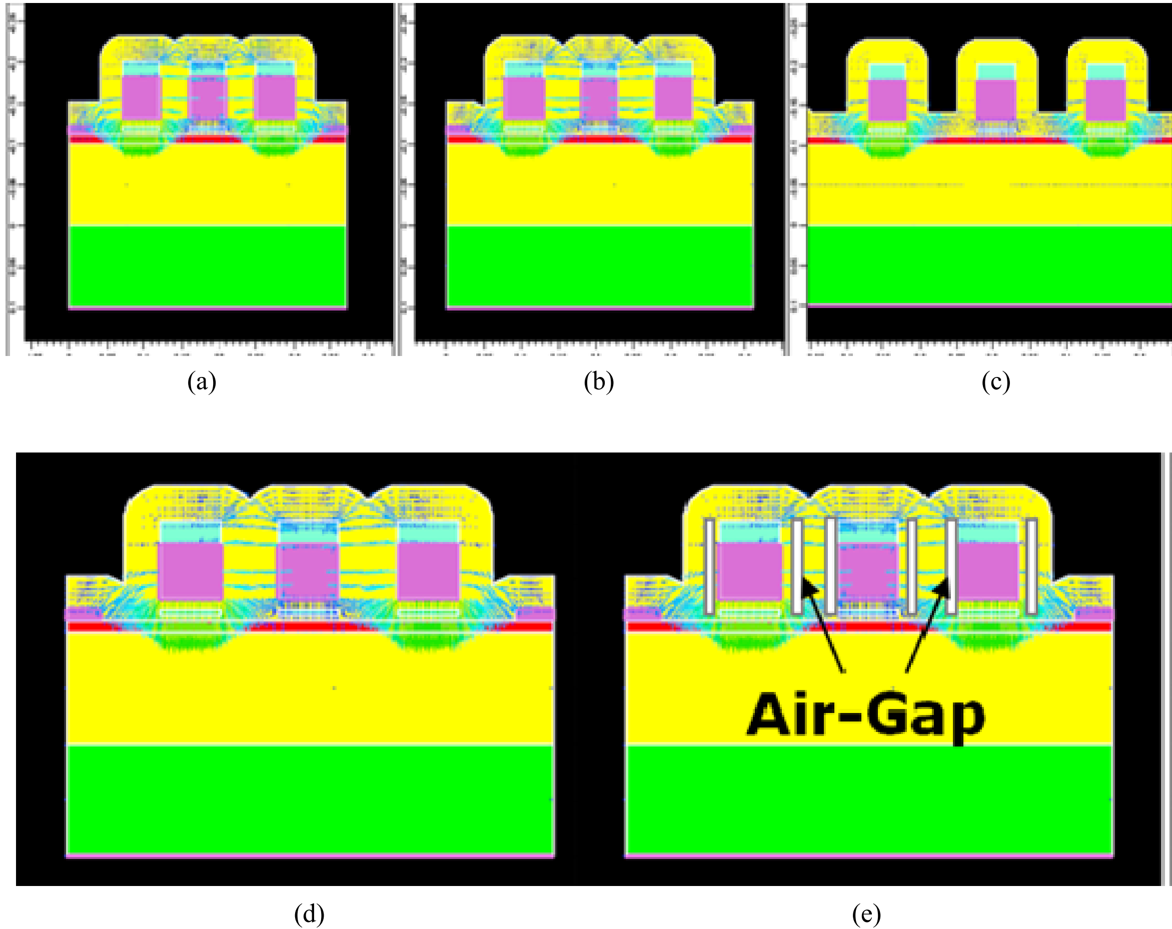


Figure 6.2: Vertical view of NAND flash cell structure. (a) –(c) the coupling effect is increased as the space between cell transistors is decreased. (d) the conventional cell structure (e) the cell structure with air-gaps.

In DRAM processes, this vacuum gap technology can be applied to the cell transistor, bit-line, and interconnect processes. The cell transistors usually have SAC process because of small density so that the vacuum spacer is very attractive. The capacitance of bit-line is important to bit-line sensing margin. If the vacuum gap technology is applied to the bit-line process, the bit-line capacitance can be easily reduced as shown in Figure 6.1.

In NAND flash memory process, the capacitance of the cell transistor is important. If the vacuum spacer is used to the NAND cell transistor, we can decrease the neighboring cell coupling effect which is called the Yupin effect. Figure 6.2 shows that the Yupin effect is increased as the technology node gets smaller so that the vacuum spacer technology gets more and more important for future devices.