Linear Propagation Methodology in Compact Variability Modeling

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Linear Propagation Methodology in Compact Variability Modeling

by Ying Qiao

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Abstract

As integrated circuit manufacturing enters the nanometer regime, system performance variations are increasingly introduced through the growing complexity of the processing steps. Compact variability modeling has been widely studied for statistical circuit simulation to connect technology and design activities. Conventional statistical compact model parameter extraction methodology is not aware of the hybrid-hierarchical variation structure in the manufacturing processes. In this work we propose an efficient variability aware compact model characterization methodology based on variance linear propagation. Hierarchical spatial variability patterns of selected compact model parameters are directly calculated from transistor array test structure current/voltage measurements.

In our implementation, spatial variability models of selected compact model parameters are created by linear regression on spatial pattern fitting coefficients with spatially modified sensitivity matrix. Good match is realized between our results and compact model parameter reference set obtained by full-wafer, direct model parameter extraction on a simple compact model and 65nm SOI industrial measurement data. Proper selection of both variability-aware model parameters and sensitive electrical measurements are also studied in this thesis work. Extensions on the proposed methodology can be applied to more complex compact models and more advanced hybrid-hierarchical variability models.

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Chapter 1

Introduction

1.1 Motivation

Reductions in cost-per-gate and improvements in overall integrated circuit performances have pushed the silicon manufacturing into the nanometer technology era. However, the benefits of aggressive scaling on transistor feature sizes are diminishing due to the variations introduced through the increasingly complicated processing steps. Though compact variability modeling has been studied ever since 1990s [1-1], the impact of both random [1-2] and systematic [1-3] variations has evolved dramatically with new manufacturing techniques and transistor structures.

With restrictive layout design rules and limited transistor geometric diversity, simpler compact variability models for statistical circuit simulations establish a critical link between technology and design activities. Statistical circuit design requires concise and simple models capturing nominal, corner and distributional information of process variations. Conventional statistical

compact model characterization methodology, i.e. model parameter extraction, is not aware of the hybrid-hierarchical variation structure in the manufacturing processes. This motivated us to find a proper way of characterizing compact models used in statistical circuit simulation for accurate prediction on circuit performance deviations caused by process variations.

The flow of compact variability model characterization is shown below. Implied in this flow is the need for efficient test structures to capture key elements of process variability; and reliable characterization methods to extract variability-aware compact model parameters [1-4]; we will finally integrate these advanced compact variability models into the existing statistical circuit design flows. Therefore, in this thesis work, we propose and implement a linear propagation based method for compact model variability characterizations. Hierarchical spatial variability patterns of selected compact model parameters are directly calculated from transistor current/voltage measurements. Effectiveness and efficiency of our methodology are evaluated, while possible improvements are also discussed.

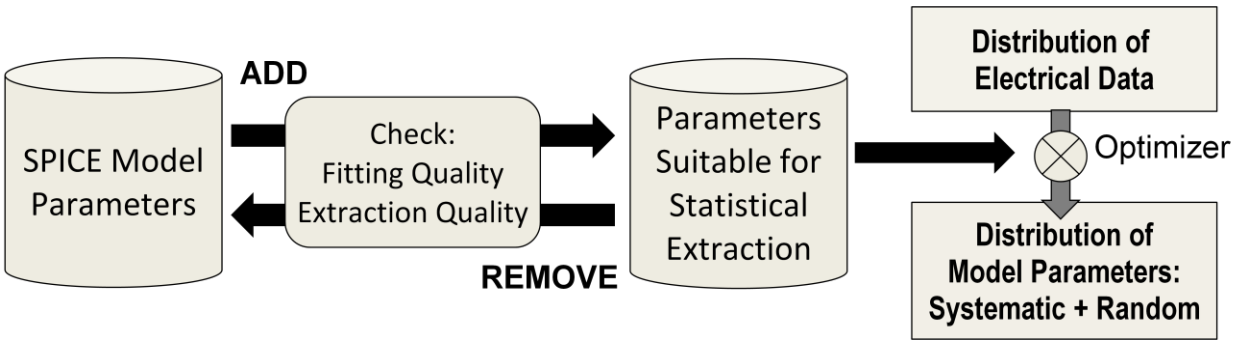

Figure 1-1 Compact Variability Model Characterization Flow

1.2 Thesis Organization

The remainder of this thesis is organized as follows. A review of the statistical compact modeling and recent work on compact variability model parameter extraction will be presented in Chapter 2. A spatial variability pattern linear propagation method is proposed in Chapter 3 for compact variability model characterization. Test bench implementation along with simulation results and verifications are also presented in Chapter 3. Next, selection of extractable compact model parameters and measurement data points used in our proposed methodology are discussed in Chapter 4. Finally, Chapter 5 will present a summary of the work and give conclusions, along with possible directions for future work.

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Chapter 2

Statistical Compact Modeling

2.1 Compact Modeling for Statistical Circuit Design

With the aggressive scaling in the manufacturing society, circuit designers rely more on the statistical design methodology for overall yield guarantee. Most analog and digital circuit designers working on the cutting-edge technology employ SPICE-based simulators to perform complete statistical verification on the nominal design. Monte Carlo analyses on primitive cells combined with statistical static timing analysis are widely used in digital IC designs, while worst-case corner analysis leads the statistical simulation in analog/mixed signal designs. For both circuit designers and technology developers, compact models establish a critical link between the two societies [2-1].

Development of a truly physical and predictive compact model equation that covers geometry, bias, temperature, DC, AC, RF, and noise characteristics becomes a major challenge when

technology goes into the nanometer regime. Moreover, as for statistical circuit simulation accuracy and efficiency, compact model developers are required to provide proper corner model parameter files as well as model parameter variability distribution files [2-2]. This imposes more challenges onto the model characterization and parameter extraction procedures.

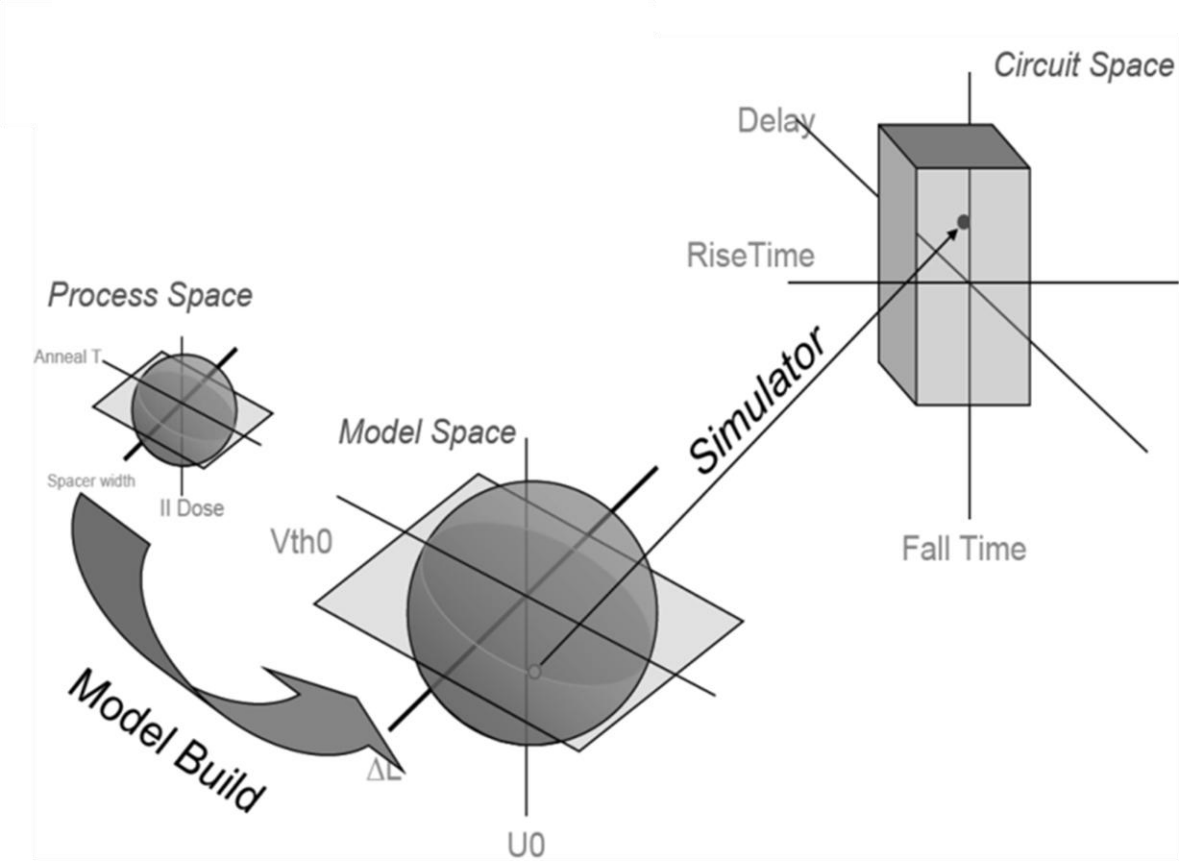

Figure 2-1 Compact Modeling for Statistical Circuit Design Scheme [2-3]

2.2 Statistical Compact Model Characterization

Several statistical compact modeling techniques are reviewed in this section with more focus on the compact model parameter characterizations. For better conceptualization of the statistical

variations in the IC manufacturing, a four-level scheme is used to demonstrate different statistical modeling levels [2-4]. Modeling at the SPICE compact model parameters ***s*** is the most common way; while with physics-based predictive compact models, statistical compact modeling is more preferably done at the physical process parameters ***p*** level, which has fewer variables and simpler variability correlation structure. We will discuss more on this topic in the next chapter.

Table 2-1 Statistical Variations Modeling Levels

Level	Examples	Number	Comment
process inputs ***i***	implant doses and energies anneal ramps, times, temperatures oxidation ramps, times, temperatures	100's	Uncorrelated
Process parameters ***p***	R: ρ_S, $\Delta_L r$, $\Delta_W r$ MOS: N_b, T_{ox}, V_{fb}, Δ_L, Δ_W BJT: ρ_{sbe}, N_{epi}, Δ_{Le}, $J_{be}i$, ρ_{sb}	10's	Nearly Uncorrelated
SPICE parameters ***s***	R: ρ_s, Δ_{Lr}, Δ_{Wr} MOS: Nb, Tox, Vth, ΔL, ΔW BJT: *IS, BF, CJE, VAF, RB, IKF*	100's to 1000's	Highly Correlated, poor statistically
Device/circuit performances ***e***	Device: R, V_{th0}, I_{dsat}, g_o, I_c, β Circuit: τ_p, P_{dis}, V_{ol}, ϕ_m, P_{1DB}	∞	

2.2.1 Generic Compact Variability Model Equation

Most commonly used statistical compact models fall into the following two categories: 1) corner models for circuit worst-case analysis and 2) variability distributional models for Monte Carlo circuit simulation. Industrial standard compact models [2-5], including BSIM, PSP, HiSIM

and EKV, ACM, are extended to generate statistical compact sub-models or parameter files in either category for statistical circuit design.

A generic compact variability model equation can be used for statistical compact modeling with any specific nominal compact models [2-6].

$$\begin{pmatrix} \Delta \boldsymbol{p_1} \\ \vdots \\ \Delta \boldsymbol{p_m} \end{pmatrix} = \boldsymbol{G} \begin{pmatrix} \boldsymbol{x_1} \\ \vdots \\ \boldsymbol{x_M} \end{pmatrix} \ , \ \boldsymbol{G} = \begin{pmatrix} \boldsymbol{g_{11}} & \cdots & \boldsymbol{g_{1M}} \\ \vdots & \ddots & \vdots \\ \boldsymbol{g_{m1}} & \cdots & \boldsymbol{g_{mM}} \end{pmatrix} \tag{2.1}$$

$$\begin{pmatrix} \Delta y_1 \\ \vdots \\ \Delta y_n \end{pmatrix} \cong \boldsymbol{R} \begin{pmatrix} \Delta p_1 \\ \vdots \\ \Delta p_m \end{pmatrix} \ , \ \boldsymbol{R} = \begin{pmatrix} r_{11} & \cdots & r_{1m} \\ \vdots & \ddots & \vdots \\ r_{n1} & \cdots & r_{nm} \end{pmatrix} \ \ and \ \ r_{ij} = \left. \frac{\partial y_i}{\partial p_j} \right|_{p_0} \tag{2.2}$$

In this generic compact model variability model, $\boldsymbol{x_i}$ is an independent random variable of standard normal distribution. $\boldsymbol{\Delta p_i}$ is the deviation from nominal value of the $\boldsymbol{i^{th}}$ compact model parameter, while $\boldsymbol{\Delta y_i}$ is the deviation from global average of the $\boldsymbol{i^{th}}$ specific measurable electrical quantity of interest. Here, the $\boldsymbol{G}$ matrix represents the Gaussian variances in the parameters.

Though variations are more strictly described with hierarchy, e.g. global systematic effects due to manufacturing, plus local effects intrinsic to device structure [2-7], the simplified assumption in the model above is efficient-effective for single device statistical compact modeling. Moreover, different nominal compact models will generate different $\boldsymbol{R}$ sensitivity matrixes, which establish the basic equations for further statistical model characterization. The linearization in the model sensitivity calculation is valid for small process variation, i.e. small $\boldsymbol{x_i}$, which is common in mature or near-mature technology.

Though various nominal compact models are developed with different emphasis on device physics description and circuit performance prediction, the statistical extensions on model

equations are similar to the ones above. It is indeed the model characterization or parameter extraction methodology that distinguishes different statistical compact models.

2.2.2 Compact Variability Model Parameter Extraction

In addition to a generic compact variability model equation, we need to develop statistical model parameter characterization methodology [2-8] and a generic flow is shown below.

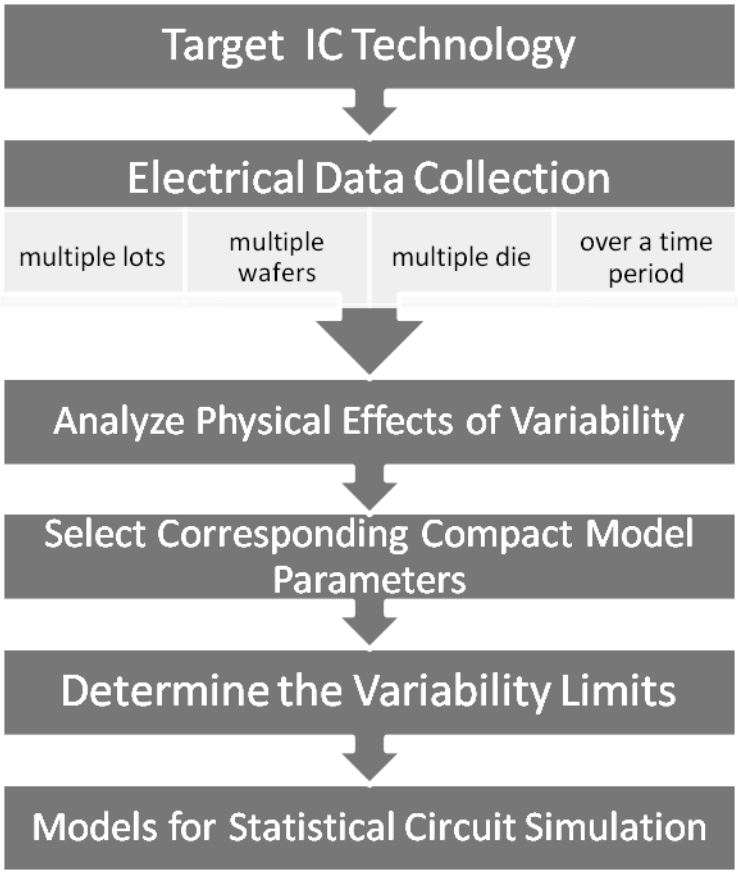

Figure 2-2 A Generic Statistical Compact Modeling Characterization Flow

As standard worst-case models first proposed in 1986 [2-9], researchers have developed optimized statistical compact corner models for statistical circuit design [2-10]. Variability distributional models proper for Monte-Carlo simulations are also developed with the help of

first principle, atomistic-level device simulations [2-11]. We will briefly review the pros and cons of several compact variability model characterization methods. This section establishes a good background for further discussion in the next chapter.

A Performance-Aware Model (PAM) [2-10] was recently proposed to generate accurate and application-specific, i.e. speed, power, gain, etc., model cards at any yield levels for both corner analysis and Monte Carlo simulation. PAM presents an improved methodology for determining the variations of the SPICE model parameters from both physical parameter variations and electrical-test data variations, as shown below.

PAM methodology demonstrates good compatibility with current EDA tools and industrial-standard nominal compact models. Pseudo electrical-test distribution data can be generated using predictive technology model to assist variation capturing in critical model parameters, e.g. V_{th} and mobility. However, as traditional corner model methodology, PAM only addresses the device intrinsic random variations but not systematic proximity-related variations. Statistical characterization and parameter extraction is also time-consuming due to the large number of application-specific model cards generated.

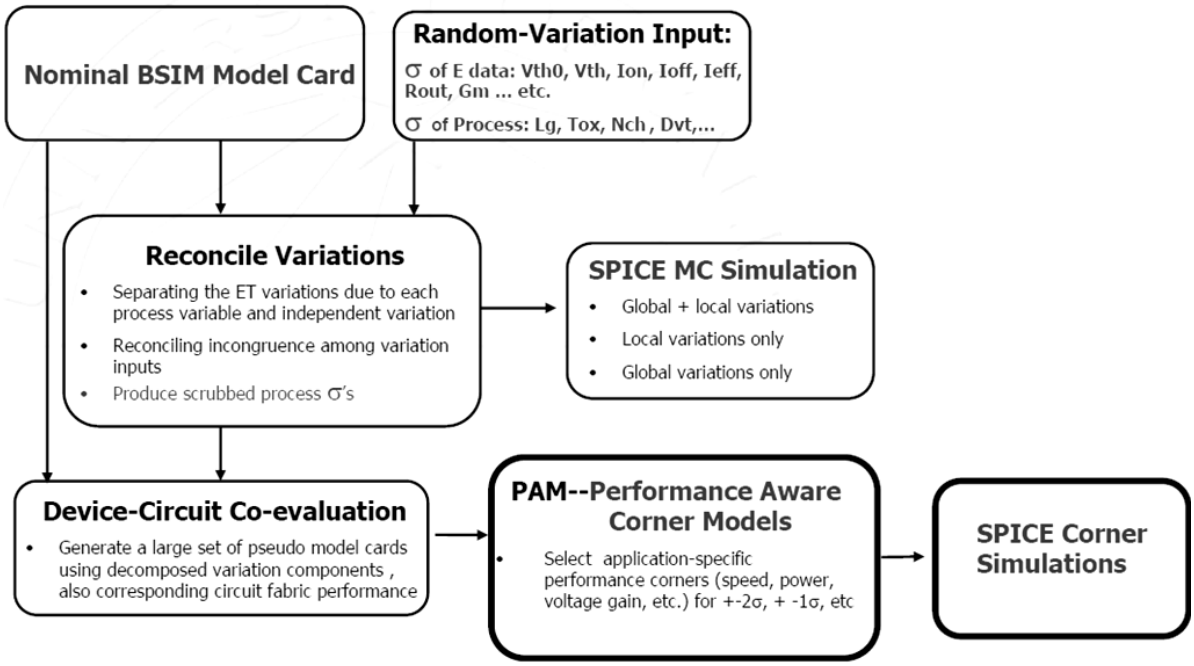

Figure 2-3 Standard flowchart for PAM variation characterization [2-10]

Atomistic-level device simulations have been recently used to establish a two-stage statistical compact model parameter extraction strategy to capture the process variations [2-11]. The procedure is shown below. A set of compact model parameters are chosen to capture the combined statistical variability sources. The final outcome of this direct statistical parameter extraction strategy is a statistical set of compact models with particular parameters representing physical variations within the devices.

By applying this strategy, the correlations established in the nominal compact model between key transistor figures of merit are well preserved. This leads to good correlation between simulated electrical performances and key statistical compact model parameters, which indicates that their physical meaning is maintained during statistical extraction. However, the lengthy simulation time of atomistic-level 3D device representation limits the application of this strategy.

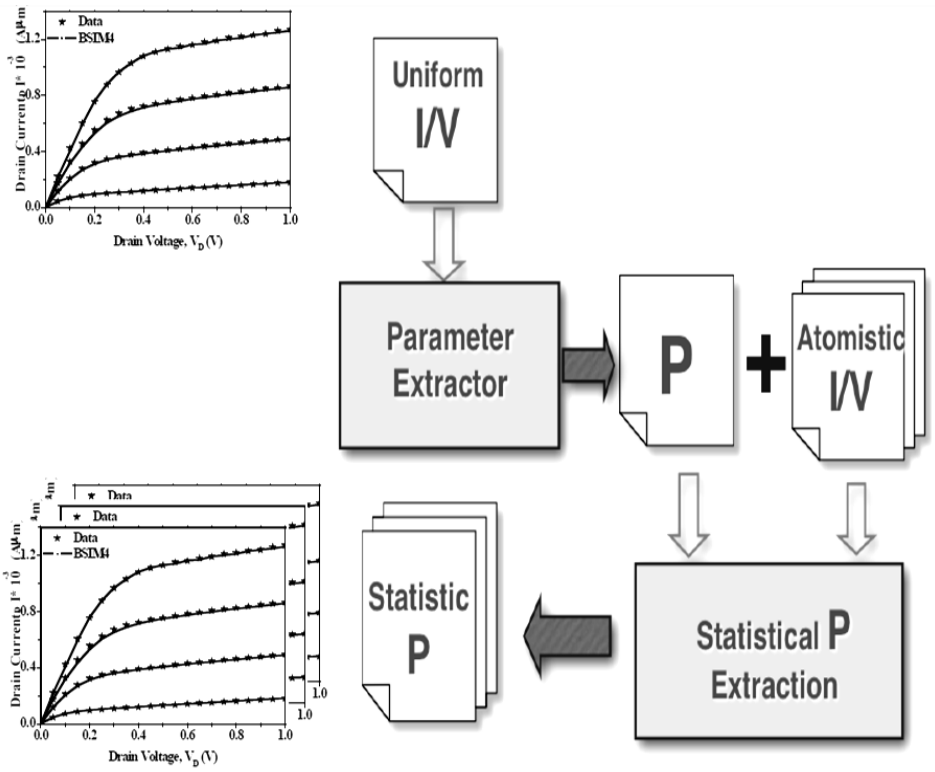

Figure 2-4 Atomistic-level Simulation Enabled Compact Model Parameter Extraction Scheme [2-11]

Process variability structure-aware compact model parameter statistical extraction procedure is newly developed by targeting general goodness of fit of all transistors across the wafers [2-12]. The proposed procedure, shown below, divides compact model parameters into groups and performs statistical extraction only on the group of compact model parameters which have first-order effects on device electrical performance and have weak correlation to process control measurements.

This method enables the hierarchical variability structure being preserved within the carefully selected set of compact model variability-aware parameters. Physical correlations between model parameters within the nominal compact model are also well preserved. However, the large number of needed individual device compact model parameter extractions increase the overall characterization time despite the small parameter subgroup size.

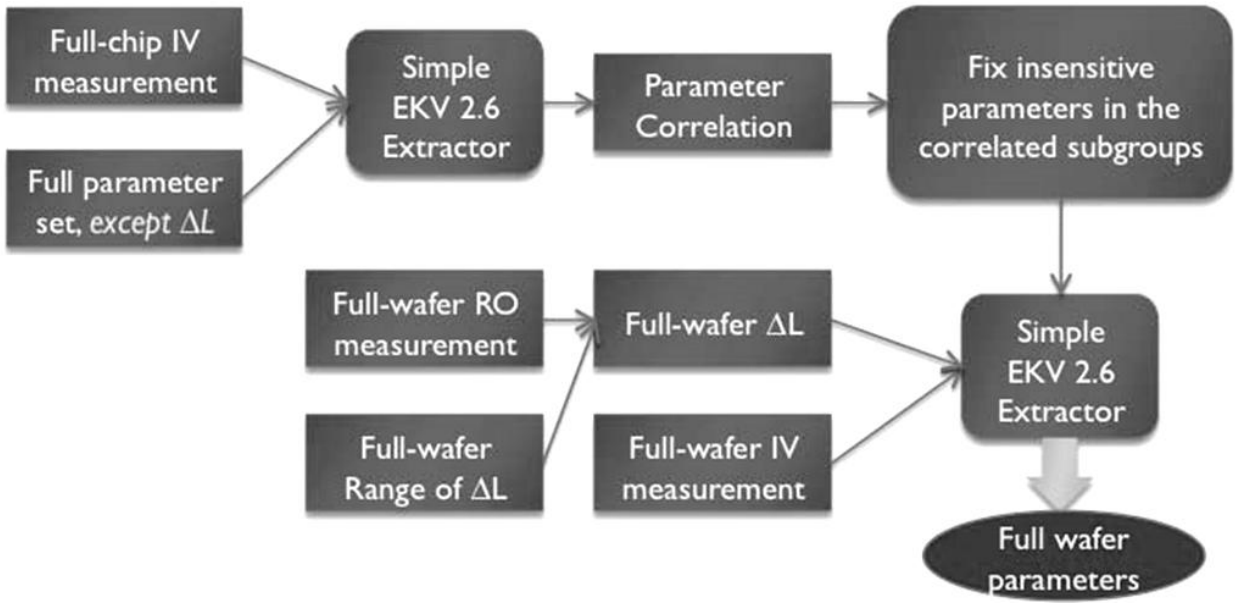

Figure 2-5 Variability Structure Aware Compact Model Parameter Extraction Procedure Example [2-12]

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Chapter 3

Linear Propagation in Compact Variability Modeling

Statistical compact models properly characterized for process variability are important for the design of high-yield integrated circuits. Although it is important to understand the underlying physical mechanisms that cause variations in device performances, the ultimate goal of compact statistical modeling is to accurately represent variations of simulated circuit characteristics. This chapter includes a brief review of a statistical compact modeling method, namely Backward Propagation of Variance (BPV), and then proposes a spatial variability pattern linear propagation method based on BPV for fast statistical compact model characterization. Basic calculation results are presented here while further improvements will be discussed in the next chapter.

3.1 Backward Propagation of Variance

The Backward Propagation of Variance (BPV) method is a unified approach for physically based statistical compact modeling. The method was first proposed to better characterize BJT compact modeling [3-1][3-2], while recent extensions and enhancements [3-3][3-4][3-5] make it suitable for characterizing global and local statistical process variations via industrial-standard compact models.

The BPV method formulates statistical models using a set of independent, normally distributed process parameters $\boldsymbol{p}$. These parameters control the variations seen in the device electrical performances $\boldsymbol{e}$ through the behavior described in the SPICE nominal compact models. With hierarchically structured variations captured in electrical data, calculated compact parameters using BPV can maintain the hierarchical variation structure and thus support more accurate simulation results for statistical circuit design. Here *backward propagation* refers to estimating the model (or process) parameters ($\boldsymbol{p}$) from electrical data ($\boldsymbol{e}$) through sensitivity characterization. This should be distinguished from *forward propagation* (from $\boldsymbol{p}$ to $\boldsymbol{e}$) through SPICE simulation.

MOSFET electrical performances (i.e. I_{dsat}) are collected from test wafer measurement data e_i $(i = 1,2, \dots, m)$; while process related compact model parameters (i.e. V_{th0}) are selected among the characterization set p_j $(j = 1,2, \dots, n)$while avoiding including parameters that are strongly correlated with each other. With the typically small manufacturing variations at a stable technology node, it is acceptable to use a local linear approximation around the nominal values of $\bar{\boldsymbol{p}} = (\bar{p}_1, \dots, \bar{p}_n)^T$:

$$e_i \cong e_i(\bar{\boldsymbol{p}}) + \sum_{j=1}^{n} s_{ij}(p_j - \bar{p}_j) \qquad \textbf{(3.1)}$$

$$\sigma_{e_i}^2 = \sum_{j=1}^{n} s_{ij}^2 \sigma_{p_j}^2 \quad \textbf{(3.2)}$$

The respective sensitivities are then defined as

$$s_{ij} = \left.\frac{\partial e_i(\boldsymbol{p})}{\partial p_j}\right|_{\boldsymbol{p}=\overline{\boldsymbol{p}}} \quad \textbf{(3.3)}$$

For *m* electrical performance measurements $\boldsymbol{e} = (e_1, \ldots, e_m)^T$ and *n* process related compact model parameters $\boldsymbol{p} = (p_1, \ldots, p_n)^T$, we have an $m \times n$ linear system

$$\Delta\boldsymbol{e} \cong \boldsymbol{S}\Delta\boldsymbol{p};\ \ \Delta\boldsymbol{e} = \boldsymbol{e} - \boldsymbol{e}(\overline{\boldsymbol{p}}),\ \Delta\boldsymbol{p} = \boldsymbol{p} - \overline{\boldsymbol{p}},\ \boldsymbol{S} = \left[s_{ij}\right]_{i=1,2,\ldots,m;\, j=1,2,\ldots,n} \quad \textbf{(3.4)}$$

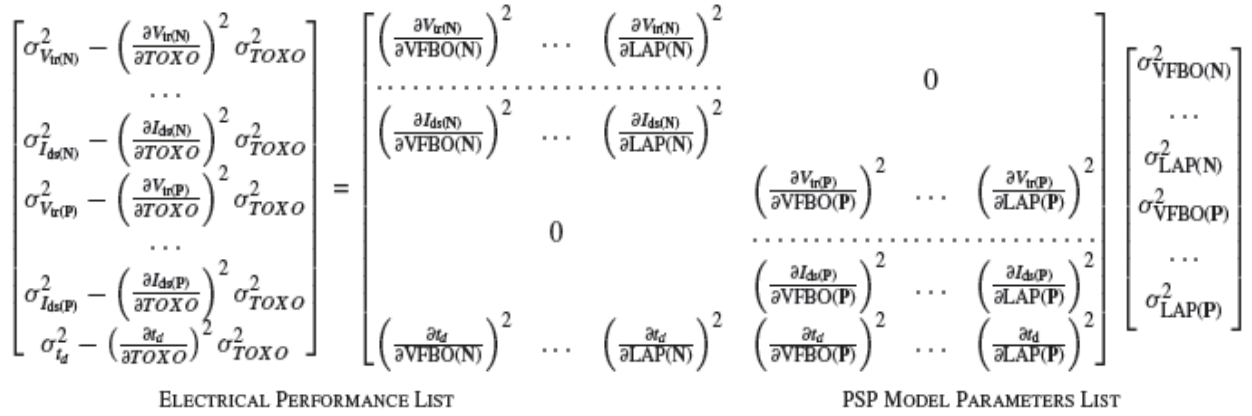
$$\boldsymbol{\sigma_e^2} = \boldsymbol{T}\boldsymbol{\sigma_p^2};\ \boldsymbol{\sigma_e^2} = \left(\sigma_{e_1}^2, \ldots, \sigma_{e_m}^2\right)^T, \boldsymbol{\sigma_p^2} = \left(\sigma_{p_1}^2, \ldots, \sigma_{p_n}^2\right)^T \quad \textbf{(3.5)}$$

And the sensitivity matrix is

$$\boldsymbol{T} = \left[\left.\left(\frac{\partial e_i(\boldsymbol{p})}{\partial p_j}\right)^2\right|_{\boldsymbol{p}=\overline{\boldsymbol{p}}}\right]_{i=1,2,\ldots,m;\, j=1,2,\ldots,n} \quad \textbf{(3.6)}$$

For a complete set of device performance electrical test measurements (large *m*) and carefully selected variation-aware compact model parameters (small *n*) so that *m*>*n* and Eq. **(3.4) (3.5)** are solved using multivariate least square fit or other linear regression methods.

Note that scaling is needed for some variables (either $\boldsymbol{e}$ or $\boldsymbol{p}$) to improve the condition number of the matrix; while this scaling is implied, it will not be explicitly shown in the following application example of BPV with PSP MOFET model [3-4].



ELECTRICAL PERFORMANCE LIST

PSP MODEL PARAMETERS LIST

Device (W/L, μm)	e_i	Description
Large (10/10)	V_{tr}	Threshold voltage for large devices
Short (10/0.2)	V_{ts}	Threshold voltage for short devices
	I_{ds}	Saturation current for short devices
Narrow (0.24/10)	V_{tn}	Threshold voltage for narrow devices
Small (0.24/0.2)	V_{tm}	Threshold voltage for small devices
	I_{dm}	Saturation current for small devices
RO	t_d	Gate delay for ring oscillators

Model Parameter	Description
TOXO	Oxide thickness
VFBO	Geometry-independent flat band voltage
VFBL	Length-dependent flat band voltage
UO	Zero-field mobility
LAP	Channel length variation
WOT	Channel width variation

Figure 3-1 BPV Characterization Method Implemented with PSP Compact Model [3-4]
Here T_{ox} is obtained from process monitoring data and therefore TOX0 is calculated directly in advance;

This application example also demonstrates the selection criteria of ***e*** in the BPV method. Electrical measurements of devices that strongly affect target circuit performances are selected as key quantities in ***e***. Knowledge of circuit applications and device operations should guide this selection. From the above example, the saturated drain current (I_{dsat}) of a short channel device (*wide/short*) is highly correlated with the switching speed of ring oscillators (t_d), and thus is chosen as one of the $\boldsymbol{e_i}$'s. Conversely, bias conditions or device geometries that are far removed from typical circuit applications are less likely to be chosen. Moreover, selection of ***e*** is also required to make ***p*** observable, and this requires that the sensitivity matrix ***S*** which is at the core of the BPV linear system is well-conditioned.

A comprehensive formulation of the BPV procedure [3-5] that handles quadratic nonlinearities in the ***e-p*** mappings is reviewed below. A second-order Taylor expansion of ***e*** around nominal ***p*** gives

$$e_i \cong e_i(\bar{\boldsymbol{p}}) + \sum_{j=1}^{n} s_{i,j}\delta p_j + \sum_{j,k=1}^{n} s_{i,jk}\delta p_j \delta p_k\,; \quad \delta p_j = p_j - \bar{p}_j \tag{3.7}$$

The second-order sensitivities are

$$s_{i,jk} = \frac{1}{2}\frac{\partial^2 e_i(\boldsymbol{p})}{\partial p_j \partial p_k}\bigg|_{\boldsymbol{p}=\bar{\boldsymbol{p}}} \tag{3.8}$$

and the first two statistical moments of ***e*** are

$$\mu_{e_i} = e_i(\bar{\boldsymbol{p}}) + \sum_{j=1}^{n} s_{i,jj}\sigma_{p_j}^2 \tag{3.9}$$

$$\sigma_{e_i}^2 = \sum_{j=1}^{n} s_{i,j}^2\sigma_{p_j}^2 + 2\sum_{j,k=1}^{n} s_{i,jk}^2\sigma_{p_j}^2\sigma_{p_k}^2 \tag{3.10}$$

From previous work on BPV, the linear version is often sufficient and the quadratic version is only necessary occasionally. We will show in later sections that linear BPV is suitable for our test-bench implementation.

3.2 Spatial Variability Linear Propagation Method

The Backward Propagation of Variance (BPV) method is highly extendable to incorporate hierarchical variation models [3-6], which accurately describe the variability structure in the electrical measurement data. The superimposition property of linear systems makes linear BPV applicable to spatial variability characterization in compact models, as discussed in this section.

3.2.1 Hierarchical Variability Modeling

Process variations usually have very different properties, and among them, spatial variations are of critical importance in linking design and manufacturing activities. Statistical spatial variations include both deterministic and random components. Certain types of deterministic variations are hierarchical in nature, while random variations can be modeled as white noise and added to the baseline, as depicted in the following figures.

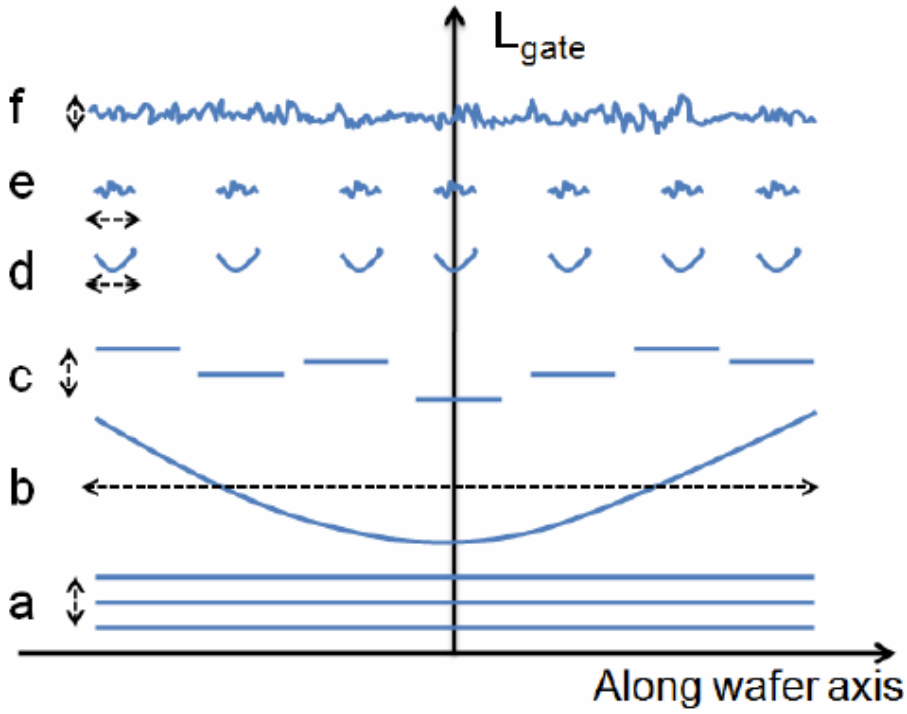


Figure 3-2 Illustration of variability hierarchy [3-6]:
a) wafer-to-wafer [random shift] b) across wafer [systematic pattern]
c) die-to-die [random shift] d) across die [systematic pattern]
e) (within die) layout dependent [systematic] f) (within die) device-to-device [random white noise]

For simplicity, and without loss of generality, the total variation can be expressed as

$$P = P_0 + \Delta P_{w2w} + \Delta P_{a-w} + \Delta P_{d2d} + \Delta P_{a-d} + \Delta P_{layout} + \varepsilon_{device} \quad \textbf{(3.11)}$$

In the expression **(3.11)**, $\boldsymbol{P}$ represents the actual parameter value while $\boldsymbol{P_0}$ is the nominal value. Wafer-to-wafer shift $\boldsymbol{\Delta P_{w2w}}$ and die-to-die shift $\boldsymbol{\Delta P_{d2d}}$ are typically random numbers. Across wafer $\boldsymbol{\Delta P_{a\text{-}w}}$ and across die $\boldsymbol{\Delta P_{a\text{-}d}}$ systematic spatial patterns are usually parabolic due to the circular wafer shape and approximate radial symmetry in most processing chambers, as shown below.

$$\Delta P_{a-w} = a + bx + cy + dxy + ex^2 + fy^2 \qquad \textbf{(3.12)}$$

As for variations from devices within a single die, both layout dependent deterministic components $\boldsymbol{\Delta P_{layout}}$ and pure random components $\boldsymbol{\varepsilon_{device}}$ exist. As the technology advances into the nanometer regime, local random variation sources for devices, such as line-edge roughness (LER) and random dopant fluctuation (RDF), play increasingly significant roles in final yield.

3.2.2 Spatial Back Propagation of Variance

Assuming a hierarchical variability structure, we apply a novel extension to the linear BPV statistical compact model characterization method. The proposed method will obtain hierarchical spatial pattern of assigned compact model parameters directly from test wafer electrical measurement data. This propagation method applies linear regression on the coefficients of the hierarchical spatial variability model, i.e. $\boldsymbol{a}$ **-** $\boldsymbol{f}$ in $\boldsymbol{\Delta P_{a\text{-}w}}$**.** An illustration of this method is shown below. The compact model sensitivity analysis is done at the nominal value; and the spatial coefficients hierarchical variability model (rather than statistical moments, such as variance or mean value) in measured I-V data are linearly propagated to selected compact model parameters.

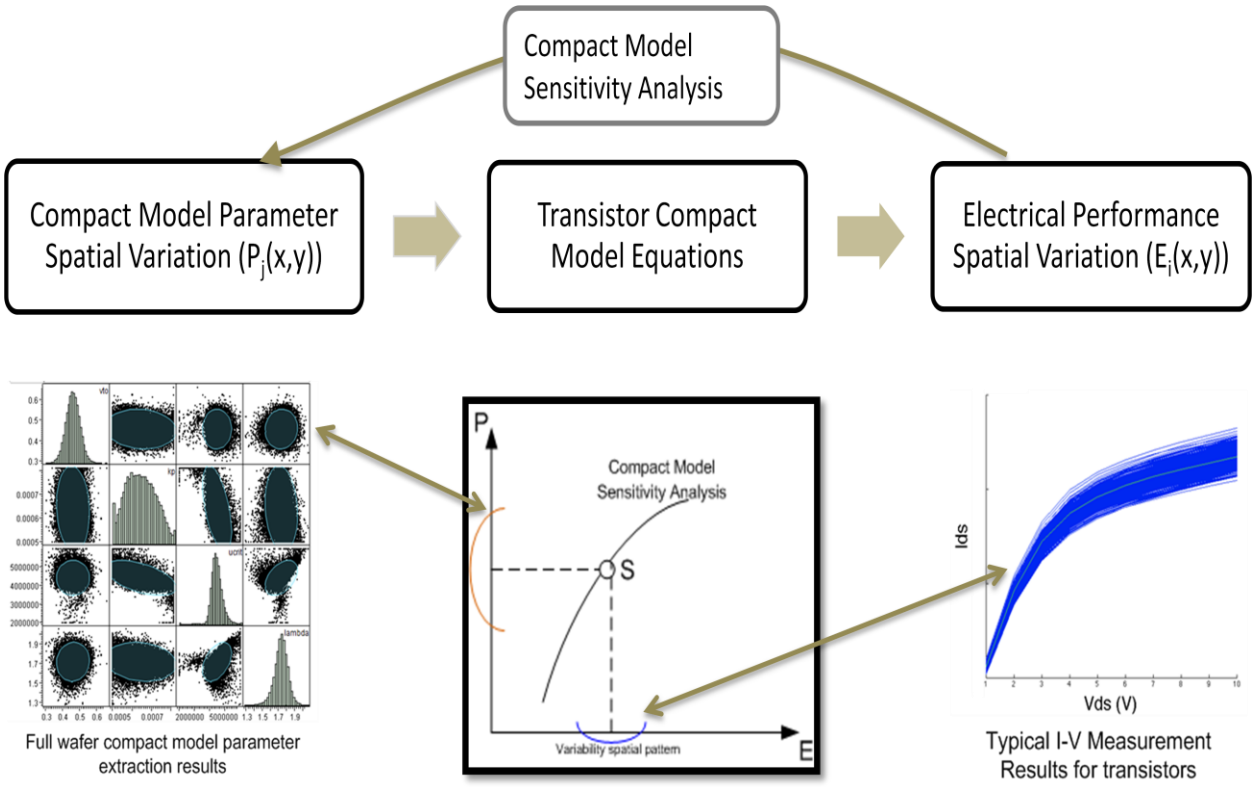


Figure 3-3 Illustration of Spatial Variability Pattern Linear Propagation Method

For better application of our method, the hierarchical variability model is modified as (for single wafer data from transistor I-V test arrays)

$$P_w = P_{w0} + \Delta P_{a-w} + \varepsilon_{residual};\ \Delta P_{a-w} = \lambda_0 + \lambda_1 x + \lambda_2 y + \lambda_3 xy + \lambda_4 x^2 + \lambda_5 y^2 \qquad \textbf{(3.13)}$$

The BPV method is extended for across-wafer component spatial pattern linear propagation. From now on we will use the term Spatial Back Propagation of Variance, or SBPV.

$$\delta e_i(x,y) = \sum_{j=1}^{n} s_{ij}\delta p_j(x,y) = \sum_{j=1}^{n} s_{ij}\left(\lambda_{0,j} + \lambda_{1,j}x + \lambda_{2,j}y + \lambda_{3,j}xy + \lambda_{4.j}x^2 + \lambda_{5,j}y^2\right)$$

$$= \sum_{j=1}^{n} s_{ij}\lambda_{0,j} + \left(s_{ij}x\right)\lambda_{1,j} + \left(s_{ij}y\right)\lambda_{2,j} + \left(s_{ij}xy\right)\lambda_{3,j} + \left(s_{ij}x^2\right)\lambda_{4.j} + \left(s_{ij}y^2\right)\lambda_{5,j}$$

$$= \sum_{j=1}^{n} (s_{ij})_{spatial} \cdot \boldsymbol{\lambda_j}^T \qquad \textbf{(3.14)}$$

The sensitivity analysis is done around the nominal value, i.e. wafer-mean

$$s_{ij} = s_{ij}(x,y) = \left.\frac{\partial e_i(\boldsymbol{p})}{\partial p_j}\right|_{\boldsymbol{p}=\boldsymbol{p_{w0}}} \tag{3.15}$$

The SBPV linear regression equation is

$$\delta \boldsymbol{e} = \boldsymbol{S}\delta\boldsymbol{p} = \boldsymbol{S_{spatial}}\boldsymbol{\lambda}$$

$$\delta \boldsymbol{e} = \left(\delta \boldsymbol{e_1}(\boldsymbol{x},\boldsymbol{y}), \dots, \delta \boldsymbol{e_m}(\boldsymbol{x},\boldsymbol{y})\right)^{\boldsymbol{T}}, \delta\boldsymbol{p} = \left(\delta \boldsymbol{p_1}(\boldsymbol{x},\boldsymbol{y}), \dots, \delta \boldsymbol{p_n}(\boldsymbol{x},\boldsymbol{y})\right)^{\boldsymbol{T}} \tag{3.16}$$

The spatial coefficients and modified sensitivity matrix are

$$\boldsymbol{\lambda} = (\boldsymbol{\lambda_1}, \dots, \boldsymbol{\lambda_n})^{\boldsymbol{T}} = ([\lambda_{0,1}, \lambda_{1,1}, \lambda_{2,1}, \lambda_{3,1}, \lambda_{4.1}, \lambda_{5,1}], \dots, \boldsymbol{\lambda_n})^{\boldsymbol{T}} \tag{3.17}$$

$$\boldsymbol{S_{spatial}} = \left[\left(s_{ij}\right)_{spatial}\right]_{\substack{i=1,2,\dots,m;\\ j=1,2,\dots,n}} = \left[\left.\frac{\partial e_i(\boldsymbol{p})}{\partial p_j}\right|_{\boldsymbol{p}=\boldsymbol{p_{w0}}} * \begin{matrix}(x,y)\\ spatial\ component\end{matrix}\right]_{\substack{i=1,2,\dots,m;\\ j=1,2,\dots,n}} \tag{3.18}$$

3.3 Test Bench Implementation

To demonstrate the effectiveness, we tested the SBPV method on actual test wafer data (transistor array I-V measurements) and standard compact models (EPFL-EKV model). Test bench setup details, including measurement data structure and compact model selection, will be discussed in this section while simulation results, verifications and discussions are shown in the next section.

3.3.1 Electrical Measurement Data Structure

A set of transistor I-V measurement data from a 65nm SOI technology test wafer is used in our test bench for illustration of our spatial variability linear propagation method. DC current/voltage measurement on transistors with 7 different W/L geometrical combinations is completed with one full test wafer containing 68 dies. There are 432 measured repetitions (48 rows, 9 columns) within one die for one particular transistor geometry. Each NMOS transistor device under test (DUT) has 100 measurement points on the I_d~V_{ds}/V_{gs} curve in the range from 0V to 1V.

Table 3-1 Transistor DUT Geometries

DUT	1	2	3	4	5	6	7
L[nm]	60	60	60	60	70	100	150
W[nm]	500	375	250	120	500	500	500

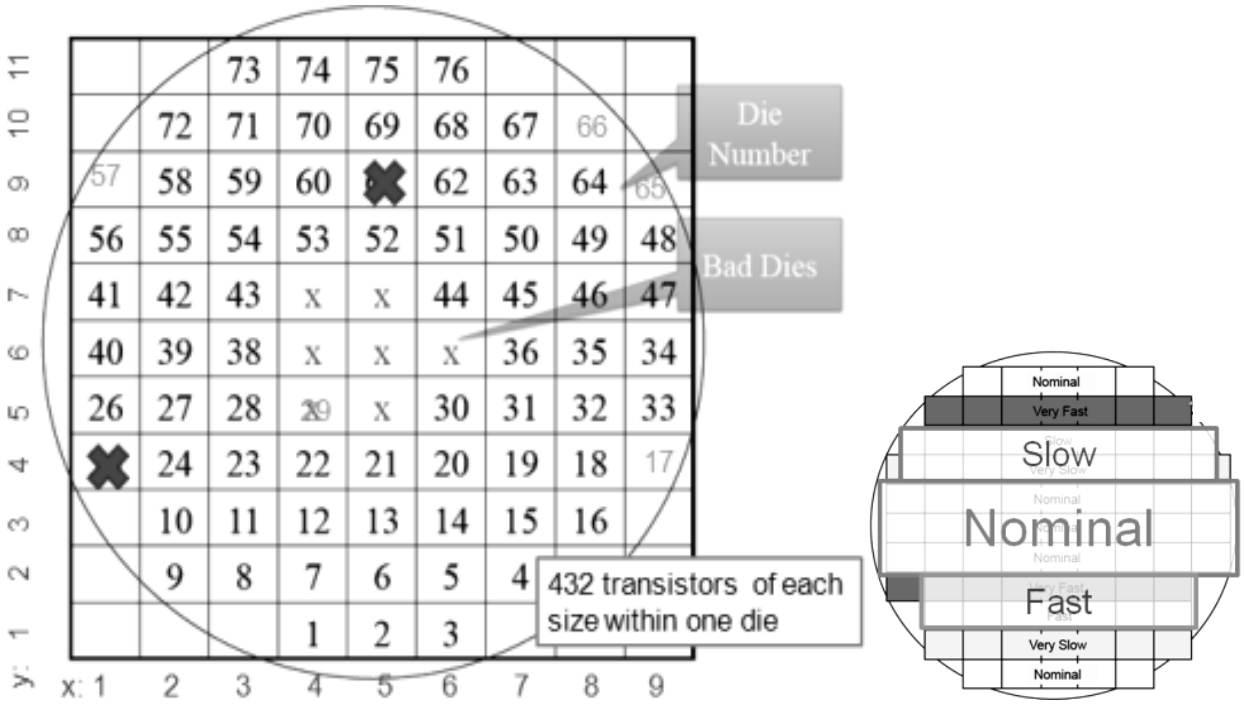


Figure 3-4 Wafer Map and Summary of Data Structure

A wafer map summary of this data set structure is shown above. As seen, the wafer is intentionally separated into fast/slow stripes in addition to nominal region. The transistor geometrical combinations are also listed above. As will be discussed later, we apply our test only on the DUTs with the smallest channel length and width, which capture more sources of variations while providing acceptable accuracy in model parameter extraction and sensitivity analysis. This device selection will help us distinguish and evaluate different components in our spatial variability linear propagation method. Moreover, a global model card that could describe transistors of any size is not achievable and individual nominal model card should be generated for each transistor size. This can be explained that modern manufacturing processes are optimized for devices of different target dimensions, e.g. optical proximity correction (OPC), and that a significant departure from the optimal channel length will induce additional localized process variability. Therefore, initial nominal compact model parameters are independently extracted for transistors of different sizes.

3.3.2 Compact Model Selection

Transistor compact models consist of complex equations covering a wide range of operating regions, from saturation to cut-off where the drain current changes by many orders of magnitude. The geometric diversity of the transistors also demands additional fitting parameters to the compact models for good overall performance curve fitting. Therefore, hundreds of model parameters are needed to be extracted before real application in SPICE circuit simulation. Many of these parameters carry vague or no physical meaning, and thus cannot be easily used in order to capture the actual variability of the manufacturing process.

As discussed above, the transistor array I-V measurements mainly describe the DC characteristics of the device compact model. Due to the lack of accurate off-current measurements, a full-scale industrial standard transistor compact model, such as BSIM or PSP model, is not necessary for our data set. Furthermore, limited transistor sizes will not support the extraction of the large numbers of parameters typical in "complex" models, which is critical for sensitivity analysis and ***S*** matrix creation. This makes these "complex" models unsuitable for testing SBPV on this particular dataset.

The EPFL-EKV model [3-7] is a scalable SPICE simulation compact model built on fundamental physical properties of MOSFET. The EKV model is also introduced within a complete, statistically efficient and simple characterization methodology [3-8].

Table 3-2 Main EKV Intrinsic Model Parameters [3-7]

Name	Description	Units
COX	Gate oxide capacitance	F/m
VTO	Nominal threshold voltage	V
GAMMA	Body effect factor	$V^{1/2}$
PHI	Bulk Fermi potential (2x)	V
KP	Transconductance parameter	A/V^2
THETA	Mobility reduction coefficient	1/V
UCRIT	Longitudinal critical field	V/m
XJ	Junction depth	m
DL	Channel length correction	m
DW	Channel width correction	m
LAMBDA	Depletion length coefficient	-
LETA	Short channel effect coefficient	-
WETA	Narrow channel effect coefficient	-

Table 3-3 Summary of Basic EKV Model Equations [3-7]

Description	Equation
Pinch-off voltage	$V_P = V_G' - \mathrm{PHI} - \gamma' \cdot \left(\sqrt{V_G' + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2} \right)$ $V_G' = V_G - \mathrm{VTO} + \mathrm{PHI} + \mathrm{GAMMA} \cdot \sqrt{\mathrm{PHI}}$
Slope factor	$n = 1 + \frac{\mathrm{GAMMA}}{\sqrt{V_P + \mathrm{PHI}}}$
Transconductance, mobility reduction	$\beta = \mathrm{KP} \cdot \frac{W_{eff}}{L_{eq}} \cdot \frac{1}{1 + \mathrm{THETA} \cdot V_P}$
Effective length & width	$L_{eff} = L + \mathrm{DL}$, $W_{eff} = W + \mathrm{DW}$
Channel length modulation & velocity saturation	$L_{eq} = L_{eff} - \Delta L + \frac{V_{DS}'}{\mathrm{UCRIT}}$ $\Delta L = \mathrm{LAMBDA} \cdot L_C \cdot \ln\left(1 + \frac{V_R}{L_C \cdot \mathrm{UCRIT}}\right)$ $L_C = \sqrt{\frac{\varepsilon_0 \varepsilon_{si}}{\mathrm{COX}}} \cdot \mathrm{XJ}$ $V_D - V_S \le V_{DS}' \le V_{DSS}$ $0 \le V_R < V_D - V_S - V_{DSS}'$ *V_{DS}' and V_R are continuous functions, V_{DSS} and V_{DSS}' depend on bias, L_{eff},* UCRIT *and* LAMBDA
Short & narrow channel effects	$\gamma' = \mathrm{GAMMA} - \frac{\varepsilon_0 \varepsilon_{si}}{\mathrm{COX}} \cdot \left[\frac{\mathrm{LETA}}{L + \mathrm{DL}} \cdot \sqrt{V_D + \mathrm{PHI}} + \left(\frac{\mathrm{LETA}}{L + \mathrm{DL}} - \frac{3 \cdot \mathrm{WETA}}{W + \mathrm{DW}} \right) \cdot \sqrt{V_S + \mathrm{PHI}} \right]$
Drain current and Specific current	$I_D = I_F - I_R$ $I_{F(R)} = \begin{cases} I_S \cdot \exp\left[(V_P - V_{S(D)}) / U_t \right] & \text{(WI)} \\ I_S \cdot \left[(V_P - V_{S(D)}) / 2U_t \right]^2 & \text{(SI)} \end{cases}$ $I_S = 2 \cdot n \cdot \beta \cdot U_t^2 \quad U_t \equiv k \cdot T / q$

In our test bench implementation, a nonlinear-least-square-optimizer based EKV model parameter extractor, provided by IBM Austin Research, is used to obtain the nominal compact model. We also perform direct model parameter extraction using this extractor on each transistor

as a reference set for result verification. This extractor is capable of extracting all the main intrinsic model parameters listed in Table 3-2 Main EKV Intrinsic Model Parametersand provides fitting error (SSE) of each extraction executed. It can also be tuned to extract partial set of model parameters with other parameter values set to nominal, which is important since we will perform various verification runs for our linear propagation method calculation.

3.4 Results and Discussions

In this section, we will present the calculation results using our proposed spatial variability linear propagation method. We will first apply the basic linear BPV on our data set as a reference and validation of our implemented algorithm as well as sensitivity matrix calculation. Then the spatial variability model is fitted on electrical measurement and linearly propagated backwards to selected EKV model parameters. We establish a "golden" verification set from time-consuming simulations, i.e. performing model parameter extractions on every individual transistor all over the wafer. Discussion on the effectiveness of our method is based on comparisons to this verification set.

3.4.1 Sensitivity Matrix Simulation and Verification

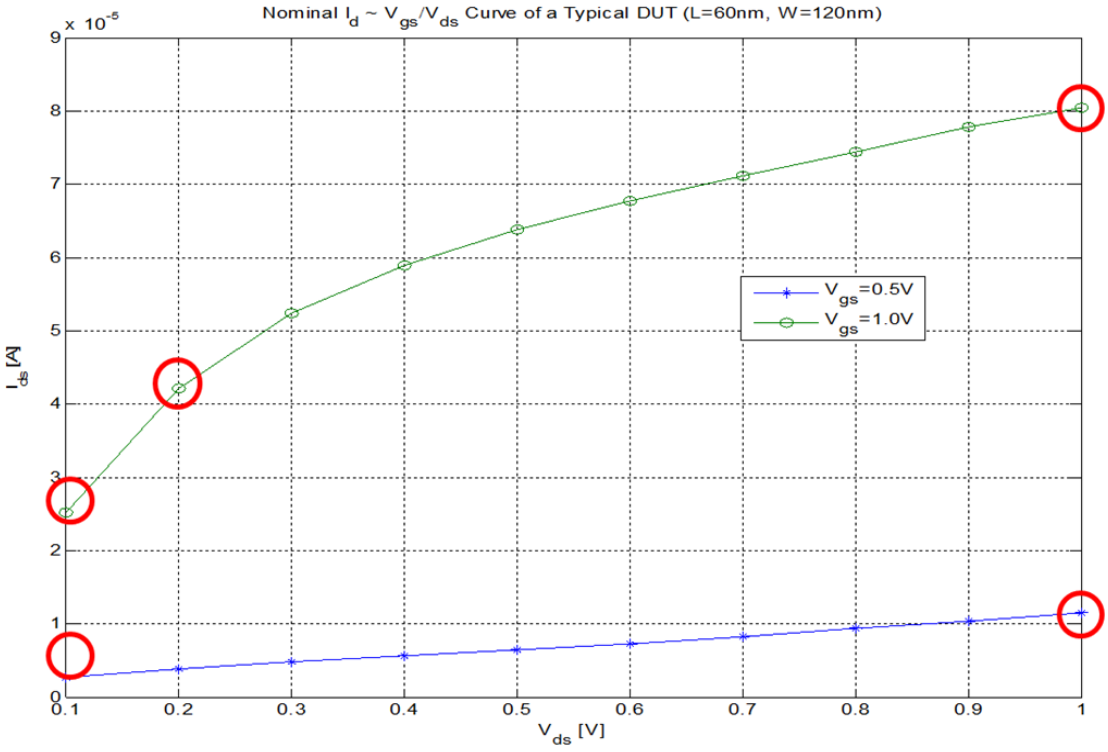
The sensitivity matrix in **(3.3)** and **(3.18)** is critical to linear BPV method and our proposed spatial variability pattern linear propagation method. In this section, we will simulate the sensitivity matrix at nominal EKV model parameter values (obtained from the wafer manufacturer's initial model) with HSPICE using finite normalized difference method (±5%

perturbation around nominal values). This sensitivity matrix is then applied in the characterization procedure using basic linear BPV for verification and validation.

As from previous work [3-10], we select 5 points on the measured I_d~V_{ds}/V_{gs} curve for our electrical performance ***e*** set, as shown below. From [3-9], four EKV first-order intrinsic model parameters are chosen as our model parameter ***p*** set, including *VTO* (long channel threshold voltage), *KP* (transconductance parameter), *UCRIT* (longitudinal critical field for mobility) and *LAMBDA* (junction depletion length coefficient). An improvement on the choice of both ***e*** and ***p*** set will be discussed in the next chapter. Here, we just establish the 5×4 linear system based on the chosen ***p*** and ***e*** sets.

Table 3-4 Electrical Performance Metrics Set *e*

I-V Points	I_1	I_2	I_3	I_4	I_5
V_{gs} [V]	0.5	0.5	1.0	1.0	1.0
V_{ds} [V]	0.1	1.0	0.2	1.0	0.1



The calculated sensitivity matrix for our linear system for the DUT (L=60nm, W=120nm) is

$$S = \left[\left.\frac{\partial e_i(\boldsymbol{p})}{\partial p_j}\right|_{\boldsymbol{p}=\boldsymbol{p_{w0}}}\right]_{\substack{i=1,2,\ldots,5;\\ j=1,2,\ldots,4}} = \begin{bmatrix} -6.0669 & 1.003 & 0.0988 & 0.1729 \\ -3.8630 & 0.9998 & -0.3363 & 4.8130 \\ -0.9795 & 1.0002 & 0.2507 & 0.1847 \\ -0.9366 & 1.0001 & 0.5507 & 0.7071 \\ -0.8924 & 1.0002 & 0.1974 & 0.0527 \end{bmatrix} \quad \textbf{(3.19)}$$

We also have built the linear system for basic linear SBPV. Here, all the figures of merit are pre-processed with centering and normalization in order to condition the above sensitivity matrix.

$$\begin{bmatrix} \delta I_{1,a-w}/I_{1,0} \\ \delta I_{2,a-w}/I_{2,0} \\ \delta I_{3,a-w}/I_{3,0} \\ \delta I_{4,a-w}/I_{4,0} \\ \delta I_{5,a-w}/I_{5,0} \end{bmatrix} = \begin{bmatrix} \frac{vto_0}{I_{1,0}}\left.\frac{\partial I_1}{\partial vto}\right|_0 & \cdots & \frac{lambda_0}{I_{1,0}}\left.\frac{\partial I_1}{\partial lambda}\right|_0 \\ \vdots & \ddots & \vdots \\ \frac{vto_0}{I_{5,0}}\left.\frac{\partial I_5}{\partial vto}\right|_0 & \cdots & \frac{lambda_0}{I_{5,0}}\left.\frac{\partial I_5}{\partial lambda}\right|_0 \end{bmatrix} \cdot \begin{bmatrix} \delta vto_{a-w}/vto_0 \\ \delta kp_{a-w}/kp_0 \\ \delta ucrit_{a-w}/ucrit_0 \\ \delta lambda_{a-w}/lambda_0 \end{bmatrix} \quad \textbf{(3.20)}$$

Here, $\boldsymbol{I_{i,a\text{-}w}}$ stands for a particular die mean value of the electrical performance metric ***i***, which averages over 432 identical transistor DUT replications within one die and only leave the across-wafer deterministic variability component unattended. The above linear system is solved using the least square fit algorithm embedded in MATLAB and repeated for all 68 dies. The derived compact model parameter sets are shown in the figure below, with the across-wafer variations clearly shown on the wafer map. The absolute values of the compact models have physical meaning and can be directly input to HSPICE simulator for statistical circuit simulations.

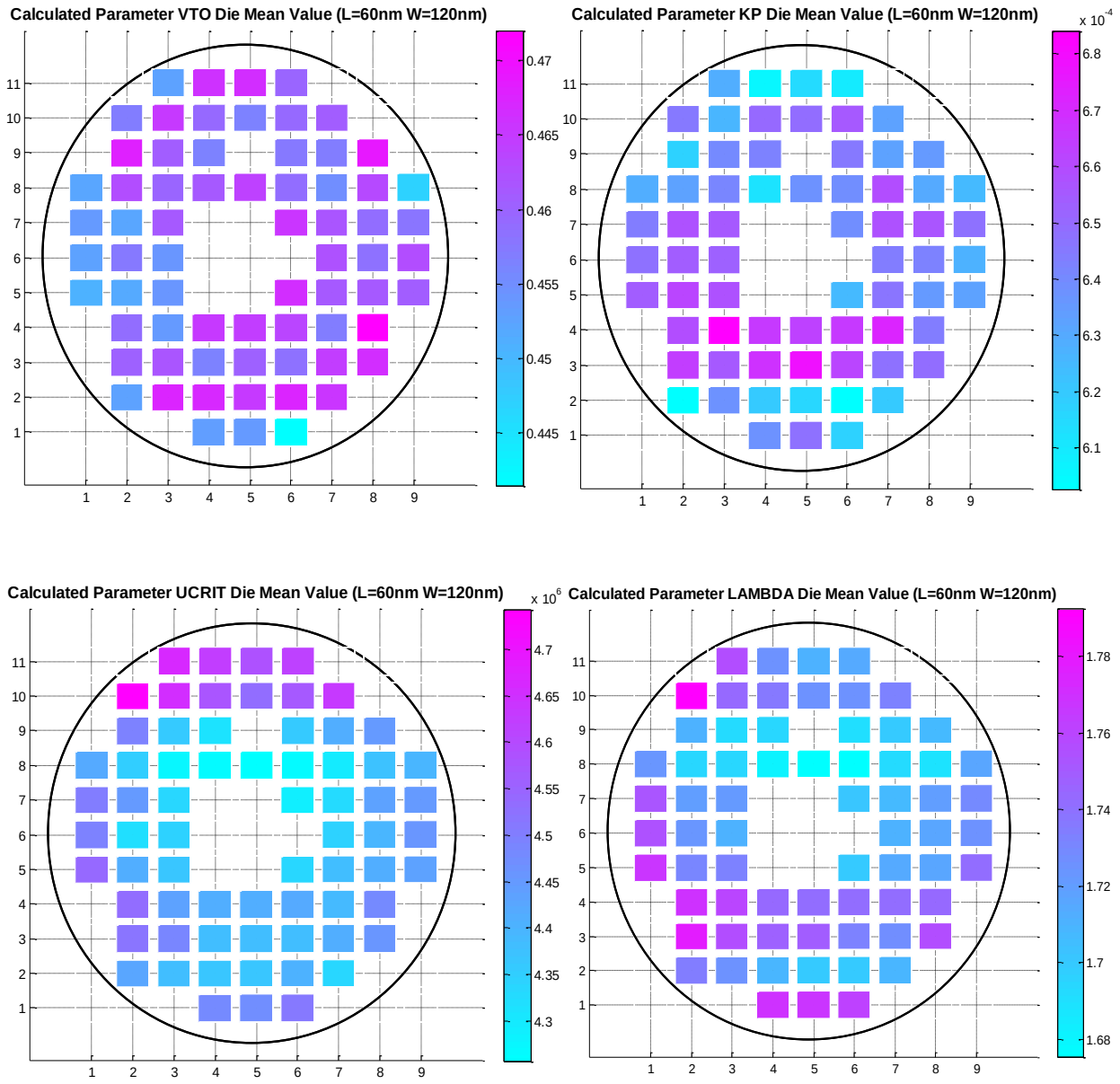


Figure 3-5 Wafer Maps of Linear SBPV Calculated EKV Model Parameters VTO, KP, UCRIT and LAMBDA across-wafer variability is clearly shown on the DUT (L=60nm, W=120nm) of the data set

We have generated a reference EKV model parameter across-wafer data set by performing compact model parameter extractions, i.e. by fixing all the other parameters at nominal values while leaving the 4 selected parameters for optimization by the extractor, on every individual

transistor across the entire wafer (for a particular geometry, total of 68×432=29376 DUTs are simulated). Statistical analysis, as shown below, is done on the voluminous extraction results in order to generate die mean values of the selected EKV model parameters.

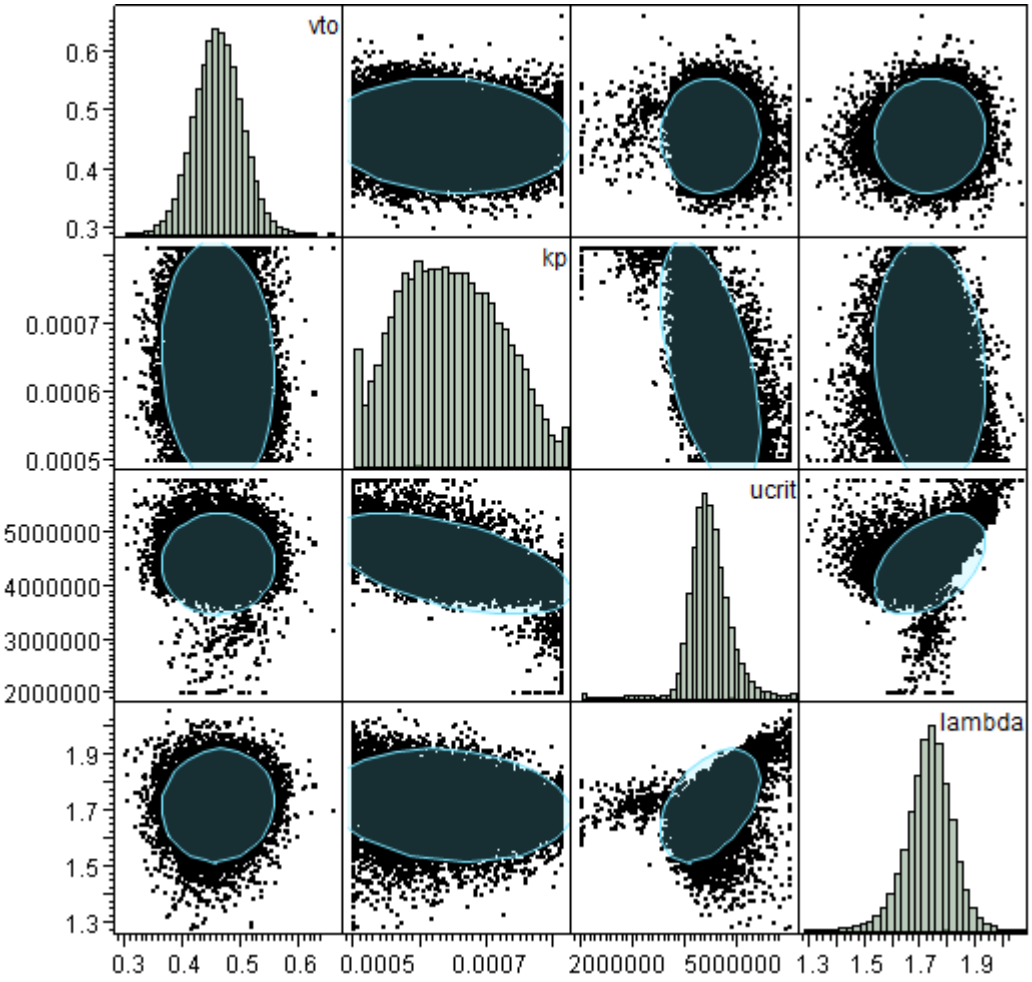


Figure 3-6 Basic Statistics of "Golden" Extraction Set
(generated by commercial software JMP)

Correlation analysis is then done on the linear SBPV calculated model parameter die mean values versus reference extraction set values. Correlation coefficients close to 1 are achieved for all 4 compact model parameters. Therefore, the sensitivity matrix ***S*** calculation is verified and

can be implemented in our proposed spatial variability linear propagation system, as discussed in the next section.

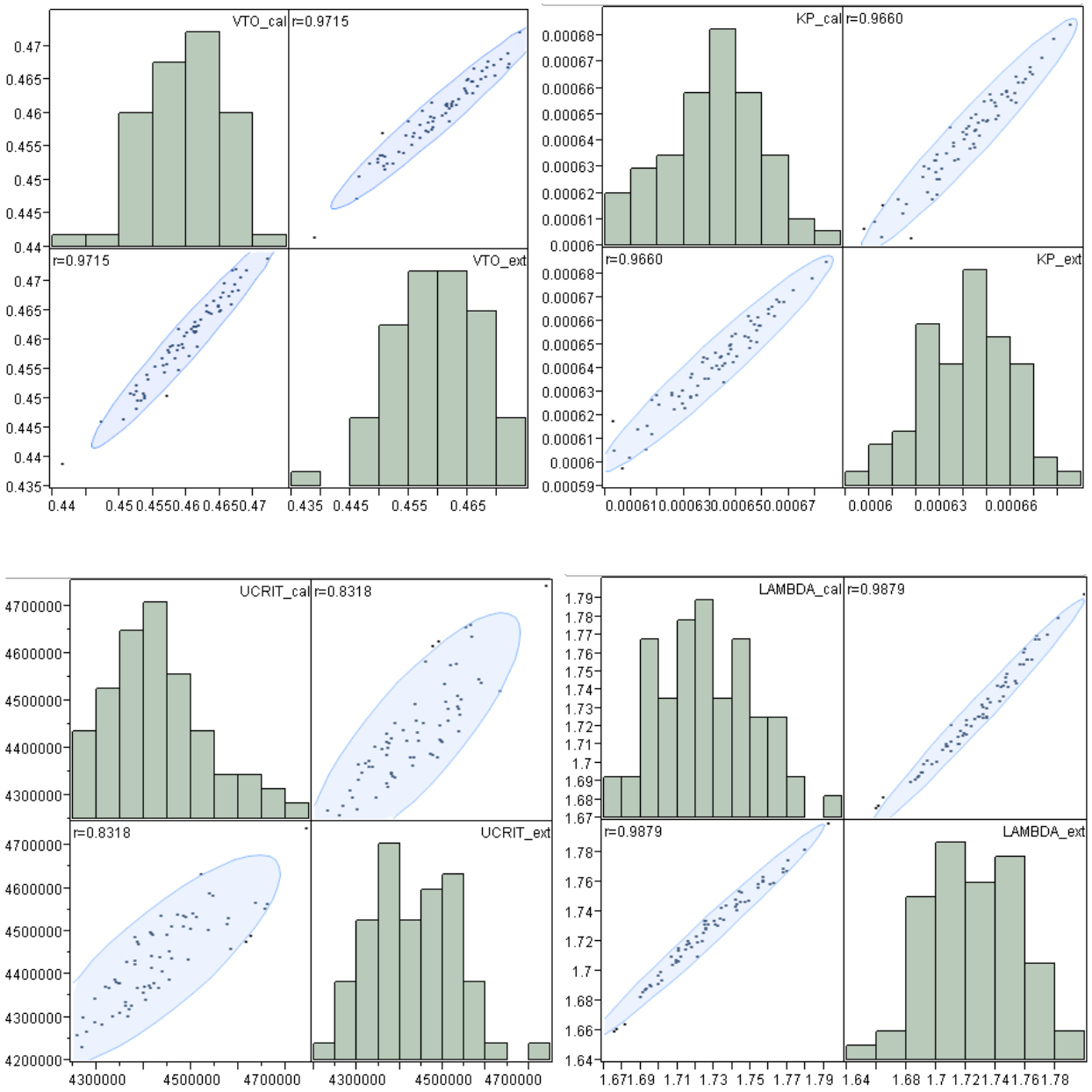


Figure 3-7 Comparison between SBPV Calculated Results and Extracted Reference Results Correlation coefficients close to 1 are achieved for all model parameters (GOOD MATCH): ρ_{VTO}=0.9715, ρ_{KP}=0.9660, ρ_{UCRIT}=0.8318, ρ_{LAMBDA}=0.9879

3.4.2 SBPV Results and Discussion

As described in the previous section, our proposed method will be tested on previously defined 5×4 linear system with electrical performance data (I_1,,..., I_5) and EKV model parameters (*VTO*, *KP*, *UCRIT* and *LAMBDA*).

Similar to **(3.12)** and **(3.13)**, we can rewrite the compact model parameter across wafer variability pattern as

$$\delta vto_{a-w}(x_{die\#}, y_{die\#}) = \lambda_{0,vto} + \lambda_{1,vto}x + \lambda_{2,vto}y + \lambda_{3,vto}xy + \lambda_{4,vto}x^2 + \lambda_{5,vto}y^2 \qquad \textbf{(3.21)}$$

Here, spatial coordinate variables, *x* and *y*, are the corresponding die positions (vertical and horizontal, as shown in Figure 3-4 Wafer Map and Summary of Data Structure on the wafer. The parabolic pattern shows good but not perfect fit for the spatial variability model; we will discuss more about this later in this section.

Finally, we get the normal equation for spatial variability pattern coefficient linear regression procedure.

$$\begin{bmatrix} \frac{\delta I_{1,a-w}(x_{die\#1}, y_{die\#1})}{I_{1,0}} \\ \vdots \\ \frac{\delta I_{1,a-w}(x_{die\#76}, y_{die\#76})}{I_{1,0}} \\ \vdots \\ \vdots \\ \frac{\delta I_{5,a-w}(x_{die\#1}, y_{die\#1})}{I_{5,0}} \\ \vdots \\ \frac{\delta I_{5,a-w}(x_{die\#1}, y_{die\#1})}{I_{5,0}} \end{bmatrix} = \boldsymbol{S_{spatial}} \cdot \begin{bmatrix} \lambda_{0,vto} \\ \vdots \\ \lambda_{5,vto} \\ \vdots \\ \vdots \\ \lambda_{0,lambda} \\ \vdots \\ \lambda_{5,lambda} \end{bmatrix} \qquad (\textbf{3.22})$$

Here, as shown in **(3.18)**, we implement the $\boldsymbol{S_{spatial}}$ with our previously calculated/verified sensitivity matrix and then get the spatial sensitivity matrix.

$$S = \begin{bmatrix} s_{I_1,vto} & s_{I_1,kp} & s_{I_1,ucrit} & s_{I_1,lambda} \\ s_{I_2,vto} & s_{I_2,kp} & s_{I_2,ucrit} & s_{I_2,lambda} \\ s_{I_3,vto} & s_{I_3,kp} & s_{I_3,ucrit} & s_{I_3,lambda} \\ s_{I_4,vto} & s_{I_4,kp} & s_{I_4,ucrit} & s_{I_4,lambda} \\ s_{I_5,vto} & s_{I_5,kp} & s_{I_5,ucrit} & s_{I_5,lambda} \end{bmatrix} = \begin{bmatrix} -6.0669 & 1.003 & 0.0988 & 0.1729 \\ -3.8630 & 0.9998 & -0.3363 & 4.8130 \\ -0.9795 & 1.0002 & 0.2507 & 0.1847 \\ -0.9366 & 1.0001 & 0.5507 & 0.7071 \\ -0.8924 & 1.0002 & 0.1974 & 0.0527 \end{bmatrix}$$

$$\boldsymbol{S_{spatial}} = \left[\frac{\partial e_i(\boldsymbol{p})}{\partial p_j}\bigg|_{\boldsymbol{p}=\boldsymbol{p_{w0}}} * \begin{matrix} (x,y) \\ spatial\ component \end{matrix} \right]_{\substack{i=1,2,\ldots,5; \\ j=1,2,\ldots,4}} \qquad \textbf{(3.23)}$$

$$= \begin{bmatrix} s_{I_1,vto} & s_{I_1,vto} \cdot x_{die\#1} & \cdots & s_{I_1,vto} \cdot y_{die\#1}^2 & \cdots\cdots & s_{I_1,lambda} & s_{I_1,lambda} \cdot x_{die\#1} & \cdots & s_{I_1,lambda} \cdot y_{die\#1}^2 \\ & \vdots & & & \ddots & & & \vdots & \\ & \vdots & & & \ddots & & & \vdots & \\ & \vdots & & & \ddots & & & \vdots & \\ s_{I_5,vto} & s_{I_5,vto} \cdot x_{die\#76} & \cdots & s_{I_5,vto} \cdot y_{die\#76}^2 & \cdots\cdots & s_{I_5,lambda} & s_{I_5,lambda} \cdot x_{die\#76} & \cdots & s_{I_5,lambda} \cdot y_{die\#76}^2 \end{bmatrix}$$

The proposed SBPV method is applied on the DUTs of smallest DUTs (L=60nm W=500nm) all over the test wafer. The selected 4 EKV compact model parameter spatial variability models are then built with calculated coefficients from the linear regression system. For comparison with the reference set, we calculate the absolute mean values of the compact parameters of all the dies on the wafer from this spatial variability model. Correlation analysis similar to the one employed for linear BPV implementation verification is used and the results are shown below.

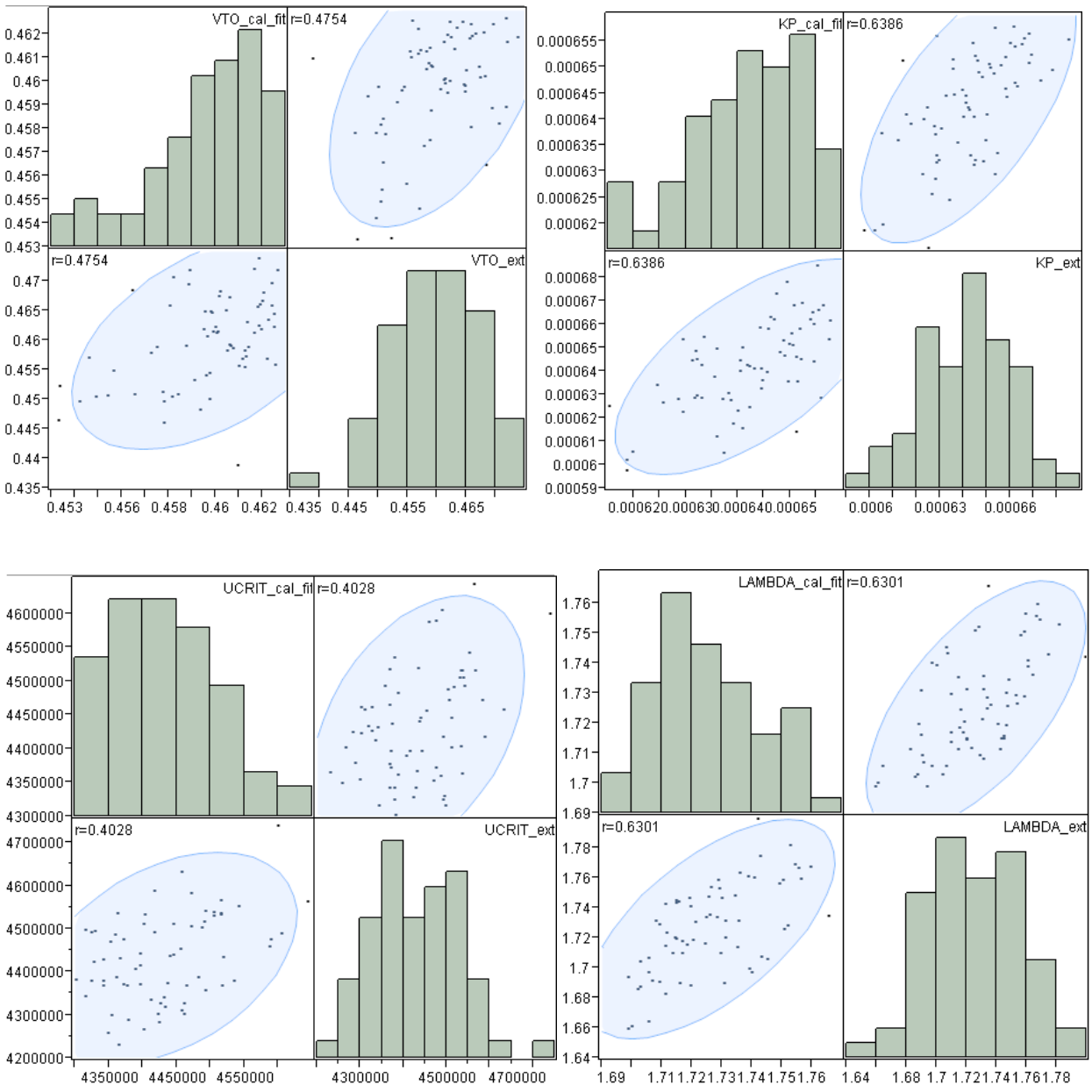


Figure 3-8 Comparison between Spatial Variability Linear Propagation Calculated Results and Extracted Reference Results
Correlation coefficients for all model parameters:
$\rho_{VTO,spatial}$=0.4754, $\rho_{KP,spatial}$=0.6386, $\rho_{UCRIT,spatial}$=0.4028, $\rho_{LAMBDA,spatial}$=0.6301

As seen from the comparison results and coefficient analyses, there is only moderate correlation (ρ around 0.5-0.6) between extracted reference values and model parameter values obtained from calculated coefficients in the spatial variability model.

The errors responsible for the errors in the moderate correlation structure come from two major sources: 1) calculation error in SBPV, i.e. linear regression on the coefficients; 2) modeling or fitting error in the simplified hierarchical spatial variability model, especially in the assumed whole wafer parabolic variability pattern. In order to decompose the errors shown here, we performed further analyses on the results. A full wafer parabolic spatial variability fitting on the reference set is done and the obtained coefficients are used to find the compact model parameter values under the assumptions of the hierarchical spatial variability model. Excluding the second error source, we performed a new correlation analysis on the model parameters; and for better illustration, fitted spatial patterns are also shown in the figures below.

As shown in the figures, good correlations are achieved in the compact model parameters spatially fitted on the parabolic pattern between calculated coefficients and reference fitting coefficients. The spatial patterns of all the compact model parameters over the full wafer also show good similarity between results from our method and reference set. Therefore, the error from the second source, i.e. our linear propagation method, is very small compared to the spatial variability pattern modeling and fitting. If a more advanced or complete hierarchical spatial variability model is applied, it will likely lead to better compact model parameter calculation results. So improvement on total error reduction, especially error from first source, will be discussed in the next chapter, along with techniques for selecting the electrical measurements and the corresponding compact model parameters to be extracted.

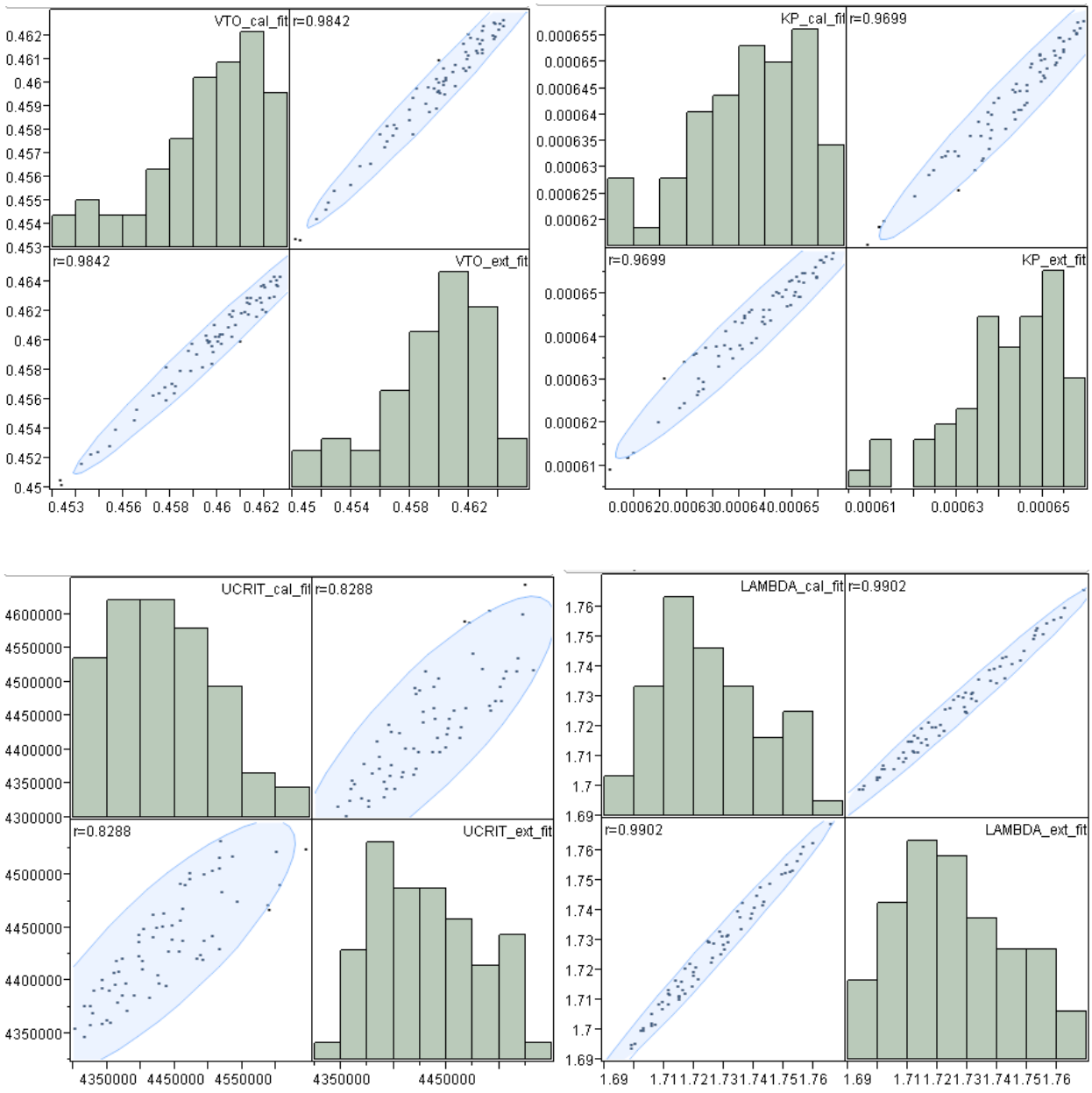


Figure 3-9 Comparison between Spatial Variability Linear Propagation Calculated Results and Extracted Reference Results, excluding hierarchical spatial variability model fitting errors
Correlation coefficients close to 1 are achieved for all model parameters (GOOD MATCH):
$\rho_{VTO,spatial,fit}$=0.9842, $\rho_{KP,spatial,fit}$=0.9699, $\rho_{UCRIT,spatial,fit}$=0.8288, $\rho_{LAMBDA,spatial,fit}$=0.9902

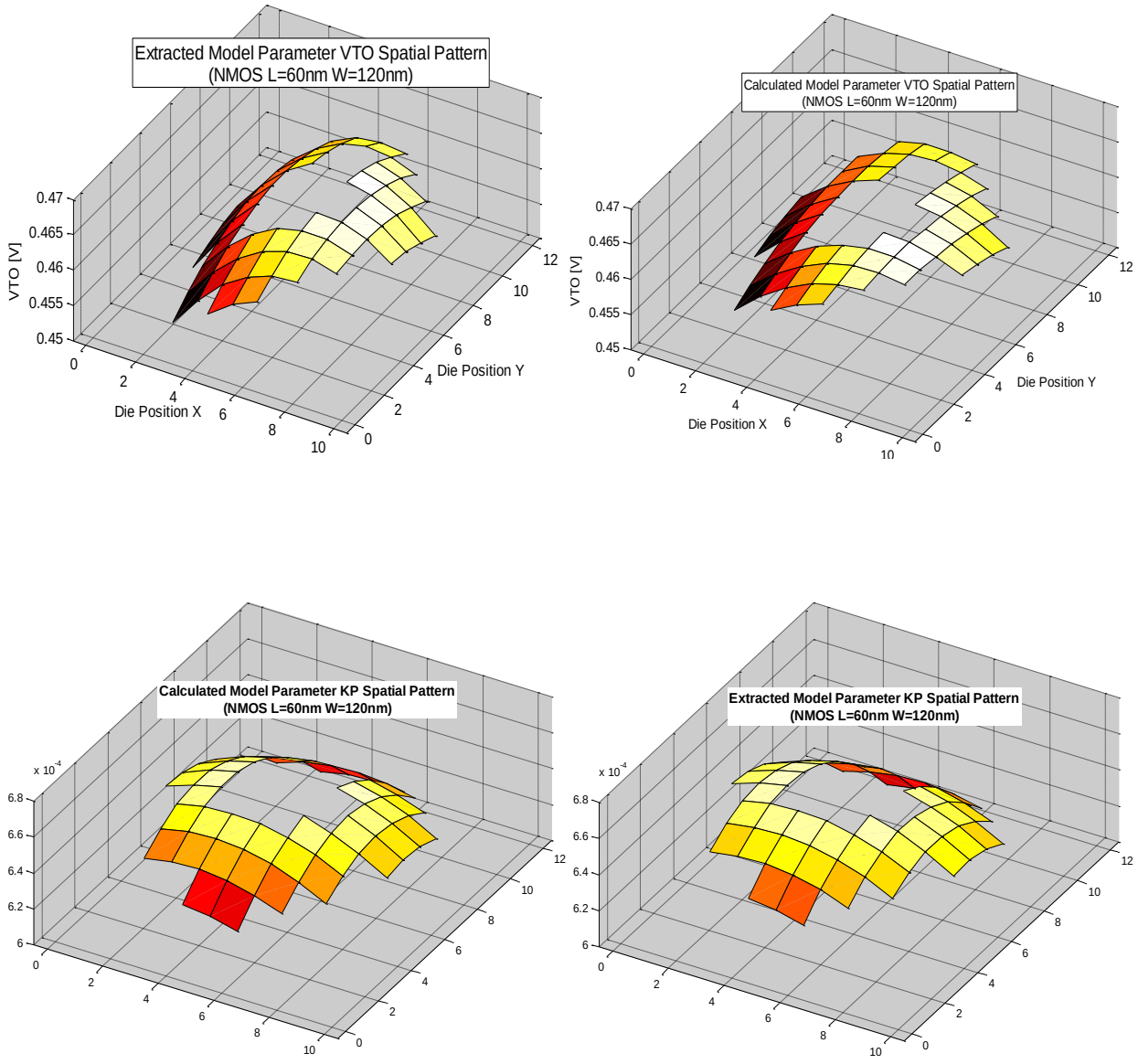


Figure 3-10 Fitted Spatial Patterns of Compact Model Parameters using calculated coefficients vs. Full-wafer Parabolic Spatial Variability Model Fitted Pattern on extracted reference set (up: VTO; down: KP)

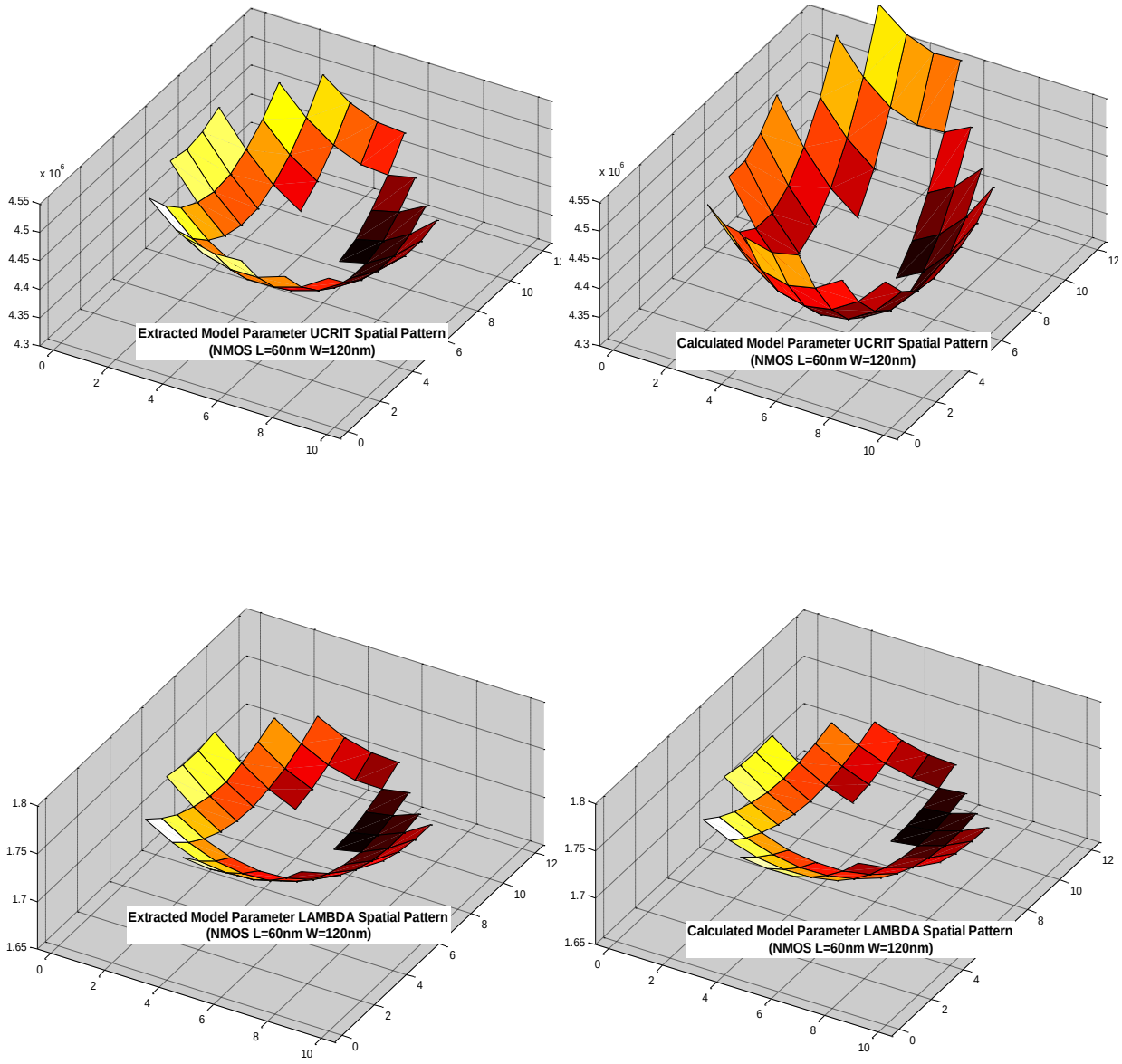


Figure 3-10 Fitted Spatial Patterns of Compact Model Parameters using calculated coefficients vs. Full-wafer Parabolic Spatial Variability Model Fitted Pattern on extracted reference set (up: UCRIT; down: LAMBDA)

Our SBPV method is not only effective for accurate statistical compact model characterization, but quite efficient in computational cost. As shown in the table below, significant reductions in total computational cost are achieved on the wafer level. The numbers shown in the table are

normalized to the unit operation, which is either one compact model parameter extraction per DUT or one linear propagation calculation step per parameter.

Table 3-5 Computational Cost for Different Compact Model Characterization Methods

Methods	Sensitivity Analysis	Extraction/Calculation
Individual Extraction	N/A	Number of DUTs per die × Number of dies = 68 ×432=29376 parameter extractions
Linear BPV	Number of e_i × Number of p_i = 4 ×5=20	1 × Number of dies = 68 linear propagations
SBPV	Number of e_i × Number of p_i = 4 ×5=20	1 × Number of variability spatial pattern coefficients = 6 linear propagations

References for Chapter 3

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Chapter 4

SBPV Parameter Selection

Compact model parameter extraction is usually done by fitting model predictions to real transistor I-V/C-V measurements, often over several transistors of different sizes. For deterministic model fitting a large set of parameters must be extracted, with the possible exception for some pre-defined technology constants. However, statistical compact model characterization only focuses on those model parameters that have physical meaning and represent actual process variations sources. Not all model parameters are suitable or necessary to be included in the extractable parameter set [4-1].

Table 4-1 BSIM and PSP Model Parameters for Statistical Compact Modeling [4-1]

Model	Parameter	Physical Meaning	Accounted Variations
BSIM	V_{TH0}	Long-channel threshold-voltage	Traditional threshold variation
	U_0	Low-field mobility	Current-factor variation
	N_{factor}, V_{OFF}	Sub-threshold	Sub-threshold slope and off-current variation
	M_{inv}	Moderate-inversion	Variations in moderate-inversion regime
	R_{dsw}	Source/drain resistance	Dopant variations in the source/drain
	D_{sub}	Drain-induced barrier-lowering	DIBL variation
PSP	*VFB0*	Flat-band voltage	Traditional threshold-voltage variation
	NSub0	Substrate doping	Random dopant fluctuations induced threshold-voltage variation
	CFL, ALPIL1	Short-channel effects	Short-channel effects variation
	U0, CS0	Mobility	Transport variation
	CT0	Interface state	Sub-threshold-behavior variation (with *NSub0*)
	RSW1	Source/drain series resistance	Variations at the source/drain region

As for the relatively simple EKV model in our test bench implementation, the small number of model parameters can still be classified into three groups based on their physical meaning and significance in device-behavior prediction [4-2][4-3]. The four parameters (*VTO*, *KP*, *UCRIT*, *LAMBDA*) used in our test bench implementation linear propagation fall basically into this group, with *LAMBDA* added into the set by a more advanced selection scheme shown below.

Table 4-2 EKV Model Parameters Classified for Statistical Compact Modeling [4-2][4-3]

Group	Parameter	Description	Note
Process-determined ***(technology constant)***	*COX*	Gate oxide capacitance	
	XJ	Junction depth	
	DL	Channel length correction	L_{eff}=L+DL
	DW	Channel width correction	W_{eff}=W+DW
First-order effects ***(statistically extractable)***	*VTO*	Long-Channel threshold voltage	Threshold-voltage variations
	KP	Transconductance parameter	Current-factor or transport variations
	UCRIT	Longitudinal critical field	
Second-order effects ***(performance insensitive)***	*LAMBDA*	Depletion length coefficient	
	THETA	Mobility reduction coefficient	
	GAMMA	Body effect factor	
	LETA	Short channel effect coefficient	
	WETA	Narrow width effect coefficient	

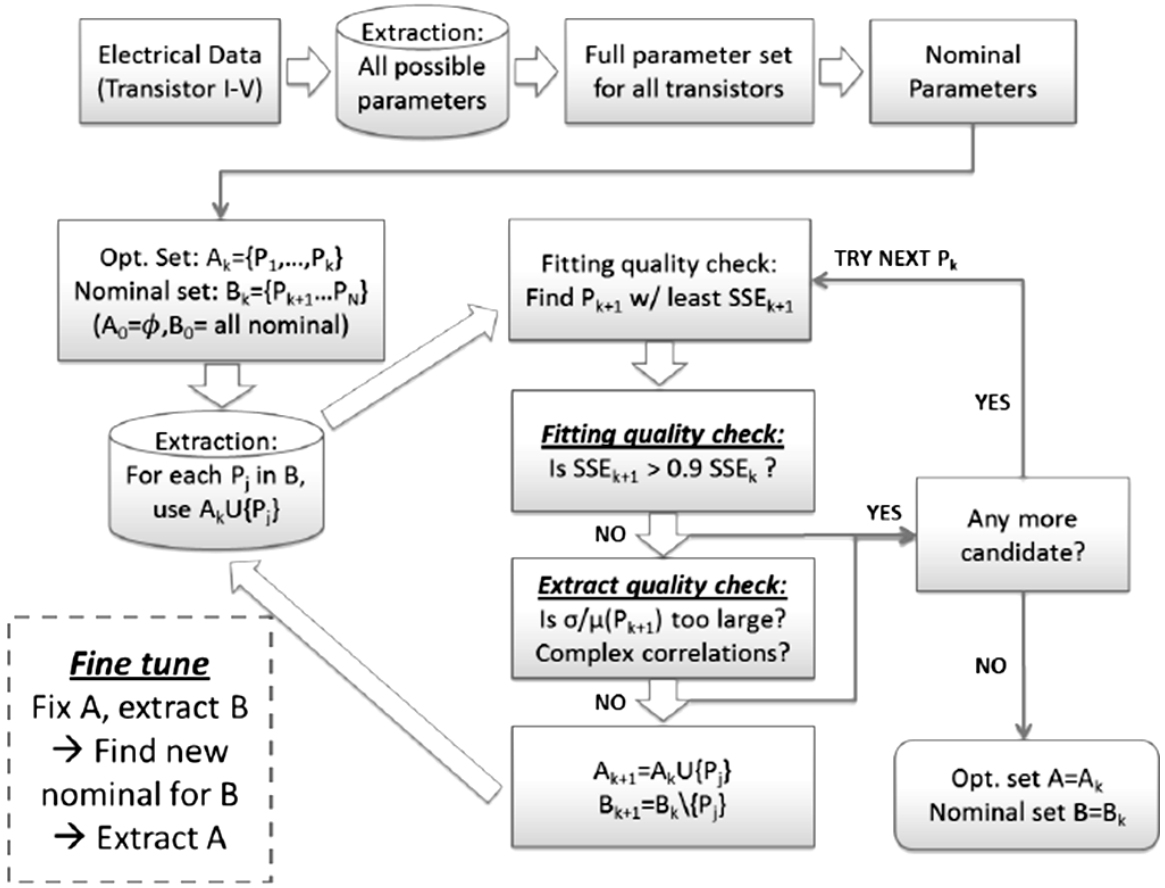

Figure 4-1 Statistically Extractable Compact Model Parameter Selection Scheme [4-3]

4.1 Electrical Measurements Selection

. As mentioned briefly when reviewing the BPV method in Section 3.1, the selection criteria for the electrical measurement set $\boldsymbol{e}$, used in the linear BPV method as well as our proposed SBPV method, should meet two criteria. First, since the purpose of compact variability modeling is better statistical circuit simulation, measurements of transistor characteristics that have large impact on circuit performance should be included in the set. This requires knowledge of circuit applications and device operations. In addition, since our method is based on linear regression of the coefficients in the spatial variability model, the measurement set selection should ensure that the spatial sensitivity matrix $\boldsymbol{S_{spatial}}$ is well conditioned for calculation accuracy. A sensitivity analysis based selection scheme is proposed for this purpose.

As shown in the flowchart in Figure 4-2, nominal compact model parameters are first determined by performing full extraction on nominal wafer data. The nominal data set is obtained by pre-processing full-wafer I_{on} measurements, as shown in figures below. Next, we fix all the compact model parameters to their nominal values except for those selected for extraction, as discussed in the previous section. Sensitivity matrix calculations are then performed on all the I-V measurement points (100 points per transistor) and the selected model parameters (4 EKV model parameters). We then examine the $\boldsymbol{S_{100\times4}}$ matrix and perform $\boldsymbol{e}$ set selection based on two criteria: 1) extreme absolute values exclusion, i.e. keep only the rows with moderate $\boldsymbol{s_{ij}}$ values (each row corresponds to one $\boldsymbol{e_i}$), which ensures non-singularity in the matrix; and 2) relative rankings of importance, i.e. select the rows with highest $\boldsymbol{s_{ij}}$ values among all columns (each column stands for one $\boldsymbol{p_j}$), which selects electrical measurements that are highly sensitive to all model parameter variations.

For fast analysis or initial calibration, it is not wise to calculate the large sensitivity matrix by blindly performing simulations on all possible ***e*** set candidates. A rough estimation of the sensitivities can be done by analytical derivation on basic compact model equations or hand calculation with knowledge of MOSFET device physics, which is discussed in detail in [4-4].

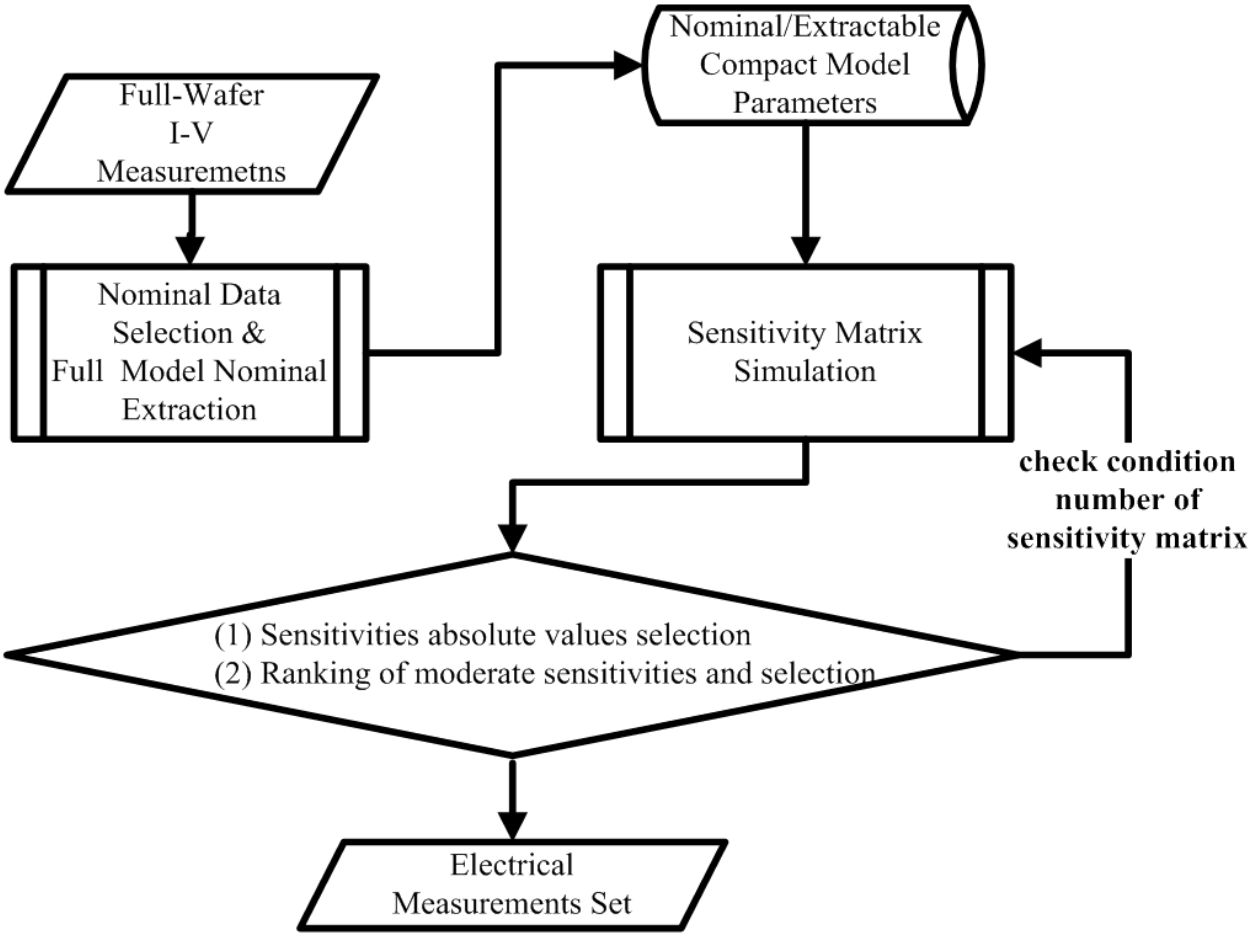

Figure 4-2 Electrical Measurement Set Selection Flowchart

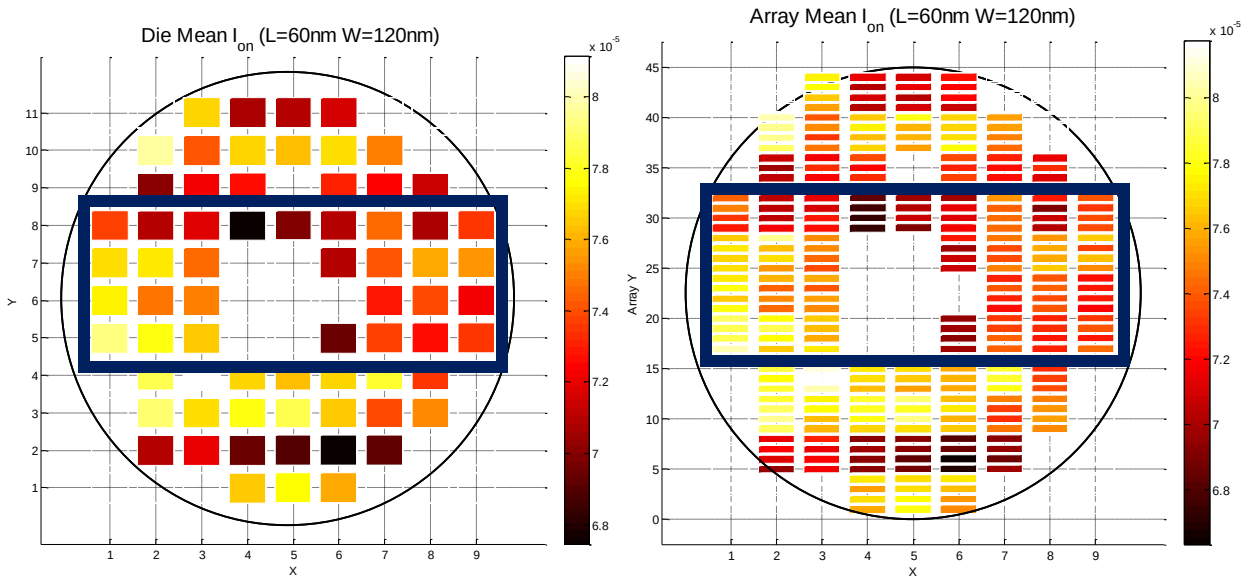

Figure 4-3 Wafermap of Electrical Measurements
The nominal dataset is chosen as measurements from the dies within the boxed area;
[Note] Mean values are calculated at the transistor array level
on the right plot in addition to ones at the die level on the left

The five electrical measurement metrics (orange) found using our selection scheme are shown on a typical MOSFET DUT I_d~V_{ds}/V_{gs} curve. Their selection is based on the sensitivity matrix simulation results shown in the following plots. The surface plots illustrate the sensitivities of I_{ds} measured at different voltage bias points (V_{ds}, V_{gs}) to the compact model parameters. As we can see from the plots, our main selection decisions are made based on the relative rankings of $s_{I,VTO}$ and $s_{I,UCRIT}$, since $s_{I,KP}$ and $s_{I,LAMBDA}$ show small changes over the entire plane.

Also shown on the MOSFET DUT I_d~V_{ds}/V_{gs} curve are the metrics (purple) used in our test implementation, which is determined using the criteria suggested in [4-4]. This selection has wider current/voltage coverage; this is because saturation and sub-threshold performance plays a key role in digital circuit applications.

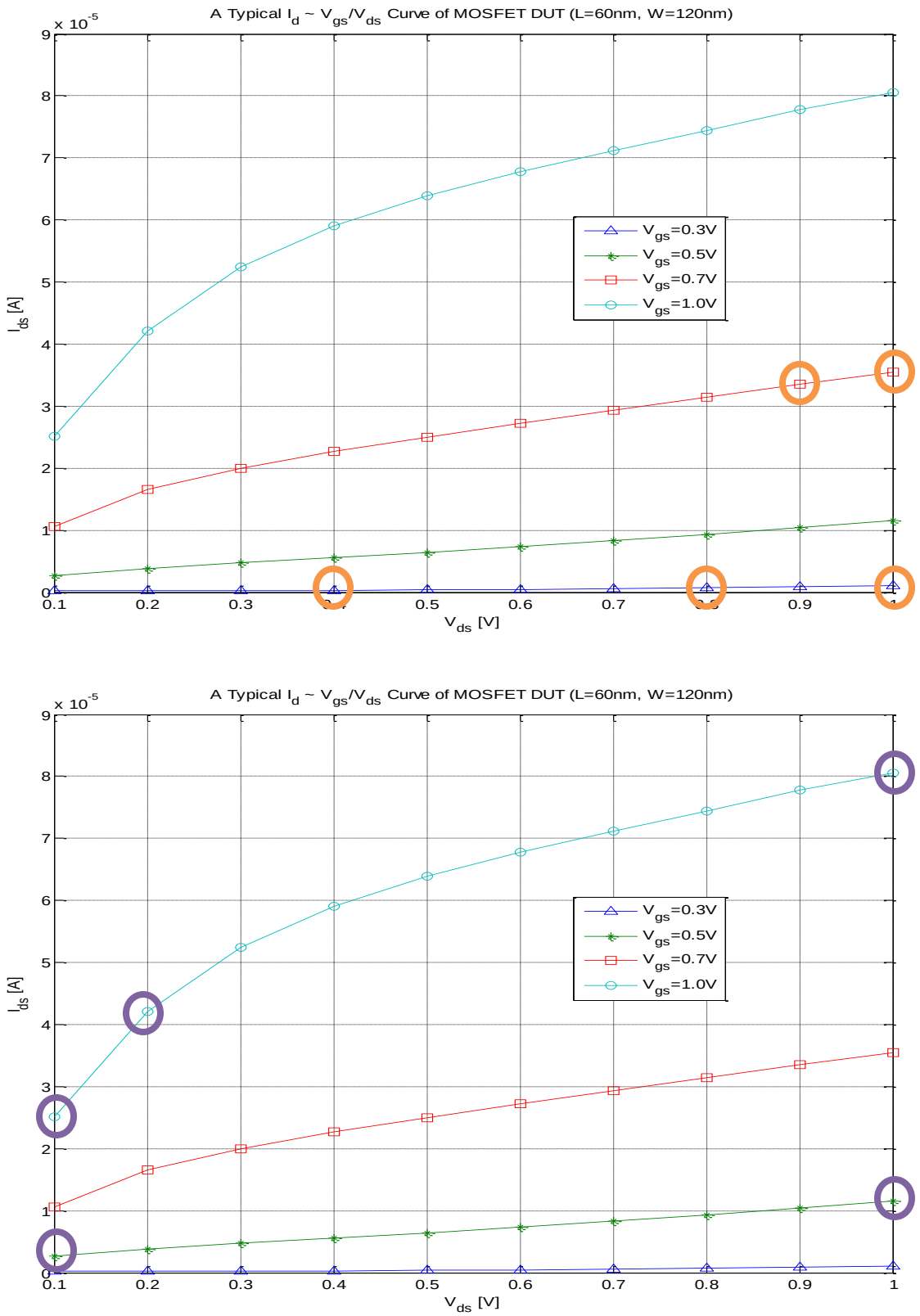

Figure 4-4 Typical I_{ds}~V_{gs}/V_{ds} Curve of MOSFET DUT
Electrical metrics set selected by our proposed scheme (orange) [upper] vs. [4-4] (purple) [lower]

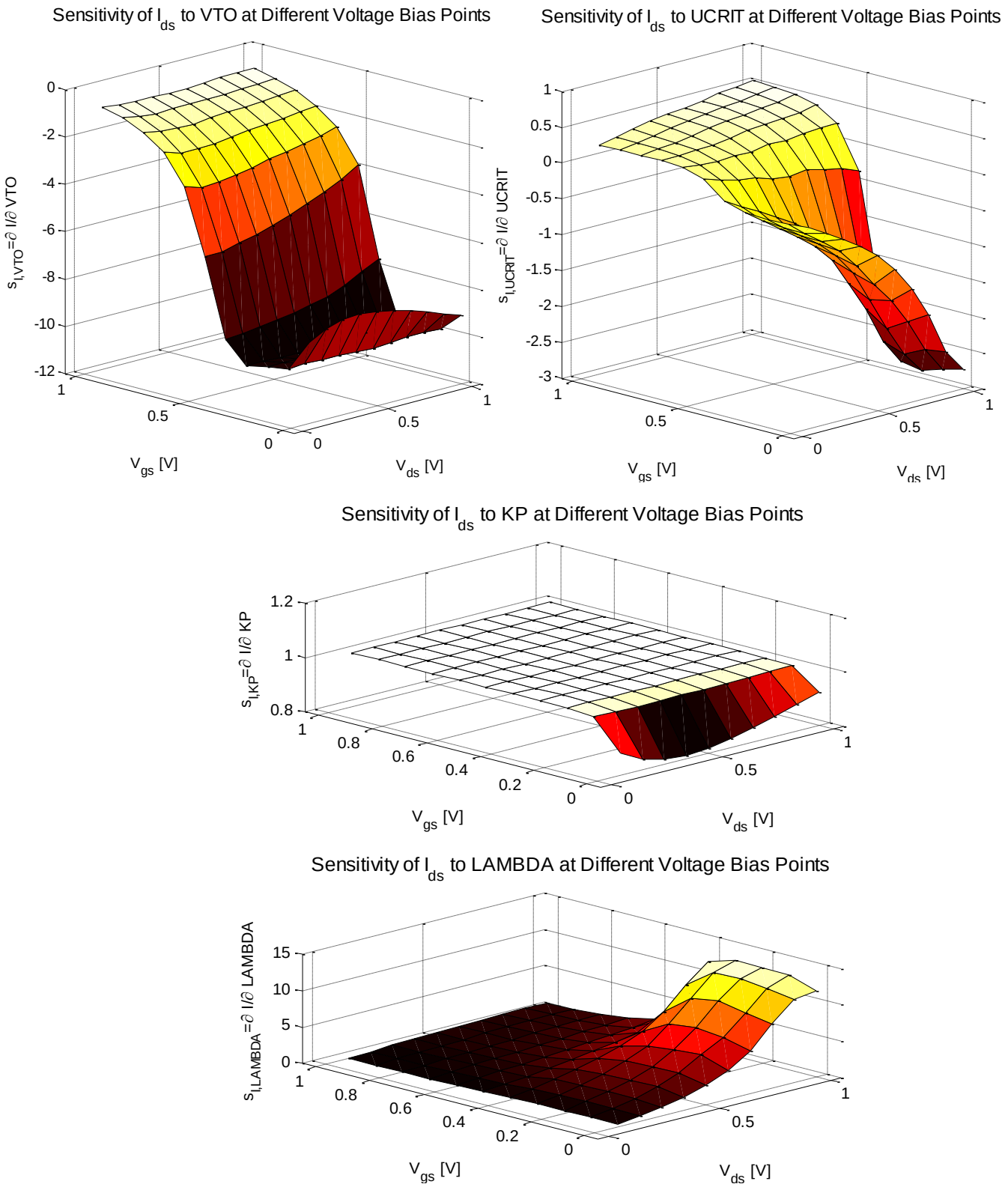

Figure 4-5 Sensitivities of I_{ds} to EKV Compact Model Parameters @ different (V_{gs}, V_{ds})

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Chapter 5

Conclusions

An efficient, variability-aware compact model characterization methodology is required to capture the hierarchical variability structure observed in modern IC manufacturing processes. Consequently, our goal was to develop a compact model variability characterization method based on statistical linear propagation, which directly transfers the hierarchical variability spatial pattern observed in electrical measurement data to specified compact model parameters. We call this method the Spatial Backward Variability Propagation method, or SBPV. This methodology has been implemented and tested using transistor I-V measurements and the EKV-EPFL compact model. The model parameters that will capture the spatial variability are characterized using linear regression on spatial pattern coefficients, using with a spatially-tuned sensitivity matrix, which is first verified by the traditional linear BPV method. Calculation results are then compared with reference set obtained by full-wafer direct model parameter extractions. Good match is realized between the “calculated” and “extracted” compact model parameters. Further

studies are done on the proper selection of both compact model parameters and electrical measurement metrics used in the method. Results are shown in comparison to those reported in the relevant literature.

The proposed spatial variability linear propagation method can be extended and applied on more complicated and complete compact models, such as the industrial standard BSIM or PSP models. More advanced hybrid-hierarchical variability models, including spatial / deterministic / random on and across device / die / field / wafer / lot levels, can be included in the SBPV procedure. Most importantly, well-designed variation-sensitive test structures fabricated using cutting-edge technology are need to build better statistical compact models and characterize with our methodology.

In addition, these variability-aware characterized compact models may be integrated into the existing statistical circuit design flow for accurate prediction on circuit performance deviations caused by process variations. Our SBPV method will serve a good role in the statistical IC design flow by providing large numbers of physical-variation-aware compact model cards for Mote Carlo simulations or customized corner simulations. More than that, since the combination of random and spatial variability often yields non-Gaussian distributions, we believe that SBPV will more realistically capture the tails of those distributions and therefore be more suitable for generating proper corner models. Due to the high efficiency of our method, model cards for different design parameters, such as transistor length and width, can be generated specifically for each design. This will help increase both the speed and accuracy in statistical circuit simulation results.

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