Characterization of Variability in Deeply-Scaled Fully Depleted SOI Devices

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Characterization of Variability in Deeply-Scaled Fully Depleted SOI Devices

by Aikaterini Papadopoulou

Research Project

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Abstract

Scaling of CMOS technology into the deep submicron regime gives rise to process variability, which in turn compromises circuit yield. One of the main sources of variability is random dopant fluctuation (RDF) in the channel. Fully Depleted Silicon on Insulator technology has been proposed as a promising alternative to bulk CMOS, due to it's undoped channel which reduces RDF, as well as due to its better electrostatic control of the channel.

A testchip for measurement and analysis of variability in a 22nm FDSOI process has been designed. Among other experiments, the tetstchip features an array of 11x11 tiles with variability measurement structures. Each tile contains circuits to measure IV and CV device characteristics, RO frequencies and resistor values. Scan chains and multiplexing are employed to enable analysis of a large number of DUTs with a limited pad count.

The goal of this testchip is to characterize variability in FDSOI. This will be achieved by extracting systematic and random variation data from specifically designed test structures. The focus of this testchip is to decouple different sources of random variation in order to electrically measure line edge roughness and silicon thickness variation due to surface roughness, characterize the effects of source and drain doping, and quantify the contribution of ground planes and back-biasing in FDSOI variability.

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1

Introduction

The rapid technology developments in the metal-oxide-semiconductor industry have lead to CMOS scaling down to the sub-20nm regime, and according to the 2009 ITRS projections (1) printed gate lengths will scale down to approximately 12nm by 2020, resulting in significant changes in both the information processing technology as well as the device manufacturing technology. From the standpoint of information processing technology, the spectrum of applications has now broadened and improved. Superior device performance and high density have given new perspective to circuit design, ranging from high speed analog front-ends to digital processors and memory. At the same time, device manufacturing technology is facing new challenges. Lithography, physics and cost limitations make sub-45nm device optimization a hard task, thus compromising the future of scaling. Under these circumstances, research in CMOS scaling and device optimization as well as in new devices and materials has the potential to determine the future steps of circuit design.

1.1 Modern CMOS evolution and challenges

Bulk CMOS has been around for more than 40 years, and in that time its manufacturing technology has been getting more and more interesting. With extreme channel length scaling, new issues and challenges appeared; increased leakage made net power a limiting factor in frequency scaling, robustness was compromised due to increased variability, interconnect scaling and complexity management also posed new limitations.

In response to the aforementioned problems, the introduction of process modifications as well as new technologies and materials was inevitable. Initially, changes in the manufacturing process such as shallow trench isolation (STI), mobility enhancements, high-K dielectrics and metal gates were used to improve device characteristics. These improvements indeed made further CMOS scaling possible for some time, but proved not to be sufficient for very aggressively scaled technology nodes. In modern sub-45nm nodes, in addition to leakage, variability turns out to be a major bottleneck. As a result, new technologies and materials are being developed. The need for higher performance and lower leakage led to the development of Partially Depleted (PD) Silicon-On-Insulator (SOI), which features an insulator layer below a partially-depleted channel, and results to lower junction capacitance and leakage. Additionally, the need for better control of short channel effects led to an increasing interest in thin-body devices resulting to technologies such as Fully Depleted (FD) SOI and FinFETs (2, 3, 4). FDSOI devices have a very thin undoped body, while FinFETs wrap the gate around two sides of the body. Both types of devices improve the electrostatic integrity, as will be further discussed in Chapter 2. Meanwhile, the academic world is exploring the option of using radically new materials and devices, such as graphene and Nano-Electro-Mechanical switches (NEMS), to cope with voltage scaling and/or leakage issues.

1.2 Research goals

The main focus of this work is the evaluation of variability in FDSOI technology at deeply-scaled nodes. In FDSOI, the undoped thin body allows for superior channel control in comparison to bulk CMOS, while the structure and fabrication is simpler than that of vertical devices like FinFETs. In addition to that, its intrinsic channel doping reduces the impact of random dopant fluctuation (RDF), which has been the most significant source of random variation in bulk technologies. However, now there are additional sources of variation that need to be considered and evaluated; the thickness variation of the thin silicon film, the oxide charges not only of the gate dielectric but also of the insulator layer, the RDF of the source and drain regions which changes the effective channel length, and the RDF of the doping below the insulator layer, all contribute to the total amount of variation in the device. Other expected sources of variation are the line edge roughness (LER), the surface roughness and the variation to due to strain or stress, which appear both in bulk and FDSOI.

The goal of this research is twofold.

1. Evaluate FDSOI technology:
   More specifically, this work aims at understanding the sources of systematic and random variability in FDSOI devices. In addition to the conventional sources of variation, this work targets at characterizing effects that are specific to the FDSOI technology. The main goals are to electrically measure the most dominant sources of variation in FDSOI, LER and T_{Si}, as well as characterize the effects of S/D doping, ground plane doping and oxide thickness variation in the insulator layer. This requires efficient and compact test structure design which will allow variability data extraction from many devices within a die.

2. Improve circuit yield:
   After the different types of variations are quantified and analyzed, this data can

be used to tune model parameters in existing models or develop new models which can more accurately capture variability, thus enabling co-optimization of performance and yield through a variability-aware circuit design process. The same data can also be utilized to improve process engineering and manufacturing steps, in an attempt to reduce variability.

2

Fully Depleted Silicon on Insulator Technology

As discussed in Chapter 1, bulk CMOS scaling comes with some major roadblocks which gave rise to research on different technologies, like FinFETs and FDSOI. The FDSOI MOSFET is one of the most promising candidates for next technology nodes, due to its potentials for low variability and excellent electrostatic integrity. The device consists of a very thin, fully-depleted transistor body on top of a buried oxide (BOX) layer, placed between the channel and the substrate. The use of undoped body eliminates the floating body effect and provides immunity to V_{th} fluctuations due to RDF, while the body thickness (T_{si}) ensures good electrostatic control of the gate.

In this chapter, details of the FDSOI process are going to be discussed, along with its potentials in terms of performance and variability.

2.1 FDSOI technology features

Fully depleted silicon on insulator technology evolved as an improvement of partially depleted SOI, in order to eliminate the memory effect. FDSOI devices are thin body devices, and the body in this case is very lightly doped or undoped. Under the channel, there is a thick ($\sim 100nm$) or thin ($\sim 10nm$) insulator layer, called the buried oxide. In a modern FDSOI process, the source and drain are typically raised and faceted, while metal gate stacks and high-K dielectric form the gate of the device. Finally, in the case of thin BOX, doping below the BOX is sometimes used, called ground plane (GP) doping. Those main features are shown in Figure 2.1, and will be discussed in more detail in the following paragraphs.

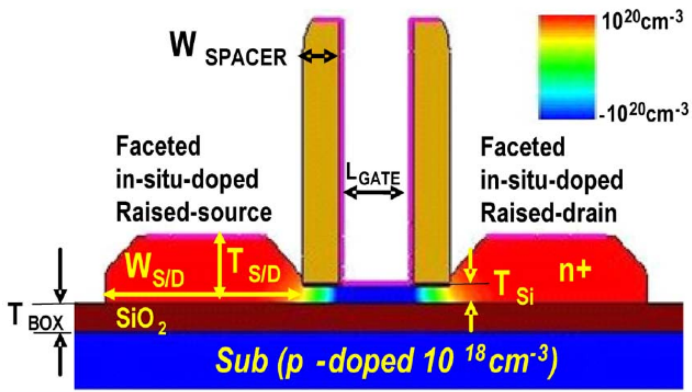

Figure 2.1: Fully depleted silicon on insulator transistor (5)

2.1.1 Undoped thin body

As implied by the name of this technology, its key distinction from previous technologies is the fact that the channel is fully depleted. In a MOSFET, application of a

positive gate bias to an N-type transistor creates a depletion layer by forcing the positively charged holes away and leaving only negatively charged acceptor ions close to the gate. In a PDSOI N-type MOSFET, the holes are pushed toward the buried oxide layer creating a region called floating body, which can store charge. That creates a modified switching threshold point, which depends on the history of the circuit. However, when the channel is very lightly doped and very thin, the depletion region fills the full length of the body, thus eliminating the floating body region. History effect is reduced by $\sim 60\%$ in FDSOI technology comparing to PDSOI with a channel thickness of 18nm, while smaller channel thickness can result in virtually zero floating body effect (6). As a result, FDSOI technology suffers from less threshold voltage variability due to the history effect.

Except for channel doping, another important feature of the channel is its thickness, also called silicon thickness (T_{si}). The importance of T_{si} can be readily understood by the definition of electrostatic integrity (EI) of a device, which is a measure of the device resistance to parasitic effects such as short-channel effect (SCE) and drain-induced barrier lowering ($DIBL$) (7).

$$EI \equiv \left(1 + \frac{X_j^2}{L_{el}^2}\right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} \tag{2.1}$$

In equation 2.1 X_j denotes the source/drain junction depth, L_{el} the electrical channel length, T_{ox} the effective oxide thickness and T_{dep} the depth of the depletion region. SCE and $DIBL$ are related to EI as shown in equations 2.2 and 2.3 (7, 8, 9, 10), where ϕ_d is the source -to-channel junction built-in potential and V_{ds} the drain-to-source voltage.

$$SCE \propto EI \cdot \phi_d \tag{2.2}$$

$$DIBL \propto EI \cdot V_{ds} \tag{2.3}$$

In other words, larger depletion depth exacerbates short channel effects, which makes thin body devices very appealing for aggressively scaled technology nodes. In the case of FDSOI devices $T_{dep} = T_{si}$, and thus a thinner body provides better control of the device. Reported T_{si} values scale down to 6nm (11).

2.1.2 Buried oxide thickness and ground plane doping

Another important characteristic of FDSOI devices is the BOX thickness. The advantage or disadvantage of using thin over thick BOX is still a controversial subject, although recent publications have demonstrated benefits of using thin or ultra-thin BOX (12, 13, 14). Device simulation has shown that in thick BOX devices there is electrostatic coupling between the drain and channel, which results to degradation in the DIBL factor and the subthreshold slope of the transistor. The coupling can be suppressed by thinning down the BOX (12). This effect can be modeled by assuming that T_{dep} can expressed as shown in equation 2.4, where λ is a fitted function of T_{BOX} and L_{el}.

$$T_{dep} = T_{si} + \lambda T_{BOX} \tag{2.4}$$

Although the electrostatic coupling is supressed, thin BOX devices have the disadvantage that they exhibit higher junction capacitances comparing to thick BOX. A thick insulator layer ($\sim 100nm$) almost completely eliminates any junction capacitance, which has been one of the main arguments for the introduction and use of PD-SOI devices. On the other hand, a thin insulator layer ($\sim 10nm$) brings that capacitance back into play, and so device performance is degraded. Comparing to bulk, however, that capacitance is still lower and much more linear with voltage.

Perhaps the greater advantage of using thin BOX occurs when ground plane doping is used as well (Figure 2.2). When the BOX is very thin, a depleted zone can extend under the BOX, which contributes to an increase in the BOX equivalent thickness. This effect can be countered by using GP doping, which limits the field penetration under the BOX (13). The result is a $DIBL$ reduction of the order of $\sim 50mV$ (14). Furthermore, the combination of a very thin BOX with GP doping in an FDSOI device with metal gate can result to threshold shifts of up to $\sim 100 - 130mV$, depending on the amount of doping and the BOX thickness (13, 14). Thinner BOX results to larger V_{th} shift. This threshold shift affects the I_{ON}/I_{OFF} curves of a transistor and allows for low power (LP) or high performance (HP) device optimization. Finally, ground plane doping enables further V_{th} modulation if a ground plane contact is added for back-biasing. The back-gate contact creates a quasi-double gate device and makes circuit-level threshold modulation possible, and thus enables the co-integration of standard threshold (SVT), low threshold (LVT) and high threshold (HVT) devices, as demonstrated in (15, 16, 17).

2.1.3 Source/drain engineering

Channel length scaling to extremely short values has made channel resistance R_{ON} very small, to the extent that the series resistance of the channel due to the source and drain regions R_{series}, which does not scale as well as R_{ON}, has become a serious limitation to the device maximum current $I_{ON} \approx \frac{V_{DD}}{R_{ON}+R_{series}}$. As an example, R_{series} is approximately 25% of R_{ON} for the 45nm technology node in bulk CMOS. The effect is even worse in FDSOI technology due to the small contact area, which leads to a large contact resistance. In order to deal with this problem, process steps have been developed to reduce the S/D resistance. The source and drain regions are raised, as shown

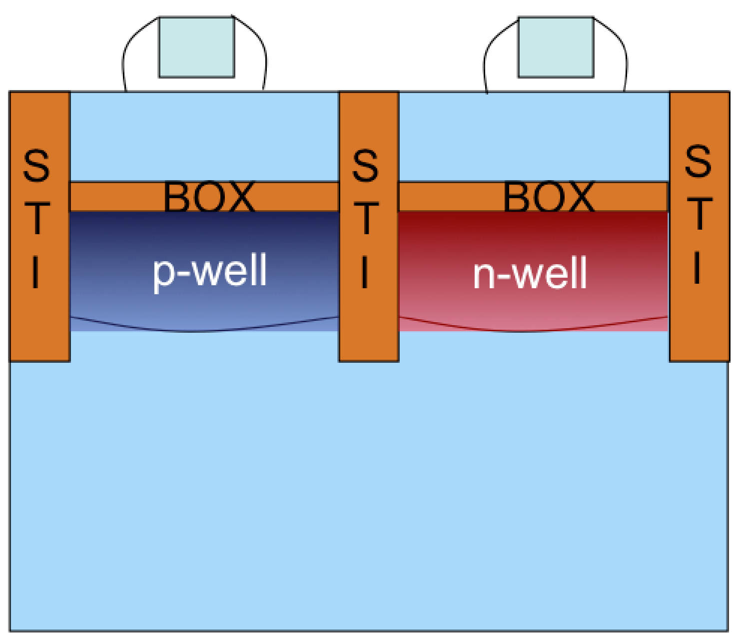

Figure 2.2: Illustration of ground plane doping in FDSOI devices

in figure 2.1, and dopants are diffused toward the channel by means of rapid thermal annealing, forming the S/D extension. Typically the raised S/D regions are formed by single epitaxial growth of doped $SiGe$, but one way to further reduce resistance is by use of double selective epitaxy, which can lead to an I_{ON} increase of $\sim 25\%$ (18). For double epitaxy, in-situ boron doped $SiGe$ is typically used for PFETs and in-situ phoshorus doped $Si : C$ for NFETs.

2.1.4 Gate engineering

The introduction of metal gate (MG) and high-k (HK) dielectrics is another process improvement that has a significant role in enabling CMOS scaling. Extreme gate oxide thickness scaling, down to $\sim 1.2nm$, brought up reliability and gate leakage problems. Consequently, HK/MG was introduced, both in bulk and FDSOI, targeting

performance improvement, power reduction and further channel length scaling. More specifically, recently published data on FDSOI process technology report the use of TiN/Al_2O_3 metal gate stack, achieving reduction of the electrical oxide thickness (EOT) down to $14\mathring{A}$, as shown in Figure 2.3. The addition of Al_2O_3 in the metal gate stack provides the possibility for modulation of the metal gate work-function, resulting in V_{th} shifts of the order of $100mV$, in order to acommodate both LP and HP device flavors (19).

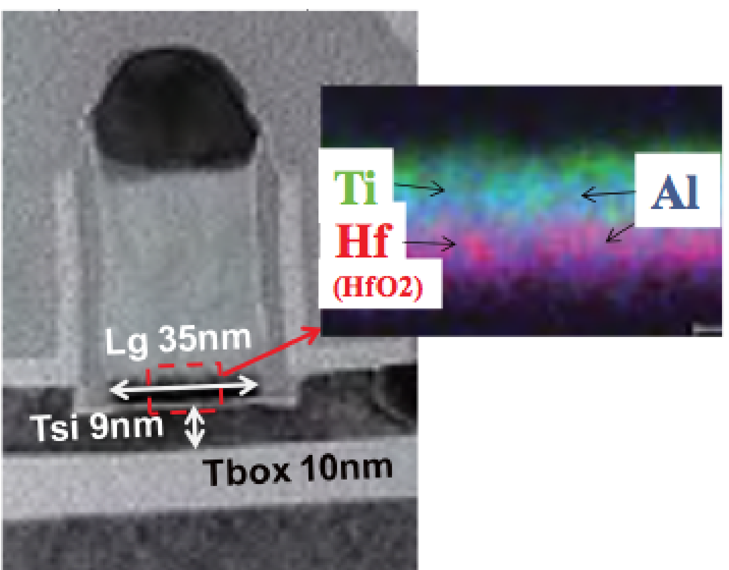

Figure 2.3: TEM cross section of an FDSOI device with Al_2O_3 inserted in the gate stack (19)

2.1.5 Other process features

Just like in bulk technology, additional process features of FDSOI technology include the use of stress and strain boosters as well as deep wells. As far as stress and strain are concerned, the technology is fully compatible with most of the existing stress options discussed in Chapter 3, like the use of STI and CESL techniques. With extreme scaling, introduction of local strain like spacers between the gate and the contact becomes increasingly difficult, making global strain options, like the use of strained-SOI (sSOI) wafers an important alternative. Another significant process improvement is the addition of deep N-well under a p-type GP doping, in order to isolate it from the p-substrate. Without a deep well, a p-type GP is shorted with the substrate, thus shorting all p-type ground planes together. The introduction of the deep N-well allows individual control of a transistor (or group of transistors) and adds design flexibility. However, it does make the manufacturing process more complicated and the layout less compact.

2.2 FDSOI performance and challenges

Low variability, good electrostatic integrity and multiple threshold device integration are some of the main advantages of FDSOI technology. However, any attempt for process improvement is meaningless if it is not accompanied by improvement in circuit design, performance and reliability. In this section, the potentials of FDSOI for efficient circuit design will be evaluated.

The current trend in digital circuit design is maximum performance for low power consumption. As mentioned above, high performance can be achieved in FDSOI by lowering the threshold, either through metal gate work-function engineering or through back-biasing. However, lowering the threshold voltage comes with the risk of forward biasing the diode between two adjacent ground planes, and thus complicates the circuit

design process. Another potential advantage of this technology stems from the fact that it has very low junction capacitances, especially in the case of thick BOX. However, the raised source and drain add extra capacitance to the gate. Changing the S/D to a faceted shape helps reduce the gate capacitance; it may still be higher than bulk though. Unless the capacitance can be lowered by appropriate process engineering, there is no clear speed advantage of FDSOI versus bulk in terms of capacitance. Finally, a device of a lower DIBL technology (see Equations 2.2,2.3) has better subthreshold slope and thus higher linear current, compared to a device optimized for the same I_{ON} and I_{OFF} in a higher-DIBL technology. This implies that the effective current in FDSOI can potentially be higher comparing to bulk, especially in the case of complex gates and stacked devices.

A more obvious benefit of FDSOI is its potential for low-power applications. Since the source and drain pn-junctions are eliminated, there is no junction leakage. Short-channel effects can be controlled by the body and BOX thickness, allowing for a less aggressive scaling of the gate dielectric, which implies that gate-induced leakage is less of a concern. Reduced V_{th} roll-off and light channel doping result in lower threshold variation, thus enabling high yield design even at lower supply voltages (5). Overall, this technology is promising for low-power design.

2.3 Conclusion

In this chapter, the most important features of FDSOI technology were presented, and its main differences from bulk CMOS technology were discussed. Low variability and good electrostatic integrity were identified as the greatest advantages of this technology. These characteristics revealed its potential for high performance and mainly for low power applications. The most common sources of variability that appear in bulk and FDSOI technologies will be discussed and compared in Chapter 3.

2. FULLY DEPLETED SILICON ON INSULATOR TECHNOLOGY

3

Systematic and random variability

While in the past the effects of variability in circuit design and operation were not as pronounced, scaling of CMOS technology into the deep submicron regime has made them increasingly significant, to the point that they are now considered a major bottleneck to further scaling. Analog circuit performance and digital circuit yield are both compromised because of increased variation in oxide thickness (T_{ox}), threshold voltage (V_{th}) and effective channel length (L_{eff}). Variability can be broadly classified as systematic or random, depending on its nature and sources. Systematic variability refers to all parameter variations that are predictible, and thus can be modeled and understood. On the other hand, random variability refers to any random mismatch caused by atomic level differences between identical devices, such as random dopant fluctuation (RDF), line-edge roughness (LER) and film thickness variation (20). Distinguishing different types of variability and understanding their sources will allow process engineers to target their optimizations in order to address the problem and circuit designers to account for variation and perform variability-aware design.

In this chapter, the various types of variability are introduced. Next, some of the

major sources of variability are discussed, and finally its effects on integrated circuits are evaluated for deeply-scaled technology nodes.

3.1 Characterization of variability

Process variations can be classified in many different ways, depending on their nature, their sources or their spatial and temporal characteristics. In (20) two main categories are used; intrinsic and extrinsic. Intrinsic variations are those that originate from atomic-scale effects, like quantum-mechanical effects and statistical variation in dopant profiles and particles. Extrinsic variations are mainly attributed to any shift in the process conditions, which causes parameter fluctuation usually with some spatial correlation. Process variations can be further classified to:

1. Lot to lot (L2L)
2. Wafer to wafer (W2W), within a lot
3. Die to die (D2D), within a wafer
4. Within die (WID)

The above classification reflects the spatial characteristics of variations. Within die variations are defined by parameters that vary significantly over distances smaller than the dimension of a die. Parameters that vary gradually across a wafer cause die to die variations. Wafer and to wafer variations cause different wafers to have different properties. In a typical design methodology, designs are made to satisfy the worst case corners which consist of the total within die and die to die variations.

3.2 Sources of variability

The main sources of variability are related to physical and chemical atomic-level phenomena, the operating environment and the manufacturing process. Perhaps the most important reason for increased random device parameter fluctuations is that CMOS technology has scaled into atomic-scale dimensions. The size of an atom is on the order of $\sim 1\mathring{A}$. In this regime, the intrinsic parameter fluctuations introduced by the discreteness of charge start to dominate (21). Smooth, continuous and distinct interfaces become granular and pebbled with atoms. Quantum mechanical properties of these discrete entities come into play and the classical models become increasingly inaccurate. Secondly, voltage and temperature variations as well as aging can contribute to device parameter variations. Another major contributor is the manufacturing process and its different steps. The implant and annealing process cause a random number of dopants to be randomly positioned in the channel. Oxide thickness variations are caused by non uniformity in the process of oxide growth. Non-uniform annealing temperature can cause further variation in the threshold voltage, while strain and stress can affect carrier mobility both in a random and a systematic fashion. Finally, lithography and etching effects induce variation in critical device sizes, like channel length and width, which are much narrower than the light wavelength used to print them.

Table 3.1 summarizes the different sources of systematic and random variability. Some sources of variability affect bulk and FDSOI devices in similar ways; channel length and mobility variation due to systematic or random effects appears in both types of devices. RDF is more prominent in bulk, since it causes variations in the channel doping. In FDSOI, there is RDF in the source and drain regions, which changes the effective channel length, and in the plane below the BOX. On the other hand, variations due to surface roughness are expected to be more prominent in thin and ultra-thin BOX FDSOI, since surface roughness changes the silicon film thickness.

Parameter	Systematic	Random
Effective channel length	Litho and etching (proximity effects, orientation)	LER
Doping concentration	Non-uniformities in implant dosage, annealing	RDF
Mobility	Systematic variation in strain boosters, STI, S/D area, contacts etc.	Random strain variation
Film thickness	Non-uniformity in oxide deposition and growth, chemical-mechanical planarization	Surface roughness

Table 3.1: Systematic and random variations of MOSFET parameters and their sources

3.2.1 Random dopant fluctuation

One of the most important sources of variability is RDF. In long-channel bulk CMOS devices, the assumption that dopants create a locally uniform volume charge density, which is related to the potential through Poisson's equation, is a reasonable assumption to make (22, 23). In reality, doping introduces discrete ions which create potential fluctuations because of their random distribution. Increased doping densities exacerbate this effect, to the extend that it can dominate over other sources of potential fluctuations, like interface charges. The impact of random dopant fluctuation is exhibited through large V_{th} variation. As shown through simulation in (21), in deeply-scaled bulk CMOS devices, RDF proves to be the most dominant component of variation. Reducing or removing the doping from the channel, as done in PDSOI and FDSOI devices respectively, can reduce the threshold variation due to RDF. However in this case the threshold voltage must be set by the gate-metal workfunction or by a separately biased back gate. In FDSOI devices with a thin BOX ground plane doping may be used in order to maintain channel control through back-gate biasing. In that case, RDF

in the GP may cause threshold voltage fluctuations as well. Also, since the source and drain regions in FDSOI are formed by diffusing dopants towards the channel, RDF in the S/D may also contribute to variations in the effective channel length.

3.2.2 Line edge roughness

Line edge roughness is another significant contributor to variability, and is caused by statistical variation in the incident photon count during lithography exposure, as well as the absorption rate, chemical reactivity and molecular composition of the photoresist (20, 24). Atomic-scale behavior of the manufacturing process creates missing chunks of atoms from the surface of the gate along the width, giving rise to edge roughness, which does not scale with length scaling. The result is variability in the effective channel length, which, in turn, causes increased threshold variability. The $\sigma_{V_{th}}$ due to LER has been shown to be proportional to $\frac{1}{\sqrt{W_{eff}}}$ through device simulation (24). In bulk CMOS, LER has not been the dominant contributor comparing with the atomistic doping effect. In modern PDSOI or FDSOI processes, though, the RDF component can be significantly reduced or even effectively eliminated, making LER along with other sources of variation increasingly important.

3.2.3 Surface roughness

Another source of intrinsic device variability arises from atomic-scale oxide thickness variations. CMOS scaling involves aggressive reduction in the physical gate oxide thickness, which is currently limited to approximately 1nm, or 5 atomic layers of SiO_2, because of the exponential increase in leakage current arising from quantum mechanical tunneling across the thin gate dielectric. With an oxide thickness variation of one or two atomic spacings (20), significant variation is introduced to several device parame-

ters, like mobility, gate tunneling current and threshold voltage. Device simulations including oxide thickness variation have shown that the $\sigma_{V_{th}}$ due to T_{ox} variation depends linearly on the correlation length Λ, when device dimensions are much larger than Λ, as well as the device geometry. This dependence is expressed by the relationship $\sigma_{V_{th}} \propto \frac{\Lambda}{\sqrt{W_{eff}L_{eff}}}$ (25). As a result, for devices with channel length below 30nm, the threshold voltage fluctuations induced by the Si/SiO_2 and $gate/SiO_2$ roughness can become comparable to the fluctuations induced by random discrete dopants. In thin-body devices, there is additional surface roughness in the buried-oxide layer, which causes silicon film thickness variations. As silicon film thickness scales down to 7nm and below to ensure better channel control (26) , T_{Si} variation becomes more and more significant.

3.2.4 Strain and stress

Starting with the 90nm technology generation, strained Si has been employed in order to enhance the mobility of carriers, and thus the drive strength of CMOS devices. This mobility enhancement is achieved by reducing the conductivity effective mass and scattering rate of the carriers, and typically affects electrons more than holes since valence band splitting is smaller than that for the conduction band, as explained in (27).

The impact of strain on transistors depends on the crystal orientation, the type of strain and the direction of strain. The crystal orientation can be either $< 100 >$ or $< 110 >$. The traditional substrate orientation is $< 100 >$, and $< 110 >$ enhances PMOS mobility and weakly affects NMOS devices, comparing to the traditional case. The interaction of surface orientation and different types of strain or stress gives different combinations of results. The different types of strain are either compressive or tensile, with respect to their effect on the channel, as shown in figure 3.1. In the $< 110 >$ orientation tensile strain increases NMOS mobility, while compressive strain increases

PMOS mobility (28). Finally, strain can be either uniaxial or biaxial, depending on if it has one direction, either parallel or perpendicular to the current flow, or two directions (both parallel and perpendicular), respectively. Threshold voltage has been shown to be more sensitive to biaxial strain than uniaxial (29).

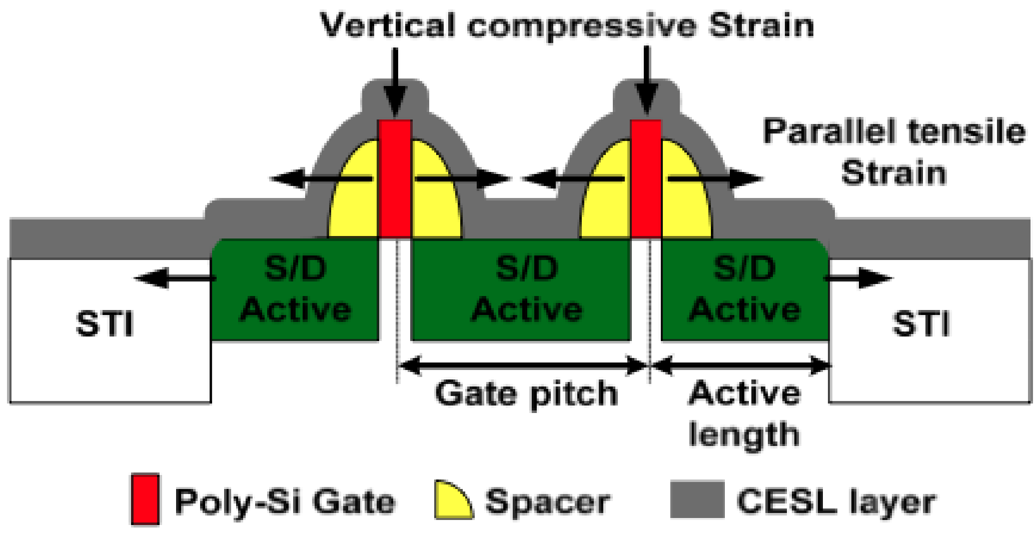

Figure 3.1: Stress and strain on CMOS devices (30)

There are multiple ways to apply strain to a device in order to improve performance, and they typically follow two basic approaches: a global approach, where stress is introduced across the entire substrate, and a local approach, where stress is engineered into the specific device (27). The global approach can include a thin Si layer on top of a thick $SiGe$ substrate. Regarding the more local approaches, shallow trench isolation (STI) is typically used to electrically isolate neighboring devices, but also creates compressive stress on the channel that is inversely proportional to the distance of the edge of the STI to the channel region. This distance, and thus the amount of stress, varies due to the manufacturing process, and its effect is systematic and has been identified and modeled. STI can also result to random variation due to surface roughness of the $SiO_2/diffusion$ interface, but this has not yet been shown to be a dominant effect on threshold voltage variation. Strain can also be applied to the channel by the use of

silicide layers or the contact etch-stop layer (CESL). Silicide layers deposited onto the active and poly-Si region of the transistor introduce compressive strain on the channel, as depicted in Figure 3.1. In the case of CESL, nitride capping layers are used to induce tensile and/or compressive strain on the channel. Finally, a local epitaxial film can be grown on the source and drain regions of the transistor, introducing uniaxial tensile or compressive stress into the Si channel. In both cases, the mobility boosters used cause both systematic and random variation of the threshold voltage. In FDSOI, a major concern is that the use of S/D implantation is no longer available because of the extremely thin body. However, successful integration of $Si : C$ and $Si : Ge$ implants, for NFETs and PFETs respectively, has been demonstrated in (31).

3.3 Effects of variability on circuits

Variability affects the yield of integrated circuits, which is inversely proportional to the cost. Yield is defined as the probability that a chip is both functional and meets the required specifications, like speed and power. Defining the maximum allowable timing or power margin for a certain yield is essential for determining the optimal point in terms of cost and performance of a circuit, which in turn is directly related to a company's overall revenue. An overestimation of the margin can increase the design complexity and time, while an underestimation can compromise the yield. Consequently, characterizing variability in a more detailed way can help improve all aspects of circuit design, including digital logic, memory and analog circuits.

So far, systematic variations and their effect on circuits have been extensively characterized (30, 32, 33, 34). In (32) it is demonstrated that the magnitude of both die-to-die and within-die parameter fluctuations influence a processor's maximum clock frequency distribution. It is also shown that the mean delay increases and the standard deviation decreases as the number of uncorrelated critical paths increases. Further

analysis of the spatial correlation of path delays can allow for more accurate statistical timing analysis (33). In (34) the problem of noise margin degradation in SRAM arrays due to increased process variability is addressed. Since variability degrades SRAM V_{min}, SRAM yield is compromised, especially in the case of low-voltage operation. Given these facts, variability-aware circuit design becomes a necessity for low power, robust design in deeply scaled technology nodes.

In a conventional circuit design process, variability is accounted for through process corners, which correspond to worst case conditions, by performing deterministic shifts in several design parameters. This conventional corner modeling has two major disadvantages. Firstly, since the circuit is designed to function under worst-case conditions, overdesigning is inevitable. All devices on chip are modeled as having identical process parameters, and the design margin is increased in order to cope with worst-case scenarios. Secondly, all variation is modeled as die to die variation, regardless of the true complexity of process variability (spatial/deterministic/random - WID/D2D/W2W/L2L). As a result, process parameter variability cannot be adequately captured, and yield cannot be accurately predicted.

3.4 Conclusion

In this chapter, variability was identified as a complex entity, with multiple sources either known and well-understood, or barely understood - or even unknown. It was also shown that variability compromises the yield of a chip, resulting in increased cost. Given the above, characterizing variability and classifying different sources of variation as systematic and random in a state-of-the-art technology can help the design process and make it more cost-effective. A set of test structures designed in a state-of-the-art 22nm FDSOI technology will be presented in Chapter 4.

3. SYSTEMATIC AND RANDOM VARIABILITY

4

Test structures

As discussed in Chapter 2, FDSOI seems to be a promising candidate for circuit design due to its potential for low variability and excellent electrostatic integrity. Consequently, there is increased interest in research in order to verify those benefits not only on the device level, but also on the circuit level. In this work, a testchip was designed in a state-of-the-art 22/16nm FDSOI technology. The goal of the testchip is to evaluate random and systematic variability at an early stage of the manufacturing process, as well as characterize performance of ring oscillators, SRAM and DRAM.

Figure 4.1 provides a quick reference of all the variations targeted by this work and the corresponding test structures and measurement procedures. In this chapter, the experiments deployed by the aforementioned testchip will be discussed and analyzed.

4.1 Technology and testchip overview

The testchip was designed in a device-oriented, fully depleted silicon on insulator process, manufactured by CEA-LETI. The devices are printed on $300mm$ wafers, using

Variation	Effect		Structure	Procedure
Random	LER		Transistor arrays with varying WL (Table 4.1)	Pelgrom plots for V_{DS}=1V and V_{DS}=50mV, low temperature measurements across all tiles
	Tsi		Transistor arrays with varying WL (Table 4.1)	Pelgrom plots for V_{DS}=1V and V_{DS}=50mV, low temperature measurements across all tiles
	RDF	S/D	Transistor arrays with varying WL (Table 4.1)	Room temperature measurements, compare with previous
		GP	Transistor arrays with varying WL (Table 4.1) and 3 GP options	Room temperature measurements, compare various GP options
Systematic	Back-biasing		Transistor arrays with 3 GP options	Measure across die (WID) and average over dies across a wafer (D2D)
	STI		Fixed W,L transistors with varying vertical and horizontal STI	Measure across die (WID) and average over dies across a wafer (D2D)
	LOD		Fixed W,L transistors with varying LOD	Measure across die (WID) and average over dies across a wafer (D2D)
	Stack and switching order		ROs with various inverter patterns (Figure 4.21)	Measure across die (WID) and average over dies across a wafer (D2D)

Figure 4.1: Summary of targeted effects and test structures

$193nm$ lithography with OPC, and e-beam in a limited number of wafers. The target gate-length is $\leq 22nm$ for logic and 22/16nm for memory, while a 2-metal layer 65nm technology is used for the back-end. For the buried oxide, a thick BOX option is used as a baseline, while wafers with ultra-thin BOX (25nm and 10nm) as well as ground plane doping will also be manufactured. A few more process details include raised and faceted S/D, single epitaxial growth of doped $SiGe$ for both NMOS and PMOS, STI, ion implantation and, finally, CESL on selected wafers.

The designed testchip includes several different experiments, as shown in the layout picture in Figure 4.2. First of all, there is a large test array that consists of 11×11 tiles. Each tile includes four different types of test structures, shown in Figure 4.3:

1. I-V measurement structures, for both NMOS and PMOS
2. C-V measurement structures

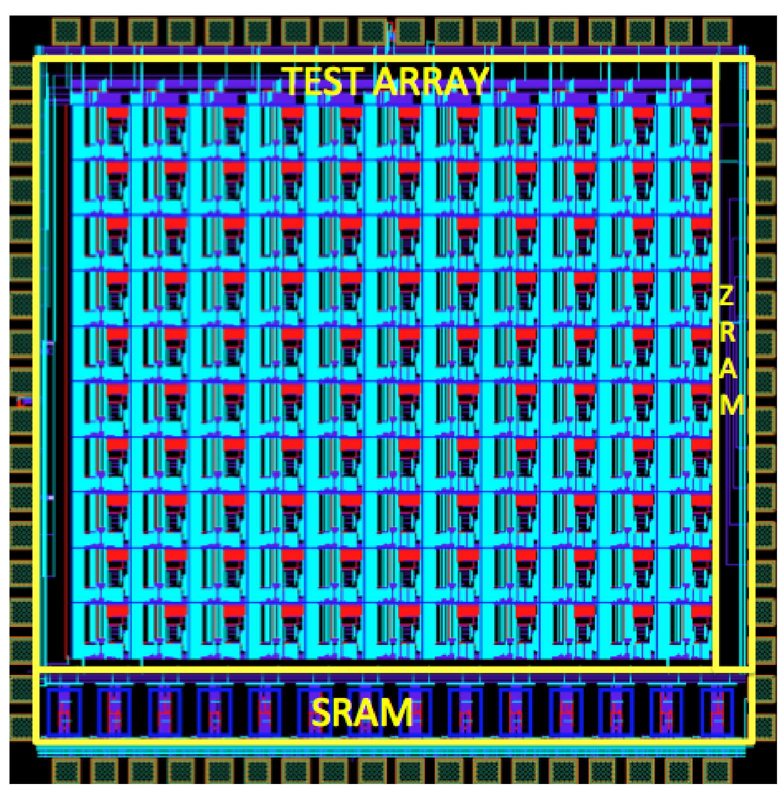

Figure 4.2: Layout picture of the testchip

3. Resistance measurement structures

4. Ring oscillators

Secondly, the chip includes 14 SRAM macros for noise margin characterization [1], and, finally, a few cells of capacitorless DRAM (also known as ZRAM) [2]. The main focus of this thesis will be the variability characterization array, more details of which will be discussed in the rest of this Chapter.

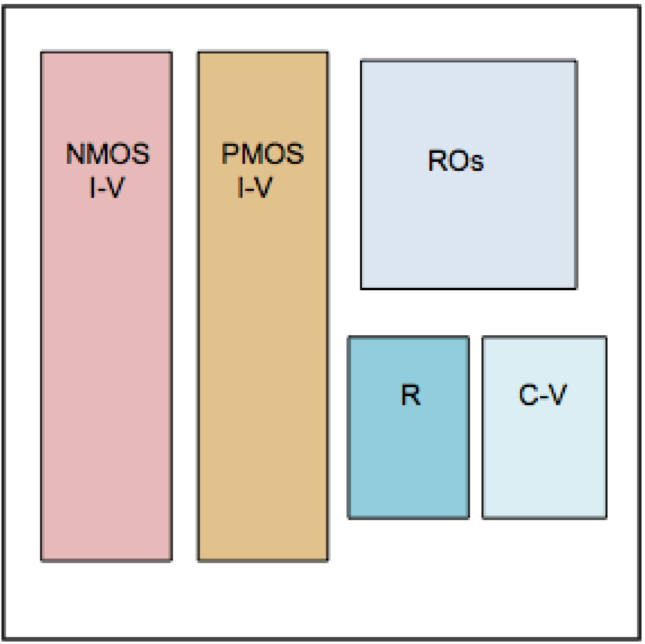

Figure 4.3: Floorplan of one tile of the test array

[1] designed by Seng Oon Toh and Nattapol Damrongplasit, at University of California in Berkeley
[2] designed by Min Hee Cho, at University of California in Berkeley

4.2 Test structures

As discussed in the previous paragraph, a dense array of test structures was used for variability characterization, similar to the one described in (35). The primary reason for employing such an array is that it provides a large amount of devices-under-test (DUTs), thus making accurate statistical analysis possible. Moreover, the array, in combination with row/column decoders, helps overcome the problem of limited pad number. Finally, it enables statistical analysis with both low and high spatial resolution and reduces design time due to its repetitive nature. The test structures included in the array, shown in Figure 4.4, will be discussed in detail in the next paragraphs.

Type	Structures	Procedure details	Targeted results
IV		• 121 devices x 24 W/L combinations per chip • 3 GP options • Low temperature • WID random variation	• Measurement of LER and Tsi, decoupled from other sources of variation. • Effect of GP on random variation
	NO WELL NWELL PWELL	• 121 test devices per chip • D2D and WID variation	• Systematic variation due to back-biasing • Spatial characteristics of variation
		• 121 test devices per chip • D2D and WID variation	• Systematic effects of LOD and STI • Spatial characteristics of variation
CV		• 121 devices x 5 sizes per chip • D2D variation	• Spatial characteristics of variation • Model parameter extraction
ROs		• 121 ROs x 8 inverter patterns per chip • D2D and WID variation	• Stack and switching order effects on systematic variation • Spatial characteristics of variation
Res		• 121 resistors x 2 types per chip • D2D variation	• Spatial characteristics of variation • Model parameter extraction

Figure 4.4: Summary of all the test structures

4.2.1 I-V measurement structures

In this testchip, transistor arrays are used in order to explore mismatch, layout-dependent effects and back-biasing effects. Extraction of device I-V curves is crucial for variability characterization, since it provides important information, like V_{th}, I_{ON} and I_{OFF}. The Figures 4.5 and 4.6 show the $I_D - V_{GS}$ curves generated by Monte Carlo simulation for an NMOS transistor of 30nm and 90nm length, respectively. In both cases, the drain-to-source voltage is set to a full V_{DD} (1V) and V_{GS} is swept from 0 to V_{DD}. The black curve represents the nominal case. From the plots, it is evident that variability at smaller geometries is significantly greater. In order to be able to fully characterize systematic and random variability, multiple devices of multiple geometries are required.

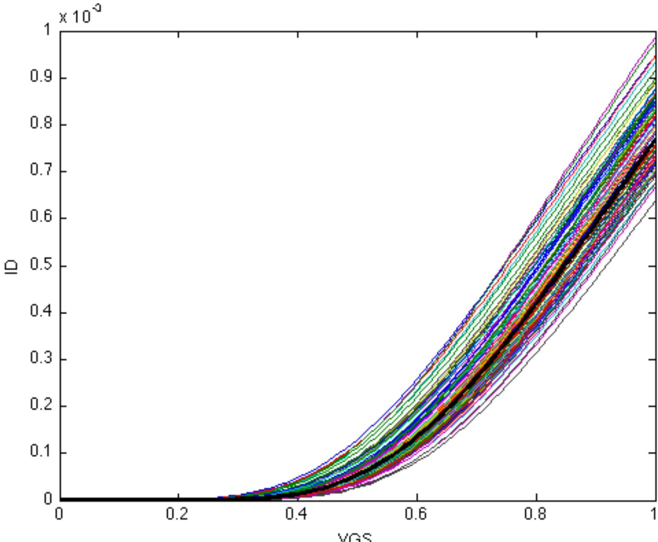

Figure 4.5: Simulated I_D-V_{GS} curves of a 30nm length transistor with $V_{DS} = 1V$

4.2.1.1 Decoupling sources of random variability

Table 4.1 shows the different device sizes used in order to extract random variability statistics. Measuring the IV curves for devices with various channel areas helps de-

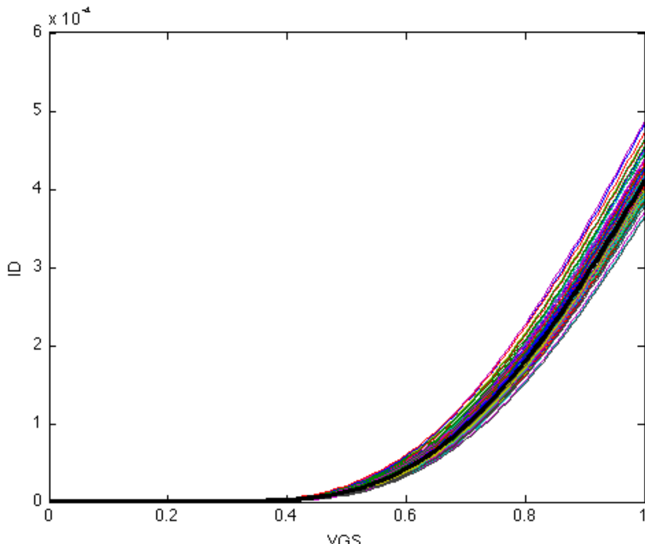

Figure 4.6: Simulated I_D-V_{GS} curves of a 90nm length transistor with $V_{DS} = 1V$

termine the Pelgrom coefficient for this technology. According to (36), the Pelgrom coefficient for a parameter P can be given by the equation:

$$\sigma_P{}^2 \approx \frac{A_P{}^2}{WL} \tag{4.1}$$

However this approximation is based on the square law transistor current model and becomes less and less valid at smaller device geometries. Figure 4.7 shows the Pelgrom plots generated by 100 Monte Carlo simulations for two different transistor channel lengths. The threshold voltage V_{th} was extracted from the $I_D - V_{GS}$ curve, and is defined by the constant current criterion as the gate-source voltage at $I_D = 10^{-7}\frac{W}{L}$. The data points were then fitted to a linear curve, the slope of which is considered to be the Pelgrom coefficient A_{Vth}. Note that the annotated values are $A_{\Delta Vth}$, which denotes the threshold difference between a pair of devices and differs from A_{Vth} by a factor of $\sqrt{2}$:

$$A_{\Delta Vth} = \sqrt{2}A_{Vth}$$

Table 4.1: Transistor sizes used in the testchip and colormap of the corresponding channel area in nm^2

Width \ Length	30nm	60nm	120nm	240nm	480nm	960nm
150nm	4500	9000	18000	36000	72000	144000
300nm	9000	18000	36000	72000	144000	288000
600nm	18000	36000	72000	144000	288000	576000
1200nm	36000	72000	144000	288000	576000	1152000

As shown in Figure 4.7, the linear fit is worse in the L=30nm case. More specifically, the root-mean-square error of the fit at 120nm is 3 times less than at 30nm, and can be expected to be even less at larger lengths, in accordance to (36). From the above, it is obvious that mismatch in deeply scaled devices is not as straightforward as predicted by Equation (4.1) and requires further investigation.

One approach for dealing with random variability, as the complex entity that it is, is to divide the variability sources in long-channel and short-channel sources (26). The long-channel are those sources that follow Equation 4.1. The short-channel sources on the other hand are related to short-channel effects that cannot be accurately captured by long-channel models, and have much more unpredictable behavior. This is due to the fact that the correlation lengths become comparable to device dimensions. In order to evaluate those, one can extract Pelgrom plots at high and low V_{DS} voltages, e.g. at $V_{DS} = 1V$ and $V_{DS} = 50mV$ (when the nominal supply is 1V), as shown in 4.8 [1]. Here only three sources of variation are considered, LER, T_{Si} and RDF, which are expected to be the most dominant short-channel sources. Threshold voltage variation is larger when short-channel effects are more prominent. The difference between the variances at each point of the Pelgrom plot in Figure 4.8 can be defined as the threshold voltage variance due to short-channel effects (Equation 4.2).

$$\sigma_{V_{th},SCE}{}^2 = \sigma_{V_{th},1V}{}^2 - \sigma_{V_{th},50mV}{}^2 \tag{4.2}$$

[1]Device simulation performed with Changhwan Shin at UC Berkeley.

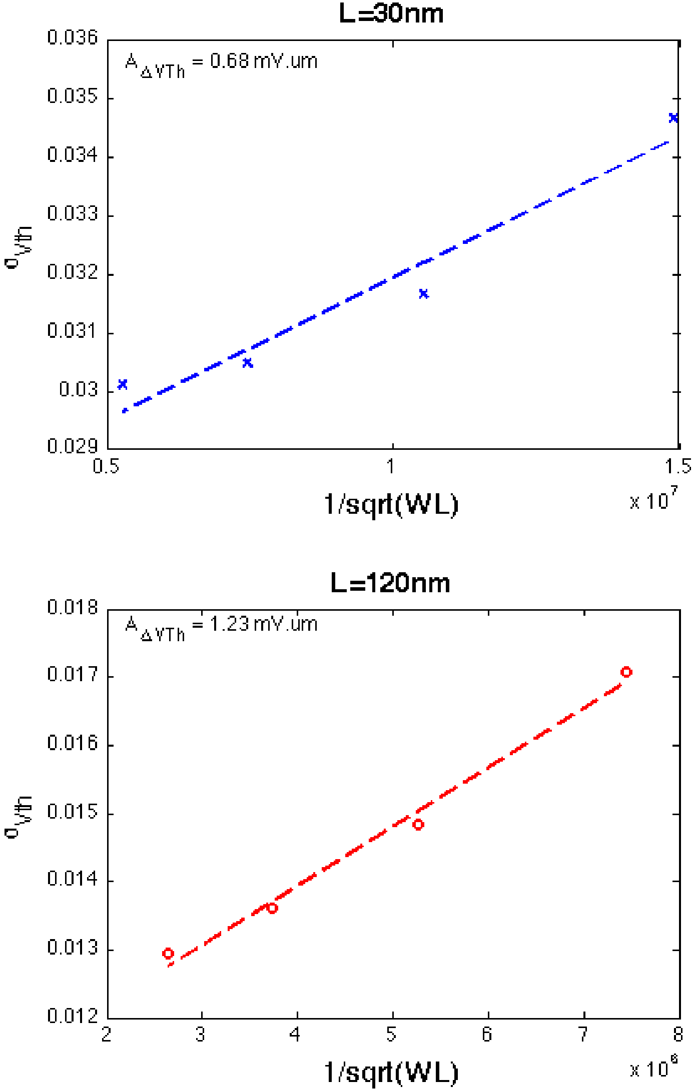

Figure 4.7: Simulated Pelgrom plots for the L=30nm and L=120nm cases of Table 4.1

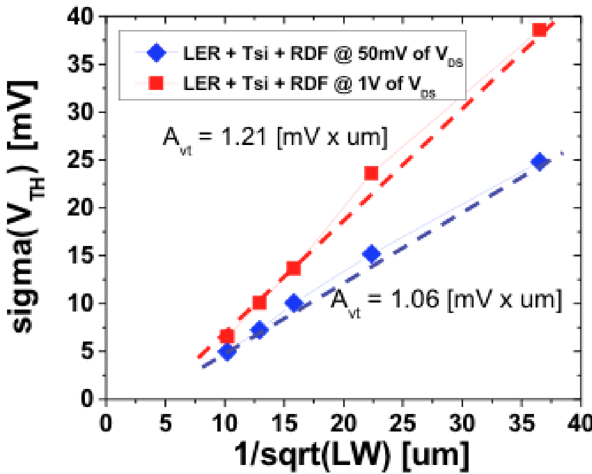

Figure 4.8: Pelgrom plots extracted from device simulation for $V_{DS} = 1V$ and $V_{DS} = 50mV$

Evaluating the amount of variation contributed by each individual source is merely impossible; simplifications are required. The argument made is that LER and silicon thickness variation are or can be made (by approximation) the dominant sources of variation. This argument is rather straightforward for LER in a 22nm node, since LER doesn't scale. Also, as analyzed in Chapter 2, random dopant fluctuation in FDSOI comes from the source and drain doping only, and should be negligible comparing to LER and T_{Si} variation at short lengths. In Figure 4.9, it is shown that LER/T_{Si} variation is more dominant in shorter devices. In longer devices however, since LER is less significant due to averaging, the effect of RDF cannot be considered negligible. Consequently, low-temperature IV measurements are necessary in order to deactivate the dopant atoms and enable decoupling RDF from LER/T_{Si}.

Naturally, $\sigma_{V_{th},SCE}$ can be affected by numerous other sources, like narrow width effect (NWE) and mobility variation due to strain and stress. In this testchip, larger widths can help eliminate NWE, and the used of a fixed and large length of diffusion can make any random component of threshold variation due to STI negligible. Since

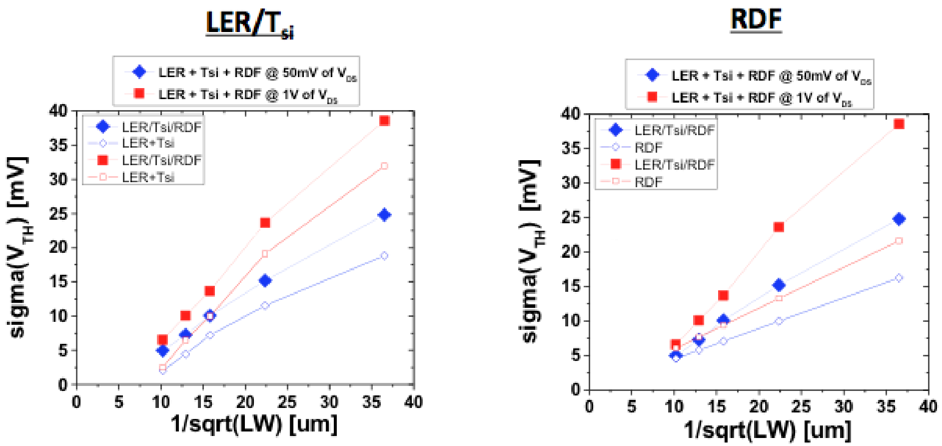

Figure 4.9: Comparison of the effects of LER/T_{Si} and RDF through Pelgrom plots extracted from device simulation for $V_{DS} = 1V$ and $V_{DS} = 50mV$

wafers without strain boosters are available, random mobility variation due to strain and its effect on $\sigma_{V_{th},SCE}$ can be ignored. As a result, $\sigma_{V_{th},SCE}$ can be approximated by the expression in Equation 4.3, under the assumptions that the random variability sources are independent and that the variations in L and T_{Si} are small enough so that the threshold voltage can be approximated as a linear function. From here, the sensitivities to L and T_{Si} can be determined from electrical measurements and from TEM transistor images, respectively, such that an estimate of $\sigma_{V_{th},LER}$ and $\sigma_{V_{th},T_{Si}}$ can be extracted. Figure 4.10 shows the estimated and simulated Pelgrom plots. The proportionality factor in Equation 4.3 was found to be ~ 1.1 and the errors in the estimated $\sigma_{V_{th},LER}$ and $\sigma_{V_{th},T_{Si}}$ were found to be 5% and and 1%, respectively.

$$\sigma_{V_{th},SCE}{}^{2} \propto \left(\frac{\partial V_{th}}{\partial L}\right)^{2} \sigma^{2}_{V_{th},LER} + \left(\frac{\partial V_{th}}{\partial T_{Si}}\right)^{2} \sigma^{2}_{V_{th},T_{Si}} \tag{4.3}$$

In order to be able to do the above analysis, multiple transistor sizes and flavors were taped-out (Table 4.1). Figure 4.11 shows the layout patterns that were used in the transistor arrays. Figure 4.12 shows the measurement setup that was used. All devices under test (DUTs) were connected in parallel to each other, sharing the same

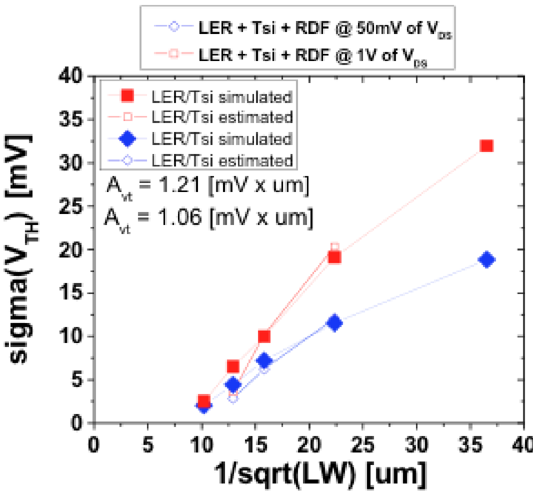

Figure 4.10: Comparison of estimated and simulated $\sigma_{V_{th},SCE}$

gate, source, drain and body buses, as on (35). During measurement, only one of the devices is enabled, through the enable signal which activates a pass-gate switch that connects the gate bus G, to the actual DUT gate. All other devices are disabled and their gates are driven to a voltage Vgx.

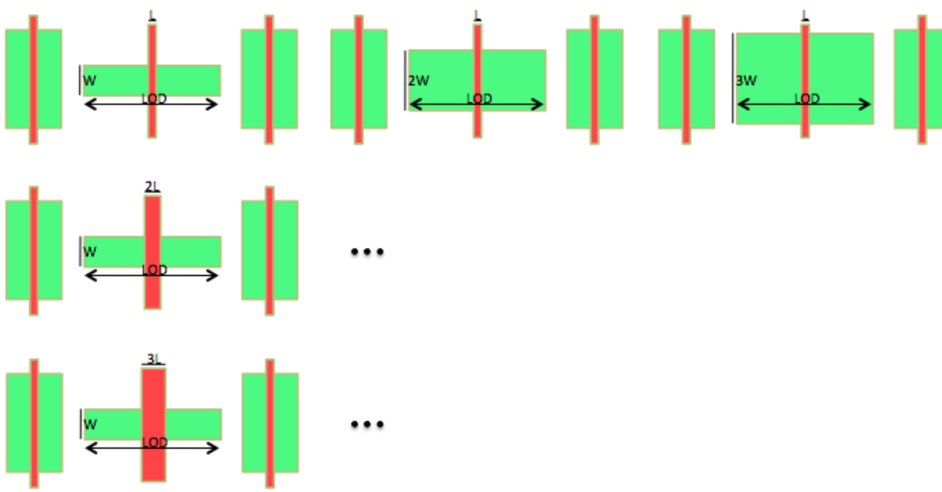

Figure 4.11: Illustration of device layouts in the transistor array

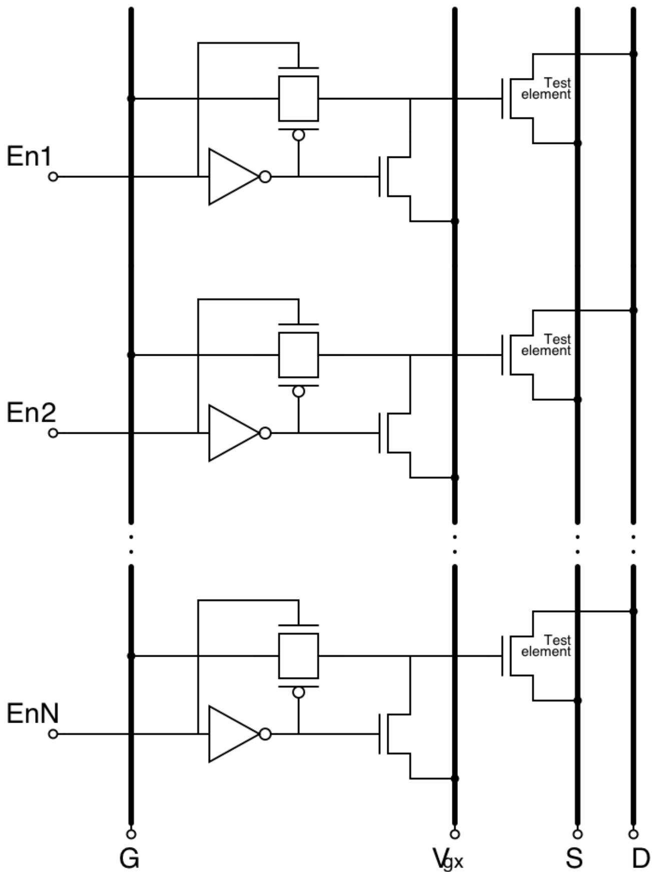

Figure 4.12: Schematic of measurement setup for I-V extraction

4.2.1.2 Characterization of back-biasing effects

In addition to random mismatch, this work aims to explore the systematic effect on variability between different devices, layouts and under different back-bias conditions. Specifically in FDSOI, the addition of a ground plane enables V_{th} modulation, but may also add variability due to RDF in the GP doping or buried oxide thickness variation. In order to include NMOS and PMOS devices and different GP options, the schematic was modified as shown in Figure 4.13, such that each device size is available in three possible ground plane doping options: P-well, N-well and no well. During measurement, all 3 types are enabled and can be measured simultaneously. This measurement will allow characterization of variability that is related to the back-bias. Also, this setup can potentially reveal information about random telegraph noise (RTN) in FDSOI.

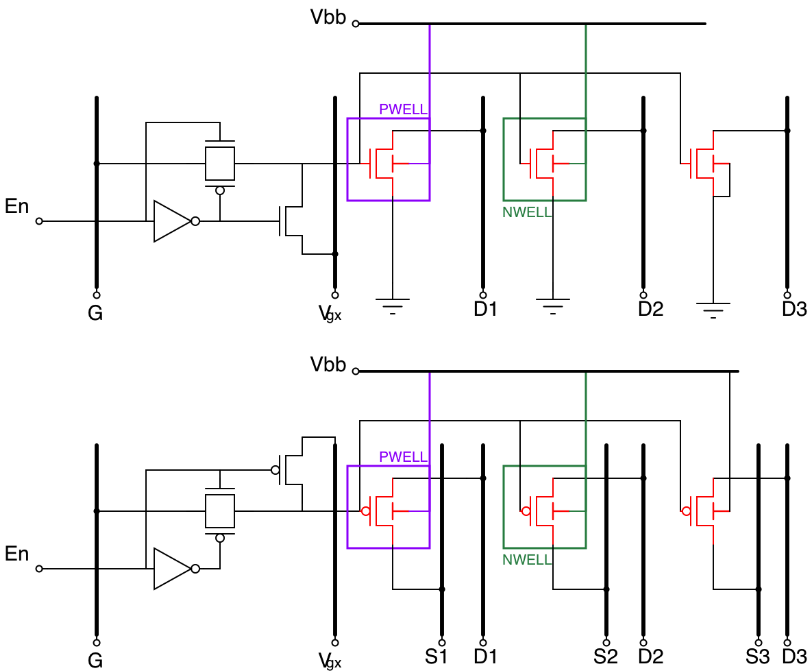

Figure 4.13: Schematic of measurement setup for I-V extraction of NMOS (top) and PMOS (bottom) devices

4.2.1.3 Characterization of stress and strain effects

Finally, in order to capture systematic variability due to stress in the channel, a few different layout options were taped out for some of the aforementioned devices. More specifically, the layouts shown in Figures 4.14 and 4.15 were used in order to characterize effects related to horizontal and vertical STI stress, and length of diffusion (LOD) induced stress, respectively.

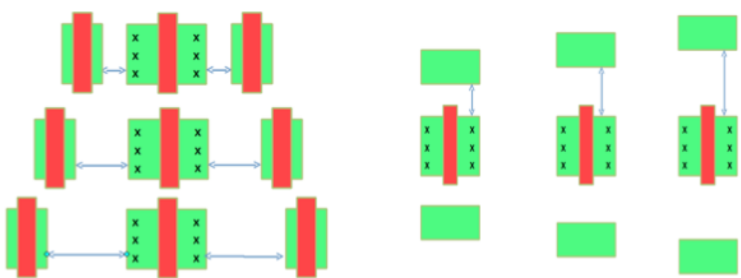

Figure 4.14: Layout for characterization of horizontal and vertical STI effects

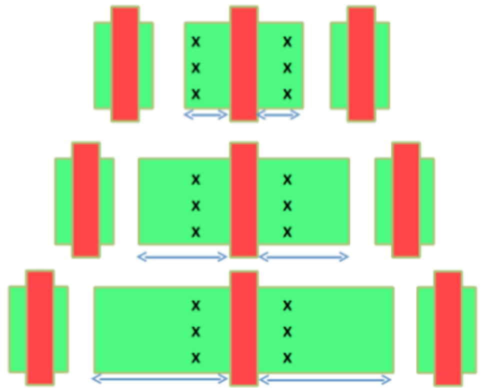

Figure 4.15: Layout for characterization of LOD effects

4.2.2 C-V measurement structures

Extraction of C-V characteristics of a device is a powerful tool for characterizing semiconductor material and techniques. C-V measurement can reveal information about the variability in oxide thickness and oxide charges, the doping profile as well as other details of the manufacturing process. Furthermore, capacitance characterization reveals

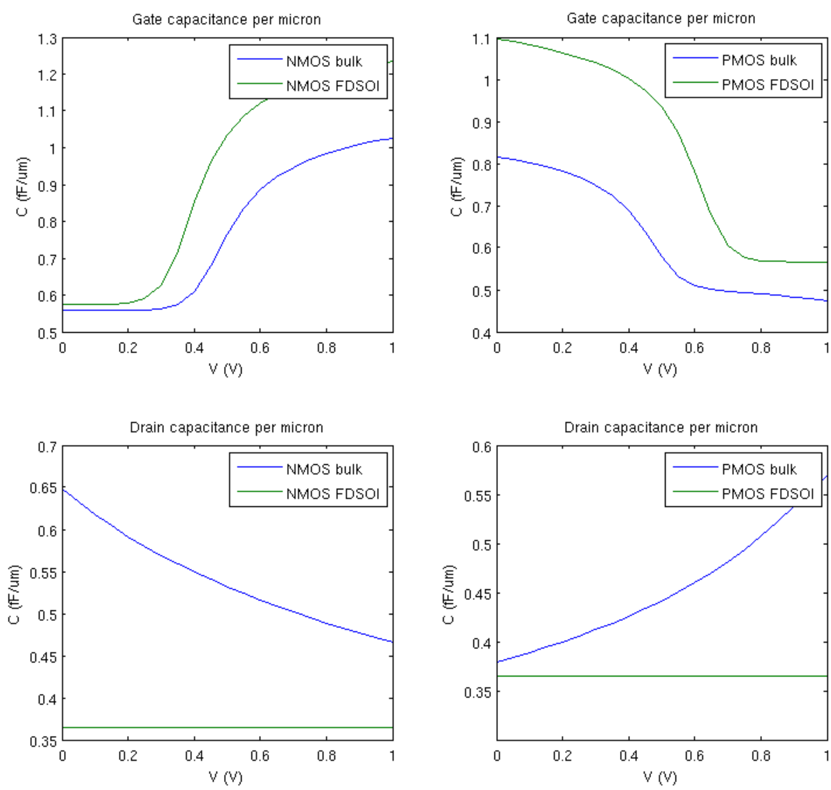

Figure 4.16: Gate and drain capacitances per μm in bulk and FDSOI NMOS/PMOS

information about technological differences between bulk and FDSOI. In the example curves shown in Figure 4.16, it is obvious that FDSOI gate capacitance has sharper slopes due to the decreased body doping, while FDSOI drain capacitance shows no dependence on voltage (relative to bulk), since it consists of the capacitance of the buried oxide. It is also evident that the plots were extracted from a thick BOX device; if very

thin BOX is used instead it is expected that there will be some dependence on voltage, since a depletion region can be created below the BOX. On the other hand, bulk drain capacitance is highly dependent on voltage because it is essentially a junction capacitance.

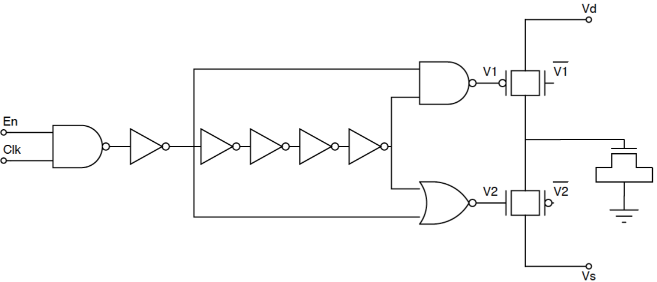

Figure 4.17: Gate capacitance measurement setup

When direct device probing is not available, MOS capacitance can be difficult to measure. In this testchip, the charge-based capacitance measurement method was employed (37). The method as well as the non-overlapping clock generation schematic are shown in Figure 4.17. The device on the right is the DUT. Along with DUTs of various sizes, in each tile there is a measurement structure without any DUT connected, which serves as the reference. Charge injections errors are mitigated both by the

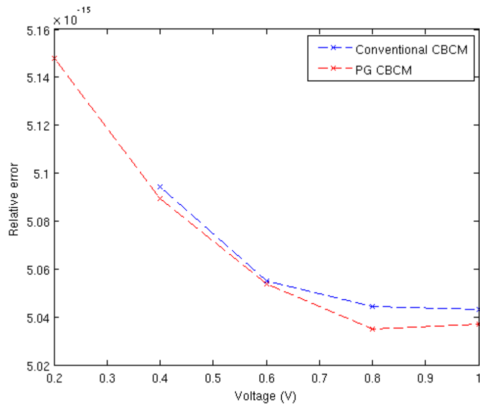

Figure 4.18: Simulated relative error in measured capacitance comparison between a conventional and a pass-gate implementation of CBCM

subtracting the reference current from the DUT current and by the use of pass-gate switches (Figure 4.18).

In each DUT test, the average current going through V_d to V_s is measured. The capacitance extracted is not only the DUT capacitance but also the parasitic capacitance of the switches and the charge injection ”capacitance”, as shown in Equation 4.4. The procedure for extracting the actual DUT capacitance is outlined below:

$$I_{TOT,avg} = \frac{(C_{DUT}(Vd) + C_{par} + C_{C.I.}) \cdot Vd}{T_{CLK}} \tag{4.4}$$

$$I_{REF,avg} = \frac{(C_{par} + C_{C.I.}) \cdot Vd}{T_{CLK}} \tag{4.5}$$

Thus:

$$I_{DUT,avg} = I_{TOT,avg} - I_{REF,avg} = \frac{C_{DUT}(Vd) \cdot Vd}{T_{CLK}} \Rightarrow$$

$$C_{DUT}(Vd) = \frac{T_{CLK} \cdot I_{DUT,avg}}{V_d} \tag{4.6}$$

Equation 4.6 shows that the accuracy of the method strongly depends on the frequency of the clock. If the clock frequency is too low, the average current becomes too small, especially for low V_d (Figure 4.19). The simulated C-V curves in Figure 4.20 do not reveal any major discrepancies. However, in practice the current measurement equipment resolution is limited and the average current curve for $f = 5MHz$ will not be as accurate as for $f = 50Mz$. If the clock frequency is too high, there may not be enough time for the capacitor to fully charge and discharge, thus the technique fails. In our case the upper frequency limit is limited by the pad specifications to $\sim 10MHz$. Additionally, the clock rise and fall times need to be small enough to avoid short-circuit

current. Since the pass-gates are kept at minimum size to reduce parasitic capacitance and charge injection, the clock slope is adequately sharp.

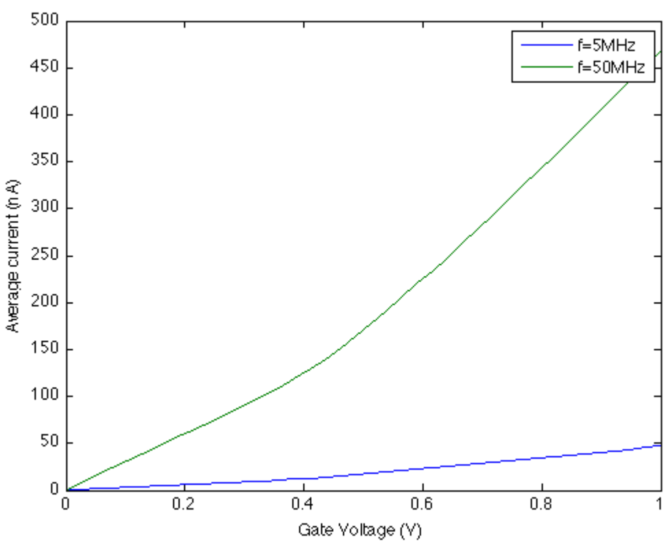

Figure 4.19: Simulated average current measured with CBCM for two different clock frequencies

4.2.3 Ring oscillators

As discussed in Chapter 2, FDSOI exhibits better electrostatic integrity than bulk, and thus lower DIBL. If we compare the $I_D - V_{DS}$ characteristics of two devices with the same I_{ON} and I_{OFF} in two different technologies, the technology which has lower DIBL will yield higher current at the linear region. The switching speed (or in other words, the effective current I_{eff}) of an inverter depends not only on the saturation current but also on the linear current through the transistors. Consequently, a technology with lower DIBL, like FDSOI, can yield higher effective current and faster switching logic.

One can argue that speed may not be improved due to higher gate capacitances in FDSOI (Figure 4.16). However, logic does not consist only of inverters, but also in-

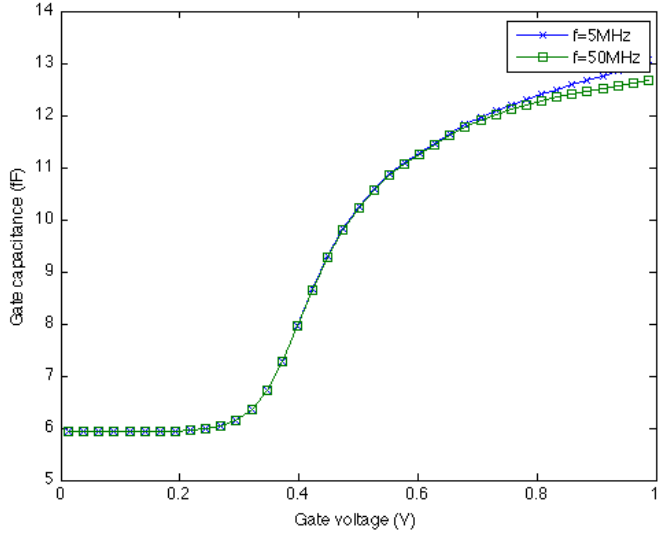

Figure 4.20: Simulated C-V characteristic extracted with CBCM for two different clock frequencies

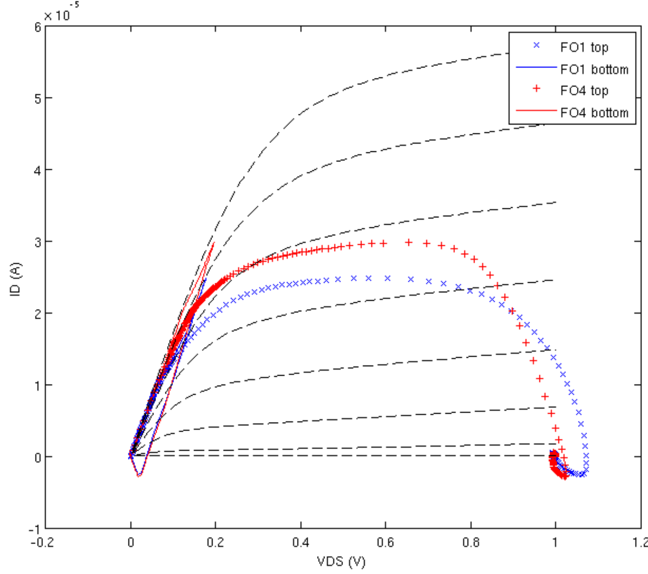

Figure 4.21: Simulated current trajectories of an inverter with a 2-NMOS stack

cludes complex gates like NANDs and NORs, which typically include stacks of transistors. Transistor stacks slow down the logic, since the effective current becomes more and more dependent on the linear current, as the stack grows. As shown in Figure 4.21, the bottom devices of an NMOS stack never really leave the linear region, thus limiting the effective current through the stack. Given this fact, a technology with larger linear current may indeed be very beneficial for high speed logic.

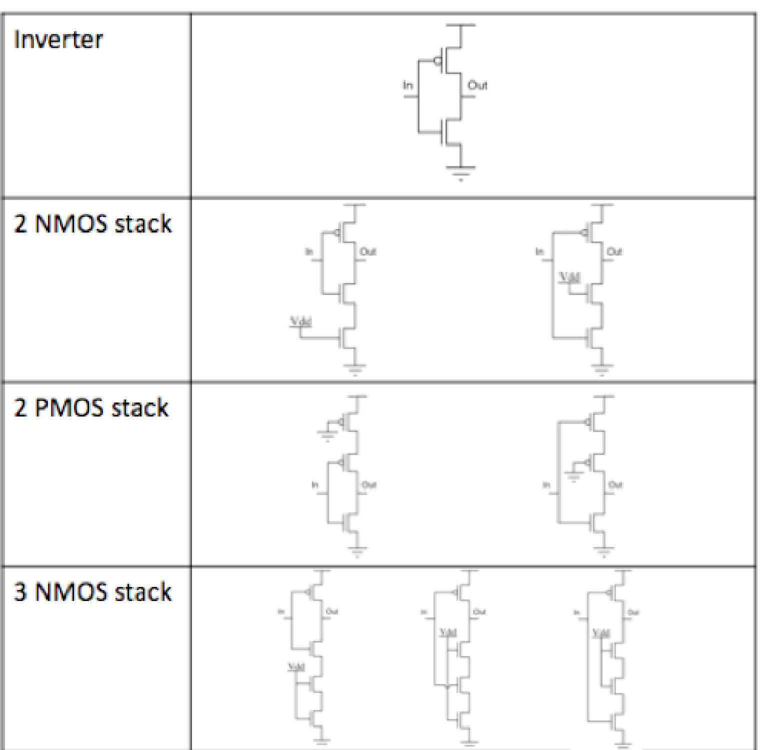

Figure 4.22: Inverter patterns used in the ring oscillators

In order to explore the speed advantages of FDSOI as well as the variation in logic speed, ring oscillators with various inverter patterns were taped-out (Figure 4.22). The reference is a ring oscillator that consists of a regular inverter. Stack and switching order effects are then explored by the use of 2 and 3 transistor stacks, and all possible input options. The output frequency was simulated to be $\sim 5GHz$, and thus was

divided down to $< 10MHz$, which is the pad specification. The various ring oscillators form an array inside of each tile, and are repeated in 11×11 tiles throughout the chip, thus allowing for circuit-topology induced variation and spatial correlation characterization.

4.2.4 Resistors

The final experiment in the characterization array included in the testchip is measurement of undoped body and higk-K metal gate resistors. Undoped body resistor measurements can reveal variation in the body and source/drain doping, while gate resistors provide information on the metal resistivity variation. Such information is useful not only for circuit yield evaluation but also for model parameter extraction.

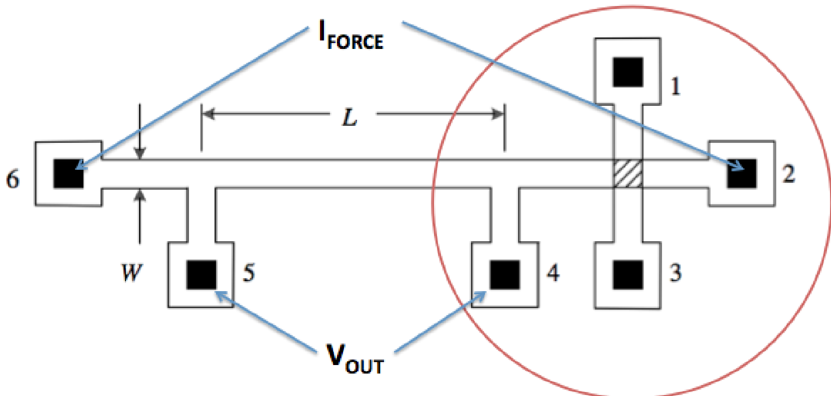

Figure 4.23: Resistance and sheet resistivity measurement setup

Figure 4.23 shows the measurement setup used in this testchip. Kelvin sensing is used in order to improve line resistance measurement accuracy by decoupling the wire resistance from the DUT resistance. A similar force-and-sense structure, known as the Greek cross, is used for sheet resistivity measurements. The two structures are combined into one, as shown in the figure.

5

Conclusion

A testchip for measurement and analysis of variability in a 22nm FDSOI process has been designed. Devices of various types and flavors can be measured through the use of a dense array of 11x11 tiles. Each tile contains circuits to measure IV and CV device characteristics, RO frequencies and resistor values. The dense array is addressed by scan chains, and provides a compact and efficient way for variability data extraction with low pad count.

The goal of this testchip is to characterize variability in a new, deeply scaled technology. This will be achieved by extracting systematic variation data and quantifying their spatial characteristics, similarly to the work done for bulk CMOS techologies in (28). In addition, this work focuses on characterizing sources of variation that are specific to the FDSOI technology. Electrical measurement of the silicon thickness variation can be achieved through IV curves extracted from specially designed structures. Low-temperature measurements are employed to decouple the effect of S/D RDF from other sources of variation. Source and drain RDF is characterized separately with the use of undoped body resistors. Finally, the effects of RDF in the ground plane and of

buried oxide thickness variation are addressed through transistor arrays with various back-biasing options.

If successful, this testchip can contribute to improvements in the circuit design process. Understanding variability and its sources can lead to process optimizations to reduce or remove systematic effects. Systematic and random variation data can be used for model parameter extraction which leads to optimized device and circuit models. Characterization of the technology can enable more accurate yield prediction and determine its potential in different areas of circuit design.

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