0.35 m CMOS Process on Six-Inch Wafers: The First Baseline Run in the New Marvell NanoLab, Baseline Report VIII.

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0.35 μm CMOS Process on Six-Inch Wafers

The First Baseline Run in the New Marvell NanoLab

Baseline Report VIII.

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Abstract

This report presents details of the eighth six-inch baseline run, CMOS200, where a moderately complex 0.35 μm twin-well, silicided, LOCOS process was implemented. This process was based on the previous 0.35 μm six-inch run, CMOS192. CMOS200 was the start-up run in the new Marvell NanoLab, showing the ability to fabricate operational MOSFETs, after the move from the Microlab.

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INTRODUCTION

For 20 years the Microfabrication Laboratory at the University of California, Berkeley, has supported a useful monitoring tool, named CMOS baseline process. Through this unique process tool, continuous monitoring and diagnosis of process modules were performed at that facility. As a kind of reincarnation – the building of a new lab in Sutardja Dai Hall – the Microlab became the Marvell NanoLab: a newer and a more modern semiconductor laboratory than it was before. The legacy of the baseline experience had an important role in the start-up of the Marvell NanoLab, by providing a vehicle for initial testing of process modules and equipment.

The legacy of the Microlab

CMOS baseline runs were processed regularly on 4 inch wafers until 2001; then the first six-inch run, CMOS150, successfully transferred the old 1 μm baseline onto six-inch wafers. CMOS150 was followed by a new and more advanced 0.35 μm process, which produced the first sub half-micron devices. CMOS161 not only established our new 0.35 μm process, but also helped in pushing the performance of some of our tools to more advanced processes [1]. In the next baseline run, CMOS170, device parameters were improved by adjusting the implantation dose. A triple metal process was implemented to satisfy IC requirements on the test chip. [2] The following baseline run, CMOS180 targeted further improving device performance; as well as introducing shallow trench isolation and Mix & Match process in the lithography steps [3]. CMOS192 was the last run completed in the Microlab and its process served as a starting point after the move to the new lab. [4]

Our main goal

The first baseline run in the new Marvell NanoLab, CMOS200, was initiated with the main goal of validating the process functionality of the new facility. The success of that validation will be shown in this report.

BASELINE RUN CMOS200

The process of run CMOS200 is based on that of the previous runs in the Microlab. Notable changes/novelties are as follows:

1. Chip design: shrunk version of previous layout; drop-in chips left out; additional in-line test structures.

2. Process changes: based on tool availability during the move.

Baseline chip layout

Figure 1. shows the new layout of the CMOS200 baseline chip.

The new test chip CMOS200 was a shrunk version of previous chips with only essential devices/circuits aimed at quickly validating the NanoLab's baseline fabrication line. This enabled us to incorporate additional test structures for in-situ metrology measurements during the process. Drop-in spaces, to enable hosting of student chip designs, were eliminated. The main reasons for these changes were to shrink the chip size such that 6 layers could be fitted on one ASML 5500/300 reticle, also take advantage of the new design to incorporate additional in line monitoring test structures. The chip has the same overall features as the previous layouts did, such as:

- MOS transistor sets
- Vernier lines
- CV test structures
- Process test structures (contact resistors, contact chains, contact holes)
- Basic test circuits (NOR and NAND gates, ring oscillator)

In our project the single-transistor section has the most important role, since this part of the design should show if we were able to accomplish our main goal, to build an operational MOSFET.

The single-transistor section of the die consists of three groups, differentiated by their design rules. Each column is based on a 7x3 array of PMOS and NMOS transistors, which are varying in channel length (L = 0.2, 0.25, 0.3, 0.35, 0.4, 0.5, and 1 μm) and channel width (W = 2.5, 5, and 7.5 μm).

In the first column on the left side we applied a more robust design rule, basically following the old layout. These transistors do not follow any specific industrial layout design rules. Gate lengths are reduced while their contacts, active areas and metal lines are kept within safe processing limits.

In the second and third groups a more aggressive lambda scale design approach was used. Column 2 transistors in the middle follow Hewlett Packard's λ=0.5 μm design rules, while transistors in the third column followed HP design rules of λ=0.35 μm.

Appendix A shows the layout rules applied in the new test chip for CMOS200.

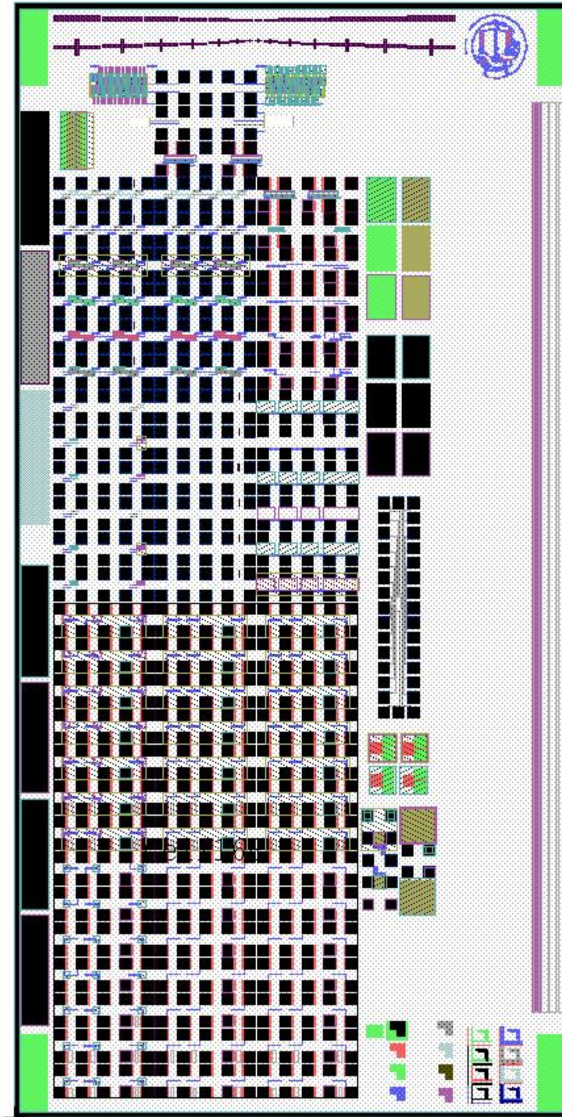


Figure 1. Layout of the CMOS200 baseline chip

ASML 300 reticle set

A complete mask set was generated for the newer/advanced ASML stepper model 300 (4X machine). A new test mask was fabricated in house ahead of the ASML300 stepper arrival. The new mask set was sent to ASML to be checked out on a similar machine at an associated semiconductor plant. Once this was done we embarked on redesigning the previous 4-fields masks to 6-fields reticles for the new baseline run.

Appendix B shows the test chip layout on the ASML 5500/300 reticle.

FABRICATION PROCESS OF CMOS200

Process flow modifications/developments were done during the run due to constant equipment moves from the Microlab to the NanoLab. Process timing, often challenging, forced us to look for alternate paths at some of the steps, whenever tool availability presented unacceptable delays or could create major problems with the run in progress.

Process modifications

The CMOS200 process flow consists of 51 steps including one metal layer module. This process creates N-channel and P-channel MOSFET devices, as well as some simple circuits.

Table 1 lists the steps used for the one-layer metal version of the baseline process. The starting material for the run was 6” P-type double polished wafers with the following parameters: <100> orientation, 20-60 Ω- cm resistivity, 635 μm ±25 μm wafer thickness.

Thin gate oxide, lightly doped drain structure, PECVD oxide spacer, titanium silicide S/D, and poly process junction engineering were also used in this run, based on the previous process flow. A 0.25 μm thick layer of undoped poly-silicon material was deposited, patterned and etched to achieve the structure of poly gate electrodes. By exposing the N- and P-channel transistor gate electrodes during S/D ion implantation, the appropriate poly gate work function was obtained.

The etching process of the Metal1 layer in Step 47 was performed in the recently re-installed (from the Microlab to the NanoLab) Centura metal chamber. Note: the endpoint detector was not working properly for aluminum; which could have had an impact on final results. This has not been confirmed.

Appendix C includes the detailed process flow of CMOS200.

Lithography

The CMOS200 process included 14 lithography steps. Table 2 lists all the lithography steps used for the fabrication of CMOS200, as well as the corresponding mask IDs and photo resist hard bake methods.

We had the first chance to try the Laboratory’s new ASML 5000/300 lithography stepper tool, which was performing each of the lithography steps during the entire process, CMOS200.

At several points in the process, a BARC (Bottom Anti-Reflective Coating; Shipley ARC-600) layer needed to be applied to achieve better performance during exposure. This special technique is detailed in Table 3.

After a few experiments, our standard photo resist was used for baseline processing: Rohm Haas UV210-0.6.

Most of the time during the lithography steps, unfortunately, we had problems with the SVGcoat/dev tracks and the UVBake tool, which caused more than one re-work step in the process flow.

Step	Process	Step	Process
0	Starting wafers	26	NMOS Vt adjustment implant
1	Initial oxidation	27	PMOS Vt adjust. implant photo
2	Zero layer photo	28	PMOS Vt adjustment implant
3	Scribe wafers	29	Gate oxidation, poly-Si dep.
4	Zero layer etch	30	Gate photo
5	Pad oxidation/nitride deposition	31	Poly-Si etch
6	N-well photo	32	P-type LDD implant photo
7	Nitride etch	33	P-type LDD implant
8	N-well implant	34	N-type LDD implant photo
9	Nitride removal	35	N-type LDD implant
10	Pad oxidation/nitride deposition	36	LDD spacer deposition
11	P-well photo	37	LDD spacer etch
12	Nitride etch	38	P+ gate and S/D photo
13	P-well implant	39	P+ gate and S/D implant
14	Nitride removal	40	N+ gate and S/D photo
15	Well drive in	41	N+ gate and S/D implant
16	Pad oxidation/nitride deposition	42	Gate and S/D annealing
17	Active area photo	43	Silicide formation
18	Nitride etch	44	PSG dep. and densification
19	P-well field implant photo	45	Contact photo
20	P-well field ion implant	46	Contact etch
21	LOCOS oxidation	47	Metal1 deposition
22	Nitride and pad oxide removal	48	Metal1 photo
23	Sacrificial oxidation	49	Metal1 etch
24	Screen oxidation	50	Sintering
25	NMOS Vt adjust. implant photo	51	Testing

Table 1. CMOS200 process steps

STEP (PHOTO)	RESIST	MASK (LAYER)	HARD BAKE (UVBAKE) PROGRAM
Zero layer	MF26A DUV	Zero layer	U
N-well	MF26A DUV	NWELL	J
P-well	MF26A DUV	PWELL	J
Active area	MF26A DUV	ACTIVE	J
P-well field implant	MF26A DUV	PFIELD	J
NMOS Vt adj. Implant	MF26A DUV	PWELL	J
PMOS Vt adj. Implant	MF26A DUV	NWELL	J
Poly gate	BARC + MF26A DUV	POLY	U
P-type LDD implant	MF26A DUV	PSELECT	J
N-type LDD implant	MF26A DUV	NSELECT	J
P+ gate & S/D	MF26A DUV	PSELECT	J
N+ gate & S/D	MF26A DUV	NSELECT	J
Contact	MF26A DUV	CONTACT	U
Metal1	BARC + MF26A DUV	METAL1	U

Table 2. Lithography steps and related information

STEP	STEP NAME	EQUIPMENT	MODULE PROGRAM	TARGET & PROCESS SPECIFICATION	NOTES
1	BARC spinning Shipley AR3-600	SVGCoat6	9, 4, 9	No HMDS, no PR coating 30 sec, 3750RPM ~600Å	Manually spin BARC on wafer; allow BARC to reach room temp. before appl.
2	BARC hardbake	SVGDev6	9, 9, 1	60 sec, 205ºC	
3	PR coat	SVGCoat6	9, 2, 1	Standard DUV coat	No HMDS required
4	Exposure	ASML		~19mJ typical	

Table 3. BARC and photoresist application process

Ion implantation

The CMOS200 baseline run required nine ion implantations, same as that of previous runs, which were processed by CORE Systems (Sunnyvale, CA).

Table 4 shows the sequence of implantation steps, indicating implant parameters and blocking layers. These parameters were the same as in previous runs.

We did use inline test wafers and monitor S/D and poly gate doping to control better this part of the process (wafers labeled as PCH, NCH, Tpoly1 and Tpoly2).

STEP	SPECIES	DOSE (CM-2)	ENERGY (KEV)/ANGLE	MASKING MATERIALS
N-well implant	Phosphorous	1E13	150	220nm Si3N4 + PR (Uvbake)
P-well implant	Boron	5E12	60	220nm Si3N4 + PR (Uvbake)
P-well field implant	Boron	2E13	80	25nm pad oxide + PR (Uvbake)
NMOS Vt adj. Implant	BF2	3E12	50	25nm pad oxide + PR (Uvbake)
PMOS Vt adj. Implant	Phosphorous	2E12	30	25nm pad oxide + PR (Uvbake)
P-type LDD implant	BF2 , BF2	5E13 5E13	10, 0° 10,180°	PR (Uvbake)
N-type LDD implant	Arsenic , Arsenic	5E13 5E13	30,0° 30,180°	PR (Uvbake)
P+ gate & S/D	Boron	3E15	20	PR(Uvbake)
N+ gate & S/D	Phosphorous	3E15	40	PR(Uvbake)

Table 4. List of implantation steps and parameters

Process tool set

Table 5 below lists the process tool set used.

After the move to the new laboratory, processes in each tool had to be re-characterized and in some cases, re-developed to bring performance within specifications. This required considerable amount of time.

PROCESS MODULE	EQUIPMENT	PROCESSSTEP
Lithography	ASML 5500/300 DUV stepper	Listed in Table 2.
	SVGCoat6	PR/BARC spinning
	SVGDev6	PR develop
	Matrix	PR removal
	Technics-C	PR removal, descum
	UVBake	Hardbake
Plasma etch	AMAT Centura-MxP+	Nitride/Oxide etch
	Lam 6	Spacer etch
	Lam 8	Poly-Si etch
	Lam 7	Aluminum etch
High temperature proc.	Tystar 1	Gate oxidation
	Tystar 2	Wet/dry oxidation
	Tystar18	Sintering
	Heatpulse 3	Silicidation
	Heatpulse 4	Annealing
CVD	AMAT P-5000 (PECVD)	Spacer/intermetal TEOS dep.
	Tystar 9 (LPCVD)	Nitride deposition
	Tystar 10 (LPCVD)	Poly-Si deposition
	Tystar 11 (LPCVD)	Spacer LTO/PSG deposition
Thin film systems	Novellus	Ti deposition
	CPA	Al deposition

Wet etch and cleaning	mSink 6	Pre-furnace piranha clean
		HF dip (10 :1, 25 :1)
		Rinse, spin dry
	mSink 7	Hot phosphoric etch
		Ti wet etch
	mSink 8	Post-lithography piranha clean
		Buffered HF etch (5 :1)
		Rinse, spin dry
Metrology and testing	ASIQ	Surface profiling
	Nanospec	Thin film thickness
	Leo	SEM
	4pt probe, Cde-resmap	Sheetresistance
	Autoprobe	Electroglass Autoprobe
	Sopra	Ellipsometer

Table 5. CMOS200 process tool set

PROCESS DEVELOPMENT AND CHARACTERIZATION

Development consisted of partial process modification of previous runs, with improved process modules as part of the new process flow. A large number of short loop experiments had to be conducted for the fabrication of the first baseline run in the new Marvell Nanofabrication Laboratory. Observations made through these short loops led to a successful run, which produced the first functional transistor from the NanoLab.

Process modifications:

Step 14, plasma etch instead of wet etch

Due to msink7 equipment problems which could have had an impact on our P-well region after the implantation, we decided to use the option of processing wafers with the Centura-mxp, using a photoresist mask to open areas to be implanted.

Recipe applied in the Centura-mxp :

1. MXP_NIT_ME (Av. 15sec)
2. MXP_NITRIDE_OE(Av.25 sec)

Step 31, process development on the lam8 poly-Si etcher tool

At this step we had to develop an etch process in the new tool, lam8 poly-Si etcher. The previous poly-Si etch tool, lam5, was decommissioned and replaced with a newer model, lam8. An etch recipe was used with native oxide break through as the main etch, with an over-etch step. Recipe: 65 sec. main etch + 20 sec. over-etch applying endpoint detection.

Figure 2 shows poly-Si etch short loop experiment results.

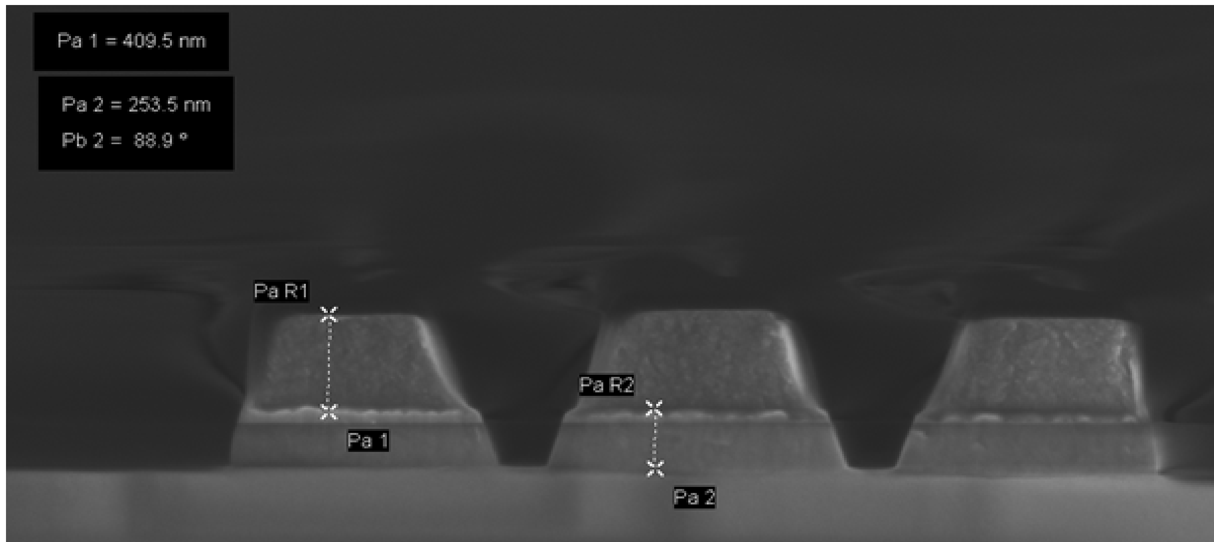


Figure 2. SEM cross-section of a sample after poly-silicon etching; photoresist (Pa1) on top of the poly-silicon layer(Pa2) [Magnification = 60.35K, EHT = 2kV, SignalA = Inlens, WD = 4.2mm]

Steps 36-37, Lightly Doped Drain (LDD) structure and poly-silicon sidewall spacer deposition and formation

Step 36:

Conformal deposition of the dielectric material plays an important role in sidewall spacer formation. The thickness of this layer determines the width of the spacer.

This step requires a deposition of 4000Å thick oxide layer which is done usually in our P5000 system (AMAT). In this low temperature process, ~450ºC, oxide is deposited from a TEOS (tetraethyl orthosilicate) source to produce conformal step coverage and superior wafer to wafer oxide thickness uniformity.

The AMAT P5000 system was down for a few weeks. Once it came up, it still had measurable non-uniformity, which motivated us to find another option as soon as possible for the LDD spacer deposition. We made a decision to split our wafer lot

into two groups (P5000 was processing with >10% non-uniformity) by taking into account that the solution will not be perfect.

1. Group I was processed in the P5000 system
2. Group II was processed by Tystar11 (LPCVD) furnace

The effect of the split had not been explored by the time this report was submitted.

Step 37:

For the sidewall spacer formation we had to find other alternatives for etching. The AMAT Centura plasma etcher was not at available due to a delay in the move; however, the newly installed lam6 was available in the NanoLab for oxide etching. This again requires short loop recipe development prior to etching CMOS200 wafers.

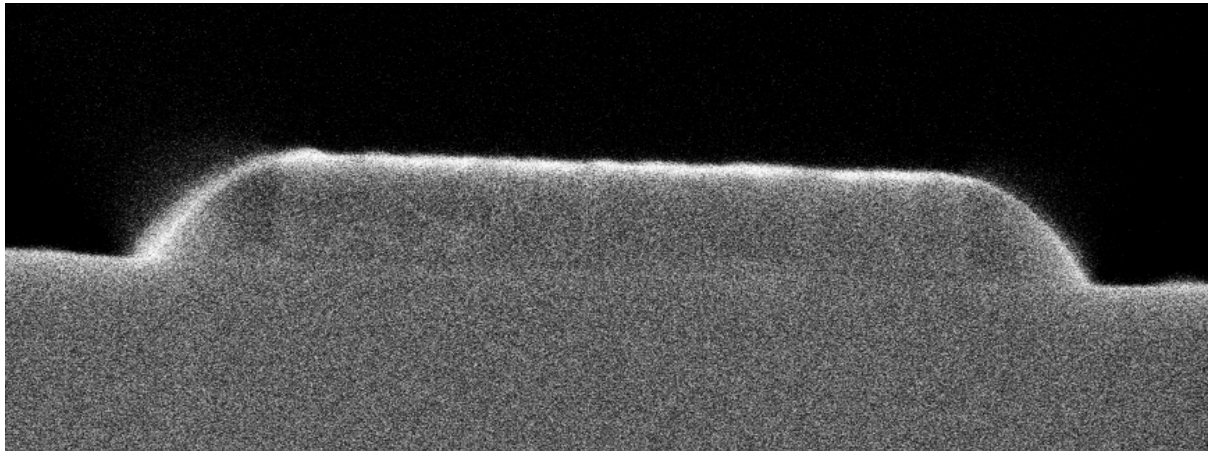


Figure 3. SEM cross-section of LTO deposition on short loop test wafer
[Magnification = 120K, EHT = 3kV, SignalA = Inlens, WD = 2.3 mm]

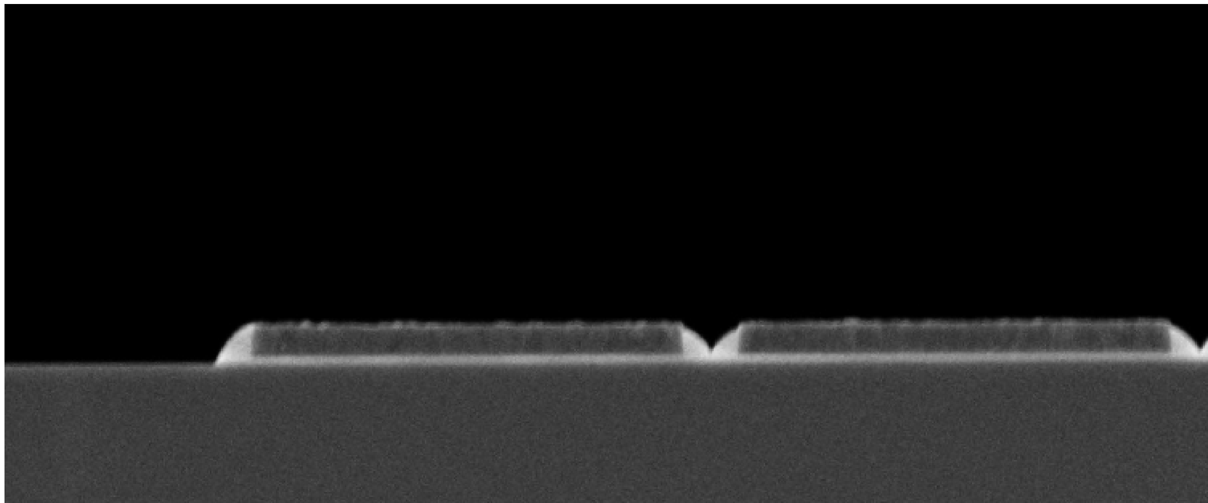


Figure 4. SEM cross-section of TEOS deposition on short loop test wafer
[Magnification = 120K, EHT = 3kV, SignalA = Inlens, WD = 2.4 mm]

Figures 3 and 4 show the cross-section of samples prepared for sidewall spacer formation, LTO and TEOS respecticely.

Table 6 lists process paramaters for the LDD spacer development process module.

STEP	STEP NAME	EQUIPMENT	RECIPE/SETUP	TARGET AND PROCESS SPECIFICATION
1	Standard cleaning	mSink6	Piranha+HF	
2	Poly-Si deposition	Tystar10	10SUPLYA	Undoped, ~2300A
3	Photoresist coat	SVGCoat6	1 2 1	
4	Poly gate photo	ASML	POLY mask	
5	Develop	SVGDev6	1 1 9	UVBake pr J.
6	Poly gate etch	Lam8	Recipe 8003	
7	Standard cleaning	mSink8	Piranha	
8	TEOS/LTO deposition	P5000/Tystar11	AH-USG / 11SULTOA	Av. 4000A TEOS / Av.3650A LTO
9	Spacer etch	Lam6	6001_OXIDE_ME	
10	Standard cleaning	mSink6	Piranha	
11	Poly deposition	Tystar10	10SUPLYA	~2300A, SEM sample prep.
12	Cleave wafer			
13	Oxide dip	Sink8	5:1BHF	10 sec
14	SEM pictures	Leo	3-5keV	

Table 6. LDD spacer development short loop process

Step 42, back side etch

Uniformity is of paramount importance in backside etch; thus, we were looking for a good sequence of steps to etch the back side of the wafers without destroying the patterned front side. Because of the earlier modifications, multi-layer depositions built up on the back sides of the wafers. This required two plasma and one wet etch steps. The best process is shown in Table 7.

PROCESS	EQUIPMENT	RECIPE SET	PROCESS SPECIFICATION
Nitride etch	technics-c	Standard nitride recipe	160 sec
Poly-Si etch	lam6	Recipe 6003	120 sec
Oxide wet etch	msink8	5:1HF	

Table 7. Backside etch process parameters

Step 43, RTA annealing of the gate and S/D in heatpulse4

Again, this step had to be started with characterizing the process in a new tool, heatpulse4. The traditional method of calibrating was used to arrive at the correct anneal temperature.

Appendix D shows RTA recipes after calibration.

The temperature can be controlled in heatpulse4 two different ways; accordingly, the CMOS200 wafer lot was split into 2 groups:

1. RTA annealing by applying the built in pyrometer of the tool,
2. RTA annealing by using the wafer-thermocouple.

Since electrical measurements were taken only on wafer #3 by the time this report was submitted, the split-anneal experiment was not completed.

THE FIRST FUNCTIONAL MOS TRANSISTOR IN THE NANOLAB

As mentioned earlier, our goal with the first baseline run, CMOS200, was to show that the lab retained full processing capability to produce MOS transistors after the move. Because of time constraints wafer #3 from the lot CMOS200 was moved ahead through silicidation to electrical measurements.

At step 44, silicidation, the Ti layer was used as interconnect. Wafer #3 was patterned with metal1 mask and plasma etched. (Steps 48, 49, 50)

Electrical measurement results of wafer #3

Electrical measurements were obtained using an automated test system. The HP4062ASemiconductor Parametric Test System utilizes an HP4085A Switching Matrix, an HP4084BSwitching Matrix Controller and an Agilent4142B Modular DC Source/Monitor Unit. The system is connected to a Model 2001X Electroglass probe station, which is controlled by a Metrics I/CV software running on a PC workstation. All the test structures and transistors were configured with proper pad array on the chip that would support a 2 x 5 pin probe card (10 tips).Test structure layout was set up this way to allow fast and accurate collection of a large amount of data on device parameters, and other process monitoring related items.

The parametric testing was performed by using the PC based Metrics software with built in measurement modules [5].

The following functions have been used to calculate and display transistor characteristics:

- BASELINE_IDVD_ – drain current vs. drain voltage measurement
- DIBL – sub-threshold slope calculation (drain induced barrier effect)
- BASELINE_Sat - Saturation current and transconductance calculation
- BASELINE_VT

Fiures 5-10 show typical I-V characteristics of CMOS200 wafer #3 transistors of 0.35μm drawn channel length and 2.5 μm width.

BASELINE_IDVD

NMOS

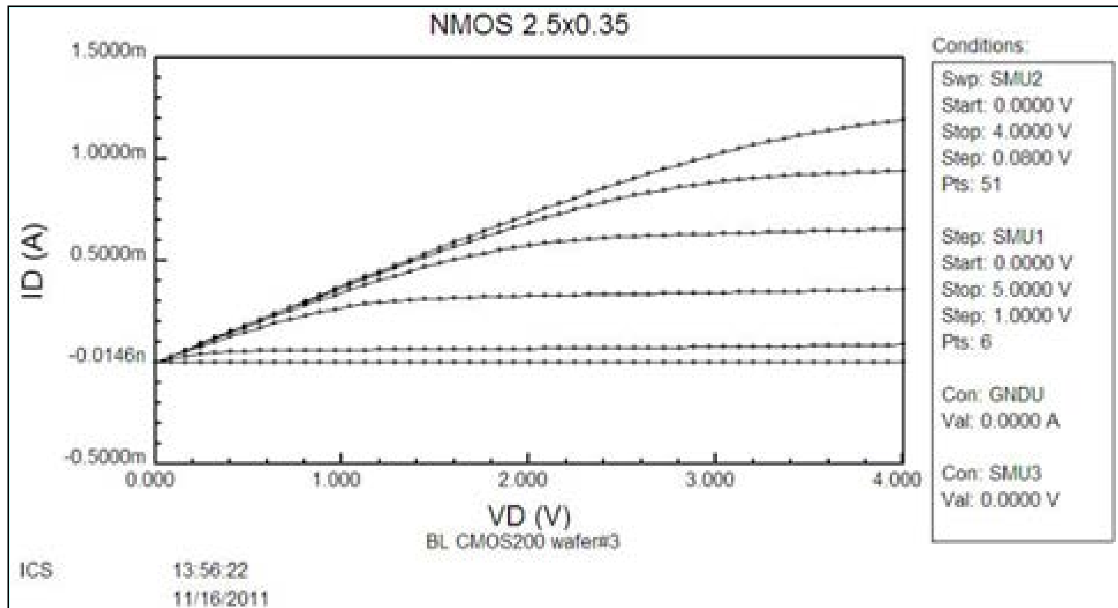


Figure 5. Id-Vd characteristics of CMOS200 wafer #3 NMOS transistors; 0.35μm drawn channel length and 2.5 μm width

PMOS

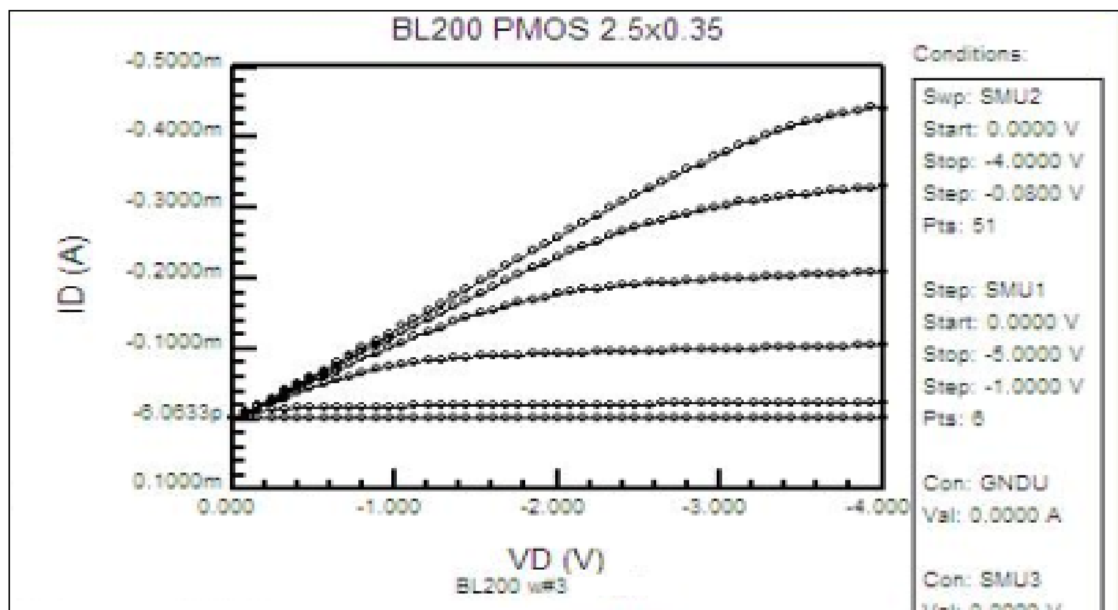


Figure 6. Id-Vd characteristics of CMOS200 wafer #3 PMOS transistors; 0.35μm drawn channel length and 2.5 μm width

BASELINE_VT

NMOS

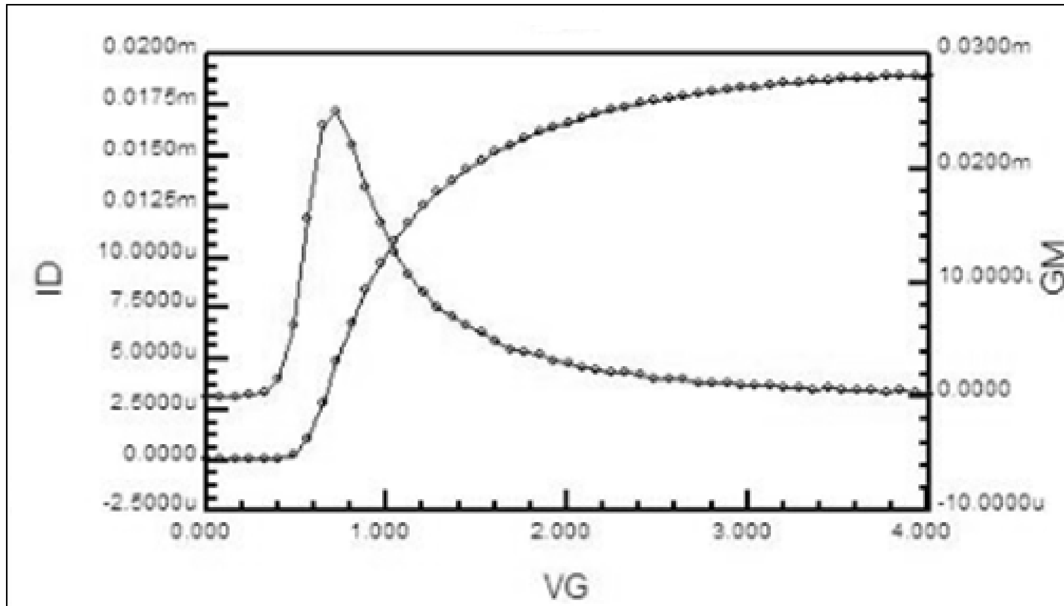


Figure 7. Id-Vg and Gm-Vg characteristics of CMOS200 wafer #3 NMOS transistors; 0.35µm drawn channel length and 2.5 µm width

PMOS

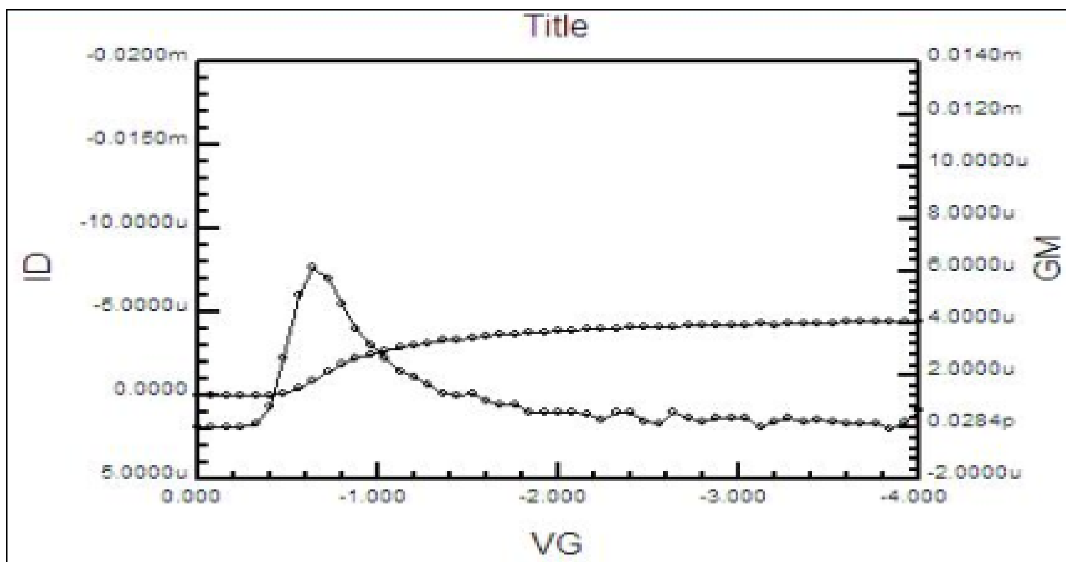


Figure 8. Id-Vg and Gm-Vg characteristics of CMOS200 wafer #3 PMOS transistors; 0.35µm drawn channel length and 2.5 µm width

DIBL – (Drain Induced Barrier Lowering) sub-threshold slope

NMOS

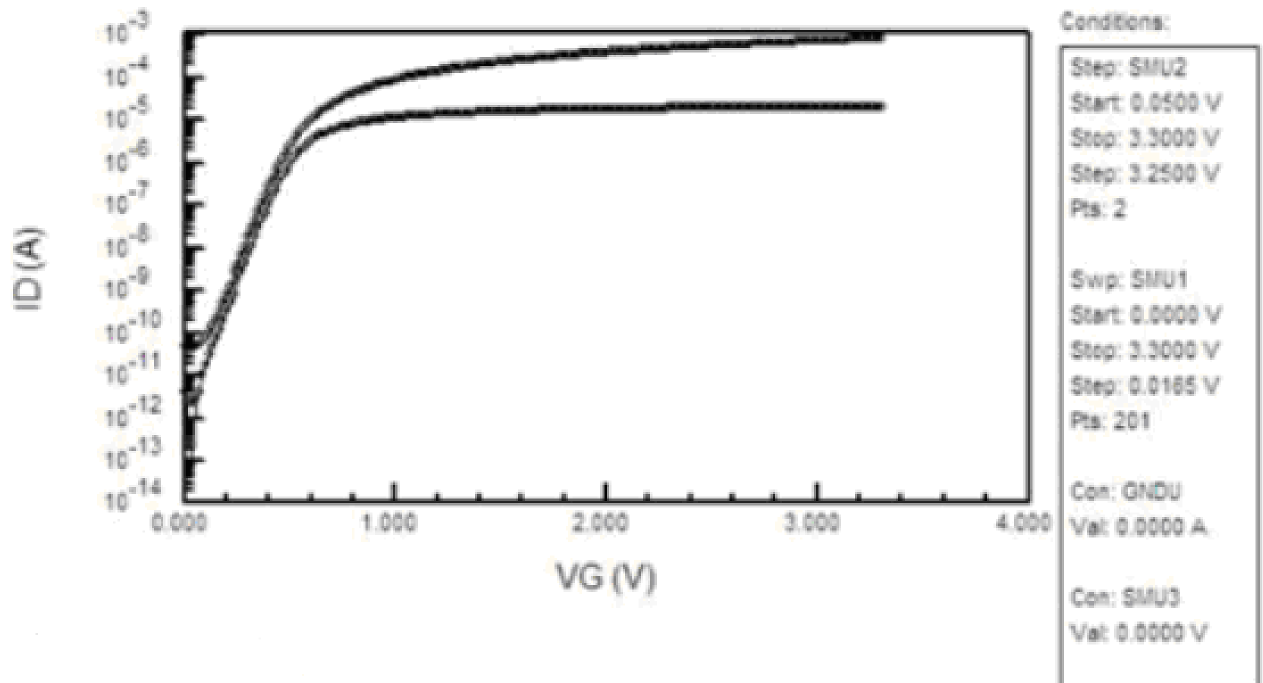


Figure 9. Id-Vg of curves of CMOS200 wafer #3 NMOS transistors; 0.35μm drawn channel length and 2.5 μm width

PMOS

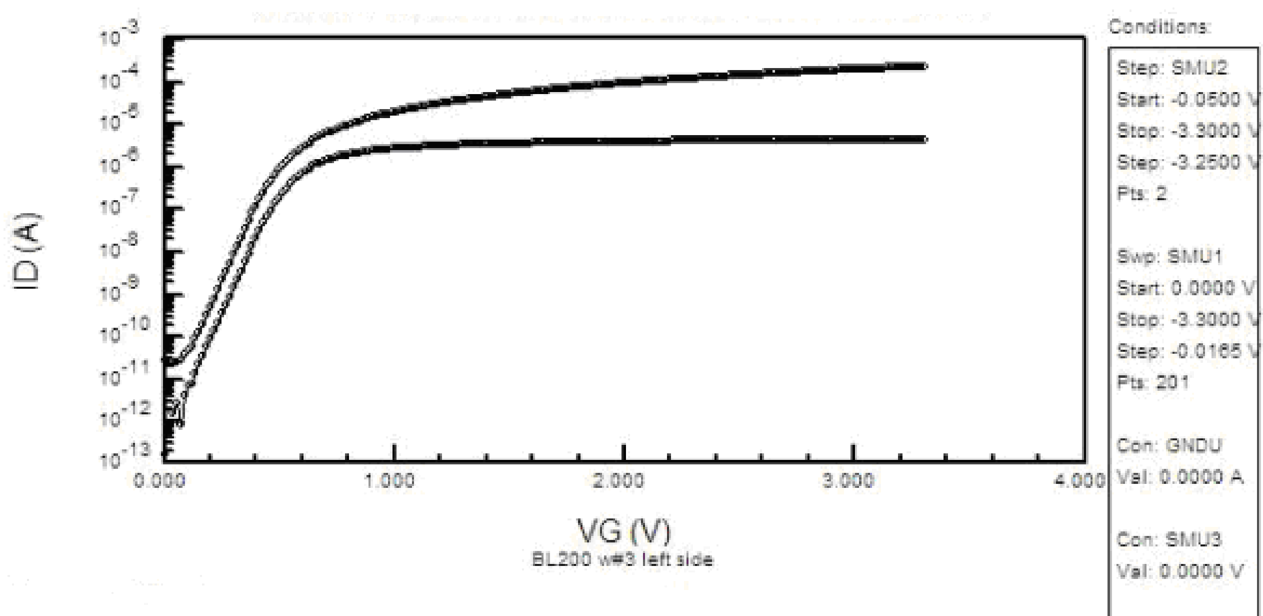
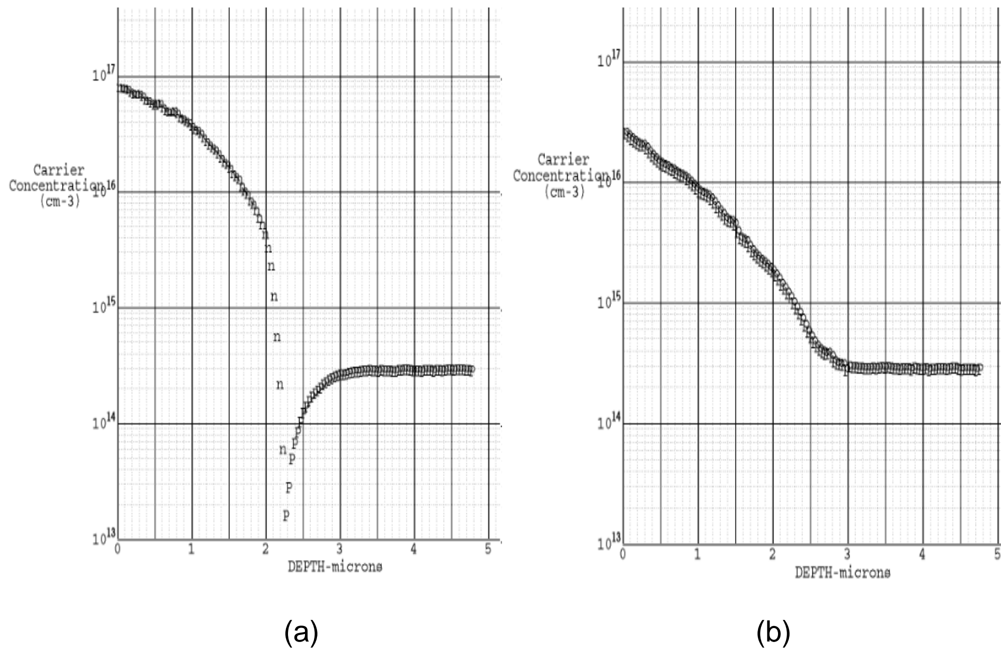


Figure 10. Id-Vg curves of CMOS200 wafer #3 PMOS transistors; 0.35μm drawn channel length and 2.5 μm width

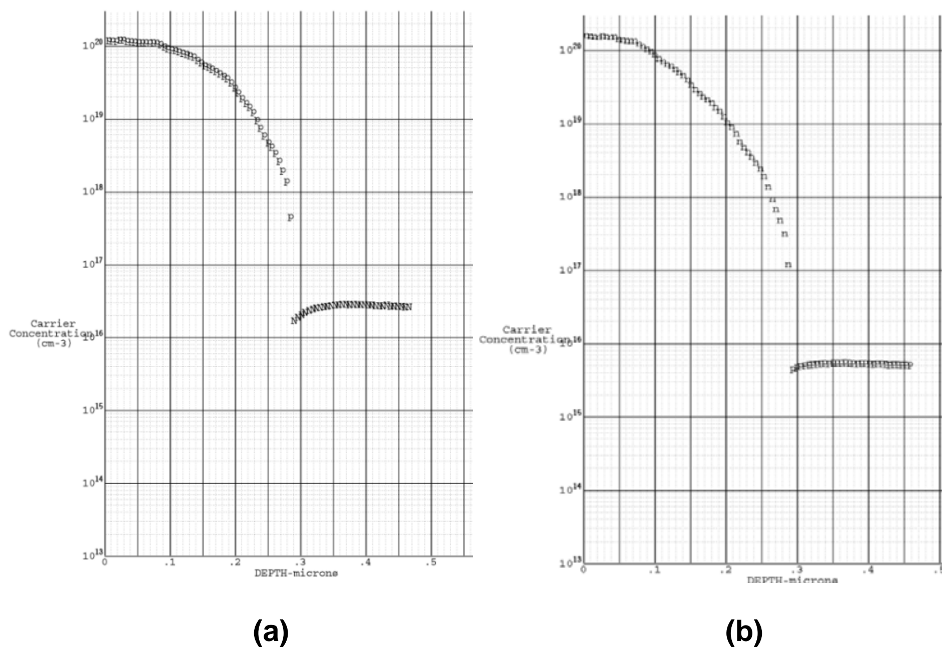
SRA – Spreading resistance analysis of process wafer #3

The Spreading Resistance Analysis was requested for doping profiles of the N-channel, P-channel, N+ source-drain and P+ source-drain regions of the N and P-channel transistors. The SRA was performed by Solecon Laboratories (San Jose, CA).The results from process wafer #3 of the lot CMOS200 are shown below.



(a) (b)

Figure 11. Experimental results for areas under the gate oxide of CMOS transistors obtained from SRA. (a) p-type transistor, (b) n-type transistor



(a) **(b)**

Figure 12. Experimental results for source-drain areas obtained from SRA (a) P+ source-drain, (b) N+ source-drain

Process and device parameters

Table 8 shows the summary of various measurements and test results of the CMOS200 process. Values shown in this table were extracted from measurements on L=0.35 μm, W=2.5 μm devices.

NO.	PARAMETERS	UNITS	NMOS	PMOS
1	Vt	V	0.52	-0.54
2	Sub Threshold Slope	mV/decade	89	90
3	Surface dopant concentration	Atom/cm3	1.9E16	6.0E16
4	Substrate dopant concentration	Atom/cm3	5.0E15	2.0E16
5	Tox (Gate)	nm	7.57	7.57
6	Xj (S-D)	μm	0.27	0.29
7	Xw (Well depth)	μm	2.9	2.3
8	Rdiff (sheet resistance) (S-D)	Ω/square	43	59
9	Rpoly (sheet resistance) (Gate)	Ω/square	466	191

Table 8. Summary of electrical measurements for CMOS200, wafer #3

1. Threshold voltages were measured by the autoprobe Vt module using the linear extrapolation method.

2. Sub-threshold slope values are hand calculated based on the autoprobe DIBLE module (log (Id) vs. Vg). Using the autoprobe's DIBL module a log (I_d) vs. V_g graph was plotted when the device was operating in the linear region: V_d = |50 mV|. By picking a decade of Id change on the y scale the corresponding Vg difference was read from the x scale.

3-4. Surface dopant concentration numbers are based on the SRA results, which matched the values measured on the autoprobe.

5. Gate oxide thickness was measured by the Sopra ellipsometer during processing.

6-7. Well depth and the source-drain depth data arise from the SRA graphs.

8-9. Sheet resistance values were obtained by four-point-probe measurements during processing.

SUMMARY

The goal of this baseline run (CMOS200) was to test and qualify the new Marvell NanoLab for CMOS processing. The lot was started when the move of the Microlab from Cory Hall to Sutardja Dai Hall was not yet fully completed, and served as a basis for prioritizing equipment moves. Each tool needed had to be re-characterized after the move, prior to committing the baseline wafers to processing in the tool. Several etchers were replaced with later models at the time of the move; processes had to be redeveloped on these. Process steps different from those of previous runs (in the Microlab) are detailed in this report. Because of time constraints only one wafer could be completed and tested. However, in spite of the upheaval we were able to produce working CMOS transistors.

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BIOGRAPHY

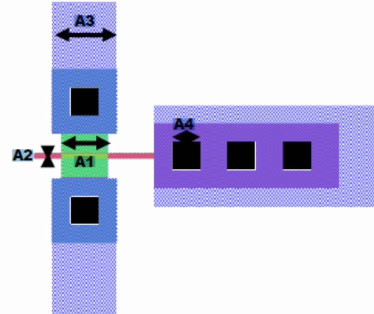
Anna Szűcs earned her Diplôme d'Ingénieur Arts&Métiers degree at École Nationale Supérieure d'Arts et Métiers (ENSAM), Paris, in 2010. She graduated with a Diploma of Mechanical Engineering from the Budapest University of Technology and Economics (BME) in 2009. She worked at the UC Berkeley Microlab and NanoLab as an Associate Specialist – Baseline engineer, 2010-11. Her main task was to transfer the CMOS baseline process from the Microlab in Cory Hall to the new Marvell NanoLab in Sutardja Dai Hall, UC Berkeley.

APPENDIX A - Design rules in transistor layout

In the CMOS200 baseline process we introduced additional transistors with standard, lambda scaled design rules.

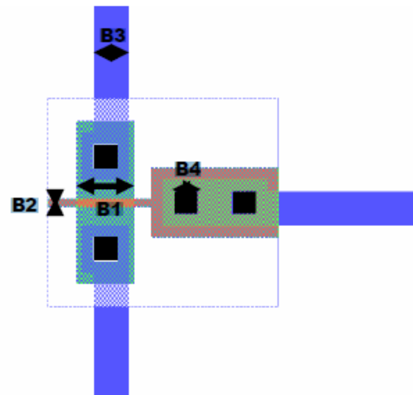
1st column of transistors with robust design (In house design rules applied)

A.1. Gate length: 2.5 µm
A.2. Gate width: 0.3 µm
A.3. Metal line width: 3.5 µm
A.4. Contact hole: 1.5 µm



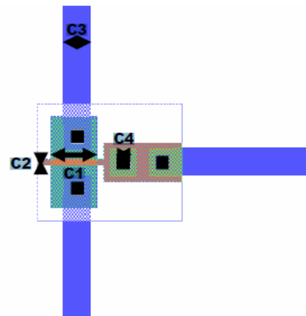
2nd column of transistors with λ=0.5 µm (HP design rules applied)

B.1. Gate length: 2.5 µm
B.2. Gate width: 0.3 µm
B.3. Metal line width: 1.5 µm
B.4. Contact hole: 1 µm

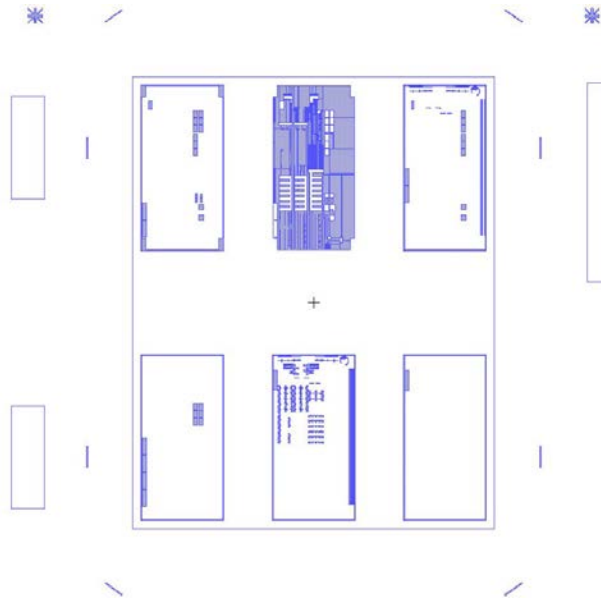


3rd column of transistors with λ=0.35 µm (HP design rules applied)

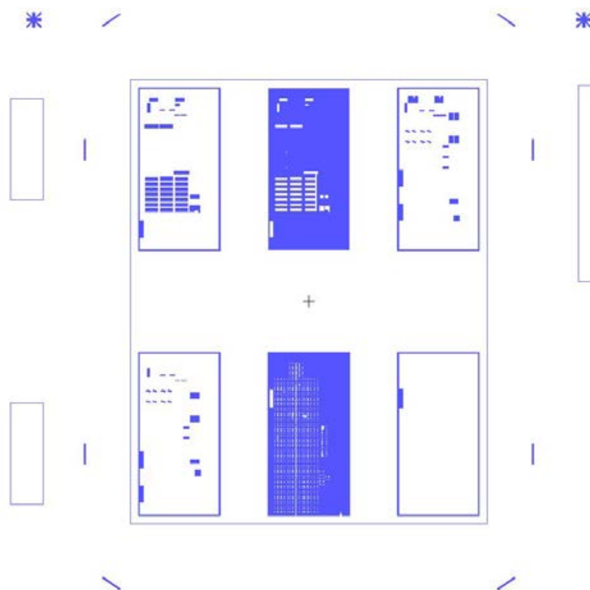
C.1. Gate length: 2.5 µm
C.2. Gate width: 0.3 µm
C.3. Metal line width: 1.5 µm
C.4. Contact hole: 0.7 µm



Appendix B - ASML mask layouts



Tape-out mask plates fabricated by Benchmark Technologies; including Active, Poly, P-field, N-field, Contact and Metal layers.



Tape-out mask plates fabricated by Benchmark Technologies; including N-well, P-well, N-select, P-select, Vias

Appendix C – CMOS200 Process flow

Step	Process step	Substeps	Equipment / recipe	Target and process specification	Notes
0	**STARTING WAFERS**		19-33 Ω-cm, P-type, <100>, 6"		14 wafers + 2 monitor (PCH, NCH)
1	**INITIAL OXIDATION**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	2 dummies for PM etch characterization
		b) Standard cleaning	MSink 6	Piranha + 25:1 HF until dewets	
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 250 A 950C, 30 min; 20 min N2 annealing	Measure oxide thickness
2	**ZERO LAYER PHOTO**		ASML	COMBI mask UVBAKE pr. J	Defines ASML alignment PM marks
3	**SCRIBE WAFERS**		Diamond pen	Scribe numbers into the photoresist	
4	**ZERO LAYER ETCH**	a) Etch through oxide	Centura-MxP+, recipe: MXP_OXSP_E TCH	250 A etch	
		b) Etch PM marks	Lam8, recipe: 8003	1200 A etch	
		c) Photoresist strip	Matrix	2.5 min O2 ash	
		d) Measure etch depth	ASIQ	~1450A to be measured	PM marks to be measured
5	**PAD OXIDATION / NITRIDE DEP.**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	MSink8 +MSink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: **350 A** 1000C, 21 min; 15 min N2 annealing	Include NCH, PCH, and measure ox. on them
		d) Nitride deposition	Tystar9, 9SNITA	Target: 2200 A	Do not include NCH, PCH, measure nitride
6	**N-WELL PHOTO**		ASML	Mask: NWELL UVBAKE pr. J	
7	**NITRIDE ETCH**		Centura-MxP+, recipe: MXP_NITRIDE _OE	Monitor endpoint	Measure oxide on each wafer (critical for implantation)
8	**N-WELL IMPLANT**		CORE Systems	Specie/Dose/Energy: P, 1E13, 150 keV	Include PCH
9	**NITRIDE REMOVAL**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8	Piranha	
		c) Nitride wet etch	MSink7	160C fresh phosphoric acid ~4 hours	
		d) Pad oxide wet etch	MSink8	5:1 BHF until dewets	Include PCH, NCH

10	PAD OXIDATION / NITRIDE DEP.	a) TLC clean	Tystar2, 2TLCA	2 hrs of cleaning	
		b) Standard cleaning	MSink8 + MSink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 350 A 1000C, 21 min; 15 min N2 annealing	Include NCH, PCH, and measure ox. on them
		d) Nitride deposition	Tystar9, 9SNITA	Target: 2200 A	Do not include NCH, PCH! Measure nitride
11	**P-WELL PHOTO**		ASML	Mask: PWELL UVBAKE pr. J	
12	**NITRIDE ETCH**		Centura MxP+, recipe: MXP_NITRIDE _OE	Monitor endpoint	Measure oxide on each wafer (critical for implantation)
13	**P-WELL IMPLANT**		CORE Systems	Specie/Dose/Energy: B, 5E12, 60keV	Include NCH
14	**NITRIDE REMOVAL**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8	Piranha	
		c) Nitride Dry etch	MXP_NIT_ME MXP_NITRIDE_OE	15 seconds (main) 25 seconds (OE)	Dry etch instead of wet etch - used Centura-mxp
		d) Pad oxide wet etch	MSink8	5:1 BHF until dewets	Include PCH, NCH
15	**WELL DRIVE-IN**	a) TLC clean	Tystar2, 2TLCA	2 hrs of cleaning	
		b) Standard cleaning	MSink8 + MSink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH
		c) Well drive-in	Tystar2, 2WELLDR	1100C, 150 min; 15 min N2 annealing	Measure oxide thickness
		d) Oxide wet etch	MSink8	5:1 BHF until dewet	Measure Rsq on NCH, PCH
16	**PAD OXIDATION / NITRIDE DEP.**	a) TLC clean	Tystar2, 2TLCA	2 hrs of cleaning	
		b) Standard cleaning	MSink8 + MSink 6	Piranha + 25:1 HF until dewets	Include NCH, PCH and 2 dummies
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 350 A, 1000C	Measure oxide thickness on NCH
		d) Nitride deposition	Tystar9, 9SNITA	Target: 200 A	Include PCH only and dummies, measure nitride
17	**ACTIVE AREA PHOTO**		ASML	ACTIVE mask UVBAKE pr. U	Use BARC if needed. Stop 4 wafers for STI process before this step
18	**NITRIDE ETCH**		Centura MxP+, MXP_NITRIDE _OE	Monitor endpoint, allow some overetch	
19	**P-WELL FIELD IMPLANT PHOTO**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8	Piranha	
		c) Lithography	ASML	Mask: PFIELD UVBAKE pr. J	

20	**P-WELL FIELD IMPLANT**		CORE Systems	Specie/Dose/Energy: B, 2E13, 80keV	
21	**LOCOS OXIDATION**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8 + MSink 6	Piranha + 10 sec dip in 25:1 HF	Include NCH, PCH
		d) Wet oxidation	Tystar2, 2WETOXA	Target: 5500 A 1000C, 120 min; 20 min N2 annealing	Measure oxide on NCH and 3 wafers
22	**NITRIDE REMOVAL / PAD OXIDE REMOVAL**	a) Oxide wet etch	MSink 6	10:1 HF for ~60 sec until dewets	Include PCH, remove thin ox from nitride
		b) Nitride wet etch	MSink 7	160C fresh phosphoric acid ~4 hours	Measure pad ox. on ACTV area to make sure nitride is gone
		c) Oxide wet etch	MSink 6	10:1 HF for ~60 sec until PCH dewets	Etch pad oxide
		d) Oxide wet etch on NCH	MSink7	Fresh 5:1 BHF until dewets	Remove LOCOS from NCH
23	**SACRIFICAL OXIDATION**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	MSink 6	Piranha + 10 sec dip into 25:1 HF	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 250 A 900C, 40 min; 1 sec (meaning zero) N2 annealing	Measure oxide on ACTV area
24	**SCREEN OXIDATION**	a) TLC clean	Tystar2, 2TLCA	2 hours of cleaning	
		b) Standard cleaning	MSink 6	Piranha + 25:1 HF dip until NCH, PCH dewet	Include NCH, PCH
		c) Dry oxidation	Tystar2, 2DRYOXA	Target: 250 A 900C; 15 min N2 annealing	
25	**NMOS Vt IMPLANT PHOTO**		ASML	Mask: PWELL UVBAKE pr. J	
26	**NMOS Vt IMPLANT**		CORE Systems	Specie/Dose/Energy: BF2, 3E12, 50keV	Include NCH
27	**PMOS Vt IMPLANT PHOTO**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8	Piranha	
		c) Lithography	ASML	Mask: NWELL UVBAKE pr. J	
28	**PMOS Vt IMPLANT**		CORE Systems	Specie/Dose/Energy: P, 2E12, 30keV	Include PCH
29	**GATE OXIDATON**	a) TLC clean	Tystar1, 1TLCA	2 hours of cleaning	

	and POLY DEP.	b) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8 +MSink 6	Piranha + dip in 25:1 HF until NCH, PCH dewet	Include NCH, PCH, Tox, Tpoly1, Tpoly2
		c) Gate oxidation	Tystar1, 1THIN-OX	Target: 80 A 850C, 30 min oxidation; 900C, 30 min N2 anneal	Include NCH, PCH, Tox, Tpoly1, Tpoly2
		d) Poly-Si depostion	Tystar10, 10SUPLYA	Target: 2500 A	Include Tpoly1, Tpoly2 and dummy wafers
		e) Measurements	Sopra, Rudolph	Measure oxide thickness on Tox	
			SCA	Measure Dit, Qox, Nsc, Ts on Tox	
			Nanospec		
			4PTPRB	Strip oxide from NCH and PCH; measure Rs	
30	**POLY GATE PHOTO**		ASML	Mask: POLY UVBAKE program U	Use BARC if needed
31	**POLY ETCH**	a) Poly etch	Lam8, recipe 8003	Monitor endpoint, 20sec over etch	Etch through BARC
		b) Photoresist strip	Matrix	2.5 min O2 ash	
		c) Standard cleaning	MSink7 + MSink 8	100:1 HF dip to remove polymers formed in Lam5, Piranha	
		d) Measure channel length with SEM	Leo	Check Poly-Si lines with SEM	
32	**PMOS LDD IMPLANT PHOTO**		ASML	Mask: PSELECT UVBAKE pr. J	
33	**PMOS LDD IMPLANT**		CORE Systems	Specie/Dose/Energy: BF2, 5E13, 10keV, +7° tilt @ 0 orientation; BF2, 5E13, 10keV, -7° tilt @ 180 orientation	Include PCH, Tpoly1
34	**NMOS LDD IMPLANT PHOTO**	a) Photoresist strip	Matrix	Std. 2.5 min O2 ash	
		b) Standard cleaning	MSink8	Piranha	
		c) Lithography	ASML	Mask: NSELECT UVBAKE pr. J	
35	**NMOS LDD IMPLANT**		CORE Systems	Specie/Dose/Energy: As, 5E13, 30keV, +7° tilt @ 0 orientation; As, 5E13, 30keV,	Include NCH, Tpoly2

				-7º tilt @ 180 orientation	
36	**LDD SPACER DEP.**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8 + MSink 6	Piranha	Include 3 dummies for oxide etch test
		c1) LTO deposition	Tystar11 , 11SULTOA	36 min , Av : 3650A	Process wafer lot split into two group
		c2) TEOS deposition	P-5000; recipe AH-USG	Target: 4000 A; Dep. rate: ~80 A/sec	
		d) Annealing	Tystar2; 2HIN2ANA	900C, 30 min	
		e) Measurement	Nanospec		
37	**LDD SPACER FORM.**		Lam6, recipe 6001_OXIDE_ME	Timed process : ~230sec	Verify completion of etch on ACTV area, SEM
38	**P+ GATE & S/D PHOTO**		ASML	Mask: PSELECT UVBAKE program J	
39	**P+ GATE & S/D IMPLANT**		CORE Systems	Specie/Dose/Energy: B, 3E15, 20keV	Include PCH, Tpoly1
40	**N+ GATE & S/D PHOTO**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8	Piranha	
		c) Lithography	ASML	Mask: NSELECT UVBAKE pr. J	
41	**N+ GATE & S/D IMPLANT**		CORE Systems	Specie/Dose/Energy: P, 3E15, 40keV	Include NCH, Tpoly2
42	**BACK SIDE ETCH**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8	Piranha	
		c) Coat wafers	SVGCOAT6	No litho step UVBAKE pr. J	Coat front side
		d) Oxide wet etch	MSink8	5:1 BHF until backside dewets	Dip off native oxide
		e) Nitride etching	Technics-c , standard nitride etch recipe	160 sec	
		f) Poly-Si etch	Lam6 recipe 6003	120 sec	
		g) Oxide wet etch	MSink8	5:1 BHF until backside dewets	Include NCH, PCH, Tpoly1, Tpoly2
43	**GATE & S/D ANNEAL**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	Sink8 + Sink 6	Piranha	Include NCH, PCH, Tpoly1, Tpoly2

		c) RTA annealing	Heatpulse3, recipe 1050RTA6.RCP	450C 30 sec, 900C 10 sec, 1050C 5 sec	Device chamber, N2 atmosphere
		d) Measurement	4PTPRB	Measure Rs on NCH, PCH, Tpoly1, Tpoly2	
44	**SILICIDATION**	a) Sputter etch	Novellus, recipe ETCHSTD	1 min etch	Sputter etch, include a dummy
		b) Ti deposition	Novellus, recipe TI300STD	25 sec deposition	Measure Rsq of Ti film
		c) RTA annealing	Heatpulse3, recipe 650RTA6.RCP	450C 20sec, 650C 15sec	Silicide chamber, N2 atmosphere
		d) Wet etch Ti & TiN	MSink7	Remove unreacted Ti and TiN in fresh piranha	Measure field ox on LOCOS area t osee the completion of the etch
45	**PSG DEP & DENSIFICATION**	a) Standard cleaning	MSink 6	Piranha (NO HF dip)	Include PCH, NCH, Si and TiSi test wafers
		b) PSG deposition	Tystar11, recipe 11SDLTOA	Target: 7000 A ~45 min, 450C	
		c) Standard cleaning	Sink8+Sink6	Piranha	
		d) RTA annealing	Heatpulse3, recipe 900RTA6.RCP	450C 30 sec, 900C 10 sec	Silicide chamber, N2 atmosphere
		e) Measurement	Nanospec		Measure LOCOS+TEOS on a LOCOS area
			4PTPRB		
46	**CONTACT PHOTO AND ETCH**	a) Standard cleaning	MSink8 + MSink 6	Piranha, NO HF	
		b) Litho	ASML	Mask: CONTACT UVBAKE pr. U	Overexpose contact (30-40 mJ/cm2)
		c) Contact etch	Centura-MxP+, recipe: MXP_OXSP_ET_EP	Allow 15 sec after signal drops	
		d) Measurement	Manual probe		ACT+CONT and POLY+CONT areas
47	**METAL 1 DEP.**	a) Photoresist strip	Matrix	2.5 min O2 ash	
		b) Standard cleaning	MSink8 +MSink 6	Piranha, NO HF	Include a dummy. HF damages silicide!
		c) Al deposition	Novellus: Ti liner (TI300STD) Al/2%Si (AL6KGV)	Target: 6000 A	
		d) Measure Rs	4ptprb		
			ASML	BARC litho, Mask: METAL1 UVBAKE pr. U	
48	**METAL1 PHOTO**	a) Al etch	Centura MET, Standard recipe MET AL-STD		No need to etch BARC separately

49	**METAL1 ETCH**	b) Measurement	Manual probe		R=inf on LOCOS area required
		a) Photoresist strip	Matrix	2.5 min O2 ash	
50	**SINTERING**	b) Rinse	Sink8	Rinse and spin dry, no piranha or HF	
		c) Sintering	Tystar18, recipe: H2SINT4A.018	20 min, 400C	
51	**TESTING**		Autoprobe		

Appendix D - Heatpulse calibration and recipes

Before each calibration new TC should be checked out. Specification: less than 50°C/sec temperature change. Thickness should be measured with Sopra or Ellips, than fit to curve to determine offset.

Calibration

Example of calibration recipe at 1050°C, O2 atmosphere

STEP	MODE	TIME [SEC]	TEMPERATURE [C]
1	steady	5	0
2	ramp	10	450
3	steady	30	450
4	ramp	15	1050
5	steady	180	1050
6	ramp	10	600

Process

Gate & S/D annealing (N2, device chamber) – Step 43

STEP	MODE	TIME [SEC]	TEMPERATURE [C]
1	steady	5	0
2	ramp	10	450
3	steady	30	450
4	ramp	10	900
5	steady	10	900
6	ramp	3	1050
7	steady	5	1050
8	ramp	10	600

Silicidation (N2, silicide chamber) – Step 44

STEP	MODE	TIME [SEC]	TEMPERATURE [C]
1	steady	5	0
2	ramp	10	450
3	steady	20	450
4	ramp	5	650
5	steady	15	650

PSG densification (N2, silicide chamber) – Step 45

STEP	MODE	TIME [SEC]	TEMPERATURE [C]
1	steady	5	0
2	ramp	10	450
3	steady	30	450
4	ramp	10	900
5	steady	10	900
6	ramp	6	600