# Coherent Porous Silicon Wick for a MEMS Loop Heat Pipe

*Navdeep Singh Dhillon*

Electrical Engineering and Computer Sciences
University of California at Berkeley

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by

Navdeep Singh Dhillon

B.Tech. (Indian Institute of Technology Kharagpur, India) 2004
M.S. (Purdue University, West Lafayette) 2006

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requirements for the degree of

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Committee in charge:
Professor Albert P. Pisano, Chair
Professor Liwei Lin

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by Navdeep Singh Dhillon

**Research Project**

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Approval for the Report and Comprehensive Examination:

**Committee:**

Prof. Albert P. Pisano

Research Advisor

28 JAN 2012

Date

* * * * * *

Prof. Liwei Lin

Second Reader

Jan 25, 2012

Date

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Navdeep Singh Dhillon

## Abstract

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Navdeep Singh Dhillon

Master of Science, Plan II in Electrical Engineering and Computer Sciences

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Professor Albert P. Pisano, Chair

The electronics industry desires compact high-heat-flux thermal management solutions for keeping device junction temperatures within the safe operating limit. Loop heat pipes (LHPs) are passive phase change-based thermal transport systems that can satisfy these demands, provided they can be miniaturized to fit inside compact devices and components. This can be achieved by fabricating LHPs on silicon and Pyrex wafers using MEMS microfabrication techniques. Although most of the LHP components can be easily implemented on planar substrates, the wicking structure is a major stumbling block in the successful implementation of these MEMS loop heat pipes.

This report presents the design and fabrication aspects of a coherent porous silicon (CPS)-based micro-columnated wicking structure for a micro-columnated loop

heat pipe ($\mu$CLHP). The micro-columnated wick has a vertically-wicking dual-scale topology, with the primary wick fabricated out of CPS and the secondary wick etched onto a capping wafer. This design allows for enhanced device heat flux carrying capacities due to the ability to independently optimize the capillary pumping pressures and thin-film evaporation characteristics of the wick. CPS is obtained by illuminated electrochemical etching of silicon. The theory and experimental methods used to obtain CPS are explained, an experimental etching setup is designed, and preliminary etching results are reported. A detailed fabrication process flow for the $\mu$CLHP device is outlined, and the potential issues that could arise during its implementation are discussed.

To my Family

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# Chapter 1

# Introduction

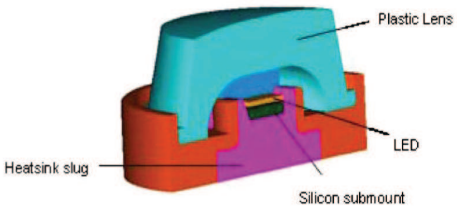
## 1.1 Motivation

Due to the principle of Joule heating, all electronic systems generate waste heat, which in the electronics industry is often referred to as the *thermal budget* of the system. The thermal budget leads to a rise in the device junction temperature or the temperature of the most critical components of the device. This is problematic since most semiconductor-based electronics needs to stay within a safe operating temperature limit, which is approximately equal to $120^oC$ for most silicon-based devices. The thermal budget or waste heat therefore needs to be removed from the device using an appropriate mechanism. The concerned field of study is usually referred to as *electronics thermal management* or *electronics cooling*.

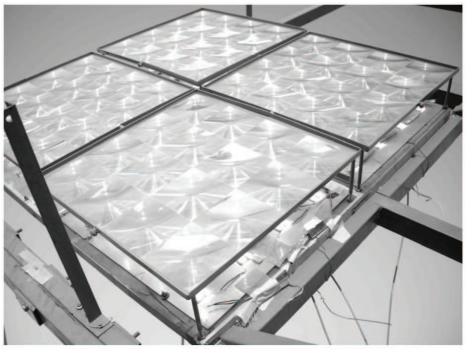
Previously, thermal management was usually an afterthought for integrated circuit


(a) Computers and Laptops

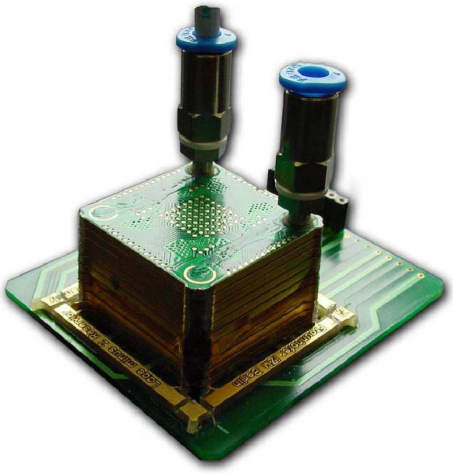

(b) Smart phones




(c) High power LEDs



(d) Concentrated photovoltaics



(e) Stacked electronic substrates

(f) Defense electronics

Figure 1.1: A diverse range of electronic systems and components where thermal management is a critical requirement.

(IC) design engineers, but that approach is no longer tenable. Pursuant to Moore's law, the number of transistors on a chip doubles every 18 months [3]. This increases the heat dissipated per unit area of the chip, which is further augmented by higher operating frequencies geared towards improving computation speeds. In addition to this, the number of chips in multi-chip modules and number of devices in small confined spaces in systems are increasing continuously [4]. All this has made thermal management a much more difficult problem to deal with, and conventional thermal management solutions such as conduction and natural convection are no longer viable for many modern electronic systems.

Figure 1.1 shows a diverse range of electronic systems and components where thermal management has become a critical design requirement. Computers and laptops, which occupy a big share of the consumer electronics market, have become much more powerful, compact, and lightweight [5]. Ultra-portable electronic devices, such as smart phones and tablet computers, are also generating more waste heat, while making it difficult to accommodate thermal management components due to their shrinking thicknesses. High power light emitting diodes (LEDs), which are fast replacing conventional sources of light, also dissipate large amounts of heat due to their low efficiencies $(15 - 30\%)$[6]. Although solar cells are one of the most promising sources of renewable energy, thermal management issues associated with high solar flux in concentrated photovoltaic systems are a major hurdle in the profitable implementation of this technology [7]. The use of three-dimensional integrated circuits,

which contain stacked electronic substrates, offers significant advantages in terms of improved electrical performance and reduced device footprint. However, since the heat has to travel a much longer distance across many interfaces, they suffer from significantly increased junction temperatures. Besides the consumer electronics market, the military and space sections need high-heat-flux thermal management technologies in order to cool such devices as gallium nitride-based power amplifiers, solid-state high energy lasers, and space solar power generation and propulsion subsystems [4].

## 1.2 Micro-Columnated Loop Heat Pipe

The process of waste heat removal from an electronic device involves providing a thermally-conductive pathway for the flow of heat from the heat source to an external heat sink. The junction temperature $T_j$ of the device is given by

$$T_j = T_c + \dot{Q} R_{th} \tag{1.1}$$

where $T_c$ is the temperature of the external heat sink, $\dot{Q}$ is the thermal power generated by the electronic heat source, and $R_{th}$ is the thermal resistance of the heat flow path from the heat source to the external heat sink. The conventional method of cooling hot electronic chips involves a conductive metal layer on the backside of the printed circuit board (PCB), which spreads the heat over a larger surface area for dissipation to the ambient by convection. In this method, the thermal resistance $R_{th}$ is usually high due to the limited thermal conductivity of the metal and the low

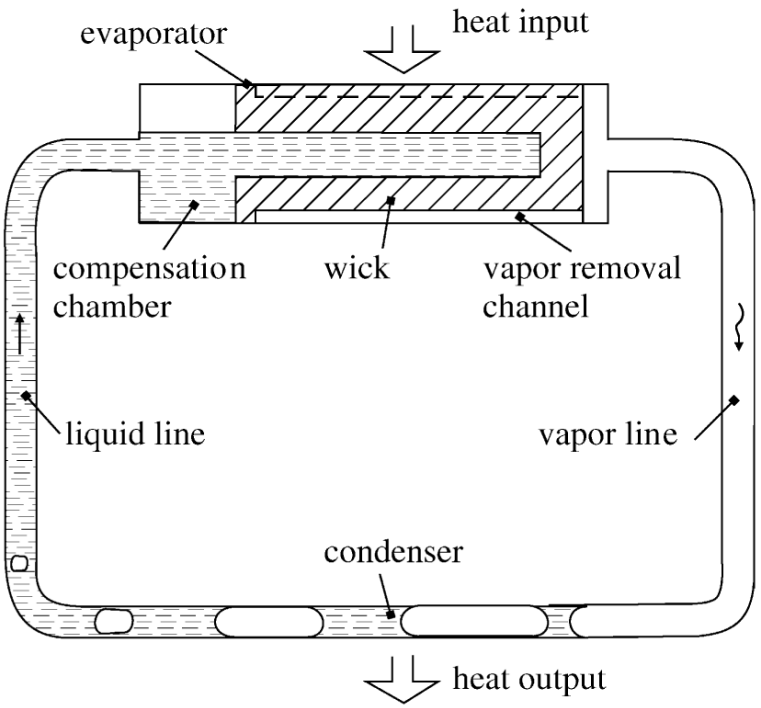



Figure 1.2: A schematic of the structure and principle of operation of a loop heat pipe (LHP) [1].

thermal convection coefficients associated with air cooling. Therefore, for high heat fluxes this approach is not suitable for keeping device junction temperatures within the safe operating limit.

Several advanced cooling techniques are currently being investigated as part of a major thrust towards tackling current and future thermal management challenges facing the electronics industry. Heat pipes, loop heat pipes, microchannel heat sinks, jet impingement, spray cooling, and thermoelectric devices are among the potential contenders for providing a high-heat-flux thermal management solution. All of these technologies, except heat pipes and loop heat pipes, are active systems that require

external power for operation. A loop heat pipe (LHP), shown schematically in Figure 1.2, is a passive, two-phase, high-heat-flux thermal transport system. Heat is absorbed in the evaporator section, resulting in evaporation of the working fluid. The vapor formed as a result travels to the condenser section, where heat is given off due to condensation. The condensed liquid is resupplied, via a compensation chamber, back to the evaporator, where the wicking structure generates a capillary pressure across the liquid/vapor interface, thus helping to drive the flow loop. The LHP was originally developed to improve the performance of heat pipes, which suffer from larger frictional flow pressure drops due to the fact that the liquid and vapor phases travel in the same conduit and the wick extends along the entire length of the device.

Conventional loop heat pipes are bulky devices fabricated out of cylindrical tubing [1]. Even the compact versions aimed at computers and laptops [8, 9, 8, 5] can only operate on the periphery of these systems, and are unsuitable for densely packed and stacked electronic substrates [10]. I propose a planar, ultra-thin, wafer-level microscale loop heat pipe to address the issue of localized cooling of high power, high heat flux electronics. Figure 1.3 shows a 3-D design schematic of the micro-columnated loop heat pipe ($\mu$CLHP). The device is designed for fabrication on a three-layer wafer stack. Most of the device components can be etched on both sides of the middle silicon wafer (layer 2), which is capped on the top and bottom by silicon and Pyrex wafers, respectively. The middle silicon wafer will have coherent porous silicon (CPS) pre-patterned on it to serve as the base for a vertically-wicking

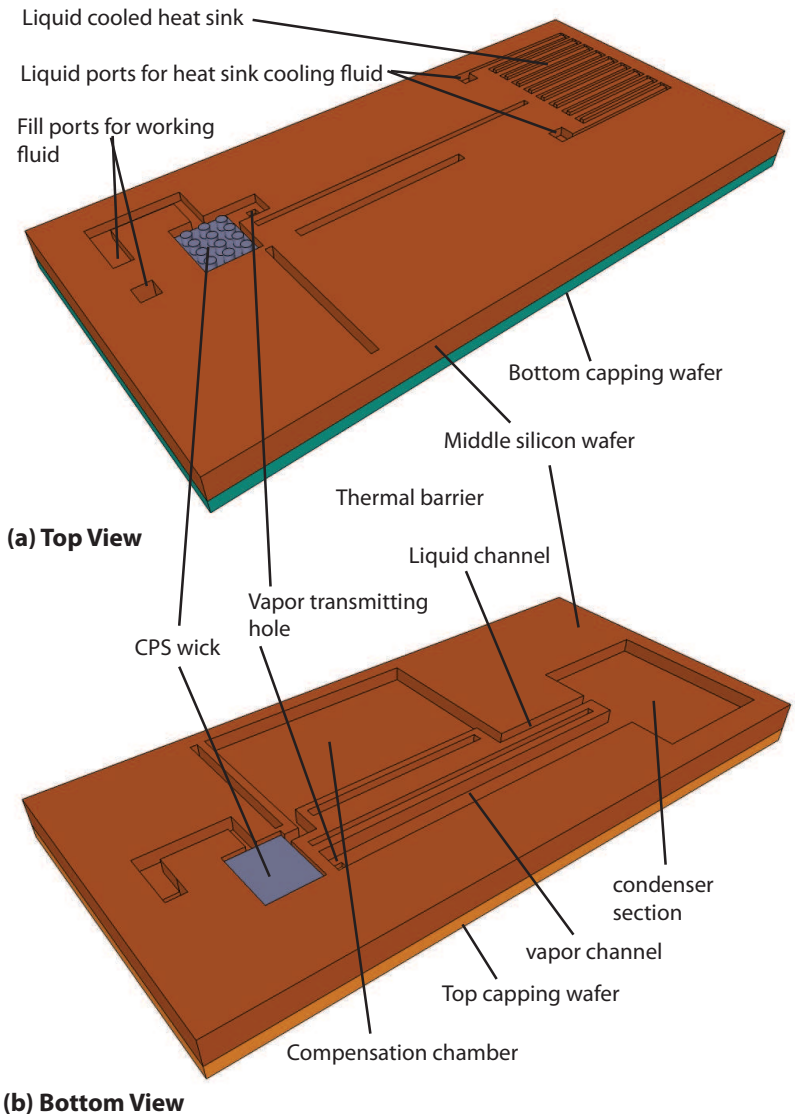



Figure 1.3: A schematic of the proposed micro-columnated loop heat pipe ($\mu$CLHP), designed for fabrication on silicon and Pyrex substrates.

micro-columnated wicking structure. The columnated primary wick interfaces with the secondary evaporator wick patterned on the top silicon capping wafer (see Figure 1.3(a)). The vapor and liquid transport channels and the condenser section are etched on the bottom of the middle silicon wafer (see Figure 1.3(b)). Vapor generated in the evaporator will enter the vapor channels via a vapor through-hole and travel

to the condenser section, which can be cooled by an in-built liquid-cooled heat sink patterned above it. The condensed liquid will travel, via the liquid channel, back to the evaporator, where it feeds into the bottom of the primary CPS wick via a liquid feeding cavity. Holes in the top capping wafer provide access to the inlet and outlet fill-ports, which can be used to degas and fill the device with the working fluid.

## 1.3 Outline

This report deals with the various design and fabrication aspects of the proposed $\mu$CLHP device. The micro-columnated wick is by far the most important component of the device. It is not only the place where evaporation takes place, but is also responsible for generating capillary suction forces that drive the flow loop. In chapter 2 is provided the design and theory of operation of the micro-columnated wick, and the various topological considerations that affect the design of the evaporator section are also discussed. Coherent porous silicon (CPS) is the base material for the fabrication of the micro-columnated wick. Chapter 3 deals with the theory and experimental methods for obtaining CPS by electrochemical etching of silicon. Chapter 4 proposes a detailed fabrication process flow for the $\mu$CLHP device, and discusses the various issues pertaining to the use of CPS in standard MEMS microfabrication processes. Chapter 5 concludes the report by providing a summary of the work and discussing future work.

# Chapter 2

# Micro-Columnated Wicking Structure

The coherent porous silicon (CPS)-based dual scale micro-columnated wicking structure can be considered the most important component of the proposed micro-columnated loop heat pipe ($\mu$CLHP). It provides the necessary capillary forces for driving the device flow loop and also ensures proper thin-film evaporation of the working fluid in the evaporator section. In this chapter, are found the design details of the micro-columnated wick, its theory of operation, and the evaporator topological considerations that influence the performance of the wick.

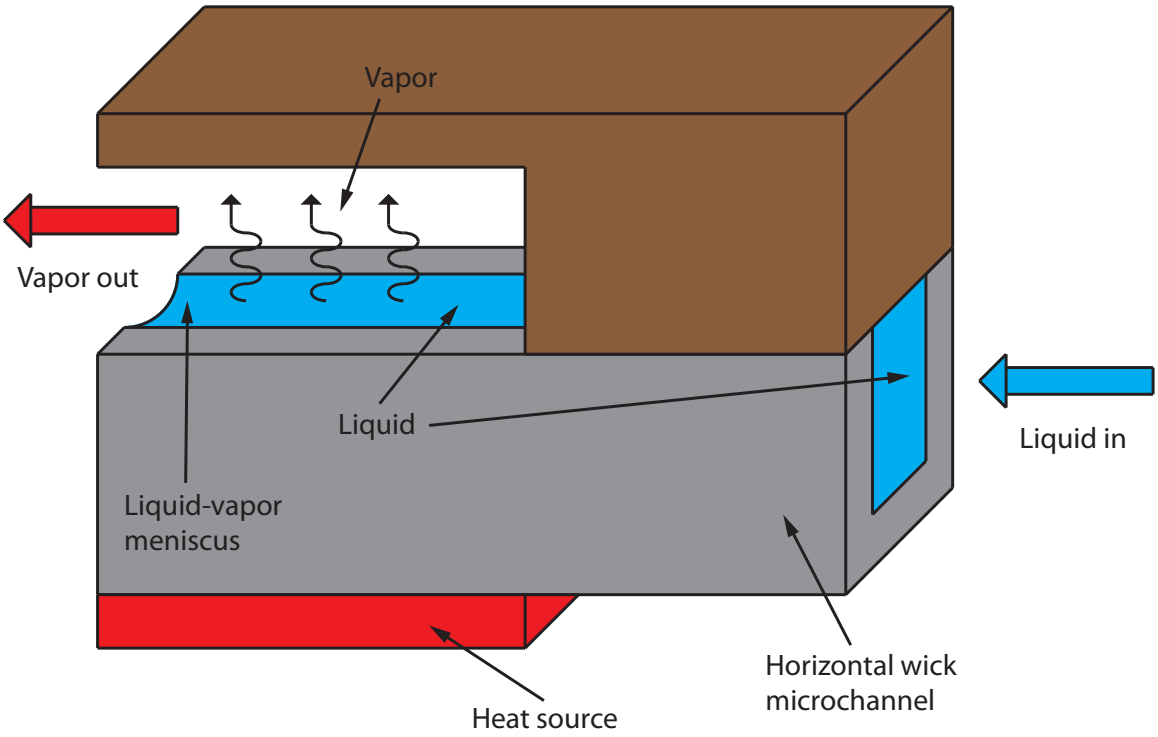



Figure 2.1: A schematic of the in-plane wicking structure employed in some MEMS-based loop heat pipes.

## 2.1 Wick Design

There are a number of design requirements that a wicking structure for the $\mu$CLHP device must satisfy. First, in order to ensure compatibility with the fabrication processes for the $\mu$CLHP device, the wick should be fabricated out of the same substrate material. This is important, since there is no way to conveniently handle conventional wicking materials such as wire meshes or sintered metal powders in MEMS microfabrication processes. Being able to fabricate the wick completely out of silicon is very important from the viewpoint of device integration. The second design requirement has to do with the operational and performance characteristics of the wick. Some of

the previous work in this field has seen the use of planar in-plane wicking structures [11, 12, 13, 14, 15, 16, 17], which are inefficient and prone to failure due to wick dry-out at relatively moderate heat flux values. As shown in Figure 2.1, the liquid comes into the in-plane wick laterally, and this leads to a non-uniform supply of liquid to the evaporating thin-film meniscus in the wick microchannels. The region of the wick farther away from the liquid inlet is prone to dry-out. A wick topology is desired that leads to uniform supply of liquid to the evaporating surface.

Figure 2.2 shows a 3-D design schematic of the micro-columnated wicking structure that has been proposed for the $\mu$CLHP device. This CPS-based micro-columnated wick has two main design features: (a) it is designed to be fabricated completely out of silicon, and (b) it operates by wicking the liquid vertically onto the evaporating surface, to ensure a uniform liquid supply over this surface. The wick has a dual-scale topology, with a CPS-based primary wick designed to generate large capillary forces and a secondary wick interfaced with the heat source to maximize the rate of liquid thin-film evaporation. The primary wick is fabricated by first electrochemically etching micron-sized vertical pores into the surface of the silicon wafer, followed by deep reactive ion etching (DRIE) of vertical columns into this coherent porous silicon (CPS) base material. The secondary wick consists of micron-sized rectangular channels etched onto a separate silicon wafer, which is then bonded to the wafer containing the primary CPS wick. This creates a vapor chamber between the columns of the primary CPS wick and the flat micro-patterned surface of the secondary wick.

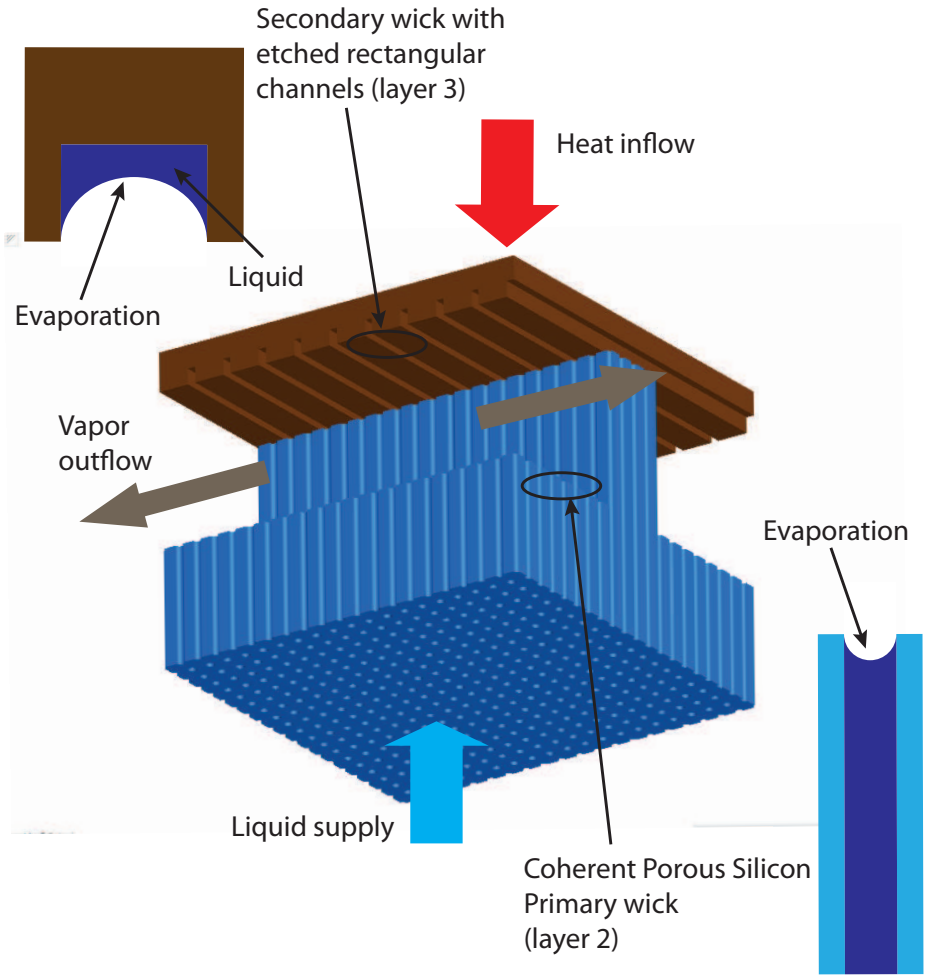



Figure 2.2: A 3-D schematic of the micro-columnated wick showing the primary and secondary parts of the dual scale wick.

## 2.2 Wick Theory of Operation

The micro-columnated wick uses a two-fold approach for supplying liquid to the evaporator section of the $\mu$CLHP and implementing liquid-to-vapor phase change. As shown in Figure 2.2, the micron-sized pores of the primary CPS wick absorb the liquid coming in from the compensation chamber, on account of the large capillary forces across the liquid-vapor menisci in these pores. The capillary suction pressure

generated in the pores is given by

$$\Delta P_c = \frac{2\cos\theta}{r}\sigma \tag{2.1}$$

where $r$ is the radius of the wick pores, $\sigma$ is the surface tension of the liquid, and $\theta$ is the contact angle. The liquid completely saturates the pores of the primary CPS wick and also travels into the microchannel patterns etched onto the surface of the secondary wick, via the columns of the primary wick in contact with this surface.

This results in the formation of two different kinds of liquid-vapor interfaces, one in the pores of the primary wick and another in the rectangular microchannels of the secondary wick. Thin-film evaporation can occur from both these interfaces, but the wick design dimensions are optimized to maximize the rate of evaporation from the secondary wick, while employing the primary wick mainly to ensure constant liquid supply via capillary action. As a result, the pores of the primary wick will in general be smaller than the width/depth of the secondary wick microchannel patterns, since smaller pore size increases capillary pressure but decreases the rate of evaporation. The micro-columnated wick designed in this manner will not only help to maximize the rate of evaporation, but also help to prevent catastrophic wick dry-out at high heat fluxes. The vertical wick topology will ensure uniform supply of liquid to the secondary wick surface, which is optimized for enhanced rates of thin-film evaporation. At high heat fluxes, the secondary wick will dry-out due to its smaller capillary suction characteristics. At this point, the primary wick, which is less prone to dry-out due to its small pore size, will take over. It will ensure absorption of the incoming heat flux

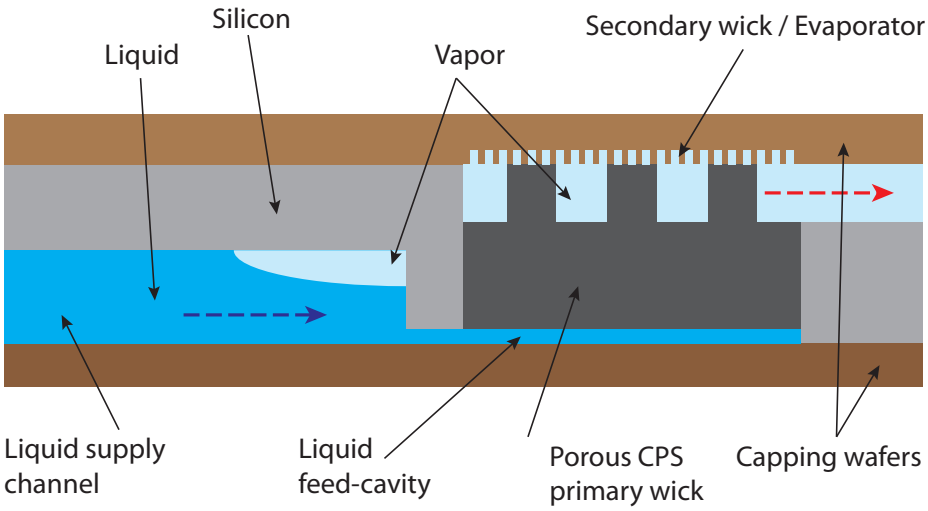



Figure 2.3: A 2-D schematic of the coherent porous silicon (CPS)-based micro-columnated wicking structure and its topological arrangement with respect to the device operator and compensation chamber.

by virtue of evaporation from its pores, albeit at high values of the wall superheat.

## 2.3 Evaporator/Wick Topological Considerations

The arrangement of the micro-columnated wick within the device evaporator, and the overall evaporator topology are very important to ensure that evaporation proceeds in the vapor chamber as expected, and no vapor intrusion into the liquid supply takes place. Figure 2.3 provides a 2-D cross-sectional view of the evaporator section of the proposed $\mu$CLHP device. We see that the micro-columnated wick lies in the evaporator section, and straddles the middle silicon wafer, which contains the primary CPS wick, and the top silicon capping wafer, which contains the secondary micro-patterned wick. However, a third capping wafer is required underneath the primary CPS wick, to form a thin liquid cavity that feeds the working fluid to the

CPS pores. This liquid cavity must be extremely thin in order to prevent any vapor bubble nucleation and growth, which will effectively disrupt the liquid supply to the wick. Vapor formation in this cavity is a concern due to parasitic heat flow across the extremely thin CPS wick. However, the required superheat for bubble nucleation and growth increases as a liquid cavity is constrained, which should prevent vapor formation in an extremely thin ($\sim 50\,\mu m$) liquid feed-cavity.

The liquid feed-cavity is connected to the liquid compensation chamber by a narrow (and thus high thermal resistance) channel, in order to minimize parasitic heat flow to the liquid in it. This is essential in order to prevent excessive vapor formation in the compensation chamber. The liquid supplied to the liquid feed-cavity by the compensation chamber is absorbed by the CPS pores of the primary wick, and transported to the secondary micro-patterned wick surface for thin-film evaporation. The vapor formed as a result collects in the vapor chamber and diffuses out into the vapor transport channels.

# Chapter 3

# Coherent Porous Silicon (CPS) Etching

To fabricate the micro-columnated wicking structure, it is necessary to first obtain coherent porous silicon by electrochemical etching of silicon. In this chapter are presented the theory, experimental setup, and preliminary results concerning the electrochemical etching of silicon for obtaining a porous structure that can form the base of the micro-columnated wick.

## 3.1 Theory of Electrochemical Etching of Silicon

Figure 3.1 illustrates the physics behind the electrochemical etching of silicon, as originally proposed by Lehmann *et al.* [2, 18]. Minority carriers can be generated either by illumination or by using a high electric field, leading to the formation of a

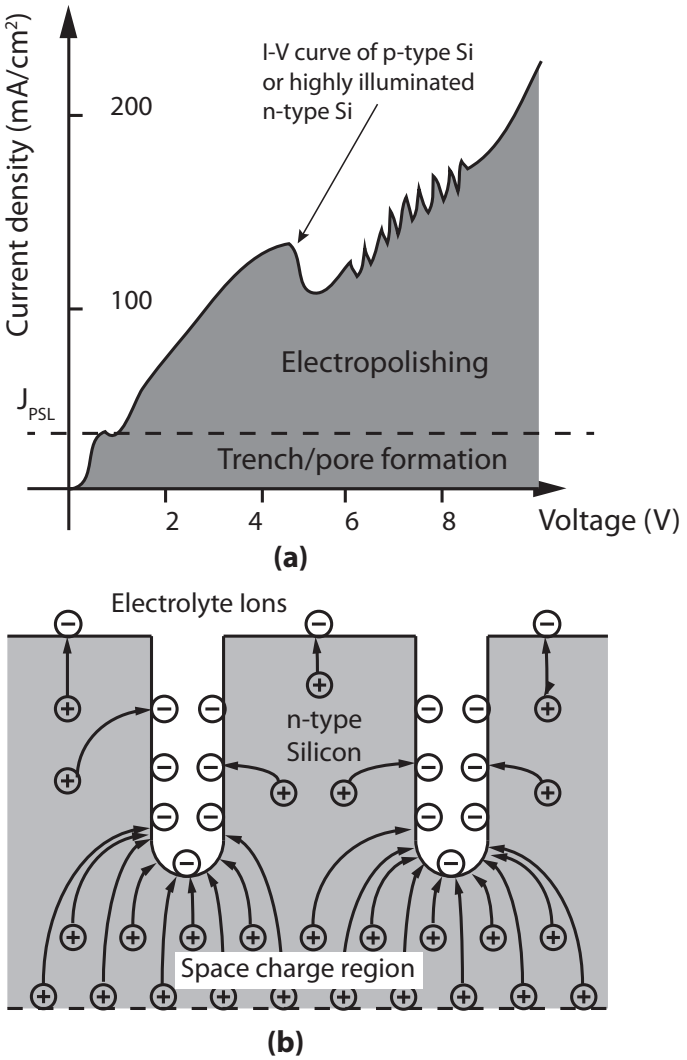



Figure 3.1: The physics of electrochemical etching of n-type silicon under anodic biasing [2]: (a) Plot of the anodic bias voltage against the measured photocurrent. Trench or pore formation is observed for current densities below $J_{PSL}$. (b) Schematic of the electric field lines in the silicon space charge region during anodization in a hydrofluoric acid electrolyte.

space charge region.In Figure 3.1, the electrochemical etch current density is plotted against the applied voltage for an anodically biased silicon wafer. It is seen that a p-type Si wafer and a highly illuminated n-type Si wafer exhibit almost the same I-V curve. For the n-type wafer, the photocurrent can be varied by changing the

illumination intensity, to cover almost the entire area under the curve. It is observed experimentally that for current densities less than $J_{PSL}$ a porous silicon layer (PSL) is formed on the surface of silicon, and hence the name. For $J < J_{PSL}$ trench/pore formation is observed on the wafer, while for $J > J_{PSL}$ the surface of the wafer undergoes electropolishing. This can be explained based on the electric field lines and space charge distribution inside an anodically biased n-type silicon wafer immersed in an electrolyte, as shown in Figure 3.1b. Under anodic bias, the holes in the silicon wafer ($h^+$) combine with the negative $F^-$ ions available in the electrolyte, to cause the etching of silicon. If there is an excess of holes, as in p-type silicon, the diffusion-controlled flow of active ions becomes the rate determining step, and the top surface of silicon is etched faster than the deeper trenches, which leads to electropolishing. For low photocurrents, the availability of holes becomes the rate determining step, and in the case of a backside illuminated wafer most of them are collected by the trench tips from the deeper space charge region. This leads to electrochemical trench etching where the trench formation is random. It can be made ordered by first etching pyramidal etch pits using a silicon oxide mask and KOH etching, followed by electrochemical etching.

## 3.2 Experimental Etching Setup

Figure 3.2 shows the electrochemical etching setup that was implemented in order to obtain coherent porous silicon from a plain silicon wafer. A <100> n-type

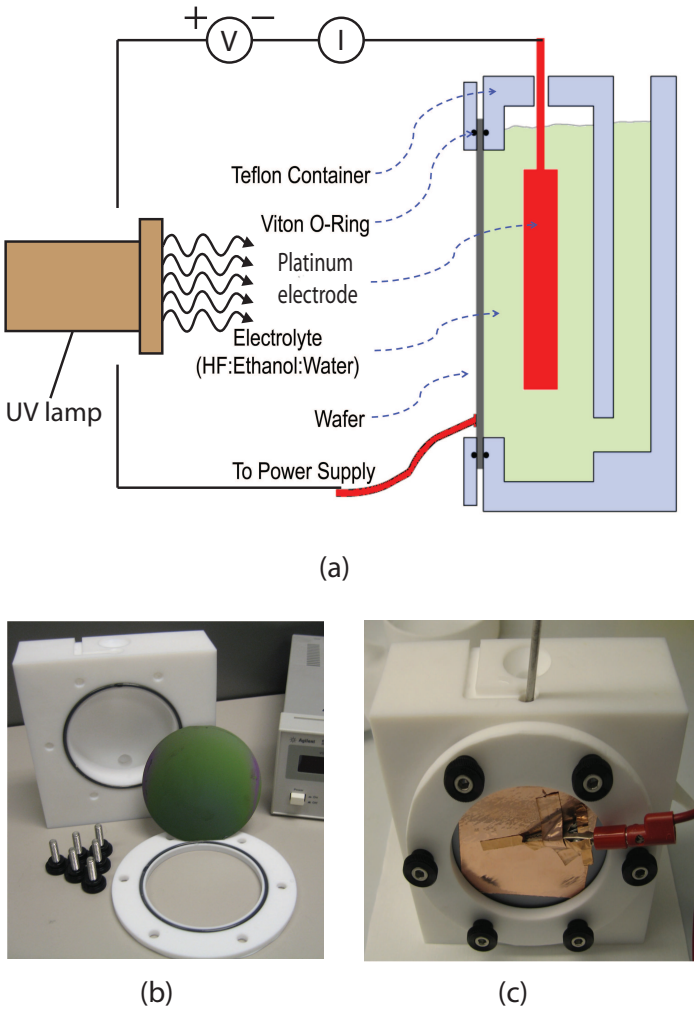



Figure 3.2: The wafer-level electrochemical etching setup designed for the fabrication of coherent porous silicon from a plain $< 100 >$ silicon wafer: (a) The front of the wafer is exposed to the electrolyte in a machined Teflon container, in the presence of an anodic bias and backside illumination. (b) The components of the Teflon etching container. (c) The assembled Teflon etching container, with the positive and negative electrodes.

silicon wafer is exposed to an electrolyte (hydrofluoric acid) inside a machined Teflon container. The wafer is clamped using a Viton O-ring, with its front side in contact with the electrolyte and its backside exposed. The wafer is anodically biased with a voltage source, while a platinum wire dipped in the HF solution acts as the

negative electrode. Current in the circuit is also measured. Backside illumination of the wafer, using a lamp and appropriate optical filters, is recommended as the best method for obtaining vertical cylindrical pores [2]. A good ohmic contact to the silicon wafer needs to be established in order to provide a uniform potential across the wafer. When working with smaller samples, a Ga-In Eutectic can be rubbed on parts of silicon not being etched, for obtaining an ohmic contact [2]. For a larger wafer, ideally, the backside of the wafer should be doped in order to create an ohmic contact. A less desirable alternative is to deposit a thin metal layer on the back, but this can potentially block the light coming from the backside illumination source. The use of 2.5 weight percent (w/o)(= 1.25 $M/kg$) hydrofluoric acid (with a few drops of a wetting agent) as an electrolyte has been reported in literature [2]. The solution must also be stirred gently in order to remove hydrogen bubbles from the silicon surface.

## 3.3 Preliminary Etching Study

In order to obtain a coherent porous silicon base with accurately controlled pore diameters and trench topology, the relevant process parameters need to be properly studied and documented. In this study, preliminary die level experiments were conducted to understand the dynamics of the etching process.

Figure 3.3a shows a simple die level electrochemical etching setup that was implemented without a controlled illumination source. A platinum cathode is dipped in a 25% hydrofluoric acid solution contained in a Teflon dish at room temperature.

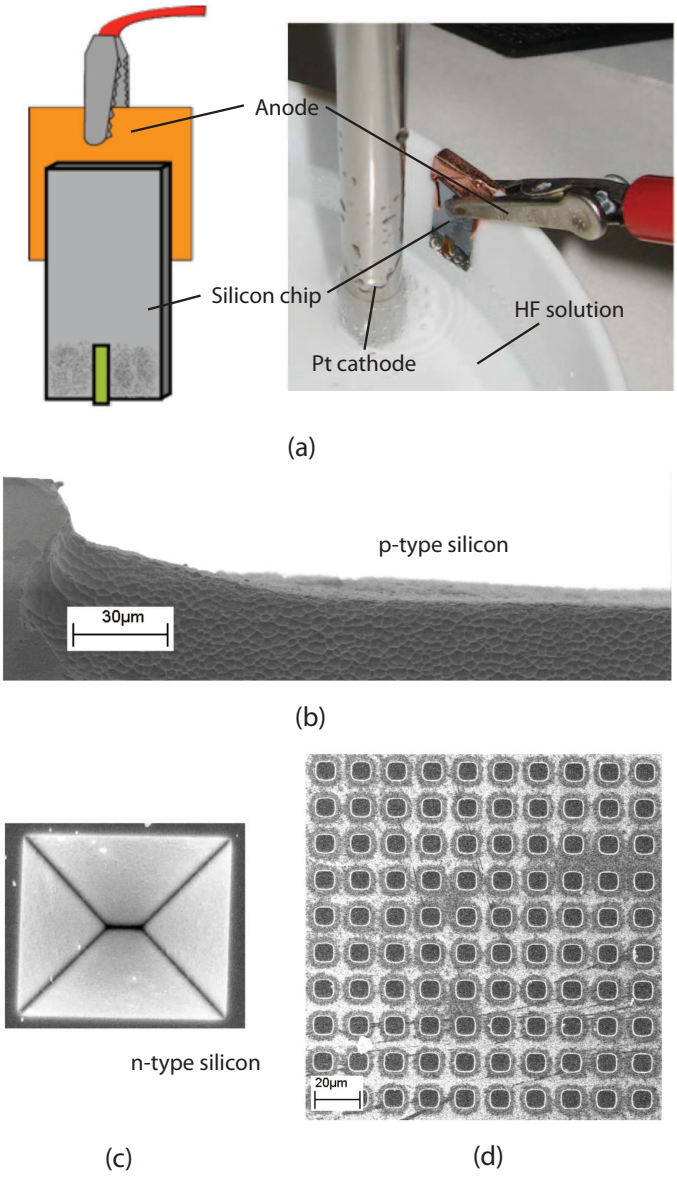



Figure 3.3: Preliminary electrochemical etching results obtained without the use of a controlled illumination source: (a) A simpler die level CPS etching setup for etching p-type and n-type silicon dies in 25% hydrofluoric acid. (b) Un-patterned electrochemical etching of p-type silicon yields a random array of pits. (c) A single $8 \times 8\,\mu m^2$ pyramidal trench from an array of trenches obtained by KOH etching of n-type silicon. (d) Coherent pores obtained by electrochemically etching the n-type silicon die with KOH trench pits.

Anodic bias is applied, using an alligator chip, to the silicon die dipped in the electrolyte. Both p-type and n-type silicon samples were etched, with and without the use of pre-patterned etch pits. Figure 3.3b shows that a random array of shallow pits are obtained after etching a plain p-type silicon substrate, with most of the etching happening on the surface. This result agrees with the theory of electrochemical etching, which predicts electropolishing of substrates with excess supply of holes ($h^+$). Figs. 3.3c-d show electrochemical etching results for a n-type silicon substrate that had pre-patterned pyramidal etch pits obtained by KOH etching. Although backside illumination was not used, some amount of trench etching was observed, with the etching taking place preferentially in the pits.

# Chapter 4

# Wick and Device Fabrication

In this chapter is outlined the detailed fabrication process flow for the proposed micro-columnated loop heat pipe ($\mu$CLHP). Several issues that could potentially arise in the implementation of this process flow are also discussed.

## 4.1 Fabrication Process Flow for the $\mu$CLHP

Figure 4.1 shows the detailed fabrication process flow for the $\mu$CLHP, which integrates the fabrication of the coherent porous silicon (CPS)-based micro-columnated wick with the fabrication process for the rest of the device components. The device will be fabricated using two silicon wafers and one Pyrex wafer, with most of the processing done on the middle silicon wafer. Etching most of the device components on both sides of the middle silicon wafer minimizes any requirements regarding its alignment with the top and bottom capping wafers.

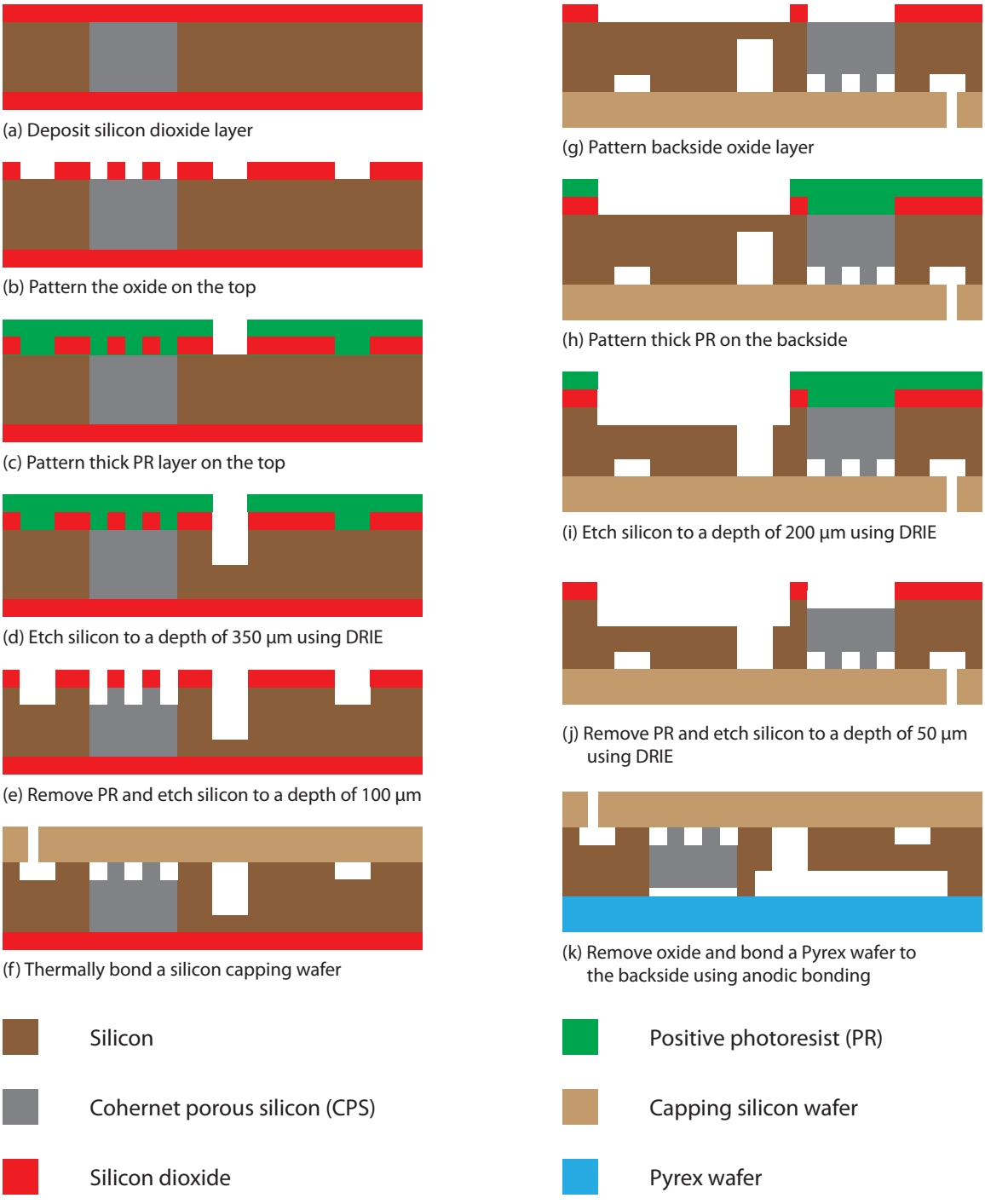



Figure 4.1: Fabrication process flow for the micro-columnated loop heat pipe ($\mu$CLHP), which employs a coherent porous silicon (CPS)-based micro-columnated wicking structure.

The process starts with a 6-inch <100> silicon wafer that has undergone patterned illuminated electrochemical etching, to completely convert the silicon in the evaporator region of the $\mu$CLHP to CPS. The details regarding this process were discussed in chapter 3, and once the process parameters have been characterized they can be appropriately set to yield the required pore size for the CPS material.

The wafer is piranha-cleaned to remove organic impurities and dipped in HF to remove the native oxide layer. Following this, the wafer is thoroughly rinsed in water and dried. A low pressure chemical vapor deposition (LPCVD) process is used to deposit a 2 $\mu m$ thick silicon dioxide layer in a $450^oC$ thermal furnace (Figure 4.1(a)). A phosphorous-doped low temperature oxide (LTO) recipe should be employed, which yields phospho-silicate glass (PSG). Because it reflows at high temperatures, the thickness of the PSG layer can be made more uniform, and its stress reduced, by annealing it at $1000^oC$ for a few hours in a thermal furnace.

Following this, the wafer is piranha cleaned, treated with HMDS for better photoresist adhesion, and deposited with a $3\mu m$ thick layer of G-line positive photoresist. The photoresist is exposed to UV light using the first mask and developed. This patterns features that are to be etched onto the topside of this middle silicon wafer (see Figure 1.3), including the columnated vapor chamber, the channels connecting the vapor chamber to the fill-ports and the vapor transmitting hole, the thermal barriers, and the liquid-cooled heat sink microchannels above the condenser section. The photoresist should be then hardbaked in a $120^oC$ oven for about 2 hours. Using the pat-

terned photoresist as the etch mask, the underlying oxide layer is etched in a plasma etching system. The hardbaked photoresist is then removed by dipping the wafer in a hot photoresist stripping solution (PRS-3000) for 12-24 hours (Figure 4.1(b)).

The wafer is once again cleaned in a piranha solution and treated with HMDS. A 10 $\mu m$ thick G-line photoresist layer is deposited, exposed to UV light using the second mask, and developed, which patterns the thermal barriers and the vapor transmitting hole (Figure 4.1(c)). The photoresist is hardbaked at $120^oC$ for 2 hours, and then used as an etch mask for deep reactive ion etching (DRIE) of the silicon wafer to a depth of approximately $350\mu m$ (Figure 4.1(d)). The hardbaked photoresist is removed using the photoresist stripper and the wafer is piranha-cleaned. The wafer is also dried in a $120^oC$ oven for a few minutes to ensure the removal of water from the CPS pores. Using the oxide layer as the etch mask, the silicon wafer is etched to a depth of approximately $100\,\mu m$ (Figure 4.1(e)). This etches the columnated vapor chamber and all the other features on the top surface.

A 6-inch silicon capping wafer is now thermally (or using a eutectic) bonded to the top surface of the middle silicon wafer (Figure 4.1(f)). This capping wafer has the secondary wick, thermal barriers, and through-etched holes (obtained using DRIE), which align with the fill-ports on the middle silicon wafer. The device is now turned upside-down and the backside oxide is plasma-etched using a patterned $3\,\mu m$ G-line photoresist as the etch mask (Figure 4.1(g)). This patterns the condenser section, the liquid feed cavity, the thermal barriers, and the vapor transmitting hole. Another

6 $\mu m$ G-line photoresist layer is patterned in order to etch all the above features except the liquid feed-cavity (Figure 4.1(h)). Using this hardbaked photoresist as the etch mask, the backside of the silicon wafer is etched to a depth of approximately 200 $\mu m$ using DRIE (Figure 4.1(i)). Following this, the photoresist is removed using a dry-etching process, and the silicon is etched further to a depth of 50 $\mu m$ using the oxide as an etch mask (Figure 4.1(j)). After this step, the thermal barriers should have etched through the entire middle wafer and the vapor transmitting hole should have reached the vapor transport channels. A shallow 50 $\mu m$ liquid feed-cavity also forms underneath the primary CPS wick.

The backside oxide is now removed using plasma etching. Note that it is advisable to avoid wet etching processes for removing the photoresist in Figure 4.1(i) and the oxide in Figure 4.1(j) due to the fact that the liquid reagents might get trapped inside the device components. The two-wafer stack is now bonded to a bottom Pyrex wafer using anodic bonding at $350^oC$ and 1000 $V$. Prior to this process, the bonding surfaces must be properly cleaned to remove particulate matter that might prevent proper contact between the surfaces.

## 4.2 Potential Fabrication Problems/Challenges

Several issues can potentially arise during the implementation of the microfabrication process flow outlined above. The alignment of the two silicon wafers during the bonding step in Figure 4.1(f) requires some sort of alignment marks on the back-

side of the middle silicon wafer. These alignment marks can be created by shifting the backside oxide etching step in Figure 4.1(g) to the beginning of the process flow (i.e. before Figure 4.1(b)). But this could potentially expose the CPS material to oxidizing gases during the thermal bonding of the silicon wafer in Figure 4.1(f). An alternate solution would be to perform the alignment in Figure 4.1(f) using a light source to which silicon is transparent.

Another issue concerns the wet processing of wafers the after wafer bonding step in Figure 4.1(f). It will have to be seen if wet etching of the oxide and photoresist etch masks, and the cleaning in piranha solution will cause any problems due to liquid intrusion into the enclosed device cavities. Although photoresist and oxide removal in Figure 4.1(i) and Figure 4.1(j), respectively, can be done using dry etching techniques, the cleaning of the wafers prior to anodic bonding in Figure 4.1(h) most likely will have to be performed using a piranha solution.

# Chapter 5

# Summary and Conclusions

This report dealt with the design and fabrication of a micro-columnated loop heat pipe ($\mu$CLHP) that employs a novel vertically-wicking dual-scale micro-columnated wicking structure for improved device performance. In chapter 1 was outlined the importance of this work in terms of the thermal management requirements of a host of modern electronics devices and systems. An overview of the structure and principle of operation of the $\mu$CLHP was also provided. In chapter 2 was presented the design and topological characteristics of the dual-scale micro-columnated wicking structure, which is by far the most important $\mu$CLHP design component. It was shown how this vertical out-of-plane wick topology helps to not only enhance the rate of thin-film evaporation, but also prevents wick dry-out under sudden large heat fluxes.

Since the micro-columnated wick has to be fabricated out of coherent porous silicon (CPS), chapter 3 dealt with the theory and experimental details of illuminated

electrochemical etching of silicon. It was shown how, by changing the process parameters, the etch characteristics of the process can be modified. In chapter 4 was provided a detailed microfabrication process flow for the $\mu$CLHP device. The complexity of this process can be mainly attributed to the presence of the CPS wick. Potential challenges to the implementation of this fabrication process were also noted.

Future work on this topic should involve a detailed characterization of the coherent porous silicon etching process, using the experimental setup discussed in chapter 3. Once it becomes possible to pattern a CPS base on a silicon wafer, the next step will be to implement the $\mu$CLHP fabrication process flow outlined in chapter 4.

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