Effectiveness of Strain Solutions for Next-Generation MOSFETs

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Technical Report No. UCB/EECS-2012-223
http://www.eecs.berkeley.edu/Pubs/TechRpts/2012/EECS-2012-223.html

December 1, 2012

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By

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A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering - Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

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Spring 2012

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Abstract

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The conventional planar bulk MOSFET is difficult to scale down to sub-20nm gate length, due to the worsening performance variability and short channel effects. Thin body transistors, including Multiple-Gate (FinFET & Tri-Gate FET) and Fully Depleted SOI (FD-SOI) MOSFETs are anticipated to replace the current transistor architecture, and will be used in future CMOS technology nodes. Strained Silicon technology is widely used today to boost planar bulk transistor performance. Thus it's technically important to examine the strain-induced performance enhancement in these thin body transistors, for nanometer scale channel length. A comprehensive study on impact of channel stress on ultra-thin-body FD-SOI MOSFETs is presented. It's found that strain-induced mobility enhancement diminishes with Silicon body thickness scaling below 5nm for electrons, but not for holes. Strain-induced carrier transport enhancement is maintained with gate-length scaling. By applying forward back biasing (FBB) through the ultra-thin Buried Oxide layer, both carrier mobilities and their responses to strain get enhanced. For Multiple-gate FETs, the impact of performance enhancement through various types of stressors (including CESL, SiGe Source/Drain, Strained SOI and Metal Gate Last process) is studied, for different fin crystalline orientations and aspect ratios, to provide guidance for 3-D transistor design optimization.

To my parents for their unbounded love and support.

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Acknowledgements

First and foremost, I would like to express my deepest gratitude to my research advisor, Professor Tsu-Jae King Liu, who is a great mentor and guided me from the unsure beginning as a fresh researcher to the bleeding-edge in my field of study. She has always been cordial, attentive, responsible and supportive throughout all the peaks and valleys during my whole Ph.D. journey. There is much about her supervision and management style that I would like to learn and to bring with me in my future careers.

I am grateful for all the support and advices of Professor Andrew Neureuther, chairing my qualifying examination and serving as a member of my dissertation committee. His keen perspective on Technology CAD tool development was exceptionally helpful, and his sincere advice on leading my research opportunities toward a very meaningful contribution in the device and manufacturing interdisciplinary field. I also thank Professor Sayeef Salahuddin and Professor Paul Wright for serving on both my qualifying examination committee and my dissertation committee.

Dr. Lee Smith served as a mentor during my internship period at Synopsys in 2010. His firm and rigorous semiconductor band structure and transport knowledge has provided a great learning experience for me. His experience in semiconductor industry was also helpful for developing my future career. Dr. Koen Martens served as a mentor during my visiting scholar stay at imec in 2011. For the first time, I learned about basic heat transport theories from him and during my visit at Leuven, Belgium I had received really lots of help from him, on both research and life.

I would like to thank all my research partners with regards to this thesis work. With Dr. Xin Sun (IBM), Dr. Lynn T.-N. Wang (Globalfoundries) and Byron Ho, I could perform my research more elaborately. They provided the kindest assistance (especially during the conference deadlines) and countless great discussions on strain-induced enhancement in MOSFETs, advanced transistor structures, and semiconductor process issues.

This work has been funded through a few sources, such as the UC Berkeley Graduate Fellowship and the UC Discovery Grant ele07-10283 under the IMPACT program. In addition, fabrication of the test chips for studying advanced thin-body MOSFETs was done and donated by Texas Instruments (Dr. Weize “Wade” Xiong), CEA-LETI Minatec (Dr. François Andrieu, Dr. Olivier Faynot, Dr. Olivier Weber, Dr. Thierry Poiroux), imec (Dr. Nadine Collaert, Malgorzata Jurczak) and Soitec (Dr. Carlos Mazuré and Mrs. Bich-Yen Nguyen). Dr. Victor Moroz and Dr. Munkang Choi from Synopsys also contributed in the FinFET channel stress study. I would like to express my sincere gratitude for their technical and intellectual supports, and I am looking forward to continuing the collaborations with them in future.

In addition to the above, several others have provided assistance. Dr. Changhwan Shin (Univ. of Seoul), Dr. Darsen Lu (IBM), Dr. Vincent Pott (IME, ASTAR), Dr. Renaldo Vega (IBM), Dr. Louis Hutin, Dr. Jaeseok Jeon (Rutgers Univ.), Dr. Hei "Anderson" Kam (Intel), Min Hee Cho, Rhesa Nathanael, Nattapol Damrongplasit, Zachery Jacobson, Wookhyun Kwon, Sung Hwan Kim, Peter Matheu, Eung Seok Park, I-Ru "Tim" Chen, Yenhao "Philip" Chen, Jack Yaung, Feng Pan, Dr. Jiezhi Chen (Tokyo Univ.), Yi-Bo Liao (National Cheng Kung Univ.), Daniele Leonelli (imec), Yaohua Tan (Purdue Univ.), Zhaoyi Kang, Lu Ye, Ying Qiao, Dr. Ya-Mei Chen (Lam Research), Dr. Kun Qian (Globalfoundries), Dr. Chenlu Hou (McKinsey), Dr. Qiang Lu (Synopsys), Dr. Jing Xue (Synopsys), Dr. Hiu-Yong Wong (Synopsys), Weijian Yang, Xiao Sun (Yale Univ.), Shimeng Yu (Stanford Univ.), Yi Wu (Stanford Univ.), Chen Chen (Stanford Univ.), Yang Fu (Univ. of Virginia), Ben Niu (Purdue Univ.), Dr. Yuhui He (Osaka Univ.), Lang Zeng (Peking Univ.), Yuning Zhao (Notre Dame Univ.), Yangyin Chen (imec), Yan Li (imec) have also provided technical, educational and personal assistance in some form. I appreciate all of their sincere help.

Finally, I would like to thank my parents, whom I can never thank enough for their unselfish and unbounded love and never-ending supports. Their love will forever hold a special place in my heart.

Chapter 1

Introduction

Historically, the continuous miniaturization of the conventional planar bulk metal-oxide-semiconductor Field-effect transistor (MOSFET) by simply scaling the device dimensions has been effective to provide for steady improvements in integrated circuit (IC) performance and cost per function with every technology node. However, the planar bulk MOSFET is difficult to scale down to sub-20nm gate length, due to the worsening performance variability and short channel effects. Thin body transistors, including Multiple-Gate and Fully Depleted SOI MOSFETs are anticipated to be used in future CMOS technology nodes. Strained Silicon technology is widely used today to boost planar bulk transistor performance. Thus it's technically important to examine the strain-induced performance enhancement in these thin body transistors, for nanometer scale channel lengths.

In this chapter, the effects of strain on the Silicon band structure and carrier mobility are discussed, for both bulk materials and MOSFET inversion layers, to reveal the physical mechanisms of performance enhancement. Next, various stressor technologies are described, from a fabrication process point of view, to show how strain is introduced into commercial IC devices. Then advanced planar bulk and thin-body MOSFET structures with strain as a performance booster are analyzed to see the strain-induced performance enhancement in aggressively scaled devices. Finally, the motivation of this thesis and a brief overview of the remaining chapters is provided.

1.1 Semiconductor Band Structure and Carrier Mobility

1.1.1 Strain Effect on Semiconductor Band Structures

Since mechanical strain reduces crystal symmetry, it will affect the crystal band structure. For example, strain which lowers the crystal symmetry lifts band degeneracies; on the other hand, the breaking of symmetry also causes band warping and hence results in carrier effective mass change [1].

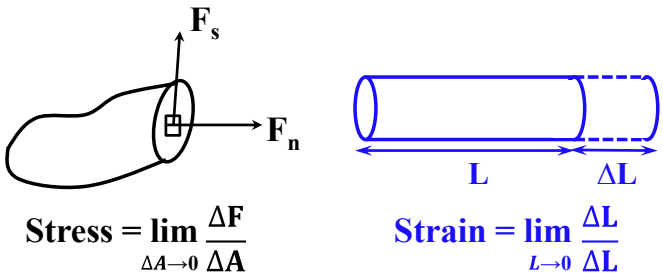

Figure 1.1. Definition of Stress and Strain in elastic mechanics, from [2].

To study strain in crystals, Elastic mechanics provide the general methodology to solve stress/strain problems in solid matter. When an external force load is applied to an object, there will be stress formed inside it. This results from the repulsive electromagnetic force between ionic cores when the lattice atoms deviate from their equilibrium positions. The definition of stress is the inside force per unit area, when the observing area is infinitesimally small. The strain mainly denotes the amount of deformation (relative change in length), as shown in Fig. 1.1 [2]. The external force can be treated as the excitation. After balance in the object system is reached after a period of time and at a certain temperature, the final responses are the stress or strain field. To fully solve this field, a couple of equations need to be satisfied. The first is the strain (e) - displacement (u) relation, which can be expressed as follows:

$$e_{ij} = \frac{1}{2}\left(\frac{\partial u_i}{\partial l_j} + \frac{\partial u_j}{\partial l_i}\right) \tag{1.1}$$

Another important relation connects strain to stress values, which is always anisotropic in crystals. Under the small deformation approximation, one can always assume the strain is linearly dependent on stress, with the ratio of modulus (E). Also, stress in a certain direction could generate strain in other directions; those effects can be included by multiplying the modulus with a coefficient, called the Poisson ratio (v). For a cubic crystal structure (e.g. Silicon), due to the symmetry, one can obtain the stress (S) –strain (e) relation tensor as follows:

$$\begin{bmatrix} e_{xx} \\ e_{yy} \\ e_{zz} \\ e_{yz} \\ e_{xz} \\ e_{xy} \end{bmatrix} = \begin{bmatrix} \frac{1}{E_x} & -\frac{\upsilon_{xy}}{E_x} & -\frac{\upsilon_{xz}}{E_x} & 0 & 0 & 0 \\ -\frac{\upsilon_{yx}}{E_y} & \frac{1}{E_y} & -\frac{\upsilon_{yz}}{E_y} & 0 & 0 & 0 \\ -\frac{\upsilon_{zx}}{E_z} & -\frac{\upsilon_{zy}}{E_z} & \frac{1}{E_z} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{G_{yz}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{G_{xz}} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{G_{xy}} \end{bmatrix} \begin{bmatrix} S_{xx} \\ S_{yy} \\ S_{zz} \\ S_{yz} \\ S_{xz} \\ S_{xy} \end{bmatrix} \tag{1.2}$$

where e_{ii} (S_{ii}) refers to the normal strain (stress), while e_{ij} (S_{ij}) stands for twice the shear strain (stress). Finally, the stress-body force (F) relations can be expressed as:

$$\frac{\partial S_{ij}}{\partial l_j} + F_i = 0 \tag{1.3}$$

which means the gradient of stress should be balanced with body force values. Combining the above expressions, and by applying appropriate boundary conditions, the exact solutions can be derived; the solving procedures, however, are always tedious and supplemental ways are needed. The Finite Element Method (FEM) is commonly adopted for finding approximate solutions of those partial differential equations (PDE), which uses Euler's method to render the PDEs into a series of ordinary differential equations that can be solved with largely reduced computing intensity [3, 4]. In this work, the mechanical strain simulations are performed based-on FEM in the three-dimensional (3-D) space.

To model the impact of strain on the semiconductor band structure, multiple methods have been proposed with the trade-off between physical accuracy and computational complexity [5-8]. Among those methods, the piezo-resistance (PR) model is the simplest one, which describes the relationship between the applied stress and the resistivity change in a semiconductor:

$$\left(\frac{\Delta\mu}{\mu}\right)_{ij} = \Pi_{ij} \cdot S_{ij} \tag{1.4}$$

where Π_{ij} is the matrix of PR coefficients, and S_{ij} is the stress vector with all normal and shear stress components included. The PR model assumes that the semiconductor resistivity (or more precisely, carrier mobility value) changes linearly with applied stress instead of taking into account the detailed change of band structure and scattering rates induced by strain, which is not accurate in most of the cases for MOSFET device modeling. For example, PR models cannot capture the channel doping and transverse electric field impact, and fail to predict the non-linear channel resistivity change at large level of strain [9]. On the other hand, "fully-physical" methods, such as Empirical Pseudo-potential Method (EPM) [6], Tight Binding (TB) [7] and *Ab-initio* [8] approach, require lots of computing threads, which are generally not favorable to meet commercial technology computer-aided-design (TCAD) requirements [9].

The k·p method is based on perturbation theory [10, 11], and serves well for predicting the strain impact on band structure while requiring reasonable computing loads by using a small set of wavefunction vectors and some empirical parameters, such as energy bandgap [1]. The conduction bands of Silicon consist of six ellipsoidal-shaped valleys (with two-fold spin degeneracy in each valley) located at Δ-point along each X-direction in 3-D space, as shown in Fig.1.2 (a-c). Based on perturbation theory, the Hamiltonian for the Silicon conduction band can be expressed as:

$$H_{\Delta 2} = \frac{\hbar^2(k_x^2 + k_y^2)}{2m_t^*} + \frac{\hbar^2 k_z^2}{2m_l^*} \tag{1.5}$$

for Δ2 valley electrons, and

$$H_{\Delta 4,i} = \frac{\hbar^2 k_i^2}{2m_l^*} + \frac{\hbar^2(k_z^2 + k_j^2)}{2m_t^*} \tag{1.6}$$

for Δ4 valley (with the ellipsoid's major axis oriented along *i*-direction) electrons. Note that the *k* in Eqn.s (1.5, 1.6) refers to approximate momentum vector shift around the Silicon conduction band edge (Δ-point). The non-parabolic terms in energy can be modeled as

$$E(\vec{k})\cdot(1+\alpha E(\vec{k}))=\frac{\hbar^2\vec{k}^2}{2m^*} \tag{1.7}$$

with α as the non-parabolic factor [12]. The strain effect is taken into account by assuming the conduction band energy changes linearly *vs.* strain applied with the ratio defined as "deformation potentials," as expressed below.

$$H_e=\sum_i \Xi_u\cdot e_{ii}+\sum_{i,j}\Xi_d\cdot e_{ij} \tag{1.8}$$

where Ξ_d and Ξ_u are the dilation and uniaxial deformation potentials at the Δ-point. Further studies suggest the shear strain components also change the ellipsoidal valley's curvature and hence affect electron's effective mass value [13]. This effect is important to electron mobility enhancement under <110> uniaxial stress and had been well modeled by considering the band splitting at the *Brillouin* zone boundary using the 2×2 k·p approach [14].

The valence bands of Silicon can be classified to Heavy Hole (HH), Light Hole (LH) and split-off (SO) hole bands, based on their state vectors $|j,m\rangle$, where *j* denotes the total angular momentum and *m* refers to the momentum projection along the z-axis [9-11]. Each one has two-fold spin degeneracy and the peak value at the Γ-point. For unstrained Silicon materials, HH and LH are degenerate at the Γ point, while an energy difference (~44meV for Silicon) exists for the SO band. When the semiconductor bandgap is much larger than the SO energy, the *Luttinger-Kohn* Hamiltonian, also known as 6×6 k·p approach, can be used to characterize the hole band structure, with the Hamiltonian expressed below [10, 11].

$$H_{L-K}=\begin{bmatrix} -P-Q & L & -M & 0 & \frac{L}{\sqrt{2}} & -\sqrt{2}M \\ -L^+ & -P+Q & 0 & -M & \sqrt{2}Q & -\sqrt{\frac{3}{2}}L \\ -M^+ & 0 & -P+Q & -L & -\sqrt{\frac{3}{2}}L^+ & -\sqrt{2}Q \\ 0 & -M^+ & -L^+ & -P-Q & \sqrt{2}M^+ & \frac{L^+}{\sqrt{2}} \\ \frac{L^+}{\sqrt{2}} & \sqrt{2}Q & -\sqrt{\frac{3}{2}}L & \sqrt{2}M & -P-\Delta & 0 \\ -\sqrt{2}M^+ & -\sqrt{\frac{3}{2}}L^+ & -\sqrt{2}Q & \frac{L}{\sqrt{2}} & 0 & -P-\Delta \end{bmatrix} \tag{1.9}$$

with P, Q, L, M defined as:

$$P=\frac{\hbar^2}{2m_0}\gamma_1(k_x^2+k_y^2+k_z^2) \tag{1.10}$$

$$Q = \frac{\hbar^2}{2m_0}\gamma_2(k_x^2 + k_y^2 - 2k_z^2) \tag{1.11}$$

$$L = \frac{\hbar^2}{m_0}\sqrt{3}\gamma_3(k_x - ik_y)k_z \tag{1.12}$$

$$M = -\frac{\hbar^2}{2m_0}\sqrt{3}[\gamma_2(k_x^2 - k_y^2) - i2\gamma_3 k_x k_y) \tag{1.13}$$

where $\gamma_{1\text{-}3}$ can capture the hole band structure curvature and Δ represents the SO energy. The strain effect is taken into account by adding the *Pikus-Bir* Hamiltonian, which shares the same form as the *Luttinger-Kohn* Hamiltonian, but has different element definitions as:

$$P_e = -a_v\left(e_{xx} + e_{yy} + e_{zz}\right) \tag{1.14}$$

$$Q_e = -\frac{b}{2}\left(e_{xx} + e_{yy} - 2e_{zz}\right) \tag{1.15}$$

$$L_e = -d\left(e_{xz} - i \cdot e_{yz}\right) \tag{1.16}$$

$$M_e = \frac{\sqrt{3}}{2}b\left(e_{xx} - e_{yy}\right) - id \cdot e_{xy} \tag{1.17}$$

Calculated hole band structures are shown in Fig.1.2 (d-f). Similarly to conduction bands, the degeneracy between HH and LH diminishes with carrier confinement and by applying biaxial or shear strain.

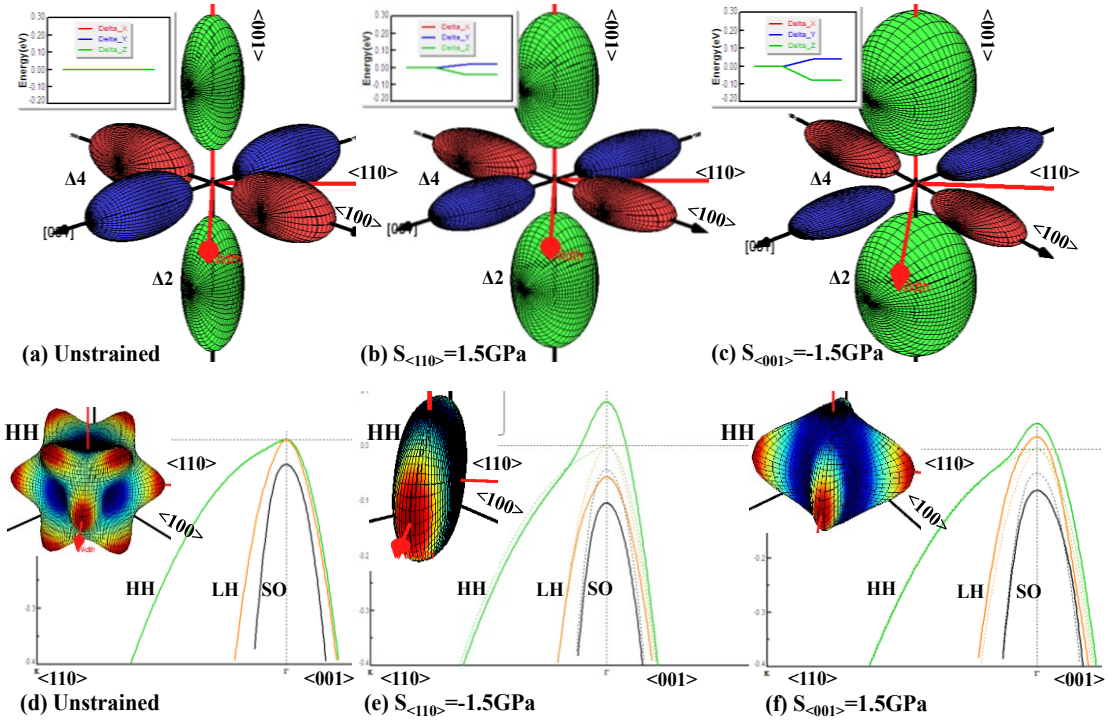

Figure 1.2. Silicon band structures calculated using perturbation method: (a)-(c) equi-energy contours for conduction band electrons; the insets show the conduction band energy for Δ4 (blue) and Δ2 (green) valley electrons. (d)-(f) Valence band energies for Silicon holes; the insets show HH band equi-energy contours, in

which clear band wrapping is found when strain is applied. Calculation is performed using MASTAR predictive modeling package [15].

1.1.2 Carrier Scatterings in Bulk Semiconductors

By accounting for the effects of strain on the semiconductor band structure, the impacts of strain on carrier mobility can be investigated. Starting from the simplest model, the low-field carrier mobility can be expressed as

$$\mu = \frac{e \cdot \tau}{m^*} \tag{1.18}$$

where m^* is carrier effective mass along current conduction direction, the so-called "transport effective mass"; τ is the momentum relaxation time (MRT). For electrons, strain-induced band splitting can suppress scatterings and hence reduce τ; on the other hand, more electrons are able to occupy $\Delta 2$ valleys, and result in lower average m^*. For holes, shear strain can largely change the band curvature and reduce m^*, to enhance hole mobility.

There are lots of scattering mechanisms which contribute to τ, among which phonon scattering is the dominant one at room temperature. Phonon scattering is caused by lattice atom oscillations with respect to their nominal positions; those oscillations may interact with carriers to change their positions or momenta to induce a time-relaxation process. For electrons, phonon scattering can take place within a conduction band valley; this is called Intra-valley scattering, which doesn't change the energy of electrons, and has the "elastic" scattering nature. If electrons are scattered between degenerate valleys (i.e. valleys oriented along the same axis), the process always causes energy change by interacting with optical phonons, which is "inelastic" in nature and often referred as "g-type" inter-valley scatterings. Electrons can also be scattered to all the other non-degenerate valleys, the so-called "f-type" inter-valley scatterings, which are always inelastic [16]. For holes, the elastic scattering process is often referred as acoustic phonon scattering, and the inelastic one as optical phonon scattering [17, 18]. The transition process can happen both within a certain hole band or between two different hole bands.

1.2 Carrier Transport in MOSFET Inversion Layer

1.2.1 Sub-band Structures from Quantum Wells

In the MOSFET structure, when the gate bias exceeds the threshold voltage (V_{th}), an inversion layer forms at the oxide/Silicon interface. The potential profile at the inversion layer's location can be approximated as a triangular potential well in which carriers are quasi two-dimensional (2-D) gas. Along the confinement direction, energy is quantized to a series of Eigen values, which are called "sub-bands". To calculate the sub-band energies, the discrete Schrödinger equation need to be solved in that quantum well. This is very convenient to incorporate with the $k \cdot p$ method, which only requires the replacement of the momentum vector k_z with $-id/dz$ in the Hamiltonian (assume z is the confinement direction), because the motion of carriers is restricted along the z-direction [18]. After the total Hamiltonian is re-constructed of many discrete $k \cdot p$

blocks based on the device mesh, the Poisson equation is self-consistently coupled to account for carrier's self-energy, which is usually known as the *Hartree-Fock* method [19]. The detailed solving procedure is listed in Fig.1.3 and will be elaborated in **chapter 2**.

Due to different effective mass values in the confinement direction, in the quantum well, the six conduction band valleys are no longer degenerate even without strain. For a (100)-confined surface, Δ2 valleys have lower energy values than the Δ4 valleys; in (110)-confined surface, Δ4 valleys have lower sub-band energy values, as shown in Fig.1.4 (a). For inversion holes, HH always have the lowest sub-band energy values independent of the surface orientation as shown in Fig.14 (b). Band warping is always seen for inversion layer holes, for example LH and SO are always mixed, causing more complicated band curvatures compared to the bulk case, as shown in Fig.1.4 (c). And these effects must be taken into account quantitatively in MOSFET channel carrier mobility modeling.

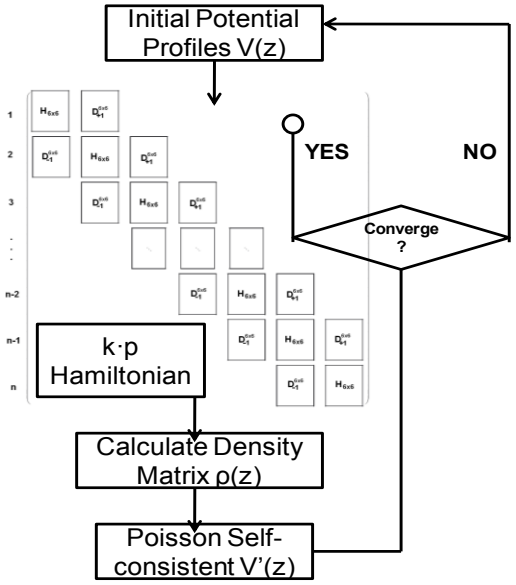

Figure 1.3. Poisson-Schrödinger self-consistent solving procedure for calculating carrier sub-band energies and wavefunctions in the quantum well.

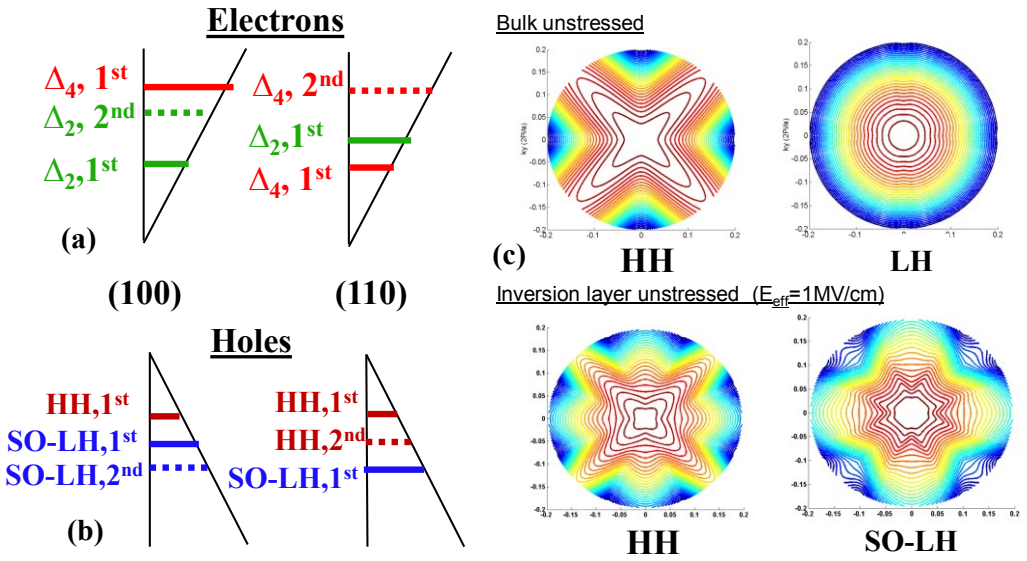

Figure 1.4. Sub-band energies in quantum well for inversion electrons (a) and holes (b) with different confinement direction; and (c) comparison between bulk holes and inversion holes equi-energy contours at k_x-k_y plane, strong band warping is clearly seen.

1.2.2 Carrier Scatterings in MOSFET Inversion Layers

In inversion layers, due to the motion of carriers being restricted to 2-D, the scatterings are also different than in a bulk semiconductor. According to the Fermi-Golden rule, the transition rate between two eigen-energy states in a quantum system depends not only on the density of states, but also the wavefunction overlap integral of the two states. This overlap integral, also known as the "form factor," determines the scattering rates between two sub-bands in the inversion layer, and has the form of

$$F_{n,n'} = \int_z dz \cdot \left| \overrightarrow{\xi_n}(z) \cdot \overrightarrow{\xi_{n'}^*}(z) \right| \tag{1.19}$$

where $\xi_{n,(n')}$ refers to the envelop wavefunction from sub-band n (n'). Note that form factors depend on both MOSFET body thickness (t_{SOI}) and transverse electric field, since both geometry and electrical potential well can contribute to the quantum confinement. As a result, inversion layer carrier mobility depends on the "effective" field, defined as the average electric field seen by the inversion layer [17, 18, 20]. Geometrical confinement is extremely important to study in thin-body MOSFETs, since carrier mobility values change quickly as t_{SOI} is scaled down: for (100)-surface electrons, mobility decreases due to the growing form factors initially, however, it starts to increase at t_{SOI} of ~3.5nm, as shown in Fig.1.5 (a), which was explained by the sub-band reoccupation effect [21]. For inversion holes, a similar effect can also be seen for the (110) surface, but not for the (100) surface, as shown in Fig.1.5 (b) [22]. Surface roughness scattering comes from the perturbation of the varying electric field at the rough oxide/Silicon interface in the inversion channel, which is not present in bulk semiconductors. It has become the dominant scattering mechanism in MOSFETs with aggressively scaled oxide thickness, especially devices fabricated on SOI substrates, due to the growing importance of the back oxide layer [23]. Carrier mobilities can also be lowered largely due to scatterings from trapped charges at oxide/Silicon

interface; which limits carrier mobility as a function of oxide thickness, as shown in Fig.1.5 (c) [23].

With the aforementioned reasons, the strain-induced carrier mobility enhancement should be investigated in inversion layers with electric field and with different gate stacks (i.e. SiO_2/poly-Si or high-κ/Metal gate stack). However, speaking of the electric field dependence, strain-induced carrier mobility enhancement generally decreases with increasing electric field, because the quantum confinement-induced sub-band splitting is subtractive to strain-induced sub-band splitting, as shown in Fig.1.5 (d) [24].

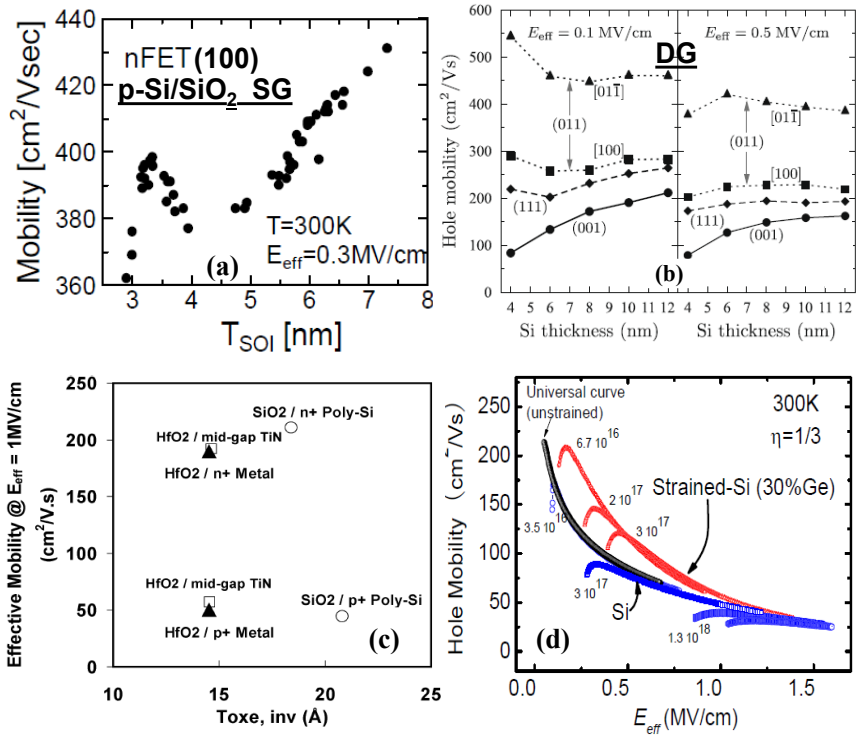

Figure 1.5 Inversion carrier mobility issues: (a) electron mobility vs. t_{SOI} in ultra-thin-body devices from [21]; (b) Hole mobility vs. Silicon thickness in Double-gated devices, from [22]; (c) Effective electron mobility values vs. gate oxide thickness, from [23]; (d) Strain-induced hole mobility enhancement vs. effective field, from [24]. *Copyright: IEEE*

1.2.3 Carrier Transport in Short-channel MOSFETs

For the conventional long-channel MOSFET, due to the large amount of scattering events in the channel, the ON-state current is mainly determined by the mobility values, which is known as the "drift-diffusion" limit. For very short channel length, when the physical channel length is even less than the carrier mean free path (MFP), non-stationary transport effect will affect the ON-state current significantly and quasi-ballistic transport takes place [25]. The carrier velocity in the channel at the location corresponding to the peak of the Source-side potential barrier determines the MOSFET ON-state current. This is confirmed by the combination of measured

data (from 40-60nm effective channel length devices) and *Monte Carlo* simulations [26], and is referred to as the "injection-velocity" limit [27].

In the linear region of a MOSFET operation, the overall impact of ballistic transport is relatively small compared to that in the ON-state [26]. Thus, the conclusions made to the long channel low-field mobility are expected to apply for the linear region current, regardless of the channel length. However, measured data show the mobility degrades with reducing the channel length, for which the physical mechanisms are still not very clear [28-30], and enhanced scatterings from the Source/Drain junction-side defects are considered to play an important role [28], as shown in Fig.1.6 (a). In the ON-state, extracted carrier velocity values saturate with channel length scaling, which clearly shows the approaching of the injection-velocity limit, as shown in Fig.1.6 (b) [31]. Further studies are carried on, by plotting the relative change between carrier ON-state injection velocities *vs.* linear region carrier mobilities induced by uniaxial strain. It's seen that a correlation exists, which can be explained by the fact that strain-induced carrier transport mass lowering still contributes significantly to improve short-channel MOSFET drive current, as shown in Fig.1.6 (c) [31].

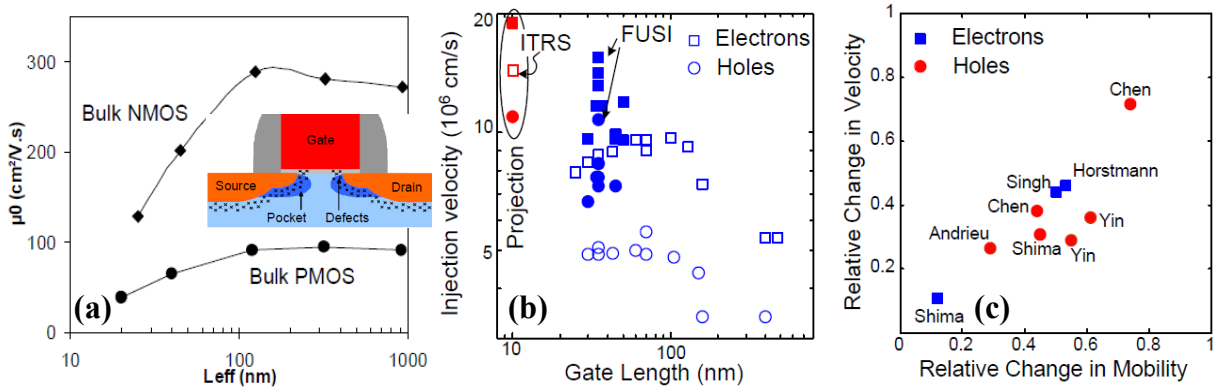

Figure 1.6 Short-channel MOSFET carrier transport issues: (a) carrier mobility degradation vs. effective channel length from [28]; (b) Injection velocity vs. gate length, from [31]; (c) Relative change in carrier velocity vs. change in mobility, induce by uniaxial strain, from [31]. *Copyright: IEEE*

1.3 Strained Silicon Technology

Although the idea of using mechanical strain to boost MOSFET performance came out very early [32, 33], most of the work used biaxial strain technology in which the strain is mainly generated from the SiGe substrate. Only until the late 1990s, uniaxial stressors such as strained capping layers [34] and embedded $Si_{1-x}Ge_x$ source/drain [35] were proposed, and became very effective in the high volume production, due to their advantageous low cost and process compatibility to the already developed CMOS platforms (compared to biaxial substrate stressors). Another feature in contrast to biaxial stressors, which generates global stress across the whole wafer, uniaxial stressors only induces stress locally (i.e. within a certain layout area). This section focuses on currently widely-used uniaxial stressor technologies, and introduces the impact of other process variations (i.e. high-κ/metal gate stack formation) on boosting MOSFET channel strain and performance.

1.3.1 Process-induced Strain

At Intel's 90nm High-Performance (HP) production node, embedded SiGe (eSiGe) source/drain (S/D) was adopted to generate high compressive strain along the channel (due to the lattice spacing of SiGe is larger than Silicon), in order to boost hole mobility and P-MOSFET drive current, as shown in Fig.1.7 (a) [35]. Additional modifications can be done to further enhance the stress transfer efficiency, such as optimizing the S/D recess depth, Ge mole fraction as well as controlling the shape of the eSiGe, as Intel later did in their 45nm HP platform (Fig.1.7 (b)) [36]. Recently, similar principle is applied to Carbon-doped Silicon (Si:C) as the N-MOSFET S/D, to generate tensile stress (due to small lattice spacing of C) and hence to enhance electron mobility [37].

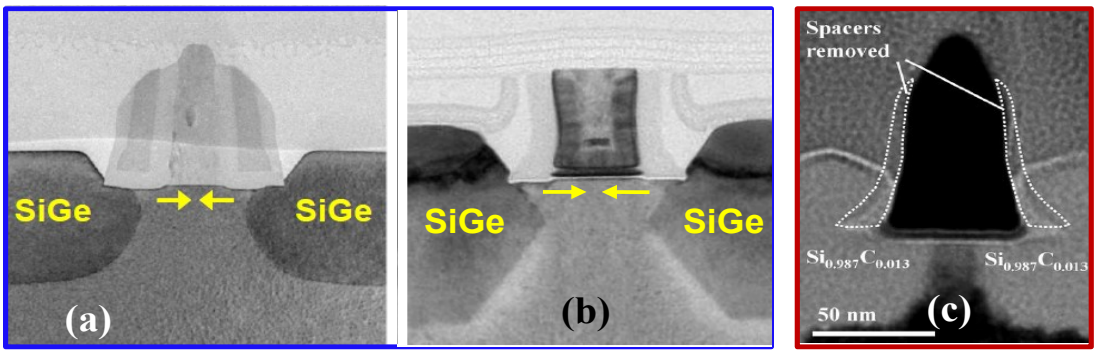

Figure 1.7. TEM cross-sectional views for (a, b) P-MOSFET using embedded SiGe as S/D, from [35, 36], (c) N-MOSFET using Si:C as S/D, from [37]. *Copyright: IEEE*

Another approach to generate local uniaxial strain is through strained Contact-etch-stop-linear (sCESL) technology [34], where the internal stress within the deposited nitride layer can be adjusted to giga-pascal (GPa) order, with tensile strain possible. In this way, sCESL was firstly used to improve the N-MOSFET performance [34, 35]. Later, compressive strain within the nitride layer has been achieved, and dual stress liner (DSL) technology is developed to boost both P-type and N-type MOSFET performance simultaneously, as shown in Fig.1.8 (b) [38].

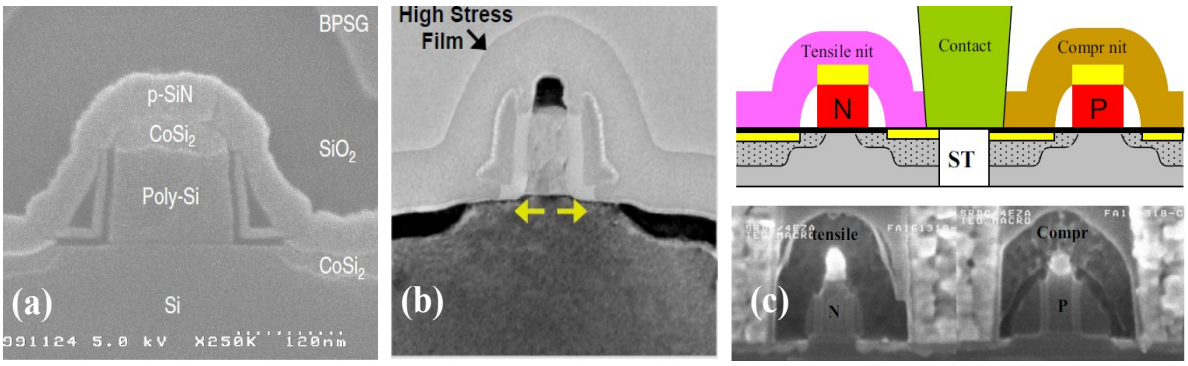

Figure 1.8. TEM cross-sectional views for using the sCESL technology in N-type MOSFET, from (a) [34], and from (b) [35]. Developed DSL technology in both N-type and P-type MOSFETs, from [38]. *Copyright: IEEE*

Stress Memorization Technique (SMT) relies on the dislocations formed after high dose implantation (HDI) process to introduce strain into the MOSFET channel. A nitride capping layer is deposited across the device after the HDI process followed by forming gas annealing (FGA) to re-crystallize the S/D (or poly-Si gate) region, which forces the S/D (poly-Si gate) "memorizing" the shape formed by the capping layer. In this way, the strain is maintained even after the subsequent removal of the capping layer. There provides two major SMT sources: 1) Compressive vertical stress (S_{zz}) from poly-Si gate, as shown in Fig.1.9 (a) [39]; 2) Tensile longitudinal stress (S_{xx}) from amorphized S/D, as shown in Fig.1.9 (b-d) [40]. Both stress configurations benefit for electron mobility enhancement.

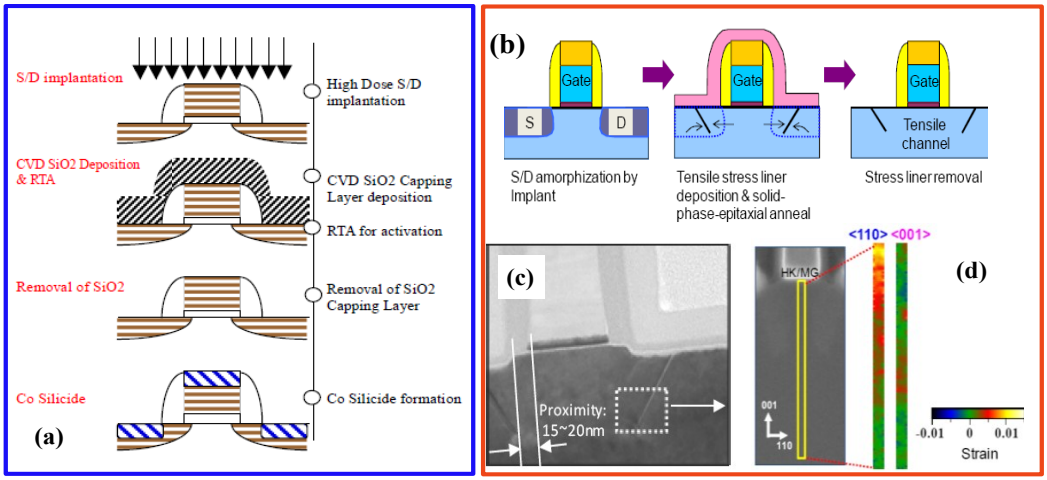

Figure 1.9. Schematic views of SMT introduced from (a) poly-Si gate, from [39], and (b) S/D dislocation stress, from [40]. *Copyright: IEEE*

When metal gate technology is used, the gate-last process (i.e. replacement metal gate) can further enhance the S_{xx} values in the channel region. This is due to the free boundary conditions at the gate stack edge after removal of poly-Si dummy gate, as shown in Fig.1.10 [36].

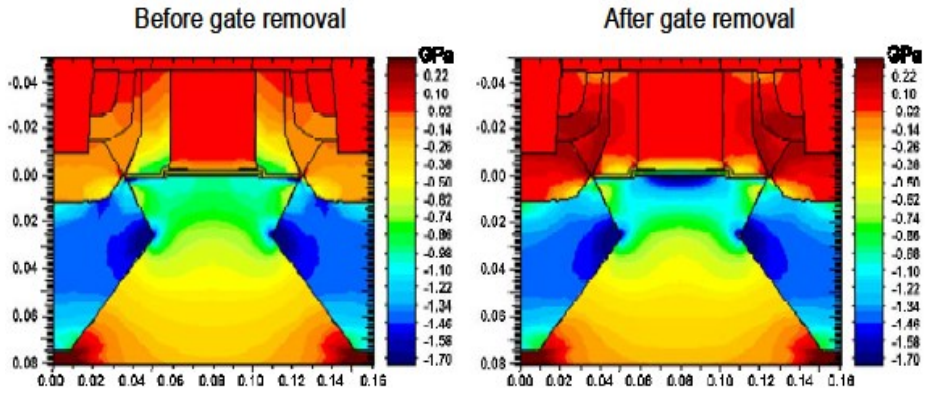

Figure 1.10. TCAD simulated S_{xx} profiles for (left) before gate removal and (right) after gate removal, clear stress enhancement is seen, from [36]. *Copyright: IEEE*

1.3.2 Strain in Advanced Planar Bulk CMOS Technologies

Intel uses high-κ/metal gate-last technology starting from its 45nm HP technology platform. For N-MOSFET, SMT is used; for P-MOSFET eSiGe S/D is adopted. Gate-last technology can further enhance S_{xx} component in the P-MOSFET channel, to boost its current [36]. In their follow-up 32nm HP platform [41], further adjustments were made upon 45nm as follows:

- Raised S/D is used for N-MOSFET, to reduce series resistance.
- The proximity of P-MOSFET SiGe S/D to the Silicon channel continues to decrease, in order to enhance channel strain, as shown in Fig.1.11 (a).

This results in the first time report of a higher linear region current in P-type than that in N-type MOSFET [41]. Overall, the 32nm technology provides 35% (I_{dlin}) and 28% (I_{dsat}) for P-MOSFET, 20% (I_{dlin}) and 19% (I_{dsat}) for N-MOSFET drive current enhancement over their 45nm technology. IBM's 32nm general purpose (GP) platform used tensile sCESL and SMT on N-MOSFET and compressive sCESL and eSiGe S/D on P-MOSFET, as shown in Fig.1.11 (b) [42]. UMC's 28nm HP platform used a "hybrid" high-κ/metal Gate technology: for N-MOSFET, gate-first approach is used, and remarkable mobility was achieved through optimized HfO_2 high-κ, TiN metal gate and LaO_x capping layer processes. For P-MOSFET, gate-last process after eSiGe S/D formation provides 30% current enhancement compared to gate-first control, as shown in Fig.11 (c) [43]. For UMC's 28nm Low-Power (LP) platforms, the eSiGe S/D was further optimized to have a "Diamond" shape, as shown in Fig.11 (d) which gives 10% P-MOSFET current enhancement compared to the control device with normal eSiGe S/D [44].

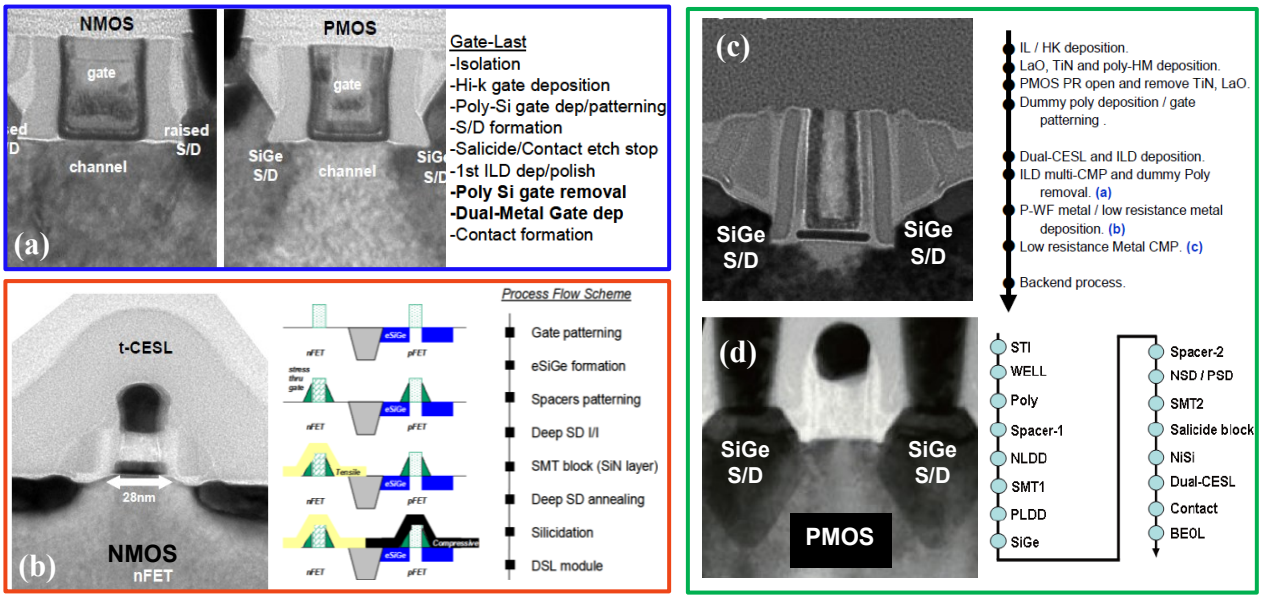

Figure 1.11. Schematic views and key process flows for advanced planar bulk CMOS platforms using strain as the performance booster. From [41-44]. *Copyright: IEEE*

1.4 Advanced Strained CMOS Technologies for the 22nm Node and Beyond

1.4.1 Advanced, Thin-Body MOSFET Structures

Increasing performance variability and OFF-state leakage current in planar bulk CMOS technology reduces device performance margin, and hence implies strong limitations to IC design. Rather than doping the channel heavily to suppress OFF-state leakage, it can be made to be very thin to eliminate sub-surface leakage paths and reduce Drain Induced Barrier Lowering (DIBL) [45]. In the latter case, the channel/body region is so thin that it is fully depleted of mobile charge carriers when the transistor is off. Such an ultra-thin-body (UTB) fully depleted (FD) MOSFET structure is most easily implemented with an extremely-thin SOI substrate [46-48]. The buried oxide (BOX) layer can be further thinned (to ~10nm) to reduce the lateral S/D electrical coupling, which makes the device as an ultra-thin-body and BOX (UTBB) FD MOSFET, as shown in Fig.1.12 (right) [48]. Another advantage is that the same IC design flow can be used for FD-SOI MOSFET technology as for planar bulk technology, which is advantageous for reduced design cost and time-to-market.

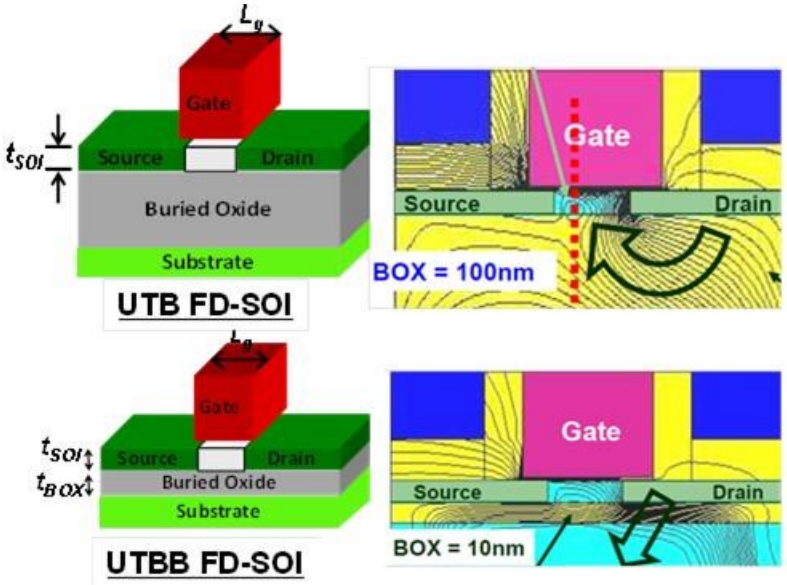

Figure 1.12. (left) Schematic view of UTB FD-SOI MOSFET and UTBB FD-SOI MOSFET, on SOI wafer. (right) TCAD simulated electric field at transistor OFF-state; thin BOX structure shows reduced of S/D coupling to the channel, from [48].

The fundamental concept behind a Multiple-Gate MOSFET (in which the gates are all tied together) is to increase gate control (*vs.* drain control) of the channel potential, particularly the source-to-channel potential barrier. The double-gate MOSFET has two gates located on opposing sides of the Silicon channel region, to control the channel potential. It is most easily implemented as a vertical structure, with a single gate electrode running across (straddling the two opposing sides of) a tall and narrow Silicon body "fin." This "FinFET" structure has been widely investigated [49-51], and can be implemented either on an SOI substrate [49, 50] or a

bulk substrate [52]. To adequately suppress short-channel effects, the width of the Silicon fin in a FinFET should be less than 1/2 of the channel length [51]. Meanwhile, to keep good layout area efficiency, the height of the Silicon fin should be two times larger than the fin width, as shown in Fig.1.13 (left). Another fin aspect-ratio design is to keep the fin width equal to the channel length, while the fin height as 1/3 of the fin width [51], as shown in Fig. 1.13 (right); this structure is always referred as "Tri-Gate" MOSFET, due to the fact that the top surface dominates the overall current conduction.

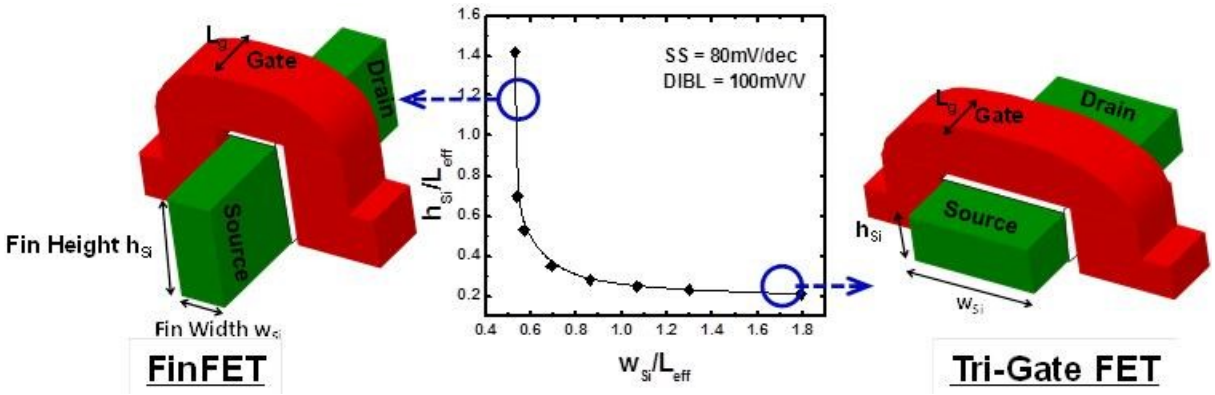

Figure 1.13. Schematic view of Multiple-Gate MOSFET, with various aspect ratios while maintaining the same OFF-state leakage and electrostatics, based on the design curve in [51]. *Copyright: IEEE*

1.4.2 Thin-body CMOS Technologies using Strain as Performance Boosters

It is straightforward to transfer the current bulk stressor technologies to UTB FD-SOI MOSFETs, due to the similar surface orientations and device architectures. IBM showed Extremely Thin (ET) FD-SOI MOSFET with good electrostatic integrity under gate length of 22nm [53, 54]. The Silicon body thickness is ~6nm, fabricated on thick BOX SOI wafers. Metal-gate-first technology is adopted, and faceted raised S/D is formed to provide higher strain than the normal vertical raised S/D and further reduce parasitic capacitance, as shown in Fig.1.14 (b) [53]. Later, sCESL technique is also used to enhance channel strain [54]. CEA-LETI demonstrated FD SOI MOSFET fabricated on thin BOX, down to gate length of 30nm [55, 56]. For the strain solution, strained SOI (sSOI) substrate is found to provide the highest N-MOSFET current enhancement; raised SiGe S/D is considered as the most effective stressor for P-MOSFET performance boosting, as shown in Fig.1.14 (c) [57]. STMicroelectronics used tensile CESL to enhance N-type FD-SOI MOSFET drive current, as shown in Fig.1.14 (d) [58].

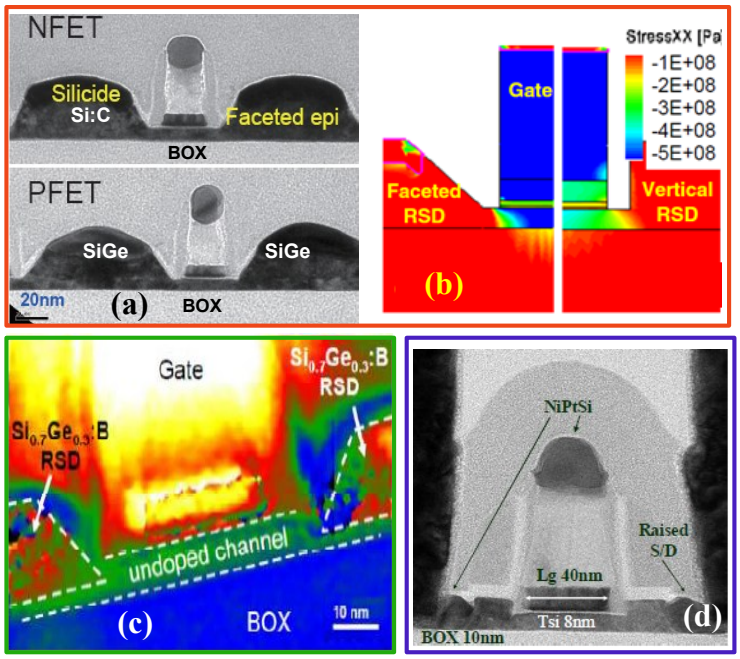

Figure 1.14. Schematic views for current FD SOI MOSFET platforms using strain as the performance booster. From [53-58]. *Copyright: IEEE*

For advanced Multiple-Gate MOSFETs, due to the complicated 3-D structure nature, no clear conclusions have been reached regarding the effectiveness of different stressor technologies. IBM demonstrated FinFET on SOI substrate, with gate length of 25nm, as shown in Fig.1.15 (a) [59, 60]. Gate-first approach is used to fabricate high-κ/metal Gate stack. For the strain solutions, raised SiGe S/D is used to enhance P-MOSFET current; for N-MOSFET, strained SOI option provide remarkable drive current enhancement, which can be attributed to the strain evolution (from biaxial to uniaxial) during the fin etching process [60]. Intel applied SiGe S/D in its bulk Tri-Gate MOSFET structure, in which undercut etch of the S/D-part fin was performed before the epitaxial growth, resulting in further strain and hole mobility enhancement in the channel, as shown in Fig.1.15 (b) [61]. TSMC showed FinFET on bulk substrate, with gate length down to 22nm [62]. Gate-last approach is used to fabricate high-κ/Metal Gate stack. Gate SMT is used for enhancing N-MOSFET's current; SiGe S/D as well as compressive CESL is used to enhance P-MOSFET's current, by combing with the gate-last process flow, the I_{on} is further enhanced.

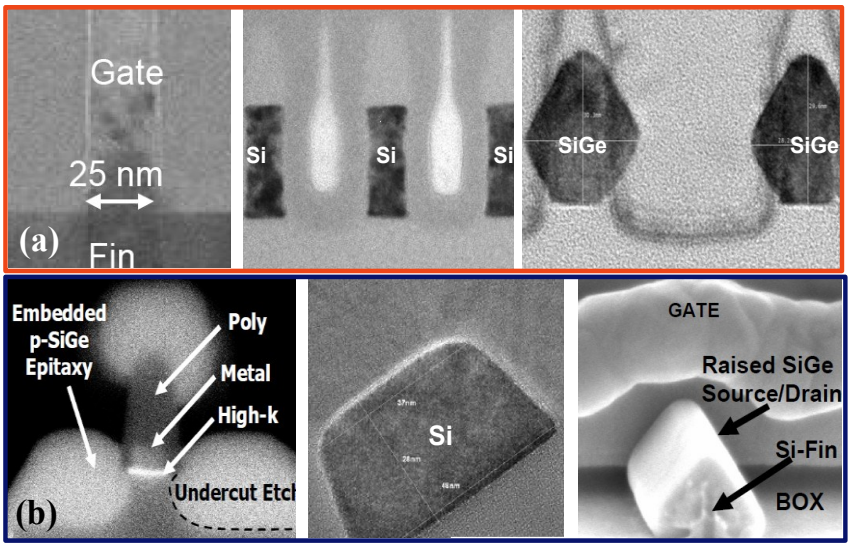

Figure 1.15. Schematic views for current Multiple-Gate MOSFET platforms using strain as the performance booster. From [59 - 61]. *Copyright: IEEE*

1.5 Research Objectives and Thesis Overview

In **chapter 2,** the stress-induced performance enhancement in Silicon UTB FD-SOI MOSFETs with special attention to the impacts of body thickness and gate length scaling are investigated. Firstly, the Poisson-Schrödinger self-consistent simulator for FD-SOI device carrier sub-band structures and mobility calculations is described. Then the strain-induced FD-SOI device carrier mobility enhancement is assessed with t_{SOI} scaling, for electrons and holes. Finally, short-channel device carrier apparent mobilities and limiting velocities are extracted after decoupling the S/D series resistance, which shows the strain-induced enhancement trend of the aforementioned parameters as gate length scales.

In **chapter 3**, the study of strain-induced carrier mobility enhancement for Multiple-Gate MOSFET technology is presented, with the impacts of different structural and process variations. The 2-D Poisson-Schrödinger self-consistent simulator is hence developed, to account for the multiple channel structure. The effects of the Multiple-Gate FET fin aspect ratio, crystalline orientation and stress design for improving performance are studied. Especially for advanced FinFET devices, different local uniaxial stressor technologies are compared, to provide the insight for maximizing the strain-induced performance enhancement in short-channel FinFET devices.

In **chapter 4**, stress-induced enhancements in electron and hole mobilities are studied comprehensively for UTB FD-SOI MOSFET and FinFET structures with high-κ/metal gate stacks. New scattering models, (i.e. remote Coulomb and surface optical phonon scatterings) are further included to account for the structural differences between the two devices. Simulation data calibrated to measurement are presented to evaluate the effectiveness of strain for boosting thin-body MOSFET performance with aggressively scaled body thickness.

In **chapter 5**, the performance modulation of back biasing on UTBB FD-SOI MOSFET is investigated, for long-channel as well as short-channel devices. Firstly, the back bias effect on UTBB FD-SOI MOSFET device electrostatics (including V_{th} and gate-induced-drain-leakage, GIDL) are presented. Then, the modulation of back biasing on carrier transport behaviors (including carrier mobility, limiting velocity and strain-induced performance enhancement) and its implications for aggressively scaled devices are presented.

In **chapter 6**, the contributions of this dissertation are summarized and suggestions for future research topics are made.

1.6 References

[1] Y. Sun, S.E. Thompson, T. Nishida, "Physics of Strain Effects in Semiconductors and metal-oxide-semiconductor field-effect transistors," AIP Journal of Applied Physics, vol.101, issue 10, 2007, 104503.

[2] Paul A. Lagace, "Structural Mechanics," MIT Open Course, 2002.

[3] G. Strang, G. Fix, "An Analysis of the Finite Element Method." Prentice Hall. 1973, ISBN 0130329460.

[4] *Sentaurus* Process User Guide, Version D-2011.09, Synopsys Co., Mountain View, CA, 2011.

[5] C. S. Smith, "Piezo resistance Effect in Germanium and Silicon," Physical Review, vol. 94, no. 1, 1954, pp. 42-49.

[6] J.C. Phillips, "Energy-Band Interpolation Scheme Based on a Pseudo-potential," Physical Review, vol. 112, 1958, pp. 685-704.

[7] J.C. Slater, G.F. Koster, "Simplified LCAO Method for the Periodic Potential Problem," Physical Review, vol. 94, no.6, 1954, pp. 1498–1524.

[8] H. van Leuken, A. Lodder, M.T. Czyzyk, F. Springelkamp, R.A. de Groot, Physical Review B, vol. 41, 1990, p.5613.

[9] *Sentaurus* Band User Guide, Version D-2011.09, Synopsys Co., Mountain View, CA, 2011.

[10] G.L. Bir, G.E. Pikus, "Symmetry and Strain-induced Effects in Semiconductors," Wiley, New York, 1974.

[11] C.Y.-P. Chao, S L. Chuang, "Spin-orbit-coupling effects on the valence-band structure of strained semiconductor quantum wells," Physical Review B, vol. 46, no.7, 1992, pp.4110-4122.

[12] V. Sverdlov, E. Ungersboeck, H. Kosina, S. Selberherr, "Effects of Shear Strain on the Conduction Band in Silicon: An Efficient Two-Band Theory," in Proceedings of the 37th European Solid-State Device Research Conference (ESSDERC), Munich, Germany, 2007, pp. 386–389.

[13] K. Uchida, M. Saitoh, S. Kobayashi, "Carrier Transport and Stress Engineering in Advanced Nanoscale Transistors From (100) and (110) Transistors To Carbon Nanotube FETs and Beyond," IEDM Tech. Dig., 2008, pp.569-572.

[14] E. Ungersboeck, S. Dhar, G. Karlowatz, V. Sverdlov, H. Kosina, S. Selberherr, "The Effect of General Strain on the Band Structure and Electron Mobility of Silicon," IEEE Transactions on Electron Devices, vol.54, No.9, pp.2183-2190, 2007.

[15] *MASTAR* User's Guide, Version 4, 2011.
[16] M.V. Fischetti, S.E. Laux, "Band Structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," AIP Journal of Applied Physics, 1996, pp.2232-2252.
[17] L. Donetti, F. Gamiz, N. Rodriguez, "Simulation of hole mobility in two-dimensional systems," IOP Semiconductor Science and Technology, vol.24, 035016, 2009.
[18] M.V. Fischetti, Z. Ren, P.M. Solomon, M. Yang, K. Rim, "Six-band kp calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain and silicon thickness," AIP Journal of Applied Physics, vol.94, no.2, 2003, pp.1079-1095.
[19] R.M. Martin, "Electronic Structure: Basic Theory and Practical Methods," Cambridge, 2004.
[20] D. Esseni, F. Conzatti, M. De Michielis, N. Serra, P. Palestri, L. Selmi, "Semi-classical transport modeling of CMOS transistors with arbitrary crustal orientations and strain engineering," Journal of Computational Electronics, vol.8, 2009, pp.209-224.
[21] K. Uchida, M. Saitoh, S. Kobayashi, "Carrier Transport and Stress Engineering in Advanced Nanoscale Transistors From (100) and (110) Transistors to Carbon Nanotube FETs and Beyond," IEDM Tech. Dig., 2008, pp.569-572.
[22] L. Donetti, F. Gámiz, N. Rodriguez, F. Jiménez-Molinos, J.B. Roldán, "Hole Transport in DGSOI Devices: Orientation and Silicon Thickness Effects," Solid-State Electronics, vol.54, 2010, pp.191-195.
[23] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, M. Metz, "High-κ/Metal-Gate Stack and Its MOSFET Characteristics," IEEE Electron Device Letters, vol. 25, no.6, 2004, pp.408-410.
[24] Y. Zhao, M. Takenaka, S. Takagi, "Comprehensive understanding of surface roughness and Coulomb scattering in biaxially-strained Si MOSFETs," IEDM Tech. Dig. pp.577-580, 2008.
[25] M.S. Lundstrom, "On the Mobility Versus Drain Current Relation for a Nanoscale MOSFET," IEEE Electron Device Letters, Vol.22, no.6, 2001, pp.293-295.
[26] F.M. Bufler, Y. Asahi, H. Yoshimura, C. Zechner, A. Schenk, W. Fichtner, "Monte Carlo Simulation and Measurement of Nanoscale n-MOSFET," IEEE Transactions on Electron Devices, vol.50, no.2, 2003, pp.418-424.
[27] D.A. Antoniadis, I. Aberg, C.Ni Chleirigh, O.M. Nayfeh, A. Khakifirooz, J.L. Hoyt, "Continuous MOSFET performance increase with device scaling: The role of strain and channel material innovations," IBM Journals of Research & Development, vol. 50, 2006, p.363
[28] A. Cros et al., "Unexpected mobility degradation for very short devices: A new challenge for CMOS scaling," IEDM Tech. Dig. 2006
[29] S. Poli, M.G. Pala, "Channel-length Dependence of Low-Field Mobility in Silicon-Nanowire FETs," IEEE Electron Device Letters, vol.30, no.11, 2009, pp.1212-1214.
[30] V. Barral, T. Poiroux, S. Barraud, F. Andrieu, O. Faynot, D. Munteanu, J.-L. Autran, S. Deleonibus, "Evidences on the physical oringin of the unexpected transport degradation in ultimate n-FDSOI devices," IEEE Transactions on Nanotechnology, vol.8, no.2, 2009, pp.167-172.
[31] A. Khakifirooz, D.A. Antoniadis, "Transistor Performance Scaling: The Role of Virtual Source Velocity and Its Mobility Dependence," IEDM Tech Dig., 2006, p.667.
[32] J. Welser, J.L. Hoyt, J.F. Gibbons, "Electron Mobility Enhancement in Strained Si N-type Metal-Oxide-Semiconductor Field-Effect-Transistors," IEDM Tech. Dig., pp.100-102, 1994.

[33] E.A. Fitzgerald, Y.H. Xie, M.L. Green, D. Brasen, A.R. Kortan, J. Michel, Y.J. Mii, B. Weir, "Totally relaxed Ge_xSi_{1-x} layers with low threading dislocation densities grown on Si substrates," Journal of Applied Physics, vol.59, no.7, 1991, pp.811-813.
[34] (**sCESL**) S. Ito, H. Namba, K. Yamaguchi, T. Hirata, K. Ando, S. Koyama, S. Kuroki, N. Ikezawa, T. Saitoh, T. Horiuchi, "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design," IEDM Tech. Dig., 2000.
[35] **(Intel-90)** T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, M. Bohr, "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," IEDM Tech. Dig., 2003.
[36] **(Intel-45)** C. Auth, A. Cappellani, J.-S. Chun, A. Dalis, A. Davis, T. Ghani, G. Glass, T. Glassman, M. Harper, M. Hattendorf, P. Hentges, S. Jaloviar, S. Joshi, J. Klaus, K. Kuhn, D. Lavric, M. Lu, H. Mariappan, K. Mistry, B. Norris, N. Rahhal-orabi, P. Ranade, J. Sandford, L. Shifren, V. Souw, K. Tone, F. Tambwe, A. Thompson, D. Towner,T. Troeger, P. Vandervoorn, C. Wallace, J. Wiedemer, C. Wiegand, "45nm High-k+Metal Gate Strain-Enhanced Transistors," Symp. on VLSI Tech Dig., 2008.
[37] (**Si:C**) K.-W. Ang, K.-J. Chui, V. Bliznetsov, C.-H. Tung, A. Du, N. Balasubramanian, G. Samudra, M.F. Li, Y.-C. Yeo, "Lattice strain analysis of transistor structures with silicon-germanium and silicon-carbon source/drain stressors," Applied Physics Letters, vol.86, 093102, 2005.
[38] (**DSL**) H.S. Yang, R. Malik, S. Narasimha, Y. Li, R. Divakaruni, P. Agnello, S. Allen, A. Antreasyan, J.C. Arnold, K. Bandy, "Dual Stress Liner for High Performance sub-45nm Gate Length SOI CMOS Manufacturing," IEDM Tech. Dig., 2004, pp.1075-1077.
[39] (**Gate SMT**) K. Ota, K. Sugihara, H. Sayama, T. Uchida, H. Oda, T. Eimori, H. Morimoto, Y. Inoue, "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," IEDM Tech. Dig. 2002.
[40] (**S/D SMT**) K.-Y. Lim, H. Lee, C. Ryu, K.-I. Seo, U. Kwon, S. Kim, J. Choi, K. Oh, H.-K. Jeon, C. Song, T.-O. Kwon, J. Cho, S. Lee, Y. Sohn, H. S. Yoon, J. Park, K. Lee, W. Kim, E. Lee, S.-P. Sim, C.G. Koh, S.B. Kang, S. Choi, C. Chung, "Novel Stress-Memorization-Technology (SMT) for High Electron Mobility Enhancement of Gate Last High-κ/Metal Gate Devices," IEDM Tech. Dig. pp.229-232, 2010.
[41] (**Intel-32)** P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo, S. Natarajan, "High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors," IEDM Tech Dig., 2009.
[42] **(IBM-32)** F. Arnaud, J. Liu, Y.M. Lee, K.Y. Lim, S. Kohler, J. Chen, B.K. Moon, C.W. Lai, M. Lipinski, L. Sang, F. Guarin, C. Hobbs, P. Ferreira, K. Ohuchi, J.Li, H. Zhuang, P.Mora, Q. Zhang, D.R.Nair, D.H. Lee, K.K. Chan, S. Satadru, S. Yang, J. Koshy, W. Hayter, M. Zaleski, D.V. Coolbaugh, H.W. Kim, Y.C. Ee, J.Sudijono, A.Thean, M. Sherony, S. Samavedam, M. Khare, C. Goldberg, A. Steegen, "32nm General Purpose Bulk CMOS Technology for High Performance Applications at Low Voltage," IEDM Tech Dig., 2008.

[43] **(UMC-28)** C.W. Liang, M. T. Chen, J. S. Jenq, W. Y. Lien, C. C. Huang, Y. S. Lin, B. J. Tzau, W. J. Wu, Z. H. Fu, I. C. Wang, P. Y. Chou, C. S. Fu, C. Y. Tzeng, K. L. Chiu, L. S. Huang, J. W. You, J. G. Hung, Z. M. Cheng, B. C. Hsu, H. Y. Wang, Y. H. Ye, J. Y. Wu, C. L. Yang, C. C. Huang, C. C. Chien, Y. R. Wang, C. C. Liu, S. F. Tzou, Y. H. Huang, C. C. Yu, J. H. Liao, C. L. Lin, D. F. Chen, S. C. Chien, I. C. Chen, "A 28nm Poly/SiON CMOS Technology for Low-Power SoC Applications," Symp. on VLSI Tech Dig., 2011.

[44] **(UMC-28)** C. M. Lai, C. T. Lin, L. W. Cheng, C. H. Hsu, J. T. Tseng, T. F. Chiang, C. H. Chou, Y. W. Chen, C. H. Yu, S. H. Hsu, C. G. Chen, Z. C. Lee, J. F. Lin, C. L. Yang, G. H. Ma, S. C. Chien, "A Novel 'Hybrid' High-k/Metal Gate Process for 28nm High Performance CMOSFETs," IEDM Tech Dig., 2009.

[45] C. Hu, "Silicon-on-insulator for high speed ultra large scale integration," Japanese Journal of Applied Physics, vol.33, 1994, pp.365-369.

[46] R. Tsuchiya, M. Horiuchi, S. Kimura, M. Yamaoka, T. Kawahara, S. Maegawa, T. Ipposhi, Y. Ohji, H. Matsuoka, "Silicon on Thin BOX: A New Paradigm of the CMOSFET for Low-Power and High Performance Application Featuring Wide-Range Back Bias Control," IEDM Tech. Dig., 2004, pp.631-634.

[47] Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, T.-J. King, J. Bokor, C. Hu, "Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era," IEEE Electron Device Letters, vol.21, no.5, 2000, pp.254-256.

[48] T. Skotnicki, ECS Symp., SOI Tech. & Dev XI, edit by S. Cristoloveanu, 2003.

[49] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, C. Hu, "Sub 50-nm FinFET: PMOS," IEDM Tech. Dig., 1999, pp. 67-70.

[50] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, C. Hu, "FinFET – A Self-aligned Double-Gate MOSFET Scalable to 20 nm," Electron devices, IEEE Transactions on, vol.47, no.12, 2000, pp.2320-2325.

[51] J.G. Fossum, L.Q. Wang, J.W. Yang, S.H. Kim, V.P. Trivedi, "Pragmatic Design of Nanoscale Multi-gate CMOS," IEDM Tech. Dig., 2004, pp. 613-616.

[52] T. Park, H.J. Cho, J.D. Choe, S.Y. Han, S.-M. Jung, J.H. Jeong, B.Y. Nam, O.I. Kwon, J.N. Han, H.S. Kang, M.C. Chae, G.S. Yeo, S.W. Lee, D.Y. Lee, D. Park, K. Kim, E. Yoon, J.H. Lee, "Static Noise Margin of the Full DG-CMOS SRAM Cell Using Bulk FinFETs (Omega MOSFETs)," IEDM Tech. Dig. 2003.

[53] **(IBM-ET-25)** K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi, L. F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet, S. Holmes, S. Mehta, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, B. S. Haran, Z. Zhu, L. H. Vanamurth, S. Fan, D. Horak, H. Bu, P. J. Oldiges, D. K. Sadana, P. Kozlowski, D. McHerron, J. O'Neill, B. Doris, "Extremely Thin SOI (ETSOI) CMOS with Record Low Variability for Low Power System-on-Chip Applications," IEDM 2009.

[54] **(IBM-ET-22)** K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, B. Haran, A. Kumar, T. Adam, A. Reznicek, N. Loubet+, H. He, J. Kuss, M. Wang, T. M. Levin, F. Monsieur, Q. Liu, R. Sreenivasan, J. Cai, A. Kimball, S. Mehta, S. Luning, Y. Zhu, Z. Zhu, T. Yamamoto, A. Bryant, C. –H. Lin, S. Naczas, H. Jagannathan, L. F. Edge, S. Allegret-Maret, A. Dube, S. Kanakasabapathy, S. Schmitz, A. Inada, S. Seo, M. Raymond, Z. Zhang, A. Yagishita, J. Demarest, J. Li, M. Hopstaken, N. Berliner, A. Upham, R. Johnson, S. Holmes, T. Standaert, M. Smalley, N. Zamdmer, Z. Ren, T. Wu, H. Bu, V. Paruchuri, D. Sadana, V. Narayanan, W.

Haensch, J. O'Neill, T. Hook, M. Khare, B. Doris, "ETSOI CMOS for System-on-Chip Applications Featuring 22nm Gate Length, Sub-100nm Gate Pitch, and 0.08μm^2 SRAM Cell," VLSI, 2011.

[55] **(LETI-FD-30)** F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J-P. Noel, C. Fenouillet-Béranger, J-P. Mazellier, P. Perreau, T. Poiroux, Y. Morand, T. Morel, S. Allegret, V. Loup, S. Barnola, F. Martin, J-F. Damlencourt, I. Servin, M. Cassé, X. Garros, O. Rozeau, M-A. Jaud, G. Cibrario, J. Cluzel, A. Toffoli, F. Allain, R. Kies, D. Lafond, V. Delaye, C. Tabone, L. Tosti, L. Brévard, P. Gaud, V. Paruchuri, K.K. Bourdelle, W. Schwarzenbach, O. Bonnin, B-Y. Nguyen, B. Doris, F. Boeuf, T. Skotnicki, O. Faynot, "Low Leakage and Low Variability Ultr-Thin-Body and Buried Oxide (UT2B) SOI Technology for 20nm Low Power CMOS and Beyond," VLSI 2010.

[56] **(LETI-FD-20)** O. Faynot, F. Andrieu, O. Weber, C. Fenouillet-Béranger, P. Perreau, J. Mazurier, T. Benoist, O. Rozeau, T. Poiroux, M. Vinet, L. Grenouillet, J-P. Noel, N. Posseme, S. Barnola, F. Martin, C. Lapeyre, M. Cassé, X.Garros, M-A. Jaud, O. Thomas, G. Cibrario, L. Tosti, L. Brévard, C. Tabone, P. Gaud, S. Barraud, T. Ernst, S. Deleonibus, "Planar Fully Depleted SOI Technology: a powerful architecture for the 20nm node and beyond," IEDM 2010.

[57] **(LETI-FD-23)** C. Le Royer, A. Villalon, M. Casse, D. Cooper, J. Mazurier, B. Previtali, C. Tabone, P. Perreau, J.-M. Hartmann, P. Scheiblin, F. Allain, F. Andrieu, O. Weber, P. Batude, O. Faynot, T. Poiroux, "First Demonstration of Ultrathin Body c-SiGe channel FDSOI pMOSFETs combined with SiGe RSD: Drastic Improvement of Electrostatics ($V_{th,p}$ tuning, DIBL) and Transport (μ_0, I_{sat}) Properties down to 23nm Gate Length," IEDM Tech. Dig., 2011, pp.394-397.

[58] **(ST-FD-30)** C. Fenouillet-Beranger, P. Perreau, L. Pham-Nguyen, S. Denorme, F. Andrieu, L. Tosti, L. Brevard, O. Weber, S. Barnola, T. Salvetat, X. Garros, M. Cassé, C. Leroux, J.P Noel, O. Thomas, B. Le-Gratiet, F. Baron, M. Gatefait, Y. Campidelli, F. Abbate, C. Perrot, C. de-Buttet, R. Beneyton, L. Pinzelli1, F. Leverd1, P. Gouraud, M. Gros-Jean, A. Bajolet, C. Mezzomo, C. Leyris, S. Haendler, D. Noblet, R.Pantel, A. Margain, C. Borowiak, E. Josse, N. Planes, D. Delprat, F. Boedt, K. Bourdelle, B.Y. Nguyen, F. Boeuf, O. Faynot, T.Skotnicki, "Hybrid FDSOI/Bulk high-k/Metal Gate platform for Low Power (LP) multimedia technology," IEDM 2009.

[59] **(IBM-Fin-25)** V. S. Basker, T. Standaert, H. Kawasaki, C.-C. Yeh, K. Maitra, T. Yamashita, J. Faltermeier, H. Adhikari. H. Jagannathan, J. Wang, H. Sunamura, S. Kanakasabapathy, S. Schmitz, J. Cummings, A. Inada, C. -H. Lin, P. Kulkarni, Y. Zhua, J. Kuss, T. Yamamoto, A. Kumara, J. Wahl, A. Yagishita, L. F. Edge, R. H. Kim, E. Mclellan, S. J. Holmes, R. C. Johnson, T. Levin, J. Demarest, M. Hane, M. Takayanagi, M. Colburn, V. K. Paruchuri, R. J. Miller, H. Bu, B. Doris, D. McHerron, E. Leobandung and J. O'Neill, "A 0.063 μm^2 FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch," VLSI 2010.

[60] **(IBM-Fin-25)** K. Maitra, A. Khakifirooz, P. Kulkarni, V. S. Basker, J. Faltermeier, H. Jagannathan, H. Adhikari, C.-C. Yeh, N. R. Klymko, K. Saenger, T. Standaert, Robert J. Miller, Bruce Doris, V. K. Paruchuri, Dale McHerron, James O'Neil, E. Leobundung, H. Bu, "Aggressively Scaled Strained-Silicon-on-Insulator Undoped-Body High-k/Metal-Gate nFinFETs for High-Performance Logic Applications," IEEE Electron Device Letters, vol.32, no.6, 2011, pp.713-715

[61] **(Intel-Fin)** J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosaljevic, U. Shah, N. Zelick, R. Chau, "Tri-Gate

Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering," Symp. on VLSI Tech. Dig., 2006.

[62] **(TSMC-Fin-22)** C.C. Wu, D.W. Lin, A. Keshavarzi, C.H. Huang, C.T. Chan, C.H. Tseng, C.L. Chen, C.Y. Hsieh, K.Y. Wong, M.L. Cheng, T.H. Li, Y.C. Lin, L.Y. Yang, C.P. Lin, C.S. Hou, H.C. Lin, J.L. Yang, K.F. Yu, M.J. Chen, T.H. Hsieh, Y.C. Peng, C.H. Chou, C.J. Lee, C.W. Huang, C.Y. Lu, F.K.Yang, H.K. Chen, L.W. Weng, P.C. Yen, S.H. Wang, S.W. Chang, S.W. Chuang, T.C. Gan, T.L. Wu, T.Y. Lee, W.S. Huang, Y.J. Huang, Y.W. Tseng, C.M. Wu, Eric Ou-Yang, K.Y. Hsu, L.T. Lin, S.B. Wang, T.M. Kwok, C.C. Su, C.H. Tsai, M.J. Huang, H.M. Lin, A.S. Chang, S.H. Liao, L.S. Chen, J.H. Chen, P.S. Lim, X.F. Yu, S.Y. Ku, Y.B. Lee, P.C. Hsieh, P.W. Wang, Y.H. Chiu, S.S. Lin, H.J. Tao, M. Cao, Y.J. Mii, "High Performance 22/20nm FinFET CMOS Devices with Advanced High-K/Metal Gate Scheme," IEDM Tech Dig., 2010.

Chapter 2

Stress-induced Performance Enhancement in Ultra-thin-body Fully Depleted SOI MOSFET

2.1 Introduction

The ultra-thin-body (UTB) Fully Depleted SOI (FD-SOI) MOSFET structure exhibits excellent short-channel control and reduced variability [1] to enable CMOS technology scaling beyond the 15nm node. Previous studies have shown that channel stress can be used to boost the performance of UTB MOSFETs [2, 3], but these were focused on relatively low stress levels or long-channel devices.

In this chapter, the limits of stress-induced performance enhancement in FD-SOI MOSFETs with gate length and body thickness scaling are assessed. In Section 2.2, the Poisson-Schrödinger self-consistent method is introduced to calculate the carrier sub-band structures in FD-SOI inversion layers, followed by the modeling approach of carrier scattering rates and mobilities. In Section 2.3, the stress impacts on FD-SOI MOSFETs are studied via both experiments and quantum mechanical simulations. Stress-induced performance enhancement trend is projected at aggressively scaled device dimensions. Section 2.4 summarizes the conclusions from these works.

2.2 Modeling for Inversion Carrier Sub-band Structures and Low-field Mobilities

2.2.1 Poisson-Schrödinger Self-consistent Solving Approach

For electrons, the effective mass approximation is used herein; the one-dimensional (1-D) stationary Schrödinger equation can be expressed as:

$$\left(-\frac{\hbar^2}{2m^*_z}\cdot\frac{d^2}{dz^2}-e\varphi(z)\right)\xi_n(z)=E_n\xi_n(z) \tag{2.1}$$

where m^*_z are the electron effective mass along the confinement (defined as z) direction, and have the values for different surface orientations as listed in Tab. 2.1.

(100)-surface	m^*_z
Δ2-valley	0.915
Δ4-valley	0.196
(110)-surface	m^*_z
Δ2-valley	0.196
Δ4-valley	0.196

Table 2.1. Electron effective mass values used in 1-D Schrödinger equation.

By using the finite difference method, the electron wavefunction derivatives at position $z=i$ can be expressed as:

$$\frac{d}{dz}\xi(z)=\frac{\xi_{z_{i+1}}-\xi_{z_{i-1}}}{dz_{i+1}+dz_i} \tag{2.2}$$

$$\frac{d^2}{dz^2}\xi(z)=\frac{2\left[\frac{\xi_{z_{i+1}}-\xi_{z_i}}{dz_{i+1}}-\frac{\xi_{z_i}-\xi_{z_{i-1}}}{dz_i}\right]}{dz_{i+1}+dz_i} \tag{2.3}$$

the LHS of (2.1) can be written as:

$$\begin{aligned}&\left(-\frac{\hbar^2}{2m^*_z}\cdot\frac{d^2}{dz^2}-e\cdot\varphi(z)\right)\xi_n(z)\\&\Rightarrow-\frac{\hbar^2}{2m^*_z}\cdot\frac{2\left[dz_i\xi_{i+1}-(dz_i+dz_{i+1})\xi_i+dz_{i+1}\xi_{i-1}\right]}{(dz_i+dz_{i+1})dz_i dz_{i+1}}-e\cdot\varphi_i\cdot\xi_i\end{aligned} \tag{2.4}$$

The total Hamiltonian can be constructed based on the 1-D real space meshing (with *n* mesh points along z-direction):

$$H_{total}=\begin{bmatrix}
\left[H_0^1\right] & \left[H_{+1}^1\right] & & & & \\
\left[H_{-1}^2\right] & \left[H_0^2\right] & \left[H_{+1}^2\right] & & & \\
 & \ddots & \ddots & & & \\
 & & \left[H_{-1}^i\right] & \left[H_0^i\right] & \left[H_{+1}^i\right] & \\
 & & & \ddots & \ddots & \ddots \\
 & & & & \left[H_{-1}^{n-1}\right] & \left[H_0^{n-1}\right] & \left[H_{+1}^{n-1}\right] \\
 & & & & & \left[H_{-1}^n\right] & \left[H_0^n\right]
\end{bmatrix} \tag{2.5}$$

with those diagonal elements expressed as:

$$H_0^i=\frac{\hbar^2}{m^*_z}\cdot\frac{1}{dz_{i-1}\cdot dz_i}-e\cdot\varphi_i \tag{2.6}$$

$$H_{-1}^i=-\frac{\hbar^2}{m^*_z}\cdot\frac{1}{dz_i\cdot\left(dz_{i-1}+dz_i\right)} \tag{2.7}$$

$$H_{+1}^i=-\frac{\hbar^2}{m^*_z}\cdot\frac{1}{dz_{i-1}\cdot\left(dz_{i-1}+dz_i\right)} \tag{2.8}$$

For holes, starting with the 6×6 k·p Luttinger-Kohn Hamiltonian as shown below [4, 5],

$$\begin{bmatrix}
-P-Q & L & -M & 0 & \frac{L}{\sqrt{2}} & -\sqrt{2}M \\
-L^+ & -P+Q & 0 & -M & \sqrt{2}Q & -\sqrt{\frac{3}{2}}L \\
-M^+ & 0 & -P+Q & -L & -\sqrt{\frac{3}{2}}L^+ & -\sqrt{2}Q \\
0 & -M^+ & -L^+ & -P-Q & \sqrt{2}M^+ & \frac{L^+}{\sqrt{2}} \\
\frac{L^+}{\sqrt{2}} & \sqrt{2}Q & -\sqrt{\frac{3}{2}}L & \sqrt{2}M & -P-\Delta & 0 \\
-\sqrt{2}M^+ & -\sqrt{\frac{3}{2}}L^+ & -\sqrt{2}Q & \frac{L}{\sqrt{2}} & 0 & -P-\Delta
\end{bmatrix} \tag{2.9}$$

with P, Q, L, M defined as:

$$P=\frac{\hbar^2}{2m_0}\gamma_1(k_x^2+k_y^2+k_z^2) \tag{2.10}$$

$$Q=\frac{\hbar^2}{2m_0}\gamma_2(k_x^2+k_y^2-2k_z^2) \tag{2.11}$$

$$L=\frac{\hbar^2}{m_0}\sqrt{3}\gamma_3(k_x-ik_y)k_z \tag{2.12}$$

$$M = -\frac{\hbar^2}{2m_0}\sqrt{3}[\gamma_2(k_x^2 - k_y^2) - i2\gamma_3 k_x k_y) \tag{2.13}$$

and by using the finite difference method, those quantities can be expressed together with hole's wavefunction derivatives at each real-space meshing point ($z=i$).

For (100)-oriented surface:

$$P \Rightarrow \frac{\hbar^2}{2m_0}\gamma_1(k_x^2 + k_y^2 - \frac{d^2}{dz^2}) \tag{2.14}$$

$$\therefore P\xi(y,z) = \frac{\hbar^2}{2m_0}\gamma_1\left\{(k_x^2 + k_y^2 + \frac{2}{dz_i \cdot dz_{i+1}})\cdot\xi_{z_i} - \frac{2}{dz_i\cdot(dz_{i+1}+dz_i)}\cdot\xi_{z_{i-1}} - \frac{2}{dz_{i+1}\cdot(dz_{i+1}+dz_i)}\cdot\xi_{z_{i+1}}\right\}$$

$$Q \Rightarrow \frac{\hbar^2}{2m_0}\gamma_2(k_x^2 + k_y^2 + 2\cdot\frac{d^2}{dz^2}) \tag{2.15}$$

$$\therefore Q\xi(y,z) = \frac{\hbar^2}{2m_0}\gamma_2\left\{(k_x^2 + k_y^2 - \frac{4}{dz_i\cdot dz_{i+1}})\cdot\xi_{z_i} + \frac{4}{dz_i\cdot(dz_{i+1}+dz_i)}\cdot\xi_{z_{i-1}} + \frac{4}{dz_{i+1}\cdot(dz_{i+1}+dz_i)}\cdot\xi_{z_{i+1}}\right\}$$

$$L \Rightarrow \frac{\hbar^2}{2m_0}2\sqrt{3}\gamma_3(k_x - ik_y)(-i\frac{d}{dz}) = \frac{\hbar^2}{2m_0}2\sqrt{3}\gamma_3(-i\cdot k_x\frac{d}{dz} - k_y\frac{d}{dz}) \tag{2.16}$$

$$\therefore L\xi(y,z) = \frac{\hbar^2}{2m_0}2\sqrt{3}\gamma_3\left\{\frac{-i\cdot k_x - k_y}{dz_i + dz_{i+1}}\cdot\xi_{z_{i+1}} + \frac{i\cdot k_x - k_y}{dz_i + dz_{i+1}}\cdot\xi_{z_{i-1}}\right\}$$

M will remain the same as that in the bulk k·p Hamiltonian. The total Hamiltonian for holes can be constructed similarly as has been done for electrons.

The 1-D Poisson equation can be expressed as

$$\frac{d}{dz}\left(\varepsilon(z)\cdot\frac{d\phi(z)}{dz}\right) = -e\left(N_D - N_A + p(z) - n(z)\right) \tag{2.17}$$

which also has the form of second-order differentials as the Schrödinger equation, and hence can also be solved using the similar Hamiltonian as in eqn. (2.5), leaving the potential profile $\varphi(z)$ as the variable to be updated during each iteration step. The sub-band charge profile is calculated as

$$n_n(z) = \frac{g_n}{(2\pi)^2}\int_{\vec{k}} d\vec{k}\cdot f(E_{\vec{k}})\cdot\left|\xi_n(\vec{k},z)\right|^2 \tag{2.18}$$

where g is the spin or valley degeneracy, and $f(E_k)$ is the Fermi-Dirac distribution function. And the total charge profile in the RHS of eqn. (2.17) is the summation of all sub-band charges, with the form

$$n(z) = \sum_n n_n(z) \tag{2.19}$$

Once the numerical convergence is reached between the Poisson and Schrödinger equation, the final carrier sub-band structures and charge profiles can be output.

2.2.2 Inversion Layer Carrier Mobility

With the output of the self-consistent Poisson-Schrödinger solver, carrier mobility can be calculated based on the Kubo-Greenwood formalism, which describes the response of a quantum mechanical system to an external field, (e.g. the change of the current due to an electric field), whereby it is assumed that the perturbation is small and therefore the relation between field and current is linear [6]. In general, in inversion layers, the carrier mobility for a certain sub-band can be expressed as [4, 7]

$$\mu_{i,j}^{n} = \frac{e}{\hbar^2} \cdot \frac{1}{k_B T} \cdot \frac{g_n}{n_n} \int_{\vec{k}} \frac{d\vec{k}}{(2\pi)^2} \cdot \tau_{i,j}^{n} \cdot \frac{\partial E_n}{\partial k_i} \cdot \frac{\partial E_n}{\partial k_j} \cdot f(E_n) \cdot (1 - f(E_n)) \tag{2.20}$$

where $\tau_{i,j}$ refers to the momentum relaxation time (MRT) in the direction (i, j) of the momentum space. The total mobility value is the weighted average of all sub-band mobility values with respect to their inversion charge concentration, and has the form:

$$\mu_{i,j}^{tot} = \frac{1}{n_{tot}} \sum_{n} n_n \cdot \mu_{i,j}^{n} \tag{2.21}$$

The inverse of MRT for the n-th sub-band can be derived as [4, 7]:

$$\frac{1}{\tau_n(\vec{k})} = \sum_{n'} \int_{\vec{k}'} \frac{d\vec{k}'}{(2\pi)^2} \cdot S_{n\vec{k},n'\vec{k}'} \times \Phi(n\vec{k}, n'\vec{k}') \tag{2.22}$$

where $S_{n,n'}$ refers to the transition rate between different sub-bands and Φ is called the momentum relaxation factor, describing the anisotropicity of those transitions [4]. According to Fermi-Golden rule theorem, the transition rate between two quantum states can be calculated as

$$S_{n\vec{k},n'\vec{k}'} = \frac{2\pi}{\hbar} \left| M(n, \vec{k}, n', \vec{k}') \right| \cdot \delta(E_n(\vec{k}) - E_{n'}(\vec{k}') \pm \hbar\omega) \tag{2.23}$$

where $M_{n,k,n',k'}$ stands for the matrix element for a scattering event from sub-band n, state k to sub-band n', state k'; and $\hbar\omega$ refers to the energy change during the transition event. The key part left is to decide the matrix element for different scattering mechanisms. Phonon and surface roughness scatterings are considered herein.

As derived in [4, 8, 9], the matrix element for elastic phonon scattering can be written as

$$M_{elast.}(n, \vec{k}, n', \vec{k}') = \frac{k_B T \Xi^2}{\rho u_l^2} \cdot F_{n,\vec{k},n',\vec{k}'} \tag{2.24}$$

where Ξ is the effective deformation potential by averaging different phonon modes (i.e. longitudinal and transverse), ρ is mass density, u_l is the longitudinal sound velocity and F is the form factor as defined in **chapter 1**, standing for the quantum mechanical probability of a certain transition. The inelastic phonon scattering matrix element can be written as [4, 8, 9]

$$M_{inelast.}(n, \vec{k}, n', \vec{k}') = \frac{\hbar^2 \pi (D_t k)^2}{2\rho(\hbar\omega)} \cdot F_{n,\vec{k},n',\vec{k}'} \cdot \left(n_{op}(\hbar\omega) + \frac{1}{2} \mp \frac{1}{2} \right) \tag{2.25}$$

where $D_t k$ is the optical deformation potential, and n_{op} is the Bose-Einstein occupation number, can be expressed as

$$n_{op}(\hbar\omega) = \frac{1}{e^{\frac{\hbar\omega}{k_B T}} - 1} \tag{2.26}$$

In eqn. (2.25) the "-" sign is for the optical absorption process while the "+" sign is for the emission process.

The surface roughness at Silicon/oxide interface is always modeled as the power spectrum density (PSD) function $S(q)$, and can have the Gaussian or exponential distribution with respect to the root-mean-square (RMS) amplitude of the roughness [10, 11]. For electrons, the matrix element can be written as [11]

$$M_{surf.rough.}(n,\vec{k},n',\vec{k'}) = \left| \int_z \xi_n(z)\cdot\vec{F}\cdot\xi_{n'}(z)dz + \left(E_n^0 - E_{n'}^0\right)\int_z \frac{d\xi_{n'}(z)}{dz}\cdot\xi_n(z)dz \right|^2 \cdot S(\vec{q}) \tag{2.27}$$

and for holes,

$$M_{surf.rough.}(n,\vec{k},n',\vec{k'}) = \left| \frac{d\overrightarrow{\xi_{n',0}}(0)}{dz}\cdot \mathrm{H}_{bulk}^{6\times6}\cdot\frac{d\overrightarrow{\xi_{n,0}}(0)}{dz} \right|^2 \cdot S(\vec{q}) \tag{2.28}$$

with $H^{6\times6}{}_{bulk}$ as the polynomial expansion of 6×6 k·p Hamiltonian [12].

At high inversion charge concentration, the screening effect has to be taken into account in mobility calculations. Lindhard screening model is used herein, which considers the matrix element has the following form after screening [13].

$$\left|M_{screen}(n,\vec{k},n',\vec{k'})\right|^2 = \frac{\left|M_{unscr.}(n,\vec{k},n',\vec{k'})\right|^2}{\varepsilon^2(\vec{q})} \tag{2.29}$$

where $\epsilon(q)$ is the dielectric function, depending on the wave vector change q during a scattering event, and can be further expressed as:

$$\varepsilon(\vec{q}) = 1 + \sum_n \frac{e^2}{2\varepsilon_s q}\cdot F_{nn}(\vec{q})\cdot\Pi_{nn}(\vec{q}) \tag{2.30}$$

where ϵ_s is the Silicon static dielectric constant, F is the form factor, and can be expressed as [14]

$$F_{nn}(\vec{q}) = \int_z dz\int_{z'} dz' \left|\xi_n(z)\right|^2\cdot\left|\xi_n(z')\right|^2\cdot\frac{e^{-q\left|z-z'\right|} + \tilde{\varepsilon}e^{-q\left|z+z'\right|} + \tilde{\varepsilon}e^{-2qt_{SOI}}\left(e^{q\left|z-z'\right|} + \tilde{\varepsilon}e^{q\left|z-z'\right|}\right)}{1-\tilde{\varepsilon}^2 e^{-2qt_{SOI}}} \tag{2.31}$$

with t_{SOI} as the body thickness, and the joint dielectric constant between Silicon and oxide as

$$\varepsilon = \frac{\varepsilon_s - \varepsilon_{ox}}{\varepsilon_s + \varepsilon_{ox}} \tag{2.32}$$

The other q-dependent term in eqn. 2.30 is the structural factor, and can be expressed as [13, 14]

$$\Pi_{nn}(\vec{q}) = \frac{g_n}{(2\pi)^2}\int_{\vec{k}} d\vec{k}\cdot\frac{f(E_{n,\vec{k}}) - f(E_{n,\vec{k}-\vec{q}})}{E_{n,\vec{k}-\vec{q}} - E_{n,\vec{k}}} \tag{2.33}$$

2.3 Stress-induced Performance Enhancement in Fully Depleted SOI MOSFET: Impacts of Scaling

2.3.1 Impact of Body Thickness Scaling

FD-SOI MOSFETs with undoped <110>-oriented channels and high-κ/metal gate stacks (1.2nm equivalent oxide thickness) were fabricated on (100) substrates [1]. The body thickness (t_{SOI}) is 7nm, and BOX thickness is 10nm. No capping stressor layer is used in this work. Inversion-layer mobility values for long-channel devices were extracted using the split-CV method. A bending apparatus was used to induce uniaxial in-plane stress [15]. To study mobility enhancement in FD-SOI MOSFETs at very high levels of stress, and the impact of body-thickness scaling, the Poisson-Schrödinger self-consistent solver was used to calculate the sub-band structure and carrier mobility values. Phonon and surface roughness scattering, as well as dielectric screening effect are considered herein. To analyze the impact of stress on short-channel FD-SOI MOSFET performance, the parameter extraction procedure developed in [16, 17] was used: first, the improved Y-function approach is used to extract gate-bias-dependent source/drain series resistance (R_{sd}); next, the method introduced in [18] is used to calculate inversion charge, accounting for V_{th} shift; from these, the linear-region ($|V_{ds}|$=10mV) carrier apparent mobility and ON-state ($|V_{ds}|$=1V) velocity are calculated.

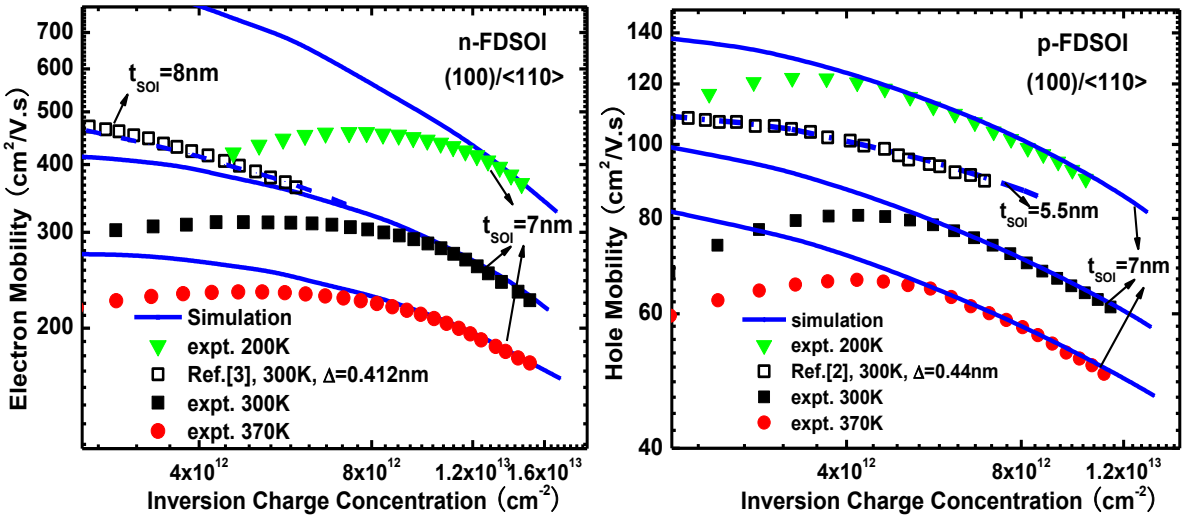

Figure 2.1, Measured and simulated (left) electron (right) hole mobility vs. inversion charge concentration in L_g=10um FD-SOI MOSFETs, at various temperatures. Dashed lines/open symbols compare results for devices with SiO_2/poly-Si gate stacks [2, 3].

Fig. 2.1 compares the extracted long-channel electron and hole mobility data against simulations, at various temperatures. The discrepancy at low carrier concentrations is likely due to remote Coulomb/phonon scattering caused by the high-κ/metal gate stack [19], since no similar discrepancy exists between simulations and measured data for devices with SiO_2/poly-Si gate stacks [2, 3].

To provide guidance for optimization of FD-SOI stress engineering, the effects of different directional stresses were measured at low levels of stress and simulated for stress levels up 1.6 Giga-Pascal (GPa), as shown in Fig. 2.2. The corresponding equi-energy contours for the 1st electron and hole sub-bands are shown in Fig. 2.3. Fig. 2.2 (left) shows how the relative change in electron mobility (μ_e) varies with the level and direction of stress. μ_e is most sensitive to longitudinal stress. As the inversion charge concentration increases, the incremental increase in enhancement decreases due to less inter-valley scattering reduction and sub-band reoccupation effects. (Shear-stress induced transport mass reduction only moderately improves μ_e.) A high level of transverse tensile stress degrades μ_e, which results from the increased transport mass (as shown in Fig.2.3). Fig. 2.2 (right) shows how the relative change in hole mobility (μ_h) increases with the level and direction of stress. In contrast to the situation for μ_e, no strong decrease in incremental μ_h enhancement is seen at high inversion charge concentrations. Longitudinal compressive stress reduces the hole transport mass and can greatly enhance μ_h. Vertical (<001> direction) tensile stress changes the sub-band curvature/occupation rate and thereby reduces hole intra-/inter-sub-band scatterings separately.

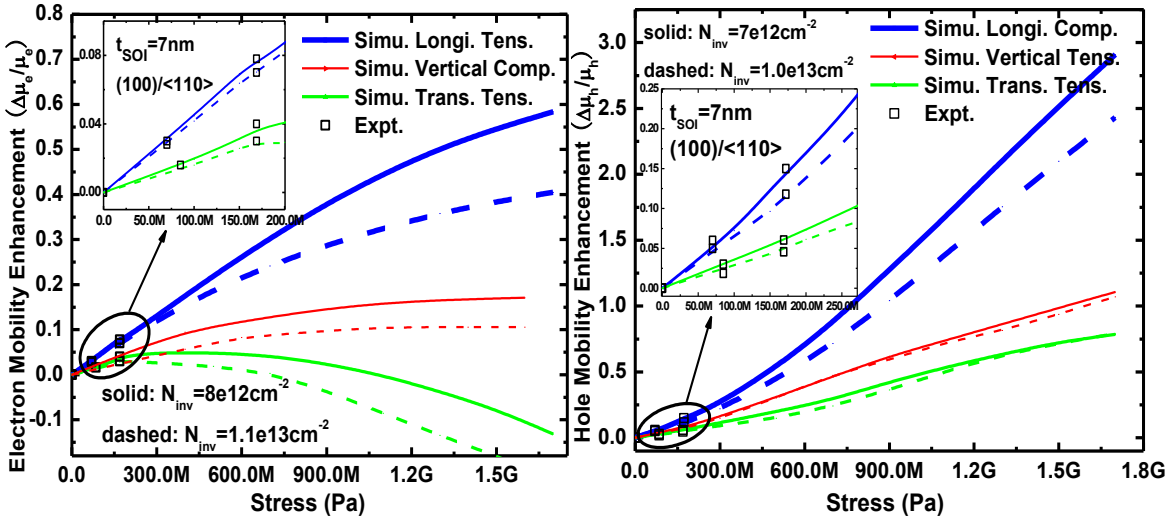

Figure 2.2, (left) electron and (right) hole mobility enhancement for different induced stress. The insets elucidate the comparisons between measured data (L_g=10um) and simulations.

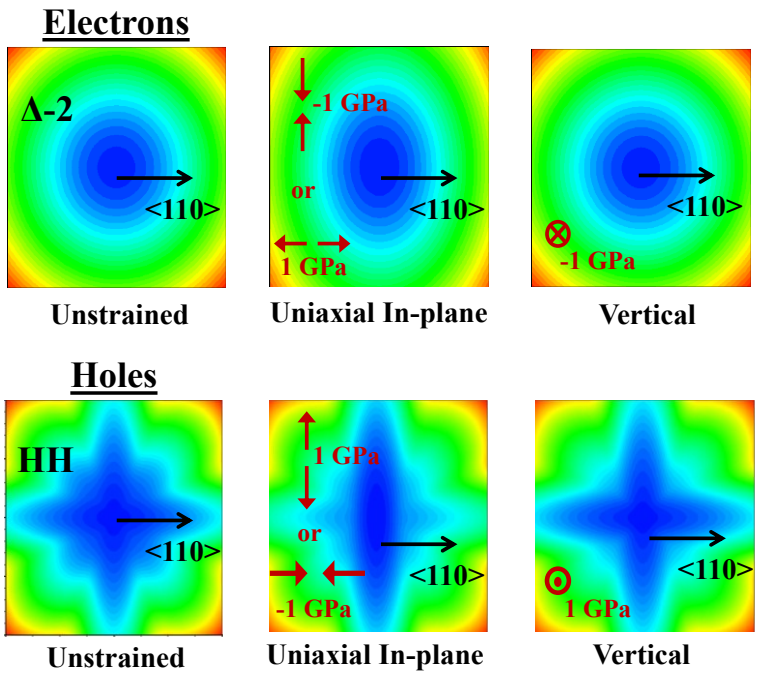

Figure 2.3, Equi-energy contours for the 1st subband of inversion electrons and holes (within ±0.2 Brillouin zone) in FD-SOI MOSFET, w/o stress and with 1GPa uniaxial stress.

Since the body thickness should be scaled down in proportion to the gate length to maintain good electrostatic integrity, it is important to examine the impact of t_{SOI} scaling on stress-induced mobility enhancement. Using the calibrated simulator, the changes in (100)/<110> μ_e and μ_h induced by 1GPa uniaxial stress are calculated and plotted as a function of t_{SOI} in Fig. 2.4. For electrons, only vertical compressive and longitudinal tensile stresses are considered in light of the results in Fig. 2.4 (left). μ_e for unstrained Silicon increases slightly as t_{SOI} is reduced below 4.5nm, due to quantum-confinement-induced sub-band splitting resulting in carrier reoccupation among the Δ-2 and Δ-4 valleys [20]. The benefit of stress for enhancing μ_e is diminished in this regime. In contrast, μ_h for unstrained Si decreases as t_{SOI} is reduced below 5nm. The benefit of stress for enhancing μ_h is maintained to lower values of t_{SOI} due to the large reduction in hole transport mass under shear stress.

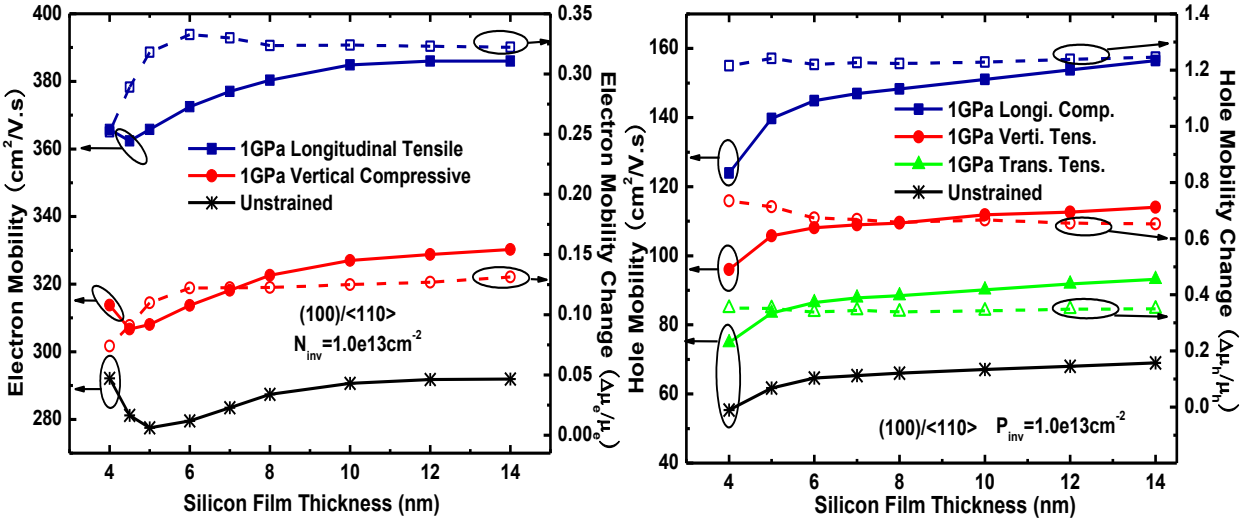

Figure 2.4, Simulated (left) electron and (right) hole mobility (solid lines) and relative enhancement (dashed lines) vs. silicon film thickness (t_{SOI}) for different stress components of 1GPa.

2.3.2 Impact of Gate Length Scaling

Fig. 2.5 plots the extracted short-channel FD-SOI MOSFET apparent mobility values as a function of gate length, for various temperatures. Degradation with gate length scaling is clearly seen and can be due to ballistic transport as well as enhanced Coulomb scatterings, since the defect density within the high-κ dielectric is higher near to the gate edges [21]. (The steeper degradation with gate length scaling at lower temperature supports this explanation.) Fig. 2.6 shows the extracted ON-state carrier limiting velocities. These are limited by scattering, as evidenced by their dependence on temperature.

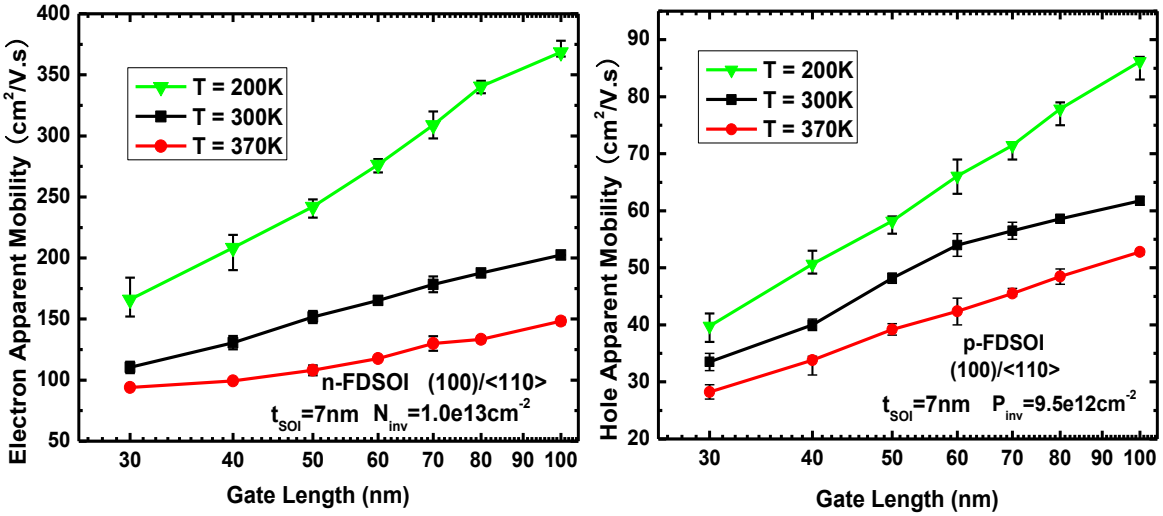

Figure 2.5, Extracted (left) electron and (right) hole apparent mobility vs. gate length from short channel FD-SOI MOSFETs measurement, at different temperatures.

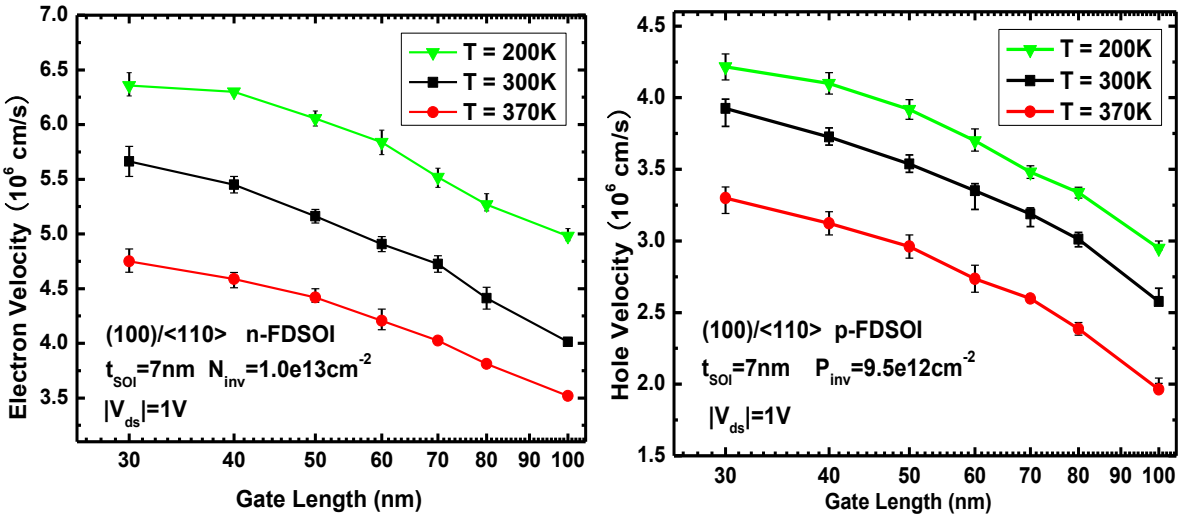

Figure 2.6, Extracted (left) electron and (right) hole limiting velocity vs. gate length from short channel FD-SOI MOSFETs measurement, at different temperatures

The relative change in apparent mobility induced by longitudinal bending stress is plotted together with the relative change in linear-region current ($I_{d,lin}$), as a function of gate length, in Fig. 2.7. Stress-induced mobility enhancement is maintained with gate length scaling, since it stems from a reduction in carrier transport mass under shear stress. $I_{d,lin}$ enhancement decreases with gate length scaling because parasitic source/drain resistance is less sensitive to stress (so that it becomes more dominant in short gate length devices). As shown in Fig. 2.8, velocity enhancement is maintained with gate length scaling. This is because carrier velocity is strongly correlated to the apparent mobility. It is interesting to note that the α coefficient (ratio of relative changes in mobility and velocity [22]) is 0.6 for n-channel FD-SOI MOSFETs and 0.5 for p-channel FD-SOI MOSFETs.

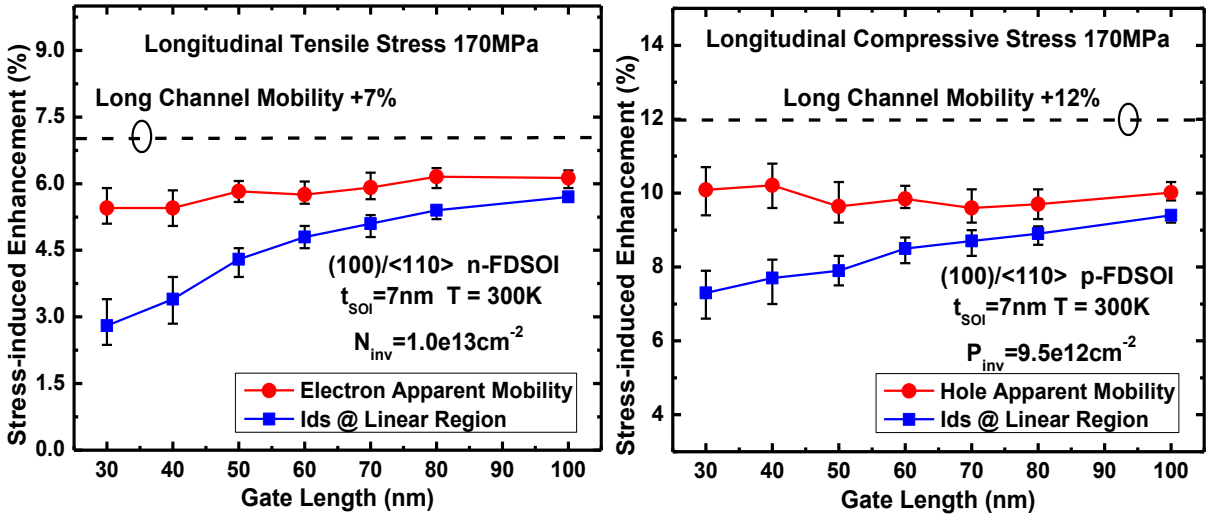

Figure 2.7, Measured (left) electron and (right) hole apparent mobility change vs. gate length, for applied longitudinal stress, and corresponding linear region ($|V_{ds}|$=10mV) current change.

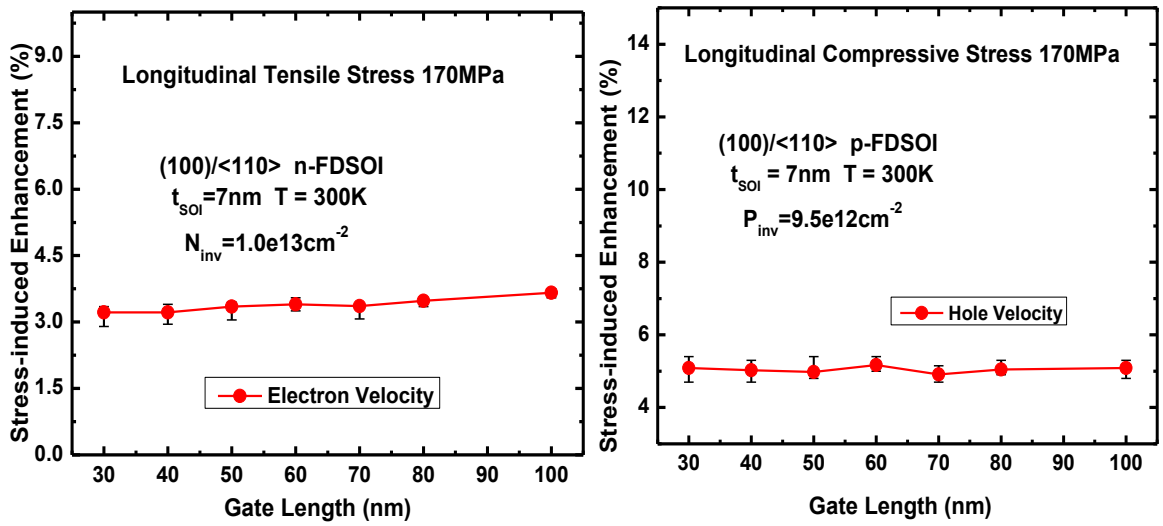

Figure 2.8, Measured (left) electron and (right) hole limiting velocity change vs. gate length under applied longitudinal stress.

2.4 Summary

Stress-induced carrier mobility enhancement in FD-SOI MOSFETs diminishes with scaling body thickness below 5nm for electrons but maintains for holes, which results from the different physical mechanisms between electrons and holes. The benefits of stress for boosting apparent mobility and limiting velocity are maintained with gate length scaling.

2.5 References

[1] F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J-P. Noel, C. Fenouillet-Béranger, J-P. Mazellier, P. Perreau, T. Poiroux, Y. Morand, T. Morel, S. Allegret, V. Loup, S. Barnola, F. Martin, J-F. Damlencourt, I. Servin, M. Cassé, X. Garros, O. Rozeau, M-A. Jaud, G. Cibrario, J. Cluzel, A. Toffoli, F. Allain, R. Kies, D. Lafond, V. Delaye, C. Tabone, L. Tosti, L. Brévard, P. Gaud, V. Paruchuri, K.K. Bourdelle, W. Schwarzenbach, O. Bonnin, B-Y. Nguyen, B. Doris, F. Boeuf, T. Skotnicki, O. Faynot, "Low Leakage and Low Variability Ultr-Thin-Body and Buried Oxide (UT2B) SOI Technology for 20nm Low Power CMOS and Beyond," Symp. on VLSI Tech. Dig., 2010, pp.57-58.

[2] K. Shimizu, G. Tsutsui, T. Hiramoto, "Experimental Study on Mobility Universality in (100) Ultra-Thin Body nMOSFET with SOI Thickness of 5nm," IEEE Int. SOI Conf. Proc., 2006, pp.175-176.

[3] S. Kobayashi, M. Saitoh, K. Uchida, "More-than-Universal Mobility in Double-Gate SOI p-FETs with Sub-10nm Body Thickness – Role of Light-Hole Band and Compatibility with Uniaxial Stress Engineering," IEDM Tech. Dig., 2007, pp.707-710.

[4] M.V. Fischetti, Z. Ren, P.M. Solomon, M. Yang, K. Rim, "Six-band kp calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain and silicon thickness," AIP Journal of Applied Physics, vol.94, no.2, 2003, pp.1079-1095.

[5] Y. Sun, S.E. Thompson, T. Nishida, "Physics of Strain Effects in Semiconductors and metal-oxide-semiconductor field-effect transistors," AIP Journal of Applied Physics, vol.101, issue 10, 2007, 104503.

[6] R. Kubo, "Statistical-Mechanical Theory of Irreversible Processes: I. General Theory and Simple Applications to Magnetic and Conduction Problems," Journal of the Physical Society of Japan, Vol.12, 1957, pp.570-586.

[7] R. Kotlyar, M.D. Giles, P. Matagne, B. Obradovic, L. Shifren, M. Stettler, E. Wang, "Inversion Mobility and Gate Leakage in High-k/Metal Gate MOSFETs," IEDM Tech. Dig., 2004, pp.391-394.

[8] D. Esseni, A. Abramo, L. Selmi, E. Sangiorgi, "Physically Based Modeling of Low Field Electron Mobility in Ultrathin Single- and Double-Gate SOI n-MOSFETs," IEEE Transactions on Electron Devices, Vol.50, no.12, 2003, pp.2445-2454.

[9] A.T. Pham, C. Jungemann, B. Meinerzhagen, "Physics-Based Modeling of Hole Inversion-Layer Mobility in Strained-SiGe-on-Insulator," IEEE Transactions on Electron Devices, vol.54, no.9, 2007, pp.2174-2182.

[10] L. Donetti, F. Gamiz, N. Rodriguez, A. Godoy, C. Sampedro, "The effect of surface roughness scattering on hole mobility in double gate Silicon-on-insulator devices," AIP Journal of Applied Physics, vol.106, 2009, 023705

[11] D. Esseni, "On the Modeling of Surface Roughness Limited Mobility in SOI MOSFETs and Its Correlation to the Transistor Effective Field," IEEE Transactions on Electron Devices, vol.51, no.3 2004, pp.394-401.

[12] A.T. Pham, C. Jungemann, B. Meinerzhagen, "Modeling of hole inversion layer mobility in unstrained and uniaxially strained Si on arbitrarily oriented substrates," Proc. of the 37th European Solid-State Device Research Conference (ESSDERC), pp.390-393, 2007.

[13] D. Esseni, A. Abramo, "Modeling of Electron Mobility Degradation by Remote Coulomb Scattering in Ultrathin Oxide MOSFETs," IEEE Transactions on Electron Devices, vol.50, no.7, 2003, pp.1665-1674.

[14] S. Jin, M.V. Fischetti, T.-W. Tang, "Modeling of Surface Roughness Scattering in Ultrathin-Body SOI MOSFETs," IEEE Transactions on Electron Devices, vol.54, no.9, 2007, pp.2191-2203.

[15] K. Uchida, T. Krishnamohan, K.C. Saraswat, Y. Nishi, "Physical Mechanism of Electron Mobility Enhancement in Uniaxial Stressed MOSFETs and Impact of Uniaxial Stress Engineering in Ballistic Regime," IEDM Tech. Dig. 2005, pp.49-52.

[16] D. Fleury, A. Cros, G. Bidal, J. Rosa, G. Ghibaudo, "A New Technique to Extract the Source/Drain Series Resistance of MOSFETs," IEEE Electron Device Letters, vol.30, no.9, 2009, pp.975-977.

[17] N. Xu, X. Sun, W. Xiong, C. R. Cleavelin and T.-J. King Liu, "MuGFET Carrier Mobility and Velocity: the Impacts of Fin Aspect Ratio, Orientation and Stress," IEDM Tech. Dig., 2010, p.194-197.

[18] A. Lochtefeld, D.A. Antoniadis, "On Experimental Determination of Carrier Velocity in Deeply Scaled NMOS: How Close to the Thermal Limit?" IEEE Electron Device Letters, vol.22, no.2, 2001, pp.95-97.

[19] F. Andrieu, O. Faynot, X. Garros, D. Lafond, C. Buj-Dufournet, L. Tosti, S. Minoret, V. Vidal, J.C. Barbe, F. Allain, E. Rouchouze, L. Vandroux, V. Cosnier, M. Casse, V. Delaye, C. Carabasse, M. Burdin, G. Rolland, B. Guillaumot, J.P. Colonna, P. Besson, L. Brevard, D. Mariolle, P. Holliger, A. Vandooren, C. Fenouillet-Beranger, F. Martin, S. Deleonibus,

"Comparative Scalability of PVD and CVD TiN on HfO_2 as a Metal Gate Stack for FDSOI cMOSFETs down to 25nm Gate Length and Width," IEDM Tech. Dig., 2006.
[20] K. Uchida, M. Saitoh, S. Kobayashi, "Carrier Transport and Stress Engineering in Advanced Nanoscale Transistors From (100) and (110) Transistors to Carbon Nanotube FETs and Beyond," IEDM Tech. Dig., 2008, pp.569-572.
[21] C.-C. Lu, K.-S. Chang-Liao, C.-H. Tsao, T.-K. Wang, "Comparison of positive and negative bias-temperature instability on MOSFETs with HfO_2/LaO_x and HfO_2/AlO_x Dielectric Stacks," Solid-State Electronics, vol.53, 2010, pp.1474-1478.
[22] M. Saitoh, N. Yasutake, Y. Nakabayashi, K. Uchida, T. Numata, "Understanding of Strain Effects on High-Field Carrier Velocity in (100) and (110) CMOSFETs under Quasi-Ballistic Transport," IEDM Tech. Dig., 2009, pp.469-472.

Chapter 3

Multiple-Gate MOSFET Performance Enhancement via Strain Engineering

3.1 Introduction

Multiple-Gate MOSFET (MuGFET) structures such as the double-gate FinFET [1, 2] and Tri-gate [3, 4] FET are slated for adoption in sub-22 nm CMOS technology nodes due to their superior electrostatic integrity as compared to the conventional planar bulk MOSFET [5-8]. Recent experimental results show that the FinFET performs well even when the fin width is reduced to ~4 nm to enable gate length (L_g) scaling down to 10 nm [8]. Since strained-silicon technology is now used in high volume production to enhance the performance of planar bulk CMOS devices [9], it is important to examine how this technology should be adapted to MuGFET transistors to achieve the best possible performance.

This chapter presents the study of strain-induced carrier mobility enhancement for Multiple-Gate MOSFET (MuGFET) technology, with special attention to the impacts of different structural and process variations. In Section 3.2, the two-dimensional (2-D) Poisson-Schrödinger self-consistent simulator is described. In Section 3.3, the impacts of the MuGFET fin aspect ratio, orientation and stress design for improving performance are presented. Section 3.4 focuses on advanced FinFET devices, and compares the different uniaxial stressor technologies. Section 3.5 summarizes the conclusions from these works.

3.2 Two-Dimensional Poisson-Schrödinger Self-consistent Solver Development for Multiple-Gate MOSFET Simulations

For electrons, the effective mass approximation (EMA) is used herein; the 2-D stationary Schrödinger equation can be expressed using the finite difference method as:

$$\left(-\frac{\hbar^2}{2m^*_y}\cdot\frac{d^2}{dy^2}-\frac{\hbar^2}{2m^*_z}\cdot\frac{d^2}{dz^2}-e\varphi(y,z)\right)\xi_n(y,z)=E_n\xi_n(y,z) \tag{3.1}$$

where m^*_y and m^*_z are the electron effective masses along the fin width (y)-direction and fin height (z)-direction, and have the values as listed in Tab. 3.1.

<100>-fin	$\mathbf{m^*_y}$	$\mathbf{m^*_z}$
x-valley	0.196	0.196
y-valley	0.915	0.196
z-valley	0.196	0.915
<110>-fin	$\mathbf{m^*_y}$	$\mathbf{m^*_z}$
2-fold	0.196	0.915
4-fold	0.323	0.196

Table 3.1. Electron effective mass values used in 2-D Schrödinger equation.

By using the mesh strategy in Fig. 3.1, and since the wavefunction derivatives at position y=i, z=j can be expressed as:

$$\frac{d}{dy}\xi(y)=\frac{\xi_{y_{i+1}}-\xi_{y_{i-1}}}{dy_{i+1}+dy_i} \tag{3.2}$$

$$\frac{d^2}{dy^2}\xi(y)=\frac{2\left[\dfrac{\xi_{y_{i+1}}-\xi_{y_i}}{dy_{i+1}}-\dfrac{\xi_{y_i}-\xi_{y_{i-1}}}{dy_i}\right]}{dy_{i+1}+dy_i} \tag{3.3}$$

$$\frac{d}{dz}\cdot\frac{d}{dy}\xi(y,z)=\frac{d}{dz}\cdot\left(\frac{\xi_{y_{i+1}}-\xi_{y_{i-1}}}{dy_{i+1}+dy_i}\right)=\frac{\xi_{y_{i+1},z_{j+1}}+\xi_{y_{i-1},z_{j-1}}-\xi_{y_{i-1},z_{j+1}}-\xi_{y_{i+1},z_{j-1}}}{(dy_{i+1}+dy_i)(dz_{j+1}+dz_j)} \tag{3.4}$$

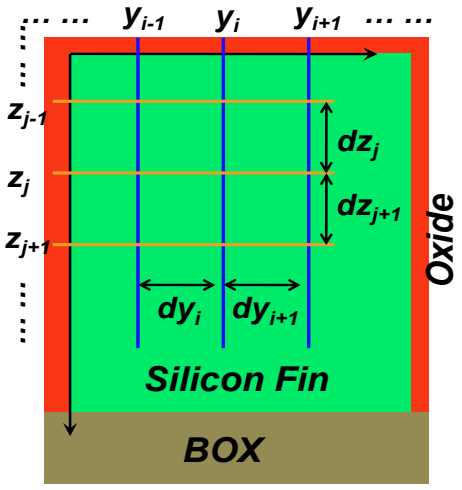

Figure 3.1, Schematic cross-section of simulated Multiple-Gate device structure showing the meshing strategy for the 2-D Poisson-Schrödinger solver.

the LHS of (3.1) can be written as:

$$\left(-\frac{\hbar^2}{2m^*_y}\cdot\frac{d^2}{dy^2}-\frac{\hbar^2}{2m^*_z}\cdot\frac{d^2}{dz^2}-e\cdot\varphi(y,z)\right)\xi_n(y,z)$$
$$\Rightarrow -\frac{\hbar^2}{2m^*_y}\cdot\frac{2\left[dy_i\xi_{i+1,j}-(dy_i+dy_{i+1})\xi_{i,j}+dy_{i+1}\xi_{i-1,j}\right]}{(dy_i+dy_{i+1})dy_i dy_{i+1}}\cdots$$
$$-\frac{\hbar^2}{2m^*_z}\cdot\frac{2\left[dz_j\xi_{i,j+1}-(dz_j+dz_{j+1})\xi_{i,j}+dz_{j+1}\xi_{i,j-1}\right]}{(dz_j+dz_{j+1})dz_j dz_{j+1}}-e\cdot\varphi_{i,j}\cdot\xi_{i,j} \tag{3.5}$$

The total Hamiltonian can be constructed based on the 2-D real space meshing (with n mesh points along the y-direction and m mesh points along the z-direction):

$$H_{total}=\begin{bmatrix}
\left[H_0^{1,1}\right] & \left[H_{+1}^{2,1}\right] & & & & \left[H_{+n}^{1,2}\right] & & \\
\left[H_{-1}^{1,1}\right] & \left[H_0^{2,1}\right] & \left[H_{+1}^{3,1}\right] & & & & \left[H_{+n}^{2,2}\right] & \\
 & \ddots & \ddots & \ddots & & & & \\
 & & \left[H_{-1}^{n-1,1}\right] & \left[H_0^{n,1}\right] & & & & \ddots \\
\left[H_{-n}^{1,1}\right] & & & 0 & \left[H_0^{1,2}\right] & \left[H_{+1}^{2,2}\right] & & \\
 & \ddots & & & \ddots & \ddots & \ddots & \\
 & & \left[H_{-n}^{n,m-1}\right] & & & \left[H_{-1}^{n-1,m}\right] & \left[H_0^{n,m}\right] &
\end{bmatrix} \tag{3.6}$$

with those diagonal elements expressed as:

$$H_0^{i,j}=\frac{\hbar^2}{m^*_y}\cdot\frac{1}{dy_{i+1}\cdot dy_i}+\frac{\hbar^2}{m^*_z}\cdot\frac{1}{dz_{j+1}\cdot dz_j}-e\cdot\varphi_{i,j} \tag{3.7}$$

$$H_{-1}^{i,j}=-\frac{\hbar^2}{m^*_y}\cdot\frac{1}{dy_i\cdot(dy_{i+1}+dy_i)} \tag{3.8}$$

$$H_{+1}^{i,j}=-\frac{\hbar^2}{m^*_y}\cdot\frac{1}{dy_{i+1}\cdot(dy_{i+1}+dy_i)} \tag{3.9}$$

$$H_{-n}^{i,j}=-\frac{\hbar^2}{m^*_z}\cdot\frac{1}{dz_j\cdot(dz_{j+1}+dz_j)} \tag{3.10}$$

$$H_{+n}^{i,j}=-\frac{\hbar^2}{m^*_z}\cdot\frac{1}{dz_{j+1}\cdot(dz_{j+1}+dz_j)} \tag{3.11}$$

For holes, the 6×6 Luttinger-Kohn k·p Hamiltonian is used,

$$\begin{bmatrix} -P-Q & L & -M & 0 & \frac{L}{\sqrt{2}} & -\sqrt{2}M \\ -L^{+} & -P+Q & 0 & -M & \sqrt{2}Q & -\sqrt{\frac{3}{2}}L \\ -M^{+} & 0 & -P+Q & -L & -\sqrt{\frac{3}{2}}L^{+} & -\sqrt{2}Q \\ 0 & -M^{+} & -L^{+} & -P-Q & \sqrt{2}M^{+} & \frac{L^{+}}{\sqrt{2}} \\ \frac{L^{+}}{\sqrt{2}} & \sqrt{2}Q & -\sqrt{\frac{3}{2}}L & \sqrt{2}M & -P-\Delta & 0 \\ -\sqrt{2}M^{+} & -\sqrt{\frac{3}{2}}L^{+} & -\sqrt{2}Q & \frac{L}{\sqrt{2}} & 0 & -P-\Delta \end{bmatrix} \tag{3.12}$$

with P, Q, L, M defined as:

$$P = \frac{\hbar^2}{2m_0}\gamma_1(k_x^2+k_y^2+k_z^2) \tag{3.13}$$

$$Q = \frac{\hbar^2}{2m_0}\gamma_2(k_x^2+k_y^2-2k_z^2) \tag{3.14}$$

$$L = \frac{\hbar^2}{m_0}\sqrt{3}\gamma_3(k_x-ik_y)k_z \tag{3.15}$$

$$M = -\frac{\hbar^2}{2m_0}\sqrt{3}[\gamma_2(k_x^2-k_y^2)-i2\gamma_3k_xk_y) \tag{3.16}$$

Using the finite difference method, those quantities can be expressed together with hole's wavefunction derivatives at each real-space meshing point ($y=i$, $z=j$).

For <100>-oriented fins:

$$P \Rightarrow \frac{\hbar^2}{2m_0}\gamma_1(k_x^2-\frac{d^2}{dy^2}-\frac{d^2}{dz^2})$$

$$\therefore P\xi(y,z) = \frac{\hbar^2}{2m_0}\gamma_1\left\{\begin{array}{l}(k_x^2+\frac{2}{dy_i\cdot dy_{i+1}}+\frac{2}{dz_j\cdot dz_{j+1}})\cdot\xi_{y_i,z_j}-\frac{2}{dy_{i+1}\cdot(dy_{i+1}+dy_n)}\cdot\xi_{y_{i+1},z_j} \\ -\frac{2}{dy_i\cdot(dy_{i+1}+dy_i)}\cdot\xi_{y_{i-1},z_j}-\frac{2}{dz_j\cdot(dz_{j+1}+dz_j)}\cdot\xi_{y_i,z_{j-1}}-\frac{2}{dz_{j+1}\cdot(dz_{j+1}+dz_j)}\cdot\xi_{y_i,z_{j+1}}\end{array}\right\}$$

(3.17)

$$Q \Rightarrow \frac{\hbar^2}{2m_0}\gamma_2(k_x^2-\frac{d^2}{dy^2}+2\cdot\frac{d^2}{dz^2})$$

$$\therefore Q\xi(y,z) = \frac{\hbar^2}{2m_0}\gamma_2\left\{\begin{array}{l}(k_x^2+\frac{2}{dy_i\cdot dy_{i+1}}-\frac{4}{dz_j\cdot dz_{j+1}})\cdot\xi_{y_i,z_j}-\frac{2}{dy_{i+1}\cdot(dy_{i+1}+dy_n)}\cdot\xi_{y_{i+1},z_j} \\ -\frac{2}{dy_i\cdot(dy_{i+1}+dy_i)}\cdot\xi_{y_{i-1},z_j}+\frac{4}{dz_j\cdot(dz_{j+1}+dz_j)}\cdot\xi_{y_i,z_{j-1}}+\frac{4}{dz_{j+1}\cdot(dz_{j+1}+dz_j)}\cdot\xi_{y_i,z_{j+1}}\end{array}\right\} \tag{3.18}$$

$$L \Rightarrow \frac{\hbar^2}{2m_0} 2\sqrt{3}\gamma_3 (k_x - \frac{d}{dy})(-i\frac{d}{dz}) = \frac{\hbar^2}{2m_0} 2\sqrt{3}\gamma_3 (-i\cdot k_x \frac{d}{dz} + i\frac{d}{dy}\frac{d}{dz})$$

$$\therefore L\xi(y,z) = \frac{\hbar^2}{2m_0} 2\sqrt{3}\gamma_3 \left\{ \begin{array}{l} \frac{-i\cdot k_x}{dz_j + dz_{j+1}} \cdot \xi_{y_i, z_{j+1}} - \frac{i\cdot k_x}{dz_j + dz_{j+1}} \cdot \xi_{y_i, z_{j-1}} \\ + \frac{i}{(dy_i + dy_{i+1})(dz_j + dz_{j+1})} (\xi_{y_{i+1}, z_{j+1}} + \xi_{y_{i-1}, z_{j-1}} - \xi_{y_{i-1}, z_{j+1}} - \xi_{y_{i+1}, z_{j-1}}) \end{array} \right\} \quad (3.19)$$

$$M \Rightarrow \frac{\hbar^2}{2m_0}(-\sqrt{3})\left\{ \gamma_2 (k_x^2 + \frac{d^2}{dy^2}) - 2\gamma_3 \cdot k_x \cdot \frac{d}{dy} \right\}$$

$$\therefore M\xi(y,z) = \frac{\hbar^2}{2m_0}(-\sqrt{3}) \left\{ \begin{array}{l} \gamma_2 (k_x^2 - \frac{2}{dy_i + dy_{i+1}}) \cdot \xi_{y_i, z_j} + \left[\frac{2\gamma_2}{dy_{i+1}\cdot(dy_{i+1} + dy_i)} - \frac{2\gamma_3 \cdot k_x}{dy_{i+1} + dy_i} \right] \cdot \xi_{y_{i+1}, z_j} \\ + \left[\frac{2\gamma_2}{dy_i \cdot (dy_{i+1} + dy_i)} + \frac{2\gamma_3 \cdot k_x}{dy_{i+1} + dy_i} \right] \cdot \xi_{y_{i-1}, z_j} \end{array} \right\} \quad (3.20)$$

For <110>-oriented fins:

$$P = \frac{\hbar^2}{2m_0}\gamma_1 (\frac{k'^2_x + k'^2_y - 2k'_x k'_y + k_x^2 + k_y^2 + 2k'_x k'_y}{2} + k'^2_z) = P' \quad (3.21)$$

$$Q = \frac{\hbar^2}{2m_0}\gamma_2 (k'^2_x + k'^2_y - 2k'^2_z) = Q' \quad (3.22)$$

P, Q hence have the same form in the finite difference formula as those for <100>-oriented fins. For L and M:

$$L = \frac{\hbar^2}{2m_0} 2\sqrt{3}\gamma_3 (k_x - ik_y)k_z = \frac{\hbar^2}{2m_0} 2\sqrt{3}\gamma_3 (\frac{k'_x - k'_y}{\sqrt{2}} - i\frac{k'_x + k'_y}{\sqrt{2}})k_z$$

$$\Rightarrow \frac{\hbar^2}{2m_0} 2\sqrt{3}\gamma_3 \left[\frac{1-i}{\sqrt{2}} k'_x - \frac{1+i}{\sqrt{2}}(-i)\frac{d}{dy} \right](-i\frac{d}{dz})$$

$$\therefore L\xi(y,z) = \frac{\hbar^2}{2m_0} 2\sqrt{3}\gamma_3 \left\{ \begin{array}{l} -\frac{1+i}{\sqrt{2}} k'_x \frac{\xi_{y_i, z_{j+1}}}{dz_j + dz_{j+1}} + \frac{1+i}{\sqrt{2}} k'_x \frac{\xi_{y_i, z_{j-1}}}{dz_j + dz_{j+1}} \\ + \frac{1+i}{\sqrt{2}} \frac{i}{(dz_j + dz_{j+1})(dz_j + dz_{j+1})} (\xi_{y_{i+1}, z_{j+1}} + \xi_{y_{i-1}, z_{j-1}} - \xi_{y_{i-1}, z_{j+1}} - \xi_{y_{i+1}, z_{j-1}}) \end{array} \right\} \quad (3.23)$$

$$M = \frac{\hbar^2}{2m_0}\sqrt{3}\left[2\gamma_3 \cdot k'_x \cdot k'_y + i\gamma_2 (k'^2_x - k'^2_y) \right]$$

$$\Rightarrow \frac{\hbar^2}{2m_0}\sqrt{3}\left[-2\gamma_3 i \cdot k'_x \cdot \frac{d}{dy} + i\gamma_2 (k'^2_x + \frac{d^2}{dy^2}) \right]$$

$$\therefore M\xi(y,z) = \frac{\hbar^2}{2m_0}\sqrt{3} \left\{ \begin{array}{l} i\gamma_2 (k'^2_x - \frac{2}{dy_i + dy_{i+1}}) \cdot \xi_{y_i, z_j} + \left[\frac{2i\gamma_2}{dy_{i+1}\cdot(dy_{i+1} + dy_i)} - \frac{2\gamma_3 \cdot k'_x}{dy_{i+1} + dy_i} \right] \cdot \xi_{y_{i+1}, z_j} \\ + \left[\frac{2i\gamma_2}{dy_i \cdot (dy_{i+1} + dy_i)} + \frac{2i\gamma_3 \cdot k'_x}{dy_{i+1} + dy_i} \right] \cdot \xi_{y_{i-1}, z_j} \end{array} \right\} \quad (3.24)$$

The total Hamiltonian for holes can be constructed similarly as has been done for electrons. The 2-D Poisson equation is coupled together with the 2-D Schrödinger equation or k·p Hamiltonian, to solve the eigen-values and eigen-functions for the carrier sub-bands, self-consistently. Fig.3.2 shows the simulated carrier distributions for a Triple-Gate structure, as increasing gate overdrive voltage. The transition from volume inversion to surface inversion is clearly seen.

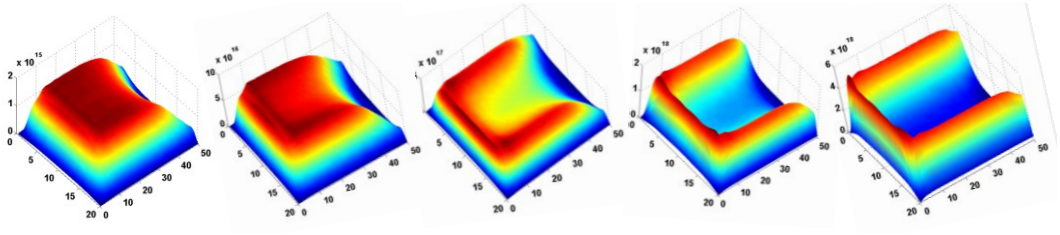

Figure 3.2, 2-D Possion-Schrödinger self-consistent simulation of inversion charge distribution across the Tri-Gate MOSFET fin region, from volume inversion to surface inversion, as increasing gate overdrive voltage.

3.3 Study of Multiple-Gate MOSFET Carrier Mobility and Velocity: Impacts of Fin Aspect Ratio, Orientation and Stress

3.3.1 Experimental and Strained Multiple-Gate FET Design Variations

MuGFETs fabricated on (100) SOI substrates, with either <100> or <110> fin orientation (current flow direction), were studied in this work [10]. The silicon fin width ranges from 20 nm to 35 nm, and the fin height is fixed at 58 nm. The top and sidewall surfaces of the fins each have thin gate oxide (2 nm SiO_2), as shown in Fig.3.3 (left). Measured I_d-V_g characteristics suggest very good electrostatics for those MuGFETs, as shown in Fig.3.3 (right). Field-effect mobility values were extracted using the split-CV method, from long-channel devices. A 4-point bending apparatus was used to induce biaxial tensile stress as described in [11].

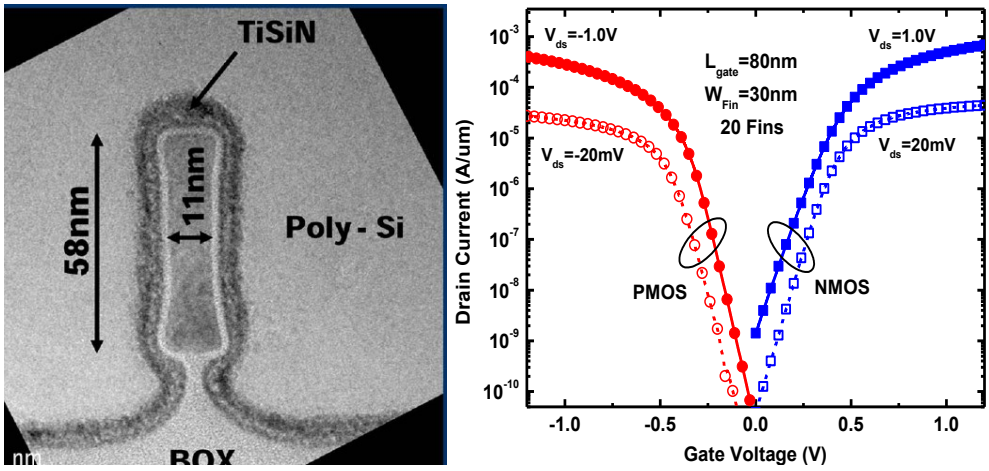

Figure 3.3, (left) TEM cross-section view of Multiple Gate MOSFET studied in this work; (right) measured I_d-V_g.

Two MuGFET designs (FinFET and Tri-Gate FET) are compared via simulations. For adequate suppression of short channel effects (SCE), a default fin aspect ratio (height:width) of 1:3 is assumed for the Tri-Gate FET structure, and a default fin aspect ratio of 3:1 is assumed for the FinFET structure [7]. Three types of stressors are considered herein (Fig. 3.4): local uniaxial stressors (e.g. from Contact Etch Stop Liner, "CESL"; Stress Memorization Technique from Source/Drain, "SMT from S/D"; or SiGe Source/Drain), biaxial-stressed substrate (i.e. strained SOI, "sSOI"), and stressed gate material (e.g. metal gate-induced stress, SMT from poly-Si gate). Three-dimensional TCAD simulations were performed to determine the relative strengths of the different channel stress components for a local uniaxial stressor. It is assumed large stresses exist along the channel (x)-direction and along the height of the fin (z)-direction, of comparable magnitude but opposite sign; thus, the ratio of S_{xx} to S_{zz} is set to be 1:-1, tensile (compressive) for n(p)-channel devices for the band structure and carrier mobility calculations. For biaxial substrate stress, the in-plane stress components (S_{xx} and S_{yy}) are set to be equal in amplitude. For gate-induced stress, large transverse compressive stresses are induced only along each fin surface (y and z directions).

Figure 3.4, Multiple-Gate FET design variations: <100> and <110> fin orientations (left) and under different stress configurations (right).

3.3.2 Multiple-Gate MOSFET Carrier Mobility Dependencies

Kubo-Greenwood formalism is used to calculate carrier mobilities, accounting for phonon, surface roughness scatterings as well as dielectric screening effect [12]. Extracted effective mobility data are plotted in Fig. 3.5, along with simulated effective mobility curves derived using the calibrated parameters. For the FinFET structure, current conduction along the sidewall channel surfaces is dominant. Thus, the effective electron mobility is larger for a <100> oriented fin (which has (100) sidewall surfaces) whereas the effective hole mobility is larger for a <110> oriented fin (which has (110) sidewall surfaces). For the Tri-Gate FET, current conduction along the (100) top channel surface – which has better surface quality [13] – is dominant. This provides for larger effective electron mobility for <100>- and <110>-oriented Tri-Gate FETs vs. FinFETs, as well as larger effective hole mobility for a <100>-oriented fin. As expected, the effective hole mobility for a <110>-oriented fin is larger for a FinFET than for a Tri-Gate FET.

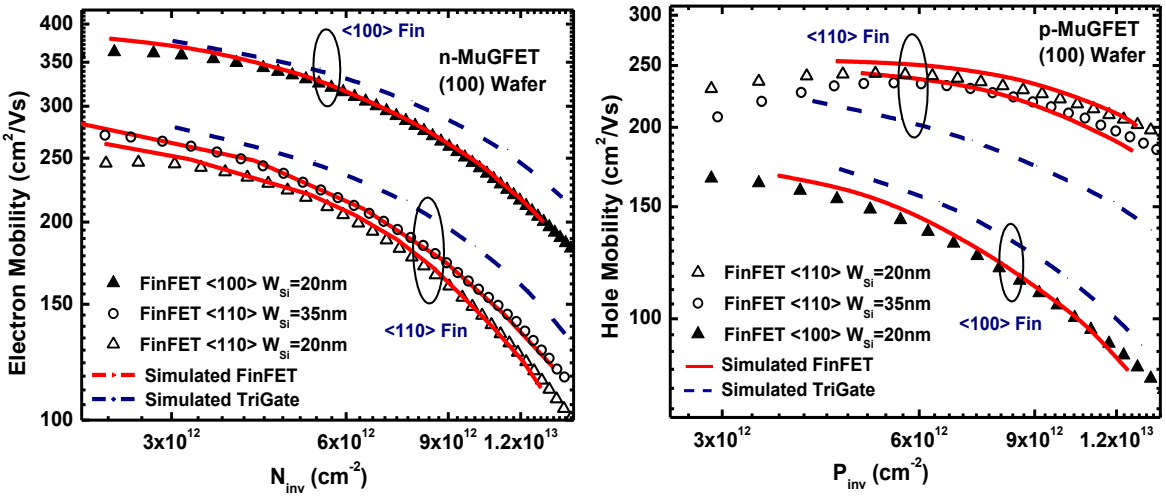

Figure 3.5, Electron (left) and hole (right) mobility data extracted from measurements of FinFETs with L_g = 10 um. Simulated mobility curves are also shown. (For the Tri-Gate FET, H_{Si}=20nm, W_{Si}=58nm.)

Fig. 6 shows that electron and hole mobility enhancements due to biaxial stress are well predicted by simulation. Note that for electrons, <100>-fin mobility enhancement decreases with increasing inversion-charge density due to carrier redistribution among sub-bands. For holes, this degradation in mobility enhancement is less remarkable in <100> fins. For <110> fins, hole mobility enhancement under biaxial stress degrades faster than electron mobility enhancement with increasing inversion-charge density.

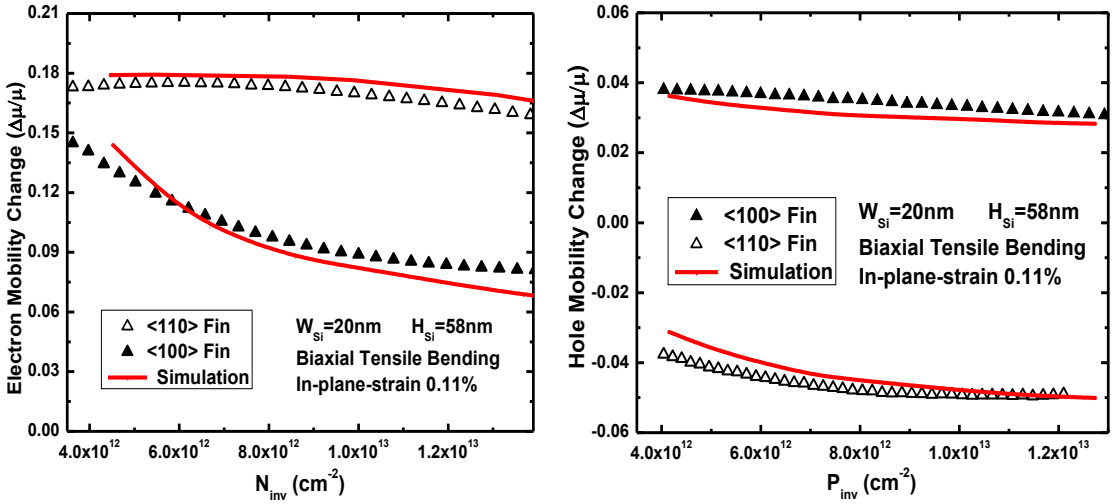

Figure 3.6, Electron (left) and hole (right) mobility enhancement under biaxial wafer bending strain. Data extracted from measurements of FinFETs with L_g = 10 um, with <100> and <110> fins. Simulated mobility curves are also shown.

To provide guidance for channel stress engineering, the impacts of the various stressors are compared via simulation. Fig. 3.7 (left) shows the relative change in n-channel FinFET effective electron mobility (μ_n) with increasing channel stress. μ_n is more sensitive to stress for a <110>-

oriented fin, and uniaxial stresses yields the most enhancement. The calculated electron scattering rates are shown in Fig. 3.7 (right), and can be seen to be negligibly impacted by stress. Thus, the uniaxial stress-induced μ_n enhancement in <110>-oriented fins can be attributed to a reduction in carrier effective mass due to shear stress (S_{xy}). Fig. 3.8 (left) shows that p-channel FinFET effective hole mobility (μ_p) is also more sensitive to stress for a <110>-oriented fin, with uniaxial stresses again yielding the most enhancement due to reductions in both carrier scattering rate and carrier effective mass (Fig. 3.8 (right)).

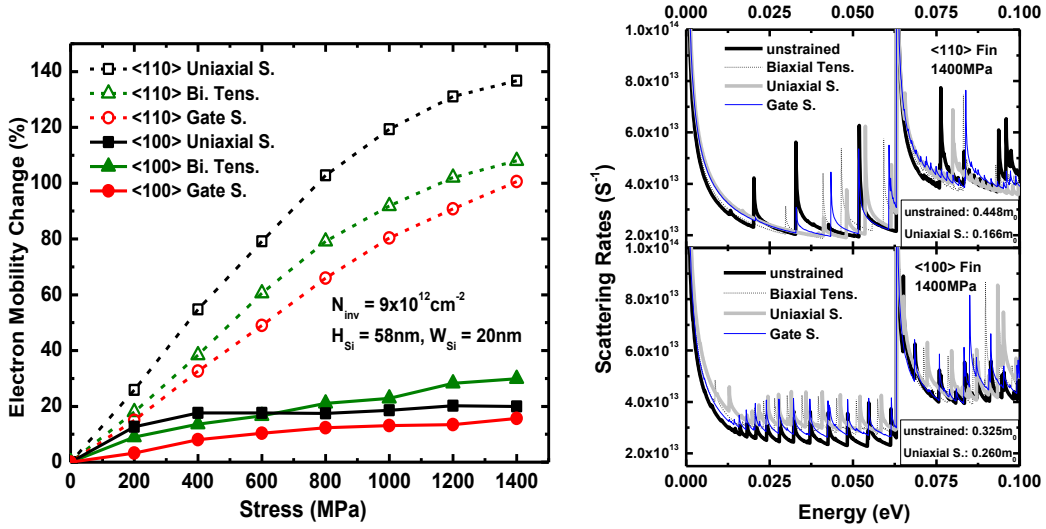

Figure 3.7, (left) Simulated enhancement in FinFET effective electron mobility, for various stressors; (right) simulated electron 1st sub-band scattering rates, and extracted averaged electron mass values (N_{inv}=9×10^{12}cm^{-2}).

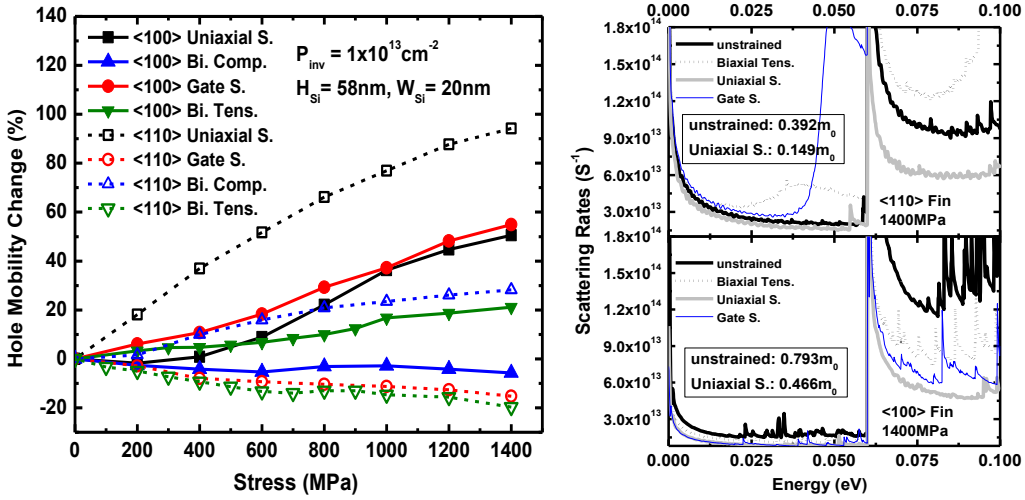

Figure 3.8, (left) Simulated enhancement in FinFET effective electron mobility, for various stressors; (right) simulated electron 1st sub-band scattering rates, and extracted averaged electron mass values (N_{inv}=9×10^{12}cm^{-2}).

Figs. 3.9 compares the effective electron and hole mobilities for FinFET *vs*. Tri-Gate FET structures. At low stress levels, μ_n is consistently higher for the Tri-Gate FET, due to the higher-

mobility (100) top channel surface. At high stress levels (above ~600 MPa), μ_n becomes comparable for a <110>-oriented FinFET *vs.* a <100>-oriented Tri-Gate FET. For <110>-oriented p-channel devices, the highest μ_p is achieved with uniaxial stresses. And at high stress levels, μ_p is highest for the FinFET.

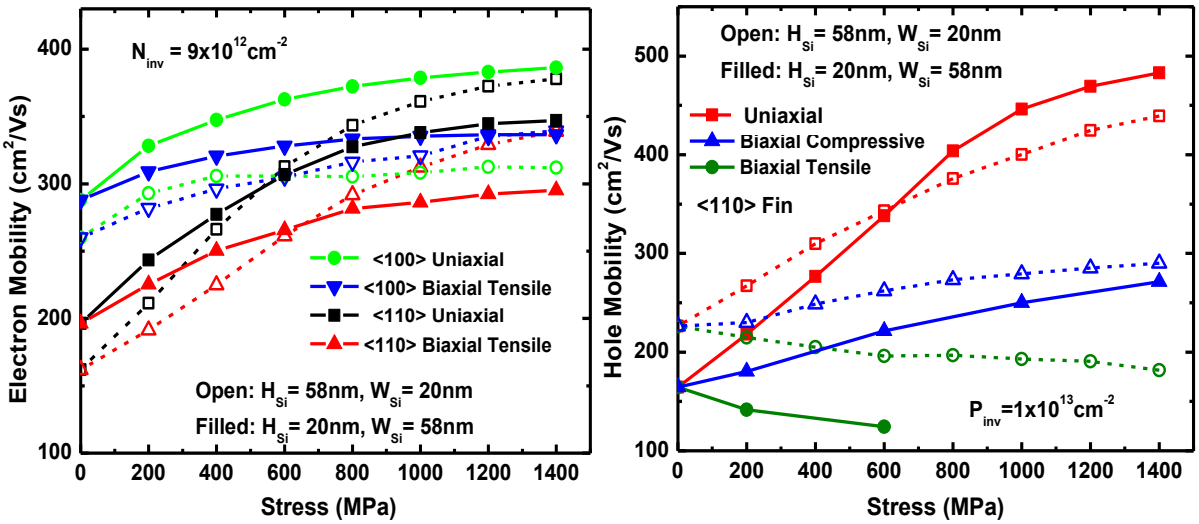

Figure 3.9, Simulated electron (left) and hole (right) mobility enhancement *vs.* stress for FinFET (H_{Si}=58nm, W_{Si}=20nm) and Tri-Gate FET (H_{Si}=20nm, W_{Si}=58nm).

3.3.3 Multiple-Gate MOSFET Carrier Velocity Dependencies

As discussed in Chapter 2, ON-state transistor current of short-channel MOSFET is limited more by the injection velocity (v_{inj}) at the source-end of the channel rather than in the high-field region at the drain end [14], so it is important to examine the stress impacts on FinFET's carrier velocities. Simulated carrier thermal velocities from unstrained and uniaxial stressed FinFETs are shown in Fig. 3.10 as a function of inversion-charge density. It can be seen that uniaxial stresses can provide for large enhancements in carrier velocity.

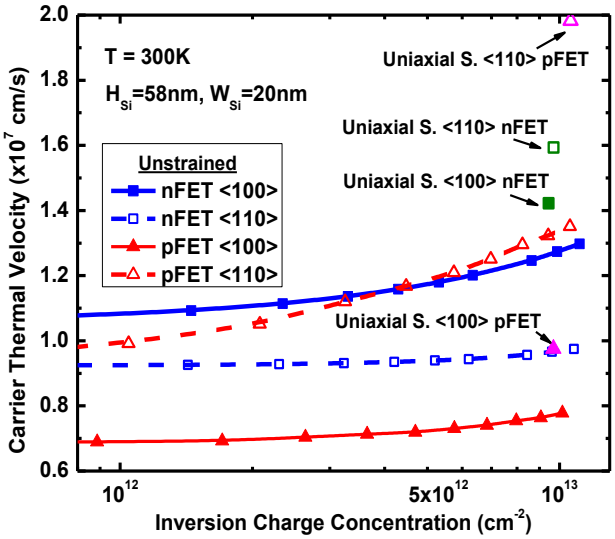

Figure 3.10. Simulated carrier thermal (ballistic-limit) velocities vs. inversion-charge concentration, for n/p-FinFETs. The points for uniaxial stressed devices are under +/-1400MPa CESL-induced channel stress.

3.4 Effectiveness of Uniaxial Stressors in Aggressively Scaled FinFET

3.4.1 Process-induced Stress Simulation Methodology

Previous studies assumed ideal uniaxial stresses [10, 13] and did not fully comprehend the impact of technology choices (*e.g.* starting substrate material, gate stack formation process) and continued transistor scaling [15]. This section presents a comprehensive simulation-based study of stress in FinFET structures induced by a strained contact etch-stop layer (CESL) or strained Source/Drain (S/D) stressors, that compares results for bulk-silicon *vs.* silicon-on-insulator (SOI) substrates and Gate-First *vs*. Gate-Last process integration schemes. The impact of the stressors on effective carrier mobility is presented to evaluate their efficacy for boosting FinFET performance, down to sub-10 nm L_g.

The process simulator within the Sentaurus technology computer aided design software suite [16], which uses the finite-element method, was used to perform 3D simulations of stress within FinFETs with (100) top and (110) sidewall surfaces and <110> channel direction. Temperature-dependent strain relaxation time and anisotropy of mechanical properties are taken into account. Fig. 11 shows a schematic plan view of nested FinFET devices, and indicates the region simulated in this work.

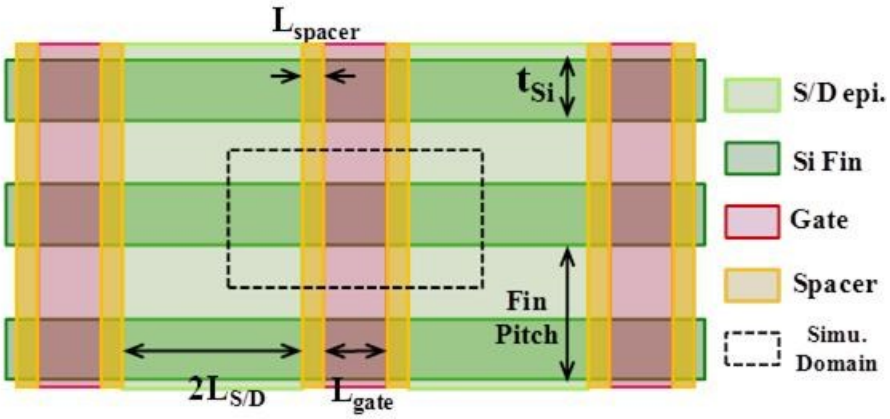

Figure 3.11. Schematic plan view of FinFETs and region simulated in this work.

Two kinds of stressors are considered herein (+1 GPa initial stress): a strained CESL, and strained S/D regions (carbon-doped silicon, Si:C, for n-channel devices and silicon-germanium alloy, $Si_{1-x}Ge_x$, for p-channel devices). The CESL is formed by depositing an amorphous silicon-nitride layer at ambient temperature, after gate stack and S/D formation [17]. Selective Si:C or $Si_{1-x}Ge_x$ epitaxial growth with the temperature of 800K is used to form the strained S/D regions for n-channel or p-channel FinFETs, respectively, to induce longitudinal stress and boost effective mobility [18-20]. For SOI FinFETs, the fin S/D regions are not etched away prior to the selective epitaxy, *i.e.* the strained-S/D regions wrap around the fin S/D regions so that only a portion of the S/D regions are strained, as shown in Fig. 12(a). For bulk FinFETs, the fin S/D regions are etched away prior to the selective epitaxy, since the bulk-silicon substrate provides a template for epitaxial growth, so that the entire S/D regions are strained, as shown in Fig. 3.12(b).

Two gate-stack formation processes are considered herein: a Gate-First (*i.e.* metal-inserted polycrystalline-silicon, or MIPS) process flow, in which the S/D epitaxy is performed after metal/poly-Si gate formation [21], as shown in Fig. 3.12 (a, b, d); and a Gate-Last (*i.e.* replacement metal gate, or RMG) process flow, in which a dummy gate is formed prior to the S/D epitaxy and then replaced by the metal gate [22], as shown in Fig. 3.12 (c). Since the Gate-Last process requires the use of chemical-mechanical polishing (CMP) which imposes some material constraints, the integration of CESL with a Gate-Last process flow is unlikely for FinFETs [22]. Table 3.2 lists the default FinFET geometrical design parameters used in this work, based on recently reported 25nm-L_g FinFET technologies [5, 6].

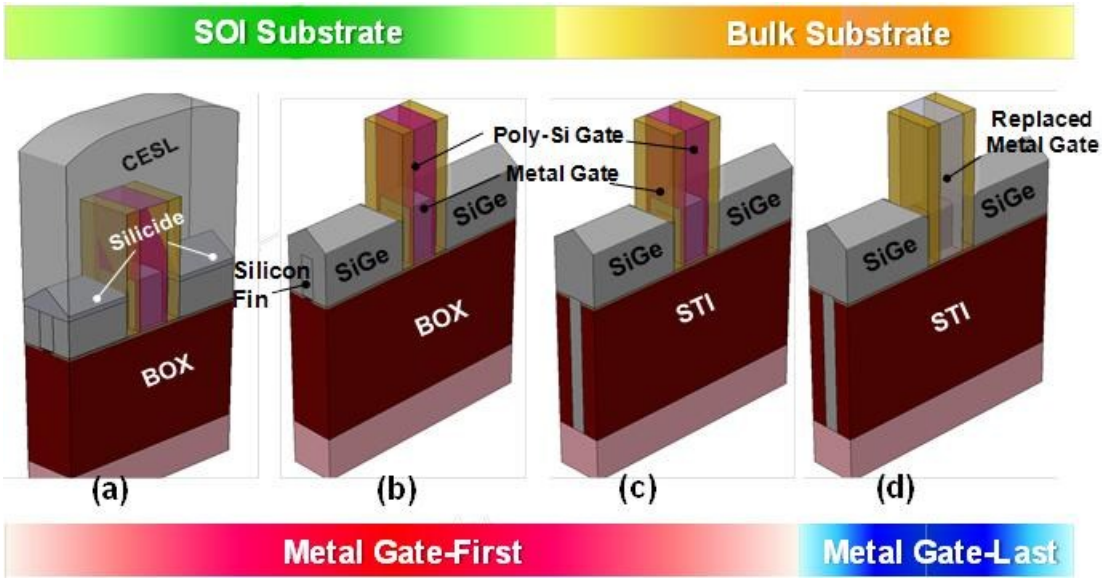

Figure 3.12. FinFET device structures studied in this work: (a) SOI FinFET with partially strained S/D, fabricated using a Gate-First process flow; (b) Bulk FinFET with fully strained S/D, fabricated using a Gate-First process flow; (c) Bulk FinFET with fully strained S/D, fabricated using a Gate-Last process flow; (d) FinFET with unstrained S/D and strained CESL, fabricated using a Gate-First process flow. SOI FinFET with partially strained S/D, fabricated using a Gate-Last flow is also studied, but the device structure is not shown here.

Fin width (t_{Si})	12	BOX or STI thickness (T_{BOX})	80
Fin height (H_{Fin})	30	CESL thickness$^{\wedge}$ (T_{CESL})	40
Gate length (L_{gate})	25	Metal gate thickness* (t_{Metal})	5
Fin pitch	36	Gate height (H_{gate})	40
Gate oxide thickness^{+} (t_{OX})	2	Source/Drain Elevation ($H_{S/D}$)	18
Spacer length (L_{spacer})	10	Silicide thickness ($T_{silicide}$)	17

units: nm
$^{+}$: high-κ dielectric material is used
$^{\wedge}$: used in CESL-strained FinFETs
*: used in Gate-First-processed FinFETs

Table 3.2: Default FinFET geometrical design parameters used in this work.

Each epitaxially grown S/D region is assumed to have no crystalline defects or distorted atomic bonds, so that the built-in stress is modeled as a single rebalancing force. In contrast, stress from the CESL must be rebalanced in several sub-steps [23] because the atomic bonds within the nitride adjust upon deposition of each atom within a very short time period (on the order of fs), and the distorted bonds are retained throughout the remainder of the CESL deposition process. Fig. 3.13 (left) shows how the CESL-induced stress profiles in the fin along

the channel changes with the number of deposition sub-steps. The 1-D stress profiles are extracted at 1 nm beneath the fin sidewall surfaces (corresponding to inversion layer position [24]), and averaged across the fin width. Fig. 3.13 (right) shows that the longitudinal stress (S_{xx}) and vertical stress (S_{zz}) profiles do not change significantly when the number of deposition sub-steps exceeds 15. Therefore, the CESL layer is deposited in 15 sub-steps for the remainder of this work. For both CESL and S/D stressors, the initial stress values are isotropic. After relaxation, the transverse stress (S_{yy}) is always negligible compared to S_{xx} and S_{zz} for the nested FinFET structure, so it is not considered further herein.

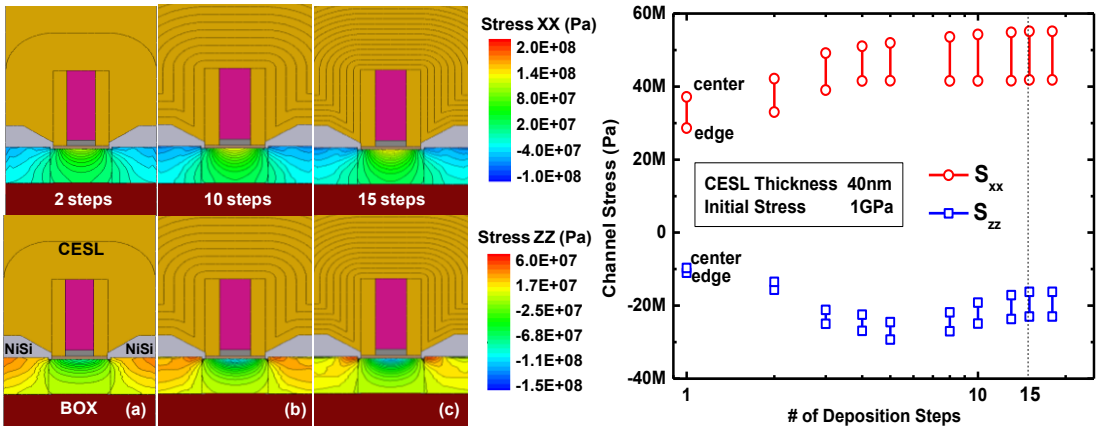

Figure 3.13. Contour plots of CESL-induced stress in the channel direction (S_{xx}) and in the vertical direction (S_{zz}), along the channel of a FinFET, showing the impact of the number of sub-steps used to deposit the CESL: (a) 2 sub-steps, (b) 10 sub-steps, and (c) 15 sub-steps.

Fig. 3.14 shows the S_{xx} and S_{zz} profiles within the fin along the channel in an n-channel SOI FinFET, for S/D length ($L_{S/D}$) ranging from 15nm to 40nm (corresponding to gate pitch ranging from 75nm to 125nm, consistent with dimensions reported in [5, 6]). It can be seen that the stress profiles are highly non-uniform along the channel direction. From Fig. 3.14(a), S/D-induced S_{xx} is most tensile at the center of the channel region and changes to be compressive in the S/D regions. From Fig. 3.14(b), CESL-induced S_{xx} and S_{zz} each reach their peak values at the center of the channel, which is different than for a planar bulk MOSFET structure [19, 25] due to the elevated S/D structure: the CESL is thicker between the faceted S/D surfaces and the gate-sidewall spacers and hence induce more stress. CESL is not as effective as S/D stressors for FinFET structures because of the larger distance between the CESL and the channel region (due to the silicide and elevated S/D regions).

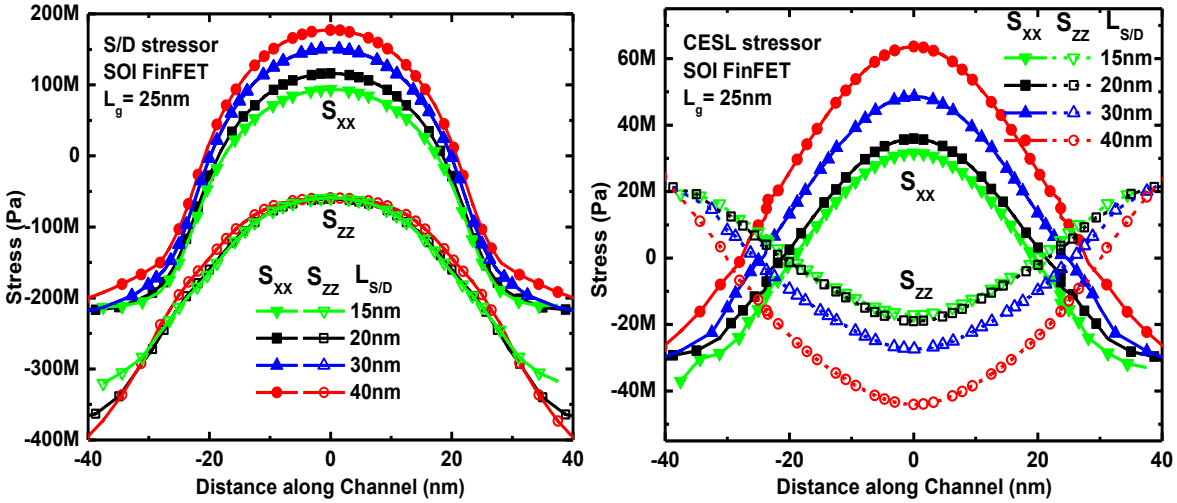

Figure 3.14. Simulated S_{zz} and S_{xx} profiles in a 25nm-L_g SOI FinFET with (a) S/D stressors or (b) CESL stressors, for various values of S/D length ($L_{S/D}$). The initial stress value was +1GPa in the stressors.

To examine the effectiveness of stressors at more aggressively scaled CMOS technology nodes, FinFET structures are simulated with L_g down to 17nm and 12nm. Other geometrical design parameters that are scaled with L_g according to ITRS specifications [26] are listed in Table III. (Parameters that are not changed from Table 3.2 are not listed again in Table 4.3.) The $L_{S/D}$ values studied are 15nm and 20nm (corresponding to gate pitches of 64nm and 74nm for 17nm-L_g FinFETs, and gate pitches of 54nm and 64nm for 12nm-L_g FinFETs).

L_{gate} (nm)	t_{Si} (nm)	$H_{S/D}$ (nm)	L_{spacer} (nm)	H_{Fin} (nm)	Fin Pitch (nm)
17	8	15	8.4	24	24
12	6	10.5	5.8	18	20

Table 3.3. FinFET geometrical design parameters for sub-20nm CMOS technology nodes, from ITRS specifications [26].

Fig. 3.15 shows the S_{xx} and S_{zz} profiles within the fin along the channel in 17nm-L_g and 12nm-L_g n-channel SOI FinFETs. It can be seen that both S_{xx} and S_{zz} are enhanced with scaling. For S/D stressors, this indicates that the effect of decreased volume for stress relaxation overwhelms the effect of decreased stressor volume.

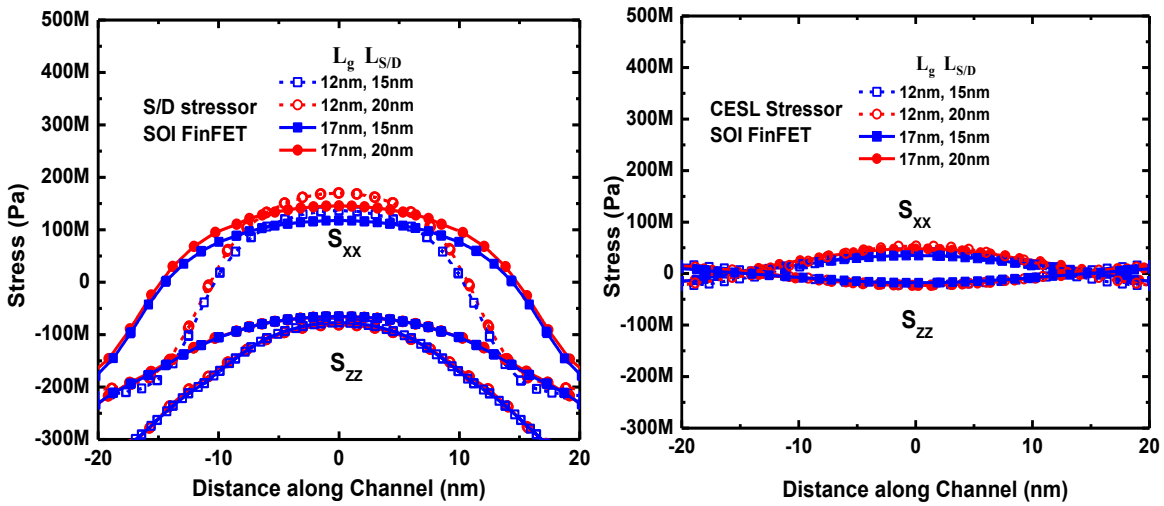

Figure 3.15. Simulated S_{xx} and S_{zz} profiles in 17nm-L_g and 12nm-L_g SOI FinFETs with S/D stressors (left) or CESL stressor (right), for 15nm or 20nm $L_{S/D}$. The initial stress value was +1GPa in the stressors.

The impact of S/D stressors on bulk FinFETs is shown in Fig. 3.16. Since the entire S/D regions are strained, greater stress is induced in the channel region of a bulk FinFET as compared to an SOI FinFET. Also, the S_{xx} profile is more similar to that for a planar bulk MOSFET [19, 25], in that it has maximum values at the edges of the channel and decays towards the center of the channel.

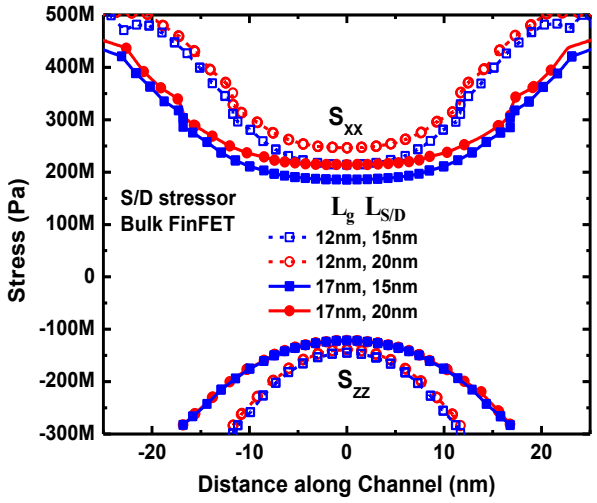

Figure 3.16. Simulated S_{zz} and S_{xx} profiles in 17nm-L_g and 12nm-L_g bulk FinFETs with S/D stressors, for 15nm or 20nm $L_{S/D}$. The initial stress value was +1GPa in the stressors.

The evolution of S_{xx} during a Gate-Last FinFET fabrication process is presented in Fig. 3.17, which indicates that 1) S_{xx} is enhanced and becomes more non-uniform along the fin upon removal of the dummy gate; and 2) the metal gate refill process does not significantly change S_{xx}. The enhancement of S_{xx} is caused by the change in stress relaxation boundary conditions between the S/D regions and the gate electrode region. Without the gate stack in place, S_{xx} is

more effectively transferred from the S/D regions into the channel region; however, S_{zz} is largely reduced due to the free surface condition at the top of the fin, as shown in Fig. 3.18.

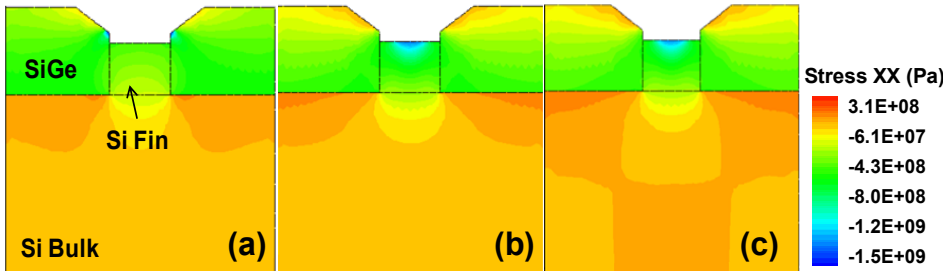

Figure 3.17. Contour plots of S/D-induced stress in the channel direction (S_{xx}), along the channel of a FinFET fabricated using a Gate-Last process on bulk substrate: (a) after epitaxial S/D growth; (b) after removal of the dummy poly-Si gate, and (c) after metal gate refill.

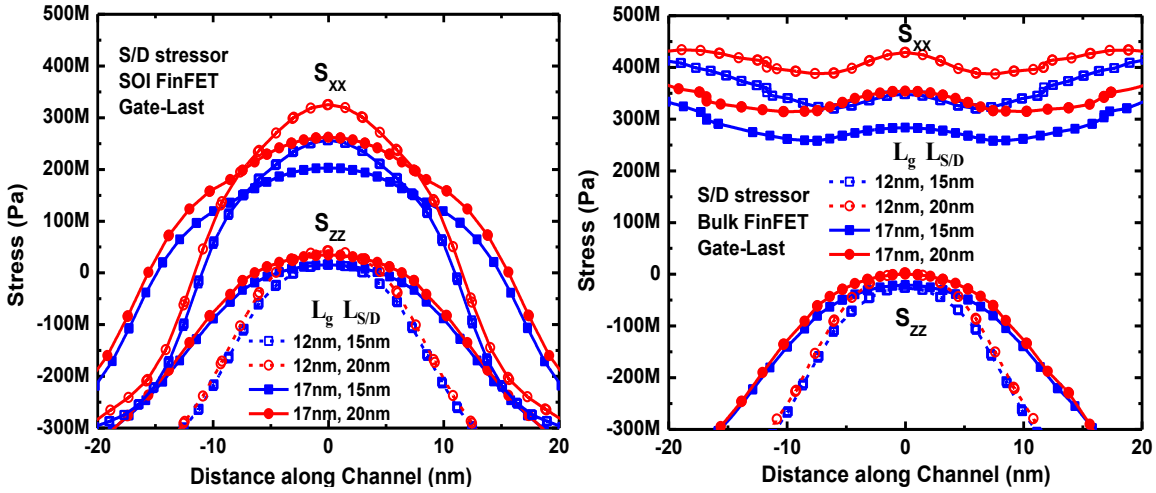

Figure 3.18. Simulated S_{zz} and S_{xx} profiles in 17nm-L_g and 12nm-L_g (a) SOI FinFETs and (b) bulk FinFETs with S/D stressors, fabricated using a Gate-Last process flow, for 15nm or 20nm $L_{S/D}$. The initial stress value was +1GPa in the stressors.

The Stress Transfer Efficiency (STE) is defined herein to be the ratio between the value of final induced stress in the channel region and the initial value of (isotropic) stress in the stressor. Table 3.4 lists the S_{xx} and S_{zz} transfer efficiency values for 12nm-L_g and 17nm-L_g FinFETs at the center of the channel, at the edges of the channel, and averaged across the length of the channel. As noted above, the STE for a CESL stressor is small compared to that for S/D stressors. S/D stressors have >50% greater STE for the bulk FinFET than for the SOI FinFET. A Gate-Last process can provide for >50% larger S_{xx}TE, at the cost of dramatically reducing S_{zz}TE.

17nm / 12nm S_{xx}/S_{zz}	Gate First			Gate Last	
	CESL	SOI S/D	Bulk S/D	SOI S/D	Bulk S/D
Edge (%)	3.0/-1.2	11.1/-9.4	23.0/-16.1	18.3/-4.0	31.5/-9.0
	4.1/-1.6	13.3/-10.7	26.2/-17.5	23.9/-3.6	38.9/-8.7
Center (%)	4.8/-2.3	14.5/-6.6	21.4/-12.2	26.2/-0.0	35.4/-0.0
	5.4/-2.2	17.0/-7.7	24.6/-13.9	32.3/-0.2	42.9/-0.2
Average (%)	4.1/-1.9	13.2/-7.3	21.4/-13.2	23.3/-1.8	33.1/-2.6
	4.9/-2.0	15.5/-8.5	24.7/-14.8	29.4/-1.3	40.4/-2.6

Table 3.4. Summary of Stress Transfer Efficiency (STE) values for different stressor technologies, for 12nm and 17nm-L_g FinFETs fabricated using Gate-First or Gate-Last process flows.

3.4.2 Soucr/Drain Stress-induced FinFET Carrier Mobility Enhancement

The self-consistent Poisson-Schrödinger equation solver is used to calculate the silicon sub-band structure and effective carrier mobility values for FinFET structures with strain, using average values of S_{xx} and S_{zz} within the channel region. Only conduction along the fin sidewall surfaces is considered, to be relevant for aggressively scaled FinFETs [27]. The initial stress is calculated using the following equation:

$$S_{ii} = \frac{E}{1-2\cdot\nu} \cdot \frac{a_{Si}-a_D}{a_{Si}} \cdot D\% \tag{3.25}$$

where i=x, y, or z; E and υ are the silicon elastic modulus and Poisson ratio for the [110] crystalline direction, respectively; a_{Si} and a_D are the lattice constants for unstrained silicon and impurity materials (*i.e.* Ge or C), respectively; and D% is the atomic percentage of the impurity in the strained S/D region.

Relative enhancement in electron mobility ($\Delta\mu_e/\mu_e$) is plotted in Fig. 3.19(a) as a function of C mole fraction [20, 26] in the S/D regions, for various FinFET structures at low and high values of inversion-layer electron concentration (N_{inv}). $\Delta\mu_e/\mu_e$ is remarkably higher for bulk FinFETs than for SOI FinFETs. Improvement with a Gate-Last process is negligible for 17nm L_g and is marginal for 12nm L_g. This is because S/D-induced S_{zz} is more effective than S_{xx} [10, 13, 28] for boosting $\Delta\mu_e/\mu_e$, and S_{zz} is largely reduced for a Gate-Last process. Relative enhancement in hole mobility ($\Delta\mu_h/\mu_h$) is plotted in Fig. 3.19(b) as a function of Ge mole fraction [18, 19, 22] in the S/D regions, for various FinFET structures at low and high values of inversion-layer hole concentration (P_{inv}). The benefit of using a bulk substrate is greater than that of using a Gate-Last process. Note that $\Delta\mu_h/\mu_h$ degrades significantly at high P_{inv}; this is due to the hole sub-band reoccupation effect for (110)-oriented fin sidewall surfaces [29].

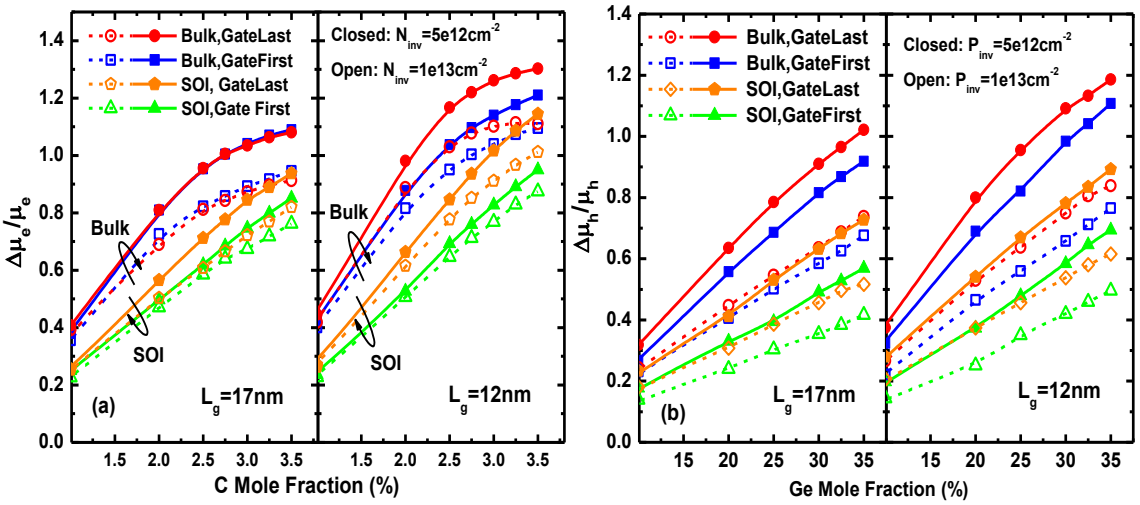

Figure 3.19. (a) Relative enhancement in electron mobility *vs*. C mole fraction in the S/D regions, and (b) relative enhancement in hole mobility *vs*. Ge mole fraction in the S/D regions, for various FinFET structures with $L_{S/D}$=20nm.

3.5 Summary

For Multiple-Gate MOSFET, fin crystalline orientation and aspect ratio have significant impacts on effective carrier mobilities. <110>-oriented fins (with (110) sidewall surfaces) are more sensitive to strain than <100>-oriented fins (with (100) sidewall surfaces). Uniaxial stressor technology can provide the highest carrier mobility enhancement at a given stress value. For <110> channels, electron mobility is higher for the Tri-Gate MOSFET than that for FinFET for unstrained or low-strain channels; at higher strain, the two device architectures are comparable in electron mobility values. Hole mobility is lower in the FinFET than in the Tri-Gate MOSFET until the stress applied reaches ~600MPa.

Among the uniaxial stressor technologies, strained CESL is not as effective as S/D stressors for inducing stress within the channel region of a FinFET. Bulk FinFETs with strained-S/D regions are projected to outperform SOI FinFETs with strained-S/D regions. For FinFET structures with S/D stressors, although a Gate-Last process can further increase longitudinal stress (S_{xx}), its benefit for boosting carrier mobility will be marginal in future technology nodes, due to the largely reduced vertical stress (S_{zz}).

3.6 References

[1] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, C. Hu, "Sub 50-nm FinFET: PMOS," IEDM Tech. Dig., 1999, pp. 67-70.

[2] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, C. Hu, "FinFET – A Self-aligned Double-Gate MOSFET Scalable to 20 nm," Electron devices, IEEE Transactions on, vol.47, no.12, 2000, pp.2320-2325.

[3] B.S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, A. Murthy, R. Rios, R. Chau, "High Performance Fully-Depleted Tri-Gate CMOS Transistors," IEEE Electron Device Letters, Vol. 24, no. 4, 2003, pp. 263-265.
[4] B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, R. Rios, R. Chau, "Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout," Symp. on VLSI Tech. Dig., 2003, pp.133-134.
[5] K. Maitra, A. Khakifirooz, P. Kulkarni, V. S. Basker, J. Faltermeier, H. Jagannathan, H. Adhikari, C.-C. Yeh, N. R. Klymko, K. Saenger, T. Standaert, R. J. Miller, B. Doris, V. K. Paruchuri, D. McHerron, J. O'Neil, E. Leobundung, H. Bu, Aggressively Scaled Strained-Silicon-on-Insulator Undoped-Body High-k/Metal-Gate nFinFETs for High-Performance Logic Applications," IEEE Electron Device Letters, Vol. 32, no. 6, 2011, pp. 713-715.
[6] V. S. Basker, T. Standaert, H. Kawasaki, C.-C. Yeh, K. Maitra, T. Yamashita, J. Faltermeier, H. Adhikari. H. Jagannathan, J. Wang, H. Sunamura, S. Kanakasabapathy, S. Schmitz, J. Cummings, A. Inada, C. -H. Lin, P. Kulkarni, Y. Zhua, J. Kuss, T. Yamamoto, A. Kumara, J. Wahl, A. Yagishita, L. F. Edge, R. H. Kim, E. Mclellan, S. J. Holmes, R. C. Johnson, T. Levin, J. Demarest, M. Hane, M. Takayanagi, M. Colburn, V. K. Paruchuri, R. J. Miller, H. Bu, B. Doris, D. McHerron, E. Leobandung and J. O'Neill, "A 0.063 μm^2 FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch," Symp. on VLSI Tech. Dig., 2010, pp.19-20.
[7] J.G. Fossum, L.Q. Wang, J.W. Yang, S.H. Kim, V.P. Trivedi, "Pragmatic Design of Nanoscale Multi-gate CMOS," IEDM Tech. Dig., 2004, pp. 613-616.
[8] J.B. Chang, M. Guillorn, P.M. Solomon, C.-H. Lin, S.U. Engelmann, A. Pyzyna, J.A. Ott, W.E. Haensch, "Scaling of SOI FinFETs down to Fin Width of 4nm for the 10nm technology node," Symp. on VLSI Tech. Dig., 2011, pp.12-13.
[9] S. E. Thompson, G. Sun, Y.S. Choi, T. Nishida, "Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap," Electron Devices, IEEE Transaction on, Vol. 53, no.5, 2006, pp. 1010-1020.
[10] K. Shin, W. Xiong, C.-Y. Cho, C. R. Cleavelin, T. Schulz, K. Schruefer, P. Patruno, L. Smith, T.-J. King Liu, "Study of Bending-Induced Strain Effects on MuGFET Performance," IEEE Electron Device Letters, Vol. 27, no. 8, 2006, pp.671-673.
[11] K. Uchida, T. Krishnamohan, K.C. Saraswat, Y. Nishi, "Physical Mechanism of Electron Mobility Enhancement in Uniaxial Stressed MOSFETs and Impact of Uniaxial Stress Engineering in Ballistic Regime," IEDM Tech. Dig. 2005, pp.49-52.
[12] N. Xu, X. Sun, W. Xiong, C. R. Cleavelin, T.-J. King Liu, "MuGFET Carrier Mobility and Velocity: Impacts of Fin Aspect Ratio, Orientation and Stress," IEDM Tech. Dig. , 2010, pp. 194-197.
[13] M. Saitoh, A. Kaneko, K. Okano, T. Kinoshita, S. Inaba, Y. Toyoshima, K. Uchida, "Three-Dimensional Stress Engineering in FinFETs for Mobility/On-Current Enhancement and Gate Current Reduction," Symp. on VLSI Tech. Dig., 2008, pp.1-4.
[14] M.S. Lundstrom, "On the Mobility Versus Drain Current Relation for a Nanoscale MOSFET," IEEE Electron Device Letters, Vol.22, no.6, 2001, pp.293-295.
[15] K. Shin, C.O. Chui, T.-J. King, "Dual Stress Capping Layer Enhancement Study for Hybrid Orientation FinFET CMOS Technology," IEDM Tech. Dig. , 2005, pp. 988-991.
[16] Sentaurus Process User Guide, Version D-2011.09, Synopsys Co., Mountain View, CA, 2011.

[17] G. Eneman, M. Jurczak, P. Verheyen, T. Hoffmann, A. De Keersgieter, K. De Meyer, "Scalability of Strained Nitride Capping Layers for Future CMOS Generations," The Proceedings of European Solid-State Device Research Conference (ESSDERC), Tech. Dig., 2005, pp.449-452.
[18] J.G. Fiorenza, J.-S. Park, A. Lochtefeld, "Detailed Simulation Study of a Reverse Embedded-SiGe Strained-Silicon MOSFET," Electron Devices, IEEE Transaction on, Vol. 55, no.2, 2008, pp. 640-647.
[19] G. Eneman, P. Verheyen, R. Rooyackers, F. Nouri, L. Washington, R. Degraeve, B. Kaczer, V. Moroz, A. De Keersgieter, R. Schreutelkamp, M. Kawaguchi, Y. Kim, A. Samoilov, L. Smith, P. P. Absil, K. De Meyer1, M. Jurczak, S. Biesemans, "Layout Impact on the Performance of a Locally Strained PMOSFET," Symp. on VLSI Tech., 2005, pp.22-23.
[20] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi, L. F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet, S. Holmes, S. Mehta, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, B. S. Haran, Z. Zhu, L. H. Vanamurth, S. Fan, D. Horak, H. Bu, P. J. Oldiges, D. K. Sadana, P. Kozlowski, D. McHerron, J. O'Neill, B. Doris "Extremely Thin SOI (ETSOI) CMOS with Record Low Variability for Low Power System-on-Chip Applications," IEDM Tech. Dig. 2009, pp.49-52.
[21] F. Arnaud, J.Liu, Y.M.Lee, K.Y.Lim, S.Kohler, J.Chen, B.K.Moon, C.W. Lai, M.Lipinski, L.Sang, F.Guarin, C. Hobbs, P.Ferreira, K.Ohuchi, J.Li, H.Zhuang, P.Mora, Q. Zhang, D.R.Nair, D.H. Lee, K.K.Chan, S.Satadru, S.Yang, J.Koshy, W.Hayter, M.Zaleski, D.V.Coolbaugh, H.W.Kim, Y.C. Ee, J.Sudijono, A.Thean, M.Sherony, S.Samavedam, M.Khare, C.Goldberg, A.Steegen, "32nm General Purpose Bulk CMOS Technology for High Performance Applications at Low Voltage," IEDM Tech. Dig., 2008, pp. 633-636.
[22] C. Auth, A. Cappellani, J.-S. Chun, A. Dalis, A. Davis, T. Ghani, G. Glass, T. Glassman, M. Harper, M. Hattendorf, P. Hentges, S. Jaloviar, S. Joshi, J. Klaus, K. Kuhn, D. Lavric, M. Lu, H. Mariappan, K. Mistry, B. Norris, N. Rahhal-orabi, P. Ranade, J. Sandford, L. Shifren, V. Souw, K. Tone, F. Tambwe, A. Thompson, D. Towner, T. Troeger, P. Vandervoorn, C. Wallace, J. Wiedemer, C. Wiegand "45nm High-κ+Metal Gate Strain-Enhanced Transistors," Symp. on VLSI Tech., 2008, pp.128-129.
[23] K.V. Loiko, V. Adams, D. Tekleab, B. Winstead, X.-Z. Bo, P. Grudowski, S. Goktepeli, S. Filipiak, B. Goolsby, V. Kolagunta, M.C. Foisy, "Multi-Layer Model for Stressor Film Deposition," International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Tech. Proc. 2006, pp.123-126.
[24] L. Donetti, F. Gámiz, N. Rodriguez, F. Jiménez-Molinos, J.B. Roldán, "Hole Transport in DGSOI Devices: Orientation and Silicon Thickness Effects," Solid-State Electronics, vol.54, 2010, pp.191-195.
[25] N. Xu, L. Wang, A. Neureuther, T.-J. King Liu, "Physically Based Modeling of Stress-Induced Variation in Nano-scale Transistor Performance," Device and Material Reliability, IEEE Transactions on, 11, 2011, pp. 378-386.
[26] International Technology Roadmap for Semiconductors, 2009 Edition.
[27] M. van Dal, N. Collaert, G. Doornbos, G. Vellianitis, G. Curatola, B. Pawlak, R. Duffy, C. Jonville, B. Degroote, E. Altamirano, E. Kunnen, M. Demand, S. Beckx, T. Vandeweyer, C. Delvaux, F. Leys, A. Hikavyy, R. Rooyackers, M. Kaiser, R. Weemaes, S. Biesemans, M. Jurczak, K. Anil, L. Witters, R. Lander, "Highly manufacturable FinFETs with sub-10 nm fin

width and high aspect ratio fabricated with immersion lithography," Symp. on VLSI Tech. Dig., 2007, pp. 110–111.
[28] N. Serra, D. Esseni, "Mobility Enhancement in Strained n-FinFETs: Basic Insight and Stress Engineering," Electron devices, IEEE Transactions on, vol.57, no.2, 2010, pp.482-490.
[29] K. Shimizu, T. Saraya, T. Hiramoto, "Physical Understandings of Si (110) Hole Mobility in Ultra-Thin Body pFETs by <110> and <111> Uniaxial Compressive Strain," IEDM Tech. Dig. 2009, pp.474-477.

Chapter 4

Thin-Body MOSFET Carrier Mobility and the Impact of High-κ/Metal Gate Stack

4.1 Introduction

Thin-body MOSFET structures (including planar ultra-thin body and BOX (UTBB) fully depleted silicon-on-insulator (FD-SOI) MOSFET and the FinFET) are slated for adoption in sub-20nm CMOS technology nodes due to their superior electrostatic integrity as compared to the conventional planar bulk MOSFET [1, 2]. Previous studies have shown how channel stress can boost thin-body MOSFET performance, but these only focused on devices with poly-Si/SiO_2 [3, 4] or poly-Si/SiO_xN_y gate stacks [5], for which remote Coulomb scattering and surface optical phonon scattering is not significant. Since high-κ/metal gate stacks already have been adopted in the most advanced CMOS technologies [6], it is important to examine the impact of channel stress on thin-body MOSFETs with high-κ gate stacks, considering all of the aforementioned scattering mechanisms. Also, a comparison of carrier transport and strain-induced performance enhancement in UTBB FD-SOI MOSFETs vs. FinFETs is needed to guide CMOS technology development for future high-performance (HP) applications.

In this chapter, stress-induced enhancements in electron and hole mobilities are studied comprehensively for UTBB FD-SOI MOSFET and FinFET structures with high-κ/metal gate stacks. Simulation data calibrated to measurement are presented to evaluate the effectiveness of strain for boosting thin-body MOSFET performance with aggressively scaled body thickness.

4.2 Modeling for High-κ/Metal Gate Stack-induced Scattering Mechanisms in Thin-Body MOSFETs

4.2.1 Remote Coulomb scattering

Coulomb scattering, also referred as "Rutherford scattering", describes the carrier's change of momentum under the perturbation (scattering) potentials induced by some external charges (ionized impurities, trapped charges, etc.). For a poly-Si/SiO_2 gate stack, the most important

Coulomb scattering sources are depletion charges from the poly-Si gate and heavily-doped channel region [7], which can be overcome by using a metal gate and undoped channel region in thin-body MOSFETs. However, during the high-κ layer deposition and later-on high temperature annealing process, additional interface charges will be generated, with the profile peak located between the high-κ and SiO_2 interfacial layer (IL) [8]. In contrast to the depletion charge located close to the inversion-layer channel, these charges will scatter the channel carriers, remotely (i.e. across the thickness of the SiO_2 IL), and hence cause "Remote" Coulomb (RC) scattering.

Starting with the general form for Coulomb scattering, considering a charge located in 3-dimensional space (0, 0, z_0), the screened Coulomb scattering potential is [9]

$$\phi(q,z,z_0) = \int_0^\infty dz_1\, K(z,z_1)\phi(q,z_1,z_0) + \frac{e}{2\epsilon_{Si}q}\exp(-q|z-z_0|) + A_1\exp(-qz) \tag{4.1}$$

where A_1 is a constant to be determined, and K(z, z_1) is called the "screening kernel", which describes the strength of carrier screening from the external field induced by the point charge, and has the form

$$K(z,z_1) = -\sum_i |\xi_i(z_1)|^2\, S_i \int_0^\infty dz_2\, |\xi_i(z_2)|^2 \frac{1}{q}\exp(-q|z-z_2|) \tag{4.2}$$

S_i is the screening constant for the i^{th} sub-band as [10]

$$S_i = \frac{e^2}{2}\cdot\frac{N_S^i}{k_BT\left(1+e^{\frac{E_i-E_f}{k_BT}}\right)ln\left(1+e^{\frac{E_f-E_i}{k_BT}}\right)} \tag{4.3}$$

In the oxide, neglecting the existence of free charge, the Poisson equation has the explicit solution [9]

$$\phi(q,z,z_0) = \frac{e}{2\varepsilon_{ox}q}\exp(-q|z-z_0|) + A_2\exp(-qz) + A_3\exp(qz) \tag{4.4}$$

Under the random phase approximation (RPA), (i.e. the different Coulomb scattering sources are uncorrelated in position) the total squared scattering matrix element is simply given by the summation of the squared matrix elements produced by each scattering source. For each source, the matrix element can be expressed as

$$M_{i,j}^0(q,z_0) = \frac{e}{A}\int_0^\infty dz\, \phi(q,z,z_0)\xi_i(z)\xi_j(z) \tag{4.5}$$

Thus, the total square matrix element is

$$\left|M_{i,j}^0(q)\right|^2 = A[\int dz_0\, N_{cont}(z_0)\left|M_{i,j}^0(q,z_0)\right|^2 + N_{intf}\left|M_{i,j}^0(q,0)\right|^2] \tag{4.6}$$

The coefficients A_i need to be determined from boundary conditions. For example, the ionized impurities scattering potential is (unscreened part) [7]

$$\phi(q,z,z_0)^{unscr} = \frac{e}{2\epsilon_{Si}q}\exp(-q|z-z_0|) + \left(\frac{\epsilon_{Si}-\epsilon_{SiO2}}{\epsilon_{Si}+\epsilon_{SiO2}}\right)\frac{e}{2\epsilon_{Si}q}\exp(-q(z+|z_0|)) \tag{4.7}$$

In particular, for the Coulomb centers located right at the oxide/silicon interface, the potential can be expressed as [7]

$$\phi(q,z,0)^{unscr} = \frac{e}{(\epsilon_{Si}+\epsilon_{SiO2})q}\exp(-q|z|) \tag{4.8}$$

For the RC scattering problem, in a high-κ/metal gated device (as shown in Fig. 4.1), assuming the charges are all located at the high-κ/IL interface [8], in the planar bulk MOSFET, the scattering potential within the high-κ region is

$$\phi(q,z,z_0) = \frac{e}{2\epsilon_{HK}q}\exp(-q|z-z_0|) + A_4\exp(-qz) + A_5\exp(qz) \quad (4.9)$$

Combining the unscreened potentials in the silicon channel and SiO_2 IL, and imposing the following boundary conditions:

$$\phi \; continuous \; at \; z = 0, -t_{SiO2} \quad (4.10)$$

$$\phi = 0 \; at \; z = -t_{SiO2} - t_{HK} \quad (4.11)$$

$$\frac{\partial\phi}{\partial z}\,\epsilon_{SiO2}\Big|_{z=0^-} = \frac{\partial\phi}{\partial z}\,\epsilon_{Si}\Big|_{z=0^+} \quad (4.12)$$

$$\frac{\partial\phi}{\partial z}\,\epsilon_{HK}\Big|_{z=-t_{SiO2}^-} - \frac{\partial\phi}{\partial z}\,\epsilon_{SiO2}\Big|_{z=-t_{SiO2}^+} = eN_{it} \quad (4.13)$$

One can get, in the silicon channel:

$$\phi(q,z,z_0)^{unscr} = \frac{e}{\epsilon_{Si}q}\cdot\frac{3N_{it}e^{q(t_{ox}-z)}(1-e^{2qt_{HK}})}{(\alpha-1)(e^{2qt_{HK}}-2e^{2qt_{ox}})+(\alpha+1)(1-2e^{2q(t_{ox}+t_{HK})})} \quad (4.14)$$

where $\alpha=\epsilon_{HK}/\epsilon_{SiO2}$ and $\epsilon_{Si}/\epsilon_{SiO2}=3$ is assumed in the derivation. The total Coulomb scattering potential also should include the screened part.

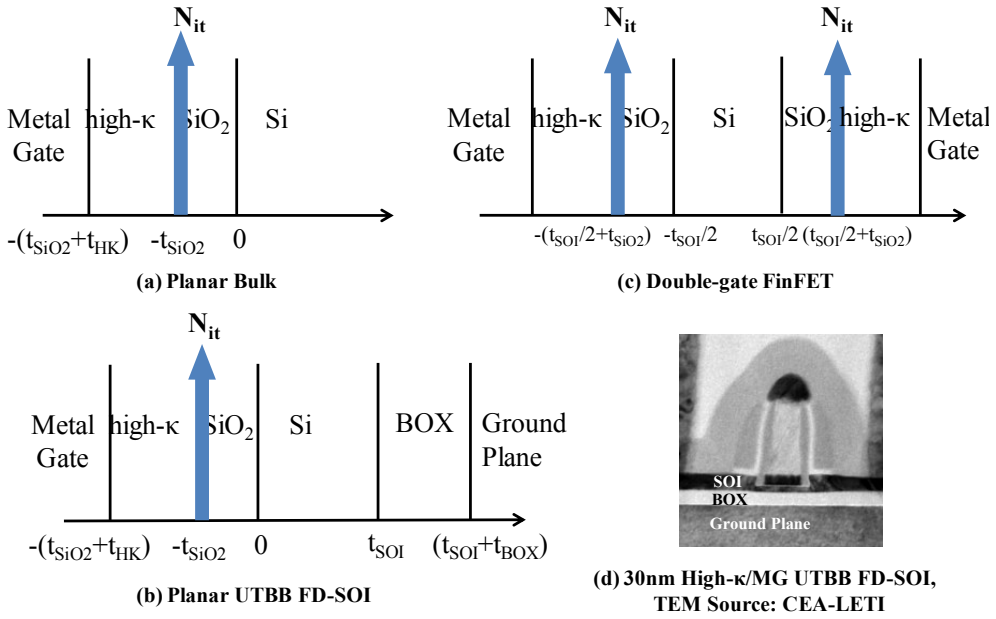

Figure 4.1, Gate/channel material stacks for (a) planar bulk MOSFET, (b) double-gate FinFET and (c) planar UTBB FD-SOI MOSFET and their definition of coordinates used in deriving the RC scattering potentials; the arrows show the locations of RC scattering charges. (d) shows the TEM cross-sectional view of a UTBB FD-SOI MOSFET with gate length of 30nm, fabricated by CEA-LETI [11].

For the UTBB FD-SOI structure (as shown in Fig. 4.1(b)), the Coulomb scattering potential induced by charge at high-κ/IL interface can be expressed as

$$\phi(q,z,z_0) = \frac{e}{2\epsilon_{Si}q}\exp(-q|z-z_0|) + A_1\exp(-qz) + A_2\exp(qz) \quad (4.15)$$

within the Silicon channel layer and

$$\phi(q,z,z_0) = \frac{e}{2\epsilon_{SiO2}q}\exp(-q|z-z_0|) + A_6\exp(-qz) + A_7\exp(qz) \tag{4.16}$$

within the BOX layer. The depletion charge in the substrate is ignored, since the BOX layer is usually thick (>10nm) so that the exponentially decayed Coulomb potential is negligible. By adding the extra boundary conditions as

$$\phi = 0\ at\ z = -t_{SiO2} - t_{HK}, t_{SOI} + t_{BOX} \tag{4.17}$$

$$\frac{\partial\phi}{\partial z}\ \epsilon_{Si}\Big|_{z=t_{SOI}^-} = \frac{\partial\phi}{\partial z}\ \epsilon_{SiO2}\Big|_{z=t_{SOI}^+} \tag{4.18}$$

One can get, in the Silicon channel:

$$\phi(q,z,z_0)^{unscr} = \frac{e}{\epsilon_{Si}q}\cdot\frac{3N_{it}e^{q(t_{ox}-z)}(1-e^{2qt_{HK}})(e^{2qz}+2e^{2qt_{SOI}})}{(\alpha-1)\left(2e^{2q(t_{HK}+t_{SOI})}-4e^{2q(t_{ox}+t_{SOI})}+e^{2qt_{ox}}-2e^{2qt_{HK}}\right)+\cdots} \tag{4.19}$$
$$\cdots(\alpha+1)(e^{2q(t_{HK}+t_{ox})}+2e^{2qt_{SOI}}-4e^{2q(t_{ox}+t_{HK}+t_{SOI})}-2)$$

Noted that when t_{SOI} is very large, the above expression approaches the planar bulk MOSFET case.

For the FinFET structure, (as shown in Fig. 4.1 (c)), due to the structural symmetry, the induced Coulomb potentials within the 2 high-κ layers are

$$\phi_{HK,\pm}(q,z,z_{0,\pm}) = \frac{e}{2\epsilon_{HK}q}\exp\left[\pm q\left(z-z_{0,\pm}\right)\right] + A_1\exp(\mp qz) + A_2\exp(\pm qz) \tag{4.20}$$

And within the SiO_2 IL, the potentials can be expressed as

$$\phi_{SiO2,\pm}(q,z,z_{0,\pm}) = \frac{e}{2\epsilon_{SiO_2}q}\exp\left[\pm q\left(z-z_{0,\pm}\right)\right] + A_3\exp(\mp qz) + A_4\exp(\pm qz) \tag{4.21}$$

Within the silicon channel, the potential has the form as

$$\phi_{Si}(q,z,z_{0,\pm}) = \frac{e}{2\epsilon_{Si}q}\left\{\exp\left[-q\left(z-z_{0,+}\right)\right] + \exp\left[q\left(z-z_{0,-}\right)\right]\right\} + A_5[\exp(qz) + \exp(-qz)\ ] \tag{4.22}$$

where $z_{0,\pm}$ refers to the charge (- for left gate, + for right gate) locations. By adding the extra boundary conditions as

$$\phi = 0\ at\ z = \pm(t_{SiO2} + t_{HK} + t_{SOI}/2) \tag{4.23}$$

ϕ is continuous at SiO_2/high-κ and Si/SiO_2 interface (4.24)

$$\frac{\partial\phi_{Si}}{\partial z}\ \epsilon_{Si}\Big|_{z=t_{SOI}} = \frac{\partial\phi_{SiO2}}{\partial z}\ \epsilon_{SiO2}\Big|_{z=t_{SOI}} \tag{4.25}$$

One can get the potentials in FinFET channel as:

$$\phi(q,z,z_0)^{unscr} = \frac{e}{\epsilon_{Si}q}\cdot\frac{3N_{it}\left[e^{q\left(t_{ox}+\frac{t_{SOI}}{2}\right)}+2e^{q\left(t_{ox}+\frac{3t_{SOI}}{2}\right)}\right](1-e^{2qt_{HK}})(e^{-qz}+e^{qz})}{(\alpha-1)\left(2e^{2q(t_{HK}+t_{SOI})}-4e^{2q(t_{ox}+t_{SOI})}+e^{2qt_{ox}}-2e^{2qt_{HK}}\right)+\cdots} \tag{4.26}$$
$$\cdots(\alpha+1)(e^{2q(t_{HK}+t_{ox})}+2e^{2qt_{SOI}}-4e^{2q(t_{ox}+t_{HK}+t_{SOI})}-2)$$

Once the screened RC scattering potentials have been determined, the matrix element and momentum relaxation rates (MRT) can be calculated using the Kubo-Greenwood formalism.

4.2.2 Surface Optical Phonon scattering

Compared to the classical gate dielectric material (i.e. SiO_2), the oxygen-metal bonds in a high-κ material easily polarize to screen the external electric field. These "soft" oxygen-metal bonds have lower optical phonon energy values, compared to those "hard" oxygen-Si bonds with high optical phonon energy values. Due to the oscillating nature of the ionic polarization at the oxide/silicon interface, there are scattering potentials induced from the dipoles, whose strength can be related to the static and optical permittivity (ϵ_0 and ϵ_∞, respectively) of the high-κ layer [12]. This scattering mechanism is called "surface" optical phonon (SOP) scattering, in contrast to conventional "bulk" optical phonon scatterings, and can be especially severe for a high-κ layer, due to the large difference between ϵ_0 and ϵ_∞, and the rather low optical phonon energy values (as shown in Tab. 4.1).

	SiO_2	HfO_2	ZrO_2
ϵ_0^{ox}	3.90	22.0	24.0
ϵ_i^{ox}	3.05	6.58	7.75
ϵ_∞^{ox}	2.50	5.03	4.00
$\hbar\omega_{TO,1}$(meV)	55.60	12.40	16.67
$\hbar\omega_{TO,2}$(meV)	138.1	48.35	57.70

Table 4.1. Frequency-dependent permittivity and optical phonon energy values for different oxide materials, from [12].

As derived in [13], the SOP scattering potentials at the front and back oxide interfaces (considering only the SiO_2/Si interfaces) are

$$\phi_{FI}(z) = \left[\frac{\hbar\omega_{SO}}{2\pi\widehat{\epsilon_s}q}\right]^{\frac{1}{2}} e^{-qz} \tag{4.27}$$

$$\phi_{BI}(z) = \left[\frac{\hbar\omega_{SO}}{2\pi\widehat{\epsilon_s}q}\right]^{\frac{1}{2}} e^{-q(t_{SOI}-z)} \tag{4.28}$$

where q is the wave vector change during the scattering event, $\hbar\omega_{SO}$ is SOP energy. The joint permittivity $\widehat{\epsilon}$ has different forms for the 2 SO modes (TO1 and TO2 for SiO_2)

$$\frac{1}{\widehat{\epsilon_1}} = \frac{1}{\epsilon_i^{ox}+\epsilon_{Si}} - \frac{1}{\epsilon_0^{ox}+\epsilon_{Si}} \tag{4.29}$$

$$\frac{1}{\widehat{\epsilon_2}} = \frac{1}{\epsilon_\infty^{ox}+\epsilon_{Si}} - \frac{1}{\epsilon_i^{ox}+\epsilon_{Si}} \tag{4.30}$$

where *0, i* and ∞ denote the static, intermediate and optical frequency permittivity. By assuming the phonon energy values are constant with the wave vector q:

$$\hbar\omega_{SO,1} = \left[\frac{\epsilon_0^{ox}+\epsilon_{Si}}{\epsilon_i^{ox}+\epsilon_{Si}}\right]^{1/2} \hbar\omega_{TO,1} \tag{4.31}$$

$$\hbar\omega_{SO,2} = \left[\frac{\epsilon_i^{ox}+\epsilon_{Si}}{\epsilon_\infty^{ox}+\epsilon_{Si}}\right]^{1/2} \hbar\omega_{TO,2} \tag{4.32}$$

Due to the large wave vector change, screening effect is neglected, SOP scatterings are restricted to intra-valley transitions. The total squared matrix element can be written as

$$\left|M_{SO}^{i,j}(q)\right|^2 = 4\pi^2 e^2 \left[\left|\int_0^\infty dz\, \xi_i(z)\xi_j(z)\phi_{FI}(z)\right|^2 + \left|\int_0^\infty dz\, \xi_i(z)\xi_j(z)\phi_{BI}(z)\right|^2\right] \quad (4.33)$$

The scattering rates are calculated based on inelastic phonon scattering from [13]

$$\frac{1}{\tau_i(E)} = \frac{2\pi}{\hbar}\sum_j \int \left|M_{SO}^{i,j}(q)\right|^2 \times \frac{1-f_0(E\pm\hbar\omega)}{1-f_0(E)} \times \left[N_{op} + \frac{1}{2} \mp \frac{1}{2}\right] \times (1-cos\theta)d^2k \quad (4.34)$$

For the high-κ/metal gate stack, a comprehensive form was derived in [12] as follows.
Firstly, the permittivity is modeled as function of phonon frequency as

$$\epsilon^{HK}(\omega) = \epsilon_i^{HK} + \frac{\epsilon_0^{HK} - \epsilon_i^{HK}}{1-\left(\frac{\omega}{\omega_{TO}}\right)^2} \quad (4.35)$$

$$\epsilon^{ox}(\omega) = \epsilon_i^{ox} + \frac{\epsilon_0^{ox} - \epsilon_i^{ox}}{1-\left(\frac{\omega}{\omega_{TO}}\right)^2} \quad (4.36)$$

The low (TO1) and high (TO2) frequency from the high-κ layer are:

$$\hbar\omega_{SO,1(2)}^{HK} = \left[\frac{\epsilon_{0(i)}^{HK} + \epsilon_{Si}}{\epsilon_{i(\infty)}^{HK} + \epsilon_{Si}}\right]^{1/2} \hbar\omega_{TO,1(2)} \quad (4.37)$$

$$\hat{\epsilon}^{HK}{}_{high(low)} = \epsilon_{i(0)}^{HK}\left[\frac{\epsilon^{ox}(\omega)+\epsilon_{Si}}{\epsilon^{ox}(\omega)-\epsilon_{HK}(\omega)}\right]^2 e^{2qt_{ox}} + \epsilon^{ox}(\omega)\left\{\left[\frac{\epsilon^{ox}(\omega)+\epsilon_{Si}}{2\epsilon^{ox}(\omega)}\right]^2 (e^{2qt_{ox}}-1) + \ldots\left[\frac{\epsilon^{ox}(\omega)-\epsilon_{Si}}{2\epsilon^{ox}(\omega)}\right]^2 (1-e^{-2qt_{ox}})\right\} + \epsilon_{Si} \quad (4.38)$$

where the above frequency-dependent quantities should be evaluated at $\omega_{SO,1(2)}^{HK}$ separately.

The SiO_2 interfacial layer will totally induce a total of 4 TO modes: for low (TO1) and high (TO2) frequency; and one from Si/SiO_2 IL interface (-), the other from SiO_2 IL/high-κ interface (+)

$$\hbar\omega_{SO,1(2)}^{ox+} = \left[\frac{\epsilon_{0(i)}^{ox} + \epsilon_{\infty}^{HK}}{\epsilon_{i(\infty)}^{ox} + \epsilon_{\infty}^{HK}}\right]^{1/2} \hbar\omega_{TO,1(2)} \quad (4.39)$$

$$\hbar\omega_{SO,1(2)}^{ox-} = \left[\frac{\epsilon_{0(i)}^{ox} + \epsilon_{Si}}{\epsilon_{i(\infty)}^{ox} + \epsilon_{Si}}\right]^{1/2} \hbar\omega_{TO,1(2)} \quad (4.40)$$

$$\hat{\epsilon}^{ox}{}_{high(low)} = \epsilon^{HK}(\omega)\left[\frac{\epsilon^{ox}(\omega)+\epsilon_{Si}}{\epsilon^{ox}(\omega)-\epsilon_{HK}(\omega)}\right]^2 e^{2qt_{ox}} + \epsilon_{i(0)}^{ox}\left\{\left[\frac{\epsilon^{ox}(\omega)+\epsilon_{Si}}{2\epsilon^{ox}(\omega)}\right]^2 (e^{2qt_{ox}}-1) + \ldots\left[\frac{\epsilon^{ox}(\omega)-\epsilon_{Si}}{2\epsilon^{ox}(\omega)}\right]^2 (1-e^{-2qt_{ox}})\right\} + \epsilon_{Si} \quad (4.41)$$

where all the above frequency-dependent quantities should be evaluated at $\omega_{SO,1(2)}^{ox+/-}$ separately.

In thin-body structures, the SOP scattering is even worse [13] than that in the planar bulk MOSFET. The reasons are twofold: first, due to the existing 2 oxide/silicon interfaces, SOP scattering potentials are present at both the front and back interfaces; second, the spatial-

dependence of the SOP scattering potential (as seen in eqns. (4.27), (4.28)) suggests that when the silicon body thickness is reduced, the decay of scattering potential will be smaller, which results in overall high SOP scattering rates. However, by replacing the poly-Si gate with a metal material, the SOP scattering is largely reduced and high channel mobility values (i.e. close to that for a poly-Si/SiO_xN_y gate stack) are observed, experimentally [14]. This is attributed to the metal gate screening effect, which will remove the transverse optical modes from the high-κ layer, as explained in [14, 15]. In general, SOP scattering in high-κ/metal gate MOSFET is less important than RC scattering, in terms of the carrier mobility degradation.

4.3 High-κ/Metal Gate Thin-Body MOSFET Carrier Mobility Enhancement via Strain Engineering

4.3.1 Experimental

UTBB FD-SOI MOSFETs with undoped channels and high-κ/metal gate stacks (1.2nm EOT) were fabricated on (100) silicon substrates. The silicon body thickness (t_{SOI}) is 7nm and BOX thickness (t_{BOX}) is 10nm. Field-effect mobility values were extracted using the split-CV method from long-channel devices. To study the effect of strain, a wafer-bending apparatus was used to induce uniaxial in-plane stress up to ±170MPa.

To adequately suppress OFF-state leakage, the silicon body thickness is 1/3 of the gate length (L_g) for a UTBB FD-SOI MOSFET and 1/2 of L_g for the FinFET [16], which are also consistent with ITRS specifications [17]. Besides having different channel surface crystalline orientation ((110) for the FinFET vs. (100) for the UTBB FD-SOI MOSFET), the FinFET is more sensitive to RC scattering because it has 2 surfaces gated by a metal gate/high-κ stack, as illustrated in Fig. 4.2.

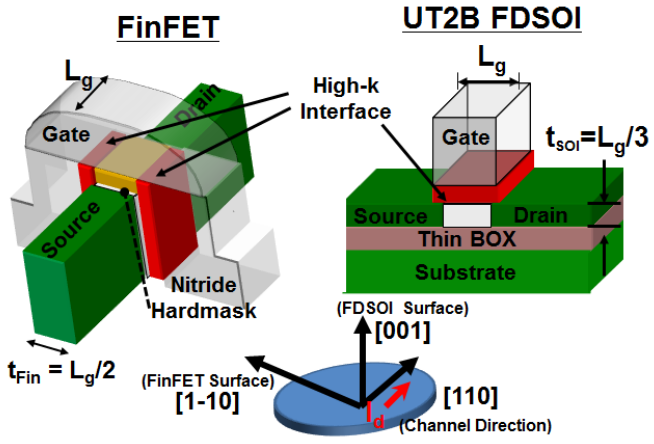

Figure 4.2, Illustration of high-κ/metal gate MOSFET structures studied in this work, with [110]-oriented channels. Note that the silicon body thinness requirement is different for the FinFET vs. the UTBB FD-SOI MOSFET.

Simulated long-channel UTBB FD-SOI MOSFET carrier mobility vs. inversion charge concentration curves are fitted to experimental data measured at various temperatures and with

longitudinal bending-induced stress, as shown in Fig. 4.3. The FD-SOI surface roughness amplitude (Δ) and correlation length (L_c) are extracted herein, while the phonon and the FinFET sidewall surface roughness parameters are taken from [18]. For both structures, the roughnesses of the two SiO_2 IL/Si interfaces are assumed to be non-correlated [19]. To account for RC scattering effect on carrier mobilities, following the above derived formalism, surface charge is added between the high-κ dielectric and SiO_2 IL. It has been shown in [14, 20] that RC scattering is the dominant Coulomb scattering mechanism for mobility degradation in high-κ/metal gate MOSFETs. As shown in Fig. 4.3, it is evident that stress-induced mobility enhancement is diminished at low inversion charge concentrations.

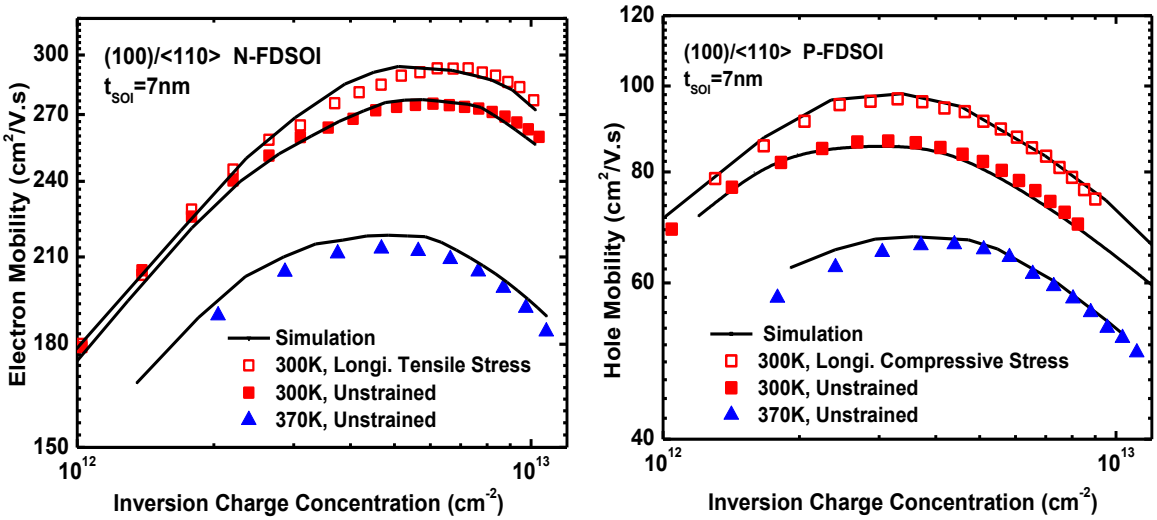

Figure 4.3, Measured and simulated electron (left) and hole (right) mobility versus inversion charge concentration in L_g = 10 um UTBB FD-SOI MOSFETs, at various temperatures, w/o stress and with ±170 MPa uniaxial longitudinal stress. With phonon and surface roughness parameters calibrated at high inversion charge concentration first, a surface charge of 1.4e13 cm^{-2} is extracted for the high-κ/IL interface, from fitting simulations with measured data.

4.3.2 Benchmarking of Thin-Body MOSFETs Carrier Mobility

Sub-band structures were calculated by Poisson-Schrödinger self-consistent simulators, using the non-parabolic effective mass approximation (EMA) for electrons and 6×6 k·p approach for holes. Fig. 4.4 shows the equi-energy contours for the lowest-energy subband in the thin body region of these 2 FET structures. Longitudinal [110] stress – which is commonly used to enhance the performance of planar bulk MOSFETs – is an effective mobility booster mainly for a p-channel UTBB FD-SOI MOSFET (due to a large reduction in transport mass, *i.e.* band curvature change caused by the shear strain); for p-channel FinFET, the transport mass reduction is marginal.

Carrier mobility values for scaled UTBB FD-SOI MOSFETs and FinFETs were simulated using the calibrated parameters, and are plotted vs. inversion charge concentration, for various values of L_g. The IL thickness and RC density are fixed at 1 nm and 1.4×10^{13} cm^{-2}. For FD-SOI and p-channel FinFET structures, longitudinal stress (as compared to other directional stresses) is

most effective to enhance carrier mobilities, because shear strain components can reduce carrier transport mass remarkably. For the n-channel FinFET, vertical stress provides the largest electron mobility (μ_e) enhancement, which is due to significant carrier redistribution to the low-transport-mass Δ-2 valleys [21].

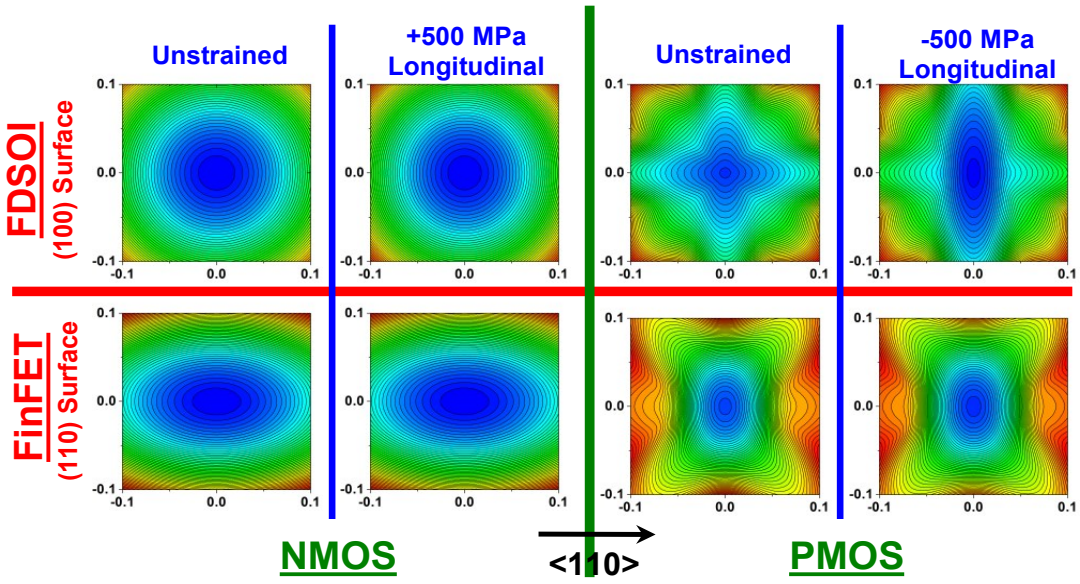

Figure 4.4, Calculated equi-energy contours for the lowest sub-band of inversion electrons (left) and holes (right) (within +/- 0.1 Brillouin zone) in UTBB FD-SOI MOSFET (upper) and FinFET (lower), w/o stress and with +/- 500MPa longitudinal stress.

Fig. 4.5 (top) compares μ_e for the thin-body MOSFET structures. The UTBB FD-SOI MOSFET has higher μ_e than does the FinFET due to the smaller transport mass for the (100) plane; this advantage diminishes with decreasing t_{SOI}, however. When the occupation of Δ-2 valleys by inversion electrons increases (by increasing geometric confinement or strain-induced sub-band splitting), μ_e is more vulnerable to RC scattering [7]; thus the benefit of reduced transport effective mass will decrease, and μ_e enhancement will diminish. Since the UTBB FD-SOI MOSFET requires a thinner body at the same L_g, this degradation in mobility enhancement is larger. Note that a previously observed μ_e peak for the (100) surface with a poly-Si/SiO_2 gate stack at t_{SOI} ~3.5nm [22] is not seen here, due to the impact of RC scattering. The screening effect is modeled by scalar dielectric functions [23] in this work; as a result, μ_e for the FinFET is underestimated for the range of t_{Fin} values considered herein. Thus, the μ_e advantage of the FD-SOI MOSFET likely will be smaller and may disappear altogether for sub-10 nm gate lengths.

Fig. 4.5 (bottom) compares hole mobility (μ_h) for the thin-body MOSFET structures. The higher μ_h advantage of the FinFET (resulting from the (110) high μ_h sidewall surfaces) is diminished at low inversion charge densities. This is because the inversion (hole) layer centroid is closer to the oxide interface (and hence the remote Coulomb charge centers) for the (110) channel surface orientation than for the (100) orientation [24]. However, μ_h degrades more quickly with decreasing t_{SOI} in the UTBB FD-SOI MOSFET, because the phonon scattering form factor and transport effective mass grow more quickly with decreasing silicon layer thickness for

the (100) channel surface orientation than for the (110) orientation [24]. Thus, the FinFET μ_h advantage increases with body thickness scaling.

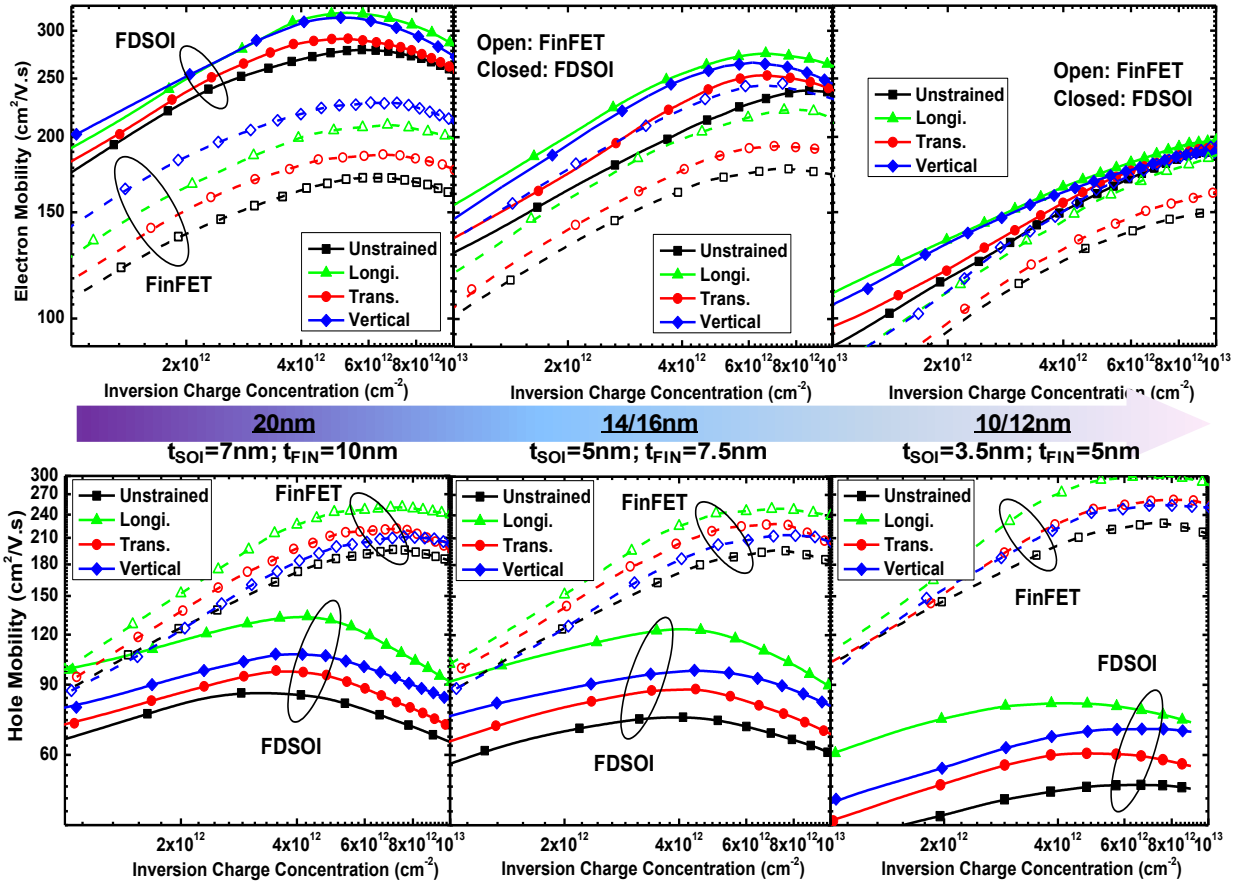

Figure 4.5, Simulated (top) electron and (bottom) hole mobility in high-κ/metal gated UTBB FDSOI MOSFET and FinFET devices, with scaling of the silicon body thickness. Within each plot, the effect of uniaxial stress for each of the 3 directions (for NMOS, +500 MPa Longitudinal & Transverse, -500 MPa Verticalal; for PMOS, -500 MPa Longitudinal, +500 MPa Transverse & Vertical), is shown.

4.4 Summary

Stress-induced carrier mobility enhancement with body thickness scaling is studied for UTBB FD-SOI MOSFETs and FinFETs with high-κ/metal gate stacks. It is found that the advantage of the high-μ_e (100) surface for the UTBB FD-SOI MOSFET will diminish, whereas the advantage of the high-μ_h (110) surfaces for the FinFET will be maintained with scaling. Mobility trends can be used to project enhancements in short-channel device performance due to the determinative role of carrier scattering in silicon MOSFETs.

4.5 References

[1] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi, L. F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet, S. Holmes, S. Mehta, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, B. S. Haran, Z. Zhu, L. H. Vanamurth, S. Fan, D. Horak, H. Bu, P. J. Oldiges, D. K. Sadana, P. Kozlowski, D. McHerron, J. O'Neill, B. Doris "Extremely Thin SOI (ETSOI) CMOS with Record Low Variability for Low Power System-on-Chip Applications," IEDM Tech. Dig. 2009, pp.49-52.

[2] V. S. Basker, T. Standaert, H. Kawasaki, C.-C. Yeh, K. Maitra, T. Yamashita, J. Faltermeier, H. Adhikari. H. Jagannathan, J. Wang, H. Sunamura, S. Kanakasabapathy, S. Schmitz, J. Cummings, A. Inada, C. -H. Lin, P. Kulkarni, Y. Zhua, J. Kuss, T. Yamamoto, A. Kumara, J. Wahl, A. Yagishita, L. F. Edge, R. H. Kim, E. Mclellan, S. J. Holmes, R. C. Johnson, T. Levin, J. Demarest, M. Hane, M. Takayanagi, M. Colburn, V. K. Paruchuri, R. J. Miller, H. Bu, B. Doris, D. McHerron, E. Leobandung and J. O'Neill, "A 0.063 μm^2 FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch," Symp. on VLSI Tech. Dig., 2010, pp.19-20.

[3] K. Shimizu, G. Tsutsui, T. Hiramoto, "Experimental Study on Mobility Universality in (100) Ultra-Thin Body nMOSFET with SOI Thickness of 5nm," IEEE Int. SOI Conf. Proc. , 2006, pp.175-176.

[4] T. Irisawa, K. Okano, T. Horiuchi, H. Itokawa, I. Mizushima, K. Usuda, T.Tezuka, N. Sugiyama, S. Takagi, "Electron Mobility and Short-Channel Device Characteristics of SOI FinFETs With Uniaxially Strained (110) Channels," IEEE Transactions on Electron Devices, Vol.56, no.8, 2009, pp.1651-1658.

[5] M. Saitoh, A. Kaneko, K. Okano, T. Kinoshita, S. Inaba, Y. Toyoshima, K. Uchida, "Three-Dimensional Stress Engineering in FinFETs for Mobility/On-Current Enhancement and Gate Current Reduction," Symp. on VLSI Tech., 2008, pp.18-19.

[6] C. Auth, A. Cappellani, J.-S. Chun, A. Dalis, A. Davis, T. Ghani, G. Glass, T. Glassman, M. Harper, M. Hattendorf, P. Hentges, S. Jaloviar, S. Joshi, J. Klaus, K. Kuhn, D. Lavric, M. Lu, H. Mariappan, K. Mistry, B. Norris, N. Rahhal-orabi, P. Ranade, J. Sandford, L. Shifren, V. Souw, K. Tone, F. Tambwe, A. Thompson, D. Towner, T. Troeger, P. Vandervoorn, C. Wallace, J. Wiedemer, C. Wiegand "45nm High-κ+Metal Gate Strain-Enhanced Transistors," Symp. on VLSI Tech., 2008, pp.128-129.

[7] F. Driussi, D. Esseni, "Simulation Study of Coulomb Mobility in Strained Silicon," IEEE Transactions on Electron Devices, Vol.56, no.9, 2009, pp.2052-2059.

[8] C.-Y. Lu, K.-S. C.-Liao, P.-H. Tsai, T.-K. Wang, "Depth Profiling of Border Traps in MOSFET With High-κ Gate Dielectric by Charge-Pumping Technique," IEEE Electron Device Letters, vol. 27, no.10, 2006, pp.859-861.

[9] D. Esseni, A. Abramo, "Modeling of Electron Mobilioty Degradation by Remote Coulomb Scattering in Ultrathin Oxide MOSFETs," IEEE Transactions on Electron Devices, Vol.50, no.7, 2003, pp.1665-1674.

[10] K. Yokoyama, K. Hess, "Monte Carlo study of electronic transport in $Al_{1-x}Ga_xAs/GaAs$ single-well heterostructures," Physical Review B, vol.33, no.8, 1996, pp.5595-5606.

[11] F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J-P. Noel, C. Fenouillet-Béranger, J-P. Mazellier, P. Perreau, T. Poiroux, Y. Morand, T. Morel, S. Allegret, V. Loup, S. Barnola, F. Martin, J-F. Damlencourt, I. Servin, M. Cassé, X. Garros, O. Rozeau, M-A. Jaud, G.

Cibrario, J. Cluzel, A. Toffoli, F. Allain, R. Kies, D. Lafond, V. Delaye, C. Tabone, L. Tosti, L. Brévard, P. Gaud, V. Paruchuri, K.K. Bourdelle, W. Schwarzenbach, O. Bonnin, B-Y. Nguyen, B. Doris, F. Boeuf, T. Skotnicki, O. Faynot, "Low Leakage and Low Variability Ultr-Thin-Body and Buried Oxide (UT2B) SOI Technology for 20nm Low Power CMOS and Beyond," Symp. on VLSI Tech. Dig., 2010, pp.57-58.

[12] M. V. Fischetti, D. A. Neumayer, E. A. Cartier, "Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high-κ insulator: The role of remote phonon scattering," Journal of Applied Physics, 90, 9, 2001, pp. 4587-4608.

[13] D. Esseni, A. Abramo, L. Selmi, E. Sangiorgi, "Physically Based Modeling of Low Field Electron Mobility in Ultrathin Single- and Double-Gate SOI n-MOSFETs," IEEE Transactions on Electron Devices, Vol.50, no.12, 2003, pp.2445-2454.

[14] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, M. Metz, "High-κ/Metal-Gate Stack and Its MOSFET Characteristics," IEEE Electron Device Letters, vol. 25, no.6, 2004, pp.408-410.

[15] K. Maitra, "Electron Transport in Bulk-Si NMOSFETs in presense of High-κ Gate Insulator – Charge Trapping and Mobility," Ph.D. Thesis, available on-line at: http://repository.lib.ncsu.edu/ir/bitstream/1840.16/3246/1/etd.pdf

[16] J.G. Fossum, L.Q. Wang, J.W. Yang, S.H. Kim, V.P. Trivedi, "Pragmatic Design of Nanoscale Multi-gate CMOS," IEDM Tech. Dig., 2004, pp. 613-616.

[17] International Technology Roadmap for Semiconductors, 2009 Edition.

[18] N. Xu, X. Sun, W. Xiong, C. R. Cleavelin, T.-J. King Liu, "MuGFET Carrier Mobility and Velocity: Impacts of Fin Aspect Ratio, Orientation and Stress," IEDM Tech. Dig. , 2010, pp. 194-197.

[19] D. Esseni, "On the Modeling of Surface Roughness Limited Mobility in SOI MOSFETs and Its Correlation to the Transistor Effective Field," IEEE Transactions on Electron Devices, vol.51, no.3 2004, pp.394-401.

[20] M. Casse, L. Thevenod, B. Guillaumot, L. Tosti, F. Martin, J. Mitard, O. Weber, F. Andrieu, T. Ernst, G. Reimbold, T. Billon, M. Mouis, F. Boulanger, "Carrier Transport in HfO_2/Metal Gate MOSFETs: Physical Insight Into Critical Parameters," IEEE Transactions on Electron devices, vol.53, no.4, 2006, pp.759-768.

[21] N. Serra, D. Esseni, "Mobility Enhancement in Strained n-FinFETs: Basic Insight and Stress Engineering," IEEE Transactions on Electron devices, vol.57, no.2, 2010, pp.482-490.

[22] K. Uchida, M. Saitoh, S. Kobayashi, "Carrier Transport and Stress Engineering in Advanced Nanoscale Transistors From (100) and (110) Transistors To Carbon Nanotube FETs and Beyond," IEDM Tech. Dig., 2008, pp.569-572.

[23] P. Toniutti, D. Esseni, P. Palestri, "Failure of the Scalar Dielectric Function Approach for the Screening Modeling in Double-Gate SOI MOSFETs and in FinFETs," IEEE Transactions on Electron Devices, vol.57, no.11, 2010, pp. 3074-3083.

[24] L. Donetti, F. Gámiz, N. Rodriguez, F. Jiménez-Molinos, J.B. Roldán, "Hole Transport in DGSOI Devices: Orientation and Silicon Thickness Effects," Solid-State Electronics, vol.54, 2010, pp.191-195.

Chapter 5

Back Bias Impact on Ultra-Thin-Body and BOX Fully Depleted SOI MOSFET Performance

5.1 Introduction

The fully depleted silicon-on-insulator (FD-SOI) MOSFET structure with a very thin (~10 nm thick) buried oxide (BOX) layer can well suppress OFF-state leakage current as well as random variations in threshold voltage (V_{th}), due to its superior electrostatic integrity and moderate channel dopant concentration [1-4], so that it is a promising alternative for sub-20 nm CMOS technology. An advantage of the Ultra-Thin Body and BOX (UTBB) structure is that it allows V_{th} to be easily tuned via back biasing, in contrast to thick-BOX SOI MOSFETs and FinFETs [3]. This independent 'double-gate' operation can be leveraged to optimize energy-performance tradeoffs in circuit design [4]. Recently reported UTBB FD-SOI technologies [1, 4] use a combination of metallic gate materials and back biasing to achieve multiple levels of V_{th}. It will be important to retain this V_{th} tuning capability with gate length (L_g) scaling, *i.e.* for extremely thin BOX and SOI (~5 nm thick) [2, 4]. Gate-Induced Drain Leakage (GIDL) current due to trap-assisted and band-to-band tunneling increases with reverse back bias [5] and hence imposes a limit for reverse back biasing voltage. The impact of back bias on effective mobility is of interest, since mobility will continue to be a gauge for silicon MOSFET carrier velocity and the ON-state drive current, even for devices with deca-nanometer channel length [6, 7]. Due to the sub-band re-population effect, the strain-induced carrier mobility enhancement depends on the transverse electric field [8]. Therefore, the amount of strain-induced UTBB FD-SOI MOSFET performance enhancement can be further modulated by applying back bias.

In this chapter, the impact of back bias on UTBB FD-SOI MOSFET performance is investigated, for long-channel as well as short-channel devices. Trends with SOI thickness (t_{SOI}) and L_g scaling are examined. In Section 5.2, back bias effects on UTBB FD-SOI MOSFET device electrostatics (including V_{th} and GIDL) are presented. In Section 5.3, the modulation of back biasing on carrier transport behaviors (including carrier mobility, velocity and strain-induced enhancement) in UTBB FD-SOI MOSFET and its implications for deeply scaled device performance are presented. Section 5.4 summarizes the conclusions from these works.

5.2 Back Bias Effect on Ultra-Thin-Body and BOX Fully Depleted SOI MOSFET Electrostatics

N-channel UTBB FD-SOI MOSFETs were fabricated on (100) SOI substrates, with channels oriented in the <110> direction [9]. A p-type ground plane was formed under the thin BOX. The gate dielectric is 2.5-nm-thick SiO_xN_y and the gate material is comprised of 5-nm-thick TiN capped with 100-nm-thick doped poly-Si. The source/drain extensions were formed by ion implantation and the raised-source/drain regions were formed by Selective Epitaxial Growth (SEG). Split-CV measurements were performed at 1 MHz on devices with various values of drawn gate length (L_{mask}). Parasitic capacitances are independent of L_{mask} and subtracted out to obtain the intrinsic gate capacitance values. The offset (ΔL) between L_{mask} and the effective channel length (L_{eff}) was extracted from the gate-capacitance *vs*. L_{mask} plot (not shown here). L_{eff} ranges from 52 nm to 172 nm for the devices studied in this work. Measured I_d-V_g curves with different back bias from these devices are shown in Fig.5.1.

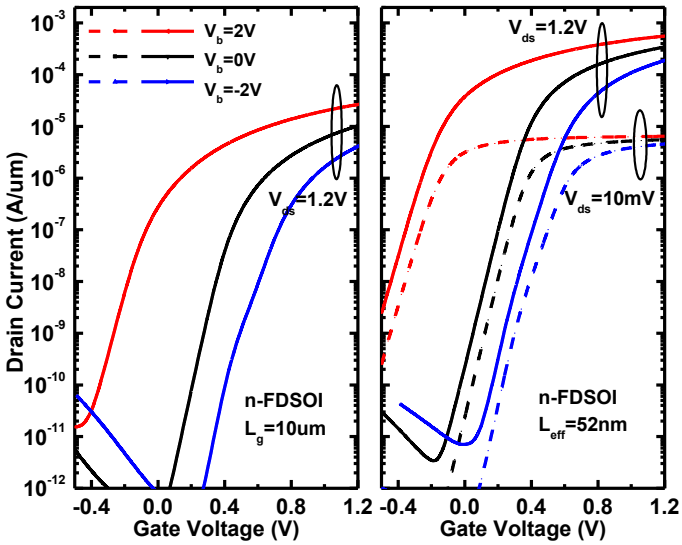

Figure 5.1, Measured I_d-V_g characteristics from UTBB FD-SOI nMOSFETs with (left) L_g=10um and (right) L_{eff}=52nm, under different back bias voltage.

To predict the impact of extreme t_{SOI} scaling on UTBB FD-SOI MOSFET electrostatics, quantum-mechanical device simulations are required. The self-consistent Poisson-Schrödinger solution method is used, with the non-parabolic effective mass approximation (EMA) and considering both Δ2-and Δ4-valley electrons [10], to simulate the one-dimensional electrostatics of the thin silicon film structure. Simulations of areal gate capacitance *vs.* gate voltage well predict the effect of back bias, as shown in Fig. 5.2, for calibrated values of BOX thickness (11 nm) and t_{SOI} (11 nm). For large forward back bias (FBB), an inversion layer is formed first at the back oxide interface as the gate voltage is increased. This results in a 'plateau' in the C-V characteristic for V_b = 2.5 V, since the capacitive coupling between the gate and the back inversion layer is lower than that between the gate and the front inversion layer.

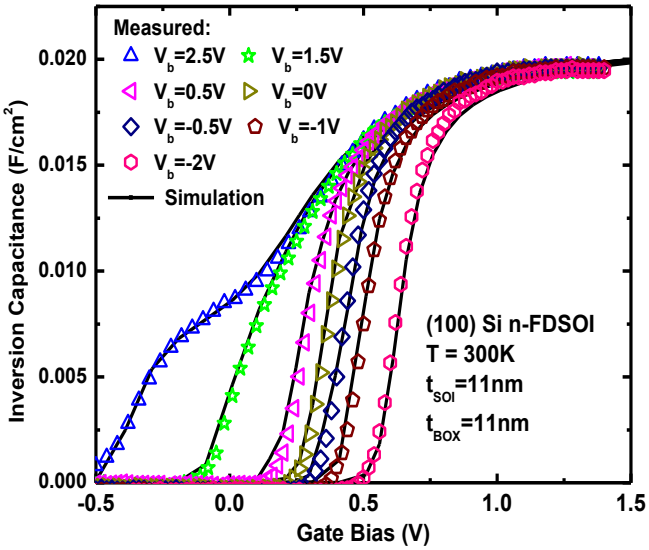

Figure 5.2, Effect of back bias on inversion capacitance compared against Poisson-Schrödinger simulation results, from long channel (L_g=10um) UTBB FD-SOI nMOSFETs.

The V_{th} of a UTBB FD-SOI MOSFET is easily adjusted by back biasing. A reverse back bias (RBB) increases V_{th}, whereas a FBB reduces V_{th}. To predict the V_{th} tuning capability for extremely thin BOX and SOI, which will be necessary to maintain good electrostatic integrity for channel length below ~15 nm [2, 4], UTBB structures with scaled values of t_{SOI} and BOX thickness (t_{BOX}) were simulated and the back bias coefficient was extracted for an inversion charge density of 1E10 cm^{-2}, corresponding to V_{th}. As shown in Fig. 5.3, the impact of back biasing is larger for FBB than for RBB –more remarkably for thinner t_{BOX}. As t_{SOI} is reduced, the FBB coefficient decreases and the RBB coefficient increases so that this difference is diminished.

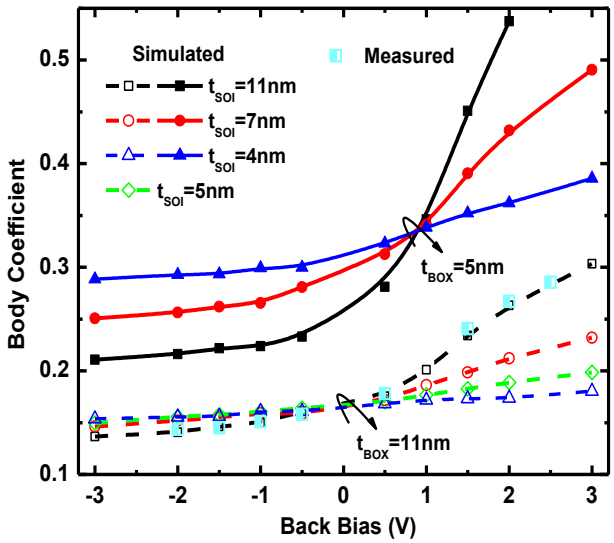

Figure 5.3, Simulated back bias coefficient vs. back bias voltage in UTBB FD-SOI nMOSFETs, for different values of t_{SOI} and t_{BOX}.

A capacitor network model is proposed herein to evaluate the dependence of the back bias coefficient on various parameters. Due to strong quantum confinement in thin silicon films, the inversion charge peak appears at some distance (so-called inversion layer thickness Z_{inv}, ~1 nm under strong inversion) below the oxide/silicon interface. At V_{th}, device with strong FBB will have the inversion layer formed first at the back oxide interface, and the front interface is depleted, as the Possion-Schrödinger simulation shows in Fig. 5.4 (left). On the other hand, Z_{inv} from device with RBB doesn't change much with varying t_{SOI} and back biasing voltage values (as shown in Fig. 5.4 (right)), which results in smaller body coefficient.

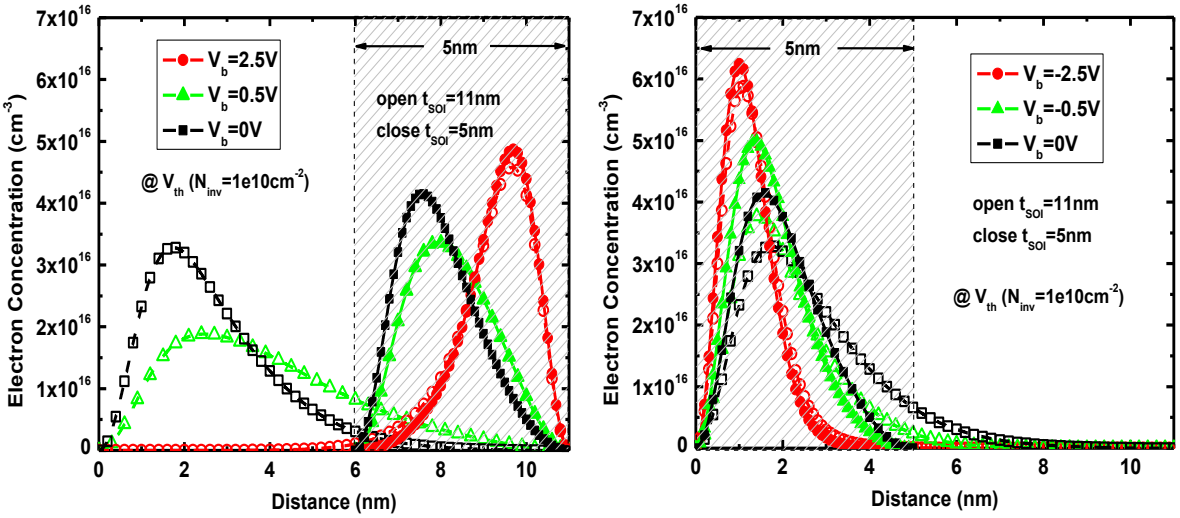

Figure 5.4, Possion-Schrödinger simulation of inversion charge distribution across UTBB FD-SOI nMOSFET thickness at V_{th} (corresponding to an inversion electron concentration of 1e10cm^{-2}), with (left) FBB and (right) RBB.

Therefore, the capacitance model for the silicon region consists of two capacitors in series, delineated by the position of the inversion charge peak. Accounting for the gate oxide capacitance and buried oxide capacitance, an expression for the back bias coefficient is derived and shown in Fig. 5.5. (*EOT* is the equivalent oxide thickness of the gate stack, and a value of 3 is assumed for the ratio of silicon and SiO_2 permittivities.) It is clear from this expression that the back bias coefficient has opposite dependence on t_{SOI} for FBB vs. RBB, due to the back-bias-modulated Z_{inv}.

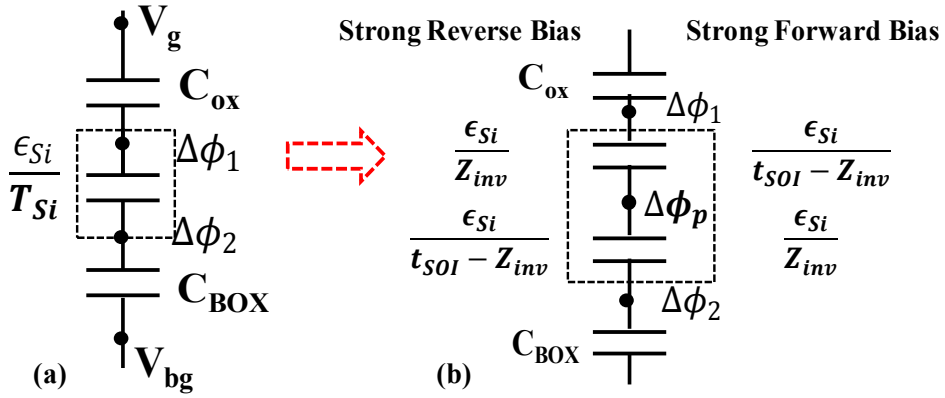

Figure 5.5, Capacitor network used to model the impact of back biasing on UTBB FD-SOI MOSFET threshold voltage.

Measured I_{off} *vs.* I_{on} plots for short-channel UTBB FDSOI nMOSFETs (achieved by varying the back bias) are shown in Fig. 5.6 (left). In these devices, the I_{off} lower limit is set by GIDL. Fig. 5.6 (right) shows how the OFF-state current of a 52-nm-L_{eff} device changes with back bias. It can be seen that GIDL current increases with increasing RBB, consistent with the trend for a planar bulk MOSFET.

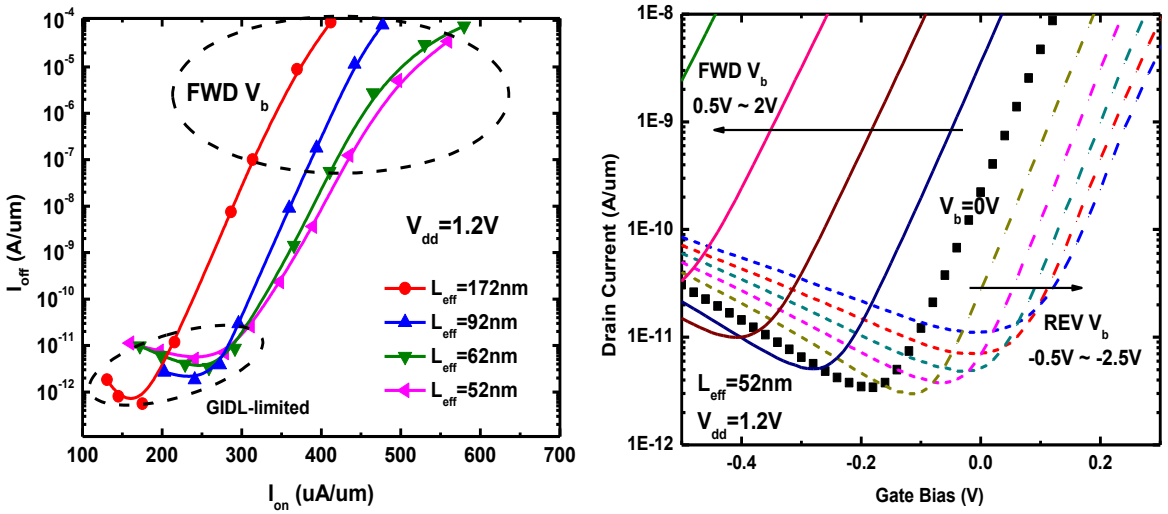

Figure 5.6, (left) Measured I_{off} vs. I_{on} for short channel UTBB FD-SOI MOSFETs; (right) measured OFF state current for a 52 nm device.

5.3 Back Biasing Modulation of Carrier Transport in Ultra-Thin-Body and BOX Fully Depleted SOI MOSFETs

5.3.1 Back Biasing Modulation of Low-Field Carrier Mobility

Within this section, UTBB FD-SOI MOSFETs with more aggressively-scaled t_{SOI} and L_g are used. These devices have undoped <110>-oriented channels and high-κ/metal gate stacks (1.2nm EOT) fabricated on (100) substrates using a gate-first process flow [1]. t_{SOI} = 7nm, and

the BOX thickness is 10nm. Field-effect mobility values were extracted using the split-CV method. A bending apparatus was used to induce longitudinal stress (S_{xx}). To study the short-channel device carrier transport characteristics, the procedure described in [11, 12] based on the Y-function approach was used: source/drain parasitic series resistance (R_{sd}) is decoupled before the short-channel apparent mobility ($|V_{ds}|$=10mV) and ON-state ($|V_{ds}|$=1V) velocity are extracted.

Fig. 5.7 compares extracted long-channel (L_g=10um) electron (μ_e) and hole mobility (μ_h) data against simulations, for different back bias voltages. Mobility improvement under FBB is clearly seen, due to reduced transverse electric field and increased distance between the inversion-layer charge centroid and the top gate dielectric (high-κ) interface. The short-channel (L_g=30nm) device shows greater mobility enhancement with FBB than the long-channel device. This is further investigated in the apparent mobility vs. L_g plots in Fig. 5.8, which show that FBB slows the degradation in apparent mobility with L_g scaling, in contrast to RBB, indicating that the dominant scattering centers in short-channel devices are located near the top gate dielectric (high-κ) interface [13].

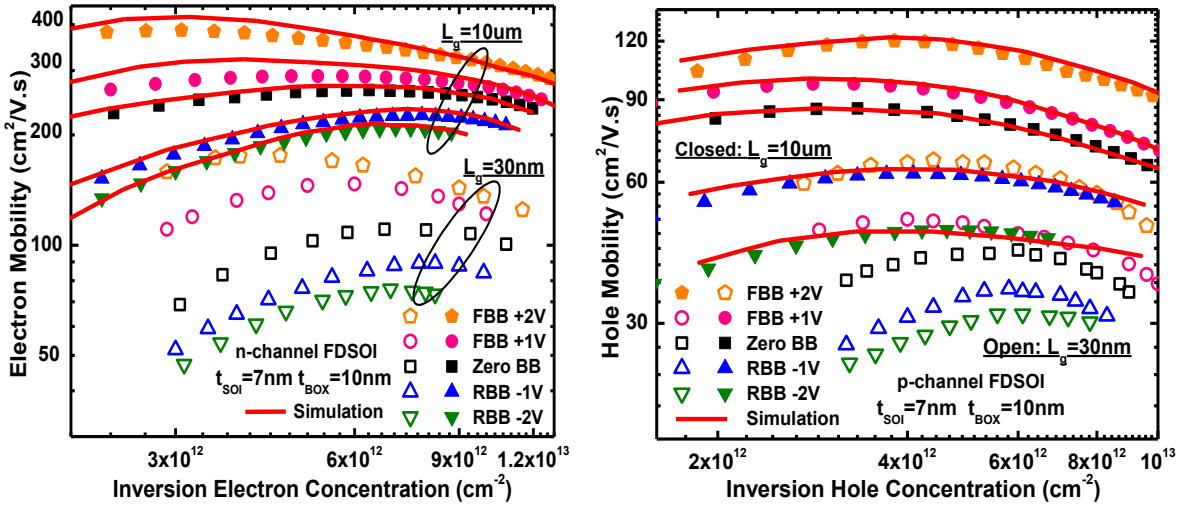

Figure 5.7, Measured and simulated (left) electron and (right) hole mobility vs. inversion charge concentration in L_g=10um UTBB FD-SOI MOSFETs, under different back bias. Open symbols show extraction results from L_g=30nm devices using method in [11, 12].

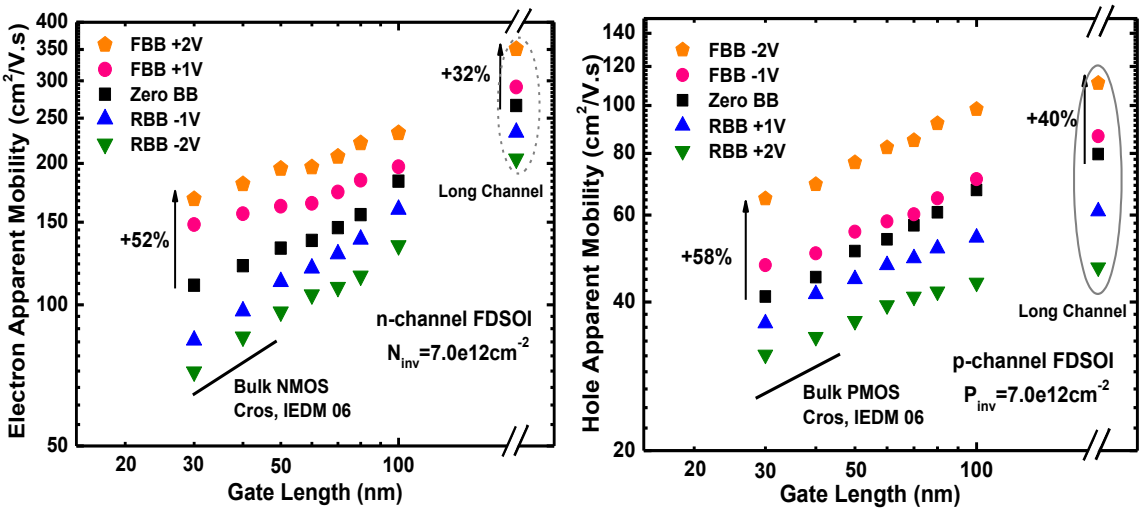

Figure 5.8, Extracted (left) electron and (right) hole apparent mobility vs. L_g in UTBB FD-SOI MOSFETs, under different back bias. Solid lines show apparent mobility degradation trends in planar bulk MOSFETs from [14].

Fig. 5.9 compares extracted values of carrier-mobility enhancement due to bending-induced S_{xx} against simulations, for different back biases. Referenced to the case of zero back bias (ZBB), FBB increases mobility enhancement while RBB reduces it. This can be explained by the fact that stress reduces inter-valley (electron) or inter-sub-band (hole) scatterings, but this benefit can be countered by enhanced sub-band reoccupation due to increasing quantum confinement [15]. Under FBB, due to the reduced quantum confinement at a certain inversion charge concentration, carriers distribute more equally among different sub-bands; strain is effective to induce large carrier re-populations towards the sub-band with lighter effective mass. Under RBB, the enhanced quantum confinement causes carriers re-populate into the lighter-mass sub-band (however, the mobility is still low due to the increased transverse electric field), and hence provides marginal room for mobility boosting by strain.

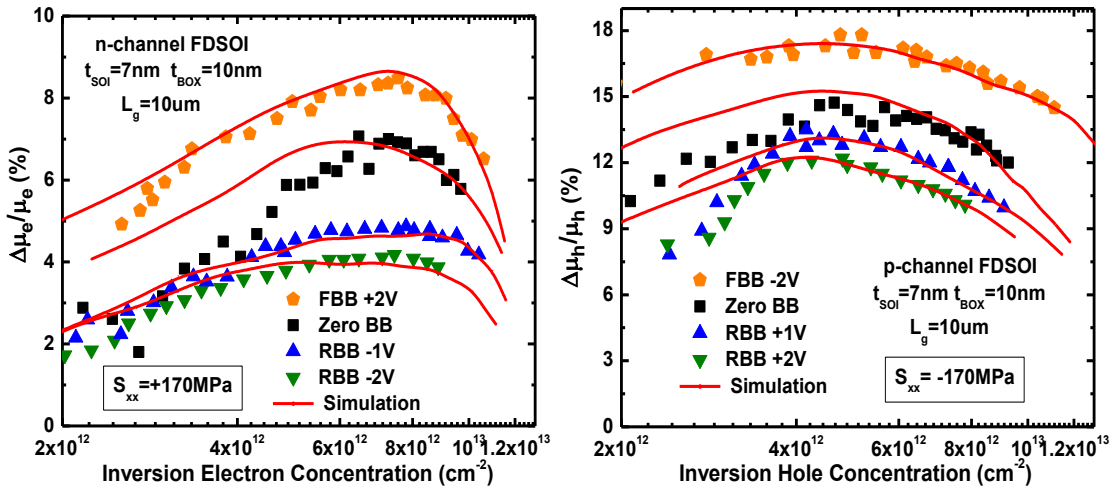

Figure 5.9, Measured and simulated (left) electron and (right) hole mobility enhancement for longitudinal, wafer-bending induced stress, under different back bias.

To maintain good electrostatic integrity, t_{SOI} should be scaled down in proportion to L_g [3, 4], so it is important to examine the impact of t_{SOI} scaling on the effectiveness of back biasing for modulating the carrier mobility and stress-induced mobility enhancement. Using the calibrated simulator [12, 15, 16], the unstrained μ_e and μ_h values are calculated for different t_{SOI} values and plotted for various back biases in Fig. 5.10. For electrons, FBB (RBB) provides +30% (-20%) μ_e enhancement (reduction) for a back bias magnitude of 2V; and the effectiveness of back biasing is not sensitive to t_{SOI} scaling. For holes, μ_h modulation is large (-40% for RBB and +100% for FBB) only for thick t_{SOI}, and is dramatically reduced at t_{SOI}=4nm due to the relatively large inversion-layer thickness for holes, which reduces the ability of back biasing to modulate the transverse electric field for an extremely thin body structure [4].

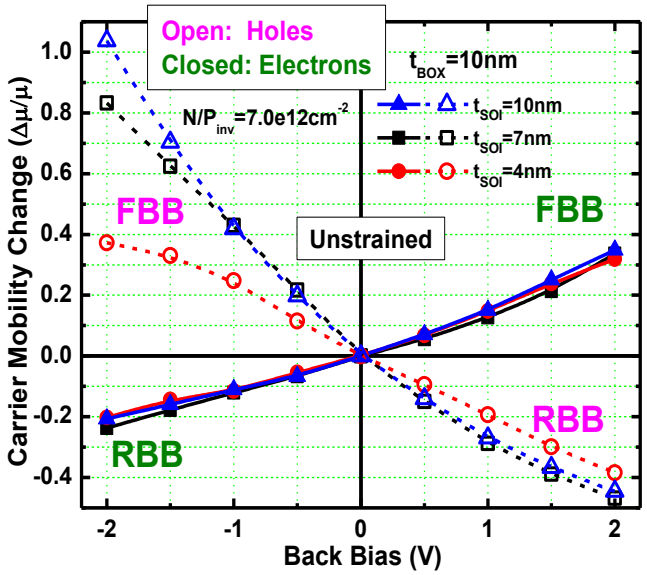

Figure 5.10, Electron (left) and hole (right) mobility enhancement under biaxial wafer bending strain. Data extracted from measurements of FinFETs with L_g = 10 um, with <100> and <110> fins. Simulated mobility curves are also shown.

Fig. 5.11 shows calculated piezo-resistance coefficients for longitudinal ($\prod_{xx}$) and vertical ($\prod_{zz}$) stress, which are the most important stress components for high-volume manufacturing of strained-silicon CMOS transistors [17, 18]. For electrons, both $\prod_{xx}$ and $\prod_{zz}$ are enhanced with FBB and are degraded as t_{SOI} decreases, due to the fact that increased-confinement-induced inter-valley scattering suppression and average transport effective mass (m_{xx}) reduction tend to mitigate the benefit of stress for μ_e enhancement. For holes, both $\prod_{xx}$ and $\prod_{zz}$ are enhanced with FBB due to more inter-sub-band scattering suppression by stress under FBB. As t_{SOI} decreases to 4nm, $\prod_{xx}$ and $\prod_{zz}$ are enhanced due to hole reoccupation into the more stress-sensitive heavy hole (HH) sub-bands in the case of very strong quantum confinement [15, 19], as summarized in Table 5.1.

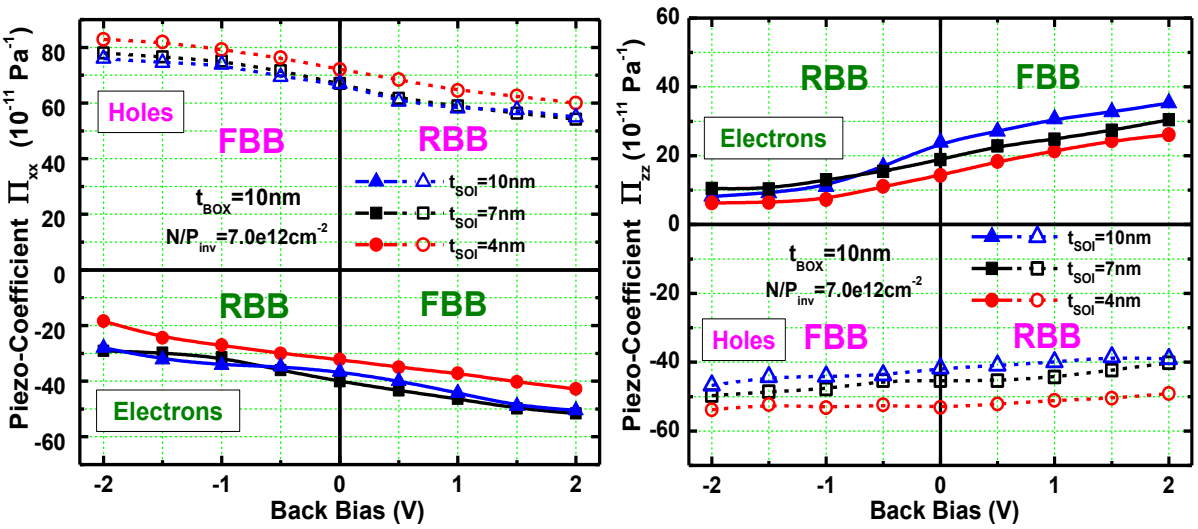

Figure 5.11, Simulated Piezo-resistance coefficients of (left) longitudinal stress and (right) vertical stress vs. back bias in UTBB FD-SOI MOSFETs, for different t_{SOI}.

		FBB	t_{SOI} Scaling	Stress becomes more (+) or less (-) effective in:
	Π_{xx}	++	-	▪ Reducing Inter-valley scatterings ▪ Reducing overall m_{xx} due to subband reoccupation
	Π_{zz}	++	-	
	Π_{xx}	+	+	▪ Reducing Inter-subband scatterings ▪ Hole reoccupation to HH, which has more pronounced m_{xx} reduction from stress
	Π_{zz}	+	+	

Table 5.1, Elucidation of FBB and t_{SOI} scaling's impacts on Π_{xx} and Π_{zz}.

5.3.2 Back Biasing Modulation of ON-state Carrier Velocity

Fig. 5.12 plots the ON-state carrier velocities extracted from measurements of short-channel devices [20] with different back biases. FBB-induced enhancement for ON-state carrier velocity is smaller than that for low-field mobility, since the carrier velocity is more closely related to m_{xx} due to ballistic transport [6, 7]. FBB causes no change (for holes) or even an increase (for electron) in m_{xx}, which mitigates the benefit of improved low-field mobility. Fig. 5.13 shows the correlation between improvements in ON-state current (I_{ON}) and linear-region current ($I_{d,lin}$) due to FBB and bending-induced stress. The lower enhancement for $I_{d,lin}$ (than for mobility) is attributed to R_{sd}, which is much less sensitive to stress or FBB, as compared to channel mobility. The correlation ratio (which indicates the relationship between carrier mobility and velocity) is similar for enhancement via FBB and enhancement via stress.

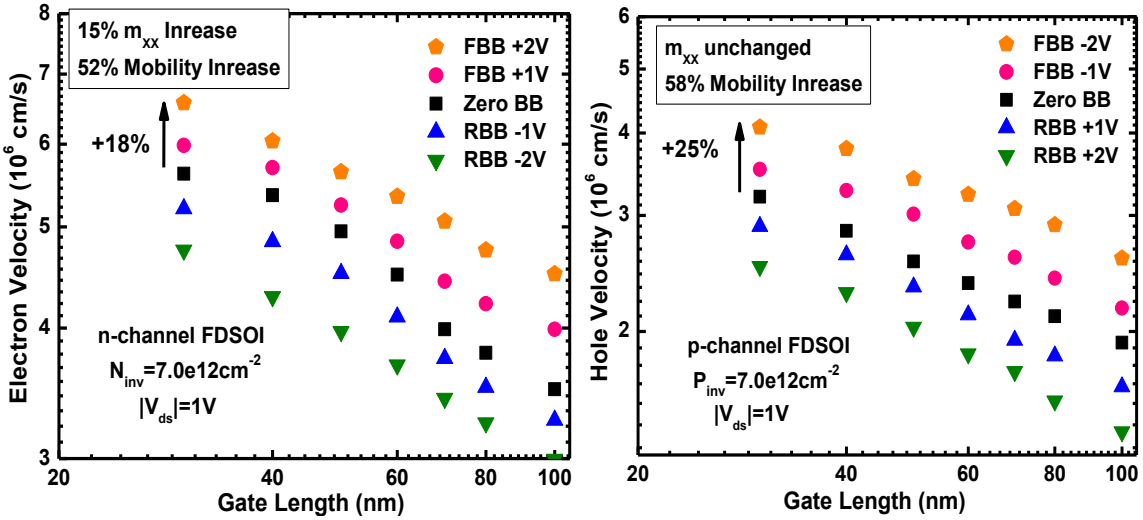

Figure 5.12, Extracted (left) electron and (right) hole ON-state velocity vs. L_g from short-channel UTBB FD-SOI MOSFETs measurement, under different back bias.

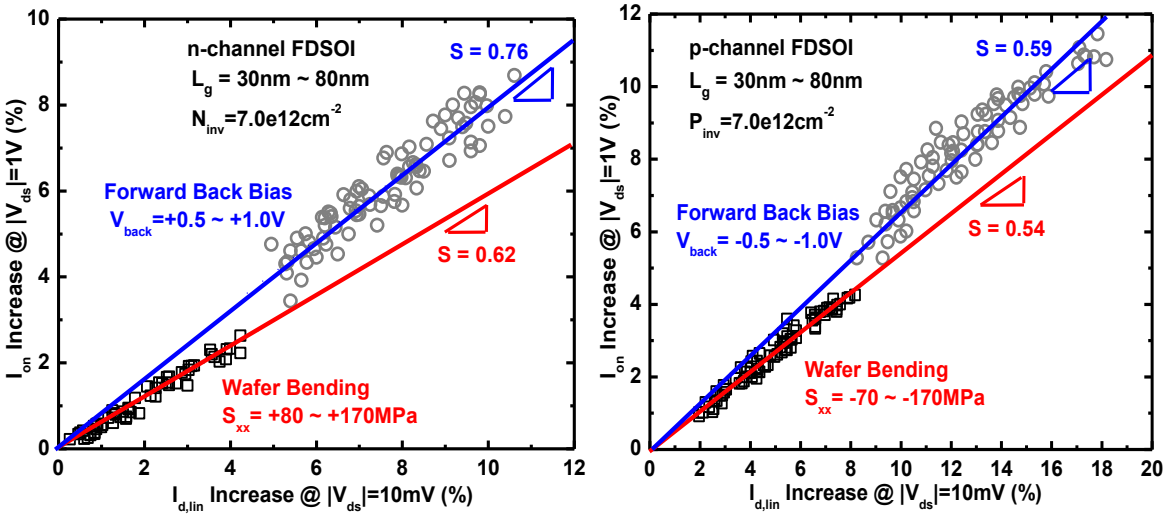

Figure 5.13, Measured relationship between I_{on} increase and $I_{d,lin}$ increase induced by wafer bending stress and FBB, for short-channel (left) n-type and (right) p-type UTBB FD-SOI MOSFETs.

5.3.3 Back Biasing Modulation of Carrier Fluctuations

The impact of back biasing on LFN is shown in Fig. 5.14. Improvement with FBB is clearly seen. The normalized I_{ds} noise spectral density in Fig. 5.15 shows that the improvement is larger at lower gate voltage, which suggests that the LFN is dominated by carrier concentration fluctuations [21, 22]; by moving the inversion-layer charge centroid further from the top gate dielectric interface using FBB, carrier trapping/de-trapping can be suppressed.

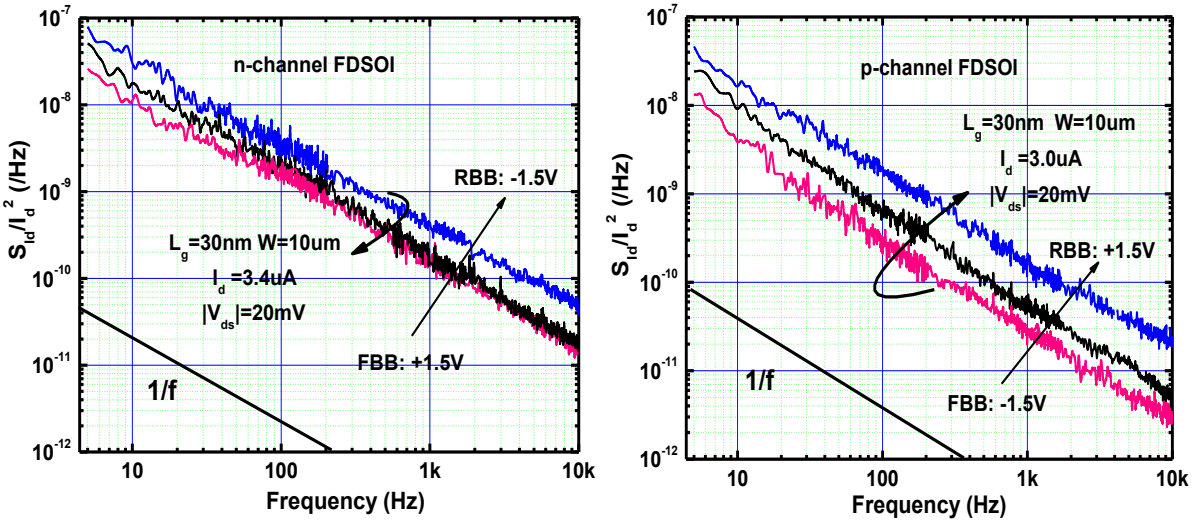

Figure 5.14, Measured I_{ds} noise spectral density for L_g=30nm (left) n-channel and (right) p-channel UTBB FD-SOI MOSFETs, under different back bias.

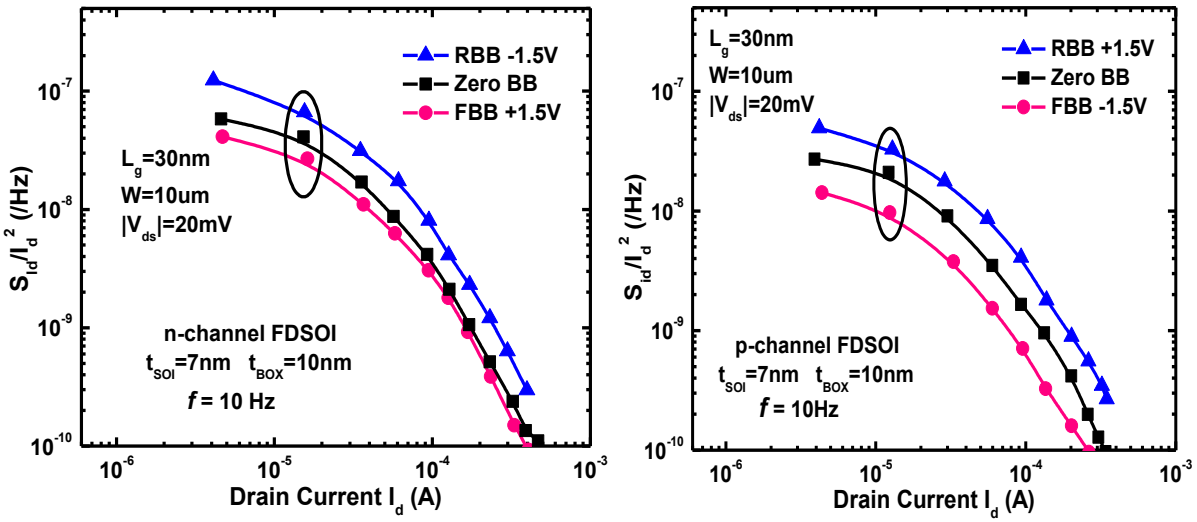

Figure 5.15, Normalized I_{ds} noise spectral density vs. I_{ds} at f=10Hz for (left) n-channel and (right) p-channel UTBB FD-SOI MOSFETs, under different back bias.

5.4 Summary

The threshold voltage of a UTBB FD-SOI MOSFET can be tuned more effectively with FBB than RBB, but this advantage diminishes as the SOI thickness is scaled down. GIDL current sets an upper limit for the RBB voltage. Forward back biasing slows degradation in mobility degradation with L_g scaling, increases stress-induced mobility enhancement, and reduces low-frequency noise. The correlation between enhancements in I_{ON} and $I_{d,lin}$ is similar for FBB as for stress. The impact of back biasing on carrier mobility modulation is maintained for n-channel (but is degraded for p-channel) UTBB FD-SOI FETs with t_{SOI} scaling.

5.5 References

[1] F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J-P. Noel, C. Fenouillet-Béranger, J-P. Mazellier, P. Perreau, T. Poiroux, Y. Morand, T. Morel, S. Allegret, V. Loup, S. Barnola, F. Martin, J-F. Damlencourt, I. Servin, M. Cassé, X. Garros, O. Rozeau, M-A. Jaud, G. Cibrario, J. Cluzel, A. Toffoli, F. Allain, R. Kies, D. Lafond, V. Delaye, C. Tabone, L. Tosti, L. Brévard, P. Gaud, V. Paruchuri, K.K. Bourdelle, W. Schwarzenbach, O. Bonnin, B-Y. Nguyen, B. Doris, F. Boeuf, T. Skotnicki, O. Faynot, "Low Leakage and Low Variability Ultr-Thin-Body and Buried Oxide (UT2B) SOI Technology for 20nm Low Power CMOS and Beyond," Symp. on VLSI Tech. Dig., 2010, pp.57-58.

[2]O. Faynot, F. Andrieu, O. Weber, C. Fenouillet-Beranger, P. Perreau, J. Mazurier, T. Benoist, O. Rozeau, T. Poiroux, M. Vinet, L. Grenouillet, J-P. Noel, N. Posseme, S. Barnola, F. Martin, C. Lapeyre, M. Cassé, X. Garros, M-A. Jaud, O. Thomas, G. Cibrario, L. Tosti, L. Brévard, C. Tabone, P. Gaud, S. Barraud, T. Ernst, S. Deleonibus, "Planar Fully Depleted SOI Technology: a powerful architecture for the 20nm node and beyond," IEDM Tech. Dig. 2010, pp.50-53.

[3]Q. Liu, A. Yagishita, N. Loubet, A. Khakifirooz, P. Kulkarni, T. Yamamoto, K. Cheng, M. Fujiwara, J. Cai, D. Dorman, S. Mehta, P. Khare, K. Yako, Y. Zhu, S. Mignot, S. Kanakasabapathy, S. Monfray, F. Boeuf, C. Koburger, H. Sunamura, S. Ponoth, A. Reznicek, B. Haran, A. Upham, R. Johnson, L. F. Edge, J. Kuss, T. Levin, N. Berliner, E. Leobandung, T. Skotnicki, M. Hane, H. Bu, K. Ishimaru, W. Kleemeier, M. Takayanagi, B. Doris, R. Sampson, "Ultra-Thin-Body and BOX (UTBB) Fully Depleted (FD) Device Integration for 22nm Node and Beyond," Symp. on VLSI Tech. Dig., 2010, pp.61-62.

[4]J.-P. Noel, O. Thomas, M.-A. Jaud, O. Weber, T. Poiroux, C. Fenouillet-Beranger, P. Rivallin, P. Scheiblin, F. Andrieu, M. Vinet, O. Rozeau, F. Boeuf, O. Faynot, A. Amara, IEEE Transactions on Electron Devices, vol.58, no.8, 2011, pp.2473-2482.

[5]T. Y. Chan, J. Chen, P. K. Ko, C. Hu, "The impact of gate-induced-drain-leakage on MOSFET scaling," IEDM Tech. Dig. 1987, pp.718-721.

[6]M.S. Lundstrom, "On the Mobility Versus Drain Current Relation for a Nanoscale MOSFET," IEEE Electron Device Letters, Vol.22, no.6, 2001, pp.293-295.

[7]A. Khakifirooz, D. A. Antoniadis, "Transistor Performance Scaling: The Role of Virtual Source Velocity and Its Mobility Dependence," IEDM Tech. Dig. 2006.

[8]T. Irisawa, K. Okano, T. Horiuchi, H. Itokawa, I. Mizushima, K. Usuda, T.Tezuka, N. Sugiyama, S. Takagi, "Electron Mobility and Short-Channel Device Characteristics of SOI FinFETs With Uniaxially Strained (110) Channels," IEEE Transactions on Electron Devices, Vol.56, no.8, 2009, pp.1651-1658.

[9] Z. Lu, N. Collaert, M. Aoulaiche, B. De Wachter, A. De Keersgieter, J. G. Fossum2, L. Altimime , M. Jurczak, "Realizing Super-Steep Subthreshold Slope with Conventional FDSOI CMOS at Low-Bias Voltages," IEDM Tech. Dig. 2010, pp.407-409.

[10] E. Ungersboeck, S. Dhar, G. Karlowatz, V. Sverdlov, H. Kosina, S. Selberherr, "The Effect of General Strain on the Band Structure and Electron Mobility of Silicon," IEEE Transactions on Electron Devices, vol.54, no.89, 2007, pp.2183-2190.

[11] K. Uchida, T. Krishnamohan, K.C. Saraswat, Y. Nishi, "Physical Mechanism of Electron Mobility Enhancement in Uniaxial Stressed MOSFETs and Impact of Uniaxial Stress Engineering in Ballistic Regime," IEDM Tech. Dig. 2005, pp.49-52.

[12] N. Xu, X. Sun, W. Xiong, C. R. Cleavelin, T.-J. King Liu, "MuGFET Carrier Mobility and Velocity: Impacts of Fin Aspect Ratio, Orientation and Stress," IEDM Tech. Dig. , 2010, pp. 194-197.

[13] C.-Y. Lu, K.-S. C.-Liao, P.-H. Tsai, T.-K. Wang, "Depth Profiling of Border Traps in MOSFET with High-κ Gate Dielectric by Charge-Pumping Technique," IEEE Electron Device Letters, vol. 27, no.10, 2006, pp.859-861.

[14] A. Cros et al., "Unexpected mobility degradation for very short devices : A new challenge for CMOS scaling," IEDM Tech. Dig. 2006

[15] N. Xu, F. Andrieu, J. Jeon, X. Sun, O. Weber, T. Poiroux, B.-Y. Nguyen, O. Faynot, T.-J. King Liu, "Stress-induced Performance Enhancement in Ultra-Thin-Body Fully Depleted SOI MOSFETs: Impacts of Scaling," Symp. on VLSI Tech. Dig., 2011, pp. 162–163.

[16] N. Xu, B. Ho, F. Andrieu, L. Smith, B.-Y. Nguyen, O. Weber, T. Poiroux, O. Faynot, T.-J. King Liu, "Carrier Mobility Enhancement via Strain Engineering in Future Thin-Body MOSFETs," IEEE Electron Device Letters, 33, 2012, pp.318-320.

[17] S. Mayuzumi, J. Wang, S. Yamakawa, Y. Tateshita, T. Hirano, M. Nakata, S. Yamaguchi, Y. Yamamoto, Y. Miyanami, I. Oshiyama, K. Tanaka, K. Tai, K. Ogawa, K. Kugimiya, Y. Nagahama, Y. Hagimoto, R. Yamamoto, S. Kanda, K. Nagano, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, S. Kadomura and N. Nagashima, "Extreme High-Performance n and p-MOSFETs Boosted by Dual-Metal/high-k Gate Demascene Process using Top-cut Dual Stress Liners on (100) Substrates," IEDM Tech. Dig., 2007, pp.293-296.

[18] S. E. Thompson, G. Sun, Y.S. Choi, T. Nishida, "Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap," Electron Devices, IEEE Transaction on, Vol. 53, no.5, 2006, pp. 1010-1020.

[19] K. Uchida, M. Saitoh, S. Kobayashi, "Carrier Transport and Stress Engineering in Advanced Nanoscale Transistors From (100) and (110) Transistors To Carbon Nanotube FETs and Beyond," IEDM Tech. Dig., 2008, pp.569-572.

[20] A. Lochtefeld, D. A. Antoniadis, "On Experimental Determination of Carrier Velocity in Deeply Scaled NMOS: How Close to the Thermal Limit," IEEE Electron Device Letters, Vol. 22, no. 2, 2001, pp. 95-97.

[21] J. Zhuge, L. Zhang, R. Wang, R. Huang, D.-W. Kim, D. Park, Y. Wang, "Random Telegraph Signal Noise in Gate-all-around Silicon Nanowire Transistors Featuring Coulomb-blockade Characteristics," Applied Physics Letters, 94, 083503, 2009.

[22] W. Feng, R. Hettiarachchi, Y. Lee, S. Sato, K. Kakushima, M. Sato, K. Fukuda, M. Niwa, K. Yamabe, K. Shiraishi, H. Iwai, K. Ohmori, "Fundamental Origin of Excellent Low-Noise Property in 3D Si-MOSFETs: Impact of Charge-Centroid in the Channel due to Quantum Effect on 1/*f* Noise," IEDM Tech. Dig. pp.630-633, 2011.

Chapter 6

Conclusion

Since the integrated circuit (IC) was invented in 1958, improvements in device performance and cost reduction have been successfully enabled by the steady miniaturization of the transistor (i.e., minimum pitch is reduced by a factor of 0.7 in every new technology generation). However, increasing OFF-state leakage and variation in transistor performance makes continuous planar bulk CMOS technology scaling to 22nm node and beyond extremely difficult. Advanced thin-body transistor structures which suppress short-channel effects more effectively than bulk MOSFET structure without the need for heavy channel doping, will be needed to overcome these challenges. Strained Silicon technology is widely used today to boost transistor drive current. Thus, the strain-induced performance enhancement to the thin-body transistors at aggressively scaled body thickness and channel length need to be studied comprehensively. For this reason, this dissertation investigates the effectiveness of different stress components as well as various stressor technologies into the performance enhancement of those thin-body transistors.

6.1 Contributions of This Work

This work contributes specifically to the following aspects: Understanding carrier mobility enhancement mechanisms by strain in various thin-body transistor architectures; study of strain-induced performance enhancement at aggressively scaled Silicon body thickness (t_{SOI}) and gate length (L_g); and investigation of process technology for maximizing the stress transfer efficiency.

Firstly, the Poisson-Schrödinger self-consistent simulator for Fully Depleted (FD) SOI MOSFET carrier sub-band structures and mobility calculations is developed. Then the strain-induced FD-SOI device carrier mobility enhancement is assessed with t_{SOI} scaling, for electrons and holes. It is found that mobility enhancement in FD-SOI MOSFETs diminishes with scaling t_{SOI} below 5nm for electrons but maintains for holes, which results from the different physical mechanisms between electrons and holes. After decoupling the Source/Drain (S/D) series resistance impact, the benefits of stress for boosting apparent mobility and limiting velocity are found to be maintained with L_g scaling [1].

The two-dimensional (2-D) Poisson-Schrödinger self-consistent solver is developed to simulate the Multiple-Gate MOSFET (MuGFET) structure. The effects of the MuGFET fin aspect ratio, crystalline orientation and stress design for improving performance are studied [2]. <110>-oriented fins (with (110) sidewall surfaces) are more sensitive to strain than <100>-oriented fins (with (100) sidewall surfaces). Uniaxial stressor technology can provide the highest carrier mobility enhancement at a given stress value. For <110> channels, electron mobility is higher for the Tri-Gate MOSFET than that for FinFET for unstrained or low-strain channels; at higher strain, the two device architectures are comparable in electron mobility values. Hole mobility is lower in the FinFET than in the Tri-Gate MOSFET until the stress applied reaches ~600MPa. Among the uniaxial stressor technologies, strained Contact-Etch-Stop-Liner (sCESL) is not as effective as S/D stressors for inducing stress within the channel region of a FinFET. Bulk FinFETs with strained-S/D regions are projected to outperform SOI FinFETs with strained-S/D regions. For FinFET structures with S/D stressors, although a gate-last process can further increase longitudinal stress (S_{xx}), its benefit for boosting carrier mobility will be marginal in future technology nodes, due to the largely reduced vertical stress (S_{zz}) [3].

Next, stress-induced enhancements in electron and hole mobilities are studied comprehensively for FD-SOI MOSFET and FinFET structures with high-κ/metal gate stacks [4]. New scattering models, (i.e. remote Coulomb and surface optical phonon scatterings) are included to account for the structural differences between the two devices. Simulation data calibrated to measurement are presented to evaluate the effectiveness of strain for boosting thin-body MOSFET performance with aggressively scaled body thickness. It is found that the advantage of the high electron mobility (100) surface for the FD-SOI MOSFET will diminish, whereas the advantage of the high hole mobility (110) surfaces for the FinFET will be maintained with scaling.

Lastly, the performance modulation of back bias on ultra-thin-BOX FD-SOI MOSFET is investigated, for long-channel as well as short-channel devices [5]. The threshold voltage of a FD-SOI MOSFET can be tuned more effectively with Forward Back Biasing (FBB) than Reverse Back Biasing (RBB), but this advantage diminishes as the t_{SOI} is scaled down. FBB slows degradation in mobility degradation with L_g scaling, increases stress-induced mobility enhancement, and reduces low-frequency noise. The correlation between enhancements in ON-state and linear-region current is similar for FBB as for stress. The impact of back biasing on carrier mobility modulation is maintained for n-channel (but is degraded for p-channel) FD-SOI FETs with t_{SOI} scaling.

6.2 Future Directions

III-V semiconductors are promising candidates as the future MOSFET channel materials, because of their high electron [6] and hole [7] mobilities, which promises high enough drive current at low operation voltage. On the other hand, to maintain good electrostatic integrity, III-V MOSFET also requires thin-body device structure. Thus, comprehensive studies should be performed on the carrier band structures and mobilities from those high mobility channels. 8×8 k.p perturbation theories can capture III-V material band structure properties by including the

coupling between conduction and valence bands, due to smaller bandgap values are usually found in III-V semiconductors, and turn out to be in good accuracy within the interested energy range compared to tight binding (TB) results [8], as shown in Fig.6.1. New scattering mechanisms, such as polar phonon scatterings [9] and alloy-disorder scattering need to be taken into account, which is different compared to the Silicon case.

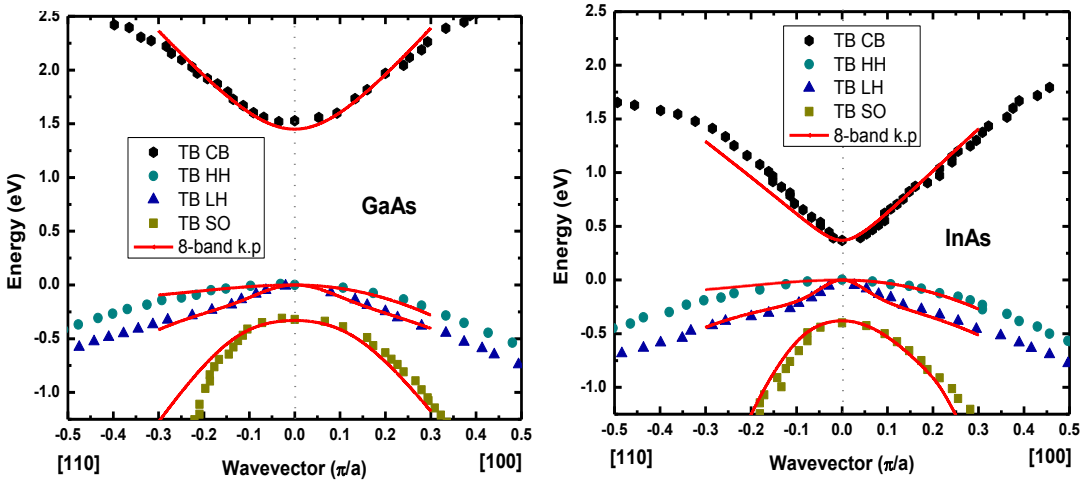

Figure 6.1, Calculated III-V material band structures using 8×8 k·p approach, compared to TB results in [8].

Another interesting study is to introduce strain from IC process to apply on those high mobility channels. Due to the lattice spacing is quite different to Silicon, and the process integration complexity, epitaxy SiGe S/D may not be applicable to P-channel III-V MOSFET. Also, because of the production cost concern, III-V MOSFETs are ideally to be fabricated on Silicon bulk substrate [10], as shown in Fig.6.2. Hence, the intrinsic strain induced by the lattice mismatch from the substrate to the channel will be important to the carrier mobilities. These aforementioned issues require further careful considerations and studies.

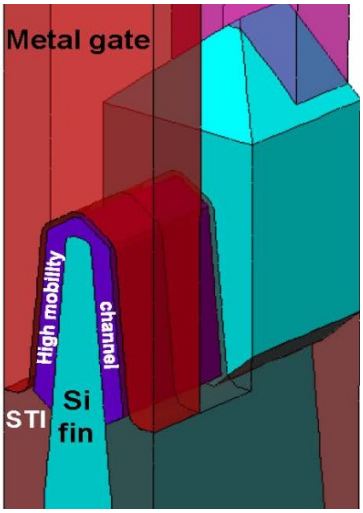

Figure 6.2, Schematic view of fabricating high mobility channel materials on a Silicon fin, from [10].

6.3 References

[1] N. Xu, F. Andrieu, J. Jeon, X. Sun, O. Weber, T. Poiroux, B.-Y. Nguyen, O. Faynot and T.-J. King Liu, "Stress-induced Performance Enhancement in Ultra-Thin-Body Fully Depleted SOI MOSFETs: Impacts of Scaling," Symp. on VLSI Tech., Dig., 2011, p.162-163.

[2] N. Xu, X. Sun, W. Xiong, C. R. Cleavelin and T.-J. King Liu, "MuGFET Carrier Mobility and Velocity: the Impacts of Fin Aspect Ratio, Orientation and Stress," IEDM Tech. Dig., 2010, p.194-197.

[3] N. Xu, B. Ho, M. Choi, V. Moroz, T.-J. King Liu, "Effectiveness of Stressors in Aggressively Scaled FinFETs," to appear in IEEE Transactions on Electron Devices, vol.59, Issue 6, 2012.

[4] N. Xu, B. Ho, F. Andrieu, L. Smith, B.-Y. Nguyen, O. Weber, T. Poiroux, O. Faynot, T.-J. King Liu, "Carrier Mobility Enhancement via Strain Engineering in Future Thin-Body MOSFETs," IEEE Electron Device Letters, vol. 33, issue 3, 2012, pp.318-320.

[5] N. Xu, F. Andrieu, B. Ho, B.-Y. Nguyen, O. Weber, C. Mazure, O. Faynot, T. Poiroux and T.-J. King Liu, "Impact of Back Biasing on Carrier Transport in Ultra-Thin-Body and BOX (UTBB) Fully Depleted SOI MOSFETs," accepted, to be presented at Sym. on VLSI Technology, 2012.

[6] Y.Q. Wu, M. Xu, R.S Wang, O. Koybasi, P.D. Ye, "High Performance Deep-Submicron Inversion-Mode InGaAs MOSFETs with maximum Gm exceeding 1.1 mS/um: New HBr Pretreatment and Channel Engineering," IEDM Tech. Dig., pp.323-326, 2009.

[7] A. Nainani, S. Raghunathan, D. Witte, M. Kobayashi, T. Irisawa, T. Krishnamohan, K. Sawaswat, "Engineering of Strained III-V Heterostructures for High Hole Mobility," IEDM Tech. Dig., pp.857-860, 2009.

[8] G. Klimeck, R. Bowen, T. Boykin, T. Cwik, "sp3s* Tight-binding parameters for transport simulations in compound semiconductors," Superlattice and Microstructures, vol.27, 77, 2000.

[9] O. Katz, A. Horn, G. Bahir, J. Salzman, "Electron Mobility in an AlGaN/GaN Two-Dimensional Electron Gas I - Carrier Concentration Dependent Mobility," IEEE Transactions on Electron Devices, vol.50, no.10, pp.2002-2007, 2003

[10] V. Moroz, M. Choi, "Strain Scaling and modeling for FETs," ECS Transactions, vol.33, no.6, 2010, pp.21-32.