On-chip Benchmarking and Calibration without External References

Cheol-Woong Lee

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2012-7
http://www.eecs.berkeley.edu/Pubs/TechRpts/2012/EECS-2012-7.html

January 7, 2012

Acknowledgement

To my father, Choon-Hwan Lee and my mother, Myoung-Sun Kim, for giving birth to me.

On-chip Benchmarking and Calibration without External References

by

Cheol-Woong Lee

A dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Engineering

in

Electrical Engineering and Computer Sciences

in the

GRADUATE DIVISION

of the

UNIVERSITY OF CALIFORNIA, BERKELEY

Committee in charge:

Professor Ali M. Niknejad, Chair
Professor Paul R. Gray
Professor Paul K. Wright

Fall 2011

On-chip Benchmarking and Calibration without External References

by

Cheol-Woong Lee

Abstract

On-chip Benchmarking and Calibration without External References

By

Cheol-Woong Lee

Doctor of Engineering in Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Ali M. Niknejad, Chair

The strong market demand for mobile applications such as iPhone makes value on the form factor of the mobile devices. The form factor means how much we can integrate many functions in a given size of the mobile devices. The external component size is almost comparable to a chip size so that elimination of external component is crucial to the success of mobile devices in addition to the cost issues of the external components. External reference resistors are often used as the standard for calibrating voltage sources, current sources, and other component values within a circuit. Often these calibrations occur at a factory, but may also occur on an electronic device as it is used. However, external reference resistors consume area and cost and it is desirable to eliminate them.

This work introduces a new way to calibrate on-chip resistance and capacitance without the external reference resistors. An integrated circuit includes a benchmarking circuitry and a tunable circuitry. The benchmarking circuit includes a target component and an internal reference component. The internal reference component exhibits a lower sensitivity to the changes in test conditions than the target component. Benchmarking Metric Measurement Module (BMMM) measures benchmarking metrics for the internal reference component and the target component. A benchmark value is calculated based on the benchmarking metrics. The novelty of this work is the powerful way to cancel the parasitic and systemic errors caused by operational amplifiers in RC tuner circuitry. This technique is broadly applicable to any RF and analog circuits that need the calibration of tunable circuit elements without external references.

To my father, Choon-Hwan Lee and my mother, Myoung-Sun Kim, for giving birth to me.

Contents

Figures

Tables

Acknowledgements

I entered Ph.D. program in EECS department at UC Berkeley in Fall 1997 and finally I filed my doctoral dissertation in Fall 2011. It took me 14 years to finish my long journey to get doctoral degree in EECS department at UC Berkeley! I had never imagined it would have taken me 14 years when I entered UC Berkeley. What made me take such a long time to complete my work toward a doctoral degree?

I joined Professor Paul R. Gray's research group in Summer 1999 and I passed my preliminary examination with score 8 of 10 in Spring 2000 and I co-received the best paper award in ISSCC 2001, which were pretty good initial outcomes in Ph.D. program. I had my ambition to unify my knowledge in both analog circuit design and digital communication system. I came up with a big idea, 'Parallel Path Receiver Architecture,' which required the design of broadband LNA, mixers, baseband filters, ADC and multiple frequency synthesizers, and a digital signal processor to combine parallel channels.

My critical mistake originated from my underestimation of project work load. I passed my qualifying examination in Spring 2004, but my design progress was still in the system level simulation without circuit level implementation in detail. Because I had many building blocks to design, my design progress in each block was very slow. Right after I passed my qualifying examination, I realized that my design task was overwhelming but I could not stop my research because my emotion did not want to give it up. I spent additional 3 years until 2007 but I found that there was paradox in Parallel Path Receiver Architecture. The cross-coupling issues between parallel channels were very challenging so that the proposed architecture lost benefit from parallel channels. Finally I decided to give up my research work and joined Qualcomm in 2008.

Since I joined Qualcomm, I learned how to define my design task within a reasonable work load. I tried to develop my new invention idea and actually filed several patents to claim my inventions and demonstrated my new idea through circuit design and measurement. Following that, I learned how to focus my energy through efficient time management and found a better way to propose a new idea to implement an experimental prototype within a reasonable amount of time and efforts.

In 2010, Professor Paul R. Gray and Ali Niknejad helped me to get a chance to file my doctoral dissertation and I had commencement with my family in May 2011 and finally I filed my dissertation in Fall 2011. I really appreciate the help from Professor Paul R. Gray and Ali Niknejad to make it work out finally. Even though I spent 14 years to get a doctoral degree, it was certainly meaningful experience to learn three valuable lessons from trial and error.

The first lesson is that time management is the most valuable skill set beyond any design skill sets.

The second lesson is that whenever I fail in something, I had better accept the failure as soon as possible.

The third lesson is that there is always a door open if I am willing to get over the failure.

1 Introduction

The strong market demand for mobile applications such as iPhone makes value on the form factor of the mobile devices. The form factor means how much we can integrate many functions in a given size of the mobile devices. The external component size is almost comparable to a chip size so that elimination of external component is crucial to the success of mobile devices in addition to the cost issues of the external components. External reference resistors are often used as the standard for calibrating voltage sources, current sources, and other component values within a circuit. Often these calibrations occur at a factory, but may also occur on an electronic device as it is used.

Examples of components external to an integrated circuit include external resistors and capacitors. The calibration of these circuit elements often occurs in a factory environment. But as conditions change during the lifetime of a mobile communication device, it is desirable to recalibrate many circuit elements as the mobile communication device is being used by the consumer. In some applications, it is acceptable to include external reference components with the electronic device for use as calibration standards. But, as mobile communication devices with increased functionality and smaller size are designed to meet consumer demand, it is becoming increasingly difficult to include external reference components. As the level of circuit integration increases to accommodate an increasing number of circuit functions in a smaller size, external components now occupy an amount of space that is comparable to the size of many of the integrated circuits of a mobile communication device. In addition, external components are a significant component of the cost of the circuitry of a mobile communications device. Thus, electronic circuitry with a reduced number of external reference components is desirable.

This work introduces a new way to calibrate on-chip resistance and capacitance without the external reference resistors. An integrated circuit includes a benchmarking circuitry and a tunable circuitry. The benchmarking circuit includes a target component and an internal reference component. The internal reference component exhibits a lower sensitivity to the changes in test conditions than the target component. Benchmarking Metric Measurement Module (BMMM) measures benchmarking metrics for the internal reference component and the target component. A benchmark value is calculated based on the benchmarking metrics. The novelty of this work is the powerful way to cancel the parasitic and systemic errors caused by operational amplifiers in RC tuner circuitry. This technique is broadly applicable to any RF and analog circuits that need the calibration of tunable circuit elements without external references.

2 Background

2.1 Component Variation

There are no perfect components which have no variation. Basically the circuit design should be robust against the component variation. In order to quantify the impact of component variation, we typically assume Gaussian distribution for component variation.

2.1.1 Gaussian Distribution

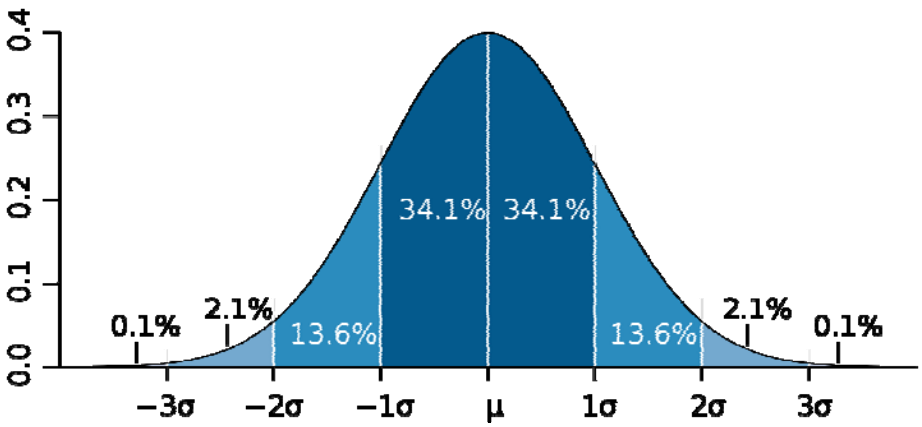

Figure 2-1 Normalized Gaussian distribution

Figure 2-1 shows normalized Gaussian distribution. 68.26% of samples belong to the component variation of 1σ, and 95.46% of samples belong to the component variation of 2σ, and 99.74% of samples belong to the component variation of 3σ [3].

2.1.2 Yield

External components or on-chip components at least requires 3σ yield performance. At most 0.26% of samples are acceptable to be out of 3σ range. Through pass/fail yield test, we remove the samples which were out of 3σ range and we deliver customers the qualified samples which meet the design specification within 3σ range. Typically when we get external components, they are almost always within 3σ range because the vendors of the external components had already excluded failed components which are out of 3σ range.

2.2 External References

System-on-chip (SOC) solutions may require external references such as external crystal oscillators and external precision resistors.

2.2.1 External Crystal Oscillators

External crystal oscillator is a modern, cost-effective device capable of realizing frequency stabilities of a few parts in 10^8 over a wide temperature range in a small size [4]-[11]. Most of system-on-chip (SOC) solutions require the external crystal oscillators because of the stringent requirement of PLL design specifications. There were several trials to replace external crystal oscillators by on-chip clock references but most of them were not so successful so far.

2.2.2 External Precision Resistors

The external precision resistors have been successfully incorporated into system-on-chip (SOC) solutions so far. Recently mobile application made value on the form factor of mobile devices so that they drive a new momentum to exclude external components which are comparable to the size of the SOC itself. The external precision resistors were useful for R tuner, voltage reference and current reference generation. The elimination of the external precision resistors may cause high challenge in generating on-chip voltage and current references and calibration of on-chip resistance and capacitance.

2.2.3 External Constant Current Source

At the time of factory test and calibration, an external constant current source may be used to calibrate on-chip resistance by measuring the potential across on-chip resistance after the external constant current source is applied. However, this external constant current source is only available during test time period and may not be repeated during the real time operation of mobile devices. On-chip resistors can be tuned using the external constant current source, but temperature dependency cannot be tuned because it is one time calibration during factory test time. Also it increases the factory test time.

2.3 Internal References

System-on-chip (SOC) solution especially mobile applications made value on the form factor of the mobile devices so that the elimination of external references is important. Instead of external references, we may substitute internal references for the external references.

2.3.1 On-chip MOM capacitors

MOM capacitors are highly linear but highly sensitive to the process variations. MOM capacitors need to be tuned, but may not be used as an internal reference.

2.3.2 On-chip MOS capacitors

MOS capacitors are the accumulation mode varactors. The oxide thickness is well controlled relatively compared with Metal-to-Metal gap thickness. The oxide thickness is critical to the performance of transistors so that process foundry invested more budget and research rather than Metal-to-Metal gap thickness control. Metal lines are typically used for routing so that the accurate control of Metal-to-Metal gap thickness is not critical as the oxide thickness between the gate and channel of a transistor or varactor. MOS capacitors may be useful as an internal reference component if the variation of MOS capacitance is acceptable for applications.

2.3.3 On-chip Polysilicon resistors

Polysilicon resistors are highly sensitive to the process variations. Polysilicon resistors need to be tuned, but may not be used as an internal reference.

2.3.4 On-chip Inductors

The area for on-chip inductors for a given inductance is almost fixed regardless of process technologies. The lithography technology is highly accurate so that the dimension of on-chip inductors is almost insensitive to the process variations. The inductor size can be reduced significantly if the inductor is operated at several tens of GHz frequency. The parasitic capacitance under the inductor structure may be sensitive to the process variations, but the DC inductance value of the inductor would be insensitive to process variations [35]. The DC inductance of on-chip inductor may be useful as an internal reference component.

2.4 Existing Research without External References

Analog circuits incorporate voltage and current references extensively. Such references are desired to be less sensitive to supply voltage, temperature and process parameters or have well-defined temperature dependence. Typically such references require on-chip resistance, which is tuned by an external reference resistor. There have been several approaches to eliminate on-chip resistance so that they do not need external reference resistors [18-29].

2.4.1 Bandgap Voltage Reference Generation without Resistor

Bandgap voltage references [12-19] are very important building blocks in a variety of analog and mixed signal integrated circuits. With the negative and positive temperature coefficients, bandgap voltage reference has a nominally zero temperature coefficient. Although bandgap references have been widely used since their invention [12-13], the sub-micron CMOS processes have faced new issues. The reduction of the minimum feature size of MOS transistors also reduces the breakdown voltages, thus making it mandatory to reduce supply voltages. As a result, several bandgap circuits are working with supply voltages near or below 1 V [14-17].

Bandgap voltage references add the forward bias voltage across a pn diode with a voltage that is proportional to absolute temperature (PTAT) to produce temperature-independent voltage reference. In a typical CMOS process technology, models for the resistors may not be reliable and the area of such resistors is increased because silicide reduces the sheet resistance of the polysilicon and diffusion layers. Typical bandgap circuits use on-chip resistors, which are sensitive to the process corners in sub-micron CMOS process technology. The more area requirement of the resistors increases not only cost but also substrate noise coupling. There were some approaches to remove on-chip resistors replaced by ratioed transistors [18-19].

2.4.2 Current Reference Generation without Resistor

Current reference as an essential block in analog circuits is needed in many analog signal processing applications such as operational amplifier and data converter bias circuits. Reference currents are often implemented by applying a bandgap voltage reference across a resistor by means of an additional voltage to current converter [20].

The main problem corresponding to this method concerns the used resistor on chip. On-chip resistors are typically highly process-dependent, while off-chip resistors are not suitable due to cost and area considerations. Replacing resistor with its switched capacitor equivalent requires a separate frequency clock source and on-chip capacitors that leads to complexity and large area. Added digital noise to the circuit is another disadvantage of the switched capacitor method [21].
A current reference with low temperature and supply sensitivity and without any external reference resistor was developed [23-27]. The circuit is based on a bandgap reference voltage and a CMOS circuit similar to a beta multiplier. An NMOS transistor in triode region has been used in place of a resistor in conventional beta multiplier to achieve a current which has a negative temperature coefficient. The bandgap reference voltage has a positive temperature coefficient to cancel the negative temperature coefficient of the beta multiplier. However, the

required clock source and on-chip capacitors tend to result in more complexity and large silicon area. Moreover, the impact of the clocking noise on the reference current circuit is another issue and the output current is still dependent on the oxide thickness variation.

Recently there were some approaches to propose an area efficient CMOS current reference circuit based on the sum of a positive temperature coefficient (PTC) current generator and a negative temperature coefficient (NTC) current generator. The scheme does not require the use of on-chip resistors or amplifiers. Moreover, since the transistors in this design are all operated in strong-inversion, it is less sensitive to process and temperature variations compared to sub-threshold operation. The temperature coefficient is 170 ppm/^{o}C, which is less sensitive to temperature. However, the average current is 10uA and the σ is 0.43uA. 3σ is 1.28uA. The max-to-min variation of the current is 25.6%, which is still sensitive to the process variation. [22]

3 Theory of Benchmarking

3.1 Motivation

External reference resistors are often used as the standard for calibrating voltage sources, current sources, and other elements within a circuit. Examples of components external to an integrated circuit include external resistors and capacitors. The calibration of these circuit elements often occurs in a factory environment. But as conditions change during the lifetime of a mobile communication device, it is desirable to recalibrate many circuit elements as the mobile communication device is being used by the consumer. In some applications, it is acceptable to include external reference components with the electronic device for use as calibration standards. But, as mobile communication devices with increased functionality and smaller size are designed to meet consumer demand, it is becoming increasingly difficult to include external reference components. As the level of circuit integration increases to accommodate an increasing number of circuit functions in a smaller size, external components now occupy an amount of space that is comparable to the size of many of the integrated circuits of a mobile communication device. In addition, external components are a significant component of the cost of the circuitry of a mobile communications device. Thus, electronic circuitry with a reduced number of external reference components is desirable.

3.2 Internal Reference Component

Changes in conditions include process, voltage, and temperature (PVT) variations that impact the performance characteristics of electrical components (e.g. resistors and capacitors) of the IC. An example of a process variation is the variation in a manufacturing process. For example, a capacitor may be specified as part of IC, but due to manufacturing process variations the specified capacitor of each manufactured IC may exhibit a slightly different capacitance. Different components may be more or less sensitive to PVT variations. In one example, an IC may employ Metal-Oxide-Metal (MOM) capacitors or Metal Oxide on Silicon (MOS) capacitors. MOS capacitors exhibit relatively low sensitivity to process and temperature variation in a typical CMOS process technology.

Process	Typical	Fast	Fast	Slow	Slow
Temperature	55C	110C	-30C	110C	-30C
MOSCAP	0%	+4%	+4%	-4%	-4%
MOMCAP	0%	-15%	-15%	+15%	+15%

Table 3-1 Example of MOSCAP and MOMCAP variation

Table 3-1 illustrates a comparison between the percentage changes in capacitance from typical test conditions of both a MOS capacitor and a MOM capacitor due to both process and temperature variation. Columns 2-6 of Table 3-1 represent five sets of test conditions under which the capacitance of both a MOS and MOM capacitor are measured. In this example, the impact of manufacturing process variation is captured by choosing test components from a group of manufactured components. The "typical" test capacitors are selected such that they exhibit a capacitance value that is typical of the group. The "fast" test scenario captures the process condition where the capacitance value of the MOM capacitors is at a minimum, the capacitance value of the MOS capacitors is at a maximum, and the resistance value of the P+ polysilicon (PP) resistors of benchmarking circuitry is at a minimum. The "slow" test scenario captures the process condition where the capacitance value of the MOM capacitors is at a maximum, the capacitance value of the MOS capacitors is at a minimum, and the resistance value of the P+ polysilicon (PP) resistors of benchmarking circuitry is at a maximum. The second row of Table 3-1 represents the temperature condition during each test. The third and fourth rows illustrate the capacitance values for each test for MOS and MOM capacitors, respectively. In this example, MOS capacitors exhibit only 8% variation (max-min), in capacitance over a range of process and temperature conditions, whereas MOM capacitors exhibit 30% variation (max-min) in capacitance over the same range of test conditions.

But, MOS capacitors also exhibit poor linearity relative to MOM capacitors over a range of operating frequencies present on an IC. MOM capacitors may be used as part of a tunable circuit element within the IC to obtain the advantage of their better linearity. To mitigate their relatively high sensitivity to changes in test conditions, the MOM capacitors are benchmarked to MOS capacitors present on the IC. The benchmarking of the MOM capacitors to the MOS capacitors results in a benchmark value useable to calibrate a tunable circuit element on the IC that includes MOM capacitors, and thus compensate for changes in performance of the MOM capacitors due to changes in test conditions.

An Integrated Circuit (IC) includes an internal reference component, a target component, and a tunable circuit element. The internal reference component exhibits a lower sensitivity to changes in conditions (e.g. process, temperature, and voltage variations) than the target component. Because of its lower sensitivity, the internal reference component may be used to benchmark the target component. A benchmark value is calculated to characterize a change in performance of the target component with reference to the relatively stable internal reference component.

3.3 Benchmarking Metric Measurement Module

The internal reference component and the target component are present within a benchmarking circuit. The benchmarking circuit generates a benchmarking metric indicative of a performance of the benchmarking circuit during operation. For a particular circuit configuration, the benchmarking circuit generates a benchmarking metric value. The internal reference component participates in the benchmarking circuit and a first benchmarking metric value is generated. The target component participates in the benchmarking circuit and a second benchmarking metric value is generated. In some examples, both the target and internal reference components participate in the benchmarking circuit and one or more benchmarking metric values are generated. The benchmark value is calculated based on the benchmarking metric values generated by the benchmarking circuit.

In a first example, the benchmarking circuit is a single ended harmonic oscillator. The characteristic time constant of the oscillator is the benchmarking metric and is based on the characteristic resistance, R, and capacitance, C, of the circuit. An internal reference component including metal-oxide-silicon (MOS) capacitors participates in the benchmarking circuit. A target component including metal-oxide-metal (MOM) capacitors participates in the benchmarking circuit. The MOS capacitors exhibit lower sensitivity to changes in test conditions than the MOM capacitors. A first benchmarking metric value is generated based on benchmarking circuit operating in the first configuration and second benchmarking metric value is generated based on benchmarking circuit operating in the second configuration. Based on these values, a first benchmark value is calculated. The benchmark value is used to calibrate tunable circuit elements that include MOM capacitors. In another example, a second benchmark value is calculated based on the first benchmarking metric value. This benchmark value is useable to calibrate tunable circuit elements that include resistors.

A benchmarking metric measurement module (BMMM) of an Integrated Circuit (IC) that generates benchmarking metric values is described. The BMMM includes one internal reference component with a sensitivity to changes in test conditions that is lower than a target component to be benchmarked on the IC. Methods for calculating benchmark values based on the benchmarking metric values generated by the BMMM are described. The benchmark values are used to compensate for changes in conditions that affect the performance of the tunable circuit elements. Tunable circuit elements are calibrated based on the benchmark value. The tunable circuit elements include components similar to target components benchmarked to the internal reference component of the BMMM. In this manner, tunable circuit elements of the IC may be calibrated to compensate for changes in conditions without external reference components.

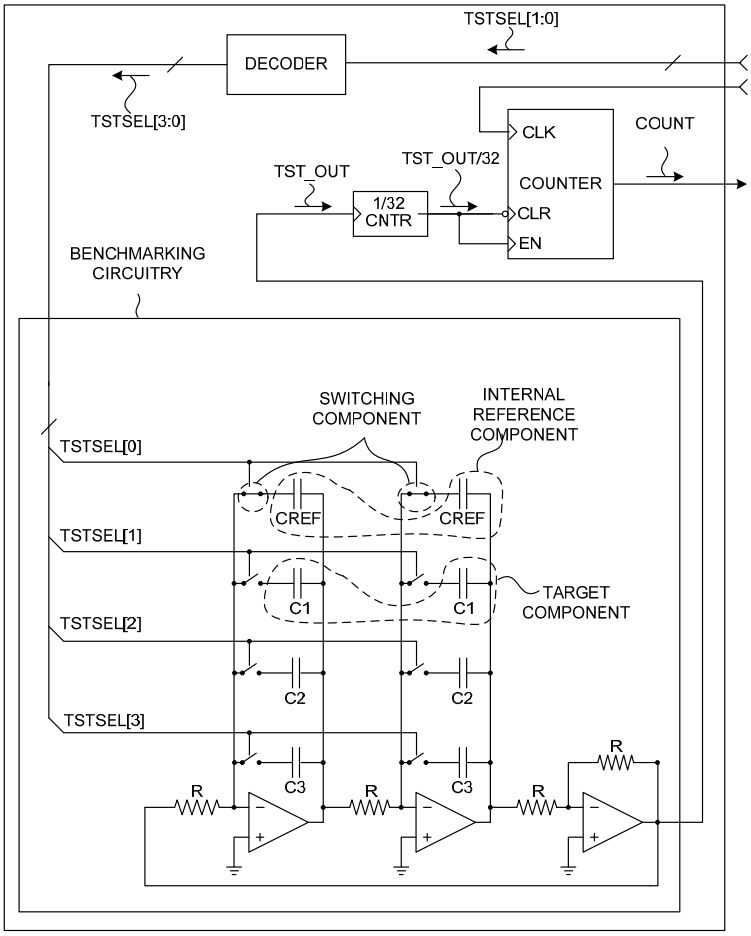

Figure 3-1 Benchmarking Metric Measurement Module (Example 1)

Figure 3-1 illustrates BMMM. BMMM includes one internal reference component with a sensitivity to changes in conditions that is lower than a target component to be benchmarked. BMMM generates benchmarking metric values useable to calculate benchmark values. BMMM includes benchmarking circuitry, decoder block, downcounter block, and counter block. BMMM is operable to receive a test control signal (TSTSEL[1:0]) and a clock signal (CLK), and output a COUNT signal. In the present example, benchmarking circuitry is a single ended harmonic oscillator that produces a sine wave output signal. Benchmarking circuitry includes a characteristic resistance, R, and capacitance, C.

Ideally, benchmarking circuitry outputs an oscillatory signal, TST_OUT, with a period of oscillation, $\tau \sim RC$. In the present example, the benchmarking metric of benchmarking circuitry is the period of oscillation associated with the sine wave output signal of benchmarking circuitry. In operation, benchmarking circuitry outputs an oscillatory signal, TST_OUT, with a period of oscillation, $\tau = RC(1+\alpha)$. Parameter, α, is representative of non-ideal behavior of benchmarking circuitry. Parasitic resistance and capacitance from the wires and the finite gain-bandwidth product of the operational amplifiers of benchmarking circuitry introduces approximately 6% inaccuracy (max-min) in the estimation of the RC time constant, τ in a typical CMOS process

technology. The unit cells of capacitors of benchmarking circuitry (e.g. internal reference component and target component) can be selectively switched by test control signal TSTSEL. The test control signal TSTSEL[1:0] is a two bit binary signal generated and communicated to BMMM. Decoder receives test control signal TSTSEL[1:0], decodes this signal, and outputs corresponding binary digital control signals TSTSEL[3:0] that control switching components of benchmarking circuitry. By alternatively closing each pair of switching components, different pairs of capacitors participate in benchmarking circuitry. One pair of capacitors illustrated is internal reference component. In the present example, internal reference component is a pair of MOS capacitors each with a nominal capacitance value of approximately 1 pF. MOS capacitors are selected as the internal reference component because they exhibit relatively low sensitivity to changes in conditions. A second pair of capacitors illustrated is target component. In the present example, target component is a pair of MOM capacitors each with a nominal capacitance value of approximately 1 pF. MOM capacitors exhibit relatively high sensitivity to changes in conditions. It is desirable to benchmark the MOM capacitors to the MOS capacitors by calculating a benchmark value useable to calibrate tunable circuit elements that include MOM capacitors, and thus compensate for changes in conditions. Other types of capacitors present with relatively high sensitivity to process variations may be included as second and third target components.

The output signal, TST_OUT, of benchmarking circuitry is processed by BMMM to generate a benchmarking metric value that is communicated to a digital baseband IC. In the present example, benchmarking metric value is a COUNT value indicative of the time constant of benchmarking circuit for a given configuration. Output signal, TST_OUT, is an oscillatory signal that is downcounted by a factor of 32 by downcounter block. Counter determines how many cycles of clock signal CLK received on BMMM occur within a half period of downcounted signal TST_OUT/32.

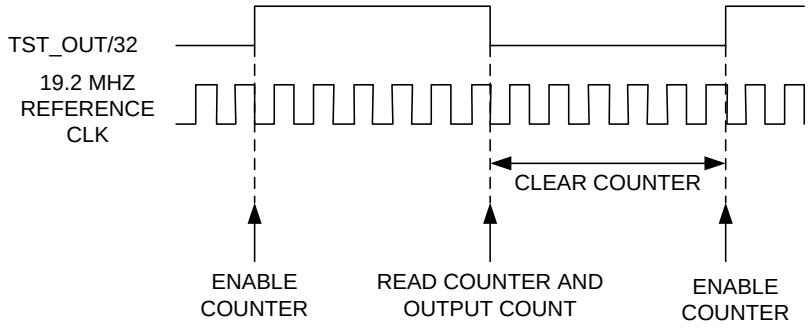

Figure 3-2 Counter Function in BMMM

As illustrated in Figure 3-2, counter circuit is enabled on each rising edge of divided down output signal TST_SEL/32. Counter then counts the number of cycles of reference clock signal CLK until the next falling edge of downcounted signal TST_OUT/32 is reached. Counter therefore counts during the high portion of the TST_OUT/32 signal illustrated in Figure 3-2. Counter outputs the measured count signal COUNT, and is then held in the cleared state until the

next rising edge of TST_OUT/32 is reached. Signal COUNT is communicated to a digital baseband IC.

The time period of oscillation of benchmarking circuitry is

$$T = 2\pi RC(1+\alpha) \tag{3-1}$$

For a clock signal oscillating at a frequency of 19.2 MHz, the time period measured by counter is

$$T_{measured} = \frac{COUNT}{19.2e6} \tag{3-2}$$

During the measurement time period, $T_{measured}$, benchmarking circuitry has oscillated sixteen times. Thus, the time period of oscillation of benchmarking circuitry can be calculated by digital baseband IC as

$$T = 2\pi RC(1+\alpha) = \frac{COUNT}{(16)(19.2e6)} \tag{3-3}$$

The time constant of an RC oscillator circuit may be defined as

$$\tau = RC(1+\alpha) \tag{3-4}$$

Thus, the time constant of benchmarking circuitry may be calculated by digital baseband IC as

$$\tau = RC(1+\alpha) = \frac{COUNT}{(16)(2\pi)(19.2e6)} \tag{3-5}$$

In this manner, benchmarking metric value is indicative of the time constant of benchmarking circuit for a given configuration.

As illustrated in Figure 3-1, in a first configuration of benchmarking circuitry, control signal TSTSEL[0] maintains switching components in a closed state, while control signals TSTSEL[1], TSTSEL[2], and TSTSEL[3] maintain the switching components under their control in an open state. Thus, only internal reference component participates in benchmarking circuit and the time constant of output signal TST_OUT is $\tau=RC_{ref}(1+\alpha_1)$. In a second configuration, control signal TSTSEL[1] maintains the switching components under its control in a closed state, while control signals TSTSEL[0], TSTSEL[2], and TSTSEL[3] maintain the switches under their control in an open state. Thus, only target component participates in benchmarking circuitry and the time constant of output signal TST_OUT in the second measurement is $\tau=RC_1(1+\alpha_2)$.

In the present example, internal reference component is a pair of MOS capacitors each with a capacitance value of approximately 1 pF. The resistors of benchmarking circuitry exhibit a resistance of approximately 100 KΩ. As benchmarking circuitry oscillates, BMMM

communicates a COUNT value representative of the time constant of benchmarking circuitry in this configuration to digital baseband IC, which calculates a time constant of benchmarking circuitry as discussed above for this configuration of benchmarking circuitry.

$$\tau_{MOS,test} = R_{test} C_{MOS,test} (1 + \alpha_1) \tag{3-6}$$

Similarly, the digital baseband IC communicates a second test selection signal to BMMM. BMMM responds by selecting a target component of benchmarking circuit as the element under test. Thus, in this second configuration, target component participates in benchmarking circuitry. In the present example, the target component is a pair of MOM capacitors each with a capacitance value of approximately 1 pF. As benchmarking circuitry oscillates, BMMM communicates a COUNT value representative of the time constant of benchmarking circuitry in this configuration to digital baseband IC, which calculates a time constant of benchmarking circuitry as discussed above for the case where a MOM capacitor is selected as the component under test.

$$\tau_{MOM,test} = R_{test} C_{MOM,test} (1 + \alpha_2) \tag{3-7}$$

In manufacture, a number of ICs, each with a benchmarking circuitry, are measured in both the configuration where the MOS capacitors participate and the configuration where the MOM capacitors participate. The results are averaged to calculate a nominal time constant of benchmarking circuitry for both each configuration.

$$\tau_{MOS,nom} = R_{nom} C_{MOS,nom} (1 + \alpha_{nom}) \tag{3-8}$$

$$\tau_{MOM,nom} = R_{nom} C_{MOM,nom} (1 + \alpha_{nom}) \tag{3-9}$$

In the present example, a benchmark value, λ, is defined as the ratio of the capacitance of the MOM capacitor under nominal conditions to the capacitance of the MOM capacitor tested during the operational lifetime of mobile communication device. Thus, benchmark value, λ, is useable to characterize a change in capacitance of the MOM capacitor from nominal conditions.

$$\lambda = \frac{C_{MOM,nom}}{C_{MOM,test}} \tag{3-10}$$

Benchmark value, λ, is a useful metric for calibrating tunable circuit elements. Based on Equations (3-6) ~ (3-9) and the definition of Equation (3-10), benchmark value, λ, can be expressed as follows:

$$\lambda = \frac{\tau_{MOM,nom}}{\tau_{MOM,test}} \cdot \frac{\tau_{MOS,test}}{\tau_{MOS,nom}} \cdot \frac{C_{MOS,nom}}{C_{MOS,test}} \cdot \frac{(1 + \alpha_2)}{(1 + \alpha_1)} \tag{3-11}$$

In a first approximation, it is assumed that the PVT variation of a MOS capacitor is negligible within an acceptable error range. Under this assumption, benchmark value, λ, can be expressed as follows:

$$\lambda \approx \frac{\tau_{MOM,nom}}{\tau_{MOM,test}} \cdot \frac{\tau_{MOS,test}}{\tau_{MOS,nom}} \cdot \frac{(1+\alpha_2)}{(1+\alpha_1)} \qquad (3\text{-}12)$$

In a second approximation, the parasitic effects associated with the wires and operational amplifiers of benchmarking circuitry during test conditions of the MOS capacitors and MOM capacitors are presumed to be the same. Under this assumption, benchmark value, λ, can be expressed as follows:

$$\lambda \approx \frac{\tau_{MOM,nom}}{\tau_{MOM,test}} \cdot \frac{\tau_{MOS,test}}{\tau_{MOS,nom}} \qquad (3\text{-}13)$$

For a given PVT condition during test, the parasitic effects are almost identical for both configurations of benchmarking circuitry. This is because both tests are performed using the same test circuit employing the same operational amplifier components. In this manner, benchmark value, λ, may be calculated with minimal influence from the systemic, parasitic errors of benchmarking circuitry. For example, presuming that τ_{MOS} is measured with a parasitic error of +25.5% and τ_{MOM} is measured with a parasitic error of +24.5%, the error induced in the calculation of λ is less than 1%. Thus, in the case where parasitic errors of the measurement circuit are 25 +/- 0.5 %, the calculation of benchmark value, λ, is practically unaffected.

This stands in contrast to the case where an external resistor is used. For the case of calibration with an external resistor, the systemic, parasitic errors of the benchmarking circuit are not cancelled. Even with a perfectly stable external resistor, the parasitic errors introduced by the benchmarking circuit are directly reflected in the measurement result, thus limiting tuning accuracy. However, by benchmarking to an internal reference component as discussed above, the systemic errors of the benchmarking circuit are largely cancelled. Thus, the tuning accuracy is primarily limited by the PVT variation of the internal reference component, rather than the systemic errors of the benchmarking circuit.

Benchmark value, λ, is calculated based on stored values and the first and second benchmarking metric values. As discussed above, the time constants $\tau_{MOM,nom}$ and $\tau_{MOS,nom}$ of Equation (3-13) are stored in memory. As illustrated in equation (3-5), $\tau_{MOS,test}$ and $\tau_{MOM,test}$ can be calculated based on the COUNT value generated by benchmarking circuitry in the first configuration and the COUNT value generated by benchmarking circuitry in the second configuration, respectively. In this manner, a benchmark value is calculated that is useable to tune circuit elements employing MOM capacitors.

Digital baseband IC may also calculate a benchmark value, γ, useful for tuning resistors. Benchmark value, γ, is defined as the ratio of the resistance of the resistors of benchmarking

circuitry when the resistors are tested during the operational lifetime of mobile communication device to the nominal resistance of the resistors.

$$\gamma = \frac{R_{test}}{R_{nom}} \tag{3-14}$$

Based on Equations (3-6) and (3-8) and the definition of Equation (3-14), benchmark value, γ, may be expressed as follows:

$$\gamma = \frac{\tau_{MOS,test}}{\tau_{MOS,nom}} \cdot \frac{C_{MOS,nom}(1+\alpha_{nom})}{C_{MOS,test}(1+\alpha_1)} \tag{3-15}$$

In a first approximation, it is assumed that the PVT variation of a MOS capacitor is negligible within an acceptable error range. In a second approximation, the parasitic effects associated with the wires and operational amplifiers of benchmarking circuitry during test conditions of the MOS capacitors is presumed to be negligible. Under this assumption, benchmark value, γ, can be expressed as follows:

$$\gamma \approx \frac{\tau_{MOS,test}}{\tau_{MOS,nom}} \tag{3-16}$$

Benchmark value, γ, is calculated based on a stored value and the first benchmarking metric value. As discussed above, the time constant $\tau_{MOS,nom}$ of Equation (3-16) is stored in memory. As illustrated in Equation (3-5), $\tau_{MOS,test}$ may be calculated based on the COUNT value generated by benchmarking circuitry in the first configuration. In this manner, a benchmark value is calculated that is useable to tune circuit elements employing resistors. In this manner, the resistance of the benchmarking circuitry is the target component that is benchmarked to the MOS capacitors.

3.4 Calibration using Benchmark Values

Benchmark values, λ and γ, can be used in several ways to compensate for changes in conditions in tunable circuit elements. Figure 3-3 illustrates central bias generator, power amplifier, and tunable resonant tank. Tunable resonant tank includes a tunable capacitor network. Central bias generator includes a tunable resistor network. Power amplifier includes a tunable current scaling network. Control logic receives a CODE signal from digital baseband IC that includes a control value calculated by digital baseband IC based at least in part on at least one benchmark value such as λ and γ. In response, control logic communicates a signal to a tunable circuit element that causes the configuration of the tunable circuit element to be changed. In this manner, the

control value calculated at least in part on a benchmark value is useable to change the configuration of tunable circuit element. In one example, control logic outputs control signal CSEL to calibrate the capacitance of capacitor network based on the CODE signal. In a second example, control logic outputs control signal TSEL to calibrate a network of transistors of current scaling network based on the CODE signal. In a third example, control logic outputs control signal RSEL to calibrate the resistance of resistor network based on the CODE signal.

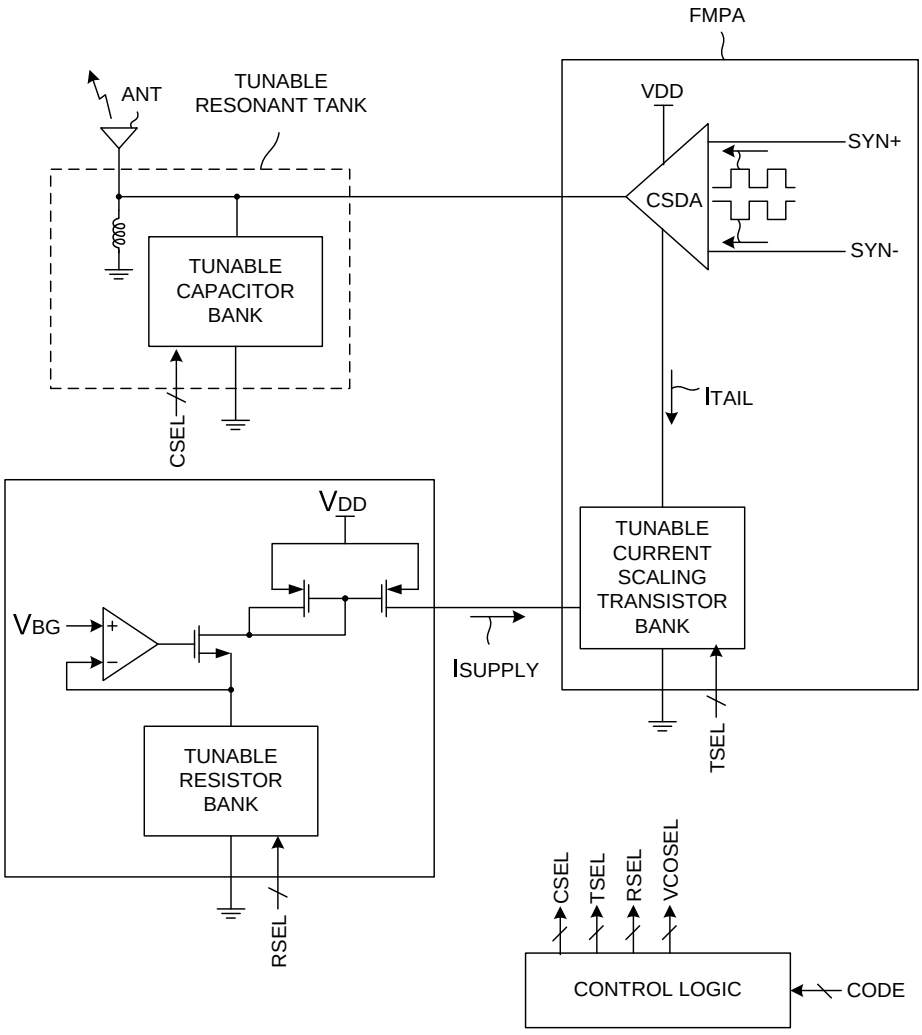

Figure 3-3 Tunable Circuit Blocks

In the first example, digital baseband IC communicates a new capacitor selection code based on the benchmark value, λ, as part of the CODE signal communicated to control logic. In this

manner, benchmark value, λ, can be used to compensate for changing capacitance due to variations in conditions.

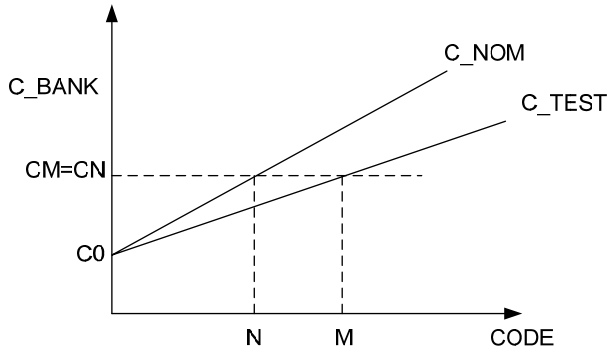

Figure 3-4 Capacitor Tuning Code Offset

Figure 3-4 illustrates a plot of the capacitance of the tunable capacitor network as a function of capacitor tuning code. In the present example, the capacitor tuning code has a range between 0 and 127 (a bank with 7 bit resolution). With the tuning code set to zero (e.g. each capacitor switch is open), the capacitor bank exhibits some parasitic capacitance, C_p. The capacitance of the capacitor bank (C_bank) increases linearly as a function of tuning code. Under nominal conditions (e.g. average factory conditions), the capacitance of the bank follows the "C_nom" line illustrated. As the tuning code is incremented by one, an additional MOM unit capacitor is added to the bank by closing its capacitor switch. Thus, under nominal conditions for a tuning code "N" the capacitance of the capacitor bank may be expressed as follows:

$$C_{bank,nom} = NC_{MOM,nom} + C_{p,nom} \tag{3-17}$$

However, as conditions change, the capacitance of each MOM unit capacitor also changes. As the tuning code is incremented, the amount of additional bank capacitance contributed by each MOM unit capacitor changes. During test conditions, the capacitance follows the "C_test" line illustrated. Under test conditions for a tuning code "M" the capacitance of the capacitor bank may be expressed as follows:

$$C_{bank,test} = MC_{MOM,test} + C_{p,test} \tag{3-18}$$

The benchmark value, λ, can be used to calculate the capacitor tuning code "M" that will provide the same capacitance as provided by capacitor tuning code "N" under nominal conditions. Under the assumption that the difference in parasitic capacitance under nominal and test conditions is negligible, the bank capacitance under test conditions with tuning code "M" is equated with the bank capacitance under nominal conditions with tuning code "N". Tuning code "M" may be expressed as follows:

$$M \approx N \frac{C_{MOM,nom}}{C_{MOM,test}} = \lambda N \tag{3-19}$$

To compensate for changes in conditions, the code of a bank of MOM capacitors operating under conditions present during test is calculated as the benchmark value, λ, multiplied by the code of the same bank of MOM capacitors operating under nominal conditions. In the present example, new capacitor tuning code "M" is communicated to control logic. Control logic communicates this code as a binary digital control signal CSEL useable to adjust the capacitance of tunable capacitor network by changing the configuration of tunable capacitor bank.

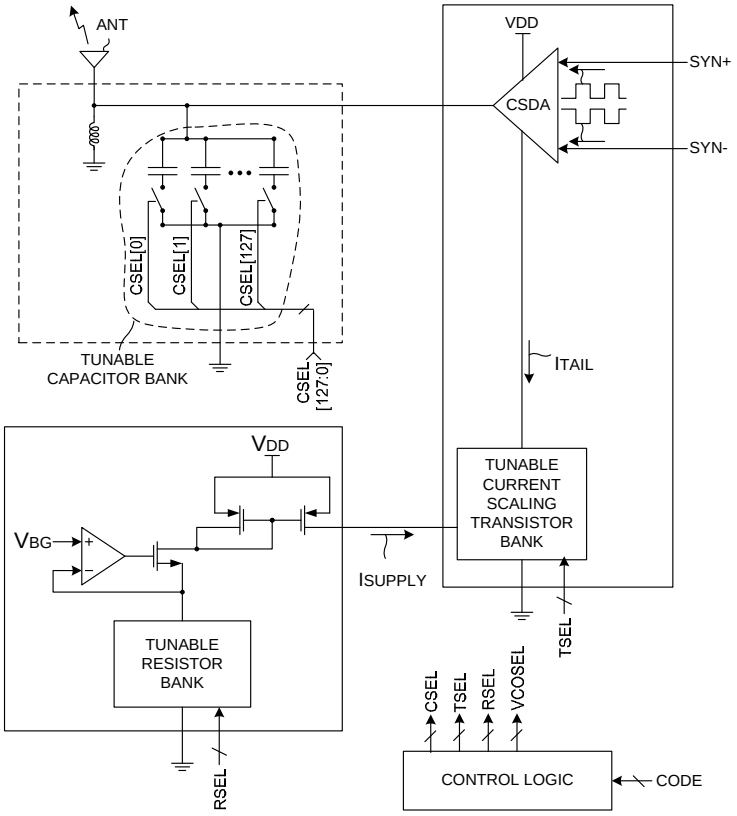

Figure 3-5 Capacitor Bank Tuning

Figure 3-5 illustrates tunable capacitor network in one example. Tunable capacitor network includes 128 MOM capacitors arranged in parallel. The capacitors are selected in coordination with inductor of resonant tank to achieve a desired oscillation frequency, for example, 76 MHz-108 MHz. In one example, inductor exhibits an inductance of approximately 150 nH. The capacitance of each capacitor is either included or excluded from the network by operation of an associated switching component. As a switch associated with a particular capacitor is closed, the capacitance of that capacitor is included as part of the capacitance of the network. In the present

example the capacitance value of each capacitor is approximately 0.25 pF. In the present example, each bit of control signal CSEL communicated from control logic addresses a corresponding switching component of network. In this manner, the resonant frequency of LC tank is calibrated based at least in part on the benchmarking metric values generated by BMMM.

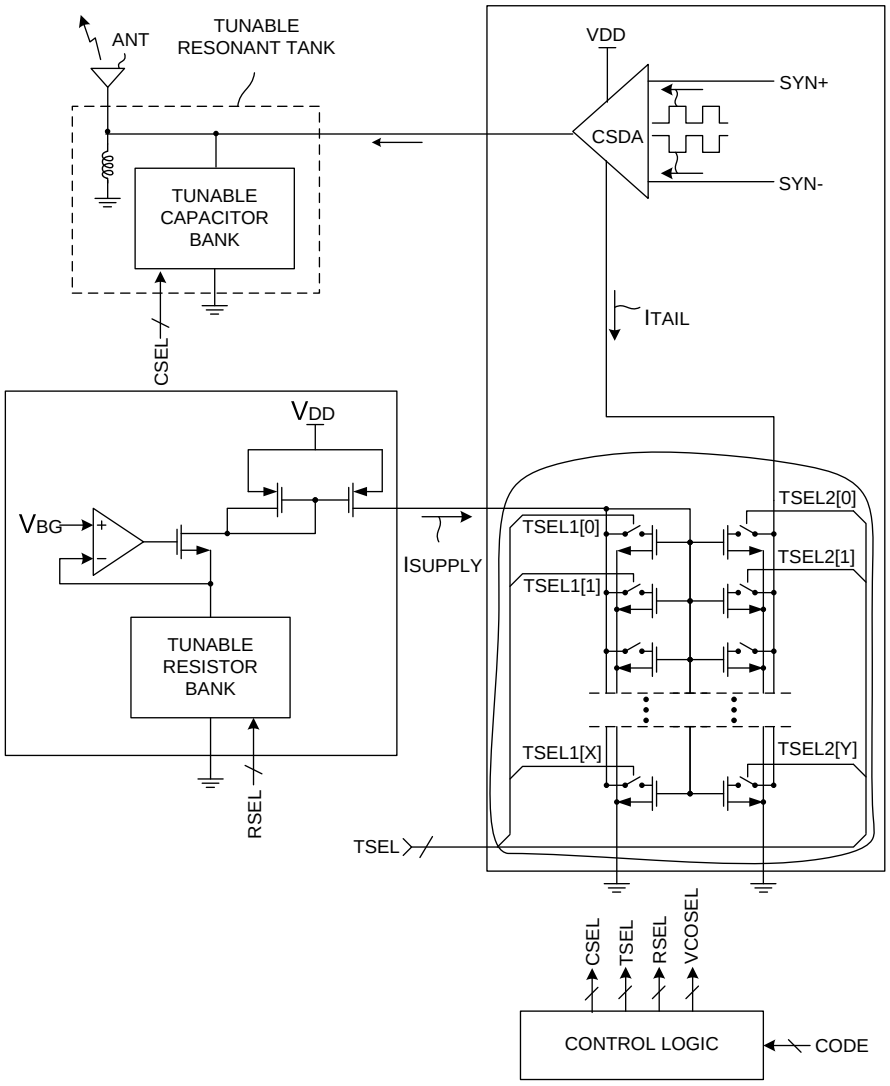

Figure 3-6 Current Scaling Bank Tuning

In the second example, digital baseband IC communicates a new transistor selection code based on the benchmark value, γ, as part of the CODE signal communicated to control logic. In this manner, benchmark value, γ, can be used to compensate for changing current levels due to variations in conditions. To maintain a relatively constant tail current in the face of varying supply current, a tunable current scaling network is employed. Network includes two banks of transistors. The transistors of each bank are arranged in parallel. By adjusting the number of transistors participating in each bank, tail current can be scaled as a function of supply current. In the illustrated example, X+1 transistors are selectively coupled in parallel between central bias

generator and ground. Supply current scaling code, TSEL1, selects the number of transistors coupled in parallel, and thus determines the supply current scaling, CS_{supply}. Similarly, Y+1 transistors are selectively coupled in parallel between CSDA and ground. Tail current scaling code, TSEL2, selects the number of transistors coupled in parallel, and thus determines the tail current scaling, CS_{tail}. The tail current is related to the supply current by current scaling ratio, CS_{tail}/CS_{supply}, as follows:

$$\frac{I_{Tail}}{I_{Supply}} = \frac{CS_{Tail}}{CS_{Supply}} \tag{3-20}$$

Central bias generator includes operational amplifier and a tunable resistor network with a resistance, $R_{network}$. Under test conditions, amplifier and network generate current from a bandgap voltage source, V_{BG}, as follows:

$$I_{Supply,test} = \frac{V_{BG}}{R_{network,test}} \tag{3-21}$$

Under nominal conditions, amplifier and network generate current from a bandgap voltage source, V_{BG}, as follows:

$$I_{Supply,nom} = \frac{V_{BG}}{R_{network,nom}} \tag{3-22}$$

Under the assumption that the bandgap voltage, V_{BG}, is relatively stable in the face of changing conditions, the ratio of supply current under nominal conditions to the supply current under test conditions can be related to benchmark value, γ, as follows:

$$\frac{I_{Supply,nom}}{I_{Supply,test}} = \frac{R_{network,test}}{R_{network,nom}} = \frac{R_{unit,test}}{R_{unit,nom}} \frac{RSEL_{nom}}{RSEL_{test}} = \gamma \frac{RSEL_{nom}}{RSEL_{test}} \tag{3-23}$$

In this example, tunable resistor network includes a number of unit resistors arranged in parallel. Switching elements under the control of binary control signal RSEL determine whether each unit resistor participates in the network. The resistance of tunable network, $R_{network}$, is the resistance of a unit resistor, R_{unit}, divided by the number of unit resistors participating in the network as determined by control signal RSEL. In this example, tunable resistor network is not tuned. Thus, the same control signal is used under both nominal and test conditions. Under these conditions, the following relationship exists.

$$\frac{I_{Supply,nom}}{I_{Supply,test}} = \gamma \tag{3-24}$$

The change in supply current is approximated by benchmark parameter, γ. Because tail current is related to supply current directly by the current scaling ratio, benchmark parameter, γ, may be used to adjust the current scaling ratio to compensate of changes in supply current and maintain a constant tail current. By equating the tail current under test conditions with the tail current under nominal conditions, the current scaling ratio under test conditions can be calculated from the current scaling ratio under nominal conditions and benchmark parameter, γ, as follows:

$$\begin{aligned} I_{Tail,test} &= I_{Tail,nom} \\ \left(\frac{CS_{Tail}}{CS_{Supply}}\right)_{test} I_{Supply,test} &= \left(\frac{CS_{Tail}}{CS_{Supply}}\right)_{nom} I_{Supply,nom} \\ \left(\frac{CS_{Tail}}{CS_{Supply}}\right)_{test} &= \gamma\left(\frac{CS_{Tail}}{CS_{Supply}}\right)_{nom} \end{aligned} \quad (3\text{-}25)$$

In the present example, a new transistor tuning code based on benchmark value, γ, is communicated to control logic. Control logic communicates this code as a binary digital control signal TSEL useable to adjust the number of transistors participating in each bank of tunable current scaling network based on scaling factor, γ.

In the third example, digital baseband IC communicates a new resistor selection code based on the benchmark value, γ, as part of the CODE signal communicated to control logic. In this manner, benchmark value, γ, can be used to compensate for changes in resistance due to variations in conditions.

Figure 3-7 illustrates central bias generator in greater detail. As discussed above, central bias generator includes operational amplifier and a tunable resistor network with a resistance, $R_{network}$. In this example, tunable resistor network includes a number of unit resistors arranged in parallel. Switching elements under the control of binary control signal RSEL determine whether each unit resistor participates in the network.

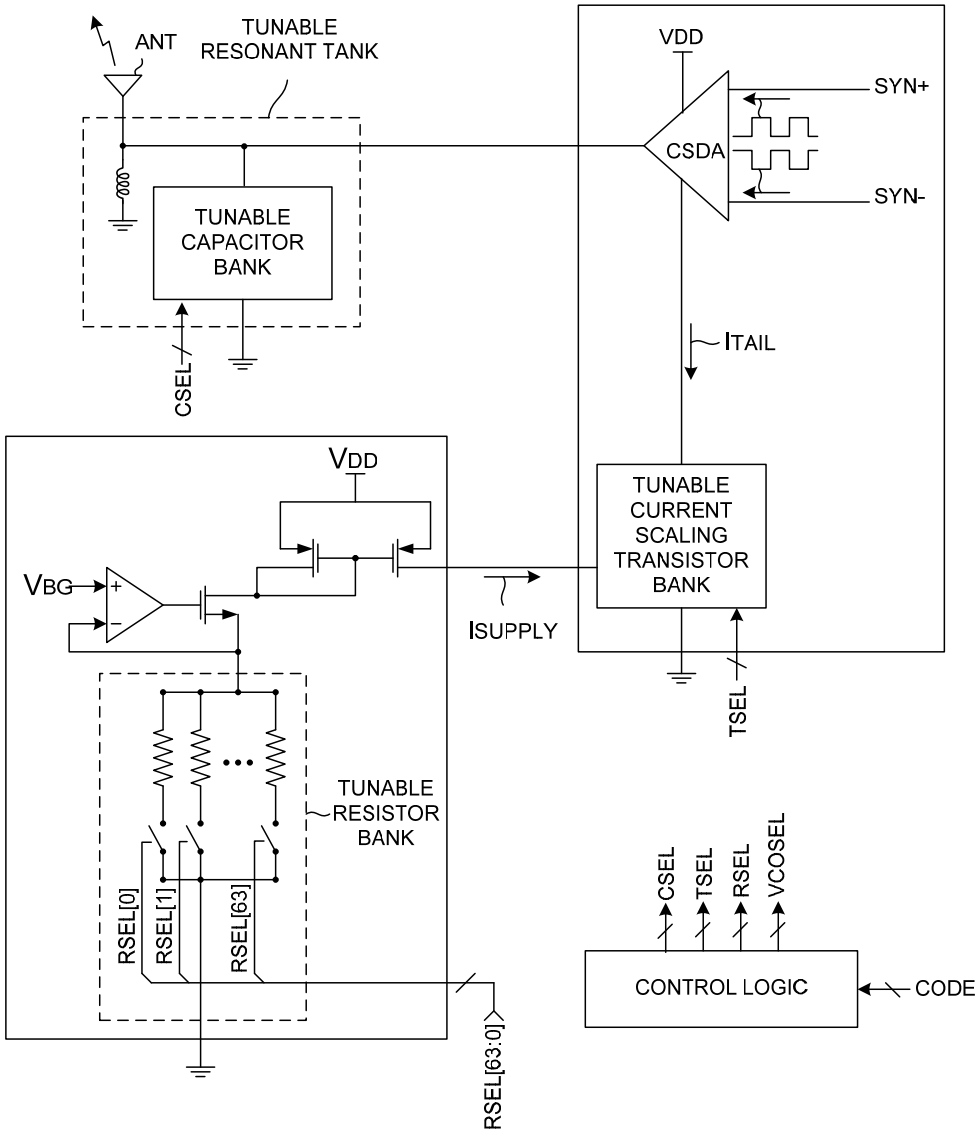

Figure 3-7 Resistor Bank Tuning

The resistance of tunable network, $R_{network}$, is the resistance of a unit resistor, R_{unit}, divided by the number of unit resistors participating in the network as determined by control signal RSEL. The resistance of each unit resistor of tunable resistor network varies as conditions change. Benchmark value, γ, can be used to compensate for variation in the resistance of tunable resistor network directly to maintain a constant supply current. It is desired to maintain the same supply current under both nominal and test conditions.

$$I_{Supply,test} = I_{Supply,nom} \tag{3-26}$$

Combining the desired relationship of equation (26) with equations (14) and (23), the following result is obtained.

$$\frac{I_{Supply,nom}}{I_{Supply,test}} = \frac{R_{network,test}}{R_{network,nom}} = \frac{R_{unit,test}}{R_{unit,nom}} \frac{RSEL_{nom}}{RSEL_{test}} = \gamma \frac{RSEL_{nom}}{RSEL_{test}} = 1 \quad (3\text{-}27)$$

Thus, a new resistor bank code may be calculated based on benchmark parameter, γ, and a nominal value of the resistor bank code.

$$RSEL_{test} = \gamma RSEL_{nom} \quad (3\text{-}28)$$

The digital baseband IC calculates a new resistor bank code by scaling the initial resistor bank code by γ, as illustrated in equation (3-28), such that the resistance of network is maintained at the same value in the face of changes in conditions. In this manner, supply current is maintained at the same value in the face of changes in conditions. In the present example, a new current scaling tuning code is communicated to control logic. Control logic communicates this code as a binary digital control signal RSEL useable to change the configuration of tunable resistor network by adjusting the number of resistors participating in tunable resistor network based on benchmark value, γ.

3.5 Other Examples of BMMM

Figure 3-8 illustrates a second example of BMMM operable to generate benchmarking metric values useable to calculate a benchmark value. The present BMMM includes central bias generator and a second example of benchmarking circuitry.

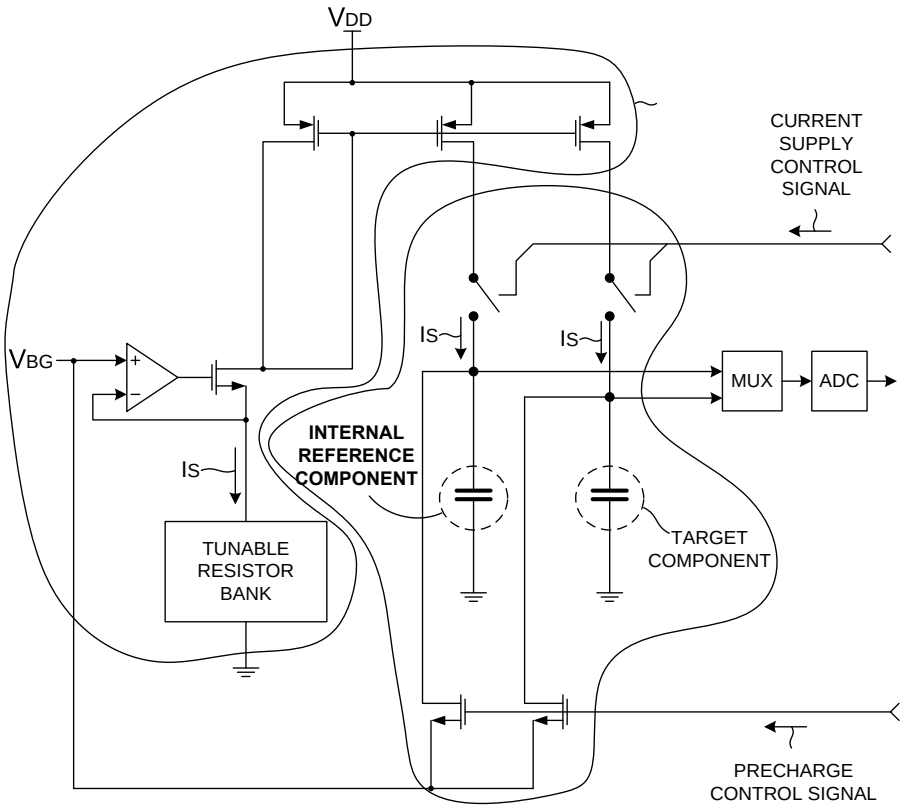

Figure 3-8 Benchmarking Metric Measurement Module (Example 2)

In the illustrated example, a supply current is generated by central bias generator. The supply current is communicated to two capacitors. The first capacitor is an internal reference component. In the present example, the internal reference component includes one MOS capacitor. The second capacitor is a target component to be benchmarked to the internal reference component. In the present example, the target component includes one MOM capacitor. A precharge control signal is communicated to BMMM. The precharge control signal causes the bandgap voltage to be communicated to both capacitors. Thus, both capacitors are precharged to the same voltage level. The voltage level is selected such that the MOS capacitor is driven in a region of operation where non linearity is not significant. After the precharge is complete, the precharge control signal is released. A current supply control signal is communicated to BMMM. The current supply control signal causes supply currents from central bias generator to charge both capacitor networks for the same fixed amount of time. After the fixed period of time, a signal indicative of the potential across each capacitor is generated by

benchmarking circuitry. In the present example, the benchmarking metric is the potential across a capacitor network and the benchmarking metric values are the potential across the MOS capacitor and the potential across the MOM capacitor. These values are multiplexed by multiplexer and converted to digital code by analog to digital converter. The resulting codes indicative of the benchmarking metric values are communicated to digital baseband IC. Because, the charging conditions of both the MOS and MOM capacitors are nearly identical, the ratio of the potential across each capacitor is equivalent to the inverse of the ratio of the capacitance of each capacitor. Under test conditions, the relationship may be expressed as:

$$\frac{V_{MOM,test} - V_{BG}}{V_{MOS,test} - V_{BG}} = \frac{C_{MOS,test}}{C_{MOM,test}} \tag{3-29}$$

Under nominal conditions, the relationship may be expressed as:

$$\frac{V_{MOM,nom} - V_{BG}}{V_{MOS,nom} - V_{BG}} = \frac{C_{MOS,nom}}{C_{MOM,nom}} \tag{3-30}$$

Benchmark value, λ, defined in Equation (3-10), can be rewritten as a function of ratio of the potential across both the MOS and MOM capacitors under both nominal and test conditions. Starting with the definition of benchmark value, λ, defined in Equation (3-10) and using Equations (3-29) and (3-30), we arrive at the following relation.

$$\lambda = \frac{C_{MOM,nom}}{C_{MOM,test}} = \frac{(V_{MOS,nom} - V_{BG})}{(V_{MOM,nom} - V_{BG})} \frac{(V_{MOM,test} - V_{BG})}{(V_{MOS,test} - V_{BG})} \frac{C_{MOS,nom}}{C_{MOS,test}} \tag{3-31}$$

Benchmark value, λ, may be expressed as a function of the ratio of the benchmark metric values generated by benchmarking circuitry under nominal conditions and under test conditions. Noting that the capacitance of a MOS capacitor under nominal conditions is approximately the same as its capacitance under test conditions, benchmark value, λ, may be expressed as:

$$\lambda \approx \frac{(V_{MOS,nom} - V_{BG})}{(V_{MOM,nom} - V_{BG})} \frac{(V_{MOM,test} - V_{BG})}{(V_{MOS,test} - V_{BG})} \tag{3-32}$$

In this manner, benchmark value, λ, is calculated based on the benchmarking metric values. Furthermore, the calculated benchmark value, λ, is useable to calibrate a tunable circuit element such as tunable capacitor network in the same manner as discussed above.

Figure 3-9 illustrates a third example of BMMM operable to generate benchmarking metric values useable to benchmark a target component to an internal reference component. The present BMMM is similar to the second example described above, except the target component includes a tunable capacitor network of MOM capacitors and the internal reference component

includes at least one MOS capacitor. In addition, a capacitor selection signal, binary digital control signal CSEL, is received by BMMM and determines a configuration of the tunable capacitor network. As discussed above, a signal indicative of the potential across each capacitor network is generated by benchmarking circuitry. The benchmarking metric is the potential across a capacitor network and the benchmarking metric values are the potential across the MOS capacitors and the potential across the tunable network of MOM capacitors.

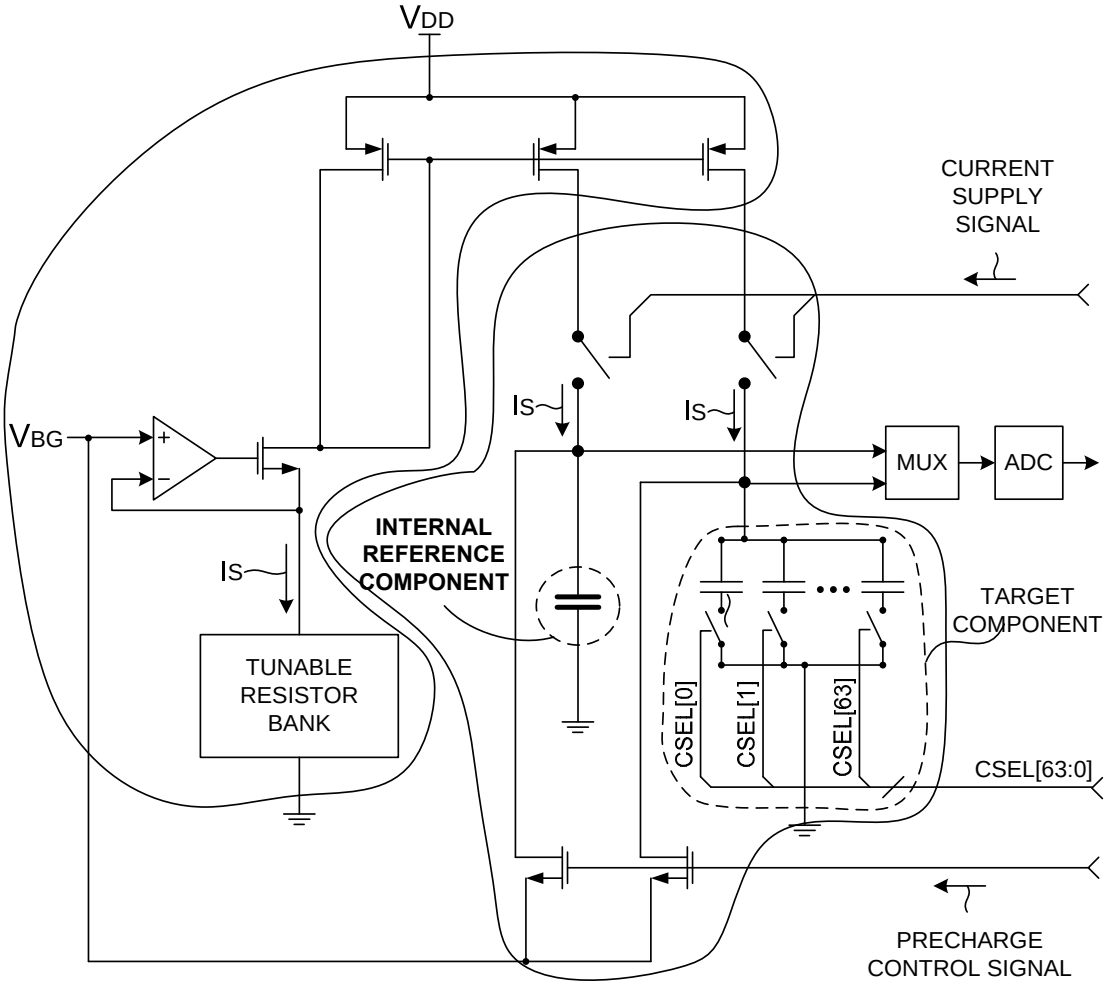

Figure 3-9 Benchmarking Metric Measurement Module (Example 3)

In the present example, the values are communicated to digital baseband IC, which executes a tuning algorithm stored in program memory that first determines a difference between the two benchmarking metric values to generate a benchmark value. In this manner, benchmark value, λ, is calculated based on the benchmarking metric values. In one example, the benchmarking metric values are communicated to digital baseband IC as digital codes and the digital baseband IC takes the difference between the values to calculate the benchmark value.

A benchmarking circuitry includes an analog comparator (not shown) that generates a difference value between the two benchmarking metric values. This difference value is converted into a digital code by ADC and the resulting code is communicated to digital baseband IC. Next, a tuning algorithm selects a new code based on the benchmark value representative of the difference in potential between MOS capacitor and the tunable capacitor bank.

The digital baseband IC may execute a binary search over the tuning code of the tunable capacitor network of MOM capacitors based on the benchmark value. The new capacitor selection code is communicated to BMMM as binary digital control signal CSEL and the configuration of tunable capacitor network is changed in response to control signal CSEL. The test is repeated until the voltage difference between the two capacitor networks converges. At this point, the capacitance of the target component is calibrated such that it is approximately the same as the capacitance of the internal reference component. Thus, BMMM and the tuning algorithm work together to iteratively benchmark the capacitance of the tunable MOM capacitor network to the capacitance of the MOS capacitor and then calibrate the MOM network to match the capacitance of the MOS capacitor.

After tuning the MOM capacitor network, resistance tuning can be performed. Resistance tuning may be performed as described above using the benchmarking circuit of Figure 3-1 where the internal reference component utilized in the benchmarking circuit of Figure 3-1 is made up of either a MOS capacitor or the tuned MOM capacitors. In other examples, resistance tuning may be performed by other circuitry operable to perform the task.

3.6 Summary

Theory of Benchmarking can be summarized by 4 steps: Internal Reference Component, Benchmarking Metric Measurement, Benchmark Value, and Calibration using Benchmark Value.

[Step 1: Internal Reference Component]

Identify one internal reference component within a first group of components of an integrated circuit that exhibits a degree of process sensitivity that is lower than a process sensitivity of a target component of a second group of components of the integrated circuit.

[Step 2: Benchmarking Metric Measurement]

Measure a first Benchmarking Metric of the first group of components and a second Benchmarking Metric of the second group of components.

[Step 3: Benchmark Value]

Calculate Benchmark Value from the first Benchmarking Metric or both the first and second Benchmarking Metrics.

[Step 4: Calibration using Benchmark Value]

Calculate a control value useable to change a configuration of the tunable circuit element based on the benchmark value. Communicate the control value to the tunable circuit element.

4 Experimental Prototype

4.1 RC Time Constant Measurement Module (RCMM)

4.1.1 Architecture

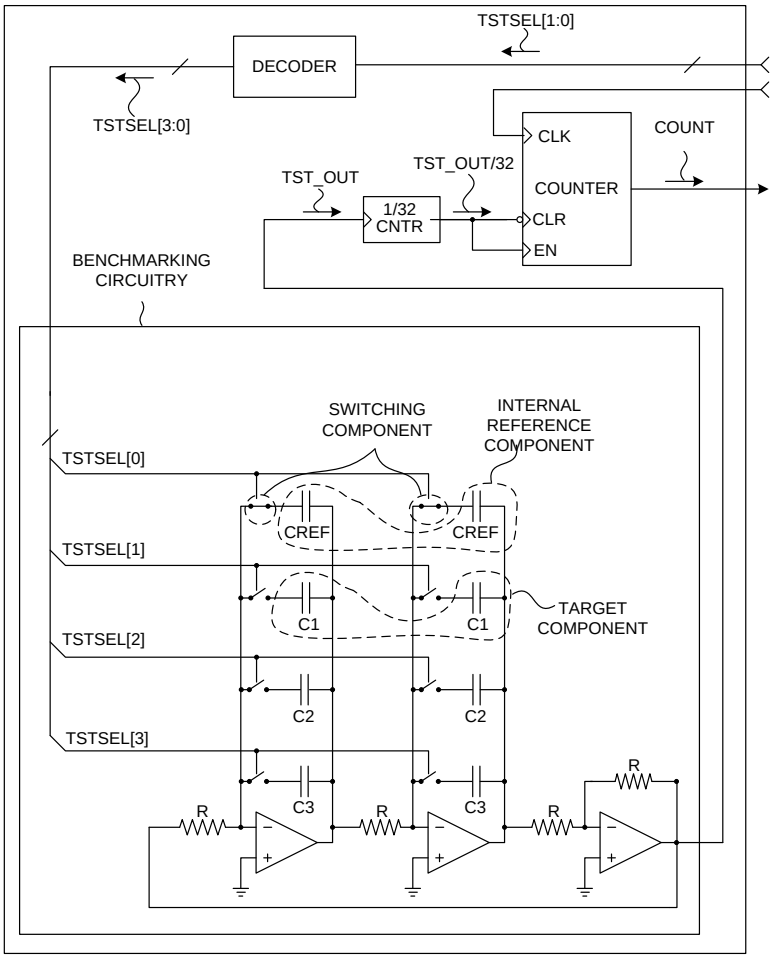

Figure 4-1 RC Time Constant Measurement Module

The block diagram of RCMM is shown in Figure 4-1. To measure an RC time constant, the module lets a counter determine how many TCXO clock cycles fit in a fixed number of cycles of a harmonic RC oscillator. A low-to-high transition of the 'start' input signal first powers up the harmonic oscillator. After waiting for a fixed amount of time to let the oscillator bias settle, it enables oscillation. The oscillator runs for some cycles during which a counter counts TCXO cycles. After the set number of harmonic oscillator cycles is finished, the measurement result is available in the counter, and the control block powers the module down. The RC measurement circuit can measure the time constant of poly resistor and three types of capacitors (set by TSTSEL<1:0>). RTMOM1 (RTMOM formed from M1 to M5), RTMOM2 (RTMOM formed from M2 to M4) and thick oxide MOSCAP and thin oxide MOSCAP.

4.1.2 Lambda Calibration without an external reference

From Equation (3-13), we can derive benchmark value, λ. Because counter values are proportional to the time constant from Equation (3-5), we can derive Equation (4-1) from Equation (3-5) and (3-13) as follows.

$$\lambda \approx \frac{Count_{MOM,nom}}{Count_{MOM,test}} \cdot \frac{Count_{MOS,test}}{Count_{MOS,nom}} \qquad (4\text{-}1)$$

PVT	COUNT (MOM_T)	COUNT (MOM_N)	COUNT (MOS_T)	COUNT (MOS_N)	λ	Code_N	Code_T
TT	237	237	211	211	1.000	44	44
FFHH	175	237	193	211	1.239	44	55
FFHL	175	237	193	211	1.239	44	55
FFCH	179	237	195	211	1.224	44	54
FFCL	179	237	196	211	1.230	44	54
SSHH	304	237	223	211	0.824	44	36
SSHL	304	237	224	211	0.828	44	36
SSCH	316	237	230	211	0.818	44	36
SSCL	317	237	233	211	0.826	44	36

Table 4-1 Lambda Calibration without an external reference

In Table 4-1, RTMOM1 (RTMOM formed from M1 to M5) was chosen and thin oxide MOSCAP was chosen. The counter values generated from RCMM were written in the columns 2 through 5 in Table 4-1. From Equation (4-1), a benchmark value, λ is calculated.

From Equation (3-19), we can derive a new sample code for capacitor bank in Table 4-1. The new sample codes are applied to tune the capacitor bank. Code_T means a new test code for a capacitor bank and Code_N means a nominal value of a code for a capacitor bank. TT means a typical corner and FF means a fast corner and SS means a slow corner. HT is high temperature (110C) and LT is low temperature (-30C). HV is high supply voltage (1.3V + 5%) and LV is low supply voltage (1.3V – 5%). At TT corner, it has 55C temperature and 1.3V supply voltage.

4.1.3 Lambda Calibration with an external reference

If we have an external precision resistor, we can make R tuner. Assuming that we can make an ideal R tuner where an external precision resistor has no variation and we can benchmark on-chip resistor under test with a perfect accuracy. Then we can derive Equation (4-2) and (4-3) through RC time constant measurement module.

$$\tau_{MOM,test} = R_{test} C_{MOM,test} (1 + \alpha_{test}) \qquad (4\text{-}2)$$

$$\tau_{MOM,nom} = R_{nom} C_{MOM,nom} (1 + \alpha_{nom}) \qquad (4\text{-}3)$$

In the present example, a benchmark value, λ, is defined as the ratio of the capacitance of the MOM capacitor under nominal conditions to the capacitance of the MOM capacitor tested during the operational lifetime of mobile communication device. Thus, benchmark value, λ, is useable to characterize a change in capacitance of the MOM capacitor from nominal conditions.

$$\lambda = \frac{C_{MOM,nom}}{C_{MOM,test}} \qquad (4\text{-}4)$$

Benchmark value, λ, is a useful metric for calibrating tunable circuit elements. Based on Equations (4-2) and (4-3) and the definition of Equation (4-4), benchmark value, λ, can be expressed as follows:

$$\lambda = \frac{\tau_{MOM,nom}}{\tau_{MOM,test}} \cdot \frac{R_{test}}{R_{nom}} \cdot \frac{(1 + \alpha_{test})}{(1 + \alpha_{nom})} \qquad (4\text{-}5)$$

In a first approximation, it is assumed that the parasitic and systemic errors of an OPAMP are negligible within an acceptable error range. Under this assumption, benchmark value, λ, can be expressed as follows:

$$\lambda \approx \frac{Count_{MOM,nom}}{Count_{MOM,test}} \cdot \frac{R_{test}}{R_{nom}} \qquad (4\text{-}6)$$

In another word, the counter values are proportional to RC time constant so that we can derive Equation (4-7) as follows.

$$\lambda \approx \frac{\tau_{MOM,nom}}{\tau_{MOM,test}} \cdot \frac{R_{test}}{R_{nom}} \qquad (4\text{-}7)$$

Table 4-2 shows Lambda calibration with an external reference which is ideal. Code_T is the best estimation of a capacitor bank code under test with a support of an ideal external reference and an ideal R tuner.

PVT	COUNT (MOM_T)	COUNT (MOM__N)	R_TEST (KΩ)	R_NOM (KΩ)	λ	Code_N	Code_T
TT	237	237	98	98	1.000	44	44
FFHH	175	237	85	98	1.168	44	51
FFHL	175	237	85	98	1.168	44	51
FFCH	179	237	88	98	1.189	44	52
FFCL	179	237	88	98	1.189	44	52
SSHH	304	237	110	98	0.869	44	38
SSHL	304	237	110	98	0.869	44	38
SSCH	316	237	114	98	0.870	44	38
SSCL	317	237	114	98	0.867	44	38

Table 4-2 Lambda Calibration with an external reference

4.2 FM Power Amplifier as Demonstration Vehicle

FM Power Amplifier (FMPA) is an FM transmitter, which transmits 200 KHz FM signal modulated into 76MHz-108MHz frequency band. One of the reasons why we chose FMPA as demonstration vehicle is that it has a resonant tank circuit of high qualify factor so that tuning of a capacitor bank is critical to minimize the output voltage variation across process, temperature and supply voltage variation. Following that, we can compare the difference in capacitor bank tuning between with and without an external precision resistor.

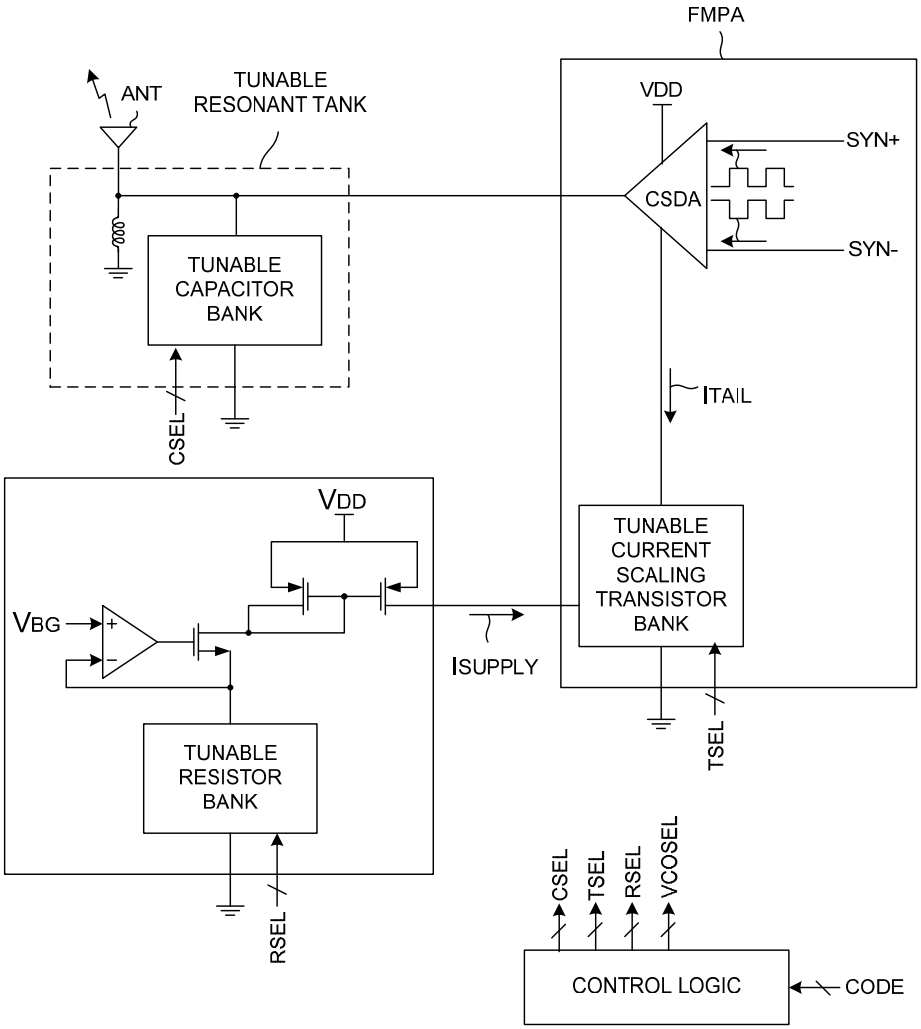

Figure 4-2 Tunable Circuit Blocks in FMPA

4.2.1 Capacitor Bank Tuning

Figure 4-2 shows tunable circuit blocks in FMPA. Tunable circuit blocks include capacitor bank, resistor bank and current scaling transistor bank. We focus on capacitor bank tuning so that

resistor bank was not considered for tuning and current scaling transistor bank was used to provide scaled tail currents. Because the capacitor bank forms a resonant tank circuit of high quality factor, the output voltage of FMPA is much more sensitive to the capacitor bank tuning code than to the resistor bank tuning code.

There are two choices for capacitor bank. One is MOSCAP and the other is RTMOM. We prefer small PVT variation as possible so that MOSCAP is desirable than RTMOM in terms of PVT variation. RTMOM has +/- 15% PVT variation, but MOSCAP has only +/-4% PVT variation assuming Gaussian distribution of 3σ standard deviation.

Process	Typical	Fast	Fast	Slow	Slow
Temperature	55C	110C	-30C	110C	-30C
MOSCAP	0%	+4%	+4%	-4%	-4%
MOMCAP	0%	-15%	-15%	+15%	+15%

Table 4-3 PVT corner variation of MOSCAP and MOMCAP

However, MOSCAP has linearity worse than RTMOM. FMPA harmonic distortion is mostly affected by the non-linearity of capacitor bank. Non-linearity of MOSCAP comes from the fact that the bottom diode of MOSCAP is highly non-linear when the switch for MOSCAP unit is turned off. So it is more desirable to choose MOMCAP to suppress FMPA harmonic distortion than MOSCAP.

4.2.2 FMPA Circuit Topology

The design challenge of FMPA is how we can convert a square waveform into an almost pure sinusoidal waveform as possible. Basically we have to suppress the high order harmonics in the output voltage of the FMPA.

Design of small signal amplifier such as Low Noise Amplifier (LNA) approximates the CMOS device as a linear transconductance (Gm) amplifier. However, design of a large signal amplifier such as Power Amplifier (PA) should not approximate the CMOS device as a linear trans-conductance (Gm) amplifier any longer. With a large swing in the input, the output of the amplifier becomes non-linear. Equation (4-8) shows that the drain current is not linear to Vgs.

$$I = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad (4\text{-}8)$$

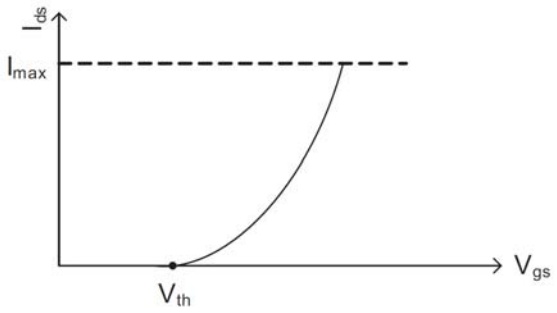

Figure 4-3 Non-linear drain current with large swing in Vgs

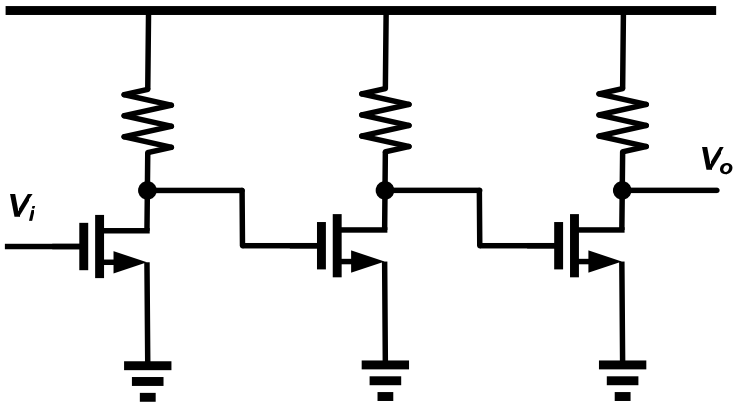

Figure 4-4 Example of Voltage Mode Driving Amplifier

Figure 4-4 illustrates three stage voltage mode driving amplifier. The linearity of each stage is getting worse as the signal level grows up. Basically the non-linearity is regenerated at each stage as we repeat using the non-linear CMOS device as an amplification stage. Voltage mode driving amplifier cannot avoid the problem of non-linearity regeneration.

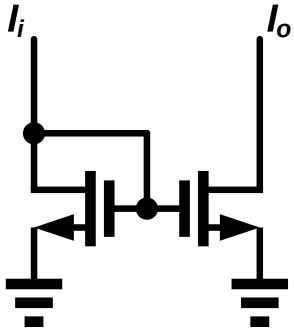

Figure 4-5 Current Amplifier

Figure 4-5 shows a typical implementation of a current source. We can utilize the current source as a linear current amplifier, as long as the device gate voltage remains sufficiently high and Vds is matched. We can make the ratio of the currents programmable so that we can implement a programmable current amplifier. In another word, the current mirror stage behaves as analog pre-distortion stage for the current source stage. The non-linearity of the CMOS device is cancelled out when we use the current amplifier.

The following circuit topology shown in Figure 4-6 is a current mode driving amplifier. It consists of two stages. The first stage is V-to-I converter and the second stage is a filtered current mirror amplifier. Non-linearity is generated once in the first stage, but it is not regenerated in the second stage, because the current amplifier has high linearity in current amplification.

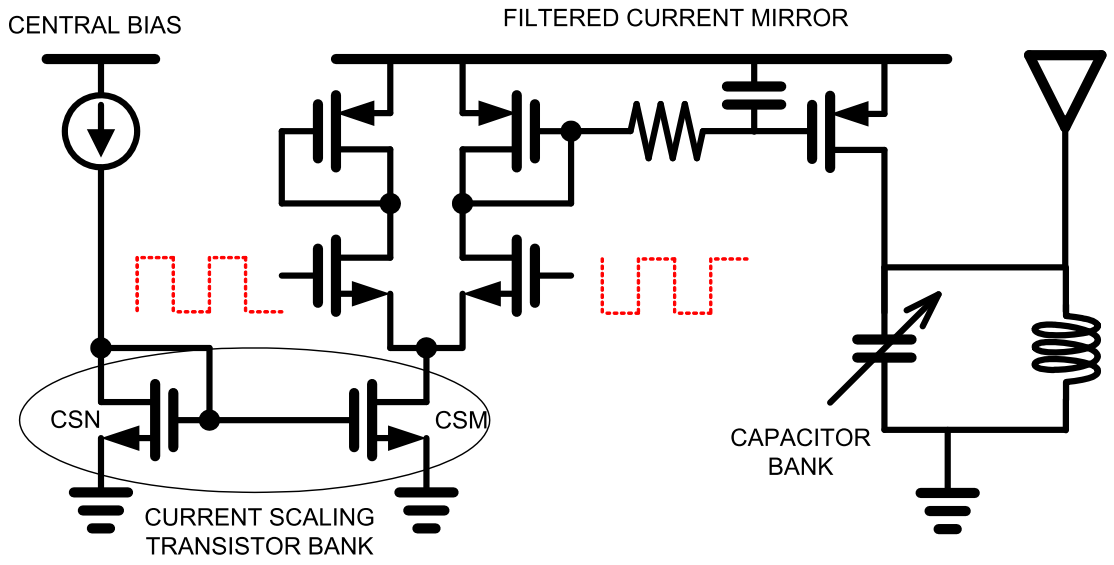

Figure 4-6 Current Mode FMPA

The differential input is a square-wave signal, which is highly non-linear. The first stage converts the square-wave voltage signal into the square wave current signal. From the second stage, we can efficiently suppress high-order harmonics, because the second stage doesn't regenerate additional non-linearity and also we can apply additional filtering function between current mirror and current source.

4.3 Simulation results

The simulation focused on comparison between untuned vs. tuned or tuned with an external reference vs. tuned without an external reference.

4.3.1 Process Corner Definition

There are 9 corners for simulation setup. Typical corner has process corner 1. Fast corner has process corner 2, 3, 4, 5. Slow corner has process corner 6, 7, 8, 9. Typical corner has TT, 55 degree, 1.3V. Fast and Slow corner has FF/SS, 110/-30 degree and 1.365/1.235 V.

Process Corner	MOS	RES	MOMCAP	MOSCAP	Temp	VDD
TT	TT	TT	TT	TT	55	1.3
FFHH	FF	FF	FF	FF	110	1.365
FFHL	FF	FF	FF	FF	110	1.235
FFCH	FF	FF	FF	FF	-30	1.365
FFCL	FF	FF	FF	FF	-30	1.235
SSHH	SS	SS	SS	SS	110	1.365
SSHL	SS	SS	SS	SS	110	1.235
SSCH	SS	SS	SS	SS	-30	1.365
SSCH	SS	SS	SS	SS	-30	1.235

Table 4-4 Process corner definition

4.3.2 Harmonic Distortion and Calibration Effect

The blue line of Figure 4-7 is the harmonic distortion specification mask. The first harmonic tone is the primary signal tone of 92 MHz 112 dBuVrms. The corner simulation results for 92 MHz 112dBuVrms in Figure 4-7 clearly demonstrates that they could not meet the harmonic distortion specification for all process corners without calibration of the capacitor bank.

The capacitor tuning is helpful to reduce the output voltage variation of the first harmonic tones across process corners, but it is not helpful to reduce high-order harmonic tones, because the resonant tank circuitry has a primary function to filter the first harmonic, not the high-order harmonic tones. Following that, Figure 4-8 and 4-9 show more suppression in high-order

harmonic distortions (dBc), because the primary tone at 92MHz is increased after calibration of the capacitor bank but high-order harmonic tones stay almost same.

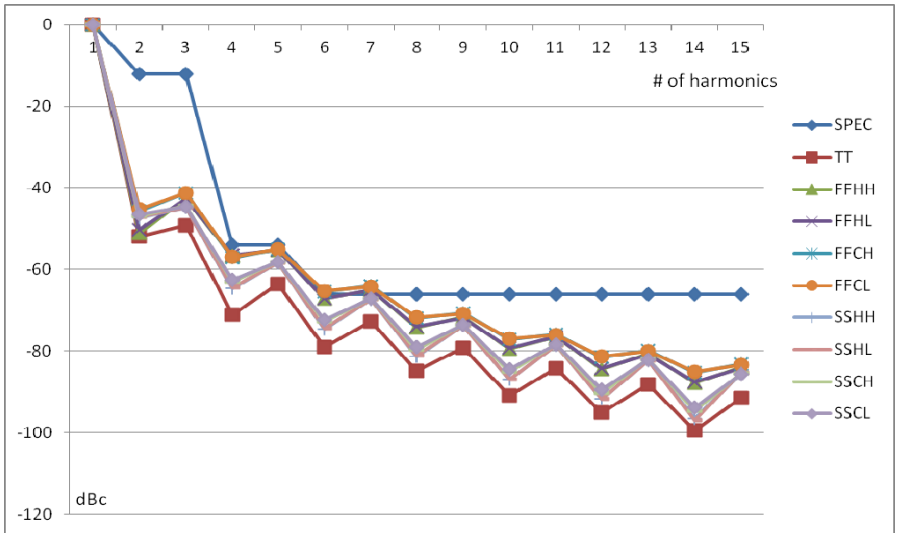

Figure 4-7 Harmonic distortions untuned for 92 MHz 112 dBuVrms output voltage

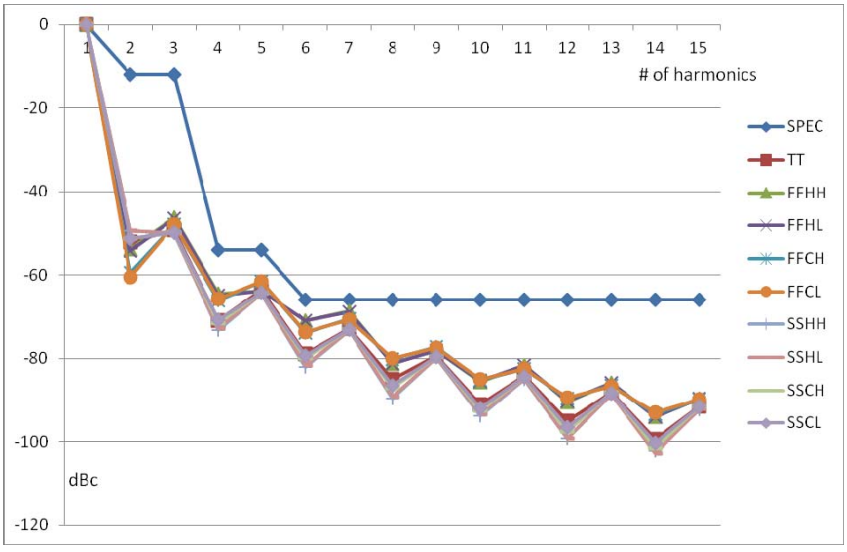

Figure 4-8 Harmonic distortions tuned with external reference resistor

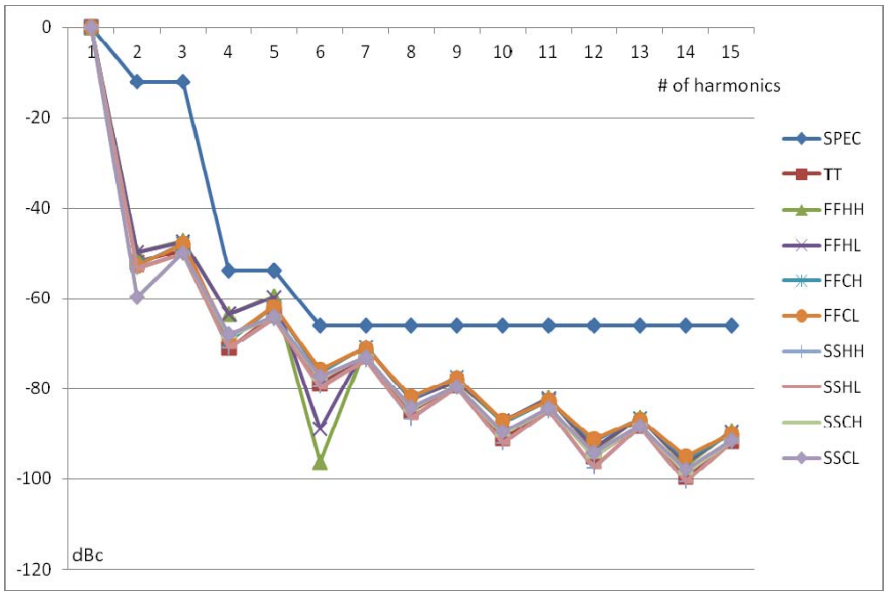

Figure 4-9 Harmonic distortions tuned without external reference resistor

4.3.3 Output Voltage (Fundamental Tone) Variation

Table 4-5 shows the comparison between tuned and untuned. Of course, the tuned case is better than the untuned case. However, the tuned case with an R tuner with an ideal external precision resistor has no benefit compared with the tuned case without an external reference. Elimination of an external precision resistor doesn't degrade the performance, because parasitic and systemic errors of OPAMP in RCMM are cancelled in λ calibration without an external reference, but parasitic and systemic errors of OPAMP in RCMM cannot be cancelled in the case with an external reference. This demonstrates the power of on-chip benchmarking and λ calibration without an external reference.

	TT	FFHH	FFHL	FFCH	FFCL	SSHH	SSHL	SSCH	SSCL	MAX	MIN	Variation
Untuned	112.71	106.59	106.22	107.43	107.04	104.63	104.25	104.97	104.64	112.71	104.25	8.46
Tuned w/ ext ref	112.71	111.59	111.21	113.44	113.03	111.38	110.93	111.64	111.21	113.44	110.93	2.50
Tuned w/o ext ref	112.71	111.91	111.53	113.72	113.31	111.55	111.12	111.58	111.17	113.72	111.12	2.60

Table 4-5 Output voltage variation of 92MHz 112dBuVrms

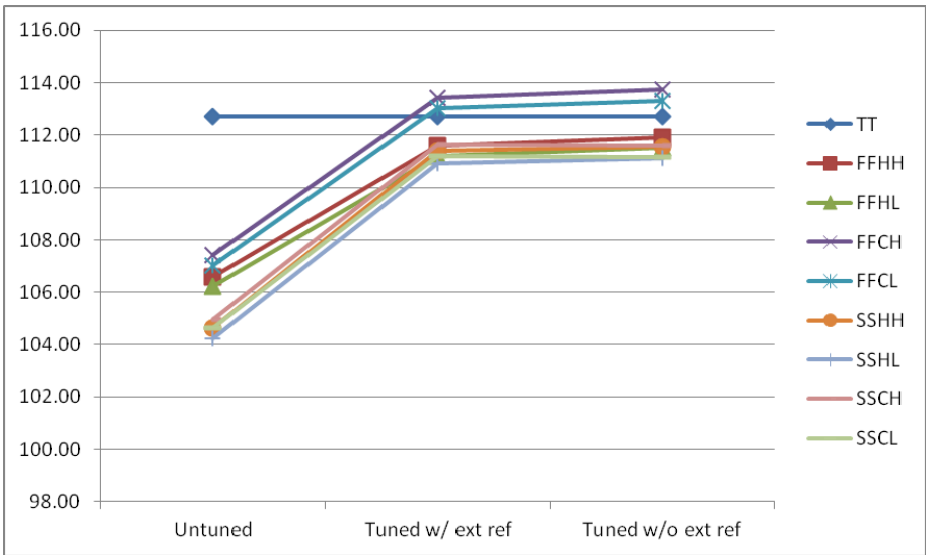

Figure 4-10 Output voltage variation of 92MHz 112dBuVrms

4.3.4 Analysis of Error Sources

Table 4-6 shows that without on-chip resistance calibration, RC tuner is not useful to tune on-chip capacitance, because on-chip resistance has high sensitivity to the process variations. Without an external reference resistor, it would be difficult to tune on-chip resistance. Then how can we tune on-chip capacitance such MOS capacitor without tuning on-chip resistance?

PVT	R (KΩ)	Normalized	Error (%)
TT	98.46	1.000	0.0
FFHH	84.95	0.863	-13.7
FFHL	84.95	0.863	-13.7
FFCH	88.43	0.898	-10.2
FFCL	88.43	0.898	-10.2
SSHH	109.70	1.114	11.4
SSHL	109.70	1.114	11.4
SSCH	114.23	1.160	16.0
SSCL	114.23	1.160	16.0

Table 4-6 On-chip resistance variation without tuning

Table 4-7 shows that there are parasitic and systemic errors in RCMM. The parasitic and systemic errors are roughly 25%. There is high correlation between the error for MOM capacitors and the error for MOS capacitors.

PVT	1+α_MOM	Error (%)	1+α_MOS	Error (%)
TT	1.247	24.7	1.234	23.4
FFHH	1.256	25.6	1.262	26.2
FFHL	1.256	25.6	1.262	26.2
FFCH	1.234	23.4	1.217	21.7
FFCL	1.234	23.4	1.223	22.3
SSHH	1.248	24.8	1.223	22.3
SSHL	1.248	24.8	1.228	22.8
SSCH	1.246	24.6	1.203	20.3
SSCL	1.250	25.0	1.218	21.8

Table 4-7 Parasitic and systemic errors in RCMM

Table 4-8 and Equation (4-9) show that the normalized relative error terms are effectively cancelled out. This error term is comparable to the variation of the external precision resistor and the variation of R tuner on-chip.

$$\frac{\tau_{MOM}}{\tau_{MOS}} = \frac{R_{MOM}C_{MOM}}{R_{MOS}C_{MOS}} \frac{(1+\alpha_{MOM})}{(1+\alpha_{MOS})} = \frac{COUNT_{MOM}}{COUNT_{MOS}} \qquad (4\text{-}9)$$

PVT	COUNT C_MOM	COUNT C_MOS	R (KΩ)	C_MOM (pF)	C_MOS (pF)	1+α_MOM	1+α_MOS	(1+α_MOM) /(1+α_MOS)	Normalized	Error (%)
TT	237	211	98	1.00	0.90	1.247	1.234	1.011	1.000	0.0
FFHH	175	193	85	0.85	0.93	1.256	1.262	0.995	0.984	-1.6
FFHL	175	193	85	0.85	0.93	1.256	1.262	0.995	0.984	-1.6
FFCH	179	195	88	0.85	0.94	1.234	1.217	1.014	1.003	0.3
FFCL	179	196	88	0.85	0.94	1.234	1.223	1.009	0.998	-0.2
SSHH	304	223	110	1.15	0.86	1.248	1.223	1.021	1.010	1.0
SSHL	304	224	110	1.15	0.86	1.248	1.228	1.016	1.006	0.6
SSCH	316	230	114	1.15	0.87	1.246	1.203	1.036	1.025	2.5
SSCL	317	233	114	1.15	0.87	1.250	1.218	1.026	1.015	1.5

Table 4-8 Cancellation of parasitic and systemic errors in RCMM

Dividing Equation (4-10) by Equation (4-11), the relative error terms, which have α, are cancelled out and the on-chip resistance values for MOM capacitors and MOS capacitors are cancelled out with an engineering tolerance. Test on-chip capacitance value of MOS capacitor is also cancelled out with nominal on-chip capacitance value of MOS capacitor. From Equations (4-12) and (3-10), we reach Equation (4-13).

$$\frac{(1+\alpha_{MOM,test})}{(1+\alpha_{MOS,test})} = \frac{COUNT_{MOM,test}}{COUNT_{MOS,test}} \frac{R_{MOS,test}C_{MOS,test}}{R_{MOM,test}C_{MOM,test}} \qquad (4\text{-}10)$$

$$\frac{(1+\alpha_{MOM,nom})}{(1+\alpha_{MOS,nom})} = \frac{COUNT_{MOM,nom}}{COUNT_{MOS,nom}} \frac{R_{MOS,nom}C_{MOS,nom}}{R_{MOM,nom}C_{MOM,nom}} \quad (4\text{-}11)$$

$$1 \cong \frac{COUNT_{MOM,nom}}{COUNT_{MOM,test}} \frac{COUNT_{MOS,test}}{COUNT_{MOS,nom}} \frac{C_{MOM,test}}{C_{MOM,nom}} \quad (4\text{-}12)$$

$$\lambda = \frac{C_{MOM,nom}}{C_{MOM,test}} \cong \frac{COUNT_{MOM,nom}}{COUNT_{MOM,test}} \frac{COUNT_{MOS,test}}{COUNT_{MOS,nom}} \quad (4\text{-}13)$$

4.3.5 Gain code sweep

We swept gain code from 0 to 255 at 92 MHz and TT. Figure 4-11 shows that the signals below 1 GHz are proportional to the gain code, but the signals from 2GHz to 3GHz do not change with gain code. The signals from 2GHz to 3 GHz should be treated as the leakage tones from parasitics and GND networks.

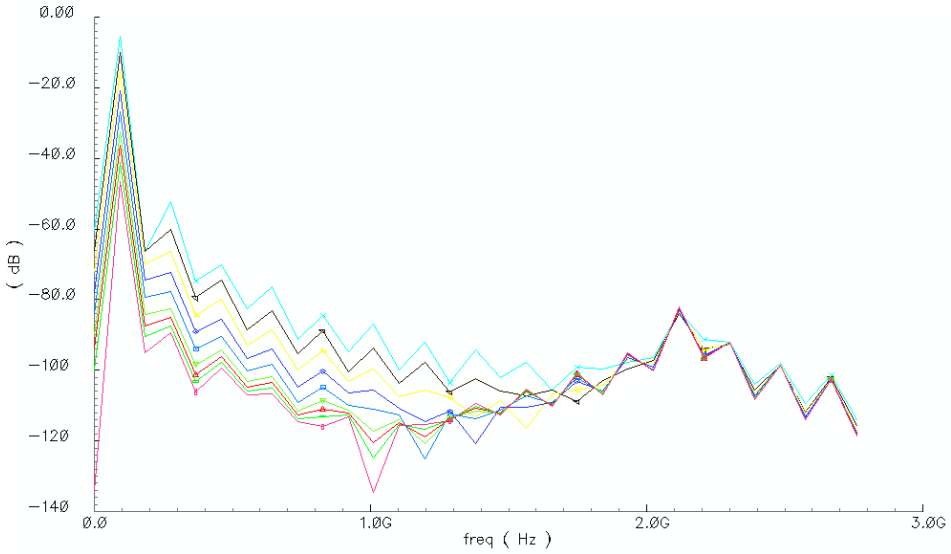

Figure 4-11 Output voltage spectrum with gain code sweep (0~255)

5 Measurement

5.1 Measurement Method

The harmonic distortions from FMPA are hard to detect with a conventional approach so that we need to develop a measurement method to detect the harmonic distortions through a spectrum analyzer.

5.1.1 Test Board

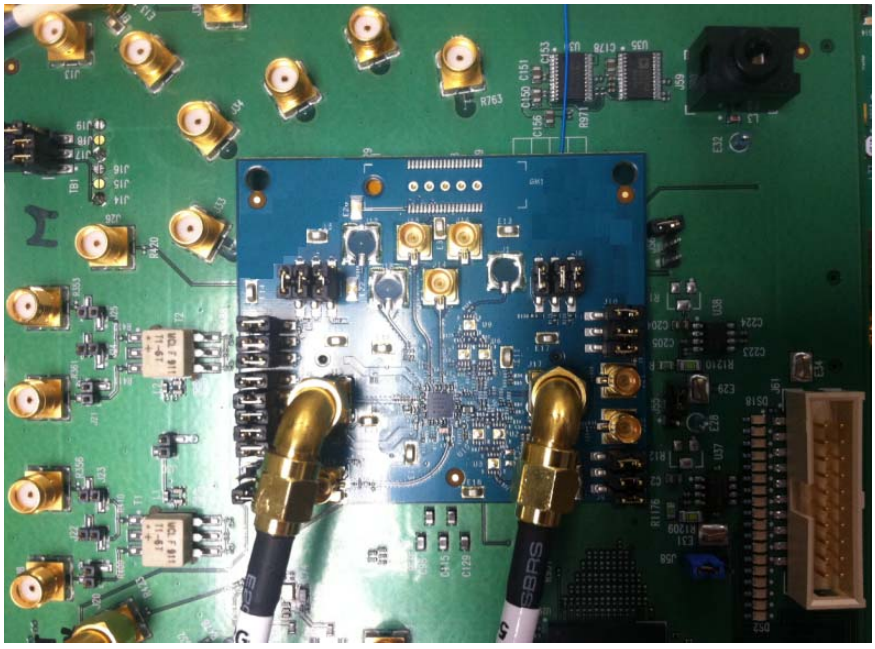

Figure 5-1 Test board for RCMM and FMPA

Figure 5-1 shows a test board for RCMM and FMPA. The test chip has flip-chip balls which were soldered down on the test board. Through the cable on the right in the Figure 5-1, an external clock source is fed into the test chip to provide a 19.2 MHz reference clock for PLL in the test chip. Through the cable on the left in the Figure 5-1, the output of FMPA is fed into a spectrum analyzer.

5.1.2 Resistor Divider Measurement Method

A conventional measurement method used the resistive divider between Rtest and 50 Ω. When Rtest = 5 KΩ, we attenuate 40 dB from the output voltage. However, Rtest still degrades the quality factor of the tank of FMPA and causes inaccuracy in output voltage measurement of FMPA. If we use Rtest = 50 KΩ in order not to degrade the quality factor of the tank of FMPA, the attenuation is 60 dB so that we may experience harmonic distortions in high frequency fall below the bottom floor of the measured spectrum through a spectrum analyzer.

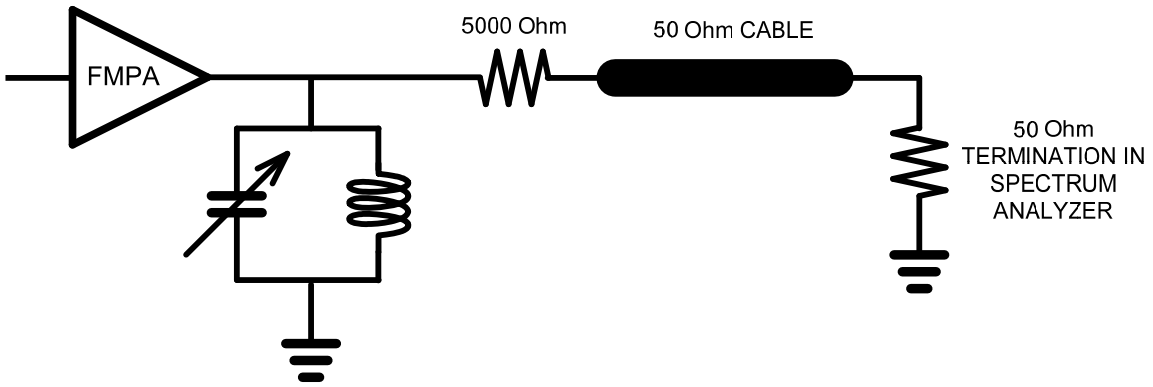

Figure 5-2 Measurement through resistor divider

5.1.3 High Pass Filter Measurement Method

We developed high pass filter measurement method. The external 1 pF capacitor has almost constant capacitance and 50 Ω from spectrum analyzer is also almost constant resistance value. 1 pF in series with 50 Ω at 92 MHz has an effective resistance of 60 KΩ in parallel with 1 pF so that degradation of quality factor is not a problem. Also the nature of high pass filter is good to characterize the high-order harmonics with less attenuation than low frequency. We calculate the frequency dependent attenuation factor and we can derive the output voltage from both the measured voltage from a spectrum analyzer and the attenuation factor. The attenuation factor is deterministic once the input frequency is identified.

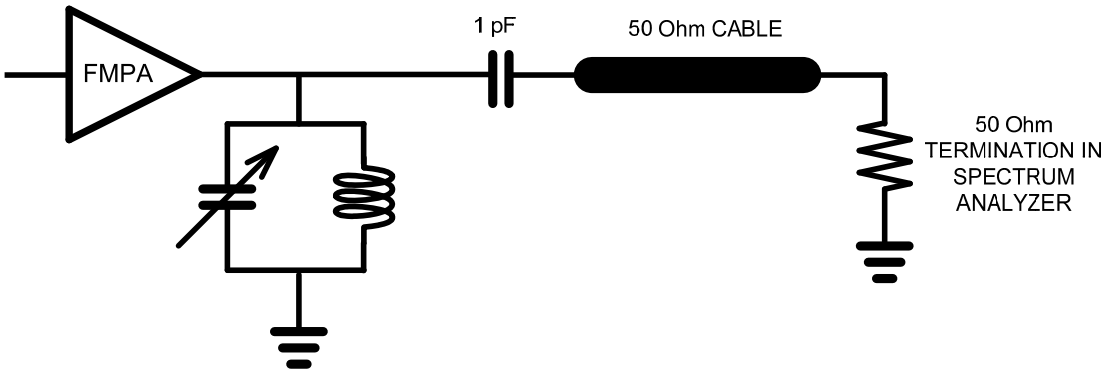

Figure 5-3 Measurement through high pass filter

Figure 5-4 shows the measured spectrum from a spectrum analyzer. The first harmonic has 80.19 dBuVrms and the HPF attenuation factor is -30.79 dB. The output voltage at 92 MHz can be derived by adding 80.19 dBuVrms and 30.79 dB so that it becomes 110.98 dBuVrms.

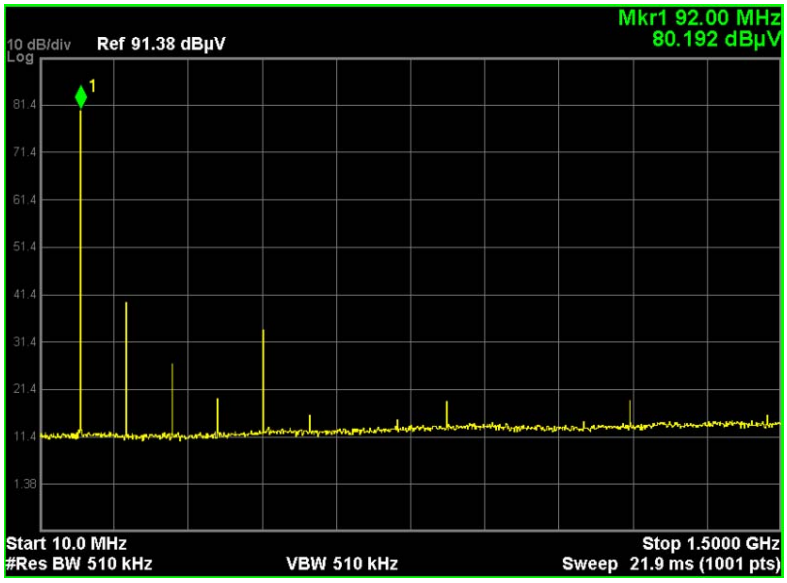

Figure 5-4 Measured spectrum for 92 MHz harmonics

Frequency MHz	Harmonic #	HPF Attenuation	Measured Data	Output Voltage (dBuVrms)
92	1	-30.79	80.19	110.98
184	2	-24.78	32.47	57.25
276	3	-21.27	38.30	59.57
368	4	-18.80	22.30	41.10
460	5	-16.89	27.47	44.36
552	6	-15.35	12.80	28.15
644	7	-14.05	22.30	36.35
736	8	-12.95	6.63	19.58
828	9	-11.98	16.97	28.95
920	10	-11.13	7.63	18.76
1012	11	-10.37	14.30	24.67
1104	12	-9.69	16.80	26.49
1196	13	-9.08	12.13	21.21
1288	14	-8.52	9.13	17.65
1380	15	-8.01	10.63	18.64

Table 5-1 Output voltage calculation using HPF Attenuation factor

5.2 Measurement Results

5.2.1 Harmonic Distortions of 112 dBuVrms output voltage

The blue lines in Figures 5-5 through 5-10 are harmonic distortion specification mask. With 112 dBuVrms output voltage level, some harmonic distortions violate the harmonic distortion specification mask for untuned cases, but all harmonic distortions for tuned cases are below the harmonic distortion specification mask across all PVT corners. This matches simulation results for tuned and untuned cases.

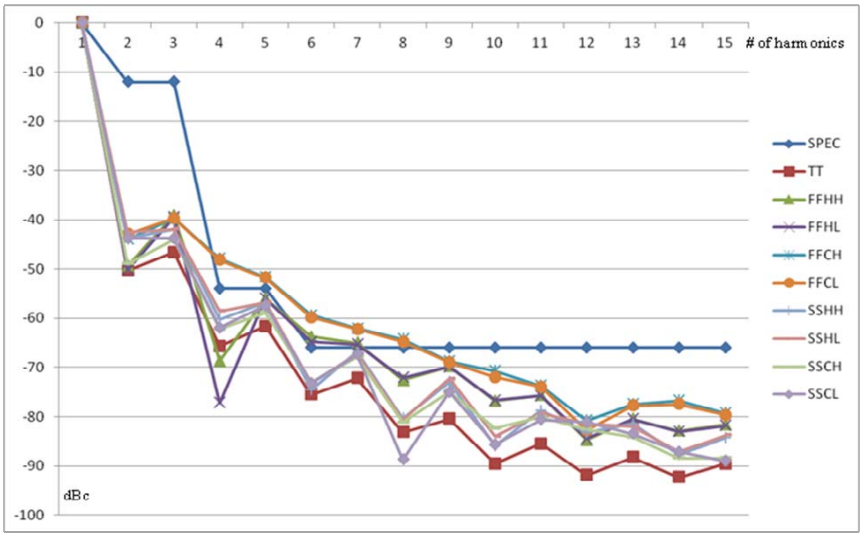

Figure 5-5 Harmonic distortions (untuned) for 112 dBuVrms at 76 MHz

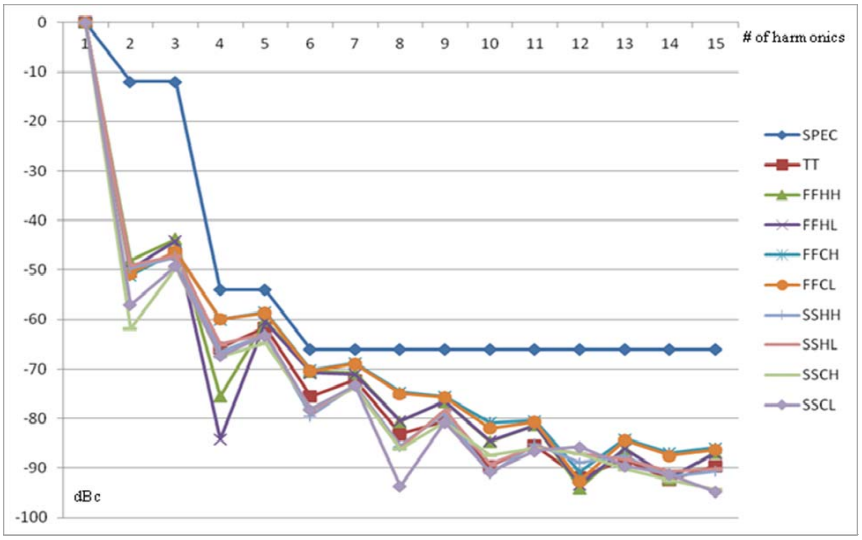

Figure 5-6 Harmonic distortions (tuned) for 112 dBuVrms at 76 MHz

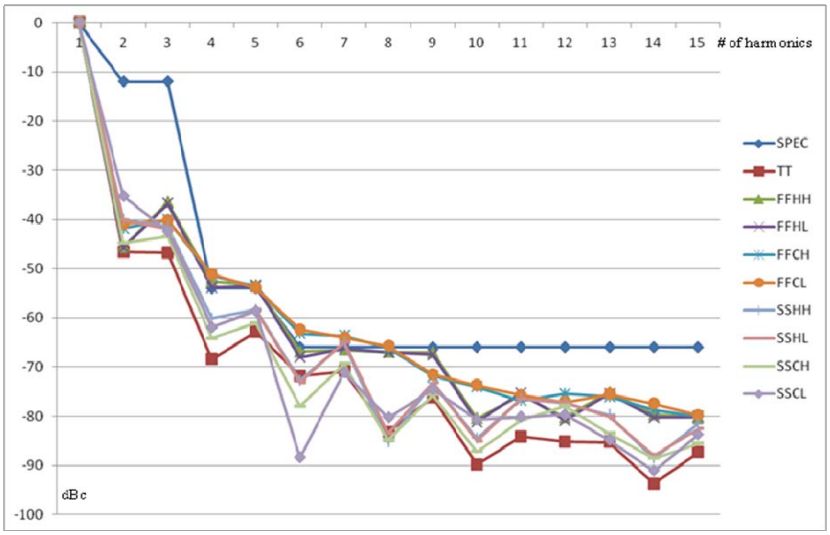

Figure 5-7 Harmonic distortions (untuned) for 112 dBuVrms at 92 MHz

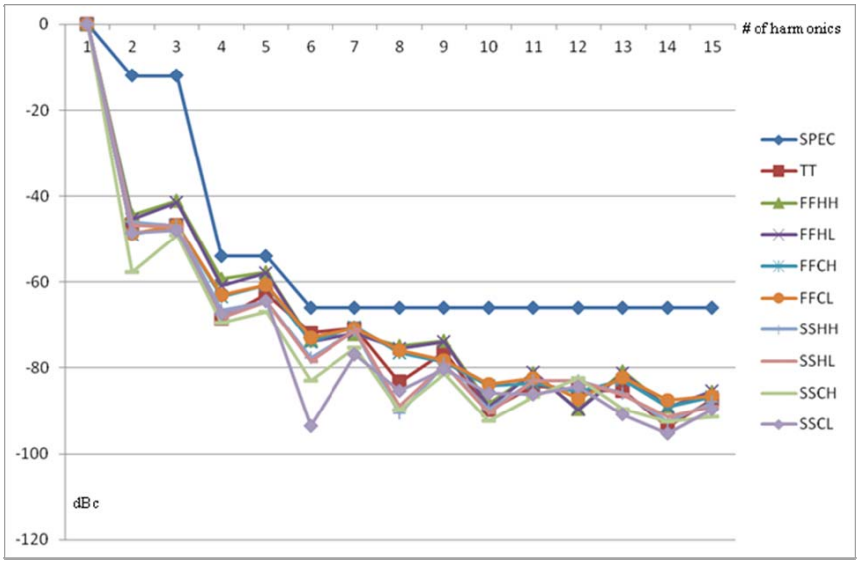

Figure 5-8 Harmonic distortions (tuned) for 112 dBuVrms at 92 MHz

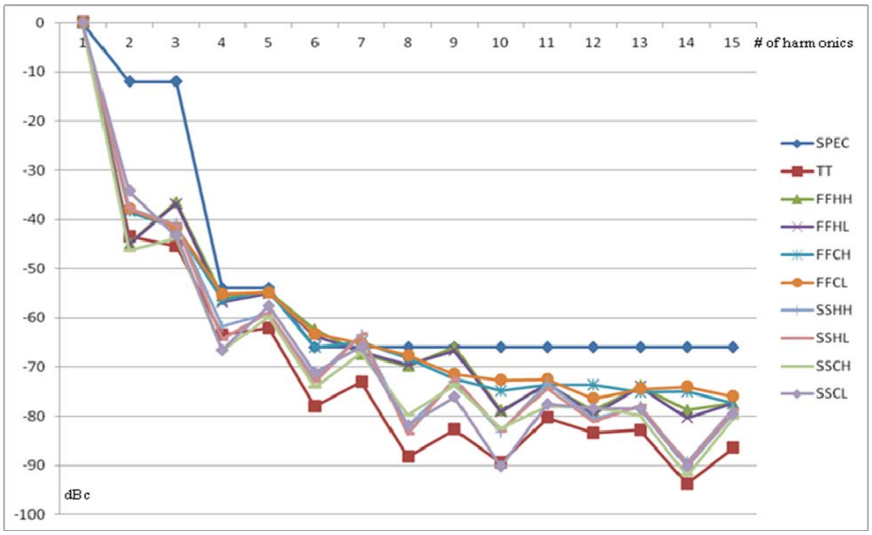

Figure 5-9 Harmonic distortions (untuned) for 112 dBuVrms at 108 MHz

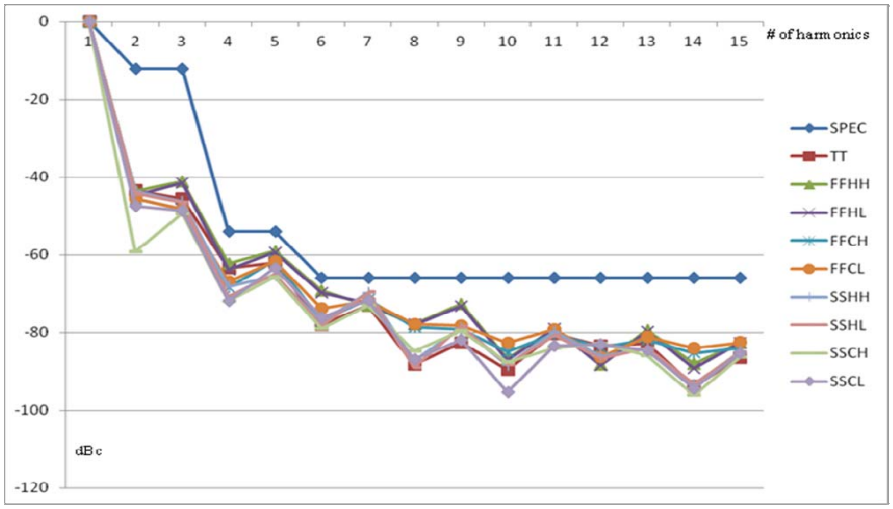

Figure 5-10 Harmonic distortions (tuned) for 112 dBuVrms at 108 MHz

5.2.2 Harmonic Distortions of 117 dBuVrms output voltage

The blue lines in Figures 5-11, 5-12, 5-13 are harmonic distortion specification mask. With 117 dBuVrms output voltage level at 76 MHz, 92 MHz and 108 MHz, some harmonic distortions violated the harmonic distortion specification mask across all PVT corners. The ESD diodes are turned on for 117 dBuVrms output voltage so that the non-linearity of ESD diodes increased harmonic distortions of FMPA. In another reason, the output voltage becomes saturated with 117 dBuVrms and above output voltages so that non-linearity is added toward higher output voltages.

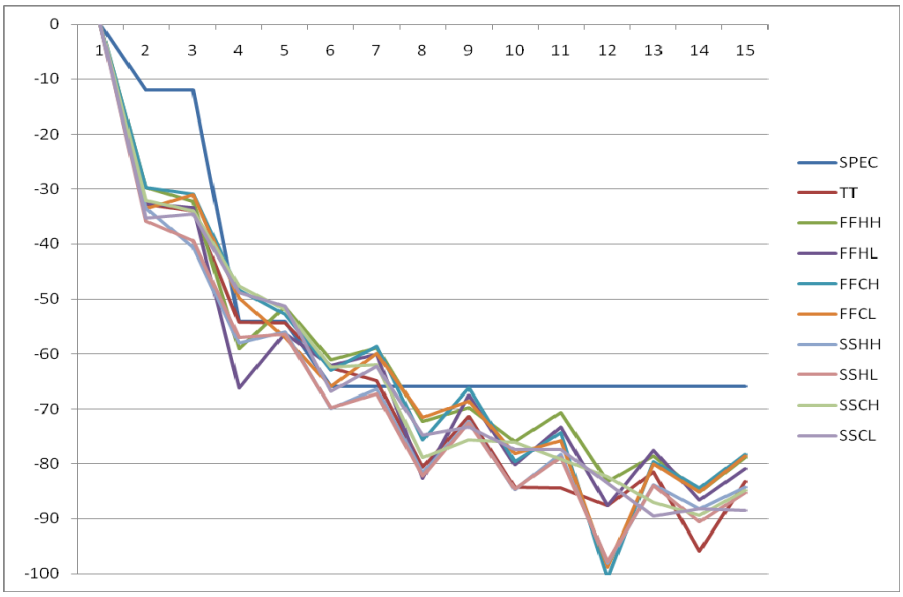

Figure 5-11 Harmonic distortions (tuned) for 117 dBuVrms at 76 MHz

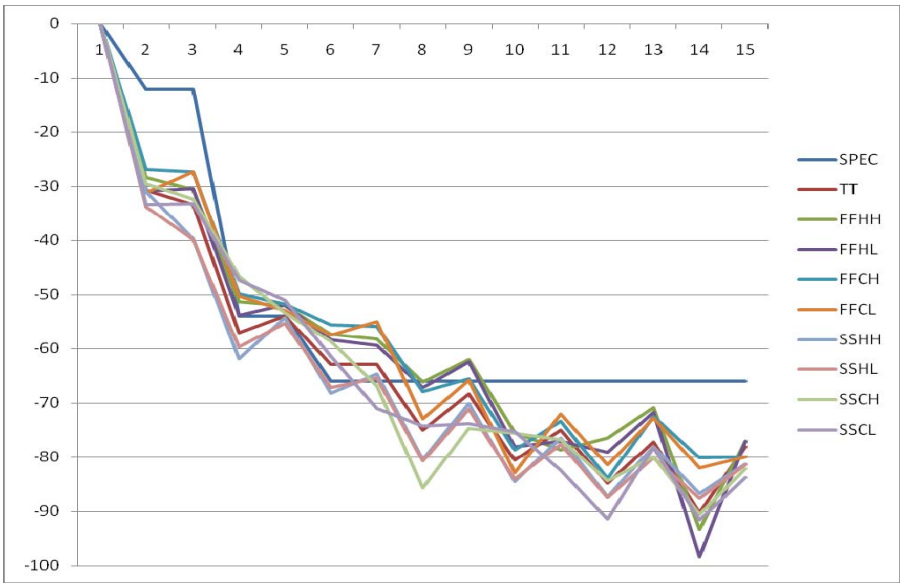

Figure 5-12 Harmonic distortions (tuned) for 117 dBuVrms at 92 MHz

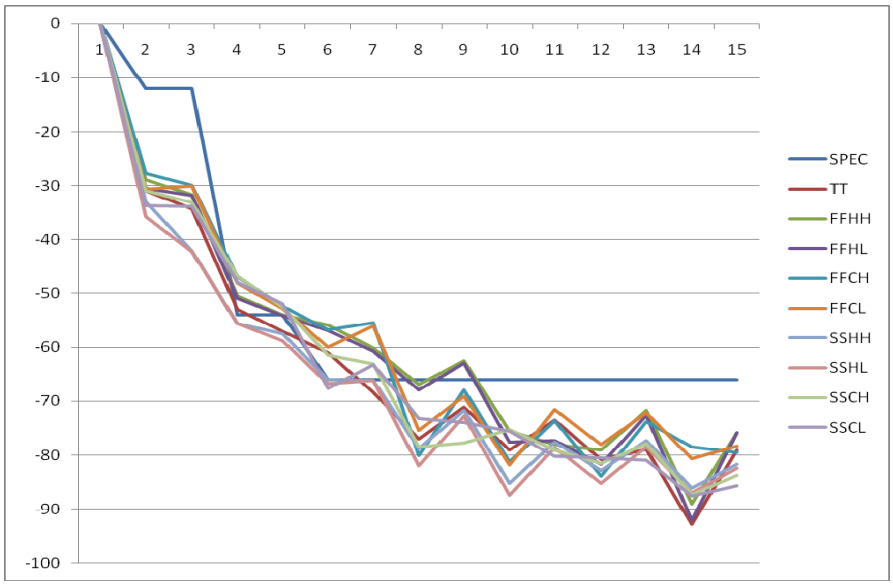

Figure 5-13 Harmonic distortions (tuned) for 117 dBuVrms at 108 MHz

5.2.3 Output Voltage (Fundamental Tone) Variation

The following table shows λ calibration of capacitor bank tuning codes. Measured counter values from RCMM were used to compute λ from Equation (4-13). We calculate capacitor bank tuning codes under test from Equation (3-19).

	TT	FFHH	FFHL	FFCH	FFCL	SSHH	SSHL	SSCH	SSCL
MOMCAP_T	267	223	223	226	225	307	308	317	318
MOMCAP_N	237	237	237	237	237	237	237	237	237
MOSCAP_T	216	210	210	206	206	245	245	247	249
MOSCAP_N	211	211	211	211	211	211	211	211	211
λ	0.909	1.058	1.058	1.024	1.028	0.896	0.893	0.875	0.880
Ctune_N (76 MHz)	81	81	81	81	81	81	81	81	81
Ctune_T (76 MHz)	74	86	86	83	83	73	72	71	71
Ctune_N (92 MHz)	44	44	44	44	44	44	44	44	44
Ctune_T (92 MHz)	40	47	47	45	45	39	39	39	39
Ctune_N (108 MHz)	21	21	21	21	21	21	21	21	21
Ctune_T (108 MHz)	19	22	22	22	22	19	19	18	18

Table 5-2 λ calibration of capacitor bank tuning codes

The following table shows output voltage (fundamental tone) variations comparing between untuned and tuned for 112 uVdBrms and 117 uVdBrms output voltages. In case of 112 dBuVrms the λ tuning effect is clear because the output voltage level is not saturated. In case of 117 dBuVrms output voltage, the tuning effect diminishes because the output voltage level is already saturated and ESD diodes are turned on.

	TT	FFHH	FFHL	FFCH	FFCL	SSHH	SSHL	SSCH	SSCL	MAX	MIN	Variation
Untuned (76MHz)	112.02	109.2535	108.9135	109.4435	108.9735	103.5735	104.0735	105.7435	105.2435	112.02	103.57	8.45
Tuned (76MHz)	112.02	110.50	110.21	110.54	110.13	108.57	109.07	110.74	110.24	112.02	108.57	3.45
Untuned (92MHz)	112	109.4851	109.1451	110.3451	109.9151	104.4151	103.9151	107.0851	106.5851	112.00	103.92	8.08
Tuned (92MHz)	112	109.92	109.60	111.05	110.62	108.59	108.26	111.42	110.76	112.00	108.26	3.74
Untuned (108MHz)	112.03	109.2538	108.8738	110.1138	109.6638	106.2238	105.5638	110.36	109.5238	112.03	105.56	6.47
Tuned (108MHz)	112.03	109.52	109.17	111.20	110.75	109.36	108.86	110.36	110.02	112.03	108.86	3.17
	TT	FFHH	FFHL	FFCH	FFCL	SSHH	SSHL	SSCH	SSCL	MAX	MIN	Variation
Untuned (76MHz)	117.01	115.6535	115.2635	116.8635	116.5135	114.6135	113.7735	116.4435	115.7735	117.01	113.77	3.24
Tuned (76MHz)	117.01	115.72	115.34	116.94	116.62	115.94	115.27	117.44	116.94	117.44	115.27	2.17
Untuned (92MHz)	117	115.4451	115.0651	116.8151	116.4651	115.2851	114.6151	116.9551	116.6151	117.00	114.62	2.38
Tuned (92MHz)	117	115.44	115.05	116.83	116.49	115.96	115.46	117.62	116.96	117.62	115.05	2.57
Untuned (108MHz)	117	114.8038	114.4538	116.6238	116.3338	114.5638	114.2238	116.7238	116.3938	117.00	114.22	2.78
Tuned (108MHz)	117	114.80	114.45	116.67	116.39	115.22	114.56	117.06	116.89	117.06	114.45	2.61

Table 5-3 Output voltage variation between untuned vs. tuned

Figures 5-14 and 5-15 explain tuning effect pictorially. For example, we can notice the untuned output voltage variation for 76 MHz, 112 dBuVrms is bigger than the tuned output voltage variation for 76 MHz, 112 dBuVrms. However, we can not tell the difference between untuned and tuned output voltage variations for 76 MHz, 117 dBuVrms.

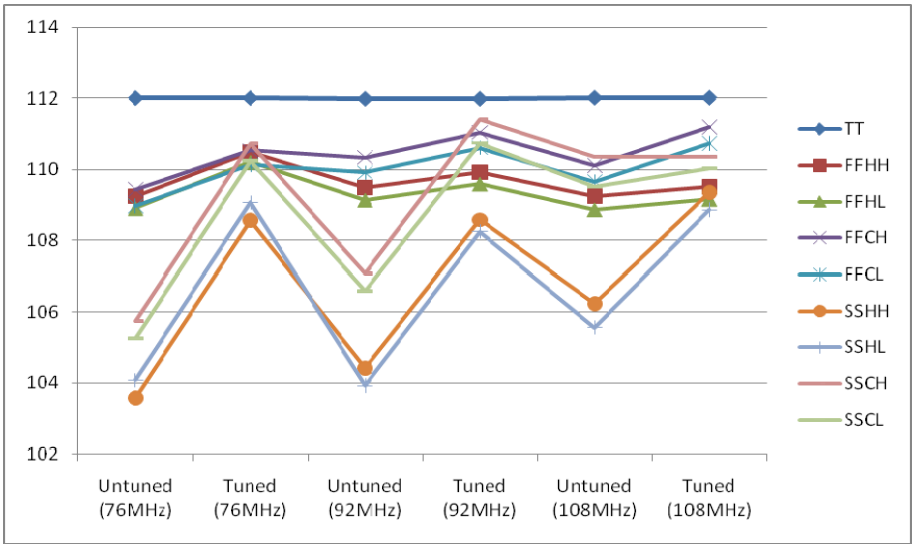

Figure 5-14 Output voltage (fundamental tone) variation for 112 dBuVrms

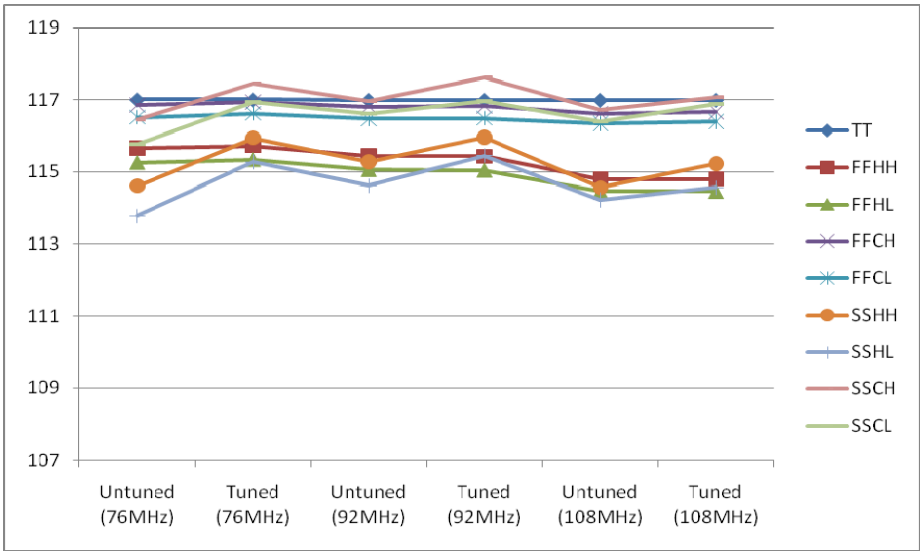

Figure 5-15 Output voltage (fundamental tone) variation for 117 dBuVrms

5.2.4 Qualify Factor Measurement

We performed frequency sweep to measure the quality factor of the resonant tank of FMPA. By setting up CSM/CNS ratio, we can boost the output currents by CSM/CSN.

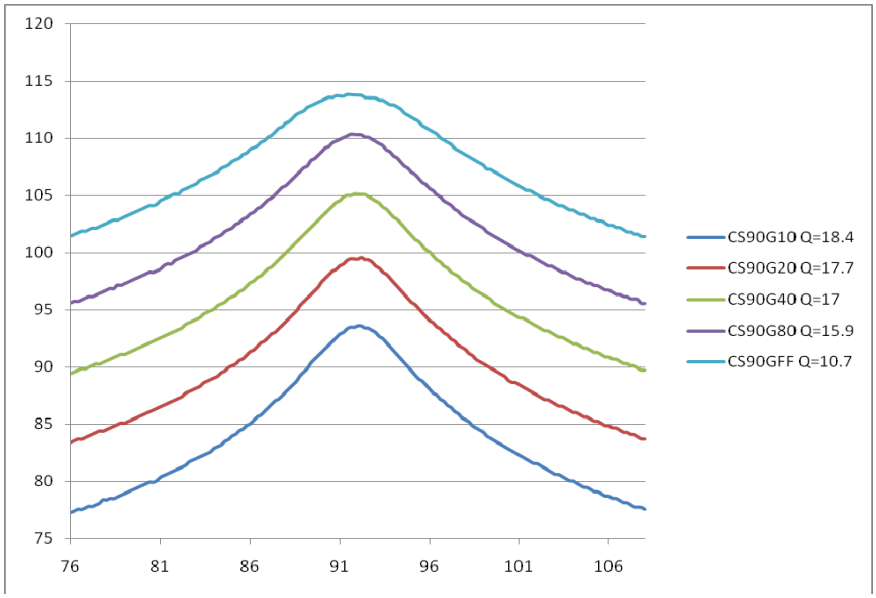

Figure 5-16 Frequency sweep from 76 to 108 MHz with CSM/CSN=16/4

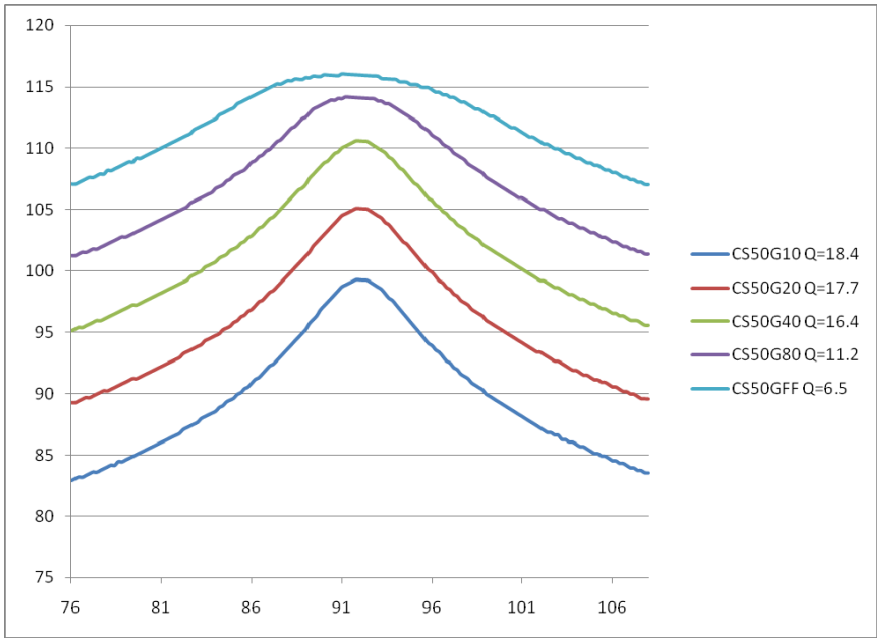

Figure 5-17 Frequency sweep from 76 to 108 MHz with CSM/CSN=16/2

With more output currents, we can boost the output voltages, but the boosting effect diminishes when the output voltages reach the saturated output voltage levels.

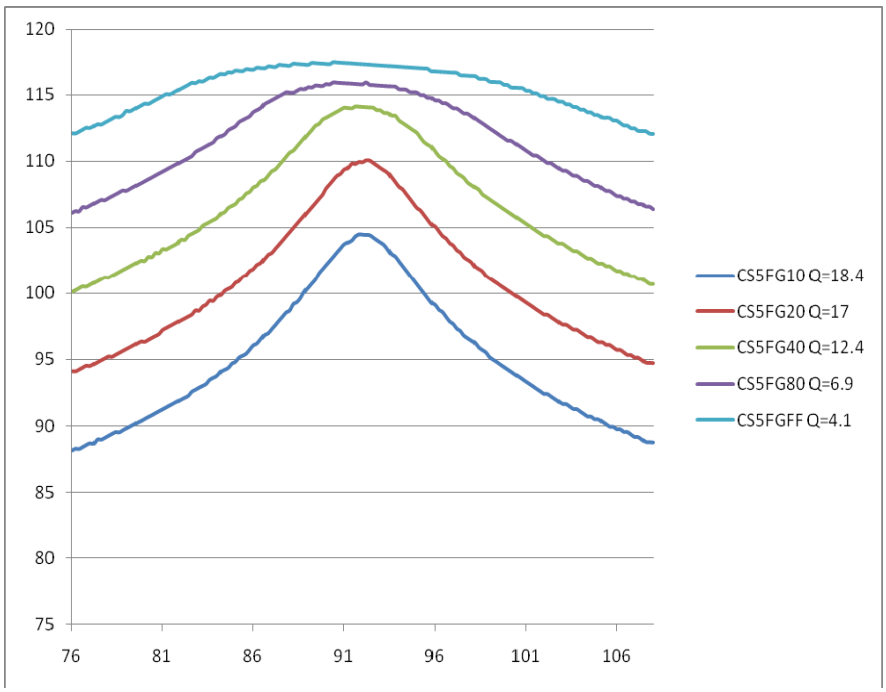

Figure 5-18 Frequency sweep from 76 to 108 MHz with CSM/CSN=31/2

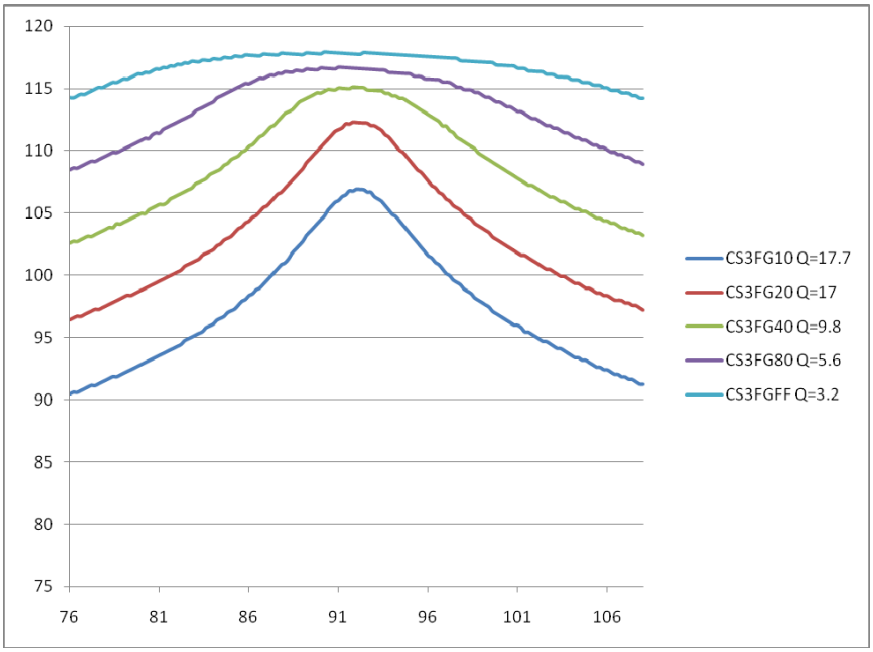

Figure 5-19 Frequency sweep from 76 to 108 MHz with CSM/CSN=31/1

6 Conclusion

6.1 Summary

We can substitute internal reference component for an external reference resistor, which occupies space in mobile devices. The internal reference component is less sensitive to PVT variations. We can eliminate an external reference resistor without degrading harmonic distortion and output voltage variation in FMPA by sharing on-chip resistance when measuring RC time constants for MOMCAP and MOSCAP.

This work introduced a new way to calibrate on-chip resistance and capacitance without the external reference resistors. An integrated circuit includes a benchmarking circuitry and a tunable circuitry. The benchmarking circuit includes a target component and an internal reference component. The internal reference component exhibits a lower sensitivity to the changes in test conditions than the target component. Benchmarking Metric Measurement Module (BMMM) measures benchmarking metrics for the internal reference component and the target component. A benchmark value is calculated based on the benchmarking metrics.

The novelty of this work is the powerful way to cancel the parasitic and systemic errors caused by operational amplifiers in RC tuner circuitry. We can generalize the theory of benchmarking broadly applicable to RF and analog circuits that need the calibration of tunable circuit elements without external references.

6.2 Future Work

The external crystal oscillator has been used as critical timing reference circuit. The external crystal oscillator may be replaced by the on-chip oscillators including on-chip inductors. The on-chip inductors are very good candidates for internal reference components. Recently there was a trial to replace crystal oscillators by LC oscillators [36]. However, the area of LC oscillator is 400 um X 550 um. The area is not small so that it may be another bottleneck for the practical use on chip. One of the ideas is to use 60 GHz inductor to implement LC oscillators to replace crystal oscillators. 60 GHz inductor occupies small area so that the total area for LC oscillator may only consume 100 um X 100 um, which is more feasible for the practical use on chip.

Bibliography

[1] Cheol-Woong Lee and Sunghyun Park, "IC Component Benchmarking Without External References," IDF #092889, February 11, 2010 (filed for patent)

[2] Cheol-Woong Lee, Sunghyun Park and Jonghoon Choi, "Current Mode Power Amplifier Providing Harmonic Distortion Suppression," IDF #101019, November 15, 2010 (filed for patent)

[3] Peyton Z. Peebles, JR., "Probability, Random Variables, and Radom Signal Principles," McGRAW-HILL, 1993

[4] G. R. Hykes and D. E. Newell, "A temperature-compensated frequency standard," Proc. 15th AFCS, May 1961, pp. 297-317.

[5] D. E. Newell, H. Hinnah, and R. Bangert, "Advances in crystal oscillator and resonator compensation," Proc. 18th AFCS, May 1964, pp. 487-534.

[6] D. E. Newell and H. Hinnah, "A report on TCXO's and segmented compensation," Proc. 23rd AFCS, May 1969, pp. 187-191.

[7] S. Schodowski, "A new approach to a high stability temperature compensated crystal oscillator," Proc. 24th AFCS, April 1970, pp. 200-208.

[8] P. C. Duckett. R. J. Peduto. and G. V. Chizak, "Temperature compensated crystal oscillators," Proc. 24th AFCS, April 1970, pp. 191-199.

[9] G. E. Buroker and M. E. Frerking, "A digitally compensated TCXO," Proc. 27th AFCS, June 1973, pp. 191-198.

[10] D. L. Thomann, "A microcircuit temperature compensated crystal oscillator (MCTCXO)," Proc. 28th AFCS, May 1974, pp. 214-220.

[11] B. Mroch and G. R. Hykes, "A miniature high stability TCXO using digital compensation,'' Proc. 30th AFCS, June 1976, pp. 292-300.

[12] R. J. Widlar, "New developments in IC voltage regulators," IEEE J. Solid-State Circuits, vol. SC-6, pp. 2–7, Feb. 1971.

[13] A. P. Brokaw, "A simple three terminal IC bandgap reference," IEEE J. Solid-State Circuits, vol. SC-9, pp. 388–393, Dec. 1974.

[14] P. Malcovati, F. Maloberti, C. Fiocchi, and M. Pruzzi, "Curvature-compensated BiCMOS bandgap with 1-V supply voltage," IEEE J. Solid-State Circuits, vol. 36, pp. 1076–1081, July 2001.

[15] H. Banba, H. Siga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," IEEE J. Solid-State Circuits, vol. 34, pp. 670–674, May 1999.

[16] M. Gunawan, G. C. M. Meijer, J. Fonderie, and J. H. Huijsing, "A curvature-corrected low-voltage bandgap reference," IEEE J. Solid-State Circuits, vol. 28, pp. 667–670, June 1993.

[17] E. A. Vittoz and O. Neyroud, "A low-voltage CMOS bandgap reference," IEEE J. Solid-State Circuits, vol. SC-14, pp. 573–577, June 1979.

[18] A. Buck, C. McDonald, S. Lewis, and T. R. Viswanathan, "A CMOS bandgap reference without resistors," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2000, pp. 442–443.

[19] A. Buck, C. Mc Donald, S. Lewis, T.R. Viswanathan, "A CMOS bandgap reference without resistors," in Journal of Solid State Circuits, vol. 37, no. 1 January 2002.

[20] E. Vittoz, "The design of high performance analog circuits on digital CMOS chips," IEEE J. Solid-State Circuits, vol. SC-20, pp. 657–665, June 1985.

[21] S. Q. Malik, M. E. Schlarmanm, and R. L. Geiger, "A low temperature sensitivity switched-capacitor current reference," in Proc. 15th ECCTD, vol. 1, Espoo, Finland, Aug 28–31, 2001, pp. 269–272.

[22] Wei Liu, Waleed Khalili, Mohammed Ismail, and Edith Kussener, "A Resistor-Free Temperature-Compensated CMOS Current Reference," Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on, pp 845-848, 2010

[23] Hosung Chun and Torsten Lehmann, "CMOS current reference generator using integrated resistors," Electronics and Information Engineering (ICEIE), 2010 International Conference On, pp 290-294, 2010

[24] Falconi, C.; D'Amico, A.; Scotti, G.; Trifiletti, A, "Low voltage CMOS current and voltage references without resistors," Circuits and Systems, 2007. ISCAS 2007, IEEE International Symposium on, vol. 5, 2007, pp. 1907–1910.

[25] Rasoul Dehghani and S. M. Atarodi, "A new low voltage precision CMOS current reference with no external components," IEEE Trans. Circuit. Syst. II, vol. 50, No. 12, pp.928–932, December 2003.

[26] P. Bernardson, "Precision, temperature and supply independent CMOS current source with no external components," Electronics Letters, vol.38, no.25, December 2002.

[27] Henri J. Oguey and Daniel Aebischer, "CMOS current reference without resistance," IEEE J. Solid-State Circuits, vol. 32, No. 7, pp. 1132–1135, July 1997.

[28] B.M. Putter, "On-chip RC measurement and calibration circuit using Wheatstone bridge," Circuits and Systems, ISCAS 2008. IEEE International Symposium on, pp 1496 – 1499, 2008

[29] B. Razavi, "Design of Analog CMOS Integrated Circuits," Boston, MA: McGraw-Hill, 2001

[30] B. Razavi, "RF Microelectronics," Prentice Hall, 1998

[31] P. R. Gray and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits," 4th ed. New York: Wiley, 2001

[32] James W. Nilsson, "Electric Circuits," 4th ed. Addison Wesley, 1993

[33] Donald A. Neamen, "Semiconductor Physics and Devices: Basic Principles," Irwin, 1992

[34] Thomas Lee, "The design of CMOS Radio-Frequency Integrated Circuits," Cambridge, 1998

[35] Ali Niknejad, "Electromagnetics for High-Speed Analog and Digital Communication Circuits," Cambridge, 2007

[36] Michael S. McCorquodale, Justin D. O'Day, Scott M. Pernia, Gordon A. Carichner, Sundus Kubba, and Richard B. Brown, "A Monolithic and Self-Referenced RF LC Clock Generator Compliant With USB 2.0," IEEE J. Solid-State Circuits, vol. 42, pp. 385–399, February 2007.