Analysis and Design of a High Speed Delta-Sigma Modulator for mm-Wave Imaging Applications

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Acknowledgements

It is my belief that in any milestone achieved in life's journey, whether small or large, it is good to reflect on all that has aided the ascension to the milestone. As I continue in my pursuance of the Ph.D. degree, I would like to take this time to acknowledge those that have helped me reach this milestone that is the Master's Degree. Without the guidance, support, encouragement, advice, and education received from these individuals I could have never reached this first milestone of my graduate tenure.

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Chapter 1

Introduction

Although the physical world remains completely analog, the processing of the analog signals is performed almost entirely in the digital domain since digital circuits are more robust and extremely small, and can produce very complex yet accurate and fast systems [1]. For this reason, data conversion continues to be a hot research topic of interest.

Data converters can be classified into two main categories: Nyquist-rate and oversampling converters. Nyquist-rate converters exhibit one-to-one correspondence between the input and output, do not use memory elements, and can convert higher bandwidth (BW) signals at lower sampling frequencies [1]. Nyquist-rate converters are typically more suitable for high bandwidth applications since they sample near the Nyquist frequency. The drawback of Nyquist-rate converters is that analog component matching directly impacts linearity and accuracy, and practical conditions of today limit these converters to approximately 14-bit resolution.

In contrast, oversampling data converters can achieve up to 20-bit resolution with high conversion speeds, and sample at much higher rates than the Nyquist rate. Oversampling converters incorporate memory elements and therefore do not exhibit the one-to-one correspondence of Nyquist-rate converters, making them more difficult to interpret intuitively. Within oversampling converters, the delta-sigma modulator (DSM) is the most popular for high-performance or high-resolution applications. A significant advantage of DSMs is their relaxation of the accuracy of

analog components in the circuit [2]. Furthermore, the ability to shift undesirable noise out of the frequency band of interest (commonly referred to as noise-shaping) makes a DSM a powerful conversion tool capable of providing very high precision results. DSMs are typically intended for low BW, high precision applications such as sensor networks, process control, audio conversion, digital video, imaging systems, and wireless and wired communications [1].

1.1   Problem Statement

Wideband pulse modulation at mm-wave frequencies could be used for radar, imaging or high-speed communication applications. Reception and detection of these pulses poses a challenge in terms of the data conversion circuits. In this research we look at the final conversion step of the time-based ultra-wideband synthetic imaging (TUSI) system currently in development at UC-Berkeley.

Fig. 1.1 provides an illustration of the problem. Currently the TUSI transceiver includes all the necessary front-end blocks to output a 20 GHz I/Q signal, which is essentially a 40 GHz data
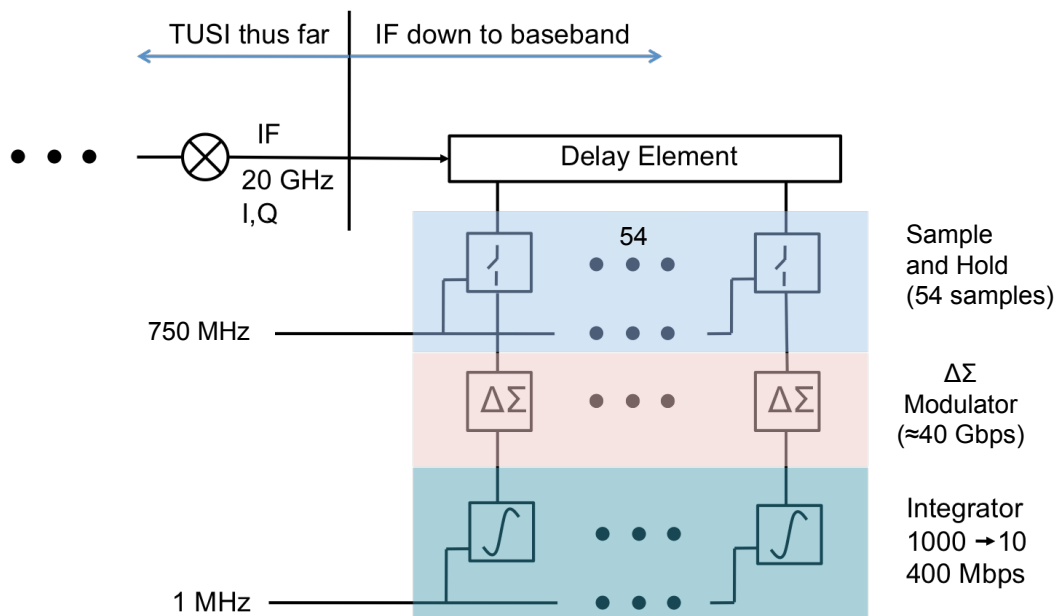
Figure 1.1: Illustration of the TUSI conversion problem.

signal. A delay line with 54 time-interleaved high-speed samplers and data converters is proposed to convert the analog signal to a digital low-frequency signal. The reason 54 data converters are used is that each of them will be operating off the internally generated 750 MHz clock signal. To accurately convert the full 40 GHz signal, 54 of these time-interleaved converters are needed, each evenly spaced across the delay line. The signal is sampled from the delay line via a high-speed sampling network, and the result is transmitted to the data converter to be converted. Note that the signal being sampled is a repetitive signal. This means that the high-speed samplers should ideally be sampling the same value, which makes the signal essentially DC. Therefore, the data converter is essentially converting DC signals since the high-speed samplers takes care of sampling the high-speed repetitive analog signal. For margin, the bandwidth specification is therefore set to 20 kHz, which is essentially a DC signal to a converter operating at 750 MHz. To convert the signal to a lower frequency that is more operable, an integrator is used to average 1000 data points down to 10 points. This results in a 400 Mbps data signal. At this point, the data conversion is complete, and the signal can be transmitted via a link to a digital signal processor to perform signal processing. This work focuses on the design of the data converter after the high-speed sampler but before the integration is performed.

In order to generate images with good contrast, imaging systems require high resolution, with better contrast requiring more resolution. From analysis of the overall TUSI system, it has been determined that 10 bit resolution is required to reproduce an accurate image from the signal. Since the data converter is to be part of the integrated transceiver, it must be as small as possible and reuse as many of the presently available on-chip control signals as possible. Furthermore, to ensure the incoming signal is synchronized with the modulator, the specified sampling clock (750 MHz) used for the data converter is a divided-down version of the internally generated clock used for the receiver. Since the signal being converted by the converter operating at 750 MHz is essentially a DC signal, the signal is drastically oversampled. To take advantage of the oversampling, an oversampling converter becomes the most promising solution for the data converter since the dynamic range is automatically improved without any additional circuitry required because of the oversampling. More dynamic range can be bought at very little expense if a noise-shaping modulator is used

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Specifications	
Input BW (physical circuit)	20 kHz
Input BW (modeled DSM)	100 kHz
Sampling Speed	750 MHz
Resolution	10 bits

Table 1.1: General specifications for the DSM ADC.

for the oversampling converter. The high oversampling rate combined with noise shaping may be significant enough that a simple, small, low-power, and more robust converter can be employed to perform the conversion [1]. To take advantage of all the aforementioned properties, a DSM Analog-to-Digital converter (ADC) is chosen to perform the conversion. The general specifications for the DSM are provided in table 1.1. Note that for the model, a bandwidth of 100 kHz is used as the specification to provide margin by overdesigning. The input bandwidth specification for the physical circuit is still 20 kHz. This factor of 5 of overdesign is chosen since this is consistent with the variation that a physical circuit may experience. Variation in processing and operating conditions can at times cause performance to vary by up to a factor of 4. To conclude, this work develops a high-speed, high-resolution DSM that meets all the specified constraints and is optimized for the TUSI transceiver.

1.2 Scope of Work

This work covers the design of a first-order high-speed, high-resolution DSM for mm-wave imaging applications. It details the analytical analysis and modeling employed to obtain the internal parameters of the DSM, based on the constraints inputted into the DSM model, necessary to realize the DSM physically. It also describes the circuit design procedure exercised to realize each of the DSM's building blocks and the overall DSM. To demonstrate the capabilities of the proposed design, the DSM was created using a commercial BiCMOS 130 nm process.

1.3   Organization

The organization of the remainder of this report is as follows. Chapter 2 discusses some of the fundamental principles that make DSMs popular, and provides a discussion on the variety of architectures that can be utilized to design a DSM for different applications. Chapter 3 discusses the modeling of the DSM system to perform behavioral simulations. The most important non-idealites that need to be considered when modeling a DSM are also provided in chapter 3, as are the behavioral simulation results of the model that identify its performance. Chapter 4 provides the circuit design details that are necessary to physically implement the DSM. It goes through each of the significant blocks of the DSM and discusses the considerations that go into physically implementing the DSM. It also provides the final sizes of the transistors in each of the key blocks. Chapter 4 concludes by providing the results of the circuit and comparing them with the results provided from the behavioral simulations. The conclusion and references follow chapter 4. An example of the DSM's operation is provided in the Appendix to conclude the thesis.

Chapter 2

Oversampling Delta-Sigma Converter Principles

2.1   Oversampling Advantages

Oversampling converters in general allow ADC designers to take advantage of the availability of low cost, low power digital filtering while trading off speed for resolution. However, two of the primary advantages of oversampling converters are the relaxation of the specifications of the analog building blocks, such as the anti-aliasing (AA) filter needed prior to sampling, and the ability to spread the quantization noise.

2.1.1   AA Filter Specification Relaxation

Consider the input signal shown in Fig. 2.1 (a). When a Nyquist converter sampling near the Nyquist rate samples the input signal, the resulting spectrum appears as in Fig. 2.1 (b). To ensure aliasing does not occur, the Nyquist sampler must follow an AA filter as depicted in Fig. 2.1 (b). For modern applications that require very high resolution and dynamic range, typical requirements for the AA filter would be a very narrow transition-band, high attenuation in the stop band, and
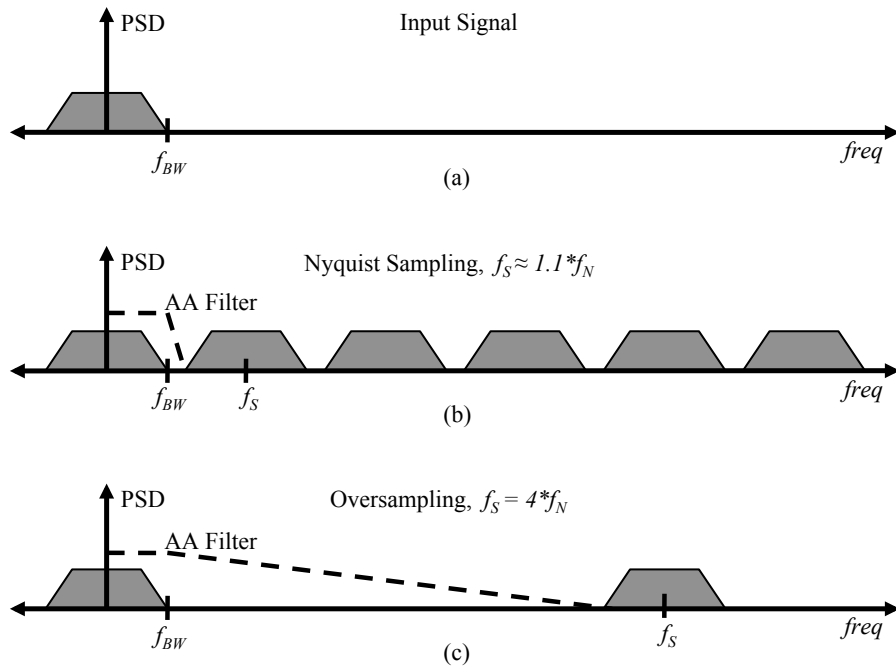
Figure 2.1: Sampling of the input signal (a) by a Nyquist sampler (b) and an oversampling sampler (c) along with the accompanying AA filters.

as little noise contribution as possible. Such specifications are very difficult to achieve even for state-of-the-art filter designs. Now consider the case when the input signal is oversampled. The resulting spectrum appears as in Fig. 2.1 (c) along with the necessary AA filter. As can be seen, the specifications for an AA filter followed by an oversampling sampler can be significantly relaxed due to a wider transition-band. In addition, more noise can be tolerated from the circuit devices and components than in the Nyquist sampled case because the quantization noise, which consumes some of the allotted noise budget, has been spread across the sampling bandwidth, and thus yields less quantization noise within the frequency band of interest as discussed next.

2.1.2   Quantization Noise Spreading

The illustration in Fig. 2.2 shows how oversampling, with no additional modifications to the ADC, can improve the in-band quantization noise. First note that the entire input signal is con-

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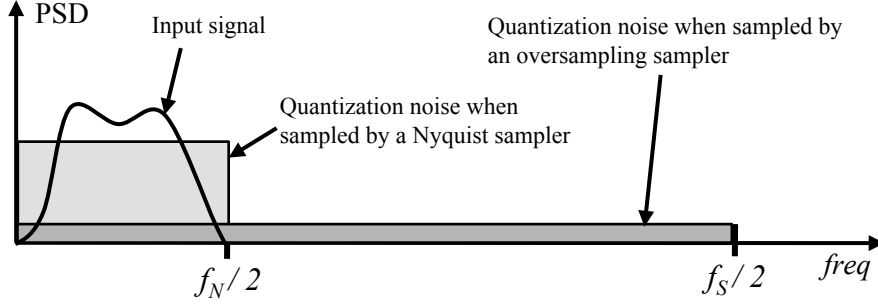
Figure 2.2: Quantization noise PSD within f_{BW} ($\approx f_N/2$) when a Nyquist converter and an over-sampling converter is utilized.

tained within $f_N/2$ as required by the Nyquist theorem. The quantization noise is shown for both of the sampling cases. When the signal is sampled by a Nyquist sampler all the quantization noise power is contained within $f_N/2$ just like the input signal power. However, when the signal is oversampled the quantization noise is distributed across a larger frequency range, namely $f_S/2$, although the total quantization noise remains unchanged. By following the oversampling ADC with a low-pass filter (LPF) with a corner frequency of $f_N/2$, the out-of-band noise can be filtered out leaving less quantization noise in-band than in the Nyquist sampling case. This result directly improves the signal-to-quantization-noise ration (SQNR) of the ADC.

To show the result analytically, first note that if we assume the quantizer with a quantization step of Δ has its quantization noise error uniformly distributed from $-\Delta/2$ and $+\Delta/2$, then the quantization noise variance (power) $\overline{e_q^2}$ is given by

$$\overline{e_q^2} = \frac{\Delta^2}{12} \tag{2.1}$$

as shown in [3]. When the ADC is sampled by a Nyquist sampler, the quantization noise power gets distributed across the sampling bandwidth and the power spectral density (PSD) becomes

$$\overline{N_{q,f_N}^2(f)} = \frac{\overline{e_q^2}}{f_N} = \frac{\frac{\Delta^2}{12}}{f_N}. \tag{2.2}$$

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If the signal is oversampled, then the quantization noise power gets distributed across a wider spectrum, f_S, and assuming the LPF is ideal, the total in-band noise is found by integrating the quantization PSD between $-f_N/2$ and $f_N/2$, yielding the total in-band quantization noise power $\overline{N^2_{q,in-band}}$ evaluated as

$$\overline{N^2_{q,in-band}} = \int_{-f_N/2}^{+f_N/2} \overline{N^2_{q,f_S}(f)}df = \int_{-f_N/2}^{+f_N/2} \frac{\frac{\Delta^2}{12}}{f_S}df = \frac{\Delta^2}{12}\frac{2f_{BW}}{f_S} = \frac{\Delta^2}{12}\frac{f_N}{f_S} \tag{2.3}$$

where f_S/f_N is the oversampling rate (OSR). From the result, it is clear that increasing the OSR reduces the baseband noise power, thereby directly increasing the SQNR without any modifications to the ADC modulation scheme. Therefore, any Nyquist ADC, such as the SAR ADC, can have its SQNR improved simply by oversampling the signal. However, oversampling alone is not sufficient to achieve very high resolution ($\sim$20 bits) with a Nyquist-rate ADC since there are practical limitations to sampling speeds. To achieve very high resolution, oversampling is combined with advanced ADC architectures, such as DSMs.

2.2 Architecture Variations and Applications

The standard block diagram architecture for an oversampling ADC utilizing delta-sigma modulation is shown in Fig. 2.3. The significance of the analog AA filter and the oversampling sampler have been discussed previously. The decimator consists of a digital filter with a narrow transition band with a corner frequency of f_{BW} for removing the out-of-band quantization noise, and
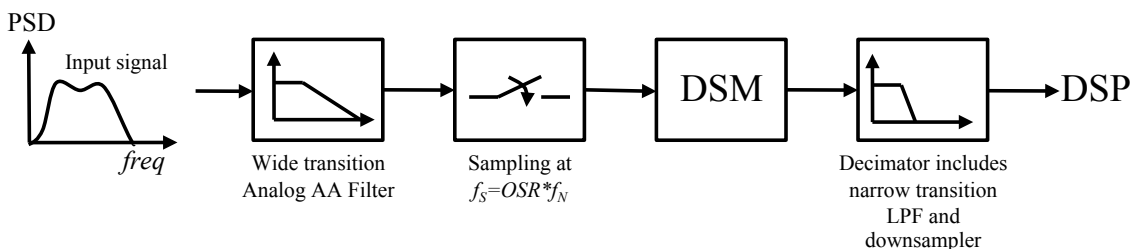
Figure 2.3: Standard block diagram architecture for an oversampling ADC.

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a decimation filter to reduce the data rate to a rate more useful with digital signal processors. Advancements in delta-sigma ADCs have focused primarily with the DSM architecture–the block that converts the analog signal, after sampling, to a digital signal consisting of a 1-bit pulse density stream. Depending on the application and the specifications, the optimal architecture and the order of the DSM can vary significantly. DSMs have been realized with system transfer functions up to the eigth order [4–10]. Furthermore, these advanced DSM architectures have been applied to a variety of applications, such as wideband, RF baseband, thermocouple measurement, resistance temperature detection, frequency synthesis, and digital audio applications [11–15]. Hence, the decision on a specific architecture for an application is not trivial and requires extensive analysis.

Chapter 3

System Behavioral Modeling

All DSM topologies are non-linear systems incorporating memory, which make them inherently difficult to analyze. Moreover, selection of the appropriate architecture selection, loop filter type, order and coefficients, and the number of bits in the quantizer for a DSM is a non-trivial and time-consuming task [16]. In order to accelerate the transition from theoretical design to circuit implementation, behavioral models have proven to be invaluable. The development of a model that also includes most first- and second-order non-ideality effects is essential to reduce the iteration process. The task of creating a reliable system behavioral model for the desired DSM is tackled next, but first a brief discussion on the selection of the DSM topology is presented.

3.1   Topology Selection

As discussed previously, the driving constraints for the desired converter are to provide high resolution at high speeds, to consume as small an area as possible to minimize its footprint on the overall transceiver, and to reuse as many of the available on-chip control signals including the 750 MHz clock.

Although the requirements for high resolution at high speeds generally necessitate a multi-bit or high-order topology, these topologies exhibit drawbacks in clear contrast to the other two

requirements. First, multi-bit converters impose severe linearity constraints on the digital-to-analog converter (DAC) in the feedback loop, as shown in [17], making them more difficult to adapt to requirements in place from other blocks in the system. Second, stability issues arise for higher order converters, especially when sampled at speeds approaching the GHz range. Most importantly, both topologies require additional blocks, thereby increasing the size.

To start the design process, it is often useful to have a general idea of the type of resolution that can be achieved by a specific architecture without needing to take into account the input signal or sometimes even Δ. Assuming the input signal is a full-scale sine wave with a peak amplitude of 1 and that $\Delta = 2$, the peak dynamic range (DR) of an ideal nth order DSM with an oversampling ratio OSR and B bits in the quantizer can be estimated by the known equation [18],

$$ DR_{dB} = 10 \cdot \log \left[\frac{3}{2} \cdot \left(2^B - 1 \right)^2 \cdot \frac{2n+1}{\pi^{2n}} \cdot OSR^{2n+1} \right]. \tag{3.1} $$

Based on the specifications specified earlier in table 1.1, the input signal bandwidth for the converter is approximately 100 KHz, which yields an OSR of approximately 3,750. From equation 3.1, a first-order DSM with an OSR of 3,750 utilizing a 1-bit DAC in the feedback loop can ideally achieve a peak DR of approximately 103.8 dB, which is more than sufficient resolution for the imaging transceiver. Consequently, a first-order switched-capacitor DSM utilizing a 1-bit DAC in the feedback loop is the topology chosen to meet the specifications. Among other advantages, the first-order DSM is the most stable of the topologies, and the use of a 1-bit DAC in the feedback loop makes the converter inherently linear. Furthermore, it requires minimal building blocks and is the most robust topology, thus clearly meeting the specifications imposed. Next, the system behavioral model for the first-order DSM selected is discussed.

3.2 Ideal First-order Delta-Sigma Modulator Model

The block diagram model for a first-order DSM is presented in Fig. 3.1. The block diagram includes a loop filter H(z), 1-bit quantizer (comparator), 1-bit DAC, and a summation block. DSMs
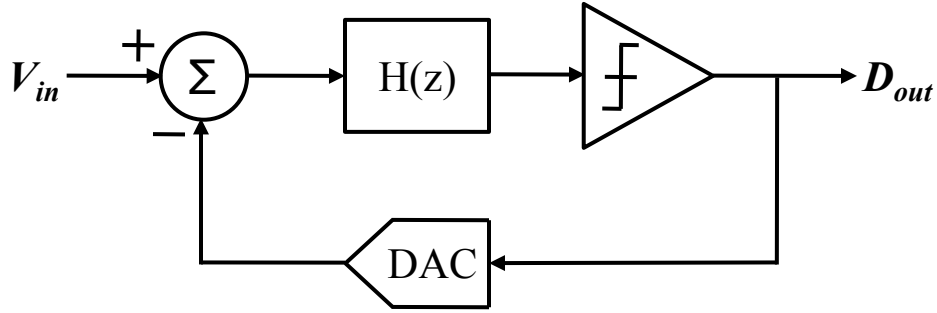
Figure 3.1: Block diagram for a first-order DSM.

can be implemented in either discrete-time or continuous-time, but in both cases the general block diagram as presented in Fig. 3.1 is the same. As described in [18], basic properties/characteristics of a DSM are:

- Maximum analog input range is equal to the DAC reference levels

- The average value of D_{out} must equal the average value of V_{in}

- Inherently linear for a 1-bit DAC

- To a first order, linearity and quantization error are not dependent on component matching

3.2.1   Signal Transfer Function

The DSM is a dynamic and nonlinear system due to the memory in the integrator and the quantization effect of the comparator, respectively, and hence mathematical analysis is a difficult task [1]. However, by utilizing linear models for the blocks, tractable qualitative analysis of the DSM can be performed. Representing the quantizer as an additive noise source linearizes the system model.

The resulting linear z-domain system model with the quantizer represented as an additive noise source is shown in Fig. 3.2. The model is presented in the z-domain since the DSM is physically implemented as a switched-capacitor circuit, which is inherently a discrete-time circuit. The standard loop filter chosen for a DSM is an integrator–chosen to accumulate the error signal, which can

then be minimized by the loop. An integrator in the z-domain can be represented in two ways–as a zero delay integrator or a delaying integrator. Fig. 3.3 shows the two types of z-domain integrators, along with their accompanying transfer function formula. For the behavioral MATLAB model discussed here the zero delay integrator is more intuitive and therefore it is employed, but for the physical circuit implementation of the DSM the delayed integrator model is utilized since it is more easily physically implemented. In any case, the results for the behavioral model and the physical circuit are the same. Note that to complete the model, based on the physical switched-capacitor DSM architecture employed, which is discussed in the next section, the value fed back by the DAC
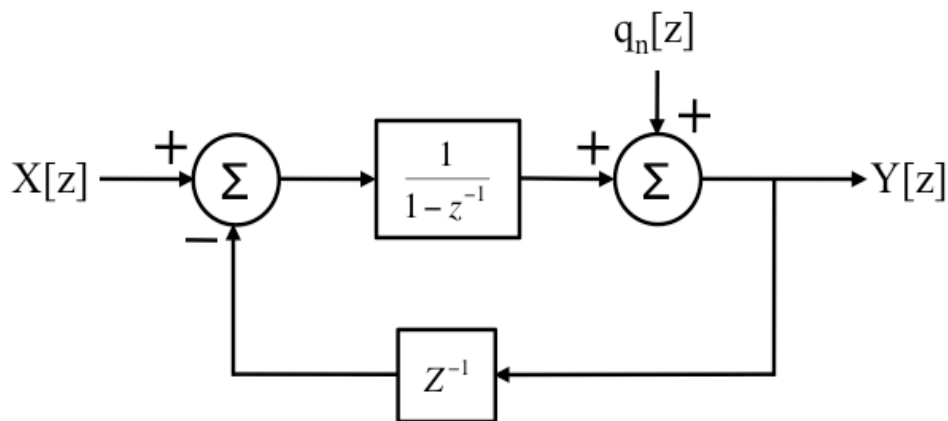
Figure 3.2: Linear z-domain block diagram for a first-order DSM.

$$H(z) = \frac{1}{1 - z^{-1}}$$

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$
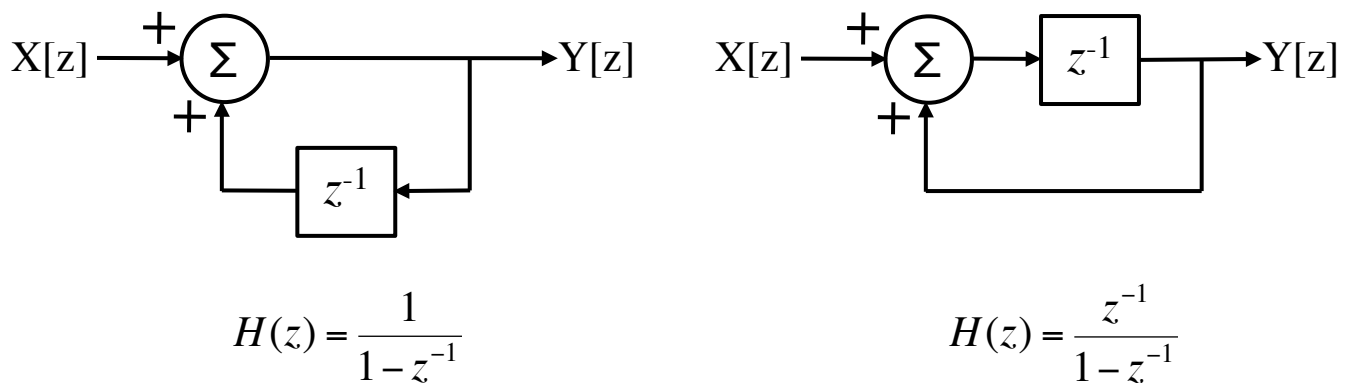
Figure 3.3: Linear z-domain block diagram and transfer function for a (a) zero delay integrator and a (b) delaying integrator.

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does not get evaluated until the next sampling phase of the system, and therefore a delay block is included in the feedback loop of the linear z-domain model to correctly model the sampling of the delayed feedback. If the delayed integrator is used in the behavioral model block diagram, the delay block in Fig. 3.2 must be removed for the two block diagrams to be equivalent. With the z-domain system block diagram explained, the mathematical analysis of the DSM model can now be undertaken.

From analysis of Fig. 3.2, the signal transfer function for the overall DSM becomes

$$H_{DSM}(z) = \frac{H_{int}(z)}{1 + H_{int}(z) \cdot z^{-1}} = \frac{1}{(1 - z^{-1}) \cdot \left(1 + \frac{z^{-1}}{1 - z^{-1}}\right)} = 1. \tag{3.2}$$

Hence, without considering the non-idealities the input is unaffected and is fed directly to the output. Note that if the delaying integrator were used, the delay block in the feedback loop would need to be removed and the resulting signal transfer function would simply be z^{-1}, which is simply a delay as expected because of the use of the delaying integrator.

3.2.2 Quantization Noise Transfer Function and Noise Shaping

The key property contributing to the effective and extensive use of the delta-sigma converter is the noise-shaping capabilities of the DSM. It was shown in section 2.1.2 that oversampling alone can reduce the in-band quantization noise, but when oversampling is performed along with the use of a noise-shaping modulator, such as a DSM, the in-band quantization noise can be reduced even further. Referencing Fig. 3.2, the quantization noise transfer function can be evaluated as

$$H_{QN}(z) = \frac{1}{1 + H_{int}(z) \cdot z^{-1}} = \frac{1}{1 + \frac{z^{-1}}{1 - z^{-1}}} = \frac{1 - z^{-1}}{1 - z^{-1} + z^{-1}} = 1 - z^{-1}, \tag{3.3}$$

which is essentially a differentiator. By setting $z = e^{j\omega T}$ as shown in [18], the squared magnitude of the noise transfer function in the frequency domain, which is necessary to calculate the total
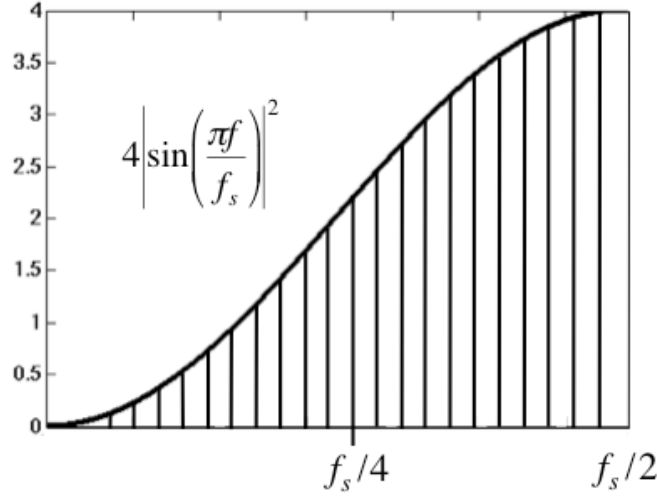
Figure 3.4: Noise-shaping function of $|H_{QN}(j\omega)|^2$.

in-band quantization noise power, can be evaluated as

$$|H_{QN}(j\omega)|^2 = \left|1 - e^{-j\omega T}\right|^2 = \left|2\sin\left(\frac{\omega T}{2}\right)\right|^2 = 4\left|\sin\left(\frac{\pi f}{f_S}\right)\right|^2. \tag{3.4}$$

Fig. 3.4 illustrates the frequency response of equation 3.4, and it is clear that $|H_{QN}(j\omega)|^2$ exhibits a high-pass response that pushes the quantization noise out-of-band by suppressing the noise at low frequencies (in-band) and amplifying it at frequencies near f_S (out-of-band).

The PSD of the quantization noise of an oversampling converter is

$$\overline{N_{q,f_S}^2(f)} = \frac{\Delta^2}{12}\frac{1}{f_S} \tag{3.5}$$

as was described in section 2.1.2 under the assumption that the quantization noise is uniformly distributed between $-\Delta/2$ and $+\Delta/2$. To calculate the total in-band quantization noise, $|H_{QN}(j\omega)|^2$ is applied to $\overline{N_{q,f_S}^2(f)}$ with the simplification that for $f << f_S$, $\sin\left(\frac{\pi f}{f_S}\right) \approx \pi f/f_S$. This yields

$$\overline{N_{q,in-band}^2} = \int_{-f_N/2}^{+f_N/2} |H_{QN}(j\omega)|^2 \cdot \overline{N_{q,f_S}^2(f)} df \approx \int_{-f_N/2}^{+f_N/2} 4\left|\frac{\pi f}{f_S}\right|^2 \frac{\Delta^2}{12}\frac{1}{f_S} df = \frac{\pi^2}{3}\frac{1}{OSR^3}\frac{\Delta^2}{12}. \tag{3.6}$$

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Assuming the input signal is a full-scale sine wave with peak amplitude A_{mag}, the SQNR is given approximately by

$$SQNR_{dB} = \frac{\overline{S^2_{input}}}{N^2_{q,in-band}} = \frac{\frac{1}{2}A^2_{mag}}{\frac{\pi^2}{3}\frac{1}{OSR^3}\frac{\Delta^2}{12}} = \frac{18\,(OSR)^3\,A^2_{mag}}{\pi^2\Delta^2}. \tag{3.7}$$

Equation 3.7 can be used as an estimate for the maximum achievable dynamic range of the design. The result shows the $SQNR$ can be improved by either increasing the input signal magnitude, reducing the quantization step size, or most importantly increasing the OSR.

3.3 Modeling of the Non-idealities
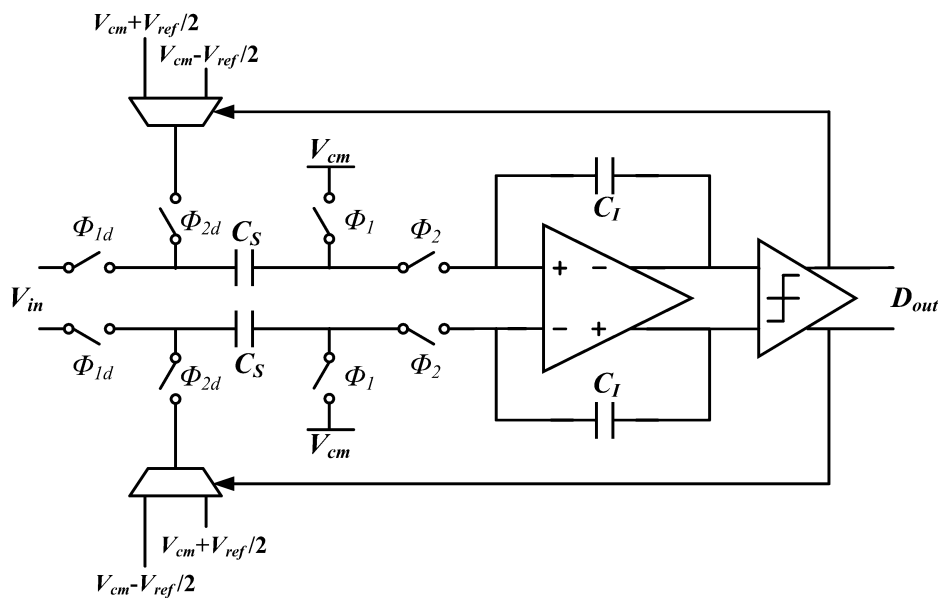
Figure 3.5: Circuit implementation of the first-order DSM.

Fig. 3.5 shows the circuit used to physically implement the DSM. More thorough details of the circuit will be provided in chapter 4, but the non-idealities associated with the circuit will be studied here to guide the circuit design of chapter 4. Once the non-idealities associated with the circuit of Fig. 3.5 are included, the model is complete, and through behavioral simulations of the

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complete model, the impact of various parameters on the entire system can be analyzed and the appropriate specifications/parameters for the DSM can be established.

3.3.1 Integrator Non-idealities

Fig. 3.6 presents the single-ended half-circuit of the DSM integrator as well as the parasitic capacitances C_P and C_L associated with the total parasitic capacitance at the input and output terminals of the operational transconductance amplifier (OTA), respectively. The overall z-domain transfer function for the non-ideal integrator is

$$H_{int}(z) = \frac{C_S}{C_I} \cdot \frac{\alpha}{1 - \beta z^{-1}}, \tag{3.8}$$

where α and β are the integrator's gain and leakage, respectively [19, 20]. Among the many non-idealities that directly impact the gain or leakage, static errors and the dynamic errors due to the integrator finite bandwidth and slewing are the primary factors that cause performance degradation in switched-capacitor DSMs. Following an approach similar to [20–22], each factor is analyzed individually in the next three sections, and then consolidated to model the integrator behavior.

3.3.1.1 Static Error

Since the DSM is implemented as a discrete-time switched-capacitor circuit, two phases exist to perform the integration–a sampling phase and an integration phase, and each phase must be
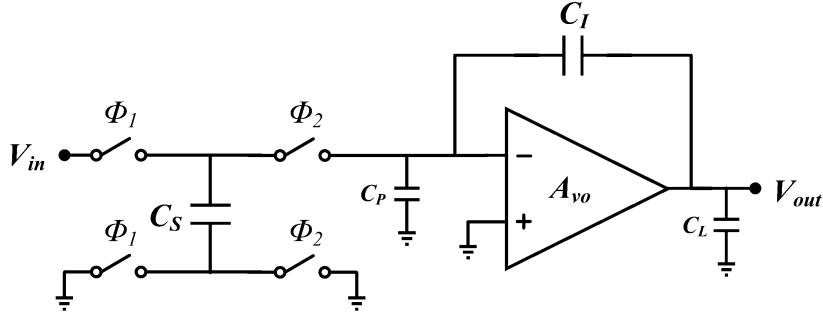
Figure 3.6: Single-ended half-circuit of the DSM integrator with parasitics included.

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analyzed separately since the error differs in each phase. Fig. 3.7 provides models for the integrator during both the sampling and integration phase. The feedback factors in each phase are

$$F_S = \frac{C_I}{C_I + C_P} \tag{3.9}$$

$$F_I = \frac{C_I}{C_I + C_P + C_S}, \tag{3.10}$$

where F_S and F_I are the dc feedback factors in the sampling and integration phase, respectively, and A_{vo} is the open-loop gain of the OTA. Allowing Ψ_S and Ψ_I to represent the closed-loop static errors in the sampling and integration phases, respectively, the closed-loop static errors can be evaluated as

$$\Psi_S = \frac{F_S A_{vo}}{1 + F_S A_{vo}} \tag{3.11}$$

$$\Psi_I = \frac{F_I A_{vo}}{1 + F_I A_{vo}}. \tag{3.12}$$

For high resolution applications, control of the parasitics is essential to keeping the static error to a minimum since large parasitics reduce the feedback factor which then requires a larger open-loop gain (and more power) to contain the static error within a specified amount.
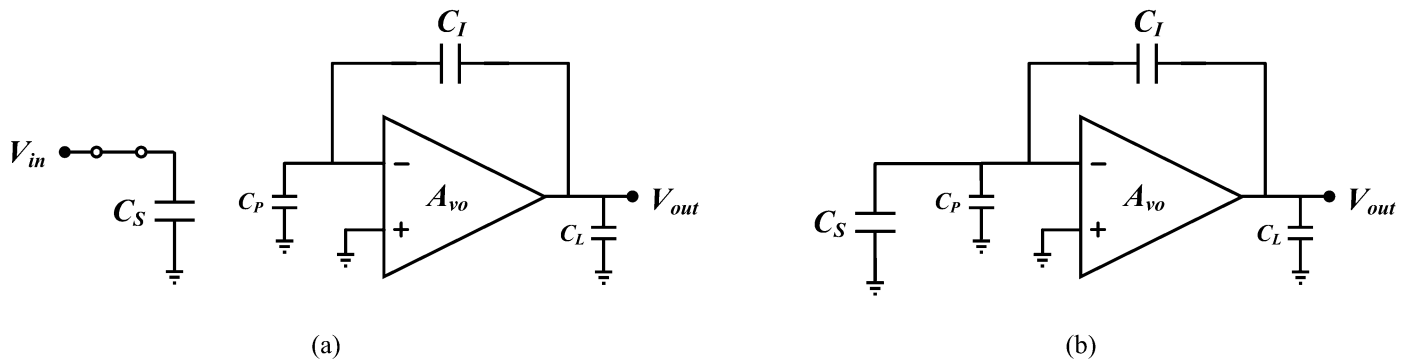
Figure 3.7: Switched-capacitor integrator during the (a) sampling phase and (b) integration phase.

3.3.1.2 Dynamic Error–Finite Bandwidth

The finite bandwidth caused by the finite closed-loop pole of the OTA is another non-ideality that further limits the settling speed of the DSM. To commence the analysis, the amplifier gain A_{vo} is needed, and is given by

$$A_{vo} = g_m R_{out} \tag{3.13}$$

where g_m and R_{out} are the transconductance and the total output impedance of the OTA, respectively. The effective closed-loop load capacitance $C_{L,eff,CL}$ that specifies the closed-loop pole $\omega_{P,CL}$ is a function of the open-loop load capacitance $C_{L,eff,OL}$ and the dc feedback factor F_I. Referring to Fig. 3.7 (b), the effective open-loop capacitance, closed-loop capacitance, and unity-gain bandwidth ω_{ugb} are defined as

$$C_{L,eff,OL} = C_L + C_I || (C_S + C_P) = C_L + \frac{C_I (C_S + C_P)}{C_I + C_S + C_P} \tag{3.14}$$

$$C_{L,eff,CL} = \frac{C_{L,eff,OL}}{F_I} = C_S + C_P + \frac{C_L (C_I + C_S + C_P)}{C_I} \tag{3.15}$$

$$\omega_{ugb} = \frac{g_m}{C_{L,eff,OL}}. \tag{3.16}$$

Including the effect of the feedback to evaluate the closed-loop pole yields

$$\omega_{P,CL} = \frac{\omega_{ugb}}{A_{vo,CL}} = \frac{g_m}{C_{L,eff,CL}} = \frac{g_m F_I}{C_{L,eff,OL}} \tag{3.17}$$

where the closed-loop gain $A_{vo,CL}$ is approximately $1/F_I$.

With the finite closed-loop pole established, the finite bandwidth dynamic settling error ξ_I is found by analyzing the time domain step response of the OTA during the integration phase, and is evaluated as

$$\xi_I = \exp\left(\frac{-t_{int}}{\tau_{ota}}\right) \tag{3.18}$$

where t_{int} represents the time available for settling during the integration phase and τ_{ota} is the

time constant defined as

$$\tau_{ota} = \frac{1}{\omega_{P,CL}}.$$ (3.19)

Equation 3.18 shows that, other than increasing the time available for settling, increasing g_m or F_I, and reducing $C_{L,eff,OL}$ can all reduce the performance degradation due to the finite closed-loop pole. Since increasing g_m also increases the power, control of parasitic capacitances once again proves to be essential since F_I and $C_{L,eff,OL}$ can both be improved by limiting the parasitics in the design.

Comparison of Ψ_I and ξ_I shows that it is best to allocate more of the settling error budget to the static error since it is often easier to improve the static error by improving the dc gain than improving the dynamic error, of which the finite closed-loop pole is only one nonideality that contributes to the dynamic error.

3.3.1.3 Dynamic Error–Slew Rate Analysis

Another significant nonideality associated with the integrator is slewing. The effect of both the finite bandwidth and the slew rate are related to each other and may be interpreted as a non-linear gain [23]. The slew rate is a direct result of the output current limitation imposed by the OTA circuit. To visualize the slewing effect, Fig. 3.8 provides the general transconductor ΔI vs. ΔV relationship for a differential OTA transistor, as well as the relevant circuitry of the OTA. As shown in Fig. 3.8 and discussed in detail in [24], the circuit begins to slew essentially when the amplitude of the input exceeds V^*, where V^*, the overdrive voltage for long channel devices, is defined as

$$V^* = \frac{2I_D}{g_m} = \frac{I_{SS}}{g_m}.$$ (3.20)

Intuitively, this result should be expected since all the current is steered completely in one direction when $V_{id,amp} > V^*$, and thus no more current is available beyond this point to speed up the settling process. Although this result is more accurate for older technologies (long channel), for modeling purposes prior to design it is still a very useful and intuitive first-order model. Therefore, in order to ensure linearity, $V_{id,amp} \leq V^*$. If $V_{id,amp} > V^*$, then the circuit becomes nonlinear and produces
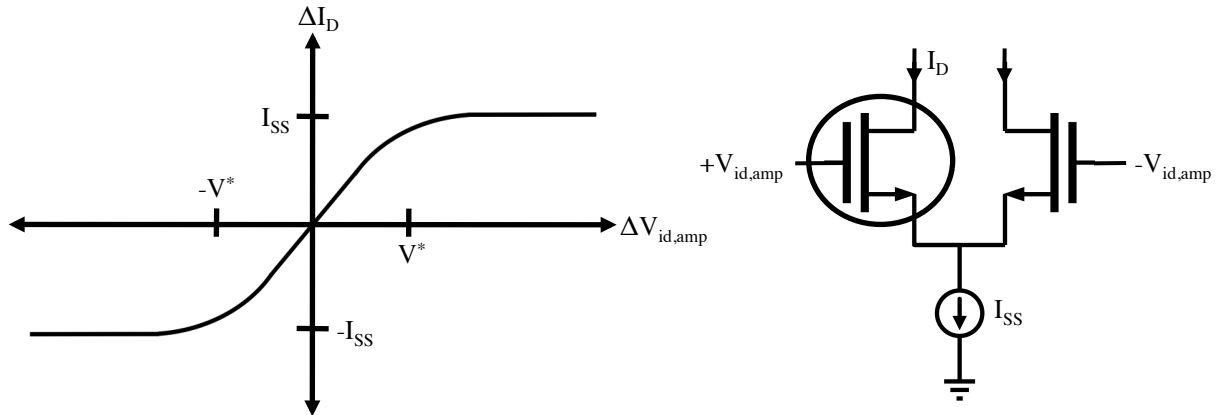
Figure 3.8: General transconductor ΔI vs. ΔV relationship for a differential OTA transistor, as well as the relevant circuitry of the OTA.

harmonic distortion reducing the total signal-to-noise and distortion ratio (SNDR) [22].

Based on the analysis of Fig. 3.8, nonlinear slewing of an amplifier can be modeled as approximately piecewise linear in which slewing with constant current is followed by linear settling exponentially. Hence, the total time needed to settle the output can be given as

$$t_{int} = t_{slew} + t_{s,lin}, \tag{3.21}$$

where t_{int} is the total settling time allowed during the integration phase, t_{slew} is the settling time spent slewing, and $t_{s,lin}$ is the linear exponentially settling time [25]. Since t_{int} is set by the sampling speed of the DSM and $t_{s,lin}$ is the time left over to settle after slewing, the significant factor that must be determined is t_{slew}. To establish t_{slew}, the slew rate SR at the output is needed, and can be represented by the known equation

$$SR = \frac{I_{SS}}{C_{L,eff,OL}}, \tag{3.22}$$

where $C_{L,eff,CL}$ is the same as in 3.15. The feedforward factor FF_I during the integration phase is used to determine the differential voltage at the input of the differential OTA during the integration

phase, and referring to Fig. 3.7 (b) it is evaluated as

$$FF_I = \frac{C_S}{C_S + C_P + \frac{C_L C_I}{C_L + C_I}}. \tag{3.23}$$

The voltage at the input of the OTA is then

$$V_{x,step} = V_{in,amp} \cdot FF_I. \tag{3.24}$$

The amount by which $V_{x,step}$ exceeds V^* dictates how much time the OTA will spend slewing with constant current. This excess voltage ΔV_x is given by

$$\Delta V_x = V_{x,step} - V^*. \tag{3.25}$$

Since the slew rate is given for the output, the excess voltage at the output is

$$\Delta V_o = \frac{\Delta V_x}{F_I}, \tag{3.26}$$

and the time spent slewing at the constant current becomes

$$t_{slew} = \frac{\Delta V_o}{SR} = \frac{\Delta V_x \cdot C_{L,eff,OL}}{F_I \cdot I_{SS}}. \tag{3.27}$$

With an expression for the time spent slewing available, the major nonidealities that impact the behavior of the integrator can now be consolidated.

3.3.1.4   Integration of the Static and Dynamic Errors

The static error and the dynamic error due to the finite BW can be incorporated into the integrator model by revisiting the transfer function presented in equation 3.8. The transfer function

is reproduced here to aid the reader.

$$H_{int}(z) = \frac{C_S}{C_I} \cdot \frac{\alpha}{1 - \beta z^{-1}}, \tag{3.28}$$

As shown in [21], the new transfer function incorporating the aforementioned non-idealities is

$$H_{int}(z) = \frac{C_S}{C_I} \cdot \frac{\Psi_I (1 - \xi_I)}{1 - \frac{\Psi_I}{\Psi_S}\left(1 - \xi_I\left(1 - \frac{\Psi_S}{\Psi_I}\right)\right) z^{-1}}. \tag{3.29}$$

From a comparison of equation 3.28 and equation 3.29, the relationship between the gain and leakage to the non-idealities is

$$\alpha = \Psi_I (1 - \xi_I), \tag{3.30}$$

$$\beta = \frac{\Psi_I}{\Psi_S}\left(1 - \xi_I\left(1 - \frac{\Psi_S}{\Psi_I}\right)\right). \tag{3.31}$$

To include the slewing effect into the model, the voltage magnitudes at the input terminals of the OTA must be evaluated during each integration cycle. Depending on the input voltages applied to the OTA, the integrator may or may not slew, and therefore the transfer function applied to the signals varies. The three cases to consider, and the appropriately applied transfer functions are:

1) The integrator does not slew $(V_{id,amp}[n] \le V^*)$:

$$Y[n] = \alpha X[n] + \beta Y[n-1] \tag{3.32}$$

2) The integrator slews, $V_{id,amp}[n] > V^*$, and $t_{int} \le t_{slew}[n]$:

$$Y[n] = SR \cdot t_{int} + \beta Y[n-1] \tag{3.33}$$

3) The integrator slews, $V_{id,amp}[n] > V^*$, and $t_{int} > t_{slew}[n]$:

$$Y[n] = SR \cdot t_{slew}[n] + (\Psi_I X[n] - SR \cdot t_{slew}[n])\left(1 - \exp\left(\frac{-(t_{int} - t_{slew}[n])}{\tau_{ota}}\right)\right) + \beta Y[n-1] \tag{3.34}$$

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Although other second-order non-idealities degrade the integrator performance, those presented here represent the most significant factors that contribute to the performance degradation of the integrator.

3.3.2   Switch Non-idealities

In the previous analysis, it was assumed that the switches were ideal with zero on-resistance and infinite off-resistance. However, since the switches are implemented with NMOS and PMOS transistors, there exists non-idealities that further degrade the performance of the DSM. The most critical non-idealities are:

- Switch-induced noise

- Finite switch resistance → Finite acquisition bandwidth

- Distortion

- Charge injection/clock feedthrough

Through the use of transmission gates for the resistors along with the utilization of bottom-plate sampling for the entire switching network, the error due to the charge injection and clock feedthrough can be made negligible [18].

To model the finite acquisition bandwidth effect, consider Fig. 3.6 and Fig. 3.7 (a) again. Note that both of the switches that are on during Φ_1 in Fig. 3.6 are lumped together when considering the switch resistance, as are both of the switches that are on during Φ_2. The resulting finite switch resistance leads to additional settling error approximated by

$$\xi_{\text{sw}} = \exp\left(\frac{-t_s}{\tau_{samp}}\right), \tag{3.35}$$

where $\tau_{samp} = R_{\text{sw}}C$ is the time constant and t_s is the time allowed to sample the signal onto the capacitor. Referring to Fig. 3.9 for the simple case where the switch is an NMOS transistor, the
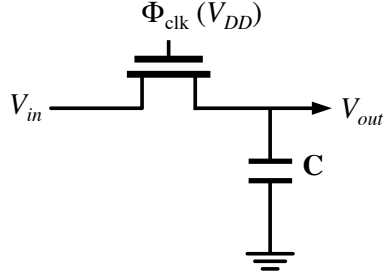
Figure 3.9: Practical sampling of a signal onto a capacitor via a CMOS switch.

on-resistance $R_{\mathrm{sw,N}}$ is

$$R_{\mathrm{sw,N}} = \frac{L}{W} \cdot \frac{1}{\mu C_{ox}\left(V_{DD} - V_{th}\right)} \cdot \frac{1}{1 - \frac{V_{in}}{V_{DD} - V_{th}}}. \tag{3.36}$$

The distortion in ξ_{sw} is a result of the input signal dependency of $R_{\mathrm{sw,N}}$ apparent in the last fractional term of $R_{\mathrm{sw,N}}$. However, through the use of transmission gates switches, the overall on-resistance of the switch is made more linear and less dependent on the input voltage, thus reducing the overall distortion due to the switch resistance. Since transmission gates are composed of the parallel combination of an NMOS and PMOS device, the overall on-resistance of a transmission gate switch can be expressed as

$$\frac{1}{R_{\mathrm{sw,NP}}} = \frac{1}{R_{\mathrm{sw,N}}} + \frac{1}{R_{\mathrm{sw,P}}}. \tag{3.37}$$

Although a transmission gate switch introduces parasitic capacitance at both terminals of the transmission gate, these parasitic capacitances are considered negligible when they are an order of magnitude smaller than the sampling capacitors, as is the case with the DSM designed in this report. Hence, equation 3.35 can be used to model the non-idealities of the switches used in the DSM, with $R_{\mathrm{sw,NP}}$ used as the resistance and either C_S or C_I used as the capacitance.

3.3.3 Noise

Sampling noise and the OTA's thermal noise are the fundamental limitations in the design of high-resolution DSMs [19]. Noise after the integrator is negligible because it is suppressed by the high DC gain of the integrator when input-referred, and it is also attenuated by the same noise shaping that attenuates the large quantization noise.

3.3.3.1 Sampling Noise

The noise power sampled onto a sampling capacitor is readily shown to be

$$\overline{v_n^2} = \frac{k_B \mathrm{T}}{C_S} \tag{3.38}$$

where k_B is the Boltzmann constant, T is the absolute temperature, and C_S is the sampling capacitance. For the circuit in Fig. 3.6, the total sampled noise power is

$$\overline{v_n^2} = \frac{2k_B \mathrm{T}}{C_S}, \tag{3.39}$$

where the factor of 2 accounts for the thermal noise of the input switches during both the sampling and integration phases. Another factor of 2 is necessary to account for the DSM being differential and not single-ended, and therefore the total sampled noise of the DSM is

$$\overline{v_{n,total}^2} = \frac{4k_B \mathrm{T}}{C_S}. \tag{3.40}$$

Although the result in equation 3.40 is used in the model to allow the filters in the decimator to remove the out-of-band noise, it is still important to calculate the total in-band noise expected prior to physical implementation since this aids the choice of capacitor sizes to use in the DSM. The total in-band noise is found by first spreading the noise across the sampling bandwidth to find the PSD

of the sampled noise as was done for the quantization noise. The resulting sampled noise PSD is

$$\overline{v_{n,total}^2}/f = \frac{4k_B\text{T}}{C_S}\frac{1}{f_S/2} = \frac{8k_B\text{T}}{C_S}\frac{1}{f_S}. \tag{3.41}$$

With the cutoff frequency of the decimator LPF set to f_{BW}, the total in-band noise becomes

$$\overline{v_{n,in-band}^2} = \frac{8k_B\text{T}}{C_S}\frac{1}{f_S}\cdot f_{BW} = \frac{4k_B\text{T}}{C_S}\frac{1}{OSR}. \tag{3.42}$$

Equation 3.42 clearly shows the significant advantage oversampling provides to reduce the noise power and dynamic range.

3.3.3.2 OTA Thermal Noise

The thermal noise of the OTA is inherently dependent on the overall design of the OTA. Different architectures will contribute different amounts of noise. In an attempt to make the modeling of the OTA noise more tractable despite this dependency, the noise is calculated at the output of the OTA, after which it can be referred back to the input if the reader chooses, although the result is the same. The total noise contributed at the output by the OTA is equivalent to the total noise sampled onto the differential output capacitors. The total noise sampled onto a capacitor was provided in equation 3.38. To include the OTA's contribution to the noise, only the noise factor that takes into account the OTA's design is necessary. The schematic for the OTA designed in this report is provided in Fig. 3.10, the details of which will be discussed in section 4.3.1. The noise factor on one output branch for such an OTA can be readily shown [25, 26] to be

$$\text{nf} = 1 + \frac{V_{in}^*}{V_{load}^*}, \tag{3.43}$$

where V_{in}^* and V_{load}^* correspond to the input device M_1 and the PMOS current source load device M_6, respectively. As an example, the expression for V_{in}^* is

$$V_{in}^* = \frac{2I_d}{g_{m,in}}, \tag{3.44}$$

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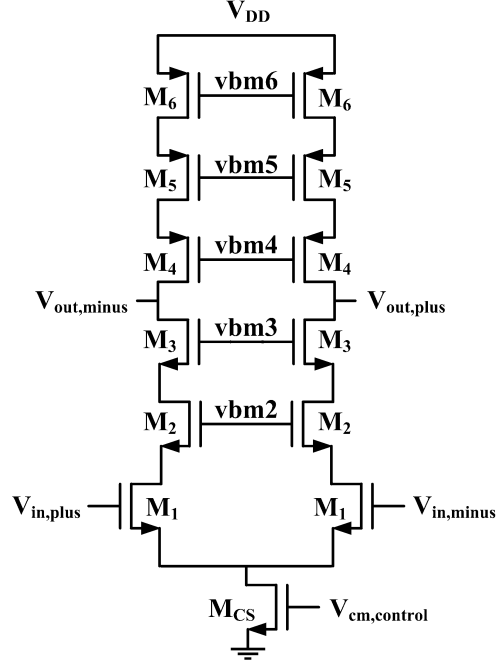
Figure 3.10: Circuit schematic of the OTA.

and its inverse represents the gain/power efficiency of the device. Equation 3.43 makes use of the simplification that the noise contribution of the cascode devices is negligible. This assumption generally holds, and thorough analysis supporting the assumption can be found in [25, 26]. Nevertheless, the result is more than sufficient for modeling purposes, and applying the noise factor to the sampled noise at the output yields the final model for the OTA output noise, approximated as

$$\overline{v_{n,OTA}^2} = \frac{2k_B\mathrm{T}}{C_{L,eff,CL}}\mathrm{nf} = \frac{2k_B\mathrm{T}}{C_{L,eff,CL}}\left(1 + \frac{V_{in}^*}{V_{load}^*}\right), \tag{3.45}$$

where $C_{L,eff,CL}$ is the effective closed-loop capacitance given in equation 3.15. The noise models for the sampling noise, OTA thermal noise, and the quantization noise provided in equation 2.1 represent the significant noise sources that are essential for the proper modeling of a DSM's performance.

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3.3.4 Other Non-idealities

Other non-idealities that can be added to the model include integrator offset voltage and comparator hysteresis. Although they are typically of minor concern, there are scenarios in which they can become problematic, especially for higher-order DSM architectures. Since the comparator hysteresis is also suppressed by the high DC gain of the integrator it is more often less significant than the integrator offset. Both non-idealities can be included into the model by simply adding a voltage source in series with the input for the integrator offset, and in series with the output for the comparator hysteresis.

3.4 Model Simulation Results

With the model completed, optimization was performed to specify the OTA parameters needed to physically implement the DSM circuit. The specified parameters provided a starting point for the circuit design, after which an iterative process back and forth between the model and the circuit was performed to arrive at the final parameters of the DSM circuit. Since the design of the analog blocks is dependent on the sampling/integrating capacitor sizes, the capacitor sizes were calculated first by utilizing the model as detailed in section 4.1 that discusses the circuit design of the sampling network. With the capacitor and switch sizes for the sampling network calculated, the values were entered into the model, and the model was optimized to obtain the necessary OTA parameters necessary to meet the specifications. Table 1.1 provided a summary of the general specifications. The parameters found from optimization of the model and multiple iterations of the circuit design are provided in table 3.1. The next chapter provides more detail into the circuit design techniques that were employed in parallel with model optimization to arrive at the final parameters provided in table 3.1.

The performance of the DSM found by simulating the model with the final parameters specified in table 3.1 is provided in Fig 3.11 and Fig. 3.12. Fig 3.11 is the standard plot used to specify the performance/resolution of a delta-sigma ADC. The resolution of the DSM is typically specified as the SNDR when the input has its highest amplitude ($V_{in,amp} = V_{ref}$). From Fig 3.11, when

Design Parameters	
C_S and C_I	400 fF
R_{SW}	200 Ω
OTA V_{in}^*	300 mV
OTA V_{load}^*	500 mV
OTA input g_m	3 mS
OTA A_{VO}	6000

Table 3.1: Design parameters obtained from model and circuit iterative design.

$V_{in,amp} = V_{ref}$ the DSM ADC has a dynamic range of 80.1 dB, which corresponds to 13 bits of resolution. Fig 3.12 is used to show the bandwidth of the DSM. As long as the signal is within the specified bandwidth of 100 kHz, the DSM ADC can achieve high resolution. Aliasing occurs as soon as the input signal frequency exceeds the bandwidth, and the performance of the DSM ADC significantly falls as expected. An example that shows the operation of the DSM model presented here is provided in Appendix A.
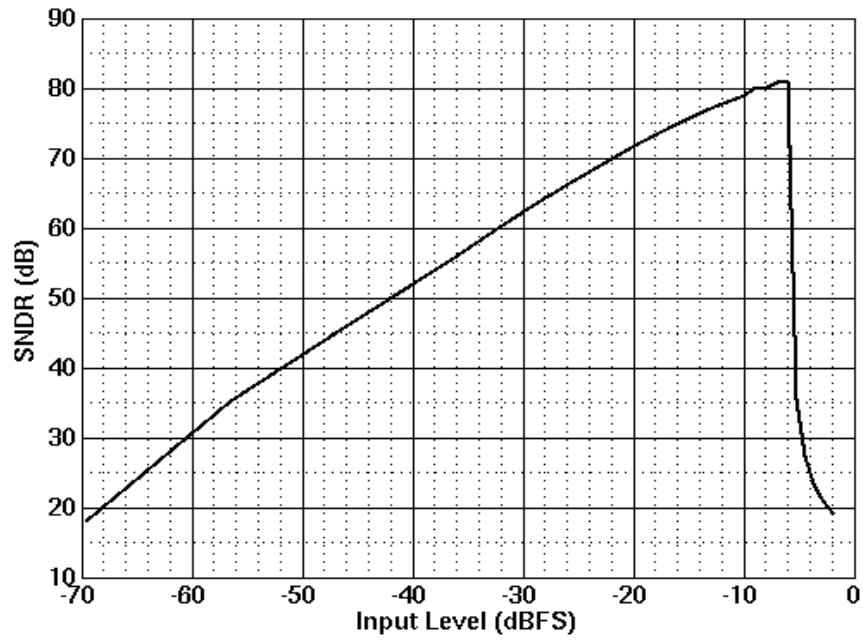
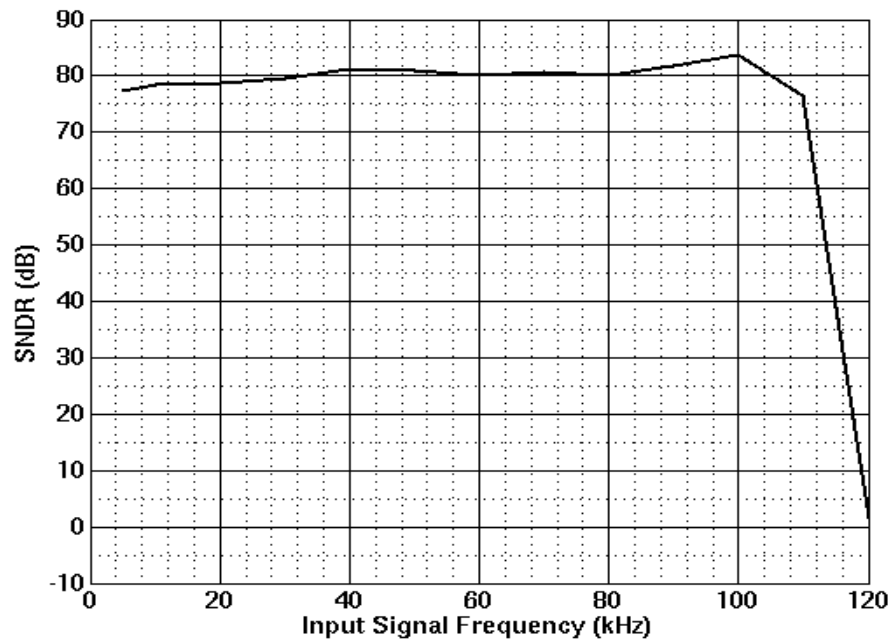Figure 3.11: SNDR versus normalized input amplitude.

Figure 3.12: SNDR versus input signal frequency.

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Chapter 4

Circuit Implementation

In order to use the model to estimate the performance of the DSM, certain parameters were required, such as C_S, C_I, device g_m, R_{sw}, etc. The choice of these parameters and the design of the circuit is done with the analysis of the previous chapter in mind. To arrive at the final parameters, an iterative process was performed in which the analysis/modeling of the previous chapter guided the circuit design, the parameters extracted from the circuit were entered into the model, the resulting performance was analyzed, and the circuit and its parameters were iteratively modified until the desired performance was achieved. This chapter presents the analysis performed to design each circuit block along with the final parameters chosen, which were presented in table 3.1. The resulting performance simulations with the physical circuit parameters included are then provided. The circuit simulation performance results are also compared with the model's performance results.

4.1   Sampling Network

Fig. 3.5 showed the circuit implementation of the DSM with the sampling network included, and it is reproduced here for convenience in Fig. 4.1 with the delays and phases of each switch included. The necessity for delayed switches and different phases will be discussed in the next section. The sampling network consists of the switches and capacitors used for sampling the input
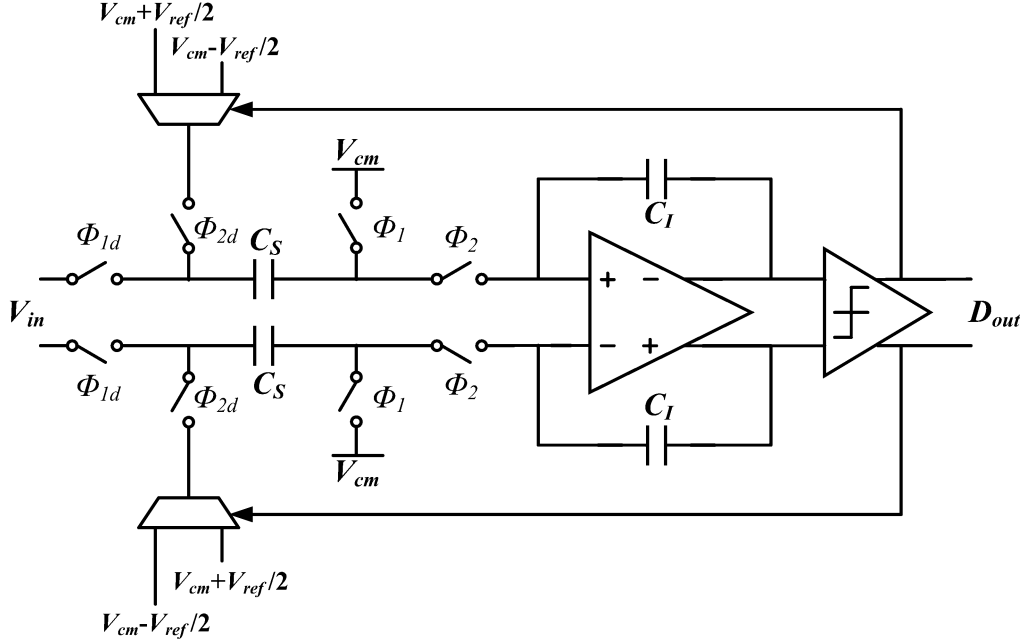
Figure 4.1: Circuit implementation of the first-order DSM.

and performing the integration. The switches are implemented as transmission gate switches to reduce clock feedthrough and to reduce the nonlinear dependency of the switch resistance on the input voltage. As shown in Fig. 4.1, the sampling network utilizes bottom-plate sampling; a decision made to reduce the charge injection and further reduce the clock feedthrough.

In equation 3.35, it was shown that the sampling network introduces additional settling error. To ensure the impact is negligible, it is typically desired to keep this error to less than one least significant bit (LSB). The LSB is dependent on the full-scale range V_{FS} of the DSM, which is twice the reference voltage V_{ref} used for the DSM. Note that the maximum value allowed for V_{ref} is specified from the design of the OTA, which will be discussed in section 4.3. The LSB value can be expressed as

$$V_{LSB} = \frac{V_{FS}}{2^B} = \frac{2 \cdot V_{ref}}{2^B}, \tag{4.1}$$

where B is the bit resolution desired. To keep the settling error due to sampling within one LSB

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the expression that must hold true is

$$V_{in,amp} \cdot \exp\left(\frac{-t_s}{\tau_{samp}}\right) < \frac{V_{LSB}}{2}, \tag{4.2}$$

where the factor of 2 is due to the fact that the analysis being presented here is done on only half of the DSM circuit since any one switch and capacitor pair only samples half of the differential signal. The worst-case error occurs when the input is largest, which occurs when $V_{in,amp} = V_{FS}/2 = V_{ref}$. Rearranging expression 4.2 to isolate the necessary time constant and replacing $V_{in,amp}$ with V_{ref} yields

$$\tau < t_s \frac{1}{\ln(2^B)}. \tag{4.3}$$

Since $\tau = R_{sw}C_S$, the bound on R_{sw} is

$$R_{sw} < \frac{t_s}{\ln(2^B)C_S}, \tag{4.4}$$

where R_{sw} is the overall resistance of the transmission gate switches used for the circuit.

As expected, the necessary R_{sw} is dependent on the value of C_S chosen for the sampling network. C_S is typically chosen such that the sampled noise that results does not limit the DSM. Equation 3.42 showed the relationship between the total sampling in-band noise and C_S. To ensure 10 bit resolution, the minimum value for C_S can be approximately established by satisfying the expression

$$SNR = 10 \cdot \log\left(\frac{\frac{1}{2}V_{ref}^2}{v_{n,in-band}^2}\right) > 62\,\mathrm{dB}, \tag{4.5}$$

similar to [27]. In equation 4.5,

$$\overline{v_{n,in-band}^2} = \frac{4k_B\mathrm{T}}{C_S}\frac{1}{OSR} \tag{4.6}$$

since the SNR in equation 4.5 is based on the differential DSM.

As an example with values used for the differential DSM, setting $V_{ref} = 300$ mV, T= 297, $B = 10$, and the input bandwidth to 100 kHz, which leads to an OSR of approximately 3,750, the minimum sampling capacitance necessary to satisfy expression 4.5 is 0.154 fF. The result is due

to the high oversampling rate that spreads out the noise across the sampling frequency spectrum, thus reducing the in-band noise and the capacitor size needed to keep the sampled noise level within a bound. The reduced sampling capacitance needed turns out to be a major advantage of the DSM over Nyquist sampling converters. However, setting $C_S = 0.154$ fF would lead to undesirable results since the parasitic capacitances in the DSM circuit will surely be along the same order of magnitude as the sampling capacitance, thus altering the DSM dynamics. For this reason, a sampling capacitance of 400 fF was eventually chosen so that the capacitance would be large enough to make parasitic capacitances negligible yet small enough to allow the DSM to operate at high speeds. C_I was set to 400 fF as well, with the choice explained in section 4.3.1 that discusses the design of the OTA core. Revisiting expression 4.4 with C_S set to 400 fF, the bound under which the switch resistance must remain to meet design constraints is approximately 240 Ω. To provide margin, the transmission gate switches implemented for the DSM were designed to have a resistance under 200 Ω across the entire input range of $\pm V_{ref}$. Fig. 4.2 provides the simulation results for the
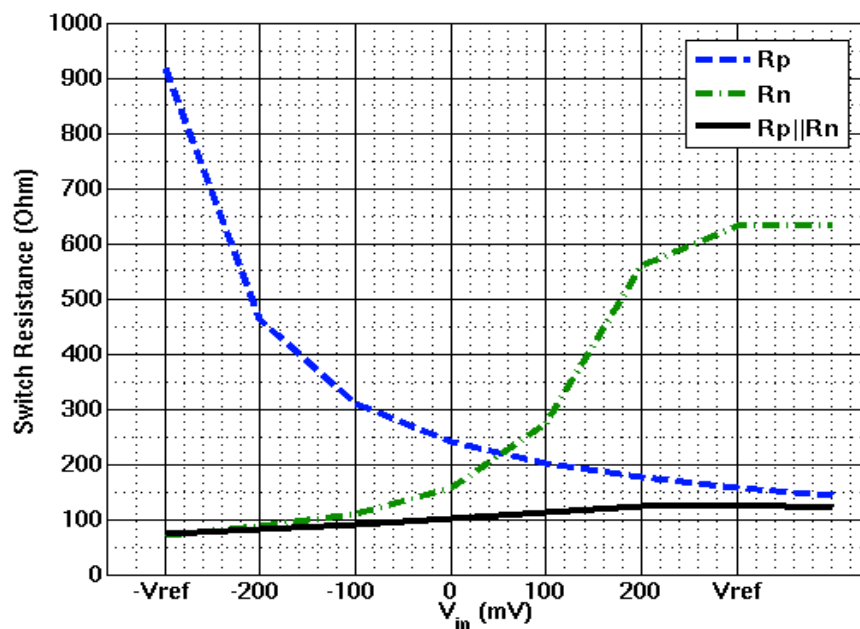

Figure 4.2: Switch resistance across the input range.

Sampling Network Design Parameters	
C_S and C_I	400 fF
TG Switch W_n/L_n	22μ/130n
TG Switch W_p/L_p	30.8μ/130n

Table 4.1: Physical design parameters for the sampling network transmission gate switches and capacitors.

switch resistance of the transmission gate switches implemented, as well as the switch resistance if only an NMOS or PMOS device were used to implement the switches. As shown and expected, the transmission gate linearizes the overall resistance across the input range by reducing the resistance dependency on the input, and is well within the required resistance range.

Note that in sizing the switches of the DSM circuit of Fig. 4.1 to meet the desired resistance constraint, linearity and charge-injection should be considered. To target linearity, the delayed switches, Φ_{1d} and Φ_{2d}, should be sized such that the resistance of the PMOS and NMOS devices are equal. Although the non-delayed switches, Φ_1 and Φ_2, can be sized to have equal PMOS and NMOS sizes to reduce charge-injection, this is not as critical since the fully-differential bottom-plate sampling configuration of the DSM further mitigates the effect of signal-dependent charge injection. Therefore, the delayed switches were used to implement the non-delayed switches as well. With R_{sw}, C_S, and C_I established, the sampling network circuit is completed. The final parameters used for the switches and capacitors of the sampling network are provided in table 4.1.

4.2   Non-overlapping Clock Generator

The previous section specified that essentially four clock signals would be needed to implement the sampling network; Φ_1, Φ_{1d}, Φ_2, and Φ_{2d}. This clocking scheme consisting of the four signals is necessary to take advantage of the benefits of bottom-plate sampling. Fig. 4.3 (b) provides a timing diagram of the clocking scheme. Consider the sampling capacitor when both Φ_1 and Φ_{1d} are on. As Φ_1 is disconnected, the injected charge due to turning off the switch is constant, and is
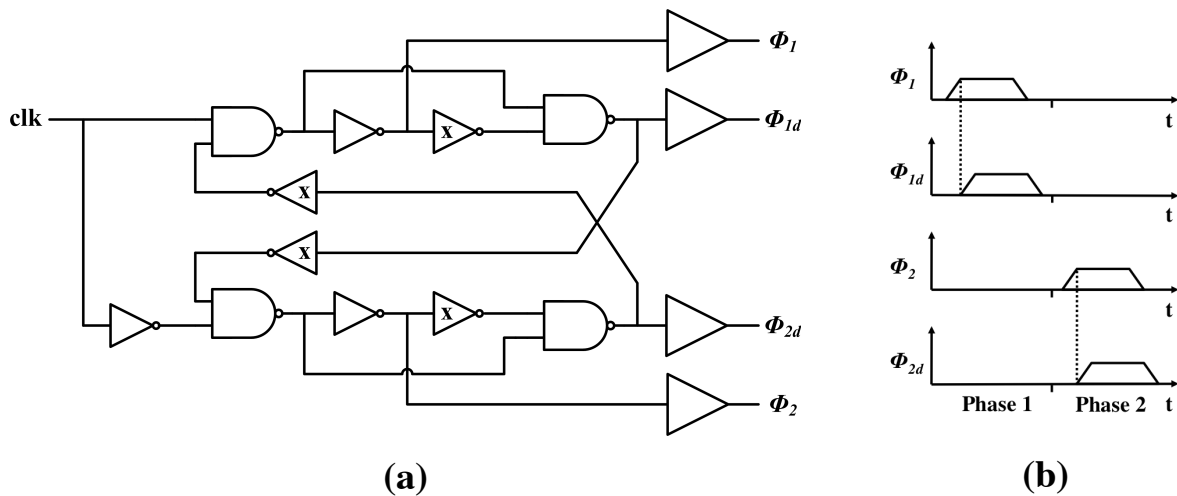
Figure 4.3: (a) Schematic of the non-overlapping clock generator and (b) the timing diagram for the clocking scheme.

therefore eliminated since the DSM is differential [18]. When Φ_{1d} is turned off, the bottom plate of C_S is already open, and thus no signal dependent charge is injected on C_S. The schematic of the non-overlapping clock generator used to generate the four clock signals for the clocking scheme is presented in Fig. 4.3 (a). Note that the four inverters marked with an 'X' in Fig. 4.3 (a) can be tweaked in size to adjust the delay and the non-overlap time.

4.3 Operational Transconductance Amplifier

The OTA is the key analog block of a DSM because its performance impacts the overall performance of the DSM more than any other block. Furthermore, the relaxation of the constraints of the other analog blocks is primarily a result of the integrator's high DC gain that essentially makes most of the error after the integrator negligible when referred back to the input. The key final parameters of the OTA were previously presented in table 3.1. In this section, the circuit design technique that utilized these parameters and was employed in parallel with the model optimization is discussed.

4.3.1   OTA Core

In choosing the architecture for the OTA, meeting the required high DC gain specification while maintaining stability and a suitable settling response was the target. While a two-stage amplifier would certainly be able to achieve the high DC gain requirement, stability becomes an issue when operated at frequencies approaching the GHz range. Furthermore, a two-stage amplifier is more susceptible to overloading of internal nodes, which no longer allows the OTA to be modeled by one pole. To ease the modeling of the OTA and mitigate any effects of overloading internal nodes, a single-stage OTA architecture was chosen. Considering that the OTA will need to operate at 750 MHz, the selection of a single-stage OTA is reaffirmed since a single-stage OTA can be modeled by a single pole and is inherently more stable than a two-stage OTA. With the OTA loaded by 400 fF integrating capacitors, stability is less critical since the load capacitance automatically acts as a compensation capacitor to stabilize the OTA. Moreover, the supply voltage for the OTA is 3.3 V, which is more than sufficient to allow multiple devices to be stacked to exploit the intrinsic $g_m r_o$ gain of the devices. This allows the OTA to meet the high DC gain specification without the need for a second amplifier. The schematic for the OTA is provided in Fig. 4.4.

To start the design, the transistors were characterized to identify the ideal operating point for the devices, which required trading off between high-speed operation, power/gain efficiency, and swing. Noise was also taken into account in specifying the operating points because as was shown in equation 3.43, a smaller input device V^* yields a smaller noise factor. From characterization and consideration of all the mentioned factors, V_{M1}^* (the input device V^*) was chosen to be 300 mV. Since V_{M6}^* directly impacts the noise, its value was set to 500 mV, which was the largest it could go without drastically impacting the power/gain efficiency and lowering the output swing. Although V_{MCS}^* also directly affects the noise factor, it could not be set too high since it also directly limits the maximum input swing allowed on the OTA, and therefore was set to 200 mV. The integrating capacitor, which strongly impacts the overall OTA load capacitance, can be sized to further improve the dynamic range at the output of the OTA should the noise factor be too large. The most important factors in deciding the operating point for the cascode devices are swing
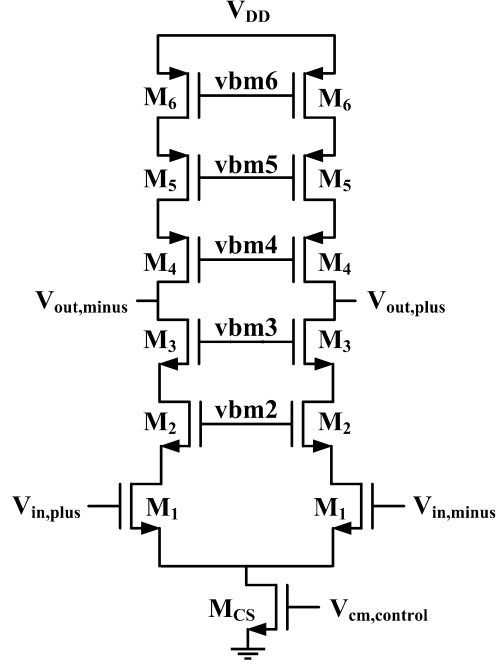
Figure 4.4: Circuit schematic of the OTA.

and efficiency, and therefore V_{M2}^*–V_{M5}^* were all set to 300 mV.

Using the V* values specified, the maximum output swing of the OTA can be calculated as

$$V_{o,swing,max} = V_{DD} - V_{M1}^* - V_{M6}^* - V_{MCS}^* - 4 \cdot V_{M2}^* = 1.1\,\text{V}. \quad (4.7)$$

Note that the output swing calculation is not essential to the design of the OTA here since the maximum input swing is specified independent of the output swing. The maximum differential input swing at the OTA input is

$$V_{in,swing,max} = [V_{DD} - V_{M6}^* - 4 \cdot V_{M2}^* + V_{\text{TN}}] - [V_{MCS}^* + V_{\text{TN}} + V_{M1}^*] = 1.1\,\text{V}. \quad (4.8)$$

The slew rate is the parameter that actually determines the maximum input swing of the DSM, which is different than the input swing of the OTA because of the feed-forward factor. With $V_{M1}^* =$

300 mV, the maximum amplitude at either input of the DSM is evaluated as

$$V_{in,amp,max} = \frac{V_{M1}^*}{FF_I}.$$

(4.9)

where FF_I is the same feed-forward factor presented in equation 3.23. Since both inputs experience the same max amplitude limitation, the maximum input differential swing of the DSM becomes

$$V_{in,diff,swing} = V_{FS,diff} = 2 \cdot V_{in,amp,max}.$$

(4.10)

At this point, the sampling capacitor can be specified based on the input swing, but its value was calculated and set to 400 fF in section 4.1 based on setting V_{ref} to 300 mV. To maintain loop stability by limiting the loop gain, the integrating capacitor C_I is typically set to be greater than or equal to C_S. Therefore, C_I was set to 400 fF since this was the smallest value it could have before the capacitive gain became greater than one. After arriving at an estimate for the parasitic load capacitance of the OTA based on the implemented circuit of the OTA, the capacitive gain is found to be 1, the feedback factor F_I is 0.49, and the feedforward factor FF_I is 0.75. From equation 4.9, the maximum $V_{in,amp,max}$ is found to be 0.4. With all the necessary parameters available, the SNR can be evaluated at the output of the OTA to determine if the dynamic range is sufficient or if parameters need to be modified to achieve better dynamic range. The maximum SNDR at the output is evaluated as

$$SNR = 10 \cdot \log \left(\frac{\frac{1}{2} V_{ref}^2}{v_{n,OTA}^2 \frac{1}{F_I}} \right) = 10 \cdot \log \left(\frac{\frac{1}{2} V_{ref}^2}{\frac{2 k_B T}{C_{L,eff,CL}} \frac{nf}{F_I}} \right).$$

(4.11)

Letting $V_{ref} = V_{in,amp,max}$, the maximum SNR at the output is calculated to be 63.5 dB, which meets the specification and thus confirms the choices made for the design parameters. This value for the SNR at the output will more than likely improve due to additional parasitic capacitance at the output of the OTA that is not modeled.

To arrive at the values for A_{vo} and g_m, all the previous parameters were entered into the model and optimized. The model takes into account all the non-idealities and error factors, both

static and dynamic, presented in section 3.3. The final parameters that produced the results given in section 3.3 were $A_{vo} = 6,000$ and $g_m = 3$ mS. The necessary current and output impedance requirements can be deduced from all the previously specified parameters. The low frequency gain A_{vo} of the OTA is evaluated as

$$A_{vo} = g_{m1} \cdot (g_{m2}r_{o2} \cdot g_{m3}r_{o3} \cdot r_{o1} \,\|\, g_{m4}r_{o4} \cdot g_{m5}r_{o5} \cdot r_{o6}) . \tag{4.12}$$

With g_{m1} and V_{M1}^* set, the bias current for the OTA can be establish since

$$g_{m1} = \frac{2I_d}{V_{M1}^*} = \frac{I_{SS}}{V_{M1}^*} . \tag{4.13}$$

The transconductance of all other devices is specified as well since the same bias current flowing through the input devices flows through the other devices, and V^* for each of the devices was already set. The key degree of freedom in sizing the devices of the OTA is the channel length. As shown in equation 4.12, the DC gain is strongly dependent on the intrinsic r_o of the devices, which is strongly dependent on the channel length of the devices. Therefore, it is desirable to make the channel lengths for all the devices other than the input device as large as possible, so long as their capacitive loading on internal nodes does not affect the bandwidth of the OTA. The final sizes for the OTA core are provided in table 4.2.

As can be seen from the schematic of the OTA given in Fig. 4.4, the output common mode is

OTA Core Design Parameters	
M_{CS}	73µ/400n
M_1	5.7µ/130n
M_2	58µ/1µ
M_3	28µ/500n
M_4	82µ/500n
M_5	214µ/1µ
M_6	37µ/500n

Table 4.2: Physical design parameters for the core OTA circuit.

dependent on device parameters, which means it is poorly defined. For this reason, a common-mode feedback network must be included to set the output common mode of the OTA. In Fig. 4.4, the common-mode is controlled via the bias voltage of the tail current source, $V_{cm,control}$, which comes from the common-mode feedback network discussed next.

4.3.2   Common-Mode Feedback Network

Common-mode feedback is required in fully differential amplifiers to define the voltages at the high impedance output nodes. The main purpose of the common-mode feedback network is to ensure that

$$I_{d,M6} = \frac{I_{d,M_{CS}}}{2}. \tag{4.14}$$

To achieve this, common-mode feedback networks perform two tasks; sense the common-mode output of the amplifier, and adjust a parameter of the amplifier to set the output common-mode.
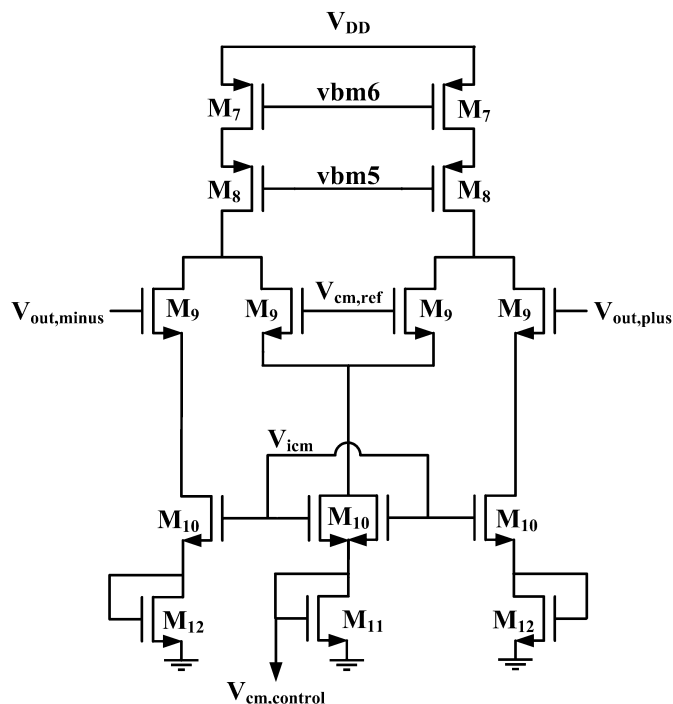

Figure 4.5: Circuit schematic of the common-mode feedback network.

The schematic of the circuit used to implement the common-mode feedback network is provided in Fig. 4.5. The topology of the network was chosen because it accurately represents the current sources in the main amplifier, and it provides minimal loading on the output of the amplifier. The M_7 devices are sized and biased exactly the same as the M_6 devices of the OTA to accurately represent the current source loads of the OTA. The M_8 devices are also sized and biased exactly the same as the M_5 devices of the OTA so that the M_7 current source devices have a V_{DS} approximately the same as the V_{DS} of the M_6 current source devices. The M_9 devices create a differential pair to compare the output of the OTA to the specified common-mode voltage $V_{cm,ref}$. The M_{10} devices, similar to the M_8 devices, are sized and biased exactly the same as the input so that the M_{11} current source device has a V_{DS} approximately the same as the V_{DS} of the M_{CS} current source device of the OTA. So as not to consume excess current in the common-mode feedback circuit, the current source device is biased with $I_{SS}/2$ but is sized so that V^* is the same as M_{CS}. The V_{GS} of the M_{11} device, $V_{cm,control}$, is fed back to the OTA to set the output common-mode. The only drawback to the use of this topology for the common-mode feedback network in our system is that for the network to work properly the M_9 devices must always be on, which limits the swing on the OTA output. The highest the output voltage of the OTA can go without turning off a device in the common-mode feedback network is given by

$$V_{out,max} = V_{DD} - V^*_{M7} - V^*_{M8} - V_{TH,M9} - V^*_{M9}. \tag{4.15}$$

CMFB Network Design Parameters	
M_7	37μ/500n
M_8	214μ/1μ
M_9	20μ/280n
M_{10}	5.7μ/130n
M_{11}	36.5μ/400n
M_{12}	18.25μ/400n

Table 4.3: Physical design parameters for the common-mode feedback network.
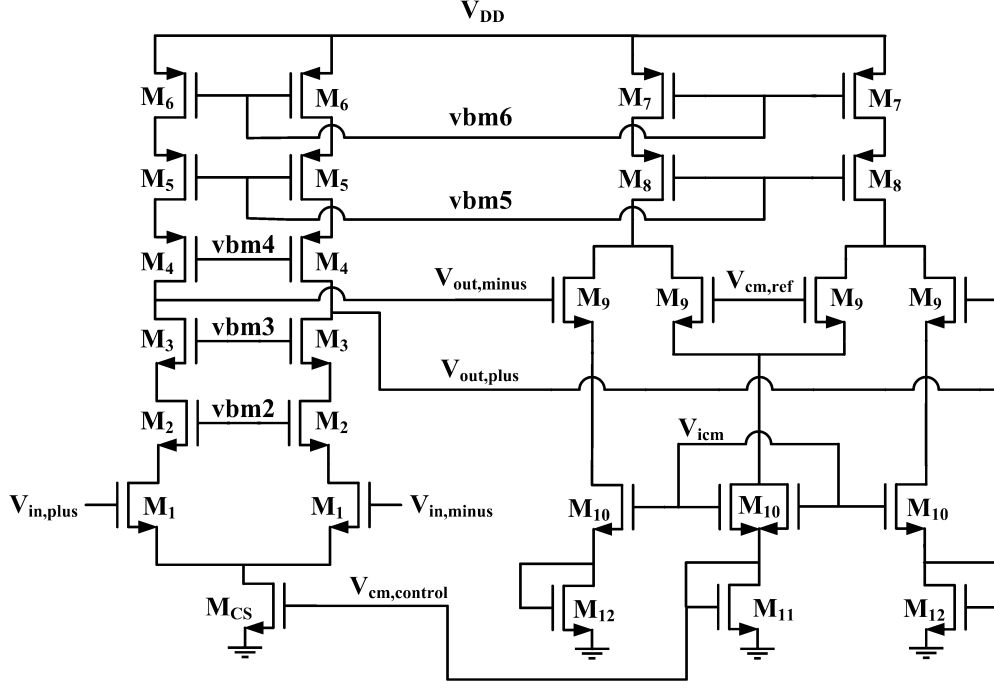
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Figure 4.6: Complete circuit schematic of the OTA with common-mode feedback network included.

With the V^* and V_{TH} of the M_9 devices set to 280 mV and 260 mV, respectively, the maximum output voltage of the OTA is approximately 1.96 V. With the output common-mode set to 1.66 V, approximately half of the supply voltage, the new maximum differential swing at the output is $\pm$ 300 mV. Since the capacitive gain of the DSM is 1, the new maximum input swing of the DSM is also $\pm$ 300 mV. For this reason, V_{FS} is set to 600 mV, and as a result V_{ref} and $V_{in,amp,max}$ are both 300 mV. The complete schematic of the OTA with both the core amplifier and the common-mode feedback network connected is provided in Fig. 4.6. For more details explaining this type of common-mode feedback network and other common-mode feedback network options, refer to [24]. The final sizes of the devices in the common-mode feedback network are provided in table 4.3.

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4.4 Comparator

The final significant block that is needed to implement a DSM is the comparator. As mentioned before, the constraints on the comparator concerning noise and input offset, typically the most important two constraints for comparators, are relaxed because the high DC gain of the integrator that suppresses these errors when referred to the input. For the DSM designed here, the comparator consists of a preamplifier followed by a regenerative latch.

4.4.1 Preamplifier

The preamplifier is necessary for the DSM designed here for two reasons; (1) it provides suppression of the kickback effect from the latch, and (2) to overcome the latch offset when the signal is extremely small. Reducing the kickback effect is important so that the clock strobe to the inputs of the latch do not disturb the value stored on the integrating capacitors. Fig. 4.7 provides the circuit schematic for the preamplifer. The bipolar devices were used to achieve high gain at a faster speed. The input NMOS devices are necessary because the bipolar devices cannot be used as input devices since the value stored on the integrating capacitors after the integration is complete can potentially leak away through the base resistance of the bipolar devices. Therefore, the NMOS devices are
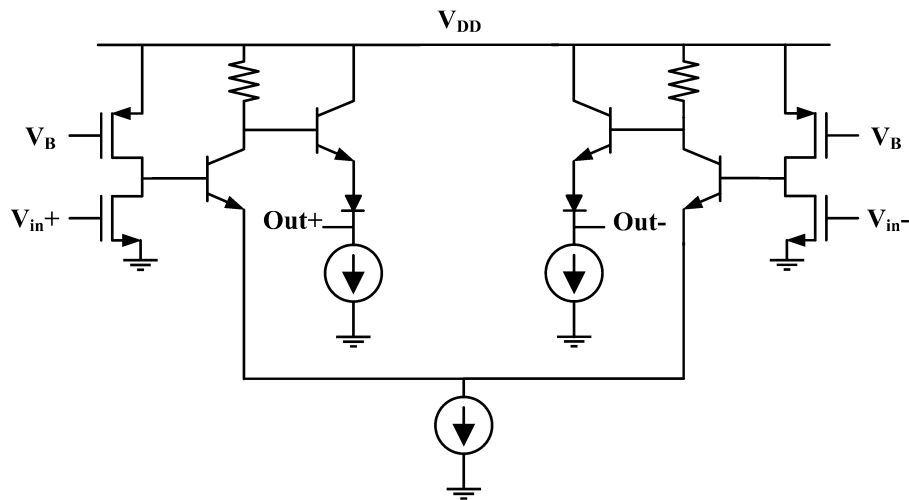

Figure 4.7: Circuit schematic of the comparator preamplfier.

Preamplifier Design Parameters	
M_{in}	36μ/280n
M_{bias}	52μ/280n
Q_{amp}	3μ
$Q_{follower}$	2μ

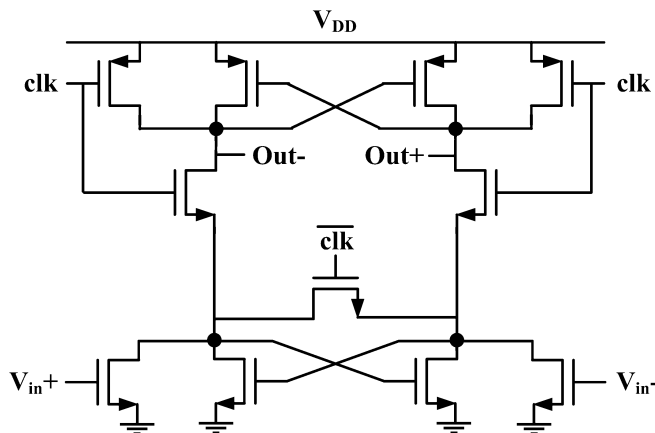Table 4.4: Physical design parameters for the preamplifer circuit.

Figure 4.8: Circuit schematic of the comparator regenerative latch.

simply buffers. The third stage is simply a level shifter using diodes to shift the output of the preamplifier operating off of a 2.5 V supply to the input range of the digital latch that operates off of the lower digital voltage supply, 1.2 V. The final sizes of the devices in the preamplifier are provided in table 4.4.

4.4.2 Regenerative Latch

With the design of the latch, the main priority is speed since the error contributions are not significant due to the high DC gain of the integrator, as mentioned. The circuit schematic of the regenerative latch is provided in Fig. 4.8. The architecture is very similar to the standard Strong Arm latch, often referred to as a Yukawa latch. During the off phase the PMOS devices and the NMOS devices are isolated, the output is charged to V_{DD}, and the NMOS drains are connected
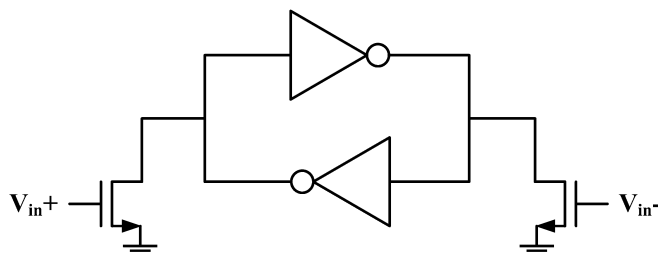
Figure 4.9: Simplified schematic of the regenerative latch during the on phase.

Latch Design Parameters	
M_{in}	15μ/130n
$M_{precharge}$	2μ/130n
M_{reset}	1μ/130n
$M_{evaluate}$	2μ/130n
M_{crossn}	8μ/130n
M_{crossp}	8μ/130n

Table 4.5: Physical design parameters for the regenerative latch circuit.

together to eliminate hysteresis. During the on phase, the NMOS and PMOS cross-coupled pairs are connected to each other. The simplified schematic of the regenerative latch during the on phase is provided in Fig. 4.9. Initially, both outputs start at V_{DD}. As time passes, both of the input NMOS devices discharge the outputs with the NMOS having a higher V_{GS} discharging the output at a faster rate. The cross-coupled pairs reinforce the discharging, and eventually the output being discharged at a faster rate is sufficient to switch the state of the other output, thus locking the outputs to their desired values. The most important issue that must be closely monitored is the sizing of the input devices. They should be large enough to be able to discharge the outputs, and cause the switching threshold to be reached, but they must be small enough not to discharge the output if the output is being charged to V_{DD} via the PMOS devices. The final sizes of the devices used in the regenerative latch are provided in table 4.5.

4.5 Results

To achieve sufficient image resolution, the delta-sigma modulator must provide 10 bits of resolution of DC signal, which corresponds to 62 dB. For circuit design purposes, to provide margin and account for fabrication variability the specified signal bandwidth was set to 20 kHz, which is essentially DC when sampled at a frequency of 750 MHz.

The circuit was implemented in a commercial BiCMOS 130 nm process. Complete pre-silicon simulations of DSM circuits are typically not performed because they require simulations of extremely long data traces due to the oversampled nature of the system [1, 18, 19]. However, for this report, 4 simulations were completed. The results are included in Fig. 4.10, which overlays the results with the modeled results presented in the previous chapter.
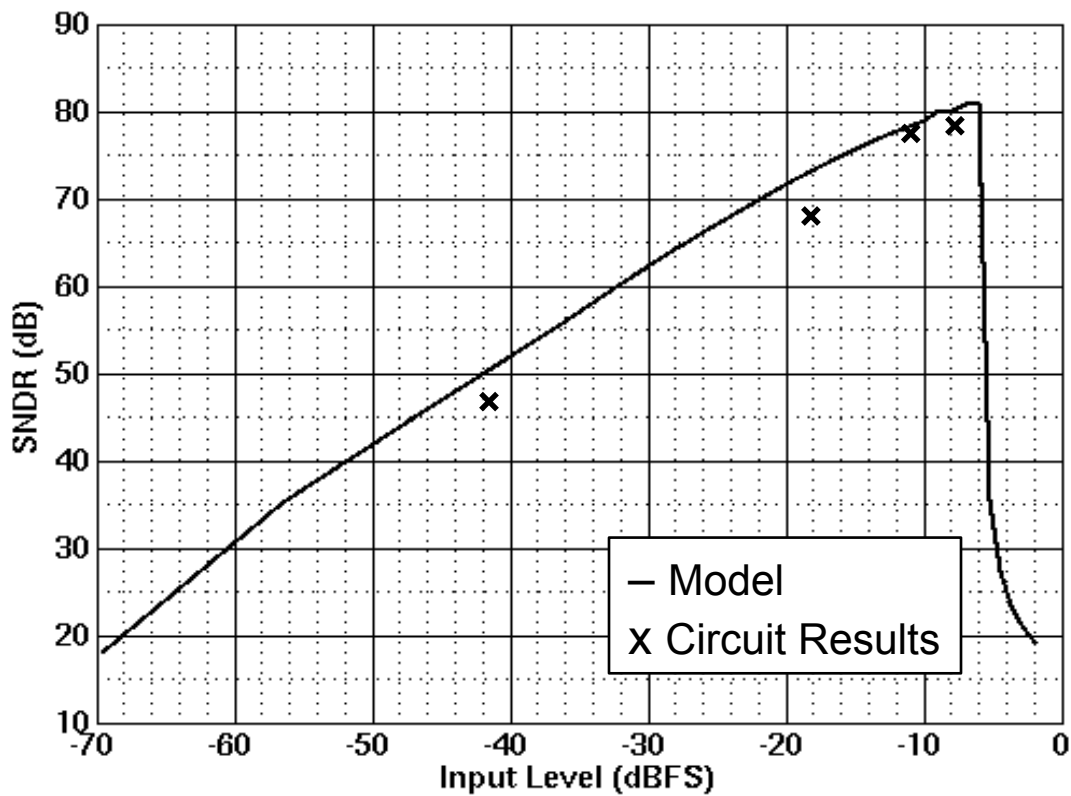

Figure 4.10: Results from the circuit overlaid on model results.

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The pre-fabrication circuit results of the DSM are summarized in table 4.6. A breakdown of the power consumption is provided in table 4.7. As can be seen from table 4.7, approximately 72% of the total power consumed by the DSM is consumed by the comparator. Therefore, significant power reduction can be achieved simply by optimizing the comparator for low power. This can most likely be done with minimal impact on the overall performance of the DSM because as has been mentioned before, the performance of the comparator is not a stringent constraint that impacts the overall performance of the DSM since the comparator's error is highly suppressed by the high DC gain of the integrator when referred back to the input.

DSM Circuit Results	
SNDR	79 dB
Input Signal Bandwidth	20 kHz
Sampling Frequency	750 MHz
Oversampling Ratio	18,750
Power Consumption	27.4 mW
Technology	130 nm BiCMOS
Die Area	205 x 132 μm^2

Table 4.6: Results for the delta-sigma modulator circuit.

Power Consumption Breakdown	
Integrator	6.02 mW
Comparator	19.8 mW
Sampling Network	0.971 μW
Non-overlapping Clock Generator	1.16 mW
Clock drivers	0.397 mW

Table 4.7: Power consumption breakdown for the delta-sigma modulator circuit.

Chapter 5

Conclusion

5.1 Summary

This work introduced a high-speed delta-sigma modulator for mm-Wave applications, and developed a model to predict the performance of the DSM and guide the circuit design. To illustrate the complete process a signal goes through when modulated by a delta-sigma modulator, an example using the model presented here was provided in the Appendix. The circuit design was heavily guided by use of the model, which led to an iterative process since the model depended on parameters that could only be determined after the circuit was designed. The target application of the DSM is the TUSI system, a wireless mm-Wave imaging system. Based on the requirements of the system, the model was optimized to identify the parameters necessary to physically implement the DSM. As proof of concept, the modeled DSM was implemented in a 130 nm BiCMOS process, and is currently in the fabrication phase. The physical DSM consumes 27.4 mW of power; 72% of which is consumed by the comparator.

5.2   Future Work

Although this work completely models the specified architecture, it does not aid in the actual choice of the architecture. It is more useful once the topology has been selected, but nonetheless models non-idealities that must be considered regardless of the architecture chosen for the DSM. To make the model more general, the model can be expanded to model the performance of multi-bit DSMs as well as higher-order DSMs. By doing so, the model can be utilized earlier in the project phase by predicting the performance of a larger number of architectures as well as identifying the design parameters needed to physically implement the chosen DSM architecture based on optimization. In addition to generalizing the model, the DSM implemented here will be measured once the chip returns, and a detailed comparison of the measurement results with the model and circuit results will be published separately.

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Appendix A

Example Simulations of a Test Signal

The DSM operation that utilizes the model to shape the noise and provide a high-resolution result is detailed next. The parameters used to perform the simulations are provided in table A.1.

Simulation Parameters	
Input Sinusoidal Frequency	15 kHz
Sampling Speed	750 MHz
Oversampling Rate	3,750
C_S and C_I	400 fF
R_{SW}	200 Ω
OTA V_{in}^*	300 mV
OTA V_{load}^*	500 mV
OTA input g_m	3 mS
OTA A_{VO}	6000

Table A.1: Simulation parameters for the appendix example.

Fig. A.1 shows the output PSD of the DSM. The noise shaping property that shifts the majority of the noise out-of-band is visible in the figure. From analysis of the PSD, the SNR is calculated to be 76 dB.
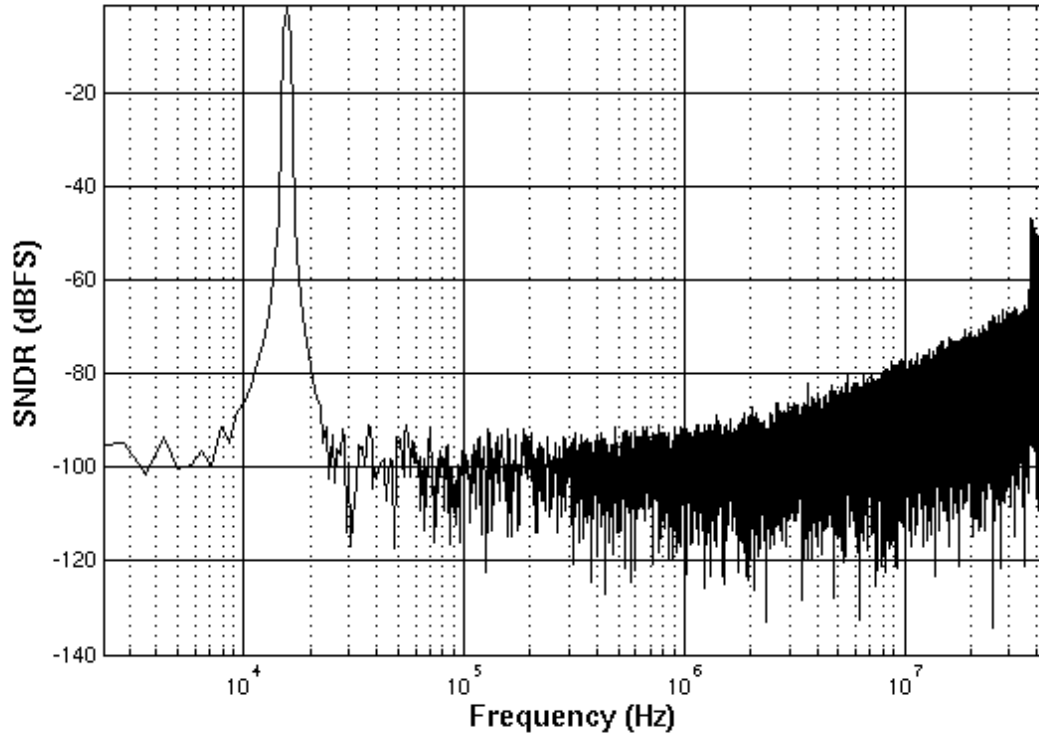

Figure A.1: Output PSD of the delta-sigma modulator.

After decimation is performed by the back-end processing, which filters out the out-of-band noise and down samples the DSM output, the signal can be reconstructed. Fig. A.2 provides the original time-domain signal as well as the reconstructed signal processed by the DSM. As can be seen from the figure, although the noise was shaped by the DSM noise transfer function, the integrity of the signal has not been distorted and the signal can be properly reconstructed with both amplitude and frequency correct.
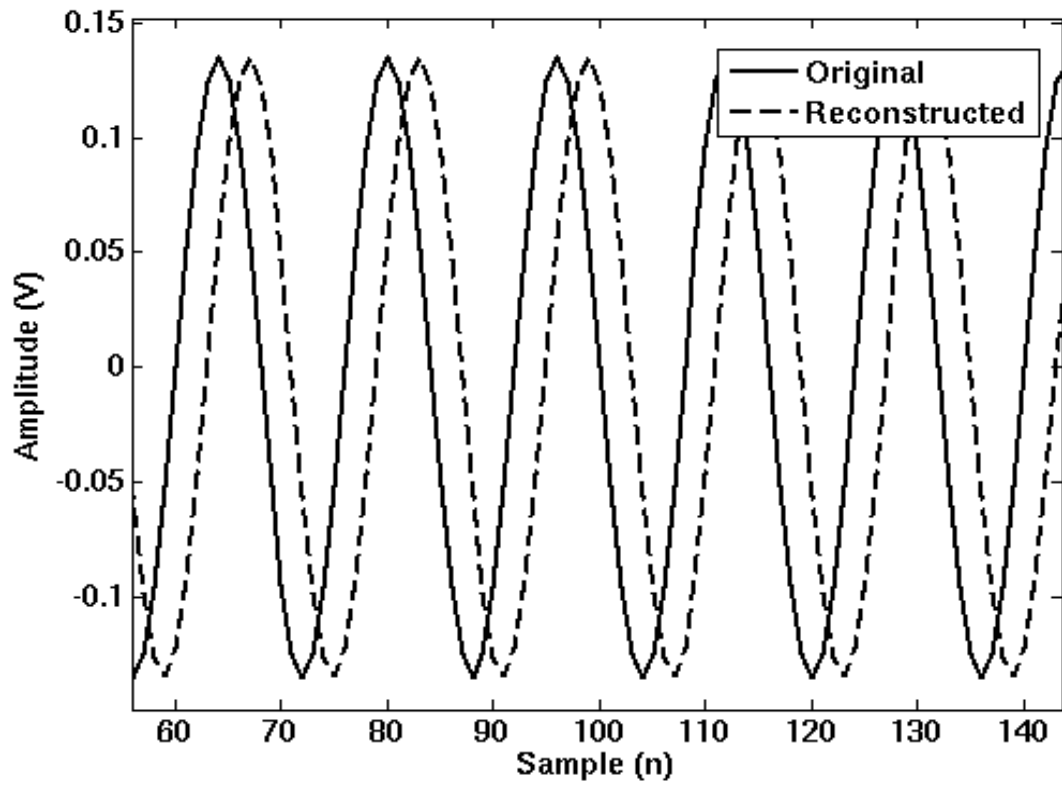
Figure A.2: Time-domain original signal and reconstructed signal after modulation by the DSM.