Zn Gas-Phase Doping of InAs Nanostructures

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Zn Gas-Phase Doping of InAs Nanostructures

by Steven Chuang

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

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Chapter 1

Introduction

Given the many challenges that silicon based transistors are facing in continued scaling, it has become highly attractive to consider alternate material platforms in the pursuit of high performance electronics, such as InAs for its high electron mobility. Traditionally InAs devices have suffered from many processing difficulties and high off currents. However many of these issues have been resolved with the introduction of III-V nanostructure on insulator platforms[1]. One interesting challenge that remains is the patterned p-type doping of InAs. The scarcity of photolithographically patternable p-type doping techniques is a major disadvantage of the InAs platform, as it prevents InAs from being applied to many known device structures. Furthermore, the commonly used ion implantation doping process induces irreversible crystal damage in InAs nanowires[2]. Even worse, the surface energy of InAs is known to be pinned in the conduction band, which makes p-type doping all the more difficult. In this project, first a novel patternable p-type doping technique was developed for InAs nanowires. In a subsequent project, this p-type doping technique was used to fabricate InAs nanoribbon tunneling field effect transistors.

This project is based off joint work with Alexandra C. Ford et. al [2][3].

Chapter 2

Zinc Gas Phase Doping of InAs Nanowires[1]

Section 2.1 Background

In the endless trend to shrink transistor dimensions to increase density and performance, planar devices are reaching the threshold for many desirable device characteristics[4]. To this end, many other novel transistor structures are being explored. In particular, much research has been devoted to transistors with nanowire (NW) channels due to their excellent electrostatic properties[5][6]. One very promising semiconductor for NW devices is InAs, due to its excellent electron mobilities[7][8][9], and ease of nanoscale, metal ohmic contact formation to the conduction band via solid source reactions[10]. However, there remain many challenges to be addressed with InAs NW device fabrication. Specifically, one fabrication issue that requires attention is the dopant profiling of InAs NWs. P-type doping of InAs NWs is particularly challenging given the surface electron-rich layer that causes the surface Fermi level to be pinned in the conduction band for an undoped NW. Although techniques such as in-situ doping during the growth have been previously reported for NWs[11][12][13], post-growth patterned doping is desired for most device fabrication schemes. Notably, conventional ion-implantation techniques are not compatible with nanoscale InAs semiconductors due

[1] Reprinted with permission from A. C. Ford, S. Chuang, J. C. Ho, Y.-L. Chueh, Z. Fan, A. Javey, Nano Lett., 10, 509–513, 2010. Copyright 2010 American Chemical Society.

to the severe crystal damage induced during the implantation process resulting in In atom clustering which cannot be fixed by a subsequent annealing process. In that regard, surface doping processes are highly attractive[14][15][16]. To address this need, here, we report patterned *p*-doping of InAs NWs with Zn atoms by using a post-growth, surface doping approach. The versatility of the approach is demonstrated by configuring the doped NWs into various device structures, including p^+-n diodes and *p*-MOSFETs.

Section 2.2 Methods

InAs NWs used in this work were grown using the vapor-liquid-solid (VLS) method by chemical vapor deposition in a two-zone tube furnace using a solid InAs powder source. As previously described, a 0.5 nm thick Ni film was annealed at 800 °C for 10 min to create nanoparticles that serve as catalysts[17]. A substrate temperature of 490 °C, source temperature of 720 ºC, pressure of 5 torr with H_2 carrier gas (200 SCCM flow rate) were used. The grown NWs were harvested by sonication in anhydrous ethanol and dropcasted onto Si substrates. To *p*-dope the NWs with Zn atoms, the samples were placed in a tube furnace with solid Zn powder used as the source. The NW substrate and Zn source were placed ~6 cm apart with the furnace temperature set at 400-415 ºC for 1 min (as counted from temperature stabilization time). A chamber pressure of 650 torr with Ar atmosphere was used. To achieve patterned doping, a SiO_2 mask was deposited to partially cover the NWs on the substrates. The diffusion length of Zn atoms can be approximated as $2\sqrt{Dt}$, where D is the diffusion coefficient and t is the diffusion time. A diffusion coefficient $D \sim 1.4\text{x}10^{-12}$ cm^2/s at 400 °C for Zn in InAs bulk substrates is reported in the literature[18]. Given this diffusion coefficient value, a

diffusion length of ~180 nm is estimated for *t*=1 min used in our experiments. This indicates that under our process conditions, InAs NWs are fully doped across their diameter (i.e., $d <$ diffusion length), but that Zn atoms are unable to diffuse far along the length of the NW or underneath the SiO_2 mask once incorporated into the NW. This is an important requirement for the fabrication of *p*-*n* junctions. This diffusion length is relatively small given that our devices are long channel devices with channel lengths of L=6-10 μm. In the future, shorter annealing times can be explored to further reduce the diffusion length, as needed for short channel devices[15]. It should be noted that the diffusion parameters used for this analysis are for the bulk substrates as there are no values reported for the NW system. In the future, detailed studies of dopant diffusion in various NW systems are needed to enable more accurate understanding of the process.

Section 2.3 Results

Subsection 2.2.a TEM Micrographs

Low-resolution and high-resolution TEM images of a Zn-doped InAs NW are shown in Fig. 1a&b. The high resolution TEM image shows the single-crystalline and defect-free nature of the doped InAs NW for which two planes, (222) and (220), are indexed. The diffraction pattern is shown in the inset with a [112] zone axis. Figure 1c shows the energy dispersion spectroscopy (EDS) quantitative analysis of a Zn-doped InAs NW for which the elemental composition of ~5 at. % Zn can be identified. Given the atomic density of $1.8\text{x}10^{22}$ cm^{-3} for InAs, this corresponds to a Zn concentration of [Zn] ~$9\text{x}10^{20}$ cm^{-3}. It should be noted that this concentration is over an order of magnitude higher than the [Zn] ~ $3\text{x}10^{19}$ cm^{-3} reported in the literature for bulk InAs

using a diffusion temperature of 500 ºC[18]. This may be the result of a fraction of the Zn atoms remaining on the surface of the NWs or that the NW system exhibits a higher solid solubility limit as compared to the bulk.

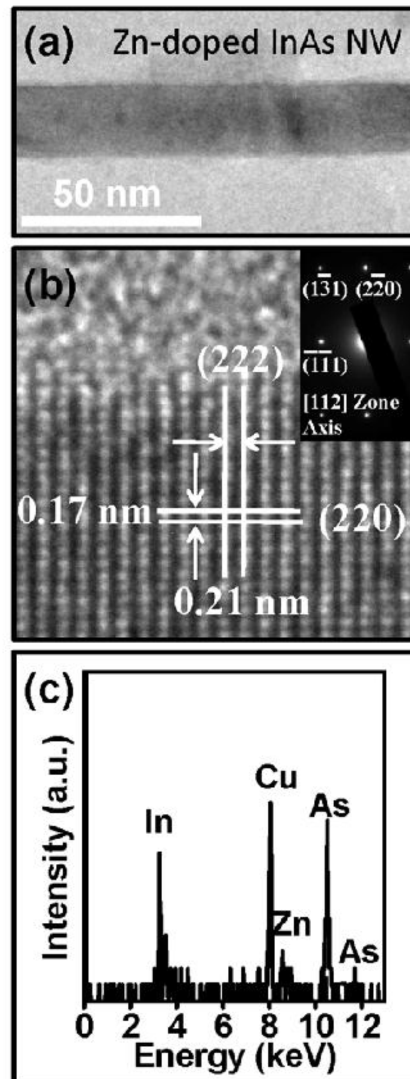

Figure 1: (a) Low-resolution and (b) high-resolution TEM images of a Zn-doped InAs NW with diffraction pattern shown in the inset. (c) EDS analysis of a Zn-doped InAs NW, depicting an elemental composition of ~5 at. % Zn.

Subsection 2.2.b Electrical Analysis

To characterize the electrically active content of Zn dopant atoms, various device structures were fabricated and tested. In one case, back-gated devices were fabricated by photolithography on the dropcasted NW substrates (p^+Si / 50 nm SiO_2) to define source (S) and drain (D). Ni was then thermally-evaporated into the S/D regions to form contacts. The inset in Fig. 2a shows a representative scanning electron microscope (SEM) image of such a back-gated NW device. Long channel lengths, L=6-10 μm, are used to make sure that transport of carriers is in the diffusive, as opposed to ballistic or quasi-ballistic, regime. This enables the extraction of intrinsic transport properties, such as carrier mobility. The *I-V* characteristics of a representative as-grown InAs NW and blank (i.e. unpatterned) Zn-doped InAs NW are shown in Figure 2. The as-grown InAs NW is n-type due to the high electron concentration that results from surface fixed charges and local imbalances in stoichiometry[19]. As previously discussed, there is a linear dependence of the device resistance on channel length, establishing that the Ni source/drain contacts to the conduction band of as-grown InAs NWs are ohmic[10]. The as-grown NW exhibits an *ON* current of ~4.4 μA at V_{DS} = 0.5V, $I_{ON}/I_{OFF} > 10^4$, and field-effect mobility of 4400 cm^2/Vs for channel length L = 8 μm and NW diameter d = 27 nm, consistent with the previously published observation[19]. The doped InAs NWs using the described process conditions are p^+ due to heavy Zn doping, exhibiting an ON current of ~0.4 μA at V_{DS} = 0.5V with minimal gate dependence (Fig. 2b). The linear behavior of the I_{DS}-V_{DS} plot (Fig. 2b inset) confirms that the contacts to the p^+ NW are near ohmic. This is primarily due to the thinning of the Schottky barriers at the contacts to the valence band of NWs arising from the heavy Zn doping. From the I_{DS}-V_{GS} characteristics, a hole

field-effect mobility of ~30 cm^2/Vs for a NW diameter of d ~ 30 nm is estimated. This field-effect mobility is reasonable given that the hole Hall mobility of bulk InAs substrates for a doping concentration of ~$1x10^{19}$ cm^{-3} acceptors is ~100 cm^2/Vs at room temperature and that the measured Hall mobility is always larger than the extracted field-effect mobility[20][21]. Using the conductance G ~ $6x10^{-7}$ S and d ~ 30 nm, the resistivity, ρ ~ 0.02 Ω-cm is estimated for the doped NW. From ρ and μ, the electrically-active [Zn] is estimated to be ~ $1x10^{19}$ cm^{-3}. This high electrically-active [Zn] corresponds to degenerate doping, with the Fermi level E_F located ~0.024 eV below the valence band edge E_v. This electrically active Zn concentration is consistent with those reported for various dopants in bulk InAs substrates[22][23]. While most (~70%) NWs exhibited p^+ behavior (minimal gate dependence) for doping temperatures of >400 ºC, some (~30%) NWs exhibited lightly p-type or ambipolar behavior. For doping temperatures <400 °C, roughly half of the NWs were ambipolar while the other half remained n-type. For the p^+ NWs, there was sufficient Zn doping to fully compensate the high intrinsic electron concentration, especially at the surface. However, for the ambipolar NWs, it is likely that the core of the NW is doped p-type while the high surface electron concentration "shell" remains n-type. This observation is especially expected for lower diffusion temperatures which effectively lowers the solid solubility limit of Zn.

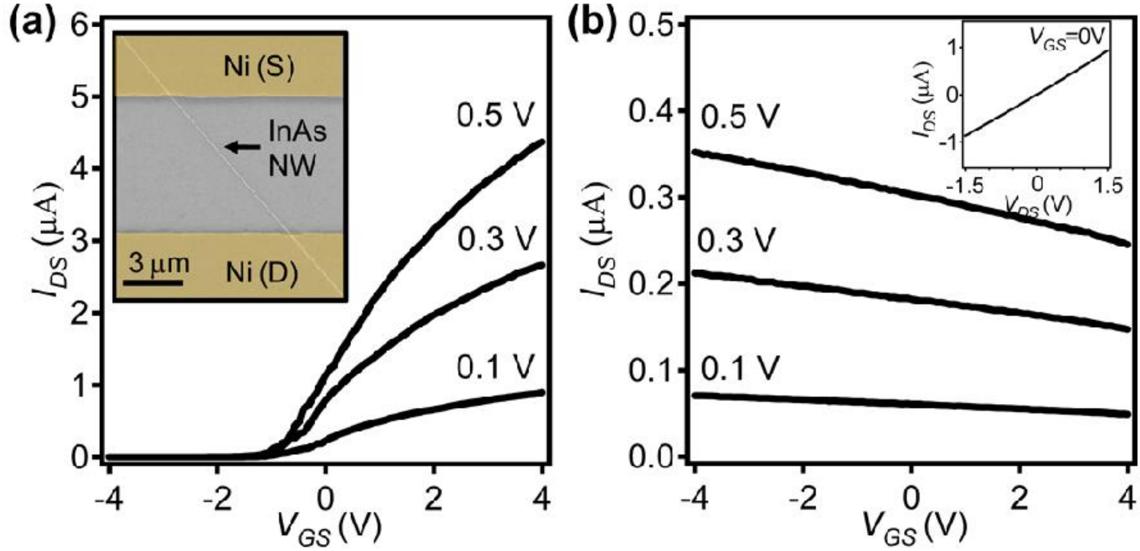

Figure 2: The I_{DS}-V_{GS} characteristics of a representative (a) as grown InAs NW with false-color SEM image of a representative device shown in the inset and (b) blank (i.e., unpatterned) Zn-doped InAs NW with I_{DS}-V_{DS} plot for V_{GS} = 0 shown in inset. The heavily doped Si substrate is used as the global back gate with a gate dielectric thickness of 50 nm SiO_2.

In order to show the versatility of the presented doping approach, various NW device structures involving dopant profiling were fabricated and tested. In one example, back-gated diodes were fabricated by patterned Zn doping of InAs NWs. The process flow is shown in Fig. 3a. First, 60 nm of Si_3N_4 was grown by PECVD on p^+ Si substrates. As-grown InAs NWs were then dropcasted on the nitride substrate and 70 nm electron-beam evaporated SiO_2 was deposited on photolithographically patterned regions to cover parts of the NWs, followed by lift-off of the resist. In this case, the evaporated SiO_2 served as the diffusion mask during the doping process. The NW substrates were then Zn-doped by the gas-phase surface doping process, with only the unmasked segments of the NWs exposed to Zn dopants. Ni contacts were then made to the Zn-doped segments of the NWs by photolithography and thermal evaporation. A final photolithography step, followed by etching in 50:1 HF to remove the SiO_2 mask and a

subsequent photolithography and Ni thermal evaporation were applied to contact the undoped regions (i.e., as-grown, *n*-type) of the NWs. The *I-V* behavior of a representative diode is shown in Figure 3b. Here, L ~ 7 μm and d ~ 28 nm. A rectifying behavior is observed for $V_{BG} > 0$. On the other hand, the device is insulating for $V_{BG} \leq 0$. This, along with the I_{DS}-V_{GS} curves of Figure 2, indicates that the Zn-doped region of the NW is in fact p^+ and is always in the hole accumulation mode, while the *n*-type region is being modulated by the back-gate. The *n*-type segment becomes fully depleted for $V_{BG} \leq 0$, but turns to the accumulation mode for $V_{BG} > 0$ and $V_{DS} > 0$. The ideality factor of the p^+-n diode shown in Fig. 3b is ~1.5, with the fit to the ideal diode equation indicated by the dotted line in the logscale inset.

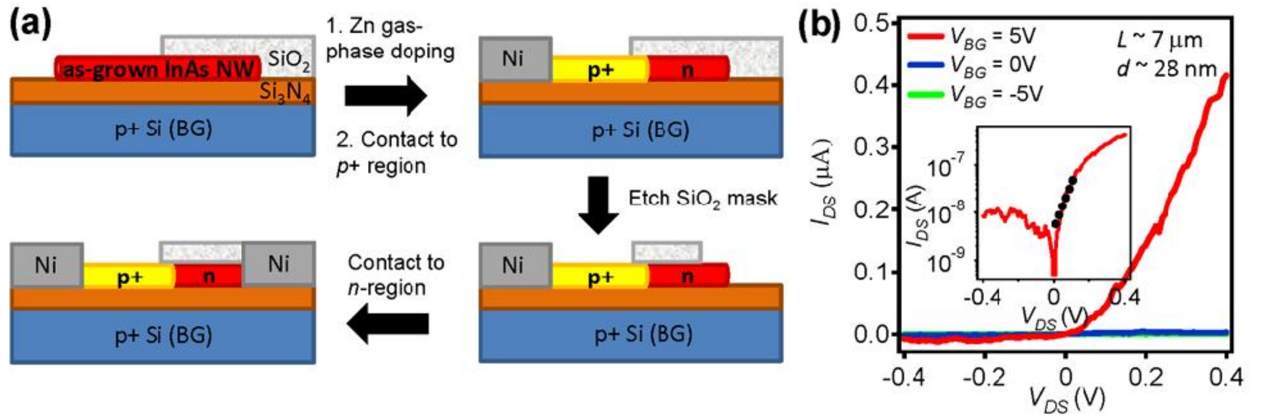

Figure 3: (a) The process flow for the fabrication of back-gated InAs NW diodes. (b)The I-V behavior of a representative diode as a function of the back-gate voltage, V_{BG}. The inset shows the log scale plot for V_{BG} = 5 V and the fit to the ideal diode equation indicated by the dotted line.

Next, back-gated InAs NW *p*-MOSFETs were fabricated utilizing the gas phase Zn-doping to define the p^+ S/D contacts, with a schematic of the process shown in Fig. 4a. Briefly, undoped InAs NWs were dropcasted on p^+Si/SiO_2 (50 nm thermally grown)

substrates and photolithography was used to pattern SiO_2 (~70 nm thick) mask regions on top of the NWs. The NWs were then Zn-doped as previously described. The exposed nanowire ends were made p^+ while the NW segment under the SiO_2 mask remained undoped. Photolithography and thermal evaporation were then employed to form the Ni contacts on the p^+ S/D regions. The heavily doped Si substrate was used as the global back gate with a gate dielectric thickness of ~50 nm SiO_2.

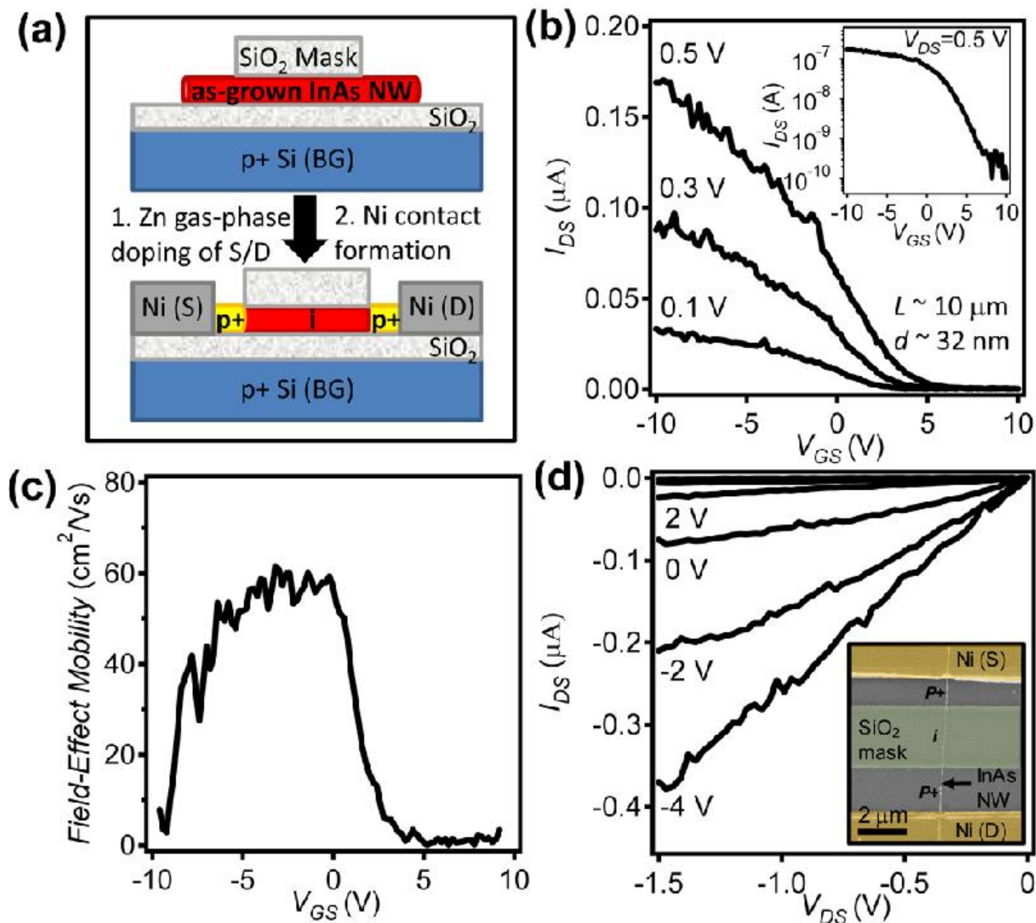

Figure 4: (a) A schematic of the back-gated InAs NW p-MOSFETs. (b) The I_{DS}-V_{GS} behavior of a representative p-MOSFET with the log scale plot shown in the inset. (c) Hole field-effect mobility of the device as a function of the back-gate voltage. (d) The output characteristics of the same NW p-MOSFET with false-color SEM image of a representative p-MOSFET shown in inset.

The *I-V* characteristics of a representative InAs NW *p*-MOSFET are shown in Fig. 4b&d, with an SEM image of a representative device as the inset in Fig. 4d. The *p*-MOSFET has I_{ON} ~ 0.17 μA and I_{OFF} ~ 0.1 nA at V_{DS} = 0.5V, with an $I_{ON}/I_{OFF} > 10^3$. The threshold voltage V_t is shifted to a positive voltage, likely as a result of fixed oxide and interface trapped charge states at the interface of the NW *n*-segment and the evaporated SiO_2 mask. The field-effect mobility as a function of V_{GS} is shown in Fig. 4c, with a peak hole mobility of ~60 cm^2/Vs. The hole mobility for InAs NWs is significantly lower than the electron mobility as expected. This mobility is ~9x lower than the Hall mobility of ~450 cm^2/Vs reported for lightly doped, p-type InAs bulk substrates[24]. The difference may be due to surface scattering and contact resistance associated with the field-effect mobility extractions. The *I-V* behavior of the patterned Zn-doped *p*-MOSFET is in distinct contrast to the behavior of the blank Zn-doped NW device shown in Figure 2b which exhibits minimal gate dependence. Furthermore, in contrast to the blank doped p^+ NW devices where the entire doped NW serves as the "channel" material, the *p*-MOSFET exhibits a higher hole mobility (~2x higher) since the channel is undoped resulting in minimal impurity scattering.

Subsection 2.2.c Comparison with Ion Implantation

For comparison, InAs NWs were also doped using Zn ion-implantation. Ion implantation energy of ~ 35 keV with dopant areal dose of 3.5×10^{12} - 3.5×10^{13} cm^{-2} were used, followed by thermal annealing at 375 ºC for 30 min. Back-gated devices fabricated from the Zn ion-implanted InAs NWs remained *n*-type with degraded ON currents and did not turn off, even after thermal annealing (Fig. 5), suggesting that the incorporated

dopants are not electrically active and that the damage to the NW lattice degraded the electrical properties and enhanced the leakage currents. The failure of the Zn ion-implantation approach to produce defect-free *p*-type NWs highlights the importance of the Zn surface doping scheme presented in this work for compound semiconductor nanostructures.

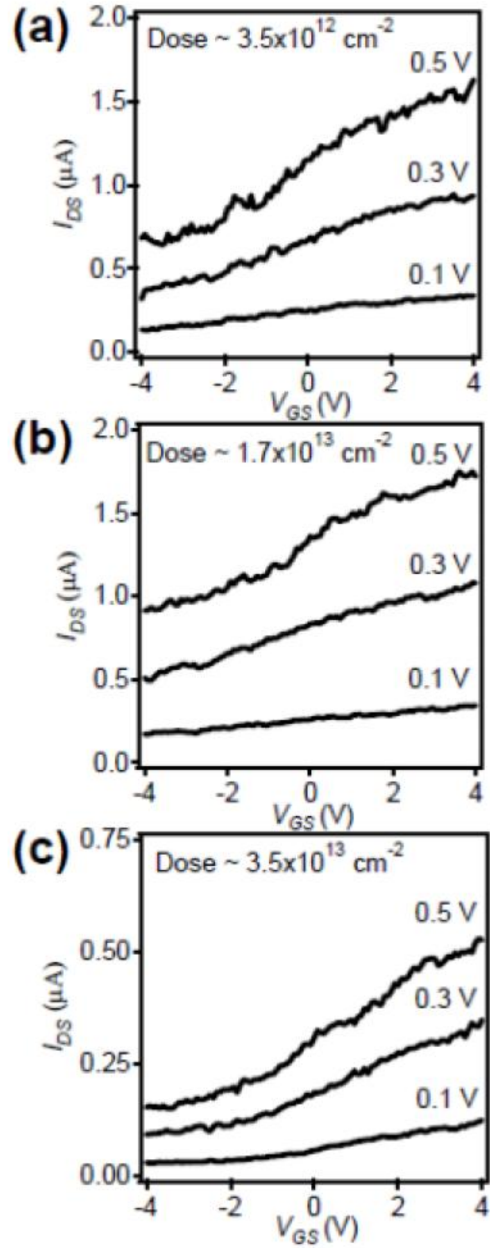

Figure 5: I_{DS}-V_{GS} characteristics of InAs NWs doped by Zn ion-implantation for dopant areal dose of (a) ~3.5×10^{12} cm^{-2}, (b) ~ 1.7×10^{13} cm^{-2}, and (c) ~3.5×10^{13} cm^{-2} and subsequent annealing at 375 C for 30 min. The channel length and NW diameter for all three devices are ~2um and ~30nm, respectively.

Chapter 3

Ultrathin InAs Tunneling Field Effect Transistors[2]

Section 3.1 Background

Recently, a method to directly integrate ultrathin layers of compound semiconductor-on-insulator has been developed by using an epitaxial layer transfer technique[1][25]. This compound semiconductor-on-insulator platform, so called "XOI" in analogy to silicon-on-insulator, offers the advantages of combining III–V semiconductors with well-established Si technology. The use of ultrathin III–V layers-on-insulator offers the benefit of reduced leakage currents due to both smaller junction areas and no junction leakage path to the semiconductor body, thereby permitting lower OFF-state currents critical to the use of low band-gap semiconductors like InAs[1][26]. Furthermore, the XOI platform potentially offers the advantage of allowing the combination of different III–V active layers with low defect density on insulator unconstrained by the original III–V growth substrates. This allows for the study of fundamental materials parameters and the exploration of various device architectures. By utilizing the XOI concept, here, we report an ultrathin body InAs tunneling field-effect transistor (TFET) on a Si substrate.

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TFETs hold promise to potentially replace or complement metal-oxide-semiconductor field-effect transistors due to their improved subthreshold swing (SS) and reduced power consumption as projected by simulation and supported in part by preliminary experimental results[27-33]. Small band-gap III–V semiconductors like InAs are ideal for use in tunneling devices, as the small direct band gap provides a low effective tunneling barrier and the low effective mass results in a high tunneling probability to achieve high ON currents[34]. Use of III–V semiconductors also allows for a spectrum of materials with tunable band alignments which could potentially enable heterojunction device exploration with extremely low effective tunneling barrier[35].

Section 3.2 Methods

A schematic of the InAs XOI TFET fabrication process is shown in Fig. 6. InAs nanoribbons (NRs) ~ 18 nm in height and ~ 350 nm in width were transferred to 60 nm low-stress silicon nitride on *p*+ Si substrates through a previously described epitaxial layer transfer process (Fig. 6a)[1]. Photolithography followed by electron-beam evaporation of 80 nm SiO_x and liftoff was used to pattern SiO_x masks to partially cover the InAs NRs (Fig. 6b). The unmasked, exposed segments of the InAs NRs were then doped *p*+ with zinc using a surface diffusion method at temperatures of 390–410 °C for ~ 30 s to 1 min[2]. The diffusion length ($x = 2(Dt)^{1/2}$, where D and t are the diffusion coefficient and time, respectively) of Zn in InAs is 130–180 nm for the doping temperatures ($D = 1.4\times10^{-12}$ cm^2/s at 400 °C) and times used, resulting in a nonabrupt lateral junction[18]. The diffusion length is longer than the InAs thickness of ~ 18 nm, resulting in the entire depth of InAs getting doped. The SiO_x masks were then etched in

50:1 HF and the *p*+ source (S) and *n*+ drain (D) Ni contacts were formed by photolithography, Ni evaporation, and liftoff (Fig. 6c). Undoped InAs is intrinsically *n*-type, making the TFET *p*+-*n* structure possible without the intentional use of an *n*-type dopant. Following S/D metal contact formation, 8 nm ZrO_2 was deposited by atomic layer deposition at 130 °C for the gate dielectric and a Ni top-gate (G) overlapping S/D was formed (Fig. 6d).

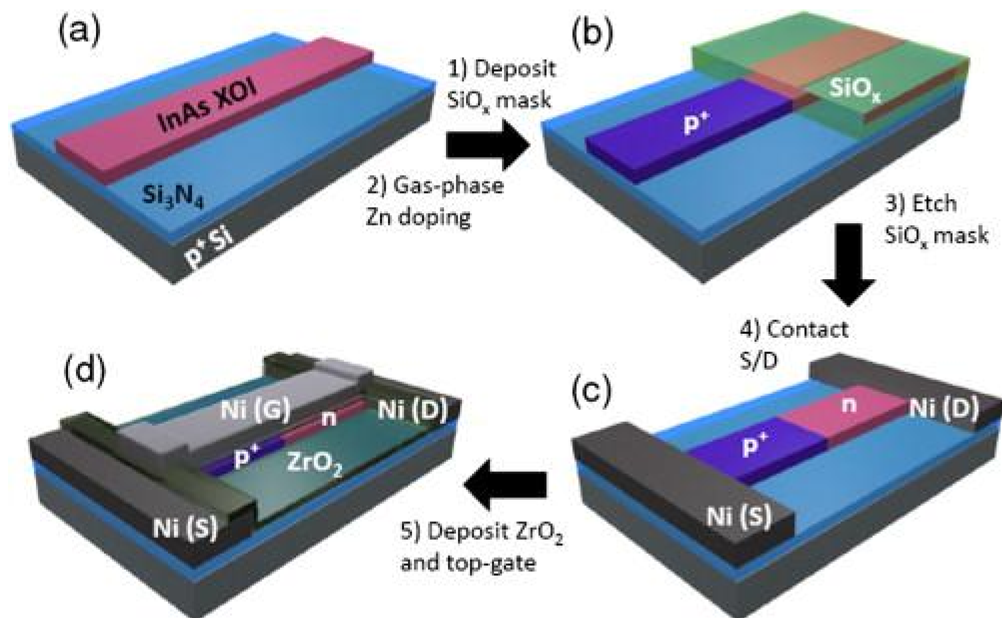

Figure 6: Schematic of the InAs XOI TFET fabrication process. (a) InAs strips (~ 18 nm thick and ~ 350 nm wide) were transferred to low-stress nitride on *p*+ Si substrates. (b) SiO_x masks were deposited followed by gas phase doping of Zn to form the *p*+ S contacts. (c) Ni S/D contacts were formed. (d) For the gate dielectric, 8 nm ZrO_2 was deposited by atomic layer deposition and a Ni top-gate (G) overlapping S/D was formed.

Section 3.3 Results

Subsection 3.3.a Electrical Analysis

Confirmation of p+ doping was obtained by fabricating back-gated InAs NR devices that were blank-doped (i.e., unpatterned). The p+ blank-doped devices (channel

length L = 5 μm) have ON current densities of ~ 15 μA/μm at V_{DS} = 1 V and V_{GS} = −4 V, with minimal back-gate dependence. The electrically active [Zn] is estimated to be ~ 1×10^{19} cm^{-3} which is in good agreement with the previously reported result for Zn-doped InAs nanowires and bulk substrates[2][18].

The room temperature I-V characteristics of a representative TFET device (channel length L ~ 2.5 μm) are shown in Fig. 7. The device has SS values of ~ 170 and 190 mV/decade for V_{DS} = 0.01 and 0.1 V, respectively (Fig. 7a). The SS exceeding 60 mV/decade is likely the result of surface trap states, and/or trap-assisted tunneling (TAT)[36][37]. Figure 7b shows the room temperature output characteristics of the same device. The ON current density is ~ 0.5 μA/μm at V_{DS} = V_{GS} = 1 V. The device is forward biased for negative V_{DS}, and under positive V_{GS}, negative differential resistance (NDR) behavior is observed, clearly confirming the interband tunneling operation of the device. The NDR peak-to-valley ratio of 1.3 at room temperature is obtained at V_{GS} = 1 V which is in good agreement with previously reported InAs tunnel diodes[38][39].

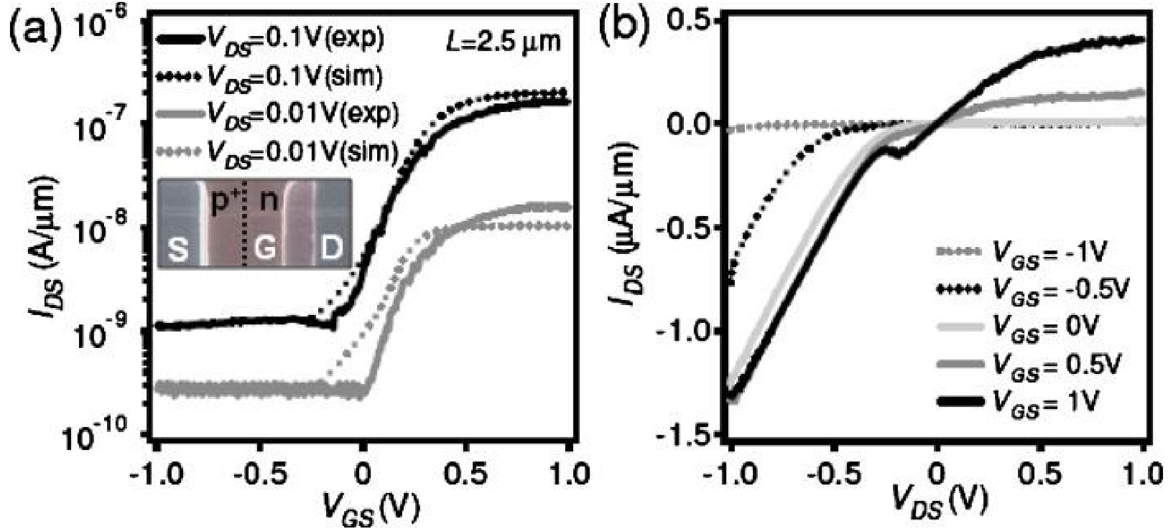

Figure 7: Room temperature (a) transfer and (b) output characteristics of a representative InAs XOI TFET (channel length $L \sim 2.5\ \mu$m).

To better characterize the XOI TFETs, temperature dependent electrical measurements were performed. Figure 8a shows the temperature dependent transfer characteristics of a device for $V_{DS} = 0.1$ V. The OFF-state current and SS decrease with decreasing temperature while the ON current is nearly independent of temperature. The OFF-state current in our device is most likely dominated by the Shockley–Read–Hall (SRH) generation-recombination current, which is strongly dependent on temperature through the intrinsic carrier concentration, and the background thermal radiation effect[37][40]. In addition, at low temperatures, interface traps freeze out, subsequently resulting in the reduction in TAT and SS. Specifically, SS is ~ 60 mV/decade at 100 K and increases with temperature to ~ 190 mV/decade at 300 K. Figure 8b shows the temperature dependent output characteristics at 100 K for the NDR operation mode. The NDR peak-to-valley current ratio increases at low temperatures and is ~ 3 at 100 K. This compares well to the peak-to-valley ratio of 2 at 150 K reported in the literature for an InGaAs TFET[37].

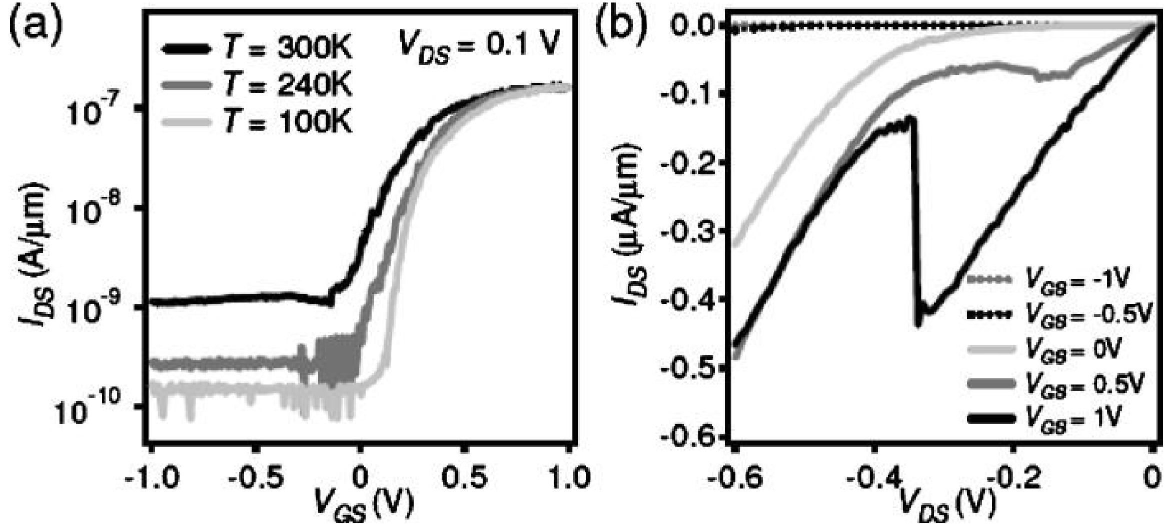

Figure 8: Temperature dependent (a) transfer characteristics of a representative TFET for V_{DS} = 0.1 V, and (b) output characteristics at 100 K for the NDR operation mode.

Subsection 3.3.b Simulation

To better understand the device operation, two-dimensional device simulations using TCAD SENTAURUS were performed. The dynamic nonlocal path band-to-band model is used. Standard SRH recombination and drift-diffusion models were used for carrier transport, and Fermi statistics were assumed. An electrically active [Zn] of 1×10^{19} cm^{-3} for the p+ source, intrinsic InAs electron concentration of 1×10^{17} cm^{-3} for the channel, equivalent oxide thickness of 2 nm, and Zn lateral diffusion length (junction abruptness) of 180 nm were used. To take into account the effects of quantization, a band gap of 0.385 eV and electron effective mass of $0.026m_o$ were used. The simulated transfer characteristics of the TFET are plotted alongside the experimental results in Fig. 7a and are in good agreement. From the Kane and Keldysh models in the uniform electric-field limit[41], the fitted A and B parameters for the simulation were 7×10^{16} $cm^{-3}\ s^{-1}$ and 1.3×10^{6} V/cm, respectively. The fitted B parameter is in good agreement

with the calculated value of 1.3×10^{6} V/cm but the fitted A parameter differs substantially from the calculated value of 9×10^{19} $cm^{-3}\,s^{-1}$ by approximately three orders of magnitude. This large discrepancy is likely the result of the density of interface traps, D_{it}, at the ZrO_2/InAs interface being unaccounted for in the simulation. The electric field in the actual device is therefore lower than in the simulation as a result of reduced gating efficiency due to D_{it}. It is also possible that there are other effects due to quantum confinement that are not fully taken into account by the simulation.

The simulated band-to-band tunneling contour plots and the corresponding vertical band diagrams for the device in the ON (V_{GS} = 0.65 V) and OFF (V_{GS} = −0.25 V) states at V_{DS} = 0.1 V are shown in Fig. 9. The band-to-band tunneling current has vertical and lateral contributions with the vertical contribution being more dominant as clearly shown on the contour plot (Fig. 9a). Figure 9b shows the vertical band diagram for the ON state. Since the p+ S overlaps the gate, it is inverted at the surface for positive V_{GS}. This surface inversion is particularly easy to achieve at a small V_{GS} swing for a small band-gap semiconductor, like InAs. The vertical depletion width of <10 nm is significantly smaller than the lateral junction abruptness of ~ 180 nm achieved by zinc doping, resulting in the vertical tunneling being the dominant current component.

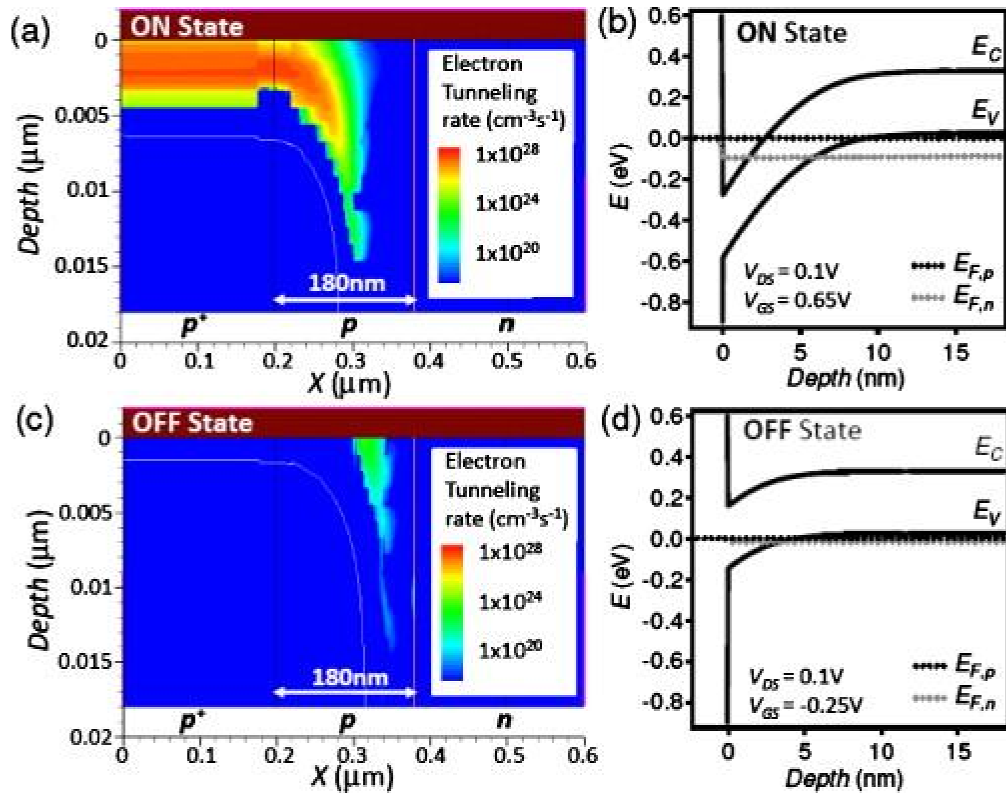

Figure 9: Simulated band-to-band tunneling contour plots and the corresponding vertical band diagrams for the device in [(a) and (b)] ON (V_{GS} = 0.65 V) and [(c) and (d)] OFF (V_{GS} = −0.25 V) states at V_{DS} = 0.1 V.

Chapter 4

Conclusions

Section 4.1 Summary

In this work, first a Zn gas phase doping process for InAs nanostructures was developed. A high active dopant concentration of ~1 x 10^{19} cm $^{-3}$ was achieved. Unlike in-situ doping or ion implantation, this technique allows for the patternable doping of InAs without inducing heavy crystal lattice damage. InAs NW p-n junction diodes and PMOSFETs were fabricated as a demonstration of this particular advantage. In the second part of this project, InAs NR TFETs were fabricated as a further testament of the versatility of this doping method. Tunneling operation is confirmed with NDR behavior observed in the forward bias region. Simulations indicate that vertical tunneling plays a non-negligible role in device operation.

Section 4.2 Future Work

In the future, there are plenty of opportunities to apply this doping technique to novel nanomaterials and device structures. One disadvantage of using Zn as a dopant in InAs is its high diffusion coefficient [18], which makes it hard to make sharp junctions. With this in mind, it is worth investigating other dopant species for gas phase doping of III-V materials. A slower diffusing dopant would have been particularly useful in the TFET project. Although the TFET fabricated in this project is primarily a

demonstration of the viability of Zn gas phase doping, its performance is not on par with state of the art III-V TFETs[36]. To further improve performance, one can consider incorporating scaling, surface engineering and heterojunctions into the TFET structure proposed in this work.

Section 4.3 Acknowledgements

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