Nanomaterials processing toward large-scale flexible/stretchable electronics

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Nanomaterials processing toward large-scale flexible/stretchable electronics

by

Toshitake Takahashi

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Committee in charge:

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Abstract

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In recent years, there has been tremendous progress in large-scale mechanically flexible electronics, where electrical components are fabricated on non-crystalline substrates such as plastics and glass. These devices are currently serving as the basis for various applications such as flat-panel displays, smart cards, and wearable electronics.

In this thesis, a promising approach using chemically synthesized nanomaterials is explored to overcome various obstacles current technology faces in this field. Here, we use chemically synthesized semiconducting nanowires (NWs) including group IV (Si, Ge), III-V (InAs) and II-IV (CdS, CdSe) NWs, and semiconductor-enriched SWNTs (99 % purity), and developed reliable, controllable, and more importantly uniform assembly methods on 4-inch wafer-scale flexible substrates in the form of either parallel NW arrays or SWNT random networks, which act as the active components in thin film transistors (TFTs).

Thusly obtained TFTs composed of nanomaterials show respectable electrical and optical properties such as 1) cut-off frequency, f_t ~ 1 GHz and maximum frequency of oscillation, f_{max} ~ 1.8 GHz from InAs parallel NW array TFTs with channel length of ~ 1.5 μm, 2) photodetectors covering visible wavelengths (500-700 nm) using compositionally graded CdS_xSe_{1-x} ($0 < x < 1$) parallel NW arrays, and 3) carrier mobility of ~ 20 cm^2/Vs, which is an order of magnitude larger than conventional TFT materials such as a-Si and organic semiconductors, without sacrificing current on/off ratio (I_{on}/I_{off} ~ 10^4) from SWNT network TFTs.

The capability to uniformly assemble nanomaterials over large-scale flexible substrates enables us to use them for more sophisticated applications. Artificial electronic skin (e-skin) is demonstrated by laminating pressure sensitive rubber on top of nanomaterial-based active matrix backplanes. Furthermore, an x-ray imaging device is also achieved by combining organic photodiodes with this backplane technology.

To my family and everyone else whom I’ve had the privilege of running into from birth to present day.

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Chapter 1
Introduction

1.1 Introduction to flexible electronics

Historically, the continuous miniaturization of the conventional metal-oxide-semiconductor field effect transistor (MOSFET) has been the main driving force for the current high performance microelectronics. The number of transistors in an integrated circuit doubles every two years according to Moore's law, resulting in improvements in energy efficiency and operating speed as well as dramatic reduction in the cost per transistor. On the other hand, there is another trend in the electronics industry, which deals with large amount of electronic devices spread over a large surface area on the order of meters on mechanically bendable and stretchable substrates. Figure 1-1 shows some of the envisioned applications enabled by so-called large-area flexible electronics. Owing to its mechanical flexibility as well as the large size, this sheet-type device on which various electrical/ sensor components are distributed can be used as artificial skin for robots, dynamic monitoring of mechanical fatigue in transportation systems, and even biological interfaces with the human brain as one example. The problem to realize the applications mentioned above, however, is that the cost per unit area of current silicon (Si) transistor is still too expensive, although the cost per transistor is drastically reduced by scaling. In addition, bulk Si is not mechanically robust enough to deal with mechanical bending or stretching. Therefore, alternative materials system which not only possess desirable electrical and mechanical characteristics, but also can be processed in cost effective way, need to be explored. More specifically noted, for the use as the active channel material in thin-film transistors (TFTs), we are interested in the materials which satisfy following three properties. First of all, the materials have to be compatible with a large-scale, low temperature, and cheap fabrication process. Secondly, the materials need to be robust enough against mechanical strain such as bending and stretching. Lastly, the electrical performance of the explored materials has to be superior in order to expand the limit of the applications.

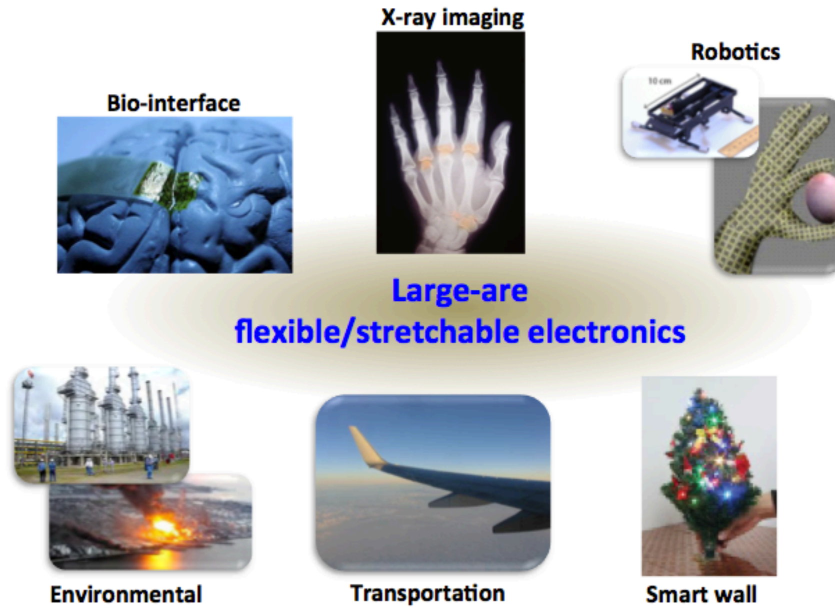

Figure 1-1. Envisioned applications enabled by large-scale mechanically flexible/stretchable electronics.

1.2 Materials system used as TFT active components

Firstly, the materials system commonly used in flexible electronics is briefly reviewed. These materials are amorphous silicon/poly-crystalline silicon, organic semiconductors, amorphous oxide semiconductors, and layer transferred semiconductor. Next, the opportunities of two kinds of nanomaterials; semiconductor nanowire and single-walled carbon nanotubes, which are the focus of this thesis, are discussed.

a) Amorphous silicon (a-Si)/ poly-crystalline silicon (poly-Si)

A-Si/ poly-Si TFTs on rigid silicon and glass substrates have been widely used as a switching element to control the gray level in a liquid crystal display (LCD)[1, 2] and to drive an organic light-emitting diode (OLED)[3, 4]. A-Si has been also intensively explored in x-ray imaging applications[5], where a-Si is used for both TFT components and photodetectors. While deposition of a-Si:H is achievable at relatively low temperature (~150 ^{o}C) in order to make the process compatible with plastic substrate, the quality of the material is inferior to that achieved with a high temperature process (typically

mobility of ~ 1 cm^2/Vs is obtained). Furthermore, the inorganic a-Si is brittle, so it is limited for the use in flexible electronics.

On the other hand, poly-Si has been used as the channel material for the applications where high mobility TFTs are required. Previously, Wagner *et al.* reported poly-Si TFTs on metal foil substrate with the mobility of 64 cm^2/Vs for electrons and 22 cm^2/Vs for holes[6]. Serikawa et al. fabricated the poly-Si TFTs on flexible steel foil using KrF excimer laser annealing of a-Si, and the mobility is 103 cm^2/Vs and 122 cm^2/Vs for n- and p-channel, respectively[7]. The disadvantage of poly-Si, however, is high temperature thermal process is required to crystallize a-Si using either from post-annealing (~900 ^oC) or local laser irradiation, which prohibit this approach from being used on a plastic substrate. Additionally, large poly-Si grain size causes poor device-to-device uniformity, which is obviously problematic when we consider this for large-scale use.

b) Organic semiconductors

Organic semiconductors have been considered as a promising candidate to replace a-Si in the applications where large-area coverage, mechanical flexibility, and low cost fabrication are required[8]. Once formulated into inks, organic semiconductors are readily applicable to solution-based printing processing. Small molecules frequently used in TFTs such as pentacene and its derivatives (the deposition is not by solution based process but by evaporation method) show mobilities of up to 1.5 cm^2/Vs under optimized condition[9], but the mobility of polymer organic molecule semiconductors such as regioregular (RR) poly(3-hexylthiophene) (P3HT)[10] and a-w-dihexyl-quinquethiophene[11], typically used with solution based printing process is around 0.1 cm^2/Vs.

So far, many groups have reported numerous applications using organic TFTs such as backplanes in active matrix displays[12, 13] and radio frequency identification (RFID) tags[14]. In display applications, for example, organic TFTs act as individual pixel switches in the active matrix backplane circuit. The mobility in the range of ~ 0.01 cm^2/Vs is good enough for small-sized devices with low resolution and low refresh rate, while organic TFTs are not a desirable candidate for medium- to large-sized liquid crystal displays (LCDs) used for monitor and television displays, where much higher ON current (i.e. higher mobility) is necessary for better resolution and faster refresh rate. Furthermore, the uncertain long-term reliability issue and difficulty of controlled doping techniques for these materials remained to be addressed.

c) Amorphous oxide semiconductors

Oxide semiconductors, especially amorphous ones, have attracted tremendous interest for the use as TFT active components because of exceptional optical transparency, air-stability and superior carrier mobility[15]. Various materials by solution

based process have been reported, including In_2O_3[16], $InGaO_3(ZnO)_5$[17], InGaZnO[18], InZnO[19], ZnO[20], ZnMgO[21]. Decent electrical properties (mobility up to ~120 cm^2/Vs as well as large I_{on}/I_{off} ratio of10^5) have been reported[22]. But these properties are only achieved after high temperature (up to 400-500 ^oC) post-deposition annealing is done, which is not compatible with plastic substrate with low glass transition temperature (Glass transition temperature: T_g ~ 70 ^oC for polyethylene terephthalate:PET and T_g ~ 400 ^oC for polyimide). The typical carrier mobility of solution-processed oxide semiconductor with modest annealing temperature (~ 150 ^oC) is in the range of 1-10 cm^2/Vs[23], which is still lower than that of poly-silicon TFT (~ 100 cm^2/Vs).

d) Layer transferred semiconductor

To achieve high quality materials, high temperature annealing process is desirable. But the use of plastic substrate imposes the upper limit of process temperature. To solve this dilemma, Roger *et al*. reported a new approach, where they fabricated nanometer- or micrometer-scale structures such as ribbons and membranes from high-quality, bulk wafers, and then transferred these with simple PDMS stamp onto plastic substrates at room temperature[24, 25, 26]. Significant advancement has been achieved using this technique, but there still remain challenges to be addressed such as fabrication cost and large-scale fabrication.

e) Semiconductor nanowires (NWs)

NWs have been intensively studied due to their size-related intriguing properties, and have been expected to be a promising potential as building blocks for nanoscale electronics[27], optoelectronics[28, 29], chemical/biological sensing[30, 31, 32], and energy conversion/harvesting[33, 34]. With a vapour-liquid-solid (VLSI) process, various types of semiconductor NWs such as group IV, II-VI, III-V and even heterostructures can be grown (left in Fig. 1-2). To fully extend this potential for practical large-scale electronics, the use of aligned NW parallel arrays as the TFT channel materials has been explored. Numerous approaches have been reported so far (see more details in Chapter 2). The approach used in this thesis is based on contact printing methodology developed in our group[35, 36, 37]. The biggest advantage of this approach is that chemically synthesized inorganic NWs are transferred on receiver substrate at room temperature, thereby preserving high quality single crystal NWs on arbitrary any substrate such as paper and plastic. In this thesis, the potential of the aligned NW parallel arrays for large scale flexible electronics using contact printing will be discussed.

f) Single-walled carbon nanotubes (SWNTs)

SWNTs have been considered as a promising material for a wide range of applications in solid-state devices owing to their superb electrical properties such as scattering-free ballistic transport of carriers at low electric fields, higher carrier mobility (>10,000 cm^2/Vs), and great gate control. Despite recent technological advancement in individual nanotube transistors, there still remains many challenges to be addressed, including reliable accurate assembly on a handling substrate, device-to-device fluctuation, just to name a few. On the other hand, the use of carbon nanotubes networks as the channel material in TFTs presents a new promising path for large-scale rigid/flexible electronics. Although electrical property of random network SWNT film is not comparable to that of single carbon nanotube due to considerable amount of contact resistance between each nanotube junctions, the SWNT network film not only holds many desirable characteristics such as superior carrier mobility (two orders of magnitude higher than a-Si or organic semiconductors), mechanical flexibility and optical transparency, but it can also be readily processed over large scale substrates with solution-based printing at room temperature. Various techniques have been reported for this purpose (summarized in Chapter 2). Though some advancement has been reported using SWNTs network film for macro-scale electronics[38, 39], additional treatments such as electrical breakdown and channel width control are inevitably required to obtain better I_{on}/I_{off} ratio due to the coexistence of metallic and semiconducting nanotubes. Therefore, highly purified semiconducting SWNTs have been desired for device applications since those significantly simplified device fabrications. To address this issue, Hersam *et al.*, successfully demonstrated the use of density gradient ultracentrifugation (DGU) to achieve electronic type separation[40]. By now, 99.9 % semiconductor-enriched SWNTs are commercially available (right in Fig. 1-2). In this thesis, we focused on this purified SWNTs and investigate the potential of purified SWNTs network film for the use in large-scale flexible electronics applications.

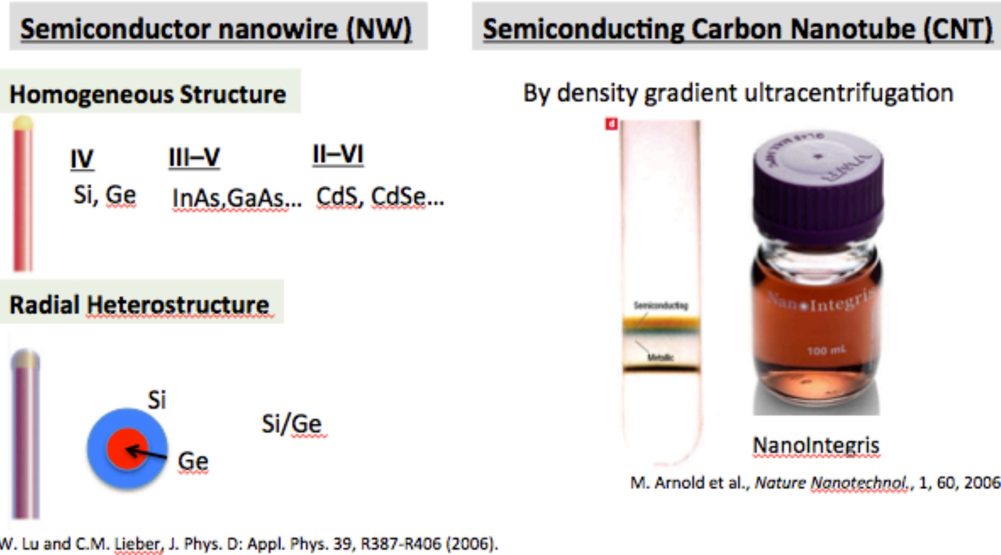

Figure 1-2. (left) various types of nanowires grown by Vapour-liquid-solid (VLS) method, (right) Commercially available semiconductor enriched single-walled carbon nanotube solutions (from NanoIntegris).

1.3 Manufacturing processing

a) Printing technique

Conventionally, electronics system has been fabricated with lithographic technique, where a series of subtractive steps are involved and each step is associated with expensive fabrication tool. In addition, the throughput is also limited by the use of each tool. In contrast to these drawbacks associated with conventional lithographic techniques, printing techniques hold several advantages. With the additive processing, the processing steps are drastically reduced, resulting in alleviated process complexity and less amount of tools required. Although total processing cost still depends on the process throughput and materials cost, this process reduction greatly simplifies the fabrication process. Several printing techniques have been studied for electronics applications, including screen printing, gravure/flexographic/offset printing, inkjet printing. Despite recent advancement in printing techniques, the linewidth and functional transistor density achieved with printing techniques, however, are still not yet comparable to those achieved by the state-of-the-art lithographic tools. Therefore, the use for printed electronics should be restricted to the applications that are area-constrained, but not function-constrained[41]. It should be also noted that reliable printing of high-k dielectric layers remains to be solved.

b) Conventional lithographic technique

The use of conventional lithography for flexible electronics is favorable since the issues associated with printing technology such as linewidth and line-edge roughness can be avoided. The process approach we developed[42], in which the handling wafer on which polymer is spin-casted, is used for device fabrication and then polymer layer is peeled off after the fabrication is completed, can be combined with the conventional lithographic technique, enabling us to fabricate complicated and sophisticated device structure on flexible substrate.

The work detailed in this thesis to achieve flexible electronics relies on the conventional lithographic approach, rather than printing technique.

1.4 Overview of this thesis

This dissertation focuses on the scalable assembly process of nanomaterials and its application to large-scale flexible and stretchable electronics. Chapter 2 describes the low temperature assembly process for semiconducting NWs and SWNTs. Thin film transistors (TFTs) composed of thus assembled nanomaterials are characterized, as detailed in Chapter 3. In this chapter, radio frequency characteristics are investigated to study the performance limit of InAs NWs parallel array TFTs. Furthermore, compositionally graded CdS_xSe_{1-x} NWs are assembled in similar fashion for tunable photodetector, and its optical responses are characterized. Chapter 4 describes the integrated device characteristics of SWNT TFTs, especially for artificial electronic skin and x-ray imager applications. Chapter 5 summarizes the contributions of this thesis and offers suggestions for future work.

1.5 References

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Chapter 2
Scalable and low-temperature assembly process for nanomaterials

2.1 Large-scale assembly of NWs

2.1.1 Introduction

To utilize NWs for practical large-scale flexible electronics, a controllable yet reliable assembly method needs to be established. For this purpose, various assembly approaches have been reported (Fig. 2-1 from ref. 1) including flow-assisted alignment[2, 3, 4, 5], Langmuir-Blodgett (LB)[6, 7, 8], bubble-blown techniques[9], and electric-field-directed assembly[10, 11, 12, 13]. Each approach has a unique advantage and demonstrated the feasibility of parallel-arrayed assembly, but suffers from certain limitations, mainly the scalability, uniformity, and/or the complexity of the process for use in macro-scale applications. To address this point for large-scale and controllable assembly of highly aligned NW parallel arrays, our lab has developed contact printing technology[14, 15, 16], where as-grown NWs are mechanically transferred on the receiver substrate with appropriate surface modification. During this printing process, shear force is utilized to effectively align the NWs. With this simple but versatile approach, parallel arrays of NWs are readily formed on literally any substrate including paper, glass and plastic substrate. This NWs contact printing technology could be an important advancement to realize fully printed flexible electronic devices (Fig. 2-2), which exhibit both low cost and high performance. The approach described in Fig. 2-2 is divided into three components; *1)* patterning of the receiver substrate to define 'sticky' and 'non-sticky' regions for selective NWs transfer, *2)* contact printing of NWs array as the active channel region, and *3)* metal contact and insulator deposition to complete the device. Since the step *3* is an intensively explored research field in organic electronics community, this topic won't be discussed here. Rather our effort is focused on steps *1* and *2* as described in following chapter.

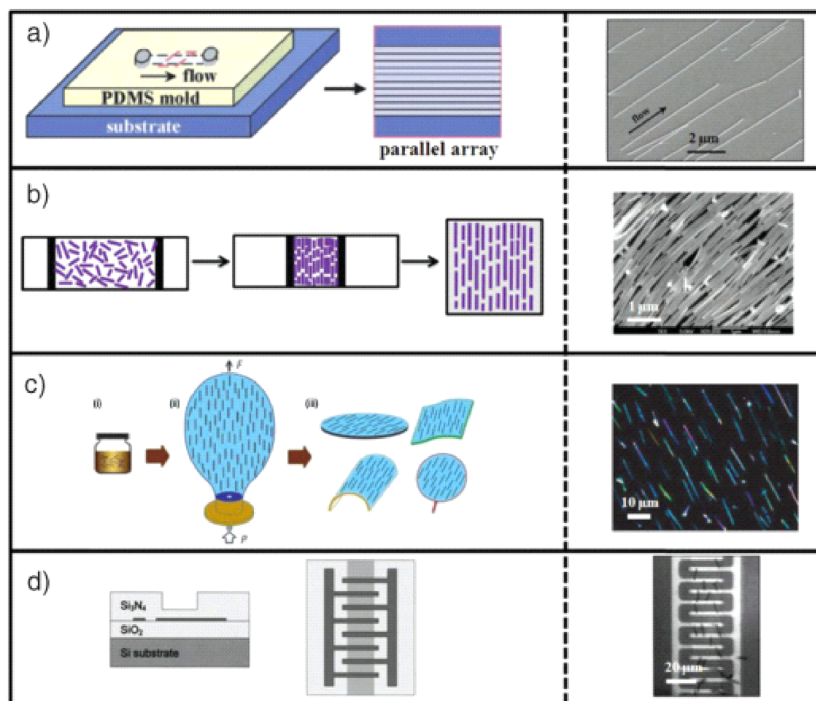

Figure 2-1. Nanowire-assembly techniques (image from reference 1.) (*a*) Schematic and the result of flow-assisted NW-assembly method[2-5], (*b*) Schematic of LB NW assembly method[6-8], (*c*) Schematic of blown-bubble NW assembly method[9], (*d*) Schematic (left) and optical image (right) of electric field alignment of NWs[10-13].

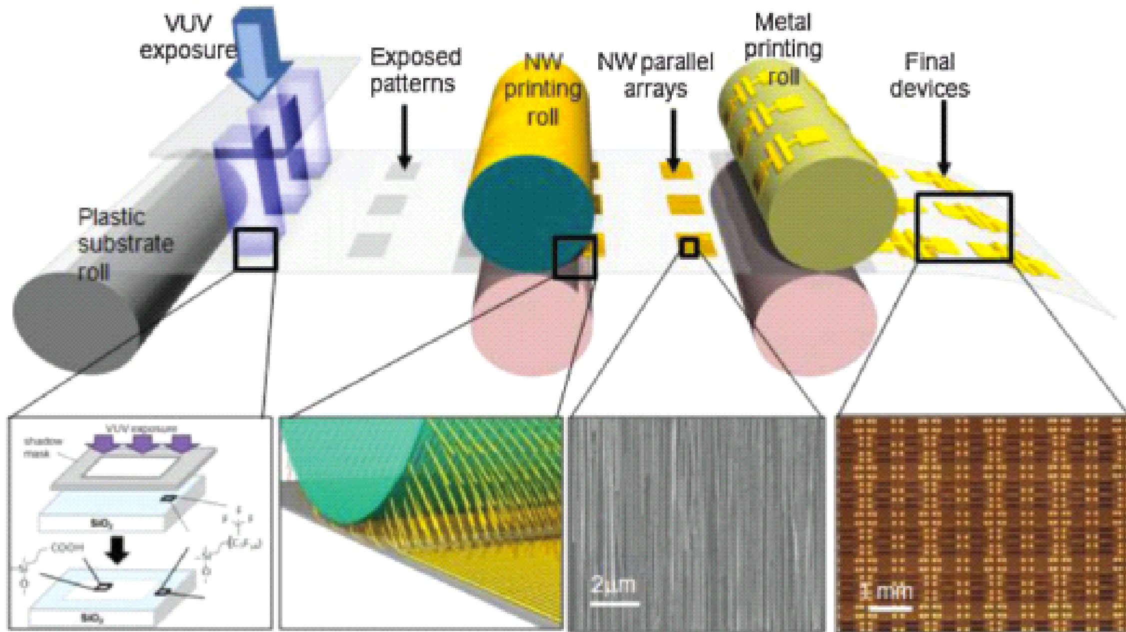

Figure 2-2. Schematic of an envisioned roll-to-roll printing set-up for NW electronics and sensors fabrication (image from reference 1). The process involves fluorinated monolayer patterning of the receiver substrate to define "sticky" and "non-sticky" regions for the subsequent patterned transfer and assembly of NWs by contact printing. Following the printing of NW active components, devices are fabricated by defining the source/drain and gate electrodes.

2.1.2 NWs contact printing methodology

The overview of contact printing process is shown in Fig. 2-3 (image from ref. 1). Here the NWs used in this process are grown by CVD (chemical vapor deposition). The NWs are typically grown on the growth substrate with random orientation, as shown in the SEM image in the inset of Fig. 2-3. Contact printing enables these as-grown NWs to be transferred on the pre-patterned receiver substrate. During this process, NWs are effectively combed by the directional shear force, and are eventually detached from the growth substrate as they are anchored by the chemically modified surface on the receiver substrate. After lift-off process, highly aligned arrays are readily obtained. This simple process can be readily applicable to the large-scale (4" wafer) assembly[1]. The density of printed NWs is controlled by using different surface modification of the receiver substrate. Figure 2-4 shows the density of printed Ge NWs on various chemically modified surfaces[1]. For the receiver substrates functionalized with –CF3 terminal groups, which are well known to be highly hydrophobic and 'non-sticky', almost no NWs are transferred. On the other hand, highly dense NW assembly are observed on –NH2 and –

N(Me)3+ terminated monolayers due to the strong surface bonding interactions. To extend this, in the next subsection, a self-assembled monolayer (SAM) is used to define 'sticky' and 'non-sticky' surface regions, followed by NW contact printing. This approach enables us to realize lithography-free fully printable electronics (Fig. 2-2).

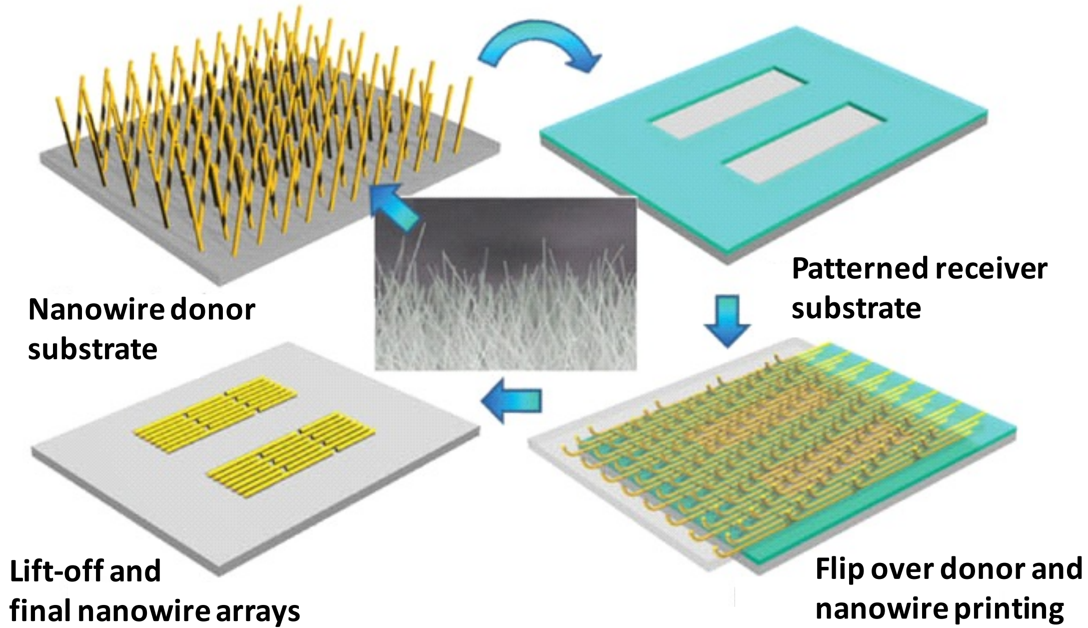

Figure 2-3. Schematic of NW contact printing process. The SEM image in the inset shows the grown Ge NWs are randomly oriented on the growth substrate. The NWs are then aligned and transferred to the receiver substrate by application of a directional shear force, resulting in the printing of sub-monolayer NW parallel arrays on the receiver substrate (Ref. 1).

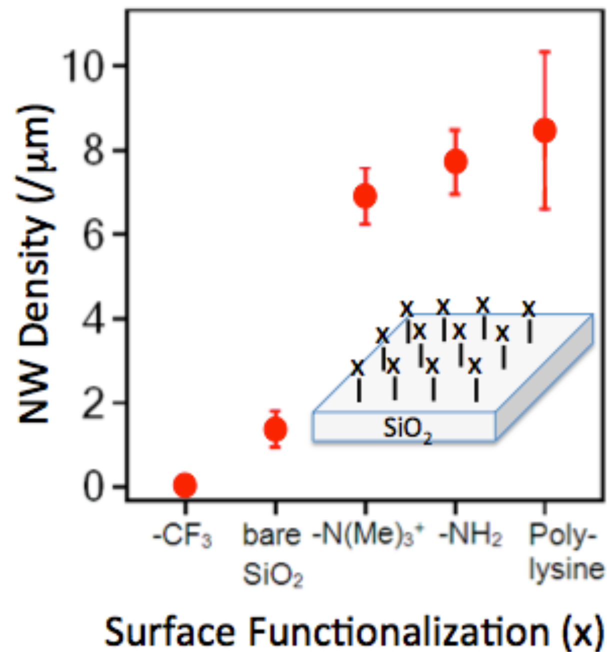

Figure 2-4. The density control of printed Ge NW by contact printing through the surface modification of Si substrate. Bare SiO_2 corresponds to the untreated SiO_2 surface, while –CF3 [(heptadecafluoro-1,1,2,2-tetrahydrodecyl) dimethylchlorosilane), -N(Me)3 (Ntrimethoxysilylpropyl-N,N,N-trimethylammonium chloride], and -NH2 (3 triethoxysilylpropylamine) correspond to the surface-modified functional groups. Note that, as expected, poly(L-lysine) functionalization results in a larger standard deviation due to the less uniform coverage of the surface by the polymeric thin film, as compared to the molecular monolayers (Ref. 1).

2.1.3 Monolayer resist for patterned contact printing◊

In recent years, single crystalline, semiconductor nanowires (NWs) have been widely explored as the potential building blocks for various technological applications, such as electronics[17], photonics[18, 19], sensors[20, 21], and energy conversions[22, 23]. To fully extend the potential, however, the development of generic assembly methods is required[24, 25]. Recently, we demonstrated a simple contact printing approach for the large-scale assembly of parallel arrays of NWs on rigid substrates as well as mechanically flexible substrates[26, 27, 28]. During this process, the direct and aligned transfer of NWs from the growth (i.e., donor) substrate to the receiver substrate is attained. This highly versatile approach is attractive for large-area printable electronics with the printed NW parallel arrays being configured as the channel or active material for transistors and sensors. Previously, the NW patterning was achieved by photolithographically patterning a polymeric resist layer on the receiver substrate prior to the printing process[6]. Following the printing process, the resist layer covered with the printed NWs is dissolved in a solvent, leaving behind only the NWs assembled at predefined locations. To further demonstrate the versatility of the contact printing process, here, we report patterned printing of NWs by using fluorinated self-assembled monolayers (SAMs) as the resist layer. By projecting a light pattern on the surface of the SAM-resist in an oxygen rich environment, sticky and non-sticky regions on the surface are directly defined in a single-step process which then enables the highly specific and patterned transfer of the NWs by the printing process, without the need for a subsequent lift-off step. This work demonstrates a novel route toward scalable, patterned printing of NWs on substrates by utilizing very ultraviolet (VUV) tunable, nanoscale chemical interactions.

The process flow for the patterned NW printing with SAM-resist is illustrated in Figure 2-5. Firstly, a Si/SiO_2 (50 nm, thermally grown) substrate is chemically reacted with (heptadecafluoro-1,1,2,2-tetrahydrodecyl) dimethylchlorosilane (HDF) to form a highly stable, fluorinated SAM on the surface of the substrate. A light pattern is then projected on the SAM-resist by using an excimer light source (172 nm, ~25 mW/cm^2) and a shadow mask (Fig. 2-5*a*). The VUV light exposure in the presence of O_2 results in the chemical cleavage of the F-C bonds and the formation of -COOH and -CHO functional end groups (Fig. 2-5*b*)[29, 30]. While the original fluorinated SAM is highly non-sticky to the NWs, the VUV-modified monolayer exhibits strong binding interactions with the NWs, most likely through hydrogen bonding. Following the patterned exposure of the SAM-resist, the NW printing is conducted by directionally sliding a growth substrate consisting of a dense forest of Ge or Si NWs (grown non-epitaxially by vapor-liquid-solid process) on top of the receiver substrate. A lubricant (octane: mineral oil, 2:1 v:v) is applied between the two substrates in order to minimize the mechanical interactions, therefore, enhancing the dominant role of the well-controlled chemical interactions in guiding the NW transfer process. During the printing process, NWs are dragged on the receiver substrate, resulting in their alignment in the direction of the shear force (Supp.

◊ The work presented here has been published in a similar form to the following reference; T. Takahashi, K. Takei, J. C. Ho, Y. –L. Chueh, Z. Fan, A. Javey, *Journal of the American Chemical Society*, 131 (6), 2102-2103, 2009.

Info.). Once anchored to the surface of the receiver substrate by chemical binding interactions, NWs are detached from the growth substrate. As a result, highly aligned NW arrays are assembled on the exposed SAM regions of the receiver substrate while no NWs are assembled on the unexposed, fluorinated SAM regions (Fig. 2-5*c*).

To characterize the properties of the VUV exposed SAMs, contact angle, XPS, and ellipsometry measurements were performed as a function of the exposure time. As shown in Fig. 2-6*a*, the contact angle of the HDF treated surface is ~100°, showing a highly hydrophobic surface property. As the monolayer is exposed to VUV, however, the contact angle decreases and the surface changes to possess a hydrophilic property. Specifically, the contact angle is reduced to ~10° after 60 min exposure in 3 Pa O_2/N_2 (21, 79 %) ambient. On the other hand, when irradiation is carried out at 10^5 Pa, it takes <20 min to achieve a similar contact angle. This accelerated chemical transformation of the monolayer by increasing the pressure depicts the important role of O_2 in the VUV enabled surface chemical modification[29, 30].

From XPS measurements (Fig. 2-6*b*), the VUV-induced, chemical modification of the monolayer is directly confirmed. While the F 1s peak at 688 eV, originating from C-F bonds, is clearly observed for the unexposed SAM, it is completely diminished after the VUV irradiation. This is also seen from the C 1s spectrum, where the C-F peak at 292 eV disappears upon VUV irradiation. On the hand, the C 1s peak at ~285 eV which corresponds to the C-C bond remains intact, even after the VUV exposure. The results suggest that the alkyl backbone of the monolayer remains intact with only the C-F bonds being oxidized upon VUV irradiation and replaced with polar –COOH and -CHO species. This is also confirmed from ellipsometry measurements where a SAM thickness of ~1.1 and 0.9 nm are observed for the unexposed and exposed SAMs, respectively. The observed results are consistent with the previously reported VUV modification of fluorinated SAMs on SiO_2 surfaces in the presence of molecular oxygen[29, 30]. In those studies, it was proposed that molecular oxygen forms highly active species upon VUV irradiation which then readily oxidize and cleave the C-F bonds. A similar surface chemical reaction is expected in our fluorinated SAMs.

Optical and scanning electron microscopy images of printed Ge NWs (d ~30 nm) on VUV-patterned fluorinated SiO_2/Si substrate are shown in Fig. 2-7. Fluorinated regions possess highly non-sticky surface properties; therefore, preventing NW transfer during the contact printing process. On the other hand, NW parallel arrays are readily assembled on the hydrophilic regions, enabled by the VUV exposure. The transferred NWs are found to be relatively dense (2-5 NW/μm) and well aligned (Fig. 2-7*d*). The density may be further enhanced in the future by using complementary surface modification of VUV-irradiated regions, which was not incorporated in this work. As clearly evident, this simple process enables a high degree of selectivity in the assembly of the NWs in well defined locations on surfaces, especially for applications that do not require nm-scale positioning, such as for large-area electronics with the device dimensions on the order of 10's of microns. In our current set-up, a resolution limit of ~5 μm is obtained which is limited by the non-ideal contact between the shadow mask and the substrate.

To further investigate the feasibility of this printing approach for electronic applications, we fabricated back-gated (gate oxide thickness ~ 50 nm SiO_2), field-effect-transistors (FETs) with channel width ~200 μm and source/drain (S/D) spacing ~3 μm by using *p*-type Si NWs (d~30 nm, B doped). Notably, the assembled NWs do not detach from the substrate during the standard microfabrication processing steps used here (Supp. Info.). Fig. 2-8 shows a representative transfer characteristic of such a proof-of-concept device structure. The transistor delivers a modest ON current of ~0.6 mA at V_{DS}=3V with I_{ON}/I_{OFF} >100. This ON current corresponds to ~1 μA/NW assuming a NW density of 3 NW/μm, which is consistent with the observed I_{ON} for a typical single Si NW FET configured in similar device geometry.

In summary, well-defined and highly specific NW assembly is achieved by combining the contact printing with direct SAM patterning on SiO_2 surfaces. Here, the SAM is effectively used as the resist for NW transfer process, enabling a highly versatile, one-step process for achieving patterned assembly of parallel arrays of NWs on substrates.

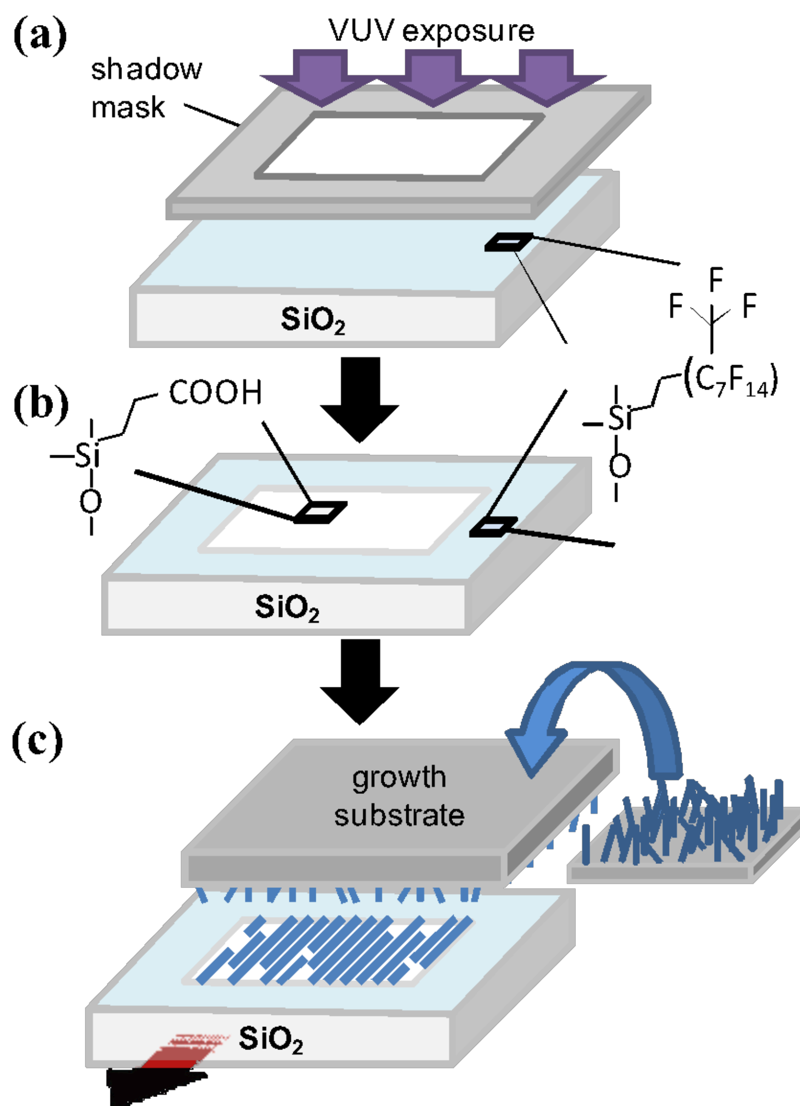

Figure 2-5. Schematic of the patterned contact printing process with monolayer resist. ***(a)*** Patterning of fluorinated SiO_2 surface is carried out by VUV irradiation in the presence of O_2. ***(b)*** C-F bonds in the exposed regions are cleaved and replaced with –COOH or -CHO functional groups. ***(c)*** Contact printing results in the aligned transfer of NWs on the VUV exposed regions.

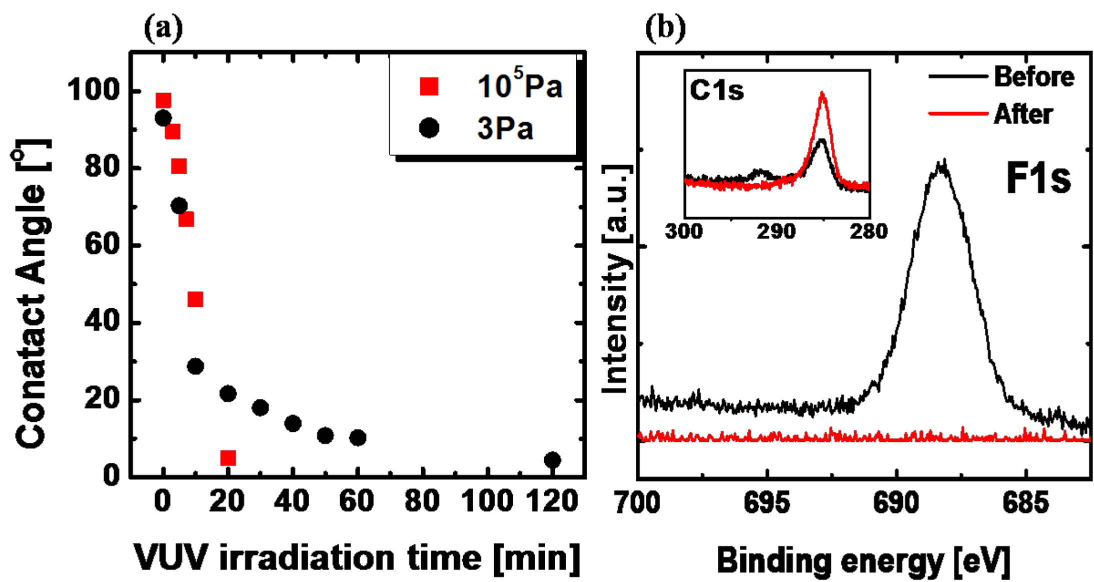

Figure 2-6. (***a***) Water contact angle as a function of VUV irradiation time. Irradiation is carried out at 10^5 Pa and 3 Pa, corresponding to 2×10^4 Pa and 0.6 Pa of oxygen partial pressure, respectively. **(*b*)** F1s and C1s (inset) XPS spectra of fluorinated surfaces before (black curve) and after (red curve) VUV irradiation for 30min at 10^5 Pa.

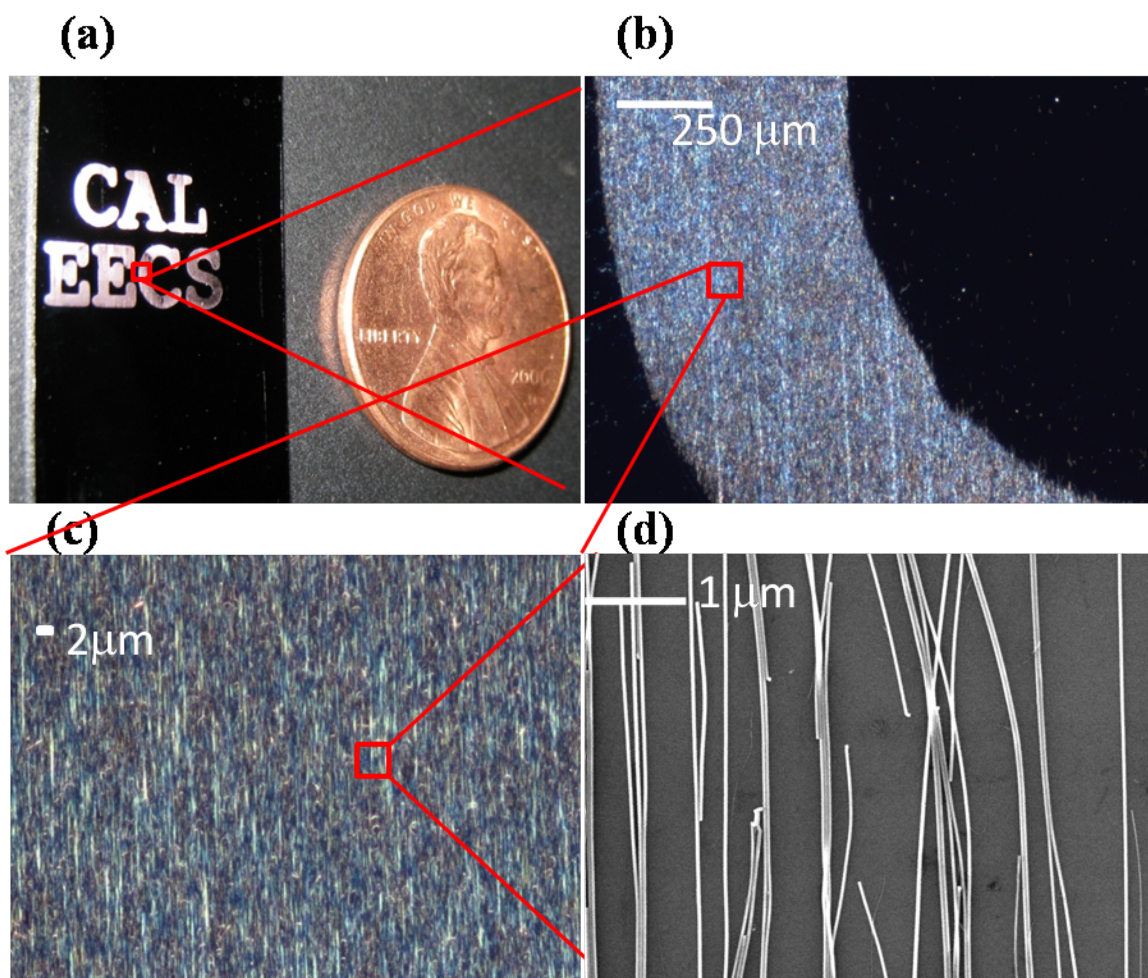

Figure 2-7. (***a***), (***b***), (***c***) Optical dark field and (**d**) SEM images of Ge NWs (d ~30 nm) printed on the VUV patterned SAM-resist.

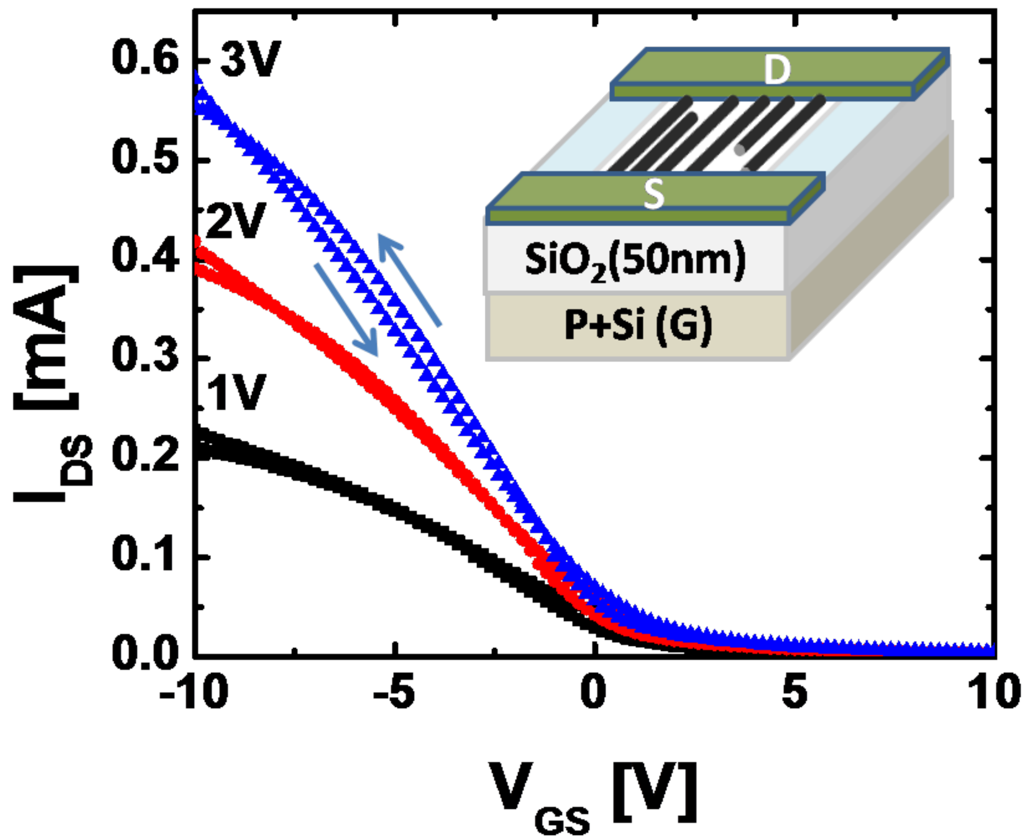

Figure 2-8. Transfer characteristics of a parallel-array Si NW FET with W~200 μm and L~3 μm, for various values of V_{DS}.

2.2 Large-scale assembly of single-walled carbon nanotubes

2.2.1 Introduction

Various assembly methods for random single-walled carbon nanotubes (SWNTs) network have been reported, including direct CVD growth[31, 32], dry filtration[33], evaporation assembly[34], spin coating[35, 36, 37], drop coating[38, 39, 40, 41], and printing[42, 43, 44, 45, 46] (Figure 2-9 from reference 47). Each of the methods has unique opportunities and challenges (see detailed info in ref. 47). In this study, we decided to focus on solution-based deposition of pre-separated single-walled carbon nanotubes (SWNTs) on macro scale substrate. In this experiment, as-received 99 % semiconductor enriched SWNT solution (IsoNanotubes-S from NanoIntegris, Inc.) is used without any densification.

2.2.2 Solution-based process using high purity semiconducting SWNTs

Figure 2-10 shows the solution-based process of high purity semiconducting SWNTs deposition. First, the surface of SiO_2 is functionalized with either poly-L-lysine (PLL) for 5 min or aminopropyltriethoxysilane (APTES) for 30 min after mild O_2 plasma treatment (30W, 1min). Then, semiconductor-enriched SWNTs solution (99 %) is casted with pipet on the surface for certain amount of time, followed by a rinse with DI water. AFM images of deposited SWNTs network from PLL- and APTES-functionalized surfaces are shown in Fig 2-11*a*, *b*. Each molecular structure used for surface functionalization is also shown on Fig. 2-11*c*, *d*. APTES is reported as commonly used polymer for SWNTs deposition[31, 35], but it didn't work for us for unknown reasons. On the other hand, PLL reliably works better as SWNT deposition, so we use this polymer for the rest of our work. It should be also noted that the density of SWNTs as a function of time is highly dependent on the particular surface being explored. Figure 2-12 shows AFM images of deposited SWNTs with different deposition time on two different surfaces; one is thermally grown SiO_2 and the other is evaporated SiO_2. Higher densities of SWNTs with higher bundling probability are observed for similar deposition times on thermally grown SiO_2 layers. Furthermore, we observed that the density depends on the nanotube solution, in part because different semiconductor-enriched products utilize different surfactants. The electrical properties of thusly deposited SWNTs will be discussed in Chapter 4.2.

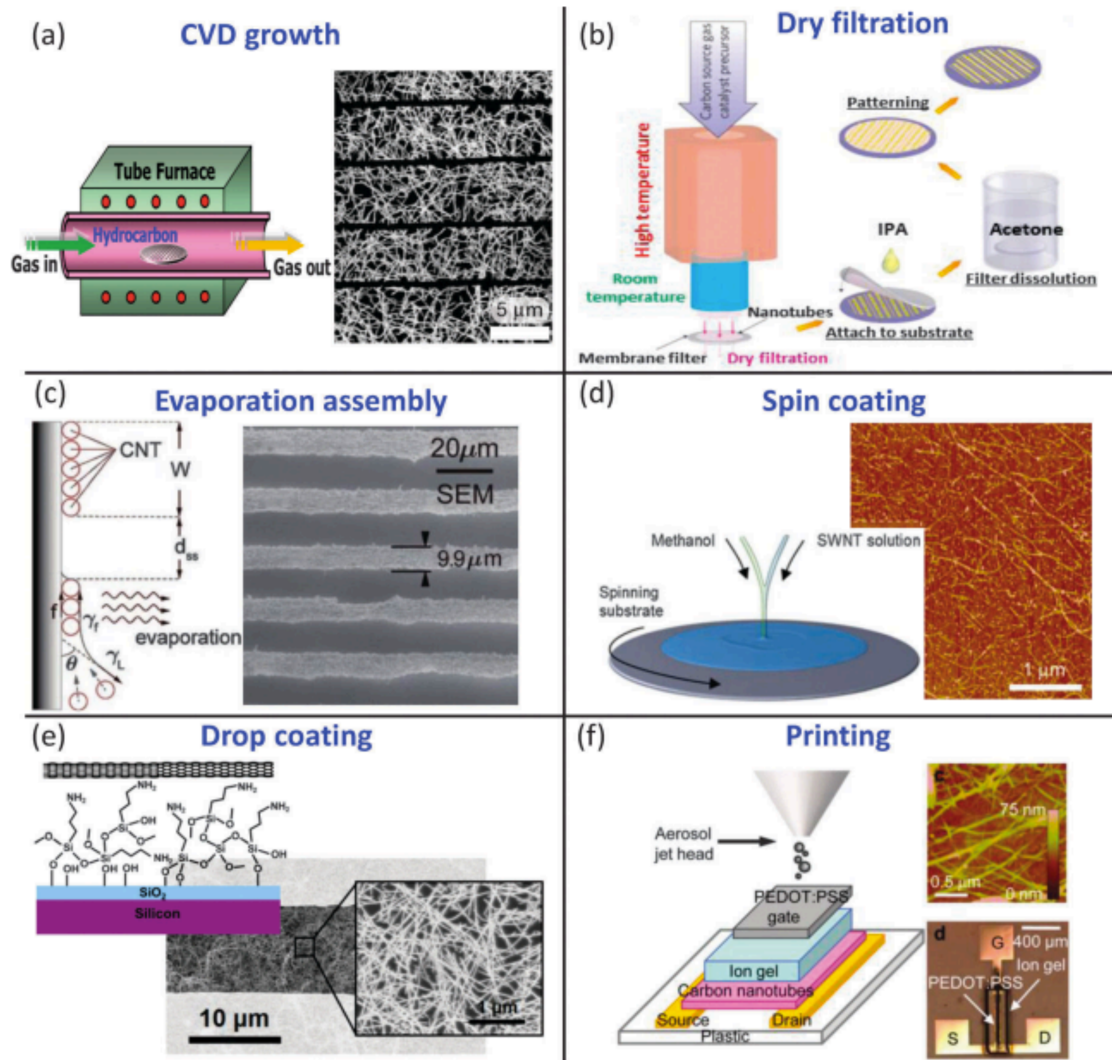

Figure 2-9. Different methods used for assembly of SWNT networks. **(*a*)** CVD growth[25, 26], **(*b*)** Dry filtration[27], **(*c*)** Evaporation assembly[28], **(*d*)** Spin coating[29-31], **(*e*)** Drop casting[32-35], **(*f*)** Printing[36-39] (from reference 47).

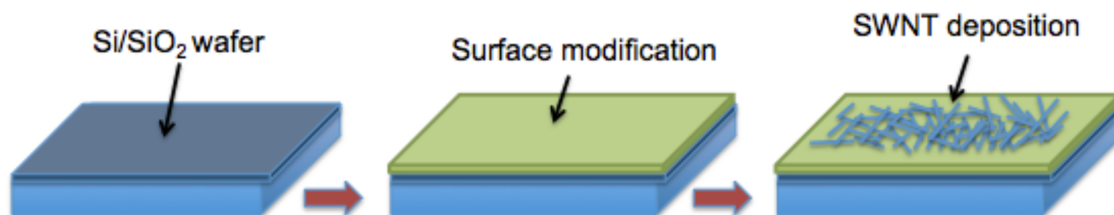

Figure 2-10. Schematic of SWNT deposition process. Surface is modified with either poly-L-lysine or aminopropyltriethyoxysilane (APTES) in this study.

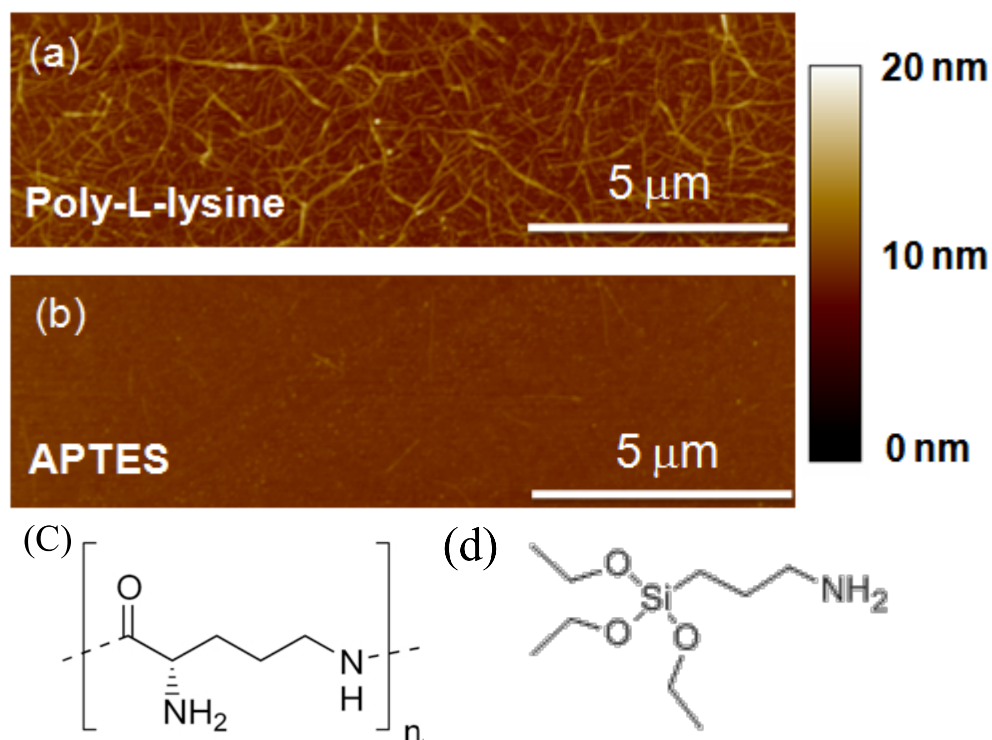

Figure 2-11. The effect of surface treatment on the deposited nanotube density. The surface is treated with ***(a)*** poly-L-lysine for 5min and ***(b)*** aminopropyltriethyoxy silane (APTES) for 30min. SWNT deposition time is 20min.Chemical structure of ***(c)*** poly-Llysine and ***(d)*** APTES.

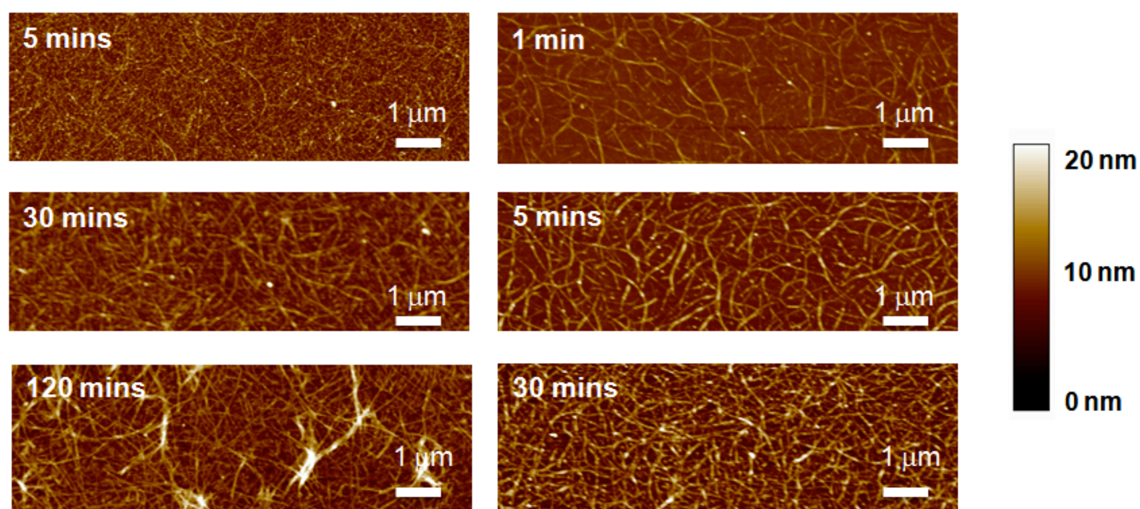

Figure 2-12. AFM images taken from different SWNT deposition time on ***(a)*** evaporated SiO_2 and ***(b)*** thermally grown SiO_2. For (*a*), 5min, 30 min, and 120 min are used, and for (*b*) 1 min, 5 min, and 30min are used as SWNT deposition time. The density increases as the deposition time increases, and eventually it forms nanotube bundles, degrading the device I_{ON}/I_{OFF} ratio.

2.3 Summary

In this chapter, simple but versatile assembly methods for parallel NWs array and random network SWNTs are discussed. Parallel NW arrays are readily printed on arbitrary substrate at room temperature with contact printing technique combined with monolayer resist, while SWNT random network is controllably deposited with proper surface modification. By using these NW arrays or SWNT networks as the active components of TFTs, the stochastic device-to-device variation is drastically reduced, thereby, presenting a viable route towards the utilization of functional nanoscale materials for practical applications.

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Chapter 3
Assembled semiconductor NWs device component

3.1 Introduction

In this chapter, electrical and optical properties of discrete parallel array NW TFTs assembled by contact printing are characterized.

Firstly, in section ***3.2***, the electrical properties of InAs NW parallel array TFTs are investigated, especially in the radio frequency regime. Previously, the electrical properties of single InAs NW grown by CVD has been systematically studied[44], showing a respectable field-effect electron mobility of 2500 cm^2/Vs for radius of 25 nm, with I_{on}/I_{off} ratio of 10^4. In this study, we assemble InAs NWs into parallel arrays with contact printing, and investigate the performance limit of InAs NW parallel array TFTs.

Secondly, the electrical and optical properties of spatially composition graded CdS_xSe_{1-x} (x=0 to 1) NWs are discussed in section ***3.3***. Due to the lattice mismatch required for epitaxial growth, bandgap control by alloying crystalline semiconductors with different bandgaps has been challenging. To address this issue, in this study we utilize CVD-grown compositionally graded CdS_xSe_{1-x} NW alloy, and transfer them into parallels array by contact printing to realize tunable-wavelength photodetectors.

3.2 Parallel Array InAs Nanowire Transistors for Mechanically Bendable, Ultra High Frequency Electronics[◊]

Over the past several years, semiconductor nanowires (NWs) have been extensively explored for electronic and sensor applications[1-8] owing to their unique physical properties with tunable and well-defined atomic composition[9]. In one specific platform, a contact printing technique is utilized for the large-scale assembly of NW parallel arrays on a support substrate, followed by the device fabrication[10-13]. Since NW arrays are utilized, the stochastic device-to-device variation is drastically reduced which is of practical importance[14-16]. The performance limits of the enabled devices, however, are still unknown. In this regard, here we characterize the radio-frequency (RF) response

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◊ The work presented here has been published in a similar form to the following reference; T. Takahashi, K. Takei, E. Adabi, Z. Fan, A. M. Niknejad, A. Javey, *ACS Nano*, 4 (10), 5855-5860, 2010.

of InAs NW-array transistors on bendable substrates, elucidating an important performance metric for determining their potential application domain. Notably, for the first time, the GHz operation of mechanically flexible, NW parallel array devices is demonstrated. The results demonstrate the potential of NW-array devices for ultra high frequency (UHF) electronic circuits.

UHF electronics operating in the 0.3-3 GHz regime are highly attractive for various analog and digital circuits[17, 18]. The ability to fabricate these devices on mechanically bendable substrates that conform to non-planar surfaces, and potentially by printing techniques may further broaden their utility and application domain. In this work, highly-aligned InAs NW arrays were utilized as the active channel material of the flexible, UHF field-effect transistors (FETs). InAs NWs are attractive for such applications due to their high electron mobility[2, 4, 19], high electron saturation velocity, ease of ohmic metal contact formation[4, 20], and miniaturized diameters that make them mechanically flexible.

InAs NWs used in this study were synthesized on Si/SiO_2 substrates by a physical vapor transport method[4]. The grown NWs had an average diameter and length of ~ 30 nm and ~ 10 μm, respectively. Subsequently, NW contact printing[10, 11, 15] was carried out by directionally sliding a growth substrate, consisting of randomly grown InAs NWs, on top of a polyimide (PI) layer (24 μm) spin-coated on a Si/SiO_2 handling wafer. During this process, NWs are directly transferred from the growth substrate to the PI surface as parallel arrays[10, 11, 15]. To achieve patterned assembly of NWs, the PI surface is first coated with a lithographically patterned resist layer, followed by NW printing and lift-off in a solvent. Nickel (~50 nm) source (S) and drain (D) electrodes were then formed, followed by atomic layer deposition of Al_2O_3 (~8 nm) at 150 ºC as the gate dielectric. Finally, Al (40 nm) top-gate (G) electrodes were fabricated. All electrodes were defined by photolithography and lift-off processes. There is ~200nm of misalignment due to the limitation of the contact aligner, resulting in the overlap of G with one of the S/D electrodes and underlap with the other, resulting in a parasitic capacitance and series resistance, respectively. The channel length (S/D electrode spacing) is L ~ 1.5 μm, and the channel width is W = 100-200 μm. The gate electrode length is L_G ~ 1.4 μm. The configuration of the electrical pads matches that of the conventional ground-signal-ground (GSG) microwave probes (150 μm pitch). Figure 3-1*a* shows the layered schematic of a NW-array RF device. The optical microscopy images of a completed device are shown in Figures 3-1*c*-*d*, clearly depicting the active NW-array region and the GSG electrode configuration. The printed NW density is ~ 4 NWs/μm as confirmed by scanning electron microscopy. After the completion of the fabrication process, the PI layer is peeled off from the rigid Si/SiO_2 handling wafer, resulting in mechanically flexible device arrays as shown in Figure 3-1*b*.

Figure 3-2*a* shows representative output characteristics of an InAs NW-array FET with W = 100 μm on a flexible PI substrate. The FET delivers a unit-width normalized ON current of I_{ON} ~ 23 μA/μm at V_{DS} = 2 V. Individual NWs with comparable lengths and diameters deliver ~10 μA of ON current based on our previous studies[4] From the current density, we estimate that ~2 NW/ μm cross the S/D electrodes with the rest of the

NWs only contacting one electrode and thereby serving as parasitic elements (i.e., they contribute to the gate capacitance but not the transconductance). A respectable ON/OFF current ratio, I_{ON}/I_{OFF} ~ 100 is observed at V_{DS} = 2.5 V as shown in the inset of Figure 3-2*b*. From the I_{DS}-V_{GS} curve at V_{DS} = 2.5 V, the peak transconductance, $g_m = \frac{dI_{DS}}{dV_{GS}}|_{V_{DS}}$ ~ 1.1 mS (i.e., ~11 µS/µm as normalized by W) is measured at V_{GS} = -0.5V (Figure 3-2*b*). From the slope of I_{DS}-V_{DS} curve at V_{DS} = 2.5 V and V_{GS} = -0.4 V, the output resistance, r_o ~ 8 kΩ is obtained, which corresponds to a gain of $A_v = r_o\, g_m$ ~ 8. A_v is the intrinsic gain of a transistor with no loading (*i.e.*, transistor is self-loaded) which is an important figure for operation amplifiers, instrumentation amplifiers, and other circuit components where large gains are desirable. Furthermore, the mechanical flexibility of the devices was tested by measuring the electrical properties as a function of the radius of curvature. The NW-array FETs do not exhibit a significant electrical degradation, even when bent to a radius of ~18 mm with compressive/tensile stress (see Appendix B, Figure B-1), which is attributed to the miniaturized dimensions of NWs. Additionally, since InAs NWs have significantly higher Young's modulus than the supporting PI substrate, the strain is mostly compensated by the substrate with the strain in the NW being only ε_{xx} ~ 0.5 % as predicted from mechanical simulations (Figure B-1).

To directly extract the high-frequency behavior, the two-port scattering parameters (S-parameters) of InAs NW-array FETs were measured in the common-source configuration using standard procedures with a Vector Network Analyzer (VNA) over a frequency range from 40 MHz to 10 GHz (Anritsu 37397C). Calibration of the probe tips were performed by employing the Short-Open-Load-Thru method (see Appendix B1) on an impedance standard substrate provided by Cascade Microtech (ISS 101-190). On-wafer pad-open and pad-short structures were used to de-embed the parasitic effects of the contact pads, that is, shunt capacitance/conductance and series inductance/resistance (see Appendix B for the details). This de-embedding does not correct for the overlap capacitances between the gate and source/drain electrodes. S-parameters were then used to analyze the RF performance of the device (Figure 3-3*a*). S_{11}, S_{22}, S_{21}, and S_{12} are respectively the reflection coefficient of the input, the reflection coefficient of the output, the forward transmission gain, and the reverse transmission gain. Figure 3-3*b* shows various RF metrics of a representative device with W = 200 µm, all derived from S-parameters. Specifically, unity transit frequency of the current gain (h_{21}) of a transistor is called f_t, and is an important factor for determining the high frequency limit of the transistor for various analog/RF and digital applications. To obtain f_t from the measurements, S-parameters are first converted to hybrid parameters (h-parameters) as described in the Appendix B. The parameter h_{21} is plotted as a function of frequency (Figure 3-3*b*), and f_t occurs at the frequency where h_{21} equals 1, that is, 0 dB. As depicted in Figure 3-3*b*, InAs NW-array FETs exhibit an impressive f_t = 1.08 GHz. Maximum stable gain (MSG), the gain a transistor can provide if suitable input and output matching networks are incorporated for an unconditionally stable amplifier design, is also extracted (see Appendix B), and plotted as a function of frequency (Figure 3-3*b*). At 1 GHz, the MSG of the FET is ~ 6 dB which confirms that designing an RF amplifier at the GHz regime is plausible. Finally, maximum unilateral gain (U, Mason gain) is extracted (Supp. Info.) as a function of frequency (Figure 3-3*b*). Mason gain is the maximum unilateral power gain the device can provide at a specific frequency of

operation. The maximum frequency of oscillation, f_{max}, is determined by extracting Mason's gain at 0 dB. It is an important figure of merit and at frequencies beyond f_{max}, a transistor cannot provide any power gain, and turns into a passive component. As shown in Figure 3-3*b*, the NW-array FET has f_{max}=1.8 GHz.

A small signal model can also be fitted to the S-parameter data to be used in the future circuit design and optimizations, and further extract key device parameters. The small signal equivalent circuit is shown in Figure 3-3*c*-*d*. At the core is the hybrid-π model of the transistor including g_m, r_o and the capacitances (C_{GS}, C_{GD} and C_{DS}). Non-quasi-static (NQS) resistance, R_{NQS} and the series resistance (R_G, R_S, R_D) and inductance (l_G, l_S, l_D) associated with the gate, source and drain interconnects are added, resulting in the match between measured data and the fitted small signal model data (Figure 3-3*a*, see Appendix B for details). The extracted component values for the small signal model are listed in Table 3-1.

To further characterize the devices, S-parameters were measured at different drain and gate voltages with the extracted f_t shown in Figure 3-4*a*. As expected, f_t monotonically increases with V_{DS} for the explored bias range due to an increase in g_m. The peak f_t is obtained at V_{GS} = -2 V, most likely corresponding to when the Fermi level coincides with the first conduction sub-band edge of the InAs NW channel. Due to the non-parabolicity of the band structure, effective mass increases as the Fermi level goes deeper into the conduction band, thereby lowering the electron mobility and saturation velocity. Since cutoff frequency is proportional to saturation velocity, it follows that as higher positive gate voltages f_t decreases. Similarly, g_m can be extracted as a function of bias from the RF measurements (Figure 3-4*b*). A peak transconductance of g_m ~ 12 μS/μm at V_{DS} = 3 V and V_{GS} = -2 V is obtained from the AC small-signal RF characteristics, which is consistent with the value obtained from the DC measurements (Figure 3-2*b*). Note that the devices in Figures 3-2 and 3-4 are not the same. Due to the device-to-device variations, the threshold voltage is slightly different.

Next, we examine the theoretical performance limit of InAs NW-array FETs. The cutoff frequency is projected from the relation, $f_t = \frac{g_m}{2\pi(C_{GS} + C_{GD})}$. In the high field operation regime (*e.g.* high V_{DS} and/or short L_G, as is the case in this work), the carriers propagate at the saturation velocity, v_{sat}, with the transconductance given as $g_m = v_{sat}(C_{ox}/L_G)$. Here C_{ox} is the gate oxide capacitance and can be obtained from $C_{ox} = C_{ox,1} \times (Wd)$, where $C_{ox,1}$ is the NW-gate capacitance for a single NW and d is the NW density. The cutoff frequency is then $f_t = \frac{v_{sat} C_{ox}}{2\pi L_G (C_{GS} + C_{GD})}$. Note that the total gate-source capacitance is given as $C_{GS} = C_{p,GS} + \frac{2}{3} C_{ox}$, where $C_{p,GS}$ is the parasitic capacitance between G/S electrodes. The exact velocity-field curve for InAs NWs is unknown, so we use the bulk curve for the purpose of this analysis. The cutoff frequency is then calculated by using the extracted capacitances for the explored device geometry (Table 3-1) and v_{sat} ~1.3×10^7 cm/s at a field of 16 kV/cm (corresponding to V_{DS} = 2.5 V and L_G = 1.5 μm).[21] From this analysis, f_t ~ 7 GHz is projected for d = 2 NWs/μm (Figure B-3) and L_g = 1.5

μm which is ~7× higher than the experimental f_t for the same NW density. This may be attributed to the dominant rote of surface scattering in the electron transport properties of un-optimized InAs NWs used in this work. In the future, exploration of surface passivation layers may help to further enhance the measured frequency response of NW RF-FETs. Additionally, by increasing the printed NW density to 20 NWs/μm (50 nm pitch), the theoretical f_t increases to ~13 GHz. Finally, in the absence of all parasitic elements, an ultimate theoretical f_t of ~14 GHz is projected, presenting the "intrinsic" cutoff frequency of the InAs transistors at the explored length scales. Further gate length miniaturization can also enhance the RF performance.

The GHz operation of our FETs compare favorably with the other previously explored flexible device concepts. For example, hydrogen terminated amorphous silicon or silicon films with various degrees of crystallinity have been widely utilized for applications in large scale electronics with the highest reported f_t of ~250 MHz on plastic substrates[22]. Organic transistors have been limited to f_t of ~10 MHz[23] due to their low carrier mobilities. Several groups have achieved GHz operation using carbon nanotube arrays on either a plastic or rigid substrate[17, 24-27], and graphene on a rigid substrate[28]. However, these devices exhibit poor I_{ON}/I_{OFF} due to the mixture of metallic nanotubes in the arrays and the small bandgap of graphene. Previous works utilizing NWs for flexible electronics resulted in devices operating at 10-100 MHz[29-31] although higher frequencies have been reported for single NWs with short channels on rigid Si substrates[32]. Egard *et al.*[33] recently reported gigahertz devices with f_t > 7 GHz and f_{max} > 20 GHz based on vertical InAs NW arrays grown epitaxially on InP wafers with a gate length of ~100 nm. This works shows the potential of InAs NWs for high frequency transistors, however, the explored structure and geometry are not compatible with flexible electronics. Recently, promising flexible devices[34] are reported using inorganic single crystalline flakes such as Si (f_t ~ 0.5-3 GHz for L_G ~ 2μm)[35, 36] and GaAs (f_t ~ 1.5 GHz for L_G ~ 2 μm)[37]. These devices are fabricated *via* top-down etching and subsequent transfer method. The RF NW device concept presented here has the advantage of potentially utilizing an all-printed fabrication scheme, without the need for complex lithographic processes.

The presented results show the potential of NW-array FETs for future microwave applications on non-conventional substrates as enabled by (i) the uniform and dense assembly of NW parallel arrays, (ii) the inherently high saturation velocity of InAs, and (iii) the appropriate device design. This technology is of particular interest given the recent rapid growth of signal communication over the UHF bands. Notably, the explored device dimensions are within the resolution limit of advanced printing processes[38], thereby, making the presented platform potentially compatible with continuous roll-to-roll fabrication processes. In the future, further miniaturization of the device dimensions, improved printed NW-array densities and the use of surface passivation layers through process optimization are projected to enhance the cutoff frequency of the devices by an additional ~10×. This projected performance cap is comparable to that of the state-of-the-art, nanoscale Si devices, but uniquely, is attainable on non-rigid substrates and with all-printed fabrication processes.

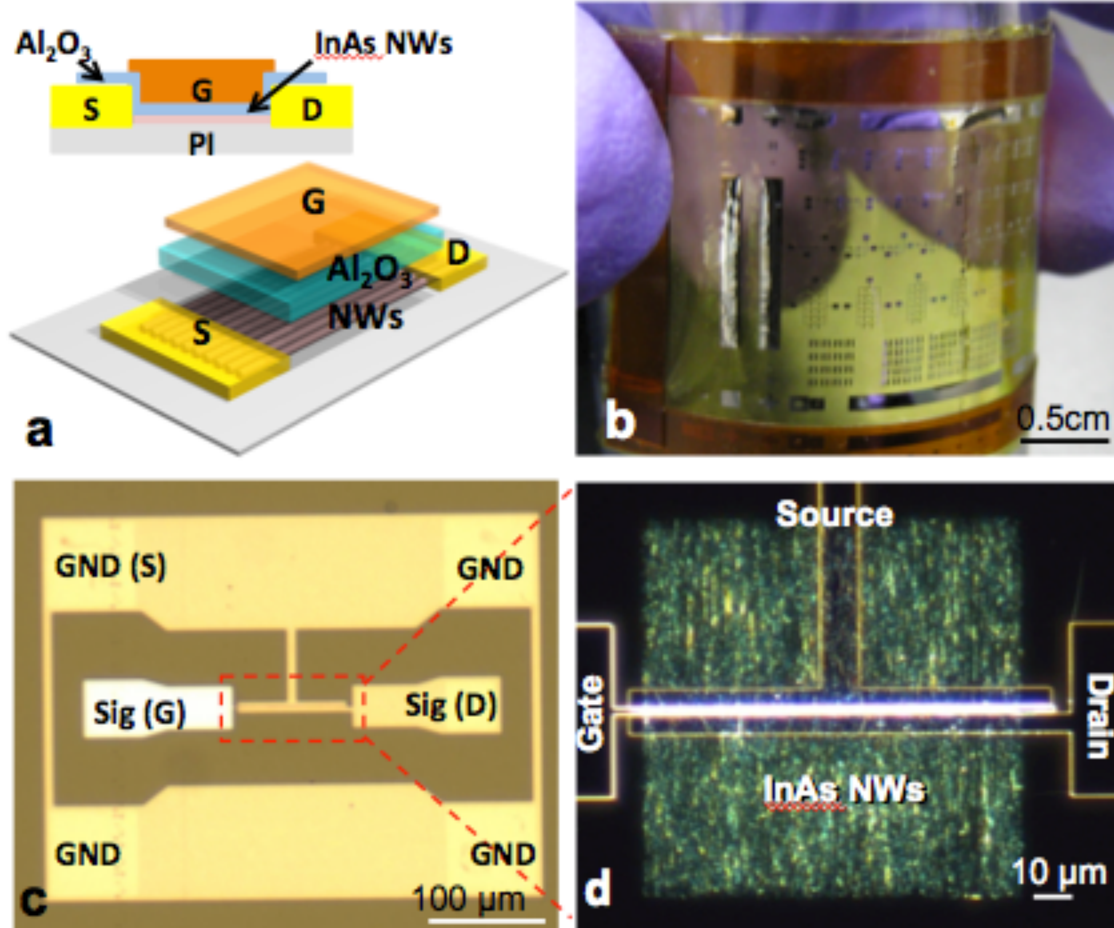

Figure 3-1. The schematic and optical images of a printed InAs NW array FET fabricated on a flexible PI substrate for GHz operation. **(*a*)** The schematic illustration of the NW parallel array FET, illustrating the various layers of the device. The cross-sectional image is shown in the top. **(*b*)** A photograph image of the fabricated NW device array on a bendable PI substrate. **(*c*)** A bright-field optical image of a NW-array FET with ground-signal-ground configuration for the RF measurements. **(*d*)** A dark-field optical image, showing the printed InAs NW region.

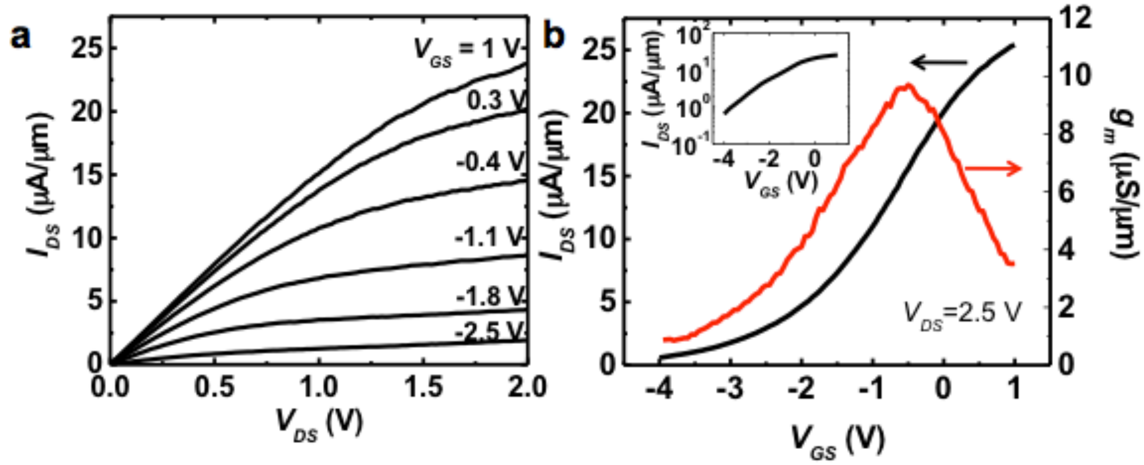

Figure 3-2. DC characteristics of an InAs NW-array FET. ***(a)*** The normalized output characteristics of a NW-array FET with a channel width, W~100 μm and gate length, L_G~1.5 μm. ***(b)*** Linear-scale transfer characteristic and the corresponding transconductance as a function of gate bias at V_{DS}=2.5V. The log-scale I_{DS}-V_{GS} at V_{DS}=2.5 V is shown in the inset.

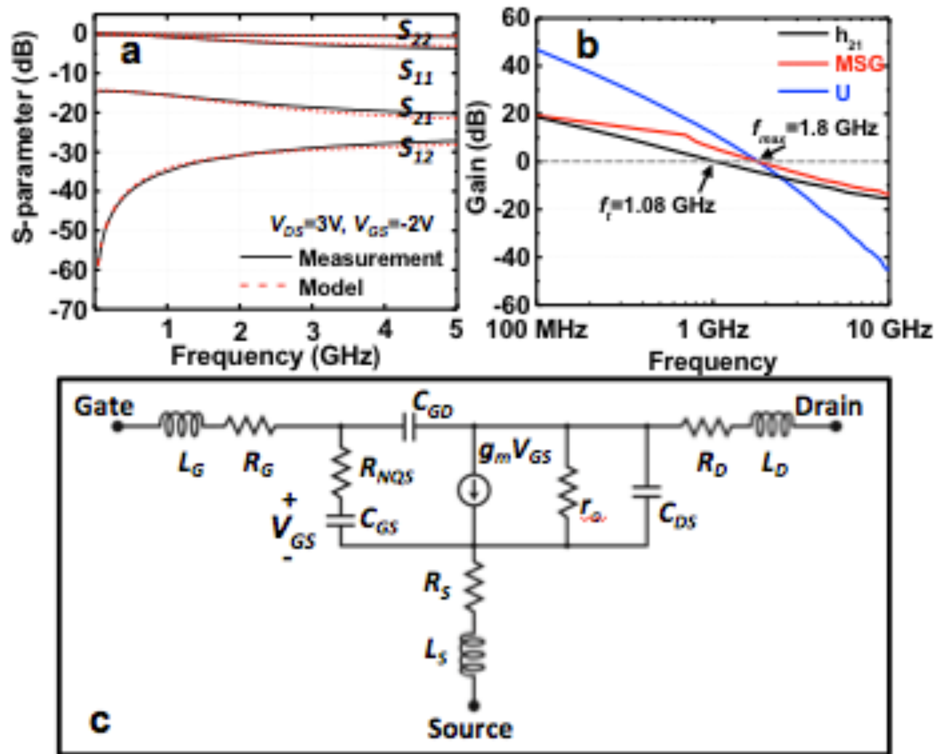

Figure 3-3. RF characterization of an InAs NW-array FET. ***(a)*** The measured (black solid line) and modeled (red dashed line) scattering parameters, S_{11}, S_{12}, S_{21} and S_{22} of an InAs NW array FET with W~200 µm after de-embedding for frequencies between 40 MHz and 5 GHz. ***(b)*** The current gain (h_{21}), maximum stable gain (MSG), and unilateral power gain (U) extracted from measured S-parameters as a function of frequency. The unity current gain frequency, f_t, and unity power gain frequency, f_{max}, are ~1.08 and 1.8 GHz, respectively. ***(c)*** Small signal equivalent circuit model and d, device schematic, illustrating the various circuit components. R_S, R_D, and R_G are composed of metal sheet resistance and contact resistance.

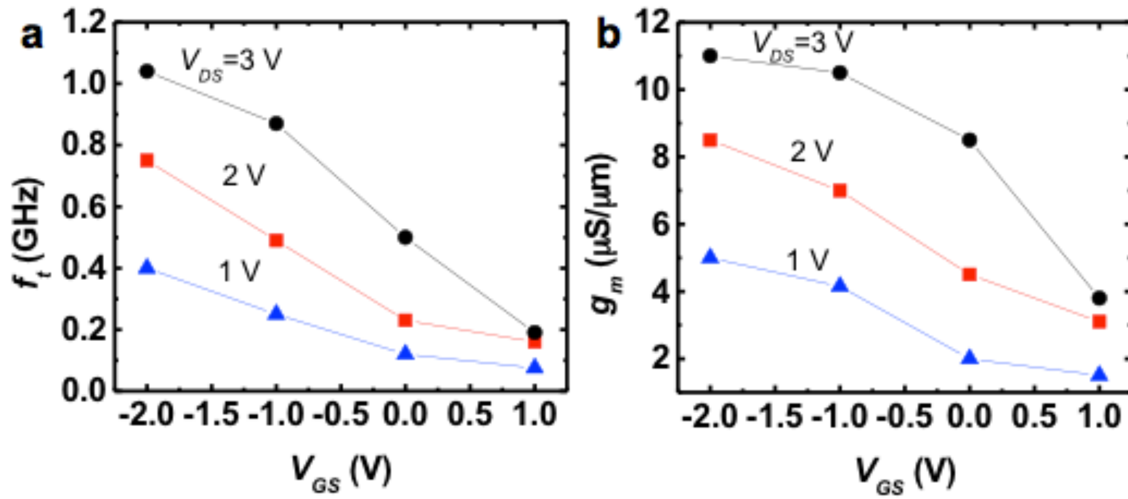

Figure 3-4. Bias dependence of the RF response. ***(a)***, ***(b)*** The measured unity current gain frequency and transconductance as a function of V_{GS} and V_{DS} for a NW-array FET with W=200 μm.

Table3-1.

g_m	r_o	C_{GS}	C_{GD}	C_{DS}	R_G	R_S	R_D	R_{NQS}	l_G	l_S	l_D
2.3 mS	13 kΩ	315 fF	35 fF	10 fF	102 Ω	66 Ω	73 Ω	85 Ω	200 pH	92 pH	148 pH

Table 3-1. The extracted and fitted parameters from small signal RF modeling for a NW-array FET with W = 200 μm and L = 1.5 μm.

3.3 Compositionally graded CdS_xSe_{1-x} NW parallel arrays for tunable photodetector[◊]

The ability to spatially tune the bandgap of semiconductors enables new applications such as tunable wavelength optoelectronic devices. Bandgap controllability by alloying crystalline semiconductors of different band gaps with existing thin film growth techniques is, however, severely limited by lattice matching required for epitaxial film growth. Recently, it has been demonstrated[39, 40] that these restrictions are dramatically relaxed by the use of nanowires (NWs)[41]. Various compositionally graded NWs grown on a single substrate have been reported for material systems such as $In_xGa_{1-x}N$[11], CdS_xSe_{1-x}[40, 42], and $Zn_xCd_{1-x}S_ySe_{1-y}$[43, 44]. This approach to semiconductor alloying has led to the first growth of quaternary alloy nanostructures in the form of ZnCdSSe nanobelts, and composition grading over the entire visible spectrum on a single substrate[44]. Specifically for the ternary CdS_xSe_{1-x} alloy, the full composition range from CdS (x=1, band gap: 2.44 eV) to CdSe (x=0, band gap: 1.72 eV) covers an important range of the visible spectrum (500-700 nm). Spatially composition graded CdSSe NWs with optically pumped lasing behavior over a broad wavelength tuning range have been reported[40]. Due to the random orientations of the as-grown nanowires, fabrication of electrical devices is challenging without subsequent re-alignment. Here, compositionally graded CdS_xSe_{1-x} NWs are combined with a previously reported contact printing method[45, 46, 47] in which as-grown NWs are directly transferred to any arbitrary substrate (p+Si/SiO_2 substrate in this work) by directional sliding, thus preserving the spatial compositional grading. With this simple one-step printing, an organized collection of parallel NW-arrays with different band gaps are assembled for subsequent device fabrication, which is otherwise unobtainable by conventional methods.

CdS_xSe_{1-x} alloy NWs spanning the full composition range are synthesized on a Si/SiO_2 substrate by the dual gradient method which combines a temperature gradient and spatial gradient of source materials across the substrate for optimal growth of each material composition[43]. Commercially available CdS and CdSe powders (Alfa Aesar, 99.995% purity) are each loaded into individual source dispersion tubes within a quartz tube furnace. The Si/SiO_2 substrate with 2 nm thick Au catalyst film is placed downstream facing the openings of the source dispersion tubes. The substrate orientation is vertical with a slight angle such that its two ends are at different axial locations within the temperature gradient region near the exit of the furnace. With 100 sccm gas flow of 5% H_2 in Ar, the pressure is maintained above 600 Torr to prevent source material diffusion while the furnace is heated slowly to 700 ^oC. The pressure is reduced to 5 Torr and held for 30 minutes of growth. The real-color photograph of the as-grown spatially composition-graded CdS_xSe_{1-x} NWs substrate is shown in Fig. 3-5*a*. It is confirmed from

◊ The work presented here has been published in a similar form to the following reference; T. Takahashi, P. Nichols, K. Takei, A. C. Ford, A. Jamshidi, M. C. Wu, C. Z. Ning, A. Javey, *Nanotechnology*, 23, 045201, 2012.

photoluminescence (PL) that the bandgaps of the as-grown NWs cover most of the visible spectrum range (data not shown here). Figs. 3-5*b-d* shows scanning electron microscopy (SEM) images of as-grown NWs taken from three different positions: a [cm] = 0, 0.3 and 0.6 with a = 0 corresponding to the Se-rich region. As the composition becomes Se-rich, the morphology of NWs becomes tapered and short (< 5 μm) due to the involvement of vapor-solid growth mechanism in addition to vapor-liquid-solid growth. The NWs are transferred as parallel arrays on a Si/SiO_2 substrate using a contact printing method[45, 46]. Next, Ti (5 nm)/Au (40 nm) is deposited with electron beam evaporation to form source/drain contact electrodes. With this simple one step printing, the photodetectors made of compositionally graded parallel NW arrays are readily achieved (Fig. 3-5*e*).

Figure 3-6*a* shows the normalized PL spectra measured at room temperature from the printed CdS_xSe_{1-x} NW-arrays. The PL peaks vary between ~525 nm and ~ 650 nm as a function of location (Fig. 3-6*a*), and the spectra show no midgap emission bands. In the inset, a representative SEM image of the printed NWs from a = 0.4 region is shown. Further growth optimization is required for the printing of NW-arrays with full composition range. Figure 3-6*b* shows the X-ray diffraction (XRD) data taken from three different locations on the printed substrate. The diffraction peaks are in good agreement with typical bulk hexagonal wurtzite crystal structures (CdS: JCPDS 41-1049). The results are consistent with previously reported transmission electron microscope studies of the as-grown CdS_xSe_{1-x} NWs[42]. The diffraction peaks from bottom to top gradually shift toward higher angles, indicating the lattice constant gradually decreases as NWs become S rich. With extracted lattice cell parameters, composition x is determined to be in the range between x=1 (CdS) and x=0.52 ($CdS_{0.52}Se_{0.48}$)[42, 43].

Next, the photoresponse of printed parallel NW arrays is investigated. The composition used in the representative device is $CdS_{0.52}Se_{0.48}$ (a ~ 0.3). Figure 3-7*a* shows the angle dependent photocurrent measurement taken under a halogen lamp (1 mW/cm^2). Photocurrent was measured by changing the polarization direction of the incident light rotated from θ = 0° (maximum) to 90° (minimum), where θ is the angle between the NW orientation and polarization direction of the incident light, and normalized with the current at θ = 0°[48, 49]. The photocurrent shows a harmonic response and can be fitted to $\cos^2\theta$ function. The polarization anisotropies are calculated to be ~0.67 according to $\rho=(I_{\parallel}-L_{\perp})/(I_{\parallel}+L_{\perp})$, where $I_{\parallel}(L_{\perp})$ are the photocurrent obtained from light illumination parallel (perpendicular) to the NW direction. This value is compatible with previous reports, where CdSe NWs are aligned either with dielectrophoresis (~ 0.75)[48] or contact printing method (~0.54)[49]. Figure 3-7*b* shows the back-gated transfer characteristics (I_{DS}-V_{GS}) at V_{DS} = 3 V with and without illumination (halogen lamp, 13.2 mW/ cm^2). This clearly indicates that the I_{ph}/I_{dark} (photocurrent/dark current) ratio can be modified depending on the back-gate bias, and a high ratio (>100) is obtained for V_{GS} = 0 ~ 1 V. Figure 3-7*c* shows the dependence of photocurrent amplitude on optical power. The amplitude is expressed with a simple power law ($I_{photo} = c_1 P^{C_2}$), where P is the optical power, c_1 is a proportionality constant, and c_2 is an empirical value. By fitting, c_2 is 1.09. This superlinearity is due to the complex combination of electron-hole generation, trapping, and recombination process[50]. Figure 3-7*d* shows the time response

of the photocurrent measured under chopped light illumination (halogen lamp: 1 mW/ cm^2). The response time and recovery time, defined as the time between 10 % and 90 % of maximum photocurrent, are 200 ms and 800 ms, respectively. The time constants for response (τ_{resp}) is 130 ms, and those for slow and fast recovery ($\tau_{rec,slow}$, $\tau_{rec,fast}$) are 80 ms and 350 ms, respectively, which are obtained by fitting the equation $I = I_0\left(1 - e^{-\frac{t}{\tau}}\right)$ and $I = I_0 e^{-t/\tau}$ to the leading and trailing edge of single pulse. Biexponential behavior of recovery is consistent with previous studies of CdS nanoribbons (NRs)[51] and CdSe NRs[52]/NWs[53].

Finally, the spectral response is investigated from the representative devices chosen from three different locations (a [cm] = ~0.2, ~0.4, and ~0.6, corresponding to, respectively, Se-rich, middle region, and S-rich region). The normalized photocurrent at V_{DS} = 3 V, illuminated with the light through low pass filter with various cutoff wavelengths, is shown in Fig. 3-8. The transition wavelengths extrapolated for a = 0.2, 0.4, and 0.6 devices are ~690 nm (1.8 eV), ~600 nm (2.1 eV), and ~510 nm (2.4 eV), respectively, demonstrating NW-array photodetectors based on different bandgap materials. This result proves that the proposed concept of optical-electrical conversion with various wavelengths on a chip can be achieved. To estimate the bandgap of a ternary alloy, the interpolation of the bandgaps from its two binaries with additional nonlinear bowing can be used.

In summary, we demonstrate the capability to controllably assemble an organized collection of semiconductor nanomaterials with tunable bandgap by a simple but versatile one-step contact printing process. Eventually, this concept can be extended to other material systems for obtaining orthogonal response in optical and chemical sensors.

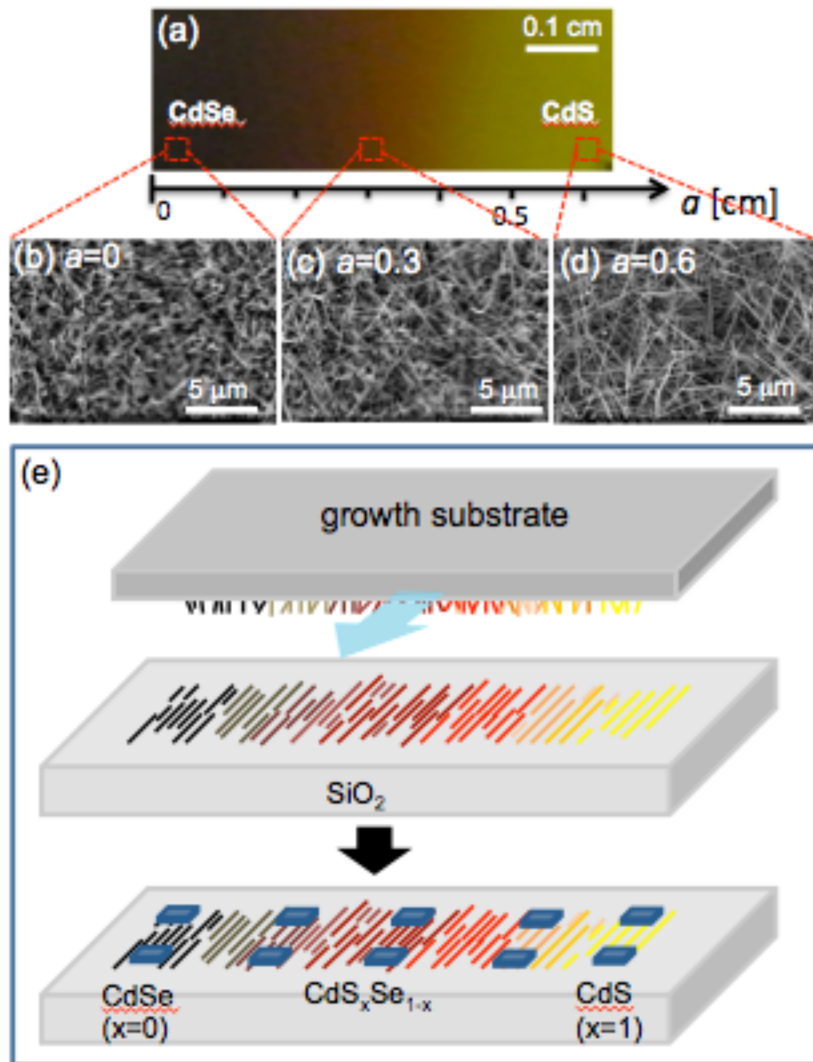

Figure 3-8. Compositionally graded CdS_xSe_{1-x} NWs. ***(a)*** Real-color photograph of as-grown spatially composition-graded CdS_xSe_{1-x} NWs. SEM images taken from three different locations, ***(b)*** Se-rich, ***(c)*** middle, and ***(d)*** S-rich region. ***(e)*** Schematic of contact printing method, and final device configuration for CdS/Se-based photodetectors.

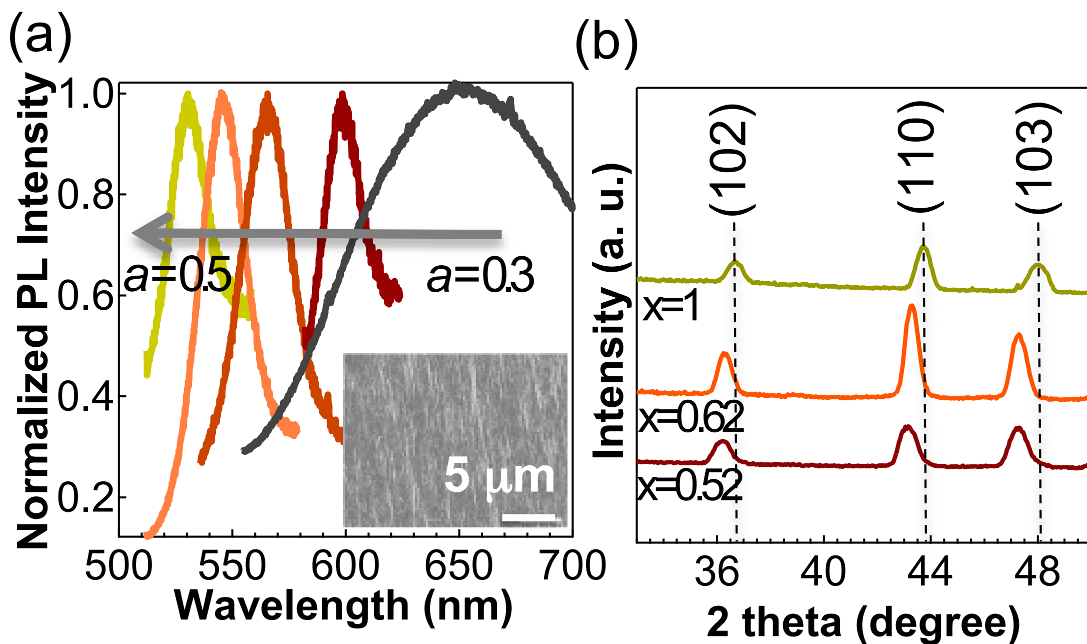

Figure 3-9. (***a***) Micro photoluminescence spectra of contact-printed compositionally-graded NW-arrays ($0.3 < a < 0.5$). SEM image of printed NWs from $a = 0.4$ region is shown in the inset. (***b***) The normalized X-ray diffraction patterns (XRD) of three different printed NW regions. The dash lines correspond to (102), (110), and (103), respectively (CdS: JCPDS 41-1049).

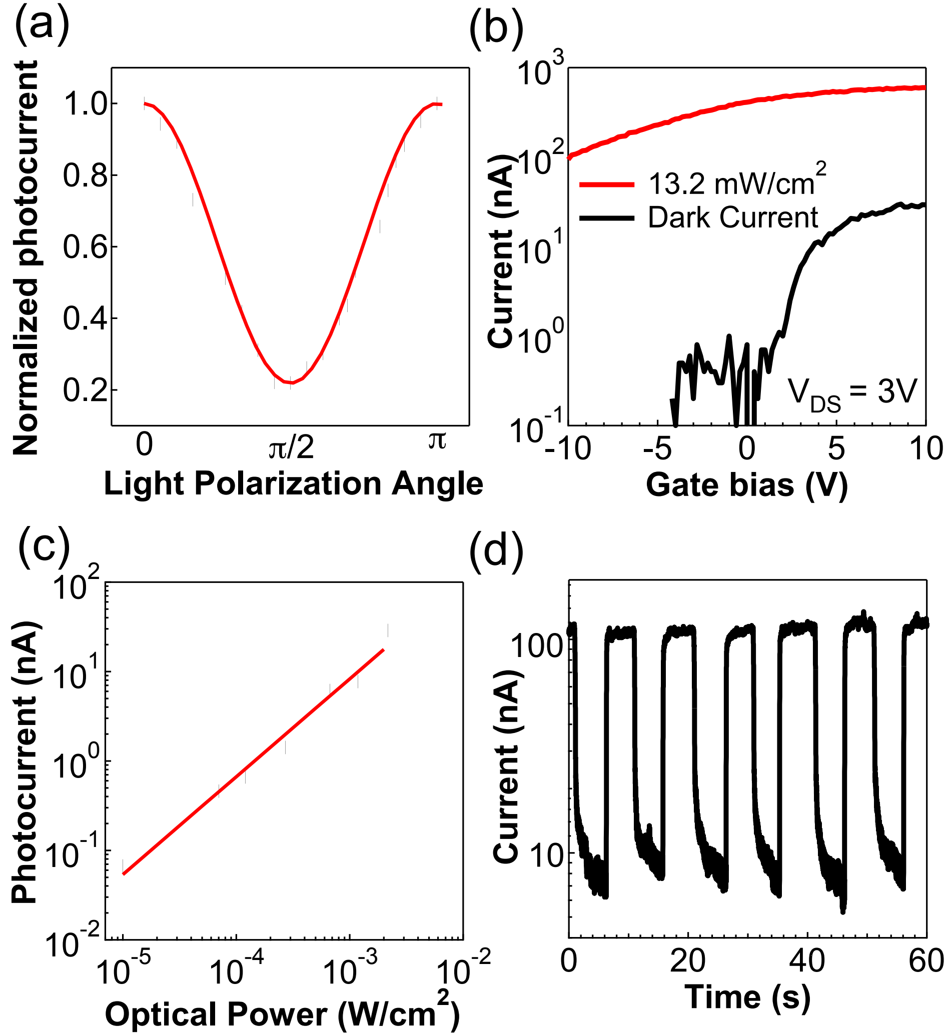

Figure 3-10. (***a***) Normalized photocurrent of $CdS_{0.5}Se_{0.5}$ NWs as a function of the angle of light polarization. Photocurrent is measured with V_{GS} = 0 V and V_{DS} = 3 V, and normalized with the current at θ = 0°. (***b***) Transfer characteristics of a $CdS_{0.5}Se_{0.5}$ NW-array device as a function of the back-gate voltage at V_{DS} = 3 V under dark (black line) and white light illumination at 13.2 mW/cm^2 (red line). (***c***) Photocurrent with V_{GS} = 0 V and V_{DS} = 3 V as a function of optical power intensity. (***d***) Time response under illumination at 2 mW/cm^2 with V_{GS} = 0 V and V_{DS} = 3 V.

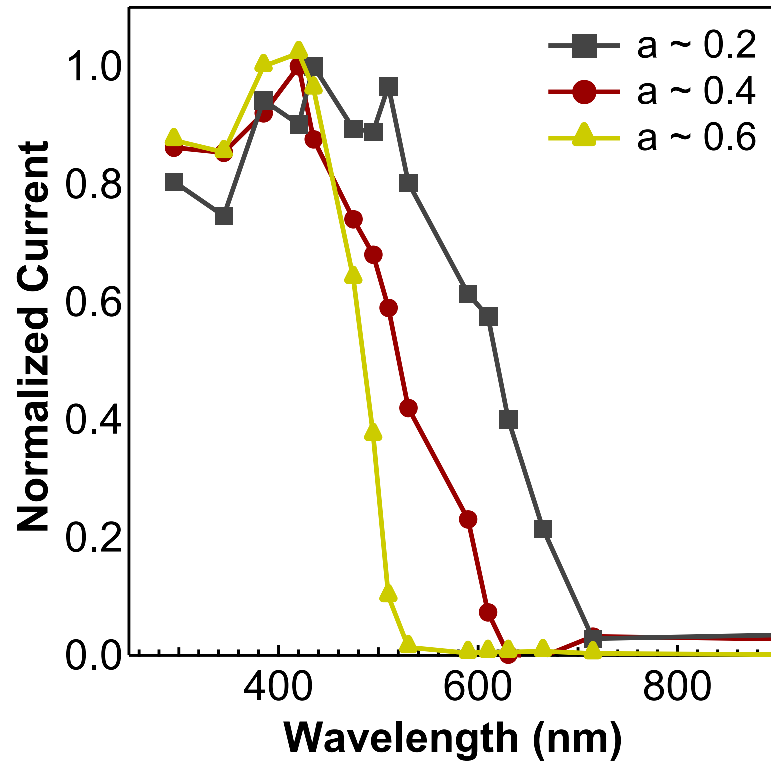

Figure 3-11. Spectral response of photocurrent obtained from three different NW-array devices corresponding to S-rich, middle and Se-rich regions.

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3.4 Summary

In this chapter, the electrical and optical properties of discrete TFTs composed of parallel InAs NW array and CdS_xSe_{1-x} NW array are characterized. InAs NW array TFTs fabricated on flexible substrates with a channel length of ~ 1.5 μm exhibit a peak transconductance of ~ 11 μS/μm at V_{DS} = 2.5 V with a maximum frequency of oscillation, f_{max} ~ 1.8 GHz and a cutoff frequency, f_t ~ 1 GHz, which are directly extracted from the radio frequency (RF) measurements. Furthermore, an array of tunable-wavelength photodetectors are demonstrated using compositionally graded CVD-grown CdS_xSe_{1-x} NWs combined with simple contact printing.

Chapter 4
System integration on large-scale flexible substrate

4.1 Introduction

In this chapter, the device characteristics of the integrated macro-scale flexible devices made of SWNTs network are discussed. At first, the electrical property of semiconductor-enriched SWNTs is studied, and the uniformity over 4-inch wafer scale substrate is discussed. Finally, artificial electronic skin (E-skin) is demonstrated, where active matrix circuitry made of SWNTs network TFTs are combined with pressure sensitive rubber (PSR). With superior electrical and mechanical properties of SWNTs to organic materials, low voltage operation (V_{DD} < 5V) and superb mechanical robustness and reliability are achieved.

In the latter half of this chapter, this active matrix circuitry is utilized to realize mechanically flexible light interactive e-skin for visible and x-ray imaging. In this device, organic photodiode: OPD (P3HT-PCBM) is used to detect either visible light or green light emitted from scintillator film (Gd_2O_2S:Tb) upon irradiation of x-ray photon, and placed in series with SWNT TFT in one pixel. 18 by 18 pixel arrays of flexible imager is achieved and its functionality is demonstrated by spatial mapping of irradiated light pattern.

4.2 Large-Scale Carbon Nanotube Active Matrix Circuitry for Conformal Electronics and Sensors[◊]

In recent years, flexible and stretchable electronics have been intensively explored for enabling new applications otherwise unachievable with the conventional Si technology[1, 2, 3]. A wide range of active channel materials have been explored, including organics[4, 5, 6, 7, 8, 9]; amorphous[10, 11], poly-[12, 13] and single-crystalline semiconductors in the shape of thin films and strips[14, 15]; printed semiconducting nanowires (NWs)[16, 17, 18]; and single-walled carbon nanotubes (SWNTs)[19, 20]. Each of these material systems presents unique opportunities and challenges for large-area electronics. For instance, randomly deposited films of SWNTs are attractive candidates given their high carrier mobility, high chemical stability, ability to deposit through solution processing, and superb mechanical

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◊ The work presented here has been published in a similar form to the following reference; T. Takahashi, K. Takei, A. G. Gillies, R. S. Fearing, A. Javey, *Nano Letters*, 11, 5408-5413, 2011.

properties such as high bendability[21, 22, 23]. A challenge, however, has been to fabricate devices with high ON/OFF current ratio, given that nanotube networks often consist of a mixture of semiconductor and metallic SWNTs[24]. In this regard, highly semiconductor-enriched (99%) SWNTs have been recently reported and commercialized through the use of a density gradient ultracentrifugation technique[25, 26]. This development has allowed for the fabrication of high performance SWNT thin-film transistors (TFTs) that exhibit high I_{ON}/I_{OFF} (>10^2) and mobility (>10 cm^2/Vs) on rigid Si substrates[27, 28, 29, 30]. This presents an important advance in the field and could result in the development of highly scalable and low-cost electronics with performances drastically superior to those of conventional organics or a-Si. Here, we extend on this work, and report the development of mechanically flexible and stretchable active-matrix backplanes based on semiconductor-enriched SWNT networks. We demonstrate fully-passivated and highly uniform SWNT TFT arrays, covering large areas of ~ 7.5 cm x 7.5 cm. As an example system, we utilize this active-matrix backplane for an artificial electronic skin (e-skin) device[8, 9, 16, 31], capable of spatial mapping of touch.

The device schematic of a mechanically deformable active-matrix backplane based on SWNT-TFTs is shown in Fig. 4-1*a*. A 24-μm-thick polyimide (PI) layer (PI-2525, HD MicroSystem) is used as the substrate. First, the PI is spin-coated twice (2000 rpm for 1min) on a Si/SiO_2 handling 4"-wafer, followed by Ni gate electrode deposition by thermal evaporation. The gate oxide consisting of three layers, with a 20-nm-thick Al_2O_3 layer deposited by atomic layer deposition (ALD) sandwiched between electron-beam deposited SiO_x layers (thicknesses, 10 nm and 15 nm on bottom and top, respectively). The bottom SiO_x layer is used to enable nucleation of ALD Al_2O_3 on the substrate, while the top SiO_x layer is used for adhesion of SWNTs. Note that it is observed that SWNTs are highly non-sticky to ALD Al_2O_3 surfaces, presumably due to fixed charges in the as-deposited alumina layer. To deposit highly dense and uniform SWNTs networks, the SiO_x surface is modified with poly-L-lysine by solution casting for ~5 min followed by a rinse with DI water. In this study, we use as-received 99 % semiconductor enriched SWNT solution (IsoNanotubes-S from NanoIntegris, Inc.), without any densification. SWNTs were then deposited by solution casting followed by rinse in DI water.

Figure 4-1*b* shows the atomic force microscopy (AFM) images of the SWNT coated substrates for three different nanotube deposition times. As evident, the density of SWNTs on the evaporated SiO_x depends on the deposition time, and is estimated to be ~6, 8 and 10 SWNTs/μm for the deposition time of 5, 30 and 90 min, respectively (Fig. 4-1*b*). It should be noted that the density of SWNTs as a function of deposition time is highly dependent on the particular surface being explored. For instance, higher densities of SWNTs with higher bundling probability are observed for similar deposition times on thermally grown SiO_2 layers (see Appendix C, Fig. C-2). Furthermore, the density depends on the nanotube solution, in part because different semiconductor-enriched products utilize different surfactants (Fig. C-1). Next, vacuum annealing at 200 ^oC for 1hr is performed to remove surfactant residues. This annealing process is essential to improve both the transconductance and I_{ON}/I_{OFF} of the devices (see Appendix C, Fig. C-3). Pd (thickness, ~35 nm) source/drain (S/D) electrodes are then patterned using

photolithography, metallization, and lift-off to enable ohmic contacts to the valence band of nanotubes for hole transport[32]. Finally, the fabrication process is completed by encapsulating the active matrix with parylene-C (~ 500 nm) to improve the mechanical robustness and chemical stability by removing environmental effects, including surface absorbed water molecules (Fig. 4-1*a*). Via contacts are made by pattern etching of parylene using photolithography and O_2 plasma etch. After the completion of the entire process, the PI layer is readily peeled off from the handling wafer, resulting in a mechanically flexible device.

Figure 4-2*a* shows the transfer characteristics of SWNT TFTs measured at V_{DS} = -5 V for three different deposition times. For each condition, 30 devices with channel length of L ~ 3 μm and width of W ~ 250 μm are randomly chosen across a 4-inch substrate and measured to study the stochastic device-to-device fluctuation. Figures 4-2*b*-*e* show the histograms of peak transconductance (g_m, unit width normalized), peak field-effect mobility (μ), log-scale I_{ON}/I_{OFF}, and the threshold voltage (V_t) for each deposition condition. The transconductance and I_{ON}/I_{OFF} are measured at V_{DS} = -5 V, and the mobility and threshold voltage are measured at V_{DS} = -50 mV. Calculation of the gate oxide capacitance must be addressed in the case of the SWNT network device[33]. Here, the effect of electrostatic coupling between nanotubes is considered with the following equation; $C_i = \left(\frac{1}{2\pi\varepsilon} \ln \left[\frac{\Lambda_0}{R} \frac{\sinh(\pi 2d/\Lambda_0)}{\pi} \right] + C_Q^{-1} \right)^{-1} \Lambda_0^{-1}$, where $1/\Lambda_0$ is the density of nanotubes, $C_Q = 4.0\times10^{-10}$ F/m is the quantum capacitance of nanotubes (ref. 34, 35), d is the oxide thickness, and R = 0.7 nm is the average radius of nanotubes. The calculated gate oxide capacitance values are 2.45×10^8 F/cm^2, 3.16×10^8 F/cm^2, and 3.78×10^8 F/cm^2 for SWNT deposition time of 5, 30 and 90 min, respectively. The field-effect mobility can then be extracted as, $\mu = \frac{L}{V_{DS}C_i}\frac{g_m}{W}$. As the nanotube deposition time increases from 5 min to 90 min, average peak g_m increases from ~0.4 to 1.5 μS/μm at V_{DS} = -5 V, resulting in an increased hole mobility, from ~ 18 to ~ 27 cm^{2}V^{-1}s^{-1}. On the other hand, I_{ON}/I_{OFF} shows the opposite trend, decreasing as the nanotube density increases. This is due to the bundling of SWNTs which makes gate control less effective, causing increased OFF-currents. In addition, by increasing the nanotube density, the probability of a direct metallic interconnection between the S/D electrodes increases given that 1% of SWNTs in the solution are still metallic[29, 30]. This point might be further improved in the future by using higher purity SWNTs and/or different surface chemistry. The relationship between mobility and I_{ON}/I_{OFF} is summarized in Fig. 4-2*f*. Due to the 99% semiconductor-enriched SWNTs used in this work, a high mobility of ~ 20 cm^{2}V^{-1}s^{-1} is obtained without sacrificing I_{ON}/I_{OFF} (~ 10^4) even for a relatively shorter channel length (L ~ 3 μm). Of particular importance, uniformity of the explored SWNT TFT technology on flexible substrates is impressive. Focusing on the 90 min deposition condition, the standard deviation for g_m, μ, log(I_{ON}/I_{OFF}), and V_t are ~11 %, 17 %, 11 % and 3 %, respectively.

The variations of the key performance metrics listed above are slightly larger than the state-of-the art organic materials[36], despite the fact that the devices are processed in non-cleanroom environment, but are sufficient for applications such as active-matrix

backplanes. Of particular importance, a high mobility, such as those obtained here, is highly desired for lowering the operating voltage and the size (i.e., width) of the FETs. This presents a major advantage for the use of SWNT TFTs over their organic counterparts for use as the active matrix backplanes, despite the fact that both are solution-processed. In addition, given the graphitic nature of SWNTs, they are highly robust and chemically stable, without degradation over time. These remarkable properties clearly set the advantage of semiconductor-enriched SWNT networks for large-area electronics. Here, we focus on the use of SWNT-TFTs for mechanically flexible and stretchable backplanes using PI as the support substrate. These backplanes could serve for development of displays, sensor arrays and imagers, just to name a few examples.

To obtain mechanically stretchable electronics, several approaches have been previously reported such as micro/nanostructures in 'wavy' layouts and open mesh substrate geometries[9, 37, 38]. Here, we utilize a honeycomb mesh structure, where an array of holes in the shape of hexagons are laser cut on a thin PI substrate with a fixed pitch of 3.3 mm and a varied hole side-length of a=1-1.85 mm (Fig. 4-3*a*). The mechanical stretchability of the PI mesh is then characterized as a function of a (Fig. 4-3*b*). The stretchability is defined as the maximum engineering strain that the substrates can tolerate before failure (i.e., breakage). The stretchability increases from zero to ~ 60 % as the side length of the hexagonal holes increases from 0 to 1.85 mm. This observation is consistent with the mechanical simulations, where the induced stress is found to be reduced by increasing the hole size (see Appendix C (Fig. C-5)). The unpatterned PI film is stiff and incapable of stretching. By cutting a honeycomb mesh pattern on the substrate, the enabled structure becomes stretchable because the PI bridges in-between the hexagonal holes can twist as evident from the optical images in Figs. 4-3*c* & *d*. Due to a structural symmetry, the honeycomb mesh is invariant to every 60° rotation, so the same stretchability can be observed for those directions. The degree of stretchability and directionality can be further tuned in the future by either changing the hole size and/or optimizing the mesh design.

Next, the mechanical stability of SWNT-TFT arrays on a honeycomb-structured PI substrate is studied. The PI substrate is laser cut into a honeycomb structure with a=1.25 mm after fully encapsulating the TFTs with parylene. Figure 4-4*a* shows the honeycomb patterned PI substrate with SWNT-TFT arrays conformably covering a baseball. Here, active devices with $L \sim 5$ μm and $W \sim 200$ μm are placed on the bridge intersects of each hexagonal as marked by blue circles in Fig. 4-4*a*. The nanotube deposition time is 60 min, corresponding to ~ 9 SWNTs/μm. The transfer characteristics at V_{DS}=-5V as a function of radius of curvature are shown in Fig. 4-4*b*. The device operates without noticeable degradation even when mechanically bent down to a 2 mm radius of curvature. In the inset of Fig. 4-4*b*, the normalized change in the conductance, $\Delta G/G_0$, where $\Delta G = G_0 - G$, and G and G_0 are the conductance for bent and relaxed (that is curvature radius is infinity) states, respectively, is shown. This bendability comes from the proper device design that exploits the neutral bending plane of the substrate, the miniaturized dimensions of SWNTs, and the mechanical robustness of the SWNTs. Similarly, the transfer characteristics as a function of unidirectional stretching are shown in Fig. 4-4*c*. Here, the substrate is pulled along its length while the TFTs are electrically

measured. The device functions with no change for stretching up to ~3 mm displacement, corresponding to ~11.5 % stretchability. The induced stress on stretching with 11.5 % of stretchability is calculated using a finite-element method simulation (Comsol Multiphysics 3.3) as shown in Appendix C. (Fig. C-5). It is clearly seen that most of the stress is introduced at the bridge regions, not on the active device regions.

Next, the thermal stability of the fully encapsulated SWNT TFTs is explored. The devices were heated in air from room temperature to 100 ^{o}C. Only a minimal change in V_t is observed (Fig. 4-4*d*), which could be attributed to a slight change of the dielectric constant of the various layers used in the devices. The results here suggest that the TFT array technology presented here are not only uniform over large-areas, but exhibit superb mechanical and thermal properties, ideal for large-area conformal electronics.

To demonstrate the utility of the proposed device scheme, as an example system, SWNT TFT active matrix backplane is used for spatial pressure mapping, consisting of a 12×18 (physical size of 6×4 cm^2) pixel array. Here, each pixel is actively controlled by a single TFT. The device effectively functions as an artificial electrical skin (e-skin), capable of detecting and mapping touch profiles[8, 9, 16]. For this purpose, a pressure sensitive rubber (PSR - PCR Technical, Japan) is laminated on top of the parylene-passivated back-plane. The drain of each transistor is electrically connected to the PSR which is then grounded by an aluminum foil. The source and gate electrodes of the TFTs are used as the bit and word lines, respectively. PSR is near insulating (~30 Mohm) in its relaxed state. However, the resistivity decreases to < 0.5 ohm/pixel by applying an external pressure of ~6 kPa due to the shortened tunneling path between the conducting carbon nanoparticles in the PSR. Figure 4-5*a* shows the output characteristics of a single pixel upon applying a normal pressure to the device. The pixel response at an operating voltage of V_{DD} = -5 V is shown in Fig. 4-5*b*. In the linear operation regime, the sensor sensitivity, S = dG /dP, is ~30 μSkPa^{-1}, which is three-fold improvement compared with previous NW-based sensor[16] resulting from improved on-current of SWNT devices. In this e-skin layout, transistor channels and PSR are placed in series, but after a normal pressure of >6 kPa, the resistivity of PSR becomes negligible compared to the TFTs, thereby, resulting in the saturation of the pixel response. To show the functionality of the integrated e-skin, an "L"-shaped weight is placed on top of the sensor array with the normal pressure of ~15 kPa (Fig. 4-5*c*). The output conductance for each pixel is measured with the word and bit line voltages of V_{WL} = -5 V and V_{BL} = -1 V, and is plotted to show the measured two-dimensional pressure mapping (Fig. 4-5*d*). The enabled pressure mapping shown here demonstrates the utility of SWNT-TFT arrays for active-matrix backplane of sensor arrays on mechanically deformable substrates.

In conclusion, high performance TFT arrays with a hole mobility of 20-30 cm^2/Vs and respectable I_{ON}/I_{OFF} ~ 10^4 are uniformly obtained on large-scale plastic substrates by solution processing of semiconductor-enriched SWNT networks. This solution-based approach can be potentially combined with inkjet printing of metal contacts to achieve lithography-free fabrication of low-cost flexible and stretchable electronics with superb electrical and mechanical properties. Notably, to achieve stretchability using robust PI substrates, a concept often used in the paper decoration industry was applied by proper

laser cutting of the substrate. The back-plane technology explored here can be further expanded in the future by adding various sensor and/or other active device components to enable multifunctional artificial skins.

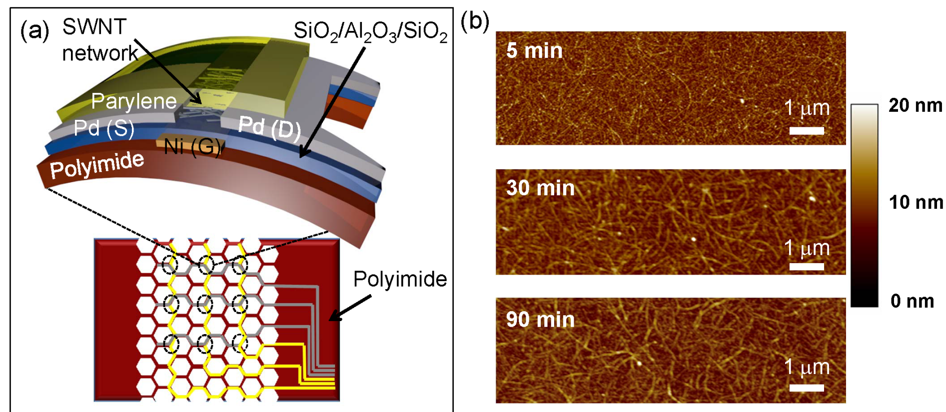

Figure 4-1. Semiconductor-enriched SWNT-TFTs on flexible substrates. ***(a)*** Schematic of a mechanically flexible/stretchable active-matrix back-plane (6×4 cm^2 with 12×18 pixel array) based on SWNT-TFTs, and an expanded schematic of a single TFT. ***(b)*** Atomic force microscopy images of SWNT networks on a PI substrate, showing that the density can be controlled by the nanotube deposition time (5, 30, and 90 min; top to bottom, respectively). Average length of nanotubes is ~ 0.8 μm.

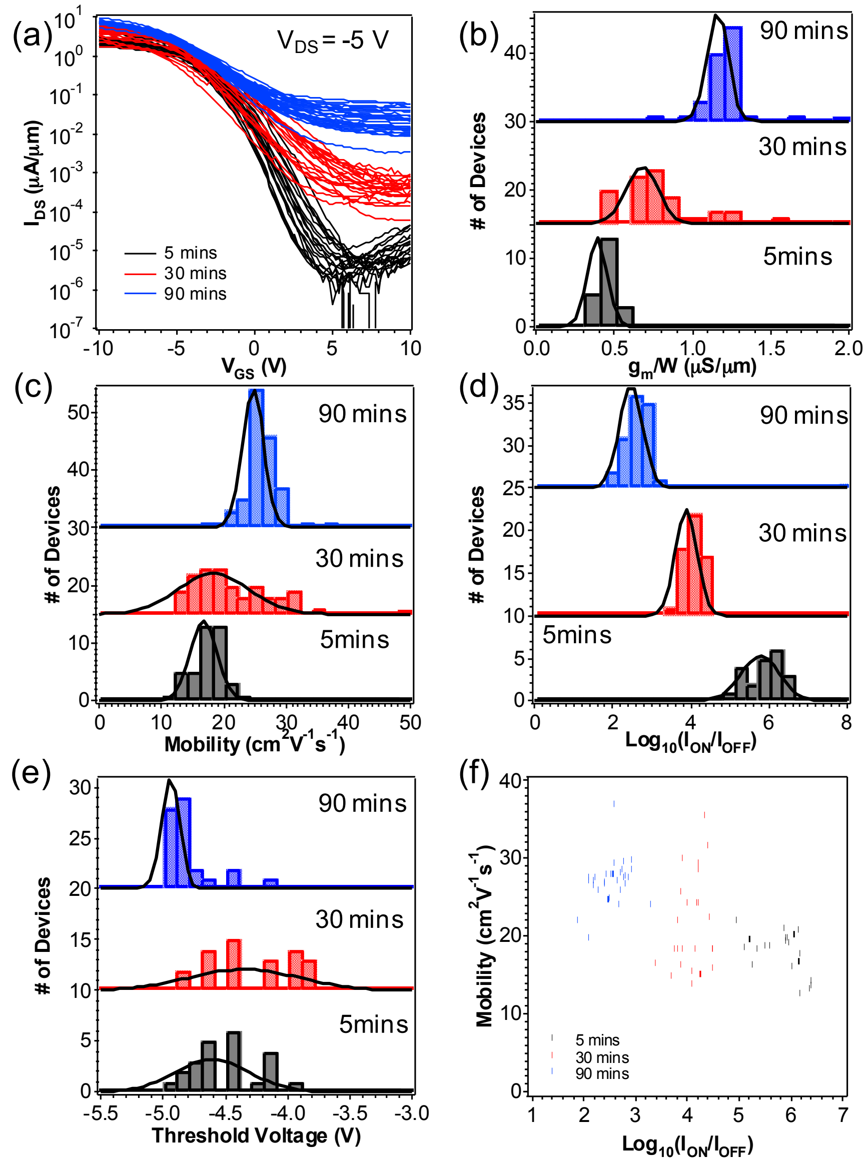

Figure 4-2. Statistical variation of the electrical properties over a 4-inch PI substrate. (***a***) Transfer characteristics of SWNT-TFTs at V_{DS} = -5 V for three different SWNT deposition times of 5, 30, and 90 min, corresponding to different nanotube densities. (***b***)-(***e***) Histograms of width-normalized transconductance, peak field-effect mobility, log-scale of I_{ON}/I_{OFF}, and threshold voltage for each deposition condition. In (***b***) and (***d***), the devices are measured at V_{DS} = - 5V, and in (***c***) and (***e***) the devices are measured at V_{DS} = -50 mV. (***d***) Peak field-effective mobility as a function of I_{ON}/I_{OFF} for various measured devices. Here, the channel length is ~3 μm and width is 250 μm.

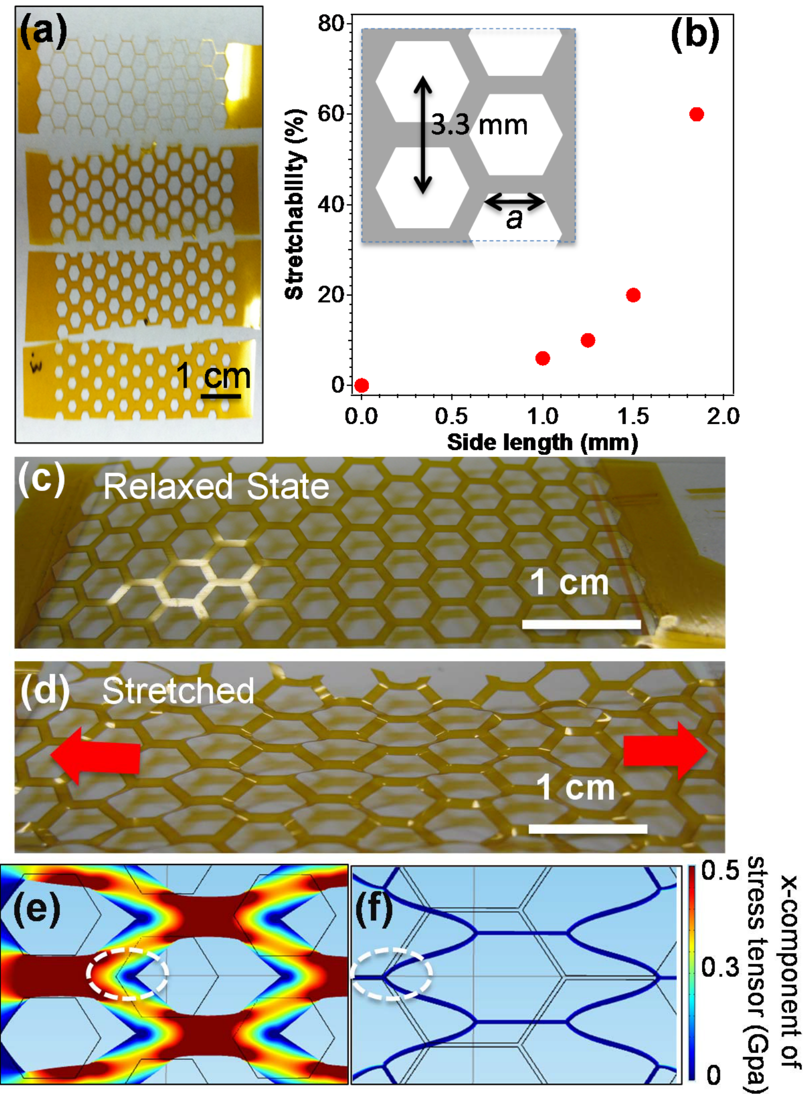

Figure 4-3. Stretchable PI substrates. ***(a)*** PI mesh substrate with four different side length of hexagonal holes (*a*=1, 1.25, 1.5 and 1.85 mm, from bottom to top). ***(b)*** Stretchability as a function of the side length, *a*, of the hexagonal holes. Here, the period of holes is fixed at 3.3 mm as shown in the inset. Optical images of ***(c)*** relaxed and ***(d)*** stretched state of the PI substrate with *a*= 1.25 mm. Mechanical simulation of ***(e)*** *a*=1.25 mm and ***(f)*** *a*=1.85 mm mesh, when the substrate is stretched by 2 mm in the horizontal direction. The location where the active devices are placed is marked with the white circle.

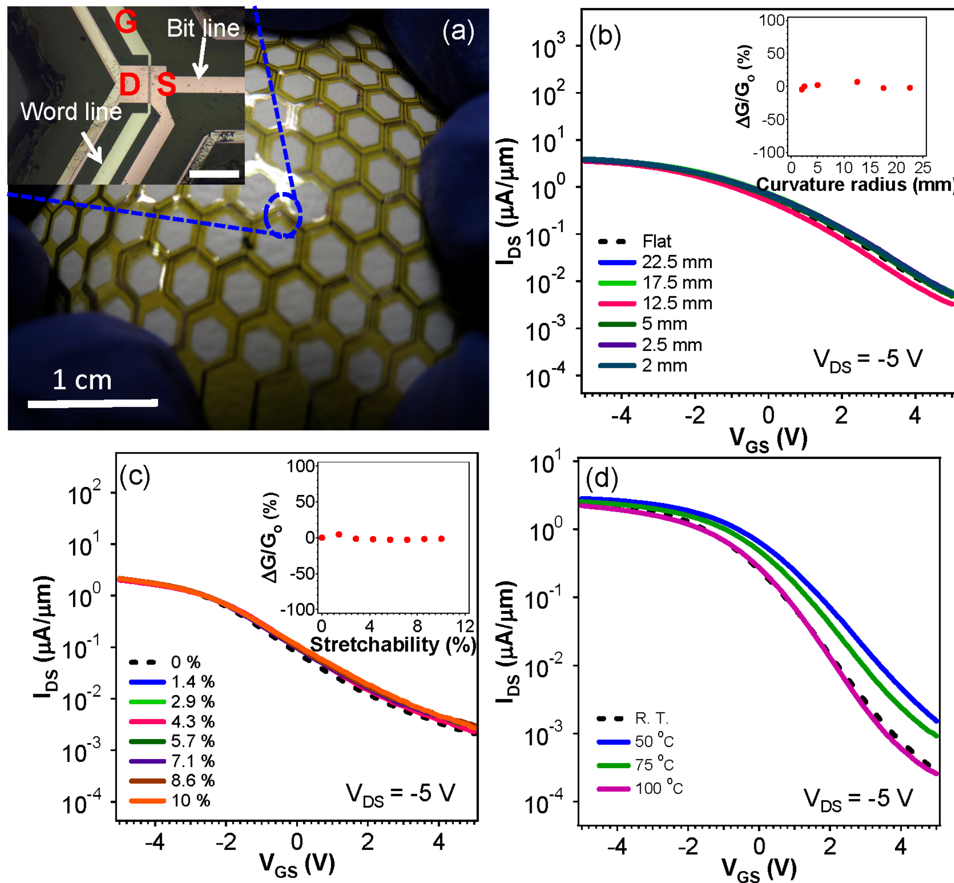

Figure 4-4. Mechanical robustness of SWNT-TFTs on honeycomb patterned PI substrates. ***(a)*** Optical images of a stretchable device array, showing conformal coverage on a baseball. Expanded image of an active device area (corresponding to the TFT for a single pixel) is shown in the inset (scale bar is 200 μm). Channel length and width are 5 μm and 200 μm, respectively. ***(b)*** Transfer characteristics at V_{DS} = -5 V measured at various bending radius. The inset depicts $\Delta G/G_0$ as a function of bending radius, showing minimal performance change even when bent down to 2 mm of bending radius. ***(c)*** Transfer characteristic at V_{DS} = -5 V as a function of stretchability. The inset shows $\Delta G/G_0$ as a function of stretchability. ***(d)*** Transfer characteristics at V_{DS}= -5 V as a function of temperature.

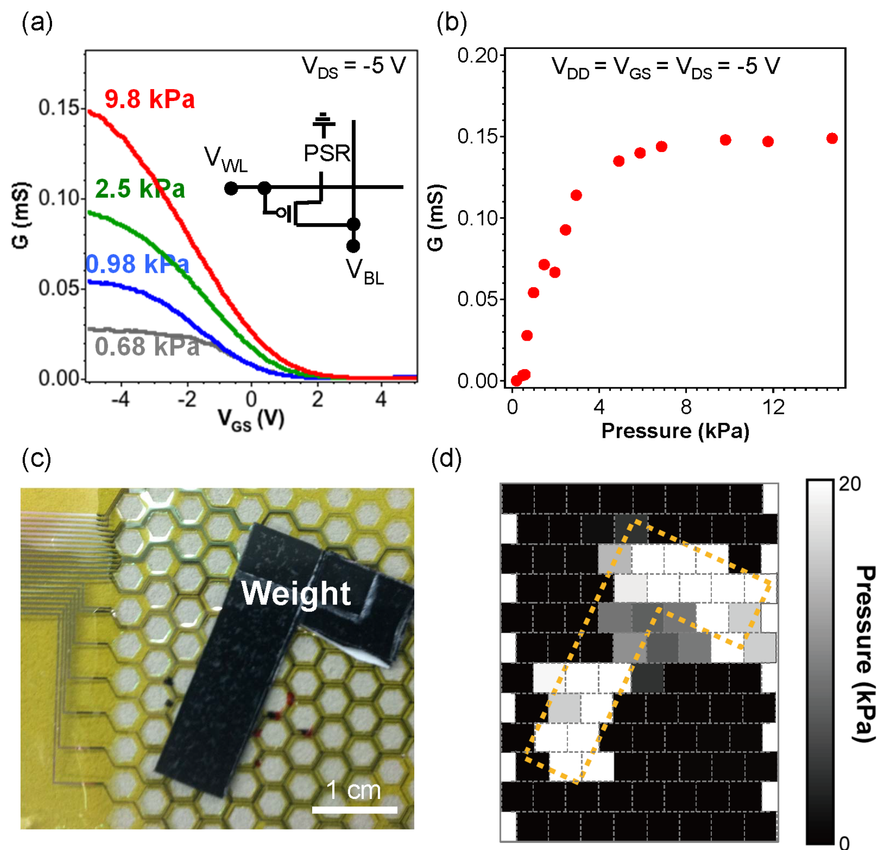

Figure 4-5. Artificial electronic-skin using SWNT-TFT active matrix back-plane. ***(a)*** Transfer characteristics as a function of the normal applied pressure for a representative pixel. ***(b)*** Output conductance at $V_{DD} = V_{GS} = V_{DS} =$ -5 V as a function of the applied normal pressure. ***(c)*** Optical image of a fully fabricated electrical skin sensor. An "L"-shaped object is placed on top. ***(d)*** The two-dimensional pressure mapping obtained from the 'L'-shaped object in (c).

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4.3 Light Interactive Electronic Skin for Visible Photon and X-ray Imaging[◊]

Recent advancements in the processing of electronically monodisperse carbon nanotubes have enabled the exploration of a wide range of functional devices based on random networks of nanotubes.[1, 2] In particular, thin film transistors (TFTs) using solution-processed semiconductor-enriched nanotubes have been demonstrated to exhibit excellent electrical properties with high uniformity on both rigid and flexible substrates.[3, 4, 5, 6, 7] High hole mobilites of up to 50 cm^2/Vs with high I_{on}/I_{off} of up to 10^6 have been reported for nanotube TFTs.[4] These reported performances clearly present an advantage over a-Si and organic semiconductor based devices which often exhibit mobilities that are lower by over two orders of magnitude as compared to those of nanotube networks. In addition, large-area processing of nanotube TFTs using inkjet and roll-to-plate processing have already been demonstrated.[8, 9, 10] Thereby, nanotube TFTs are particularly promising for low-power active matrix backplanes on a wide range of substrates, including mechanically flexible plastics. In this regard, nanotube active matrix backplanes have recently been successfully integrated with pressure sensors for the fabrication of electronic skins[3, 11] and organic light-emitting diodes for flexible displays.[11, 12] The high hole mobility of nanotube TFTs enables low voltage operation of the backplanes,[3, 4] which is important for enabling system-level, practical applications.

Here, we extend the use of nanotube backplanes for another major application domain involving large-area flexible imagers.[13, 14] We monolithically integrate organic photodetectors (OPDs) made of regioregular poly(3-hexylthiophene) (P3HT) and [6, 6]-phenyl C61-butyric acid methyl ester (PCBM) on top of a nanotube backplane consisting of an 18×18 pixel arrays (physical size is 2 cm by 1.5 cm). The absorption spectrum of P3HT:PCBM bulk-heterojunction photodetectors is optimal for visible light imaging applications.[15] Furthermore, by integrating a Gd_2O_2S:Tb (GOS) [16] scintillator film on top of the imager, a mechanically flexible X-ray detector[17] is demonstrated. In this system, the scintillator film converts incident X-rays into visible photons with an energy of ~3 eV matching the peak absorption wavelength of the OPDs. The enabled devices exhibit high performance in terms of imaging sensitivity, response time, and uniformity. This work presents a practical platform for a new form of flexible sensor networks for large-area imaging applications.

Fabrication procedure for our imagers is briefly described in Fig. 1a. First, polyimide (PI; thickness of ~24 μm) is spin-coated on a Si supporting wafer, followed by curing on a hotplate at 300 ^{o}C for 1h.[3] After insertion of SiO_x thin film (~10 nm), Ni gate (G) electrodes are then fabricated using photolithography, evaporation, and lift-off. Atomic layer deposition of Al_2O_3 (~70 nm) sandwiched between evaporated SiO_x (~ 10 nm) layers is performed to serve as the gate dielectric layer. Next, 99% semiconductor-

[◊] The work presented here will be submitted for publication in a similar form in the near future.

enriched single-walled carbon nanotube (SWNT) solution (NanoIntegris, Inc) is drop-casted on a poly-L-lysine functionalized surface,[3] followed by Ti (0.5 nm)/Pd (40 nm) source/drain (S/D) electrode formation by photolithography and metallization. Subsequently, O_2 plasma (60W, 2min) treatment is performed to burn out nanotube films outside the active regions. Next, indium tin oxide (ITO) pads (thickness of ~80 nm) are deposited using sputtering to serve as the anode of the subsequently fabricated photodiodes. Each ITO pad is in electrical contact with the drain electrode of the corresponding TFTs. A photoresist (S1818, ~2μm) layer is then spin-coated to encapsulate SWNT TFTs with only the ITO regions exposed (Fig. 1b). The sample is baked on a hotplate at 200 ^{o}C for 30 min to enhance ITO performance as well as hardening the photoresist in order to not be dissolved in organic solvents in the subsequent process steps. Next, a ~9 nm thick MoO_3 hole transportation layer[18, 19] is thermally evaporated after cleaning the ITO surface with ozone treatment. The organic semiconductor film (80 mg/ml mixture of P3HT and PCBM with the weight ratio of 1:1 in chlorobenzene) is spin-coated at 1000 rpm for 30s.[20] The film thickness is ~500 nm. Finally, Al is evaporated through a shadow mask to form the cathode electrode, followed by a thermal anneal at 150 ^{o}C for 10min in order to form a bicontinuous heterojunction network in the organic semiconductor film.[21] The PI substrate with the TFTs and photodiodes on top is then mechanically peeled off from the supporting Si substrate to form mechanically flexible imagers. The optical image of the fully fabricated device bent to a curvature radius of ~5 mm is shown in Fig. 1c.

We first studied the electrical characteristics of individual nanotube TFTs (L~ 30 μm, W~ 2000 μm) and organic photodiodes on a flexible PI substrate. The channel width normalized transfer (I_{DS}/W-V_{GS}) and transconductance (g_m/W-V_{GS}) characteristics from a representative TFT measured at V_{DS}= 0.1 V are shown in Fig. 2a. As previously reported[3, 4, 5, 7], solution-based nanotube processing produces uniform device characteristics in terms of on-current (I_{ON}), transconductane (g_m), on/off ratio (I_{ON}/I_{OFF}), threshold voltage (V_{th}), and mobility (μ). The extracted I_{ON}/W and peak g_m/W are ~8×10^{-2} [μA/μm] and ~4.5×10^{-3} [μS/μm], respectively. Using extracted peak transconductance, the field effect mobility is calculated as $\mu = (L / V_{DS}C_{ox})(g_m / W)$, where the parallel plate model is used to calculate the gate oxide capacitance, C_{ox}=6.43×10^{-8} [F/cm^2]. The calculated mobility is ~ 20 cm^2/Vs, which is comparable to previously reported values, although this value is underestimated (by ~2×) due to the overestimation of the gate capacitance since the entire surface is not covered by SWNTs.[4] More rigorous C-V analysis is required to extract actual value as performed in our previous study.[4] The output characteristics measured at V_{GS}= -5 to 5 V in 1V steps of a representative TFT is shown in Fig. 2b, exhibiting clear metal-oxide-semiconductor field-effect transistor (MOSFET)-like behavior. In this work, we are interested in developing large-area sensor networks with the size of the system being on the cm scale. In this regard, device performance uniformity is essential. To examine the uniformity, 20 TFTs are randomly chosen across the substrate, and the histogram of calculated mobility and threshold voltage measured at V_{DS}= 0.1V are shown in Fig. 2c. The average mobility and threshold voltage is 17.4 ±2.2 cm^{2}V^{-1}s^{-1} and -0.03±0.22 V, respectively. This uniformity is sufficient for the fabrication of an imager which is discussed later in this manuscript.

Optical characteristics of standalone organic photodiodes on flexible substrates are also characterized. Here, the light is illuminated from the back-side; through the PI substrate. Figure 2d shows *I-V* characteristics measured under dark and 1-sun illumination conditions. For imaging applications, it is important to obtain high light sensitivity as well as low dark current under the reverse bias condition. As previously reported in the literature[22, 23], by insertion of the MoO_3 layer as the hole transportation layer, photo-induced current is maximized without degrading dark current under reverse bias condition. Furthermore, high device stability to ambient air up to 14 days is observed even without any encapsulation layer (Fig. 2d).[24] The dark current at a reverse bias voltage of -1 V is ~ 100 nA/cm^2, which is close to the state-of-the-art OPDs reported in literature (~10 nA/cm^2).[25] To further lower the dark current, thickness engineering and device structure optimization, such as adding an electron transport layer on the cathode side, are needed.[26] Nevertheless, the reverse bias current is low enough for the current proof-of-concept demonstration, with light (1-sun) to dark current ratio of ~10^5 at -1 V (Fig. 2d).

External quantum efficiency (*EQE*) was measured for the generated photocurrent in the wavelength range of 300 – 750 nm as shown in Fig. 2e. A photodiode fabricated using the same process but on a glass substrate (instead of PI) is also added as a reference. The light absorption by the PI film occurs at wavelengths of <400 nm, which does not significantly affect visible light photoresponse of the diodes. The peak *EQE* is observed at ~ 580 nm, which matches well with the emission spectrum of the GOS for eventual X-ray imaging applications as discussed later in this paper. Figure 2f shows the photocurrent response at a reverse bias of 2 V to incident light (λ=535 nm, 500 μW/cm^2) chopped at 42 Hz. The response is characterized by a rise time, τ_r ~ 1 ms and a decay time, τ_d ~1 ms, which are compatible to other reported organic photodiodes on flexible substrates.[25]

Next, organic photodiodes are integrated with SWNT TFTs backplane to form 18 by 18 pixel arrays (physical size is 2 cm by 1.5 cm). Each pixel is composed of one organic photodiode in series with a nanotube TFT, and the word line (V_{WL}) and bit line (V_{BL}) voltages are applied to address each pixel. The cross sectional schematic of one pixel is shown in Fig. 3a with the corresponding circuit diagram shown in the inset of Fig. 3b. The integrated pixel response is characterized by measuring the current between the cathode of the photodiode and the source of the SWNT TFT at V_{BL}= -2 V as a function of V_{WL} (i.e., gate voltage of the TFT). Here, the wavelength of the incident light is λ=535 nm and the intensity is varied from 0-1500 μW/cm^2 (Fig. 3b). Strong photoresponse is clearly observed for V_{GS}<0 V, corresponding to the ON-state of the TFTs. The dark current of photodiode limits the overall current flow of the pixel, which is needed for proper operation. The log-log plot of current at V_{BL}= -2 V and V_{WL}= -5 V as a function of incident light intensity is plotted in Fig. 3c. Clearly, a linear-response is observed with a slope of ~0.15 μA/μW, corresponding to the sensitivity of the sensor. This linear response is highly desirable for the practical use of the sensors. The sensitivity value of our devices is within ~2× of the best value reported in the literature for OPDs.[27] The lowest detectable light intensity is ~ 10 μW/cm^2, corresponding to ~100 nA/cm^2 which is limited by the OPD dark current.

To demonstrate the imaging functionality of the pixel array (Fig. 4a), the device is exposed to an incident light with λ=535 nm and intensity of ~100 μW/cm^2 through a "T"-shaped shadow mask (Fig. 4b). The current of each pixel is measured by applying V_{BL}= -2 V and V_{WL}= -5 V, while the rest of pixels are turned off by applying V_{WL}= 5 V. As depicted in Fig. 4c, the irradiated light profile is successfully obtained by electronic readout. The yield of functional pixels is ~ 90 % with the defective pixels mainly caused by fabrication failure such as poor lift-off of S/D or G electrodes. This high yield indicates that the lab-scale process scheme used here for both nanotube TFTs and organic photodiodes is not only scalable but also reliable. The pixel size used in this work is set to ~ 1 mm^2. This reduces the total number of pixels, thereby, simplifying the measurement. In the future, higher resolution is easily attainable by reducing the pixel dimensions down to the photolithography limit (i.e., µm scale).

The fabricated imager can also be readily used for x-ray imaging by laminating a scintillator film on the substrate (facing the incident X-ray) as shown in Fig. 5a. In this indirect X-ray detection approach, a GOS scintillator film is used to convert X-ray photons into green light with an emission peak of ~545 nm,[16] which is then detected by the photodiodes in the imager. The cross sectional schematic of a single pixel is shown in Fig. 5b. As discussed in Fig. 2e, the peak *EQE* of P3HT:PCBM photodiodes perfectly matches the green fluorescence emission at 545 nm of the GOS film. Figure 5c is a log-log plot of measured current of a single pixel as a function of incident X-ray dose rate, showing a linear correlation down to ~10 mGys^{-1} (corresponding to a photocurrent of ~200 nA/cm^2). This is close to the resolution limit set by the dark current of our photodiodes. Further improvement in photodiode quality as mentioned above would make the pixel response to lower dose rates feasible. With the protection of the GOS film, the pixels remain stable after exposure to X-ray source. Experimentally, we observed both dark and photo currents are nearly unchanged after exposure to ~300 Gy, which was the maximum total dose tested in the measurements. Finally, spatial mapping is performed by using a dose rate of ~100 mGys^{-1} generated by a circle-shaped (~4mm in diameter) X-ray source (20 keV). The spatial profiling of the incident X-ray is electrically resolved using the fabricated imager (Fig. 5d). The results demonstrate the utility of this flexible system as a light-weight and portable X-ray imager that can readily be wrapped around body parts for future medical imaging applications.

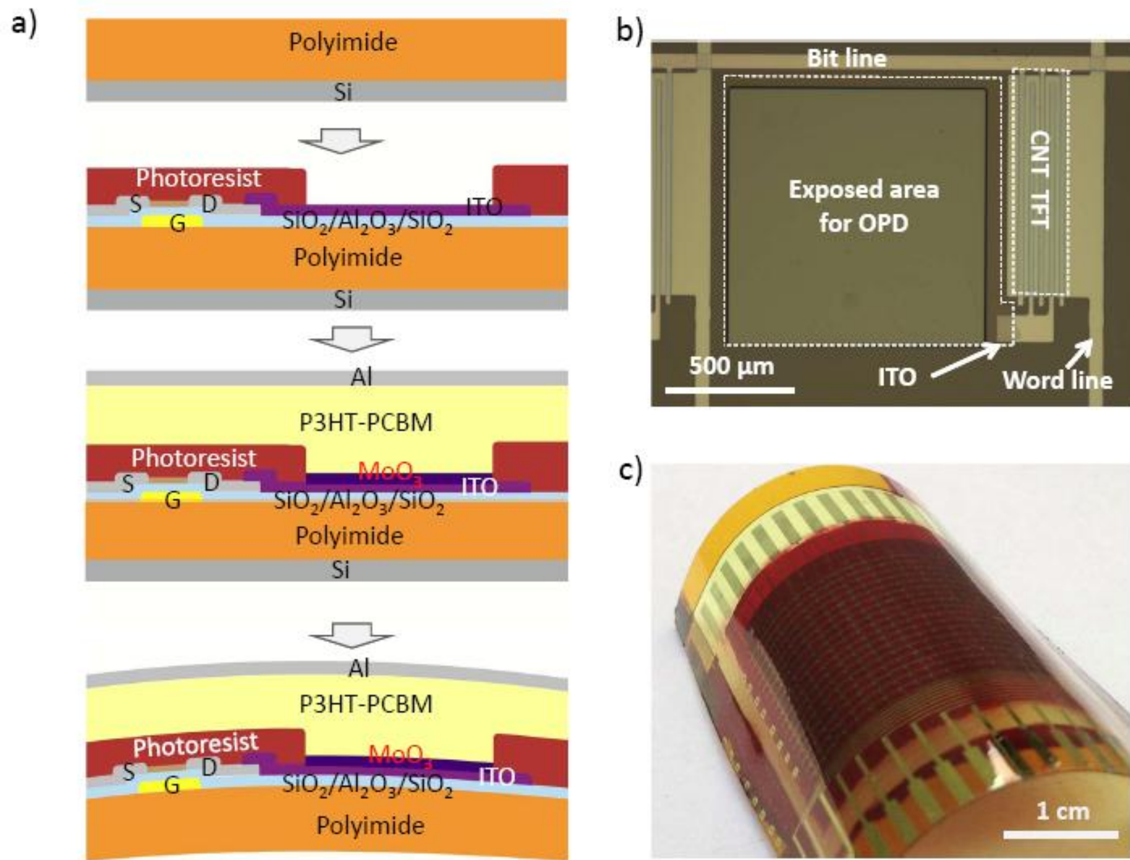

Figure 4-6. Fabrication of mechanically flexible imagers. **(a)** Step-by-step fabrication process flow. **(b)** Optical image of a single pixel after the completion of the nanotube TFT process. **(c)** Optical image of a fully fabricated imager bent to a curvature of radius of ~5 mm.

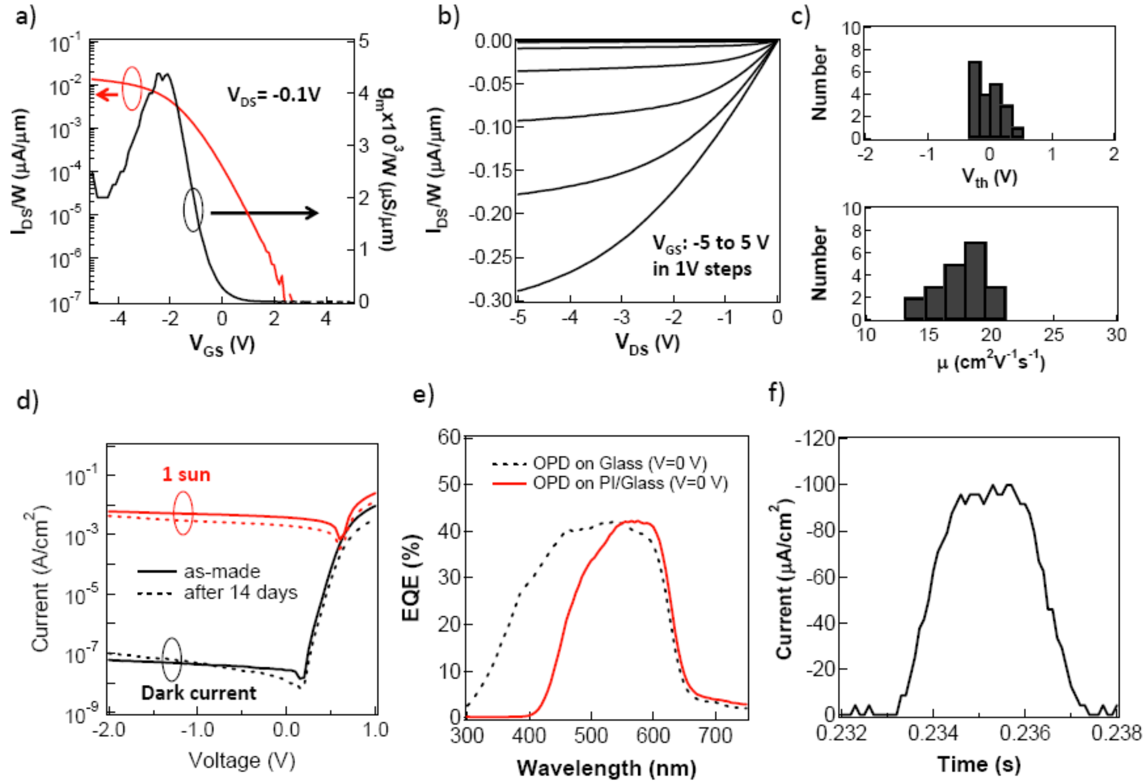

Figure 4-7. Electrical and optical characteristics of stand-alone TFTs and OPDs. **(a)** Channel width normalized drain current vs. gate voltage characteristic at a drain voltage of -0.1 V. The corresponding transconductance as a function of gate voltage is also shown. Channel length and width are 30 μm and 2000 μm, respectively. **(b)** I_D-V_{DS} characteristics for applied gate voltages of -5 V to 5V in 1V steps. **(c)** Histograms of mobility and threshold voltage for 20 randomly chosen TFTs across the substrate. **(d)** Current – voltage characteristics of an organic photodiode measured under 1-sun and dark condition (solid lines). Same device is measured again after exposure to ambient atmosphere for 14 days (dashed lines). **(e)** External quantum efficiency between 300 nm and 750 nm for an organic photodiode on PI (red line) and glass (black dashed line) substrates. **(f)** Time response of the photocurrent at a reverse bias of 2V for an incident light with λ=535 nm and intensity of 500 μW/cm^2. The light is chopped at 42 Hz.

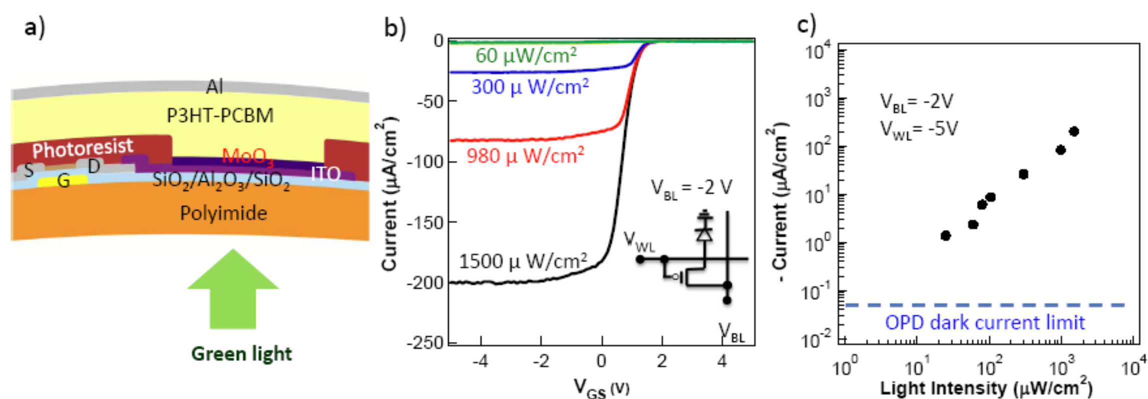

Figure 4-8. Characterization of individual pixels. **(a)** Cross-sectional schematic of a single pixel. Light is exposed from the PI side. **(b)** Transfer characteristics of one pixel under various light intensities (λ=535 nm). The inset shows the circuit schematic of a pixel. **(c)** Photocurrent response of a pixel at V_{GS}=-5V and V_{BL}=-2V as a function of incident light intensity.

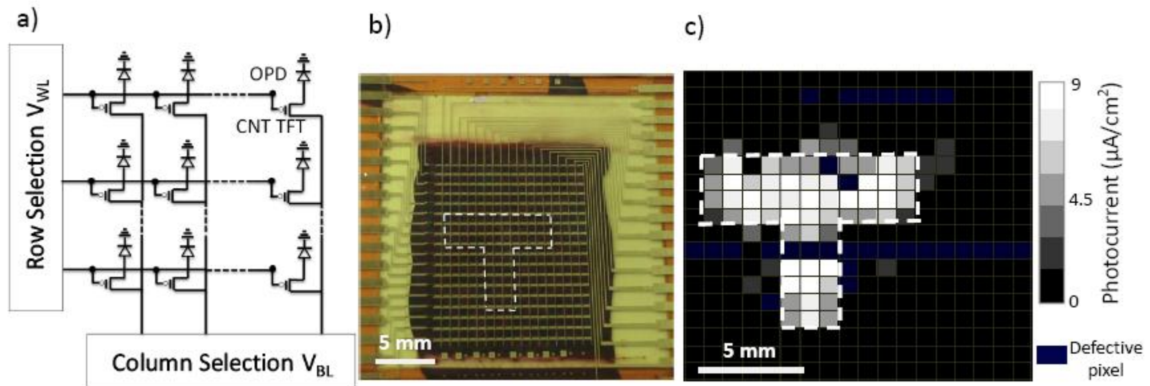

Figure 4-9. Flexible visible light imagers. **(a)** Circuit schematic of the imager. **(b)** Optical photograph of a fully-fabricated imager (18 by 18 pixels). The imager is exposed to light with an intensity of 100 μW/cm^2 and λ=535 nm through a "T"-shaped shadow mask (shadow mask is not shown here). **(c)** The corresponding two-dimensional intensity profile obtained by measuring the photocurrent of the pixels. The character "T" is readily imaged by the device.

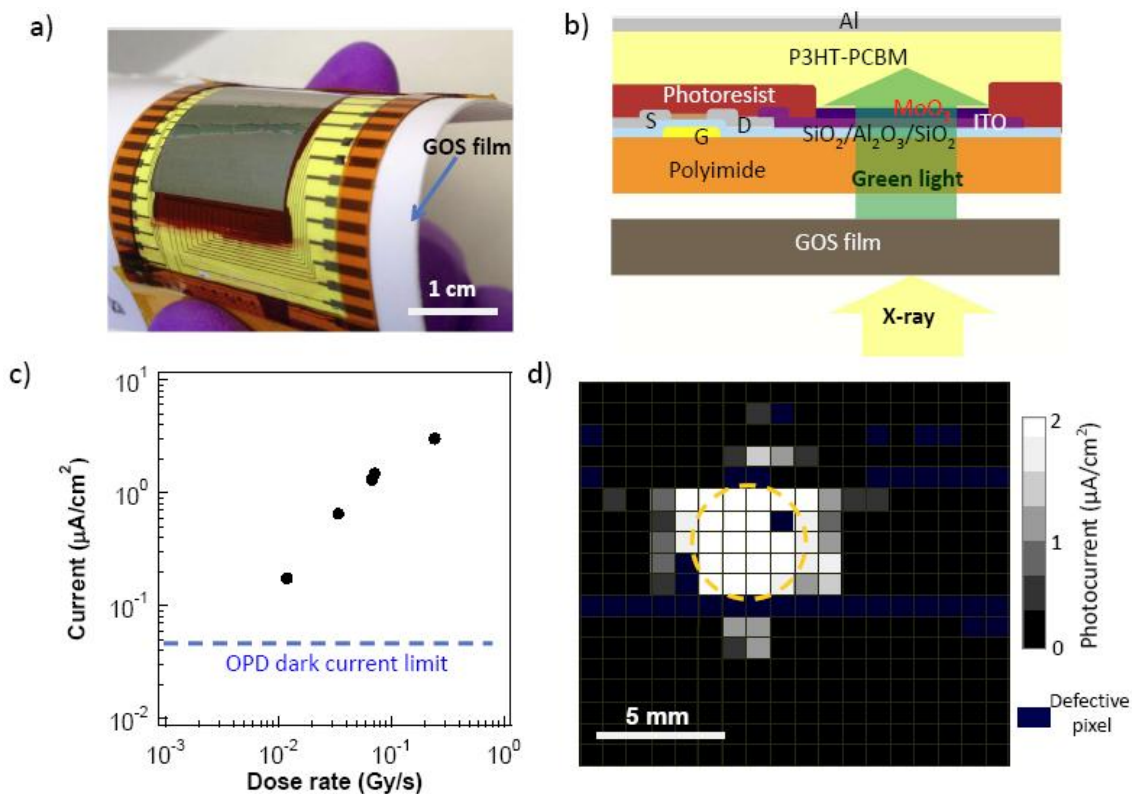

Figure 4-10. Flexible X-ray imagers. **(a)** Optical photograph of an imager placed on top of a GOS film used for X-ray detection. **(b)** Cross-sectional schematic of one pixel. X-rays are irradiated onto the GOS film, and emitted green light is detected by the OPDs of each pixel. **(c)** Measured current from one pixel at a reverse bias of 2V as a function of X-ray dose rate. **(d)** Spatial mapping when a circle-shaped (diameter of 2 mm) X-ray source is projected with a dose rate of 100 mGy/s.

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Chapter 5
Conclusion

5.1 Summary

In the past decade, there has been a tremendous research about 'bottom-up' synthetic nano materials, especially one-dimensional and quasi-one-dimensional nanomaterials because they offer their size-related intriguing physical properties and possess potential as building blocks in nanoelectronics. Although some progress has been reported, however, there is still huge barrier to be overcome before we use them in practical applications. In this thesis, aiming to use these nanomaterials in practical applications, we have decided to use them not for 'nano'electronics, but for 'macro'scale flexible electronics use by assembling them on polymer substrate in the form of either arrays or networks. With this, stochastic device-to-device variation has been drastically reduced, opening more realistic path towards to actual devices.

In Chapter 2, scalable low-temperature assembly approaches for nanomaterials have been discussed. For semiconducting NWs, simple but versatile contact printing approach is utilized to achieve highly aligned array of NWs. Furthermore, patterned assembly is realized by combining with surface chemistry. For semiconducting carbon nanotubes, commercially available separated solution is simply drop casted on the surface, and highly uniform assembly is realized.

In Chapter 3, electrical and optical characteristics of discrete single TFT with assembled InAs NW arrays and spatially composition graded CdS_xSe_{1-x} NW arrays are characterized. With simple contact printing of InAs NWs, highly dense arrays (~ 4 NW/μm) are obtained on flexible substrate, and InAs NW TFTs with channel length of 1.5 μm on flexible substrate exhibits GHz operation (cutoff frequency, f_t ~ 1 GHz and maximum frequency of oscillation, f_{max} ~ 1.8 GHz). Furthermore, by contact printing of spatially composition graded CdS_xSe_{1-x} NWs, which results from unique nanowire growth, an array of tunable-wavelength photodetectors is demonstrated, otherwise impossible to achieved using conventional epitaxial growth technique due to lattice mismatch.

In Chapter 4, to demonstrate the utility of thus-established processing scheme of nanomaterials over large scale flexible substrate, *cm* scale integrated flexible electronic skin (e-skin) is fabricated by combining various sensor components with SWNT TFT-based active matrix backplane. Pressure sensitive rubber or organic photodiode is chosen as pressure and light interactive sensor, respectively, and spatial mapping of touch (pressure mapping) and light interaction is achieved.

5.2 Contributions of this work

In this dissertation, practical applications of nanomaterials for macro-scale flexible electronics have been proposed and discussed, ranging from the assembly to actual demonstration.

First, a scalable low temperature assembly approach has been established for NWs and SWNTs. Using simple 'contact printing' approach with proper surface modification, highly dense and aligned NW arrays are selectively assembled at desired location on virtually any substrate. And with drop-cast of commercially available semiconductor enriched SWNT solutions, quite uniform assembly of SWNT network is achieved.

Secondly, it has been demonstrated that with thus-assembled nanomaterials, superior electrical characteristics (GHz operation of InAs NW arrays on flexible substrate) and unique optical characteristics (tunable-wavelength photodetectors using CdS_xSe_{1-x} NWs) are achieved.

Lastly, to demonstrate actual utility of nanomaterials, *cm*-scale flexible electronic skin (e-skin) is fabricated by combining various sensor components with SWNT-based active matrix backplanes.

5.3 Future Directions

There have been several topics to be covered in the future in order to further improve e-skin concept established in this work, ranging from materials/processing improvement to applications design.

Firstly, more rigorous control of electrical properties such as threshold voltage or subthreshold characteristics of SWNT TFTs has to be established in order to construct more sophisticated integrated circuit. To achieve this, more precise chirality specific nanotube separation is needed.

Next, off-current of SWNT TFTs has to be further lowered as off-current sets the detectable limit for light interactive sensor as discussed in chapter 4-3. This problem should be tackled either by using more highly separated nanotube solution (~ 99.9%) or by exploring better deposition approach to avoid bundling of nanotubes.

Furthermore, establishing reliable and scalable processing technique for n-type TFTs is another important research topic to be addressed.

For application point view, human interactive multi-functional e-skin should be readily achieved by adding various sensor components on the active matrix backplane. In

this dissertation, e-skin with only one sensor component is described, but by having multi sensor elements, more sophisticated e-skin will be achieved.

Appendix A:
Supporting information of monolayer resist for patterned contact printing (2.1.3)

Nanowire growth

Si and Ge NWs were synthesized by gold nanoparticle mediated vapor-liquid-solid process. Monodispersed gold nanoparticles with diameter, d=30 nm (Ted Pella, Inc.) were deposited on Si/SiO_2 (50nm, thermally grown) substrates, followed by the chemical vapor deposition growth. *p*-type Si NWs were grown at 460 ^oC and 30 torr under a constant flow of silane (4 s.c.c.m), hydrogen (4 s.c.c.m), and diborane (0.01 % diluted in H_2, 5 s.c.c.m) for 15 minutes, resulting ~120 μm long NWs. For *p*-type Ge NWs, germane (10% diluted in H_2, 10 s.c.c.m.), diborane (0.01 % diluted in H_2, 5 s.c.c.m), and H_2 (90 s.c.c.m) were used at 270 ºC and 700 torr, resulting in a growth rate of ~ 1 μm/min.

Surface functionalization of receiver substrate

Fluorination of SiO_2 surfaces was carried out by the well established siloxane-based condensation chemistry using (heptadecafluoro-1,1,2,2-tetrahydrodecyl) dimethylchlorosilane (Gelest, Inc.). A solution of ~0.5 vol% of the above compound was prepared with hexane as the solvent. Si/SiO_2 substrates were then treated in the solution for 45 min, followed by a thorough wash with the solvent and baking in an oven at 120ºC for 20 min, resulting in a highly uniform fluorinated monolayer on the SiO_2 surface.

Monolayer patterning with very ultraviolet (VUV) exposure

We used a Xe-filled dielectric barrier discharge excimer lamp with an emission wavelength of 172 nm as the light source to pattern the above described fluorinated monolayer. The samples were irradiated with VUV through a shadow mask in contact with the sample surface. During the irradiation, the chamber was kept at 10^5 or 3 Pa ambient air, corresponding to $\sim 2\times 10^4$ and 0.6 Pa oxygen partial pressure, respectively. VUV exposure is extensively attenuated due to the absorbance of oxygen molecules in air, so the distance between the light source and sample surface was kept to be less than 5 mm.

Nanowire printing

The surface modified receiver substrate was mounted on a fixed stage. The growth substrate (i.e. donor substrate) with a dense lawn of NWs was cut into the desired size and attached to a metal weight (chosen to result in a pressure of~ 10 g/cm^2). After a few drops of lubricant (Octane: mineral oil, 2:1 v:v), the donor chip along with the weight was gently contacted with the receiver substrate. Donor chip was then pushed by a micromanipulator with a constant velocity of ~20 mm/min in the direction of the VUV-irradiated patterns. After sliding for a few mm, a second weight was added to the donor chip to increase the total pressure to~54 g/cm^2 while keeping the same velocity of ~20 mm/min. This procedure enables us to avoid mechanical "stamping" of NWs when the donor is initially contacted with the receiver substrate. After the donor chip was passed over the entire receiver substrate, the donor chip was gently removed and the receiver substrate was rinsed with octane. SEM images of the donor substrate before and after the printing process is shown in Figure A-1, clearly demonstrating that NWs on the donor substrate are effectively combed by the shear force, before getting transferred to the receiver substrate. Assuming a NW density of ~5 NW/µm^2 on the donor substrate and a density of ~50 NW/100 µm^2 on the receiver substrate, we estimate that only ~10% of the NWs are transferred during the contact printing process when the donor and the receiver substrates have the same surface area. The printing process is generic for a wide range of receiver substrates, such as flexible Kapton, glass, and Si/SiO_2, as long as the surface roughness is on order of a few nm or less, and the appropriate surface chemistry is utilized[i].

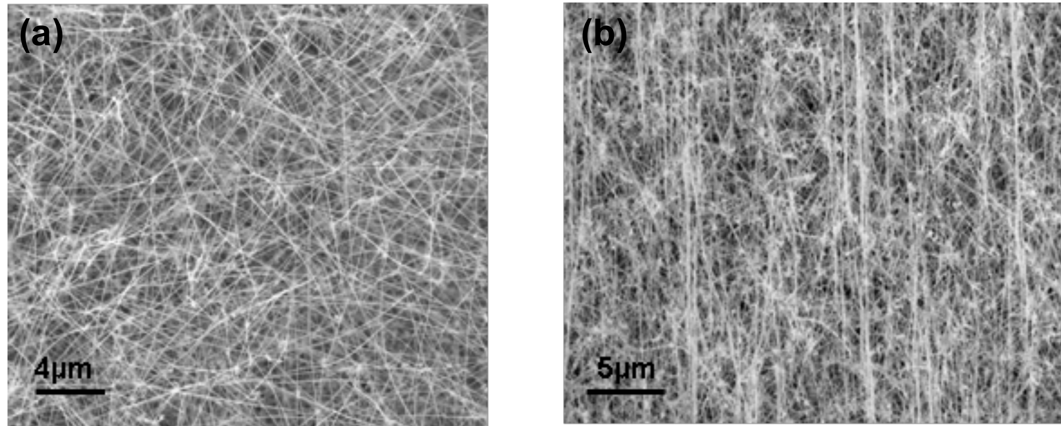

Figure A-1. Top-view SEM images of the Ge NWs on the donor substrate (a) prior and (b) after the contact printing process.

Nanowire array device fabrication and characterization

For the electrical measurements, a heavily B doped Si substrate was used as a global back-gate. Source/drain electrodes were patterned with photolithography (Karl Suss MA6 Mask Aligner), followed by Co electron-beam evaporation (~50 nm thick), and lift-off. The spacing between source and drain electrodes is ~3 µm. The sample was then annealed at 300 ^oC for 30s. After this thermal treatment, the electrical transport

properties of the devices were investigated with a probe station system (Signatone) and semiconductor parameter analyzer (Agilent 4155C) at room temperature. It should be noted that during the fabrication, we avoided using ultrasonication (for instance, during the lift-off steps) as doing so results in the gradual removal of the NWs from the substrate. By using the above fabrication procedure, the density of the assembled NWs (for the diameter range explored in this study) remains the same after the device fabrication steps, clearly indicating the strong adhesion of the NWs to the receiver substrate for fabrication processing purposes. Additionally, we have done the simple Scotch tape test in which a removable tape is gently brought in contact to the surface of the substrate and then removed. We did not observe any noticeable change in the NW density after this test (Fig. A-2).

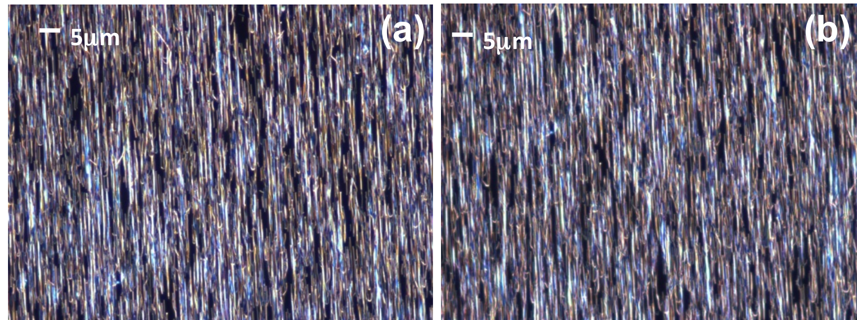

Figure A-2. Dark-field optical images of the assembled GeNW arrays (a) before and (b) after the Scotch tape test, showing no noticeable change in the density of the assembled NWs.

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[i] R. Yerushalmi, Z. A. Jacobson, J. C. Ho, Z. Fan, A. Javey, *Appl. Phys. Lett.* 2007, 91, 203104.

Appendix B:
Supporting information of "InAs nanowire parallel arrays radio frequency devices" (3.3)

Supporting Information

Mechanical bending of parallel array InAs NW FETs

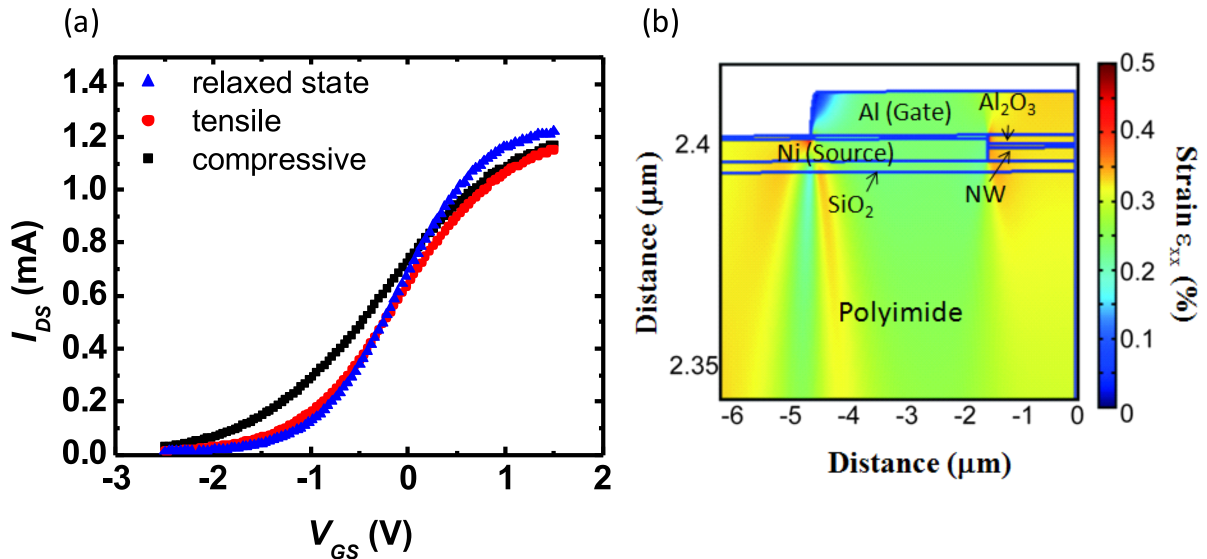

Figure B-1. Mechanical bendability of NW-array FETs. a) Transfer characteristics of an InAs NW-array FET with W = 200 μm measured at V_{DS} = 1V as a function of the imposed bending condition. The device is first measured at the relaxed state, (bending radius, r = infinity), and under a tensile and compressive strain (r = 18 mm) conditions. b) Mechanical simulation of the strain for a NW device when bent to 18 mm curvature radius. Only half of the device is shown, depicting the various layers and their strain.

Short-open-load-thru (SOLT) calibration method

Electrical cables and probes are used to connect a vector network analyzer (VNA) ports to on-chip pads in order to measure a DUT (device under test). The raw data measured by the VNA is not accurate and contains the added parasitic effects of the cables/connectors and probes at the input and output. To de-embed the effect of these interconnections and calibrate the setup down to probe-tips, firstly a known set of terminations are measured (standard impedance substrate). By measuring these terminations in different configurations, the added parasitic effects of the cable/connectors and probes are obtained and subtracted from the raw measured data and hence the calibrated data, which is only due to the DUT and not the interconnections, is extracted.

On-wafer pad-open and pad-short for de-embedding pad parasitics

Calibration of the setup through the SOLT procedure (explained above) removes all the off-chip interconnection effects and yields to the measured data of the on-chip structures, which includes input/output pads and the transistor. Since we are only interested in the inherent characteristic of the transistor, the effects of the input/output pads should be removed. One approach is to repeat the SOLT procedure with pad-open, pad-short, pad-loaded, pads-thru structures and de-embed the added parasitic effects of the pads. Since fabricating an accurate and broadband on-chip 50-ohm termination and transmission lines are challenging, and furthermore, since the total structure is small relative to the wavelength of interest, we use a lumped element pad-open and pad-short configurations to de-embed the pad effects. Pad-open gives the shunt capacitance and its associated conductance of the pad structure, and pad-short gives the series inductance and resistance of the pad/interconnect. Pad-only structures in open and short configurations were placed on the same die. These parasitic effects were then subtracted from the total pad and transistor structure, and the S-parameters of the intrinsic transistor were obtained. In Figure 3-6, the measured current gain (h_{21}), the maximum stable gain (MSG), and maximum unilateral gain (U) before and after de-embedding are shown.

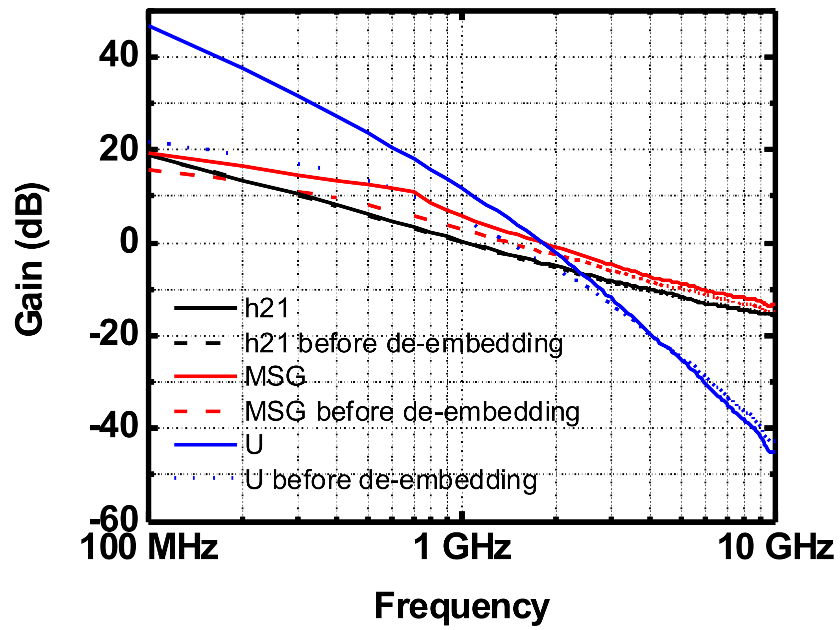

Figure B-2. The effect of de-embedding on the measured current gain (h_{21}), Maximum stable gain (MSG), and maximum unilateral gain (U).

Extraction of h_{21}, MSG and U from the S-parameters

S-parameters can be converted to h-parameters and hence h_{21} can be plotted, so f_t (which is the frequency where h_{21}=1=0 dB) can be directly extracted. Maximum stable gain (MSG) is the theoretical gain a transistor can provide if suitable lossless input and output matching networks are incorporated, and is extracted as following with the stability factor K > 1 at all measured frequencies:

$$MSG = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

Maximum unilateral gain (U, Mason gain) is the maximum unilateral power gain the device can provide and is calculated from Y or Z (admittance or impedance) parameters as following

$$U = \frac{|Y_{21} - Y_{12}|^2}{4\times(Re[Y_{11}]\times Re[Y_{22}] - Re[Y_{12}]\times Re[Y_{21}])}$$

The maximum power gain of a device is defined as the power gain delivered by a device when both input and output ports are matched to the impedance of the source and load, respectively. For a MOS device f_{max} is approximately given as: $f_{max} \approx \frac{f_t}{8\pi R_G C_{GD} f^2}$. As can be seen from this equation, f_{max} vs frequency, f, has a relation of $f_{max} \sim 1/f^2$, or f_{max} drops by 20 dB/decade as frequency increases. In this equation, the frequency effects up to the second order are considered and higher order effects are neglected. As the frequency approaches the device functionality limit, however, f_{max} drops faster than 20 dB/decade with the frequency increment. This is the reason why the experimentally obtained f_{max} is ~1.8 GHz and not 2 GHz, in spite of having 6 dB of MSG at 1 GHz.

Hybrid-π model

Transistors are nonlinear devices (nonlinear output (i_d)/input (v_g) characteristics). To design an amplifier, suitable gate and drain voltages with respect to the source should be applied to the transistor to bias it at a desired operating point. After biasing, we assume the input voltage applied to the gate is small and hence the device can be assumed linear with respect to that. Hence we can derive a small signal linear model of the transistor at that certain bias point and use that for amplifier design. This model is called the hybrid- π model of the transistor. At the core there is a voltage controlled current source, which transforms the input voltage to the output current (i_2=-g_m.v_1), g_m being the transconductance of the device. Since the drain current of the transistor (i_2) changes with the drain voltage (v_2), a shunt resistor (r_o) is added to the output (port-2) to emulate that effect. Parasitic capacitances, being present between source/gate/drain terminals, are added to the model through C_{GD}, C_{GS}, and C_{DS}. Series inductance and resistance due to the gate/source and drain interconnects can also be added to the model to make it more accurate. Finally a series non-quasi static (NQS) resistor can be added in series with C_{GS} to capture the effect of a frequency response. NQS resistance of the channel accounts for the fact that channel charge cannot respond instantaneously to the variation of gate-source voltage. NQS resistance is a distributed effect along the channel length. Electronic carriers (e.g., electrons) at any particular point within the channel of a MOSFET see a resistive element that "points" toward the source and a capacitive element that "points" toward the gate. A direct expression has been obtained for the channel charging resistance $R_{NQS} = \frac{1}{5g_m}$in reference [1].

Calculation of parameters in Table 1

To obtain the small signal model of a transistor, the measured two-port S-parameter data were exploited. The core hybrid-π core model of the transistor is realized by calculating impedance and admittance parameters (Z and Y matrixes) and using the following equations:

$g_m = -\mathrm{Re}(Y_{21})$

$r_o = 1/\mathrm{Re}(Y_{22})$

$C_{DS} + C_{GD} = \mathrm{Im}(Y_{22})/(2\pi f)$

$C_{GS} + C_{GD} = \mathrm{Im}(Y_{11})/(2\pi f)$

$C_{GS} + g_m r_o C_{GD} = 1/\mathrm{Im}(Z_{11})/(2\pi f)$

$R_{NQS} = 1/(5g_m)$

To fit the model to the measured data beyond the activity region of the transistor, series resistance and inductance associated with the gate, source and drain interconnects can be added and their values can be obtained by simulating gate, source and drain lines embedded in the oxide and substrate in an electromagnetic modeling and simulation software tool (such as Agilent Momentum). The component values calculated for the small signal model are listed in Table 1.

The effect of NW density on extrinsic cutoff frequency

To explore the performance limit of InAs NW parallel array FETs, extrinsic cutoff frequency is calculated as a function of NW density using the formula described in the main text. A previously reported saturation velocity for bulk InAs, v_{sat} ~1.3×10^7 cm/s at a field of 16 kV/cm (corresponding to V_{DS} = 2.5 V and L_G = 1.5 μm) was used for this analysis[2].

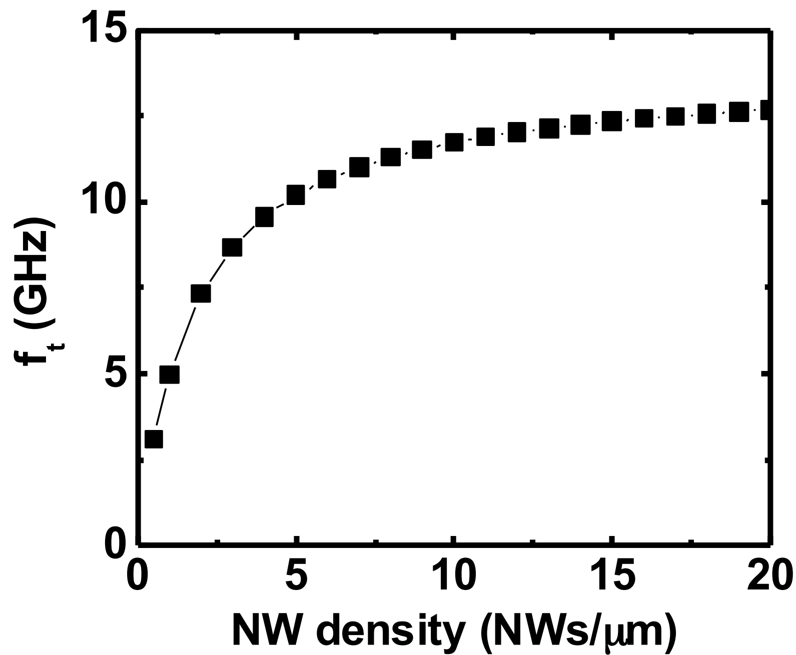

Figure B-3. The calculated cutoff frequency as a function of NW density for Lg=1.5 μm. Note that the parasitic capacitances are assumed to be the same as the experimental devices (Table 1). The dominant effect of increase the NW density is to reduce the $C_{p,GS}/C_{ox}$ ratio per unit width, thereby increasing the cutoff frequency.

Reference

[1] M. Baheri, Y. Tsividis, "A small signal dc-to-high-frequency nonquasi-static model for four-terminal MOSFET valid in all regions of operation" *IEEE Trans. Electron Devices* 1985 32, 2383–2391.
[2] K. Brennan, K. Hess, "High field transport in GaAs, InP and InAs" *Solid State Electron*. 1984, 27, 347-357.

Appendix C:
Supporting information of "Artificial electronic skin (E-skin)" (4.2)

Supporting Information

SWNT-network density as a function of surface treatment

99% semiconductor enriched SWNTs are deposited on two different substrates. One is SiO_2/Si substrate whose surface is oxygen plasma (30W for 1min) treated, followed by poly-L-lysine treatment for 5 min. The other is SiO_2/Si substrate whose surface is oxygen plasma (30W for 1min) treated, followed by APTES treatment for 30min. The particular SWNTs used here (as-received, IsoNanotubes-S from NanoIntegris, Inc) adhere readily to the poly-L-lysine treated substrate.

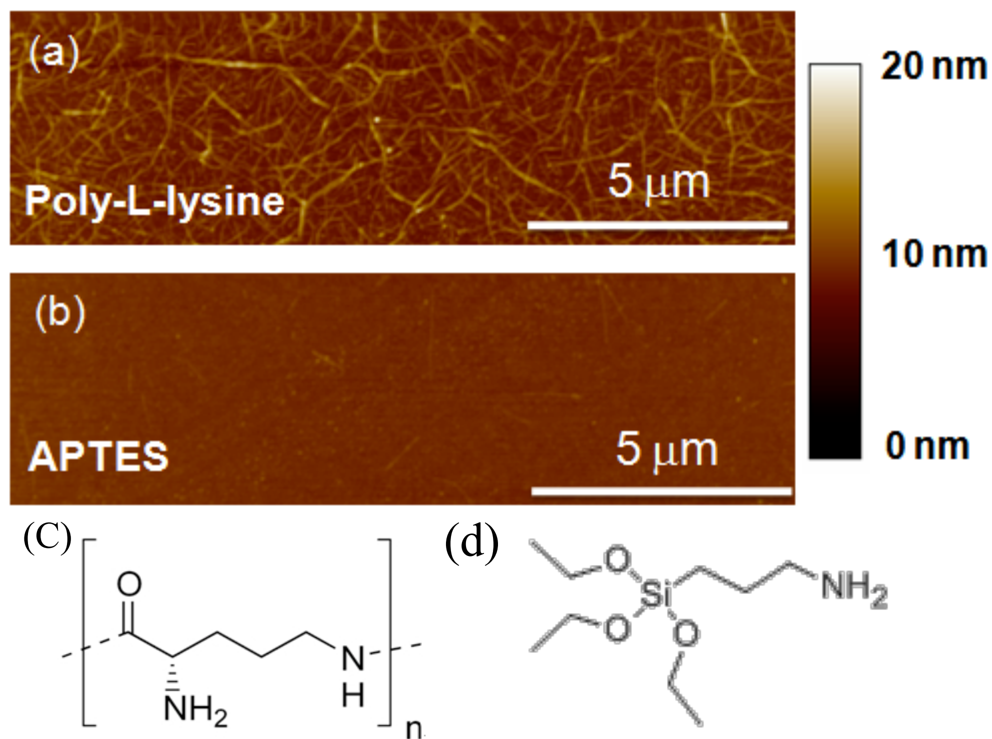

Figure C-1. The effect of surface treatment on the deposited nanotube density. The surface is treated with **(a)** poly-L-lysine for 5min and **(b)** aminopropyltriethyoxy silane (APTES) for 30min. SWNT deposition time is 20min. Chemical structure of **(c)** poly-L-lysine and **(d)** APTES.

SWNT-network density and bundling as a function of deposition time

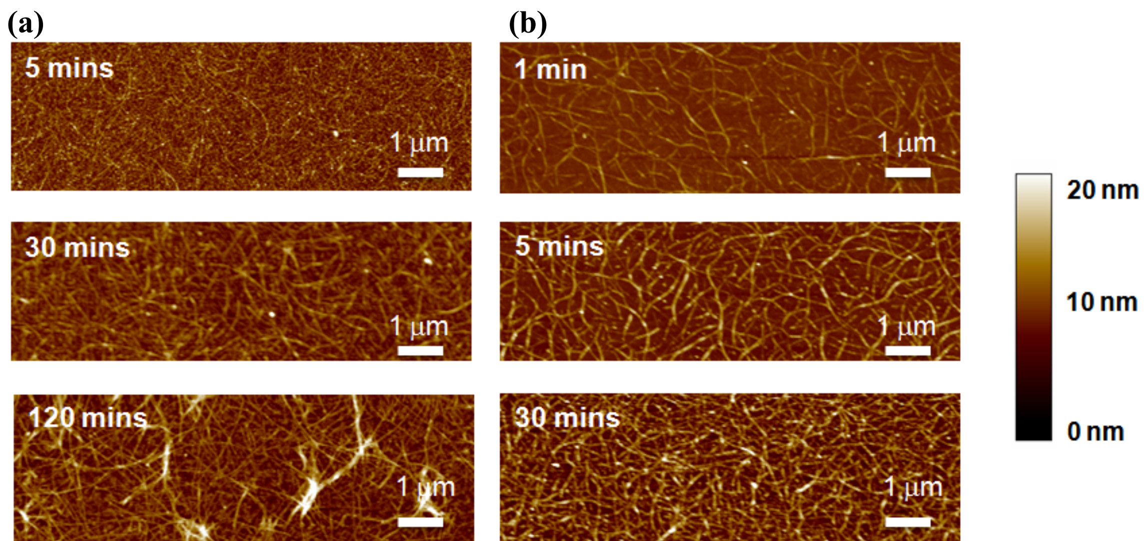

Figure C-2. AFM images taken from different SWNT deposition time on (a) evaporated SiO_2 and thermally grown SiO_2. (b). For (a), 5min, 30 min, and 120 min are used, and for (b) 1 min, 5 min, and 30min are used as SWNT deposition time. The density increases as deposition time increases, and eventually it forms nanotube bundles, which degrade the device I_{ON}/I_{OFF} ratio.

The effect of vacuum annealing on the electrical properties of SWNT-TFTs

Transfer characteristics at V_{DS} = 0.3 V and 3 V before and after vacuum annealing are shown in Fig. C-3. After vacuum annealing at 200 °C for 1h, both transconductance and I_{ON}/I_{OFF} ratio are dramatically improved. This improvement might possibly be due to the evaporation of surfactant residues.

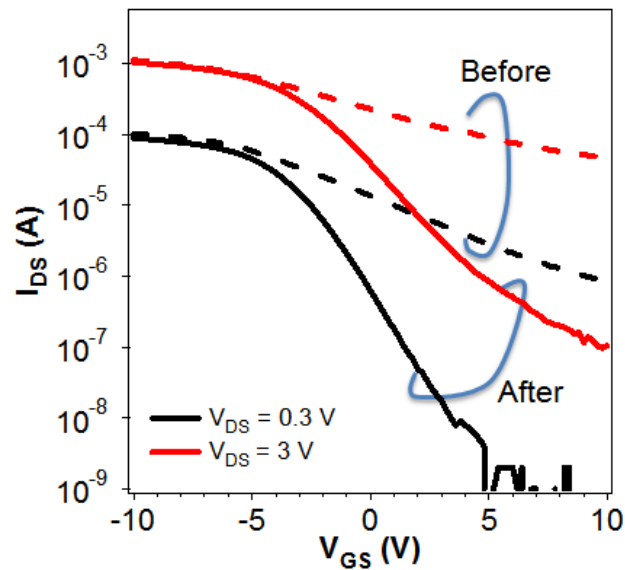

Figure C-3. The effect of vacuum annealing on the device properties. Transfer characteristics of a representative SWNT-network TFT before and after vacuum annealing at 200 °C for 1h.

Output characteristics of SWNT-TFTs

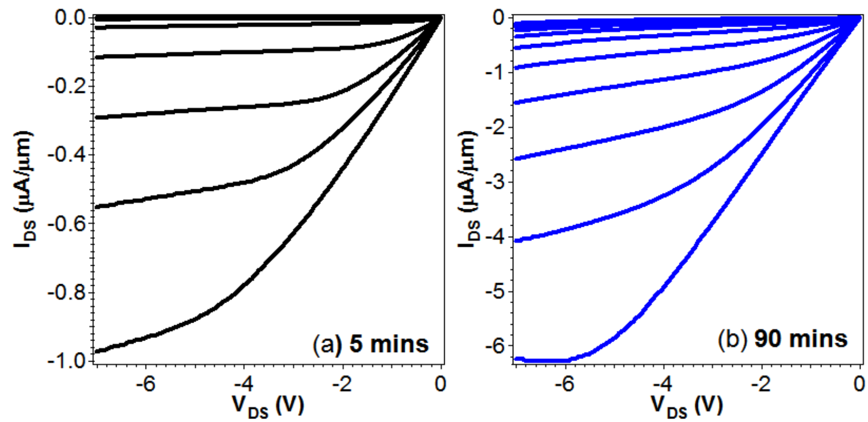

Figure C-4. Output characteristics of flexible SWNT-TFTs with two different SWNT densities. CNT deposition time of **(a)** 5 min and **(b)** 90 min. Applied V_g is from -10 V to 0 V with 1 V step from bottom to top.

Stretchable honeycomb structures

By changing the side length of the hexagonal holes with a fixed period of 3.3 mm, the stretching properties are tuned. Here, the x-component of stress tensor when the substrate is stretched by 2 mm is mechanically simulated with COMSOL for four different side lengths of hexagonal holes (from 1 mm to 1.85 mm). Clearly, the induced stress is reduced as the hole size increases, which is consistent with stretchability results in Fig. 4-3a. The active devices are placed as marked in blue circle in Fig. C-5c, where induced stress is minimum. This supports the experimental results in Fig. 4-4c.

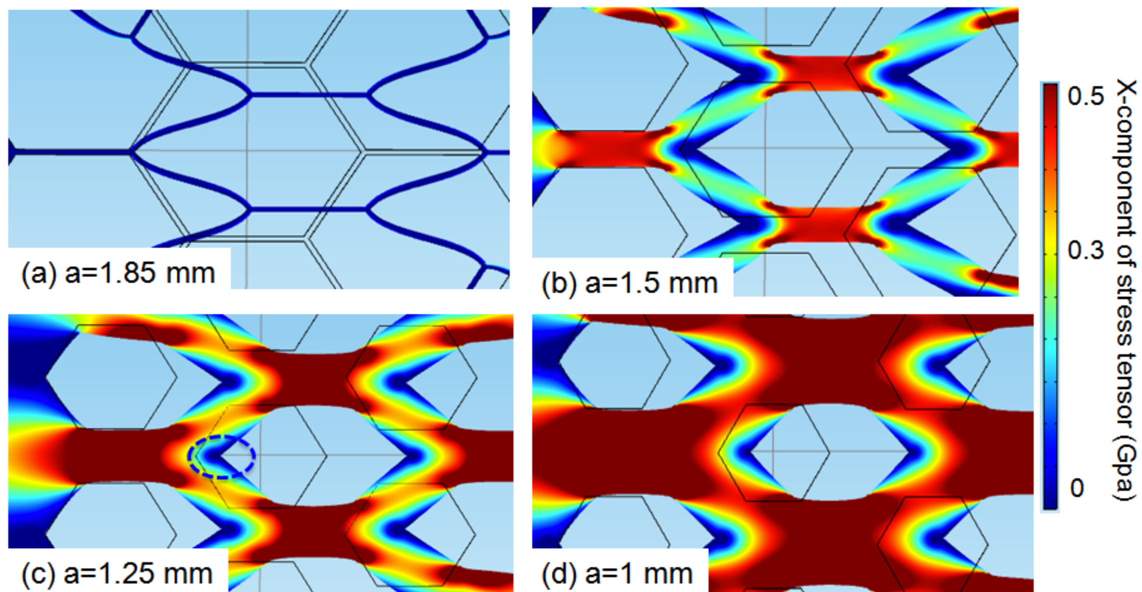

Figure C-5. Mechanical simulation results for honeycomb patterned PI substrates with a side length of the hexagon holes being **(a)** a = 1.85 mm, **(b)** a = 1.5 mm, **(c)** a = 1.25 mm, **(d)** a = 1 mm. Here, the substrate is stretched by 2 mm in the x-direction.