Harsh Environment Silicon Carbide Metal-Semiconductor Field-Effect Transistor

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by

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Committee in charge:

Professor Albert P. Pisano, Chair
Professor Tsu-Jae King Liu

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Research Project

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Abstract

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A harsh environment can be defined by one or more of the following: High temperature, high shock, high radiation, erosive flow, and corrosive media. Among all the harsh environment applications, high temperature applications have drawn lots of attention due to the emerging activity in automotive, turbine engine, space exploration and deep-well drilling telemetry. Silicon carbide has become the candidate for these harsh environment applications because of its wide bandgap, excellent chemical and thermal stability, and high breakdown electric field strength. This work details the fabrication process of n-channel silicon carbide metal-semiconductor field-effect transistors and the device performances are characterized from room temperature to 550 ℃. These devices are made along with the fabrication process of silicon carbide junction field-effect transistors. The high transconductance and on/off drain saturation current ratio for the entire temperature range suggest the possibility of using these devices for high temperature operational amplifier applications.

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Chapter 1

Introduction

1.1 Harsh Environment Sensing Application

Recently, many research efforts are focused on advancing renewable energy resources, such as solar, hydro, wind and geothermal energy. While developing on these new technologies, reducing the inefficiencies in generation and transmission should be considered. For example, the total energy lost is 61% of energy supply in U.S. in 2012 [1]. One method of addressing the inefficiencies in energy use is through the development of harsh environment sensing technology. Power systems can be advanced by integration of electronics (communication, signal processing, microactuator control, etc.) to be operated at high temperature [2, 3]. More specifically, smart harsh environment electronic sensing systems enable real-time condition based monitoring of temperature and incomplete combustion, and reduce emission of greenhouse gas (NO_x and CO_2) in gas turbine system or combustion engine [4, 5]. In addition, wireless technology helps telemetry systems to guide deep-well oil drilling operation or monitors the subsurface environments found in geothermal power plants.

Harsh environment can be defined by one or more of the following: High temperature (> 350 ℃), high shock (> 50,000 g), high radiation (> 100 Mrads), erosive flow and corrosive media [6]. Silicon is a widely used semiconductor material because of such factors as its high quality, stable oxide, and low cost. However silicon-based microelectronics are not suitable for harsh environments, because the electronic properties of silicon degrade above 300 ℃ due to the more intrinsic carrier presented than dopant carriers and mechanical properties degrade above 600 ℃ due to decline in its elastic modulus [3]. As the need increases for electronics and microelectromechanical systems (MEMS) devices suitable for harsh environment applications, including automobile, aerospace, nuclear and military purposes, several technologies such as silicon-on-insulator (SOI) or wide bandgap (WBG) electronics are needed. SOI technology can extend the CMOS operating temperature due to reduce leakage and less parasitic bipolar action [7]. Wide bandgap material has large energy bandgap of 3 eV so the generation of intrinsic carriers will not surpass the dopant carriers at high temperature.

In order to realize integration of the sensing system, the building block of the sensor system such as sensors and transistors need to be developed. Among all the harsh environment applications, high temperature application has drawn lots of attention due to the emerging activity in many areas (Table 1.1) [3]. In this work, we are focus on

developing the electronics for high temperature application. Silicon carbide (SiC) has been chose as based semiconductor material for this work due to a wide bandgap, high electric field breakdown strength, high thermal conductivity, and high saturated carrier drift velocity [8].

Application	Area	Peak ambient (℃)	Chip power (kW)	Target technology
Autimotive	On-cylinder & Exhaust pipe	600	< 1	WBG
Turbine engine	Sensors, telemetry, control	600	< 1	WBG
	Electric actuation	600	> 10	WBG
Spacecraft	Power management	300	> 10	WBG
	Venus & Mercury exploration	550	1	WBG
Industrial	High temperature processing	600	< 1	SOI & WBG
Deep-well drilling telemetry	Oil and gas	300	< 1	SOI & WBG
	geothermal	600	< 1	WBG

Table 1.1: High temperature electronics applications [3].

1.2 Silicon Carbide

The silicon carbide unit cell is the tetrahedron of four carbon atoms with a silicon atom in the center depicted in Figure 1.1. There are approximately 200 polytypes of SiC existing in the world [9]. Figure 1.2 shows the three most common polytypes of silicon carbide, consisting of different stacking sequences of SiC bilayer. They are cubic (3C, β-SiC) and hexagonal (H, α-SiC) with the number denoting the number of SiC bilayer stackings [10]. Because of the possible stacking sequences of SiC bilayer, there is lattice sites in SiC that have a surrounding layer stacking in hexagonal form and others with cubic form, which are denoted hexagonal sites and cubic sites, respectively [11]. Figure 1.3 shows that 3C-SiC has one cubic site and 2H-SiC includes only one hexagonal site. 4H-SiC has one hexagonal and one cubic site, while 6H-SiC exhibits one hexagonal and two cubic sites. 4H-SiC and 6H-SiC polytypes already have commercially available wafers and epitaxy, while 3C-SiC is the only polytype that can be grown heteroepitaxially on a Si wafer [12-18]. The basic mechanical and electrical properties of the three SiC polytypes, as well as those for Si, GaN, AlN, and Diamond are shown in Table 1.2 and 1.3 [11, 19, 20].

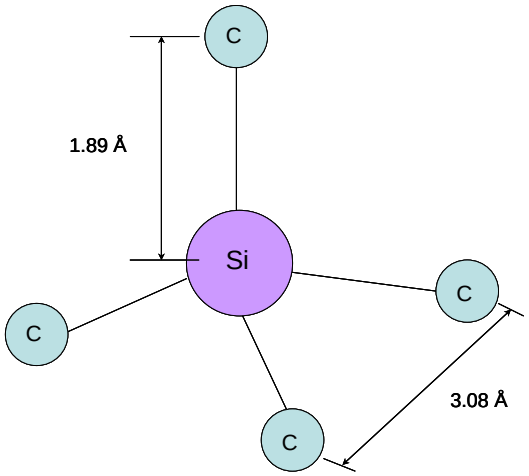

Figure 1.1: The structure of SiC crystal.

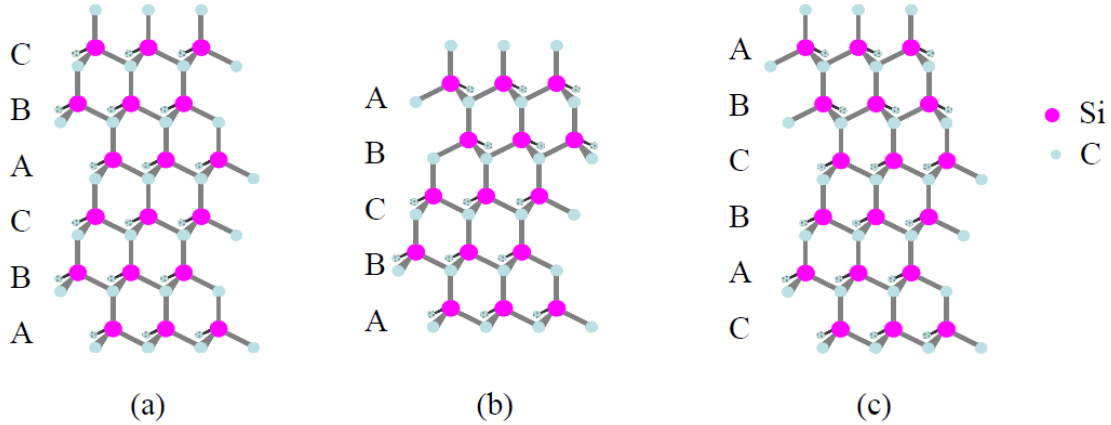

Figure 1.2: Three most common polytypes of silicon carbide [10]. *Copyright: Dr. Christopher S. Roper*

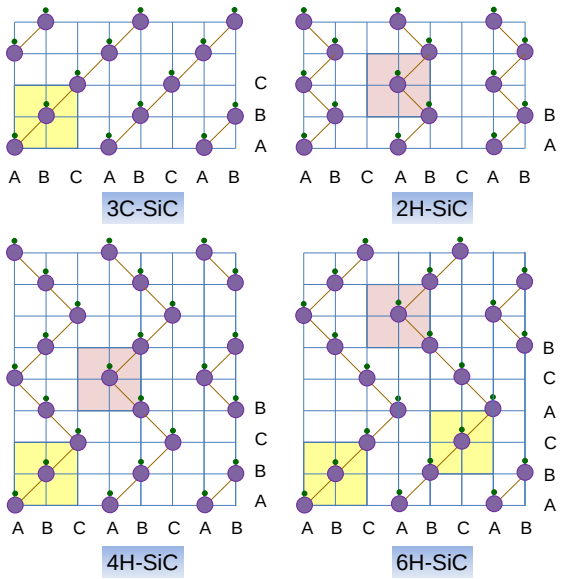

Figure 1.3: Bi-layer stacking for the SiC polytypes 3C, 2H, 4H, and 6H [11].

	Si	3C-SiC	6H-SiC	4H-SiC	2H-GaN	2H-AlN	Diamond
Lattice a (Å)	5.43	4.36	3.08	3.08	3.189	3.112	3.567
Lattice c (Å)	NA	NA	15.12	10.08	5.185	4.982	NA
Thermal expansion coefficient (10^{-6}/K)	2.6	3.28	3.35/3.25	3.3/3.16	5.59/3.17	5.27/4.15	0.8
Density (g/cm^3)	2.33	3.21	3.21	3.21	6.15	3.23	3.5
Thermal conductivity (W/cm K)	1.5	3.6	4.9	4.9	1.3	2.85	20
Melting point (°C)	1420	2830	2830	2830	2500	3000	4000
Mohs hardness	7	9	9	9		7	10

Table 1.2: Mechanical properties of Si and wide bandgap semiconductors. If the thermal expansion coefficient has two values, the first one is along the a-axis and the second one is along the c-axis.

	Si	3C-SiC	6H-SiC	4H-SiC	2H-GaN	2H-AlN	Diamond
Energy bandgap (eV)	1.12	2.4	3.0	3.23	3.4	6.2	5.6
Breakdown field(MV/cm)	0.25	2.5	2.5	2.2	3.0	2.0	20
Electron saturation velocity (10^7 cm/s)	1.0	2.5	2.0	2.0	2.5	2.0	2.7
Electron mobility (Cm/V s)	1400	1000	500/100	950/1150	1245	135	2200
Hole mobility (cm/V s)	600	50	80	120	370	14	1600
Dielectric constant	11.9	9.7	10.0	10.0	9.5	8.5	5.5

Table 1.3: Electrical properties of Si and wide bandgap semiconductors. If the electron mobility has two values, the first one is perpendicular to the c-axis and the second one is parallel to the c-axis.

Owing to the superior mechanical properties of SiC, it is very suitable for the Microelectromechanical systems (MEMS). SiC based MEMS devices have been previously used as temperature and pressure sensors in high temperature environment

[21], high-g accelerometers [22], biomedical sensors [23], and strain sensor [5]. SiC may also be suitable for high frequency MEMS resonators as micromechanical oscillators and filters due to its high E/ρ ratio, since the resonant frequency of a micromachined device can be expressed as

$$\omega = Cf\sqrt{\frac{E}{\rho}} \tag{1.1}$$

where C is constant, f is a function of Poisson's ratio, E is the material Young's modulus and ρ is the material density. SiC has been successfully used to fabricate Lamé mode MEMS resonators for signal processing [24].

SiC may be used for high temperature, high power, high frequency and radiation resistance electronics applications. For example, its wide bandgap makes SiC desirable for electronics in high temperature environments. Additionally, breakdown electric field strength (E_{max}) is perhaps the most important factor for high power applications: the E_{max} of SiC is ten times that of silicon. As high-frequency devices, the saturated electron drift velocity of SiC is twice that of silicon, thus enabling microwave devices to reach high channel currents [25-27].

1.3 SiC Electronics Low Voltage High Temperature Application

Lots of progress has been made for the development of high temperature SiC electronic devices for low voltage or low power analog and digital circuit applications. D. M Brown et al. from Generic Electric Company reported a 6H-SiC operational amplifier based on the n-channel enhancement and depletion mode metal-oxide-semiconductor field effect transistors (MOSFETs). It works up to 300 ℃ with a low frequency gain of 53 dB and the bandwidth of 269 kHz [28]. A monolithic 6H-SiC CMOS digital integrated circuits has been developed [29]. The threshold voltages of PMOS and NMOS at 300 ℃ are -6 V and 0.5 V, respectively. The effect channel mobilities of PMOS and NMOS at 300 ℃ are 7.01 and 20.8 cm^2/Vs, respectively. Raytheon has been developed the 4H-SiC CMOS integrated circuit with operating temperature of 400 ℃ [30]. The gate leakage current is less than 1 pA at 350 ℃.

A differential amplifier using 6H-SiC metal-semiconductor field effect transistor (MESFETs) and thick film hybrid technology has been reported [31]. It has a voltage gain of 61 dB, common mode rejection ratio (CMRR) of 60 dB, bandwidth of 910 kHz, offset voltage of 151 mV, and power dissipation of 178 mW at 350 ℃. NASA Glenn Research Center has demonstrated a 4H-SiC MESFET based hybrid, ultra high frequency band differential oscillator [32]. The oscillator delivers 4.9 dBm at 453 MHz at 475 ℃. M. Alexandru et al. designed and characterized 4H-SiC MESFET based inverter, NAND and NOR gates that work up to 300 ℃ [33]. 4H-SiC bipolar junction transistor (BJT) with operating temperature up to 500 ℃ has been reported [34]. The current gain is approximately 42 at 500 ℃ using Ti/TiW/Al metallization.

Numerous studies on SiC junction field effect transistor (JFETs) for high temperature applications. This is because the JFET structure is based on pn junction which are free of oxide reliability and Schottky contact stability existing in MOSFET and MESFET in the temperature range of 500 ℃. A back gate n-channel 6H-SiC JFET has been developed and modeled up to 400 ℃ [35]. Daimler Benz Research Laboratories reported the 6H-SiC implanted-gate n-channel JFETs with working temperature of 400 ℃. The transconductance is approximately 0.16 mS/mm and on/off saturation drain current ratio is ~ 106 at 400 ℃. NASA Glenn Research Center has demonstrated very stable long term operation of 6H-SiC n-channel JFETs at 500 ℃ for more than 3007 hours [36]. A 600 ℃ of NAND and NOR gates have also been developed in this center [37]. A AC coupled differential amplifier using 4H-SiC vertical JFET has been developed, and the voltage gain is 47.8 dB with CMRR of ~ 45 dB at 500 kHz at 450 ℃ [38]. A. C. Patil et al. has reported a 6H-SiC JFET based two stage differential amplifier with a voltage gain of 69.2 dB and unit gain frequency of 1.4 MHz at 576 ℃ [39].

Table 1.4 below summarizes the maximum operating temperature of recent works for low voltage high temperature single transistors including SiC, GaN and diamond. It can be seen that SiC shows promising preliminary results of high temperature electronics. However, lots of challenges still need to be address until the commercialization. First, the process of making SiC based electronics devices is not as mature as that for Si CMOS. This is because the design and process approaches for Si based electronics can not be directly used for SiC based electronics due to different materials properties. Besides, the reliability and resistivity of Ohmic contact areas need to be further improved for high temperature operations. Perhaps the most important factor however is that large scale, high quality, and low cost epitaxial or single crystal SiC films have not yet been fully developed. A technology capable of providing these would greatly improve the availability of SiC high temperature electronic devices. In summary, there exist many limitations for SiC based electronics and their integrate circuits but the superior material properties of SiC makes it desirable to be used for extremely high temperature electronics.

References	Material	Device	Max. Temperature (°C)
IMB-CNM, Spain (2012) [33]	4H-SiC	MESFET	300
Raytheon, UK (2011) [30]	4H-SiC	MOSFET	350
Semisouth Lab, USA (2009) [40]	4H-SiC	VJFET	450
JPL, USA (2010) [41]	AlGaN/GaN	MOS HEMT	450
Tokyo Insitute of Technology, Japan (2013) [42]	Diamond	JFET	450
KTH, Sweden (2013) [34]	4H-SiC	BJT	500
NASA, USA [36]	6H-SiC	JFET	500
University of Ulm, Germany (2012) [43]	InAlN/GaN	HEMT	1000

Table 1.4: A sampling of published single transistors for high temperature applications.

1.4 High Temperature Effects in 4H-SiC

To successfully design the high temperature 4H-SiC electronics, it is crucial to understand the temperature effect of the fundamental semiconductor physical properties.

The energy bandgap (E_G) in 4H-SiC as a function of temperature is approximated by [44]

$$E_G = 3.265 - 6.5 \times 10^{-4}\left(\frac{T^2}{T+1300}\right) \tag{1.2}$$

where T is temperature. The calculated bandgap of Si, 6H-SiC, and 4H-SiC are plotted in Figure 1.4. 4H-SiC has highest bandgap through the entire temperature. As temperature increases, the bandgap is reduced which results in larger intrinsic carrier concentrations, larger leakage current in pn junctions and poorer device isolation by reversed-biased junctions [39].

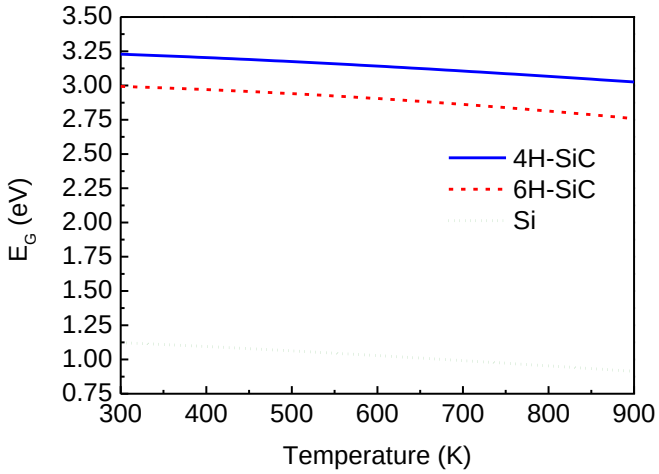

Figure 1.4: Calculated energy bandgap of Si, 6H-SiC, and 4H-SiC versus temperature.

The intrinsic carrier concentration (n_i) in 4H-SiC is given by [45]

$$n_i = \sqrt{N_c N_v}\exp\left(-\frac{E_G}{2k_B T}\right) \tag{1.3}$$

$$N_c = 2M_c\left(\frac{2\pi m_n^* k_B T}{h^2}\right)^{3/2} \tag{1.4}$$

$$N_v = 2\left(\frac{2\pi m_p^* k_B T}{h^2}\right)^{3/2} \tag{1.5}$$

where N_c and N_v are effective density-of-states of electrons in the conduction band and holes in the valence band, respectively. k_B is Boltzmann constant, h is planck's constant,

M_c represent the number of equivalent energy minima in the conduction band which is 3 for 4H-SiC, m_n^* and m_p^* are the electron effective mass and hole effective mass, respectively. Figure 1.5 compares the intrinsic carrier concentration of Si, 6H-SiC, and 4H-SiC versus temperature. For a given temperature, 4H-SiC has the smallest n_i due to the largest bandgap energy. The intrinsic carrier concentration of Si at 900 K is 4.3×10^{17} cm^{-3} which is comparable with the dopant carrier concentrations. Even at 900 K, n_i of 6H-SiC and 4H-SiC are only 4.32×10^{12} and 3.24×10^{11} cm^{-3}, suggesting a fundamental advantage of wide bandgap SiC over Si for high temperature application.

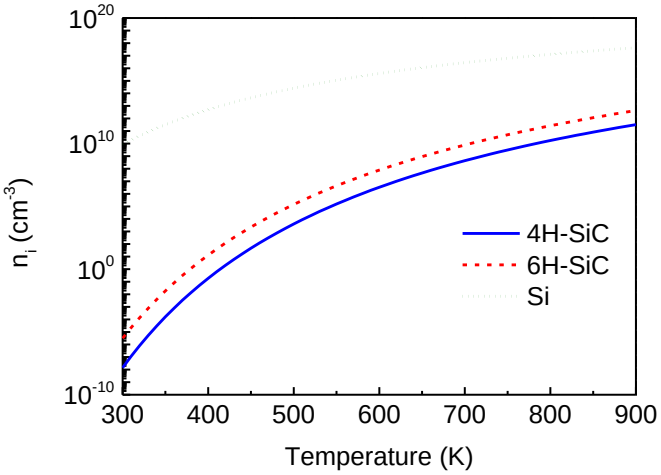

Figure 1.5: Intrinsic carrier concentration in Si, 6H-SiC, and 4H-SiC versus temperature.

1.5 Research Objective and Thesis Overview

High temperature electronics that operate at 300-600 ℃ are beneficial for in-situ monitoring of fuel combustion, subsurface reservoirs (deep well drilling), and Venus and Jupiter surface exploration. This dissertation details the high temperature performance of the 4H-SiC MESFET.

Chapter 2 describes the physics and the fabrication of the MESFET. In Chapter 3, the study of 4H-SiC n–channel MESFET is presented. The basic properties of MESFET from 25 to 550 ℃ is characterized and summarized. Finally, in Chapter 4 the contributions of this work are summarized and future research directions are suggested.

Chapter 2

Physics and Fabrication Process of Metal-Semiconductor Field-Effect Transistor

2.1 Physics of MESFET

The metal-semiconductor field-effect transistor was invented by C. Mead in 1966 [46]. It is a unipolar transistor which means only one type of carrier is involved in the operation. Unlike MOSFET for high temperature operation, MESFET eliminates the chance of metal-semiconductor-oxide interface traps, increase oxide reliability, and reduces the minority carrier instability [47]. The metal gate using low temperature process compared to pn junction made by high temperature growth or ion implantations [48]. The metal gate has better control of size scaling and hence it is beneficial for enhancing the speed of the transistor.

The fundamental operation principle of n-channel MESFET is described as follows [48-50]. First, the gate terminal is grounded and the drain voltage is 0 V. MESFET is in thermal equilibrium. As shown in Figure 2.1 (a), once the metal-n Schottky junction is deposited, the depletion width is formed. Due to the metal gate, the depletion region primarily extends into the n-channel area of the device. The device at this stage is in off state (Figure 3.1 (b)). Applying V_D to small positive voltages, the channel is formed at the non-depleted and current-carrying region as shown in Figure 3.1 (c). The channel acts like a simple resistor, and the drain current is increased linearly with drain voltage as shown in point B of Figure 3.1 (d). As V_D keeps increasing, the depletion width around drain side is widened as shown in Figure 3.1 (e). The channel region is still like a resistor, but because of the loss of the conduction channel near the drain side, the resistance between the source and drain is increased and the increasing rate of I_D is reduced which results the slope of I_D-V_D characteristic decreases at larger V_D as shown in point C of Figure 3.1 (f). If we continue to increase the V_D, the channel is further narrowed and eventually reaches the pinch-off state shown in Figure 3.1 (g). The slope of I_D-V_D characteristic is approximately zero at the pinch-off set, as shown at point D in Figure 3.1 (h), and the drain bias at this point is called saturation drain voltage (V_{Dsat}). As the drain voltage becomes larger than V_{Dsat}, the pinch-off area widens to the extent of ΔL. The voltage difference between V_D and V_{Dsat} is mainly dropped along the ΔL, and the major mechanism of current flow is through drift current as shown in Figure 3.1 (i). The

corresponding I_D-V_D characteristic saturates, namely remaining constant at the saturation drain current shown in point E of Figure 3.1 (j).

The drain current (I_{DS}) versus drain-to-source voltage (V_{DS}) characteristics of MESFET can be expressed using the conventional 3/2 power model [48]. The basic assumptions are uniformly doped channel with gradual-channel approximation (i.e., electric field perpendicular to channel is smaller than electric field parallel to channel), abrupt depletion layer, small gate leakage current and constant mobility. The built-in potential (V_{bi}) of MESFET is given by

$$V_{bi} = \phi_{Bn} - \frac{kT}{q} ln\left(\frac{N_c}{N_D}\right) \tag{2.1}$$

where q is unit electronic charge, ϕ_{Bn} is the Schottky barrier height, k is Boltzmann constant, T is temperature, N_D is donor impurity concentration, and N_C is the effective density of states in conduction band. The pinch-off potential (V_P) is given by

$$V_P = \frac{qN_D D}{2\varepsilon_s} \tag{2.2}$$

where D is the channel depth and ε_s is permittivity of 4H-SiC. The normalized pinch-off current (I_P') is given by

$$I_P' = \left(\frac{q^2 N_D n \mu_n D^3}{6\varepsilon_s}\right) \tag{2.3}$$

where n is ionized carrier concentration in the channel and μ_n is mobility of carriers. The gate threshold voltage (V_T) around which the MESFET is turned on and off is given by

$$V_T = V_{bi} - V_P \tag{2.4}$$

In triode region, where $V_{DS} < V_{Dsat} = V_{GS} - V_T$, the drain current is given by

$$I_{DS} = \left(\frac{W}{L}\right) I_P' \left[\frac{3V_{DS}}{V_p} - 2\left[\left\{\frac{V_{DS}-V_{GS}+V_{bi}}{V_p}\right\}^{3/2} - \left\{\frac{(-V_{GS}+V_{bi})}{V_p}\right\}^{3/2}\right]\right](1 + \lambda V_{DS}) \tag{2.5}$$

In saturation region, where $V_{DS} \geq V_{Dsat} = V_{GS} - V_T$,

$$I_{DS} = \left(\frac{W}{L}\right) I_P' \left[1 - 3\left(\frac{-V_{GS}+V_{bi}}{V_{po}}\right) + 2\left(\frac{-V_{GS}+V_{bi}}{V_{po}}\right)^{3/2}\right](1 + \lambda V_{DS}) \tag{2.6}$$

where W and L are channel width and length, respectively, V_{GS} is the gate-to-source voltage, and λ is channel length modulation parameter of the MESFET.

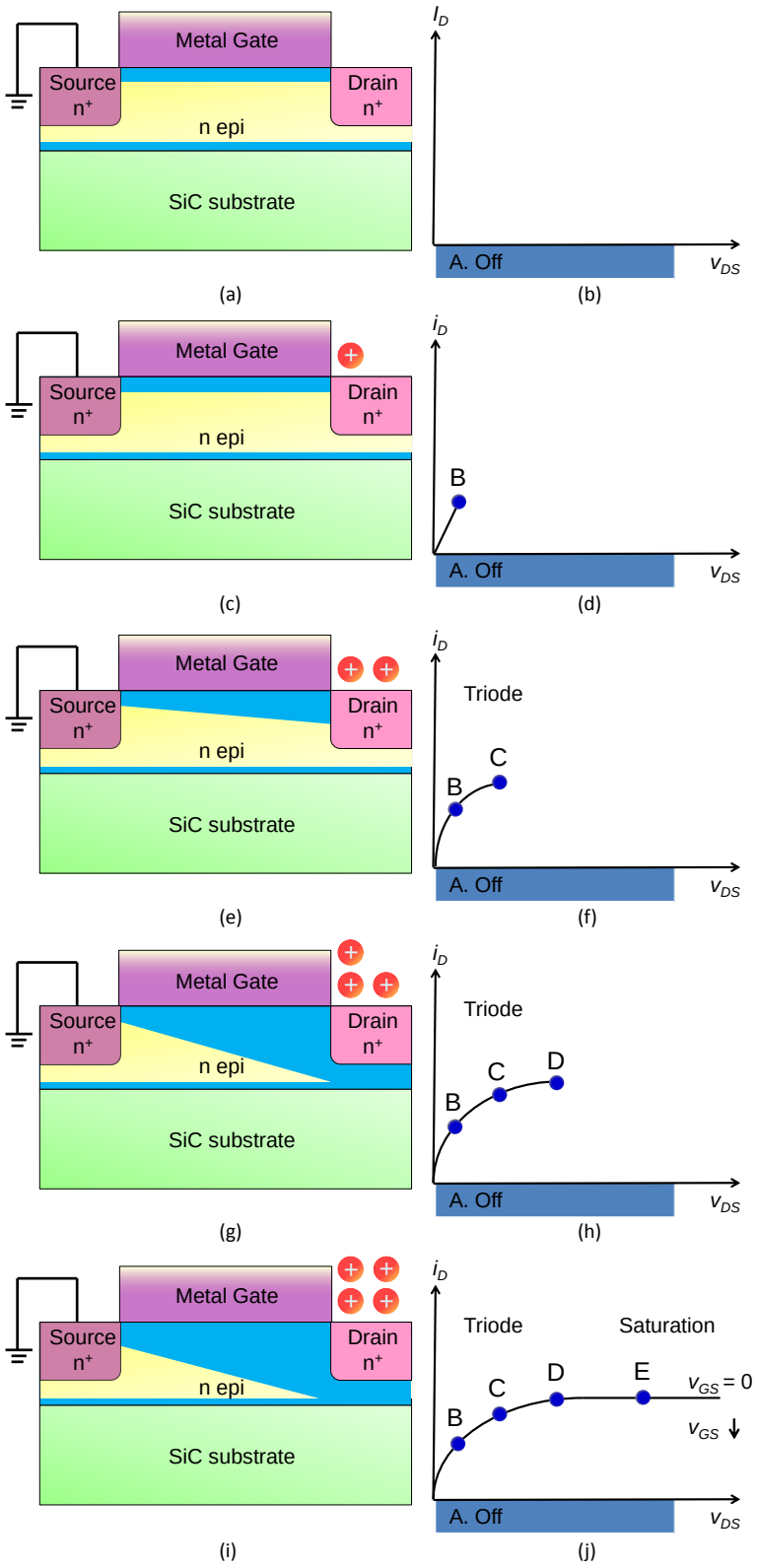

Figure 2.1: Visualization of various phases of MESFET operation and the corresponding I_D-V_D characteristics at V_{GS} = 0 V. Note the SiC substrate serves as the body biasing point. The blue color in schematic represents the depletion regions, and the yellow color shows the channel region. The shape of the channel is for the purpose of demonstration and it is not the real situation.

2.2 Fabrication Process and Characterization Methods

Figure 2.2 is a cross-sectional schematic of a lateral n-channel 4H-SiC MESFET used in this work. The device was fabricated with the same process of n-channel JFET. The transistor consists of p-type 4H-SiC wafer (from Cree Inc.) with three epitaxial layers (from Ascatron AB). A 5 μm p- epitaxial layer with doping concentration of 2×10^{15} cm^{-3}, followed by 300 nm n- epitaxial layer with doping concentration of 1×10^{17} cm^{-3} and 200 nm p^+ epitaxial layer with doping concentration of 2×10^{19} cm^{-3} were grown on the p-type wafer with the resistivity of approximately 1 Ω-cm. The entire fabrication process flow is shown in Figure 2.3 including seven lithography masks. First, the p^+ layer for gate of JFET was removed by time etched using transformer coupled plasma (TCP) etcher with 90 sccm Cl_2 and 10 sccm BCl_3 under RF bias of 150 W. 1 μm plasma-enhanced chemical vapor deposition (PECVD) SiO_2 was patterned to define the source and drain area with nitrogen implantation at 600 ˚C which facilitates Ohmic contact to the metal with reduced damage of crystallinity [51]. The implantation of a box profile was formed using 1.4×10^{15}, 7×10^{14}, and 3.6×10^{14} doses at 60, 40, and 20 keV energies, respectively. The implantation should yield a nitrogen concentration higher than 10^{19} cm^{-3}. After ion implantation, the oxide layers were removed by the buffer oxide etching solution (hydrofluoric acid). The second lighter-dose nitrogen was implanted using 3.2×10^{12}, 8×10^{11}, 8×10^{11}, and 1×10^{12} doses at 33, 24, 18, and 10 keV energies, respectively [37]. The implanted dopants were electrically activated by annealing samples capped with 2 μm PECVD SiO_2 at 1450 ℃ under an Argon atmosphere for 30 minutes. Note that the second light-dose implantation was for the purpose of reducing the resistance from the gate to source/drain of JFET, and is not necessary for MESFET. A mesa etch was then used to define the device area using a transformer coupled plasma etcher. The MESFET surface was then passivated with PECVD SiO_2 and the 50 nm Ti, 100 nm Ni, and a 50 nm TiW (10% Ti, 90% W) metal gate and contact of source/drain was deposited and patterned via lift-off to form the contact electrode. The metal contacts were annealed with rapid thermal annealing (RTA) at 1000 ℃ for 2 minute under Ar ambient. 200 nm TiW (10% Ti, 90% W) was used for the 1st level of metal interconnects. Finally, the 20 nm Cr and 180 nm Pt was used for 2nd level of metal interconnect and the backside contact of the wafer. Pt was chosen as the final contact due to the compatibility for wire bonding and also helps contacts operate for a significantly longer time under a high temperature environment by protecting the underlying metals [52].

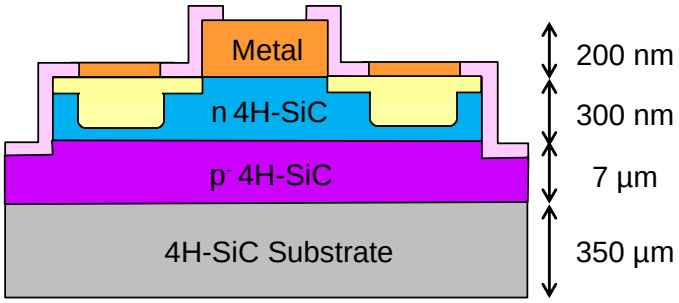

Figure 2.2: Schematic of a lateral n-channel 4H-SiC MESFET.

Devices were characterized on a hot chuck of high temperature probe station (Signatone Inc.) as shown in Figure 2.4. This high temperature probe station consists of ceramic hot chunk, thermal heater, and water cooler, and the chunk temperature goes up to 600 ℃ with low thermal noise of 10^{-9}-10^{-8} A at 600 ℃. An HP 4156B semiconductor parameter analyzer and Agilent B2912A precision source/measurement unit with tungsten probe tips were used to measure the I-V characteristics of the devices as shown in Figure 2.5.

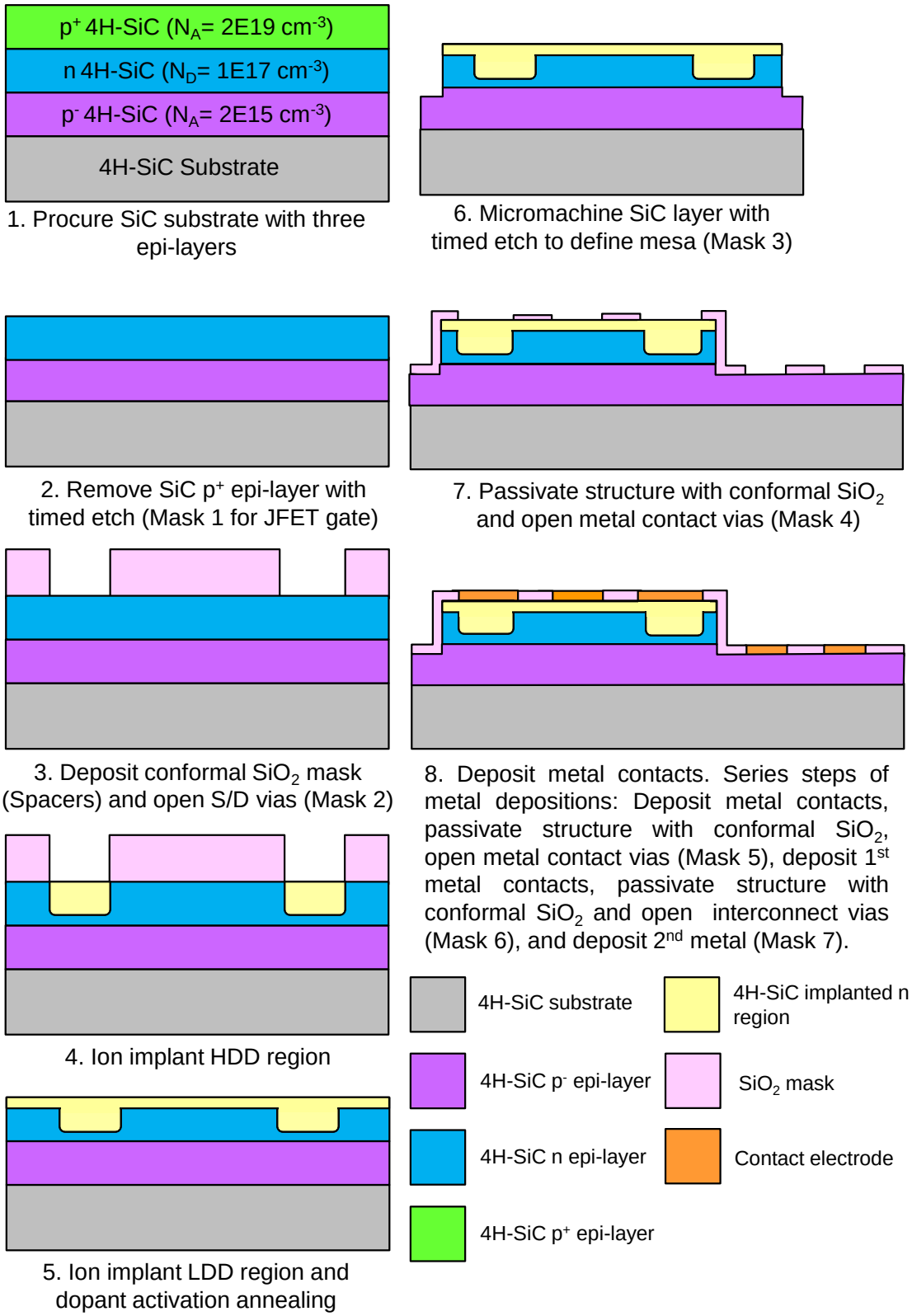

Figure 2.3: Fabrication process flow n-channel 4H-SiC MESFET.

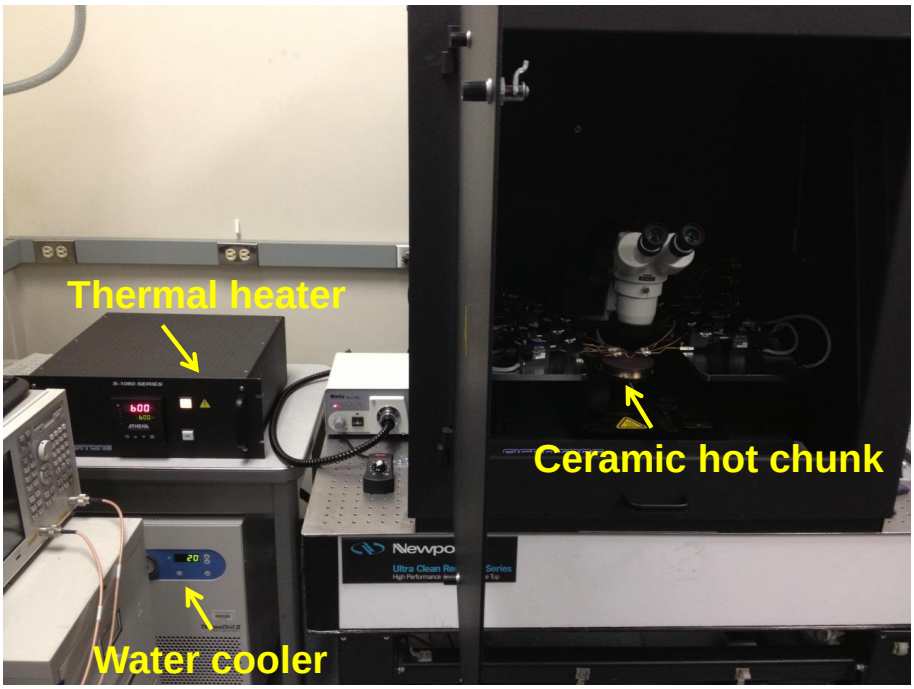

Figure 2.4: High temperature probe station.

Figure 2.5: HP 4156B semiconductor parameter analyzer and Agilent B2912A precision source/measurement unit.

Chapter 3

Silicon Carbide N-channel Metal-Semiconductor Field-Effect Transistors

3.1 Characterization of N-MESFET at Room Temperature

Figure 3.1 shows the optical images of as-fabricated 4H-SiC lateral MESFET. The device has double-finger geometry with L = 2.5 μm and effective W = 50 μm. Figure 3.2 shows the drain current versus drain-to-source voltage characteristics of a 50 μm /2.5 μm MESFET after RTA at room temperature. The device is fully-on at V_{GS} = 0 V and cut-off at V_{GS} = -9 V. λ is estimated to be 1.15×10^{-2} V^{-1}. The drain-to-source saturation current is 40.6 mA/mm and the current density is 738 A/cm^2 at V_{DS} = 20 V and V_{GS} = 0 V. Figure 3.3 (a) shows the drain current versus gate-to-source voltage characteristics at V_{DS} = 20 V and the threshold voltage can be extracted from the extrapolated intercept of x axis of $\sqrt{\frac{I_{DS}}{1+\lambda V_{DS}}}$ vs. V_{GS} plot at V_{DS} = 20 V in Figure 3.3 (b). The threshold voltage is approximately -7.07 V at 25 ℃.

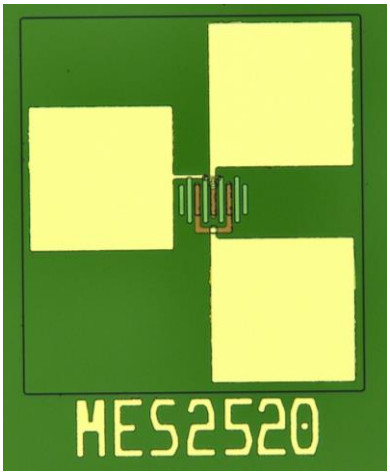

Figure 3.1: Optical image of a n-channel raised gate 4H-SiC MESFET with L = 2.5 μm and W = 50 μm.

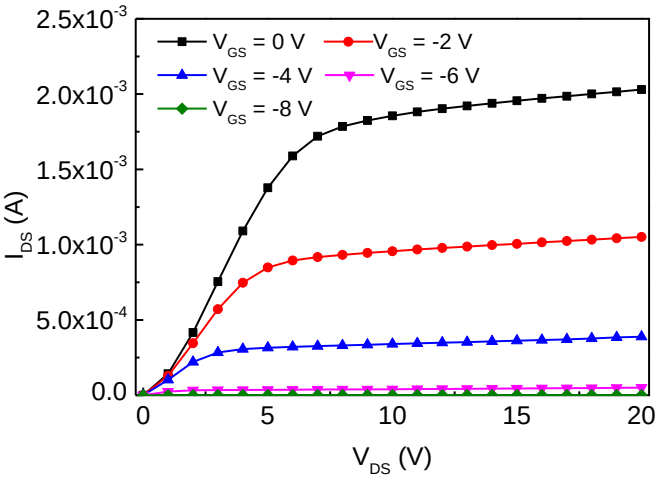

Figure 3.2: I_{DS}-V_{DS} characteristics of a n-channel 4H-SiC MESFET after RTA under different V_{GS} and with W/L= 50 µm/2.5 µm at 25 ℃.

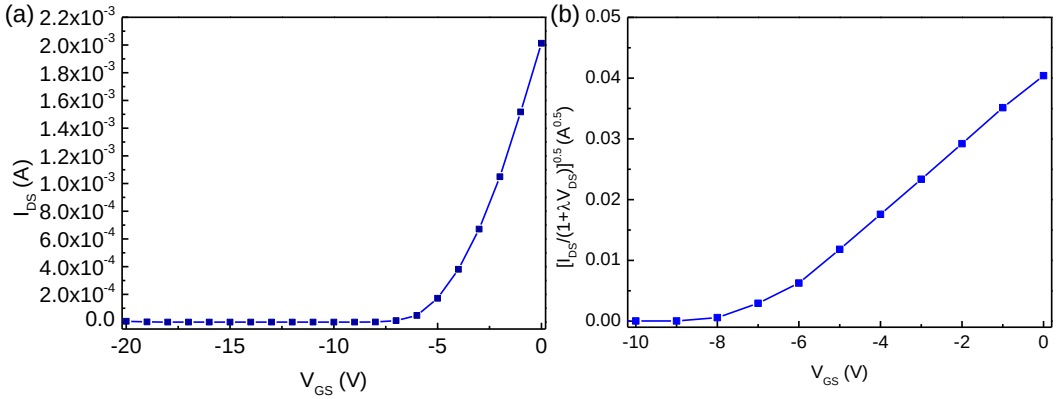

Figure 3.3: (a) I_{DS}-V_{GS} (b) $\sqrt{I_{DS}}$-V_{GS} characteristics of a n-channel 4H-SiC MESFET with W/L= 50 µm/2.5 µm and V_{DS} = 20 V at 25 ℃.

The transconductance (g_m) could be extracted from square-law model using Taylor expansion near $V_{GS} = V_T$ as follows [39, 47]

$$k' = \frac{3I_P'}{4V_{po}'} = \frac{\mu_n \varepsilon_s n}{2DN_D} \tag{3.1}$$

$$g_m = 2\sqrt{\frac{w}{L}k'I_{DS}} = \frac{2I_{DS}}{V_{GS}-V_T} \tag{3.2}$$

The estimated g_m of 4H-SiC MESFET is 11.36 µS/µm (normalized with the channel width of 50 µm) at room temperature. The estimated output resistance (r_o) is 5.22×10^4 Ω. The intrinsic gain ($g_m r_o$) of single 4H-SiC MESFET is approximately 29.6 or 29.4 dB at V_{GS} = 0 V.

3.2 Characterization of N-MESFET at High Temperatures

Figure 3.4 (a)-(g) show the I_{DS}-V_{DS} characteristics of n-channel raised gate 4H-SiC MESFET from 100 to 550 ℃. The MESFET shows excellent I_{DS}-V_{DS} characteristics over the entire temperature range. Figure 3.5 shows the I_{DS}-V_{GS} curves under a drain-to-source 20 V bias and at incremental temperatures up to 550 ℃. A monotonic decrease in saturation current is observed, and this can be attributed to the power law degradation of the electron mobility at elevated temperatures [53]. The degradation of the mobility also causes the R_{on} to increase from 9.55 to 28.17 mΩ cm^2. The I_{Dsat} of MESFET at V_{GS} = 0 V and 550 ℃ is approximately 72 % less than its value at room temperature. However, the device is fully functional that the change of I_{Dsat} is in response to the applied gate voltage at 550 ℃, as shown in Figure 3.4 (f). The off current (I_{off}) at V = -9 V increases from 9.4×10^{-10} A to 3.2×10^{-7} A as the temperature increase from 25 ℃ to 550 ℃ due to the decrease of the energy bandgap of 4H-SiC at elevated temperatures (Figure 1.4) [45, 53]. The calculated on/off drain saturation current ratio (I_{Dsat}/I_{off}) is 2.14×10^{6} at room temperature and decreases to 1.85×10^{3} at 600 ℃ suggesting a good electrostatic controllability of metal gate. Further increasing the ambient temperature to 600 ℃, the devices only work for few minutes and loss the typical I-V characteristics of MESFET. This is because the metal interconnect, 200 nm TiW in this case, has been destroyed as shown in Figure 3.6. More robust metal interconnect which is thermal stable without morphology change is required to extend the working temperature from 550 ℃ to 600 ℃.

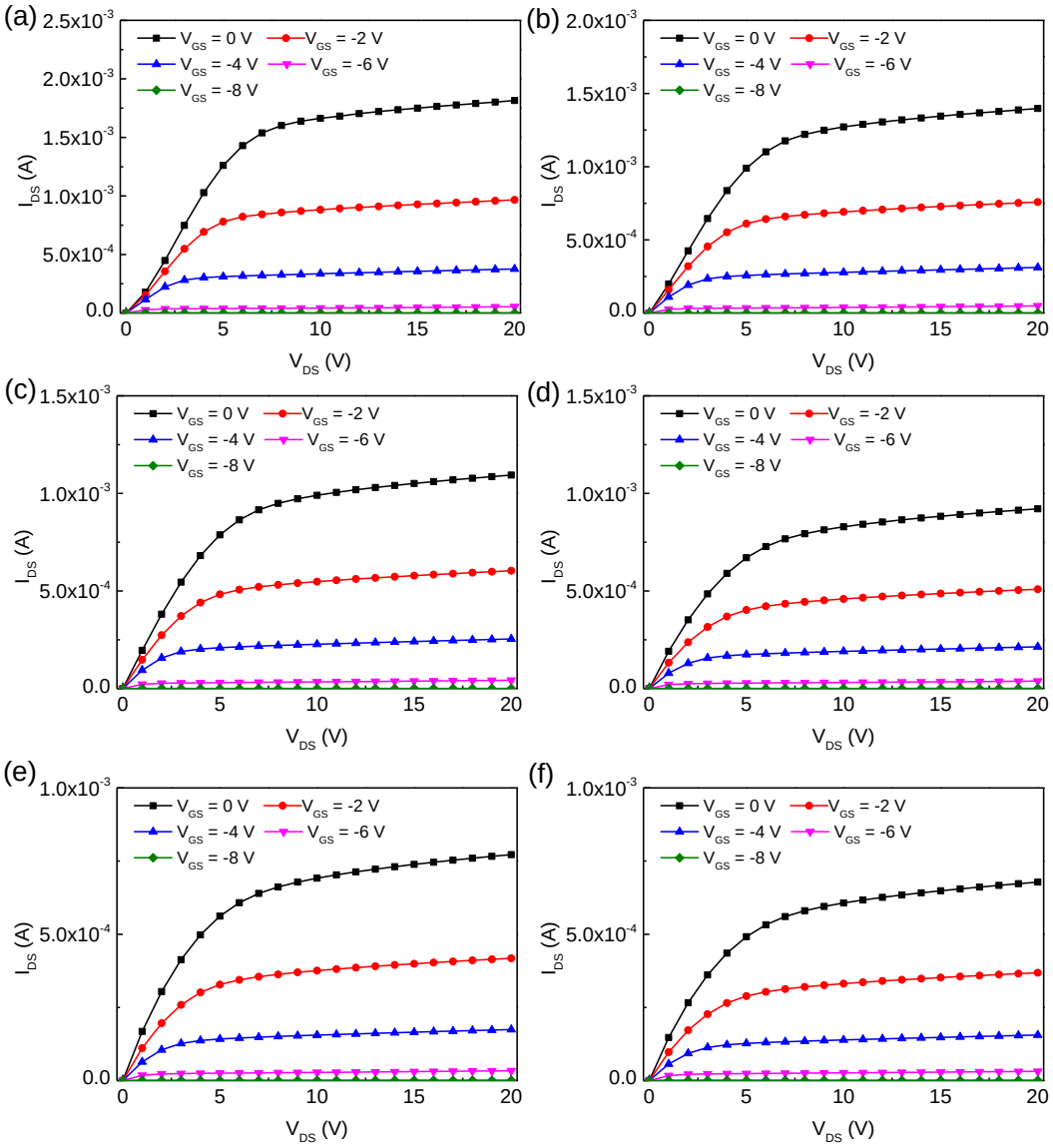

Figure 3.4: I_{DS}-V_{DS} characteristics of a n-channel 4H-SiC MESFET under different V_{GS} and with W/L= 50 µm/2.5 µm (a) at 100 ℃ (b) at 200 ℃ (c) at 300 ℃ (d) at 400 ℃ (e) at 500 ℃ (f) at 550 ℃.

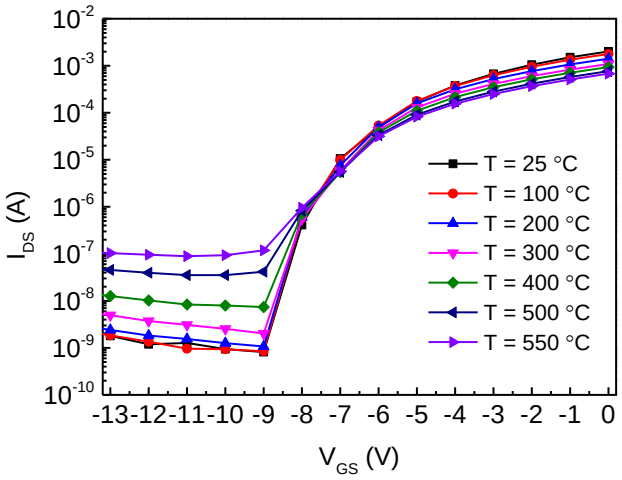

Figure 3.5: I_{DS}-V_{GS} characteristics of a n-channel 4H-SiC MESFET under V_{DS} = 20 V and with W/L= 50 µm/2.5 µm at different temperatures.

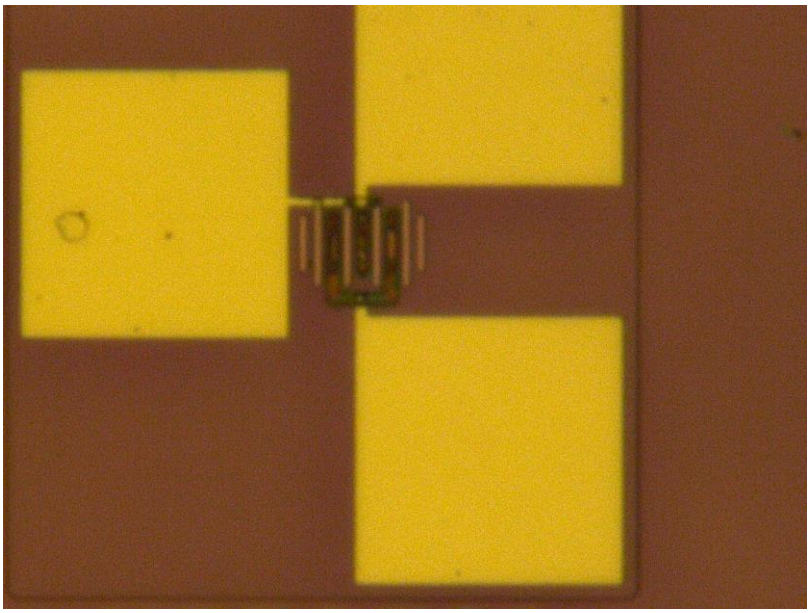

Figure 3.6: Optical image of a n-channel 4H-SiC MESFET after operating at 600 ◦C for few minutes which shows the morphology of interconnect changes.

Figure 3.7 shows the extracted threshold voltage at different temperatures. The V_T is approximately shifted with the rate of -1.03 mV/ ˚C. The temperature dependencies of estimated transconductances based on the equation 3.2 and the intrinsic gain of the MESFET at V_{GS} = 0 V are shown in Figure 3.8. The g_m at 550 ˚C is 3.52 µS/µm, which is 31 % of its value at room temperature. The intrinsic gain of the MESFET decreases with temperature, because the output resistance is increased from 5.22×10^4 to 1.36×10^5 Ω, compensating for the effect of the reduced g_m at high temperatures. The results suggest that 4H-SiC MESFET shows promising performance for high temperature amplifier applications. The complete electrical properties of n-channel 4H-SiC MESFET are listed and summarized in Table 3.1.

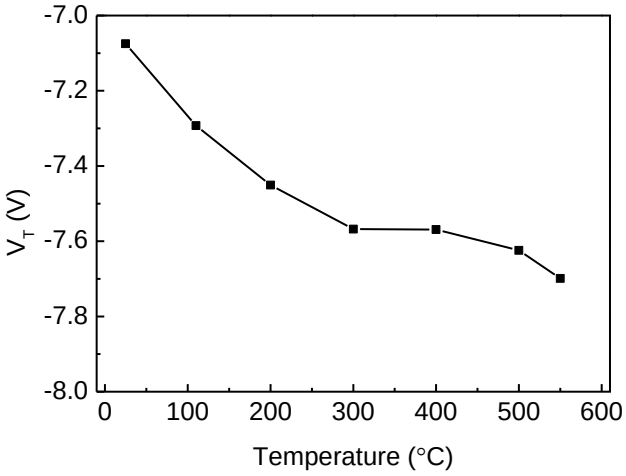

Figure 3.7: Temperature dependence of threshold voltage of a n-channel 4H-SiC MESFET with *W*/*L*= 50 μm/2.5 μm.

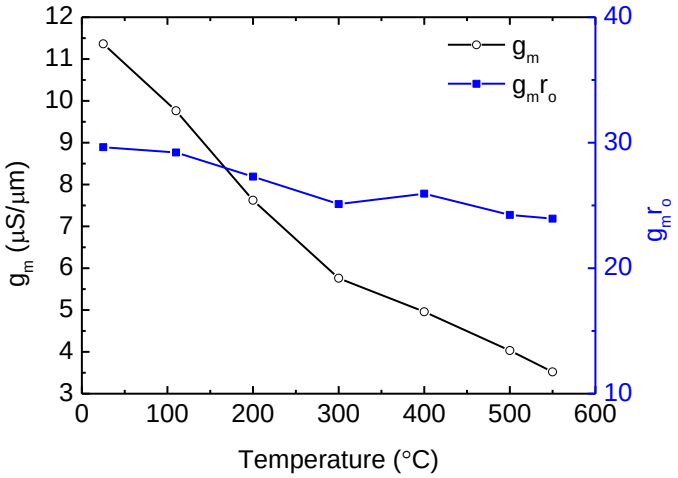

Figure 3.8: Temperature dependence of transconductance and intrinsic gain of a n-channel 4H-SiC MESFET with *W*/*L*= 50 μm/2.5 μm.

Temperature (°C)	V_T (V)	g_m ($\mu S/\mu m$)	R_{on} ($m\Omega$ cm^2)	r_o (Ω)	λ (V^{-1})	$g_m r_o$	I_{Dsat}/I_{off}
25	-7.07	11.36	9.55	5.22×10^4	0.0115	29.6	2.14×10^6
100	-7.29	9.76	10.51	5.98×10^4	0.0112	29.2	1.90×10^6
200	-7.45	7.62	13.59	7.16×10^4	0.0124	27.3	1.13×10^6
300	-7.57	5.76	17.32	8.72×10^4	0.0131	25.1	4.30×10^5
400	-7.57	4.96	20.56	1.05×10^5	0.0130	25.9	1.18×10^5
500	-7.62	4.03	24.62	1.20×10^5	0.0136	24.2	2.18×10^4
550	-7.70	3.52	28.17	1.36×10^5	0.0137	23.9	7.23×10^3

Table 3.3: Extracted parameters of a n-channel 4H-SiC MESFET with W/L= 50 μm/2.5 μm at various temperatures. g_m, R_{on}, r_o , λ and $g_m r_o$ is based on V_{GS} = 0 V. I_{Dsat}/I_{off} is the ratio of current at V_{GS} = 0 V to current at V_{GS} = -9 V.

Chapter 4

Conclusion and Future Work

4.1 Conclusion

This work details the fabrication process of n-channel 4H-SiC MESFET and the device performance is characterized in the temperature range 25 to 550 ℃. The MESFET device is made along with the fabrication process of JFET. The threshold voltage at 25 ℃ is -7.07 V with a high transconductance of 11.36 μS/μm and a small on-resistance of 9.55 mΩ cm^2. As the temperature increases, the threshold voltage shifts with the rate of -1.03 mV/ ℃. Even at 550 ℃, the MESFET still exhibits a transconductance of 3.52 μS/μm and an on/off drain saturation current ratio of 7.23×10^3. The device shows the potential for scaling of the gate length to achieve larger bandwidth of the device while maintain the decent electrostatic characteristics at high temperature.

4.2 Future Work

There are several issues need to be addressed before fully understand the temperature dependencies of 4H-SiC MESFET. The Schottky barrier height of Ti/Ni/TiW/Pt metal gate should be characterized for the entire temperature range. More thermal robust metal interconnect should be explored to further extend the operating temperature to 600 ℃. The RF performance of MESFET such as S-parameters and maximum frequency should also be studied.

Since MESFET reduces one step of epitaxial film deposition to form the pn junction in JFET structure. It might be worth to explore the possibility of complementary MESFET configuration by using both n-channel and p-channel MESFETs.

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