Fully Printed, Flexible, High Performance Carbon Nanotube Top-gated Thin-film Transistors

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Introduction

My research is in the area of printable flexible electronics. The combination of printing techniques from the collaborating group with our group's experience with high purity semiconducting carbon nanotube deposition is the motivation of my work. The goal is to produce fully printable devices with high yield, uniformity, and performance.

My work involves operating an inverse gravure printer to produce fully printable thin-film transistor devices while modifying process variables like carbon nanotube deposition duration, ink dilutions, print speed and pressure, doctoring speed and pressure and drying duration in a systematic manner. The print masks have been pre-fabricated by etching, and from those masks two possible device structures were possible, namely the bottom-gate and top-gate structure, by reversing the order of printing. Of interest is the top-gate structure that allows for the use of the proven way of depositing carbon nanotubes across the whole substrate and having the excess etched. It is simpler, yields, and performs better.

The results obtained from the top-gated devices are reported below in the following work, and it will be submitted for publication in a near identical form with the following authors: Pak Heng Lau, Kuniharu Takei, Chuan Wang, Yeonkyeong Ju, Junseok Kim, Gyoujin Cho and Ali Javey, and it is a collaborative work with the World Class University program at Sunchon National University.

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ABSTRACT - Fully printable flexible transistors are key to high throughput production of flexible electronics at low cost. In this work, the advantages of an inverse gravure printing system and the solution-processing of 99% semiconductor enriched single-walled carbon nanotube (SWCNT) solutions are combined to fabricate fully printable SWCNT flexible top-gated thin-film transistors. The fully printed transistors exhibit high performance with mobility and on/off ratio up to 7.8 cm^2/Vs and 10^4 while remaining stable when bent to 1 mm radius of curvature. With the transistors' high performance, throughput, uniformity, flexibility and stability, we have demonstrated the potential for our printing process scheme to serve as the backplane for future scalable, low cost, high throughput, flexible electronics applications.

KEYWORDS: Flexible electronics • thin-film transistors • semiconducting nanotube networks • printable electronics

Single-walled carbon nanotubes (SWCNTs) have been widely used as a high performance channel material for thin-film transistors (TFTs) with high mobility, high on/off ratio, and low operating voltage.[1,2,3,4,5,6] In addition, SWCNTs are very flexible because they are inherently extremely thin, forming a flexible network when deposited, and various demonstrations including flexible integrated circuits, displays, and sensors using SWCNT TFTs have been shown.[1,5,7,8] The fabrication of the above flexible devices usually rely on conventional photolithography-based microfabrication processes, and are thus limited in scale by the wafer size and have relatively high manufacturing cost. In order to bring to production such flexible electronics in the large area and scale as envisioned for large surface applications, printing has been proposed as a viable low cost solution.[9,10,11,12,13,14] Many advances have been made towards creating high throughput fully printable SWCNT TFTs with performance capable of replicating applications as demonstrated with traditional fabrication methods, focusing on lowering operation power and improving electrical performance. The most important performance metrics for printable transistors are the mobility, stability, operation power and device-to-device uniformity because surface roughness and thickness of printed layers deteriorate electrical performance. Fully printed field-effect SWCNT TFT devices with applications such as radio-frequency identification, D flip-flop, and full adder have been successfully demonstrated using roll-to-roll printing, a very high throughput print process.[15] However, the mobility and on/off ratio and high operation power (20V) of such devices have been limited by the nature of the printed layers. Therefore, to improve those electrical performances, partially printed devices requiring some photolithography processes have been previously demonstrated to be capable of circuitries like ring oscillators.[16]

Furthermore, fully printed SWCNT TFTs using ion-gel dielectrics as gates have also been demonstrated to lower power dissipation,[17] and are capable of driving display applications.[18] However the use of ion-gel dielectrics limit the transistor speed and reliability as compared to directly gated field-effect transistors. However, the exposure of the SWCNTs directly to the surface environment as a consequence of bottom-gate designs is a source of concern for device stability due to the sensitivity of SWCNTs.[19]

In this study, we have demonstrated flexible fully printable SWCNT top-gated field-effect TFTs using only an inverse gravure printing system with high overlay printing registration accuracy of ±10 μm, attaining high electrical performance with superior mobility up to 7.8 cm^2/Vs, while having a low maximum processing temperature of 150 ºC. Combining printing techniques and the use of purified semiconducting SWCNTs[4,7,8] has allowed us to develop a novel process scheme for fabricating high-performance fully printable SWCNT TFTs with respectable performance and device uniformity on large scale flexible substrates. Our process scheme has significant advantage over previous demonstrations in device performance and stability, and printing throughput. It has the potential to be utilized for further demonstrations of circuits with appropriate gravure plates, and be eventually implemented for different applications using it as the starting backplane. The inverse gravure printing system used is adaptable into roll-to-roll printing for even higher throughput production, allowing the demonstrated process to produce low cost, high performance, flexible backplanes for future printable device research and electronics applications.

Figure 1a shows the main steps for fabricating fully printable SWCNT TFTs on a piece of flexible polyethylene terephthalate (PET) film. The film was first cleaned and surface modified with oxygen plasma for 2 minutes.[20] Then the surface was functionalized using Poly-L-lysine solution (0.1% w/v in water; Sigma Aldrich) for 5 minutes by immersion and rinsed by deionized (DI) water to enhance SWCNT adhesion.[7,8,21] The active channel material was deposited by immersion in purified 99% semiconductor enriched SWCNT solution (NanoIntegris, Inc.) for 2 hours. It was then followed by a thorough rinse with DI water, and dried with a nitrogen gun. Most of the deposited SWCNTs in the immersed area would be excess outside the channel area and would be etched away later. The scanning electron microscope image in Figure 1e shows the high density of the SWCNT network uniformly coating the PET substrate as deposited before any printing had been done.

Using the inverse gravure printer shown in Figure 1b with three different gravure plates loaded onto the stage, the source and drain electrodes, gate dielectric, and gate electrode were printed in the respective order. The gravure plates are chrome plated flat copper sheets etched with cells that together form the print patterns. The printer has a dual camera system monitoring the alignment markers on the PET substrate and the gravure plate to make fine adjustments to the stage position and rotation before each print to ensure proper alignment between layers. Inks were dropped onto the plates using pipettes, and doctoring blades spread them evenly into the gravure cells in the plates, with the excess pushed beyond the print contact area. The barrel, with the PET substrate attached, was then lowered to contact the gravure plate with pressure. The barrel clutch was released to allow free rotation for the stage to control the printing speed. The gravure pattern in the plates would finally be printed onto the PET substrate as the stage moves and rolls the barrel across the set printing length. After each layer was printed, the samples were put into an oven at 150 ºC for one minute to cure the inks.

The source and drain electrodes were printed from the first gravure plate using silver nanoparticle ink (PG-007AA; Paru Corporation Korea) directly. Since the silver nanoparticle ink was printed over the deposited SWCNTs, the entire area of the electrodes would be in contact with the SWCNT networks, allowing the electrical contacts to be much better than if the SWCNT networks were printed over the electrodes after the electrodes were printed. The insulator was then printed using high-κ barium titanate nanoparticle hybrid poly (methyl methacrylate) ink (PD-100; Paru Corporation Korea) diluted with dietylene glycol butyl ether (ink to dietylene glycol butyl ether weight ratio: 4-1). Then, the sample was put under oxygen plasma for 2 minutes to etch away excess SWCNTs, using the printed insulator layer as a hardmask. The gate line was finally printed using the same silver nanoparticle ink, diluted with ethylene glycol (ink to ethylene glycol weight ratio: 10-1). Our gravure plates had been prefabricated to print on each substrate a 20×20 array of 400 TFTs, each with a channel length of about 83 μm and width of about 1247 μm. Figures 1c and 1d show optical images of the fully-fabricated 20×20 SWCNT TFTs backplane and the microscope image of one pixel. Ink dilutions, ink doctoring speeds, doctoring blade pressures and angles, and printing pressures and speeds were the main parameters adjusted for each gravure plate and print layer, and will have to be readjusted for different printer systems.

The electrical performance of the fully printed flexible SWCNT TFT that has the best overall performance is presented in Figure 2. The transfer characteristics measured at V_{DS} = -5 V and -1 V is presented in Figure 2a. From that, we extract the on-current (I_{ON}), transconductance (g_m), and current on/off ratio (I_{ON}/I_{OFF}). Using a width of 1247 μm, we can further extract width normalized on-current density (I_{ON}/W) and transconductance (g_m/W), which peaks at 29.1 μA/mm and 3.35 μS/mm respectively at V_{DS} = -5 V. I_{ON}/I_{OFF} is 10^4 at V_{DS} = -5 V. Output characteristics as a function of gate voltage is shown in Figure 2b, confirming ohmic contact is formed between the SWCNT network and printed silver source/drain contacts.

From the transconductance, field-effect device mobility can be extracted. The gate capacitance per unit area (C_{ox}) is assumed using the parallel plate model from capacitance data measured across the insulator. Crossbar structures across the gate dielectric were measured and an average parallel-plate capacitance of 10.84 nF/cm^2 was extracted. Using that as the C_{ox} value, the field-effect device mobility is calculated using the following equation: $\mu_{device} = \frac{L}{V_D C_{ox} W} \cdot \frac{dI_d}{dV_g} = \frac{L}{V_D C_{ox}} \cdot \frac{g_m}{W}$, where L and W are the channel length and width at 83 μm × 1247 μm, V_D = -1 V, and g_m is the transconductance extracted. The mobility extracted at V_{DS} = -1 V is plotted in Figure 2c and it peaks at 7.8 cm^2/Vs. It is worth noting that the parallel-plate capacitance value used is an overestimation of the actual gate capacitance with SWCNT networks in the channel, so the field-effect device mobility as calculated is an undersestimation.[7] In the future, one could perform detailed measurements of the metal-oxide-semiconductor capacitance in the SWCNT channel to obtain a more accurate C_{ox} value, which should result in even higher field-effect mobility. Even so, our fully printable SWCNT TFT is still performing with better mobility and I_{ON}/I_{OFF} than any previously reported fully printable SWCNT TFTs.

Extracting similar data for 100 devices, with a yield of 76%, gives us statistical data on the uniformity of the TFTs fabricated using our fully printable process. Figure 3a shows the transfer characteristics of SWCNT TFTs measured at V_{DS} = -5 V. Figure 3b-e shows the histograms of the statistical variations in threshold voltage (V_{th}), I_{ON}/I_{OFF}, I_{ON}/W, g_m/W, and field-effect device mobility. V_{th} was calculated by locating the max g_m point of each transfer characteristic curve and extrapolating a line tangent to the curve at that point to find the zero crossing voltage. The V_{th}, I_{ON}/I_{OFF}, I_{ON}/W and g_m/W were measured at V_{DS} = -5 V, and the mobility was measured as described above at V_{DS} = -1 V. The best performances measured, from different devices, are I_{ON}/I_{OFF} of 5.7×10^5, I_{ON}/W of 32.2 μA/mm, g_m/W of 5.69 μS/mm, and field-effect device mobility of 9.13 cm^2/Vs. The V_{th} lies in the negative range, making the devices enhancement mode p-FETs, which is desirable from a circuit design point of view. The average of I_{ON}/I_{OFF}, I_{ON}/W, g_m/W, mobility, and V_{th} are 9.6×10^4, 19.5 μA/mm, 2.47 μS/mm, 4.27 cm^2/Vs, and -2.29 V, respectively. As seen from the figures, our printing process is already capable of printing SWCNT TFTs with good uniformity in a noncleanroom environment due to the evenly distributed SWCNT networks from the solution-based processing of the SWCNT active material, and it can only be improved with better processing conditions.

Flexibility is important for covering and conforming to large surfaces, and performance should not be affected or degraded by bending the devices. Due to the inherent nature of SWCNTs being extremely thin and the deposition being of network structures, the active channel is very flexible and its electrical properties should not change. Figure 4a shows a device being measured while bending along the channel length. Transfer characteristics measured at V_{DS} = -5 V while the device was bent down to 1 mm radius of curvature is shown in Figure 4b. The results show that the TFT can be operated without noticeable degradation in performance when bent, and the normalized change in conductance, $\Delta G/G_0$, where ΔG is the change in conductance and G_0 is the conductance at the relaxed state, is shown in Figure 4c. This shows that our fully printable SWCNT TFTs are very suitable to be used to conform to curved surfaces and their edges for applications that require it.

Another advantage of our top-gated process design is the direct passivation of the SWCNTs by the gate dielectric layer rather than directly exposing the carbon nanotubes to air. This may remove the need for a passivation layer to be printed, or otherwise added on top of the devices to protect the active channel. The stability over 1000 measurement cycles is shown in Figure 5, and the effectiveness of the passivation via the insulator can be seen from the stable transfer characteristics, V_{th}, I_{ON}/I_{OFF}, and field-effect device mobility. The results suggest that the devices presented here exhibit superb stability over usage and are ideal for reliable large-area electronics.

In conclusion, we have demonstrated stable top-gated field-effect SWCNT flexible TFTs with high performance using a high yield and throughput fully printable process scheme that incorporates the use of highly purified 99% semiconducting carbon nanotubes as the active channel material. They exhibit excellent mobility (7.8 cm^2/Vs), stability, and uniformity for a fully printed high throughput process scheme. Performance of the devices is expected to be even better in the future with the use of higher purity semiconductor enriched SWCNT solution, with it being available at up to a purity of 99.9% commercially. This process can be used as the backplane for future research on large-scale production of devices with applications via more gravure printing steps, or in combination with other printing techniques to enable the mass production of flexible electronics.

ACKNOWLEDGMENTS

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FIGURE CAPTIONS

Figure 1. Fully printed SWCNT top-gated flexible TFTs on PET. (a) Schematic diagram showing the fully printable process. (b) Image of the inverse gravure printer. (c, d) Optical images of the fully printed 20×20 device array on the PET substrate and optical micrograph of a single TFT. The channel length and width is 83 μm × 1247 μm. (e) SEM image of SWCNT networks deposited on a PET substrate.

Figure 2. Electrical properties of a representative fully printed SWCNT top-gated flexible TFT. (a) Transfer characteristics of SWCNT TFTs measured at V_{DS} = -5 V and -1 V. (b) Output characteristics measured with V_{GS} from -10 to 2 V in 2 V steps. (c) Field-effect device mobility extracted using parallel plate capacitance with C_{ox} = 10.84 nF/cm^2.

Figure 3. Statistical variation in the electrical properties of the fully printed SWCNT top-gated flexible TFTs. (a) Transfer characteristics variation of 66 SWCNT TFTs measured at V_{DS} = -5 V. (b-f) Histograms of Vth, I_{ON}/I_{OFF}, width normalized I_{ON}, and width normalized transconductance measured at V_{DS} = -5 V, and field-effect mobility measured at V_{DS} = -1 V, with channel length and width being 83 μm × 1247 μm.

Figure 4. Flexibility of the fully printed SWCNT top-gated TFTs on PET. (a) Optical image of a TFT under measurement while bent. (b) Transfer characteristics measured at V_{DS} = -5 V for three different bending conditions of relaxed, and bent at 4 mm and 1 mm radius of curvatures. (c) $\Delta G/G_0$ as a function of bending radius of curvature (Relaxed state is infinite curvature radius).

Figure 5. Stability of the fully printed SWCNT top-gated flexible TFTs over 1000 measurement cycles. (a) Transfer characteristics measured at V_{DS} = -5 V for the 1st, 10th, 100th and 1000th measurement cycles. (b-d) V_{th}, I_{ON}/I_{OFF}, and peak field-effect device mobility as a function of measurement cycles up to 1000 cycles.

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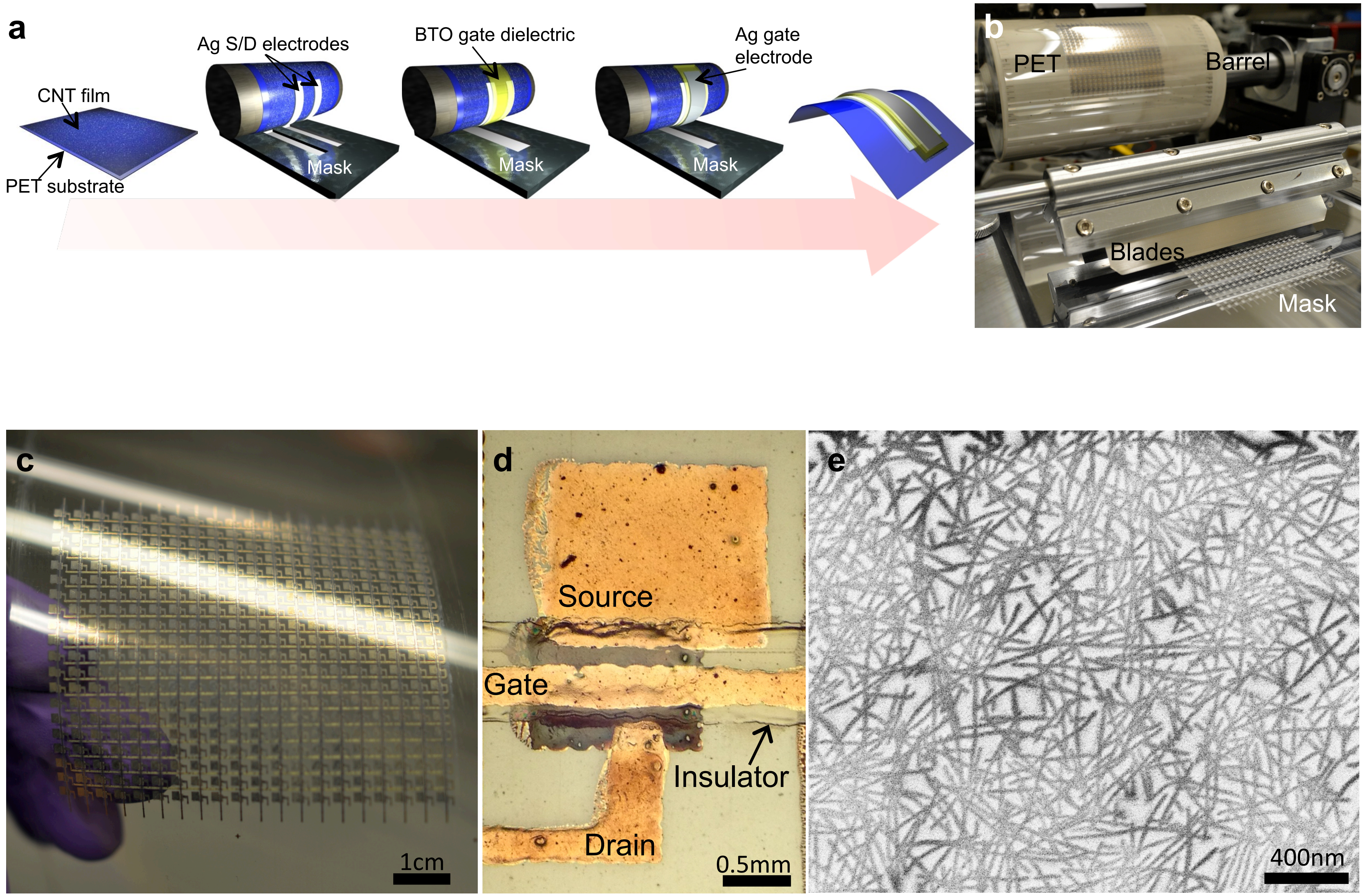
Figure 1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CNT film
PET substrate
Ag S/D electrodes
Mask
BTO gate dielectric
Mask
Ag gate
electrode
Mask
b
PET
Barrel
Blades
Mask
c
1cm
d
Source
Gate
Insulator
Drain
0.5mm
e
400nm

Figure 2

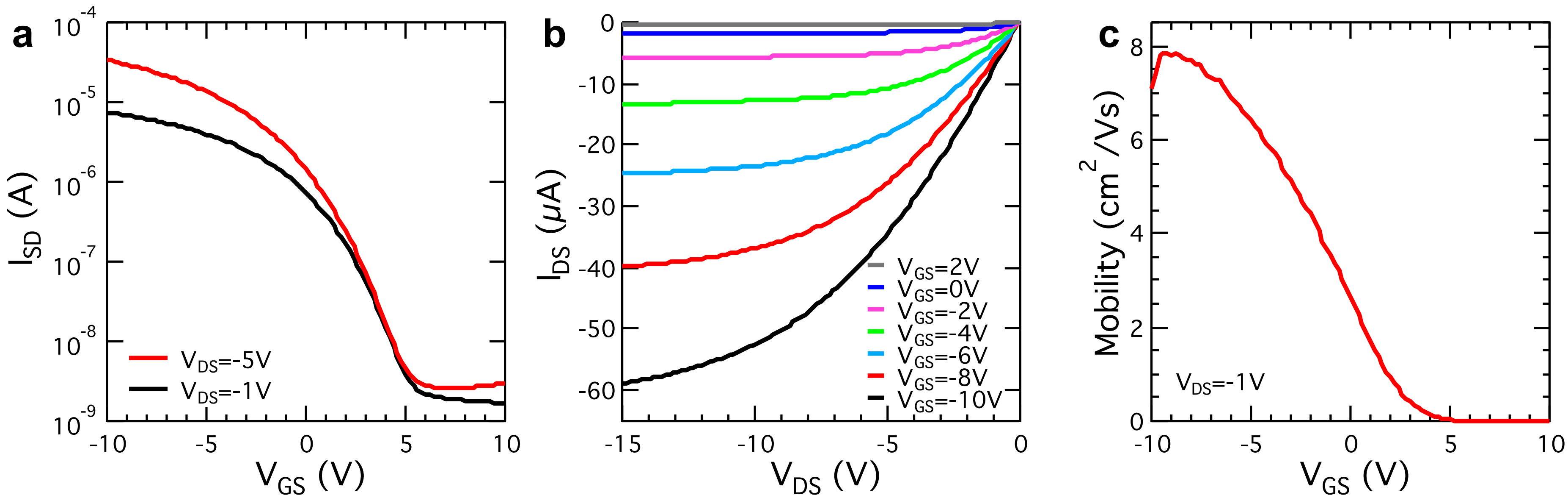

a
b
c
I_{SD} (A)
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
V_{DS}=-5V
V_{DS}=-1V
V_{GS} (V)
I_{DS} (μA)
V_{GS}=2V
V_{GS}=0V
V_{GS}=-2V
V_{GS}=-4V
V_{GS}=-6V
V_{GS}=-8V
V_{GS}=-10V
V_{DS} (V)
Mobility (cm^2/Vs)
V_{DS}=-1V
V_{GS} (V)

Figure 3

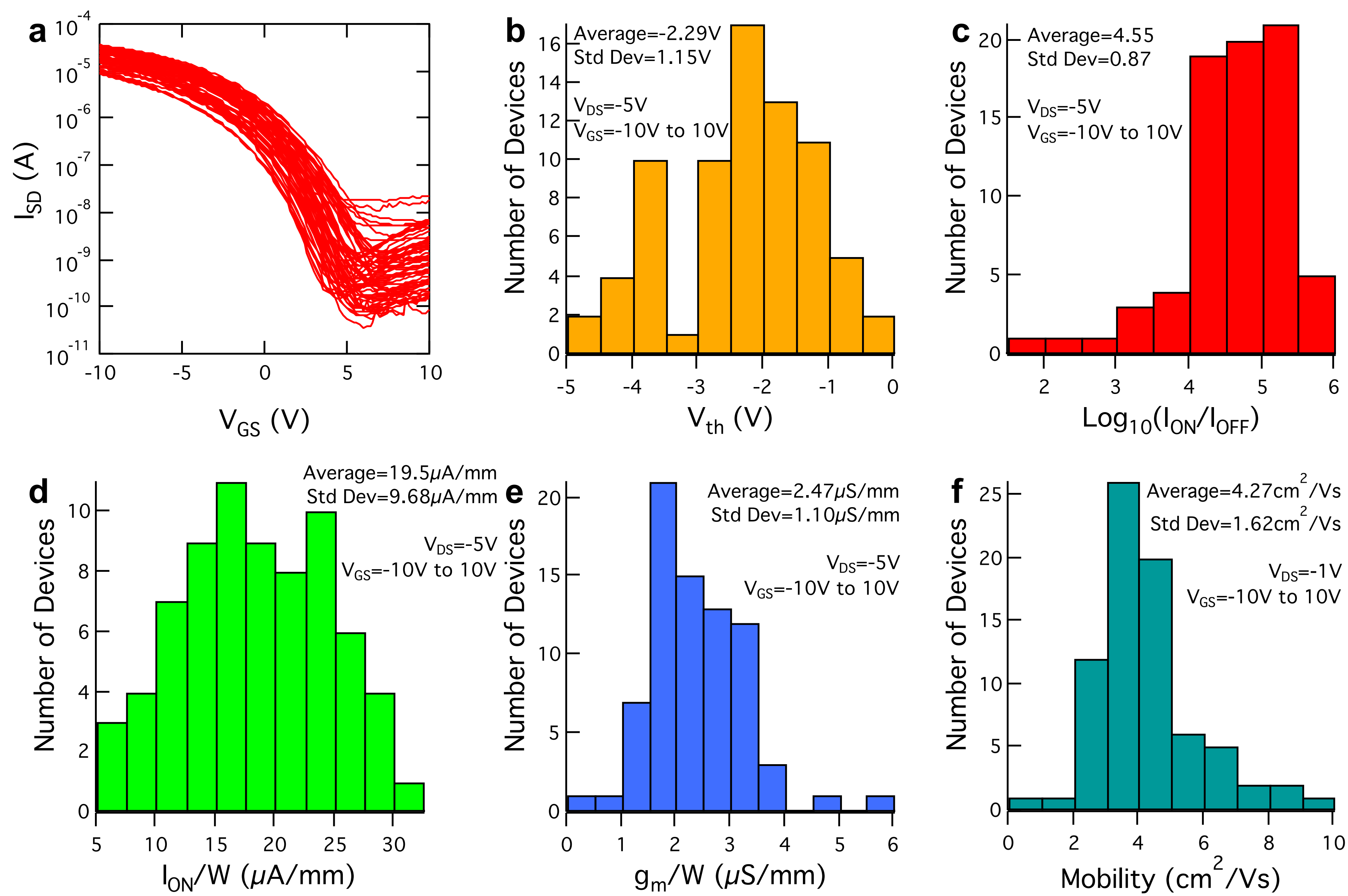

a
b
c
d
e
f
I_{SD} (A)
V_{GS} (V)
Number of Devices
V_{th} (V)
Average=-2.29V
Std Dev=1.15V
V_{DS}=-5V
V_{GS}=-10V to 10V
$Log_{10}(I_{ON}/I_{OFF})$
Average=4.55
Std Dev=0.87
I_{ON}/W (μA/mm)
Average=19.5μA/mm
Std Dev=9.68μA/mm
g_m/W (μS/mm)
Average=2.47μS/mm
Std Dev=1.10μS/mm
Mobility (cm^2/Vs)
Average=4.27cm^2/Vs
Std Dev=1.62cm^2/Vs
V_{DS}=-1V

Figure 4

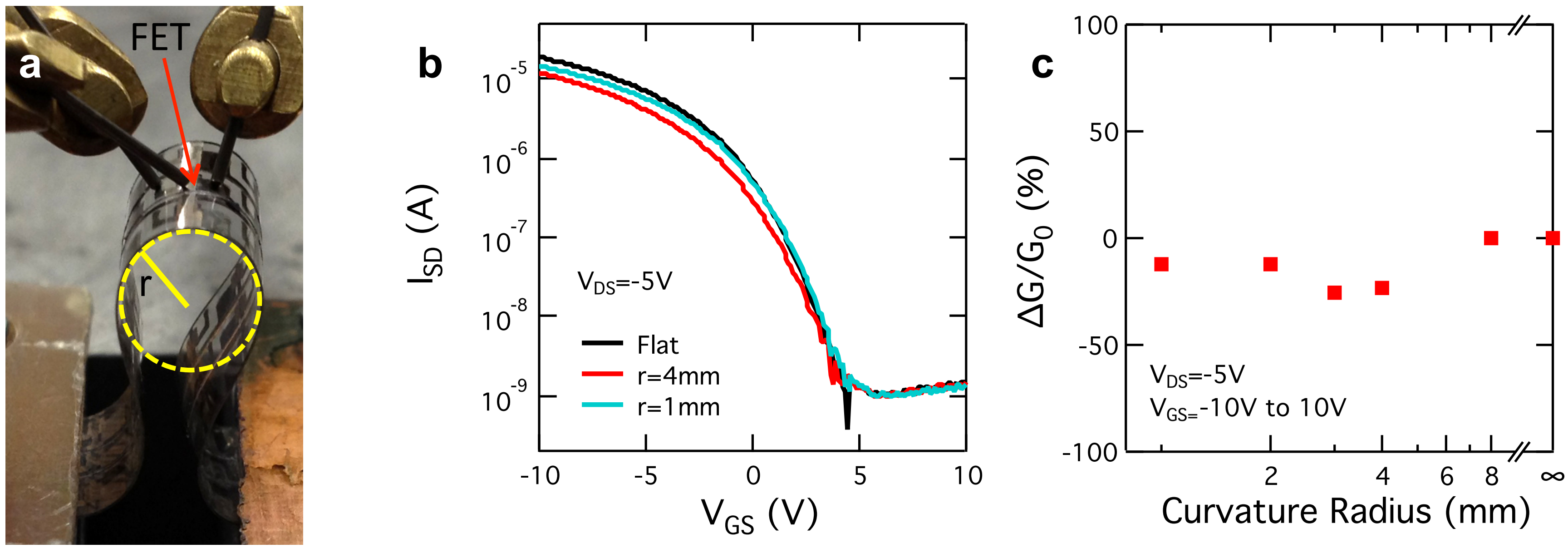
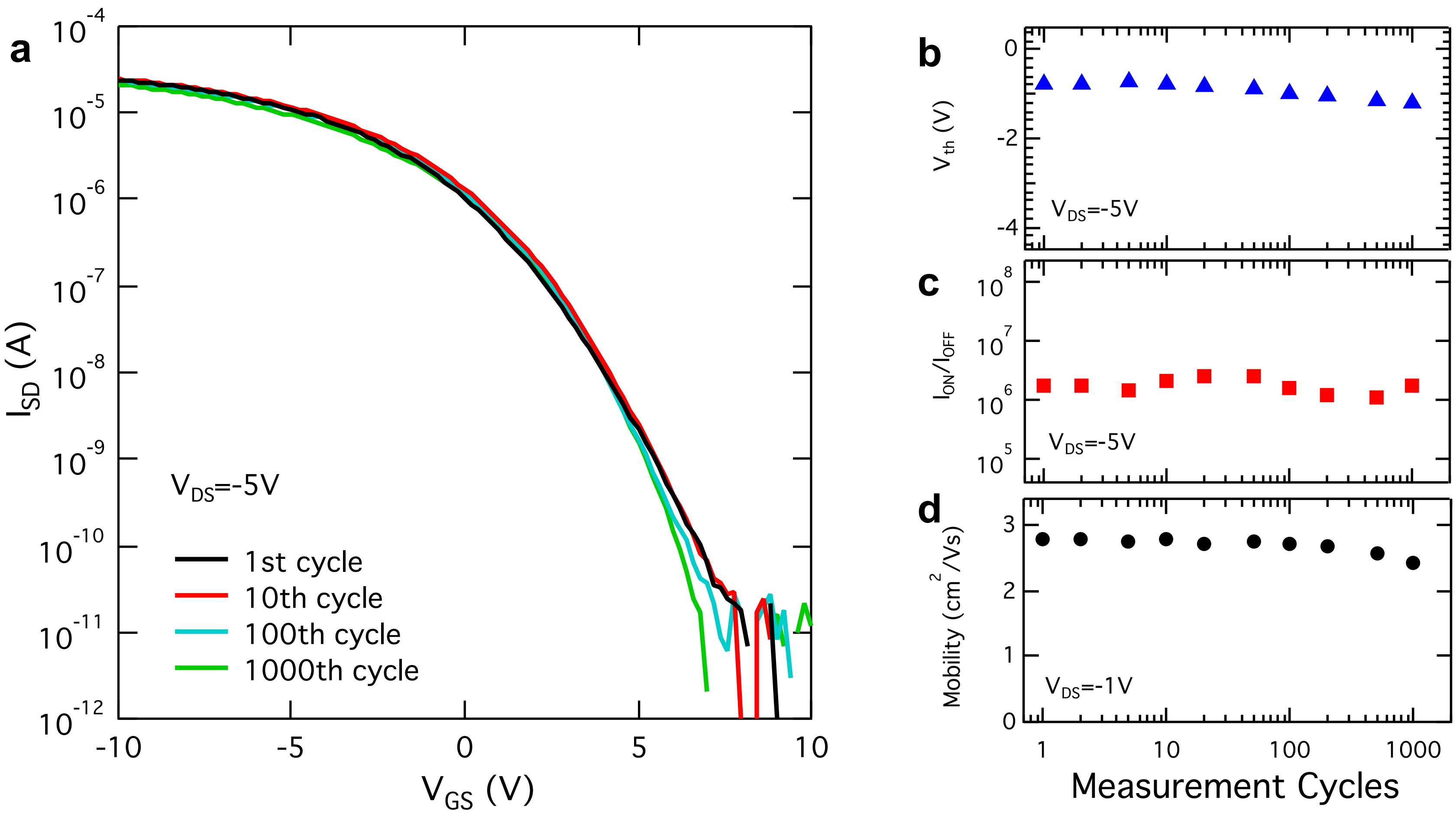

a
FET
r
b
I_{SD} (A)
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
V_{DS}=-5V
Flat
r=4mm
r=1mm
-10
-5
0
5
10
V_{GS} (V)
c
$\Delta G/G_0$ (%)
100
50
0
-50
-100
V_{DS}=-5V
V_{GS}=-10V to 10V
2
4
6
8
∞
Curvature Radius (mm)

Figure 5



a
b
c
d
I_{SD} (A)
V_{GS} (V)
V_{DS}=-5V
1st cycle
10th cycle
100th cycle
1000th cycle
V_{th} (V)
I_{ON}/I_{OFF}
Mobility (cm^2/Vs)
V_{DS}=-1V
Measurement Cycles