Transparent Micro-electrocorticography (ECoG) Arrays for Optogenetic Mapping of Surface Potentials

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Contents

1 Motivation

The electrical activity of the brain has been a compelling way to measure and quantify neural activity since Hans Berger recorded his original electroencephalograms in the late 1920s [1]. Today, in addition to the electroencephalogram (EEG), there are many other ways to record the electrical activity of the brain, differing mainly in spatial-temporal resolution[1] and spatial coverage. For recording over large cortical areas the scalp EEG remains the most practical solution, although due to the natural filtering characteristics of the scalp, large electrode sizes, and distance from the cortex inherent in the measurement EEG is extremely limited in spatial resolution and only able to capture signals below approximately 60Hz [2], [3]. For measuring the high frequency (>1 kHz) characteristic of action potentials in individual neurons, known as single unit activity (SUA) and multi-unit activity (MUA), a wide array of penetrating probes have been designed to push a recording electrode as close to an individual neuron or group of neurons as possible [3], [4]. However, these types of probes are usually very limited in terms of coverage of the brain, generally recording from fewer than 250 neurons [4], [5]. Lying in between these two modalities is a technique known as Electrocorticography (ECoG), which consists of laying an electrode directly on the brain, either above or below the dura [3], [6]. ECOG recordings provide a compromise in resolution and coverage, able to record signals up to 500 Hz (known as the local field potential, or LFP) and covering up to about 25% of the human cortex [7].

ECOG has been used for decades clinically to help localize epileptic seizures but has only recently come into vogue as a potentially useful imaging and recording modality. In addition to efforts to visualize brain activity in new ways many groups have explored the potential of utilizing ECOG for brain-machine interface (BMI) applications, where it's combination of moderate resolution and relative non-invasiveness compared to penetrating electrodes is attractive [6], [8]. This change has partially been driven by the development of new micro-electrocorticography (μECoG) arrays which take advantage of modern surface micromachining techniques to achieve extremely dense electrode arrays packed with tiny (<500μm diameter) electrodes [9–16]. These types of arrays can be used to image phenomena not possible with larger electrodes, such as highly localized spindle waves in the cortex [14]. However, because μECoG is still a relatively new technology, there is little agreement in the scientific community about what the surface LFP signals recorded by μECoG electrodes represent, especially for electrode diameters smaller than 200μm [3], [17]. The assumptions behind popular models for EEG signals break down at such small scales [18], [19], and it is not yet clear what aspect

[1] In terms of measuring electrical activity, spatial and temporal resolution are very closely related due to the increased probability of high-frequency activity in a given measurement area being asynchronous as the size of the measurement area increases [2].

of the models that exist for depth LFPs apply to the recordings made on the cortical surface [3], [17], [20–23]. For example, there is considerable disagreement over where the gamma-band oscillations viewed in many cortical recordings originate from, with some claiming layer 5 output neurons and some claiming layer 2-3 pryamidal cells [3], [17], [21].

In order to better understand the nature of the signals recorded by µECoG arrays it would be helpful to be able to use modern optical techniques, such as optogenetics, to be able to selectively activate cells in the recording area of the µECoG array [24], [25]. Such experiments could provide valuable insight into the origin of µECoG signals and the mechanisms by which they are generated. To this end, µECoG may be improved by taking advantage of the transparent µECoG array technology developed at the University of California, Berkeley, where the electrodes are manufactured out of a transparent conductive film of indium-tin-oxide (ITO) [26]. Devices manufactured in this technology have a transparent window which includes the electrode array, allowing light to image or stimulate areas directly beneath the electrodes, and thus opening up the possibility for a new class of hybrid optical/electrical experiments, studies, and systems.

This work presents in detail the design, fabrication and testing of the transparent µECoG arrays including verification of impedance, transparency, and electrical properties. These arrays have the smallest electrodes to date of any µECoG array, transparent or otherwise, enabling higher spatial-temporal resolution than previous devices. This work also extends previous work by plating the ITO electrodes with the transparent conductive polymer PEDOT [27] in order to improve electrochemical impedance properties and characterizing the results. The intent of the author is that this work can function as detailed instruction manual for designing, manufacturing, and testing µECoG devices made with transparent electrode technology. The work ends by describing next steps for utilizing the transparent µECoG arrays in research on the origin of µECoG signals in the cortex, combining optogenetics with holographically patterned light sources.

2 Design and Manufacture

The transparent µECoG arrays presented in this work are similar to the arrays presented in [26], with the main changes being 1) smaller and more tightly packed electrode geometries, 2) improved referencing, and 3) the plating of the transparent conductive polymer Poly(3,4-ethylenedioxythiophene) or PEDOT in order to improve electrode impedance characteristics. The following subsections detail the material considerations for the device, the geometrical layout for the photolithography masks, the surface micromachining process utilized for fabricating the devices, and visual results from the finished devices.

2.1 Materials

Materials considerations for the transparent µECoG presented in this work are influenced by the choices made in [26], and differentiate this work from that of other µECoG arrays [12–14], [28].

Parylene C is used as the substrate for the µECoG array for several reasons, primarily because it has been shown to be an excellent barrier for moisture, with no pinholes even at relatively small thicknesses [26], [29]. Parylene C also has advantages as a low cost coating which can be deposited at low temperature, and is often the coating material of choice for biomedical implants [30–32]. In order to improve the conductivity of the ITO electrodes, PEDOT can be plated without significantly compromising the transparency or biocompatibility of the original material [27].

For the electrode material, indium tin oxide (ITO) was chosen for its combination of transparent, conductive, and biocompatibility properties [33]. For the traces and bond-pads to the breakout printed circuit board (PCB) a platinum-gold-platinum stack was selected. Platinum has been shown to be a good adhesion layer for parylene, and gold is both flexible and can be easily deposited at a low temperature which is compatible with the parylene substrate [12].

2.2 Layout

The overall design of the transparent µECoG arrays presented in this work are similar to previous designs with an electrode array connected to a bondpad array for a breakout PCB by a flexible cable with metal interconnect [12], [26]. Two of the main elements which distinguish the work presented here from previous work are a more densely packed array with smaller electrodes and improved referencing. The more densely packed array with smaller electrodes is important because of the brittle nature of ITO, which causes the material to fracture under stress [26], [33]. The smaller electrodes and shorter traces are less likely to experience large stress gradients, and thus are more robust. The smaller electrodes should have the additional advantage of reducing the

amount of spatial averaging of the LFP signals at the electrodes, allowing for higher spatial resolution and a greater amount of high-frequency data in the output signal [3], [20], [34].

The layout used to define the photolithography masks used for this work is shown in Figure 2.1 - Figure 2.6. In these figures, the red layer defines the Pt/Au/Pt metal stack and the blue layer defines the ITO. The transparent cross-hatched layers define etch holes for opening the top layer of parylene to the outside of the probe (see subsection 2.3). This layer also defines the outlines of the arrays. Note that Figure 2.1 and Figure 2.2 show two slightly different versions of the array. The layout shown in Figure 2.1 has rectangular etch holes drawn between the electrodes intended to reduce the stiffness of the array and thus improve adhesion to the brain. The layout in Figure 2.2 leaves out these holes, allowing for an array that is easier to handle and install on the brain. The trade-offs between the two styles will be evaluated as experiments progress. Both layouts show a wrap-around referencing electrode defined in the metal layer. The positioning and size of this electrode should allow for a low-impedance, low-noise reference source compared to previous work [26].

Key geometrical parameters for the µECoG arrays presented in this work are shown in Table 2.1. While the majority of arrays were manufactured with 5mil bondpads at 10mil pitch as shown in Figure 2.5, a subset of the arrays shown on the wafer-level layout in Figure 2.4 have 3mil bondpads with 6mil spacing. This was done to investigate the feasibility of using the smaller-sized bondpad arrays for future projects, such as those smaller headstages for chronic recordings.

The masks were ordered as dark-field soda-lime glass 5" masks, direct-write chrome from Fineline Imaging http://www.fineline-imaging.com/. The minimum feature size on the masks is 10µm. All layout work was done in L-Edit from Tanner EDA under license from the Marvell Nanolab http://www.tannereda.com/products/l-edit-pro.

Table 2.1 – Geometrical parameters for transparent µECoG arrays

Number of Electrodes	64
Electrode Pitch	120µm
Electrode Diameter	40µm[2]
Transparent Window Size	1mm x 1mm
Cable Length	20mm
Bondpad Width/Pitch	5mil/10mil

[2] An approximate value since the ultimate electrode diameter is defined by timing of the oxygen-plasma parylene-opening etch described in subsection 2.3.

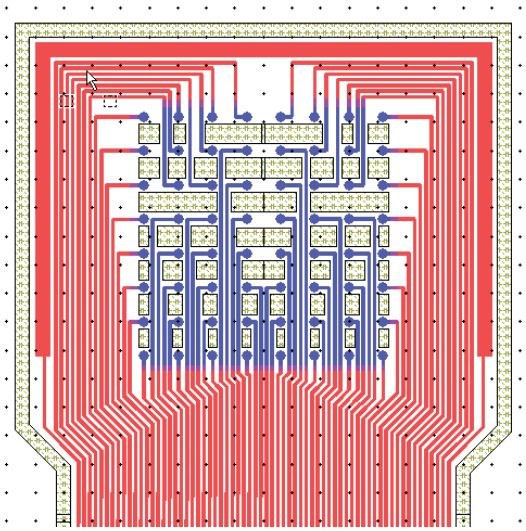


Figure 2.1 - Detail of electrode array showing referencing electrode and interconnect

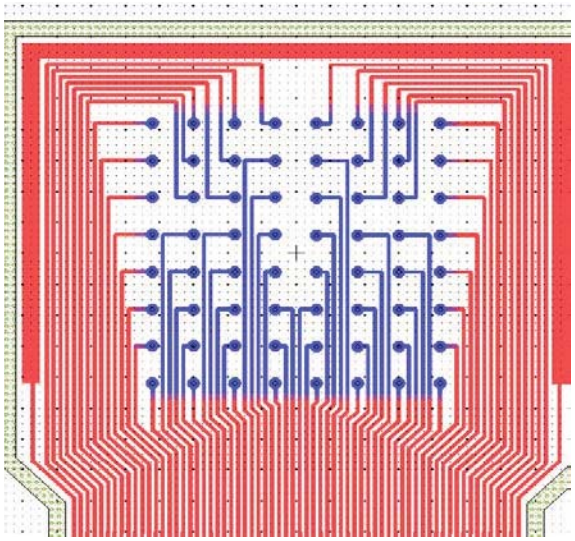


Figure 2.2 - Alternative design for electrode array without etch holes inside the array window

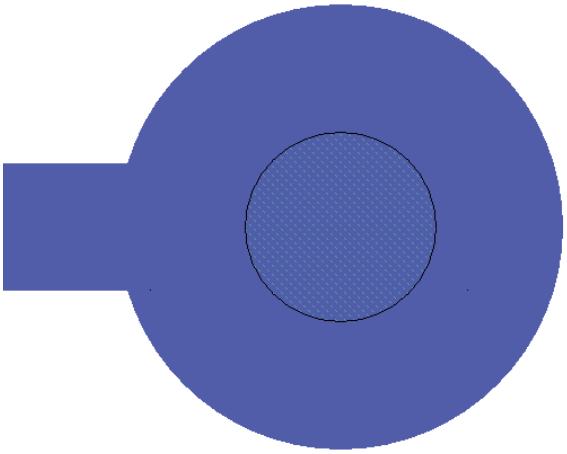


Figure 2.3 - Detail of a single electrode showing definition of mask opening for etching vias

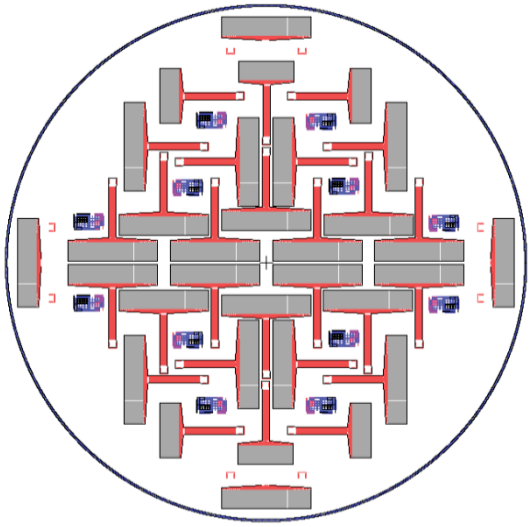


Figure 2.4 - Wafer-level layout showing 5mil and 3mil versions of devices

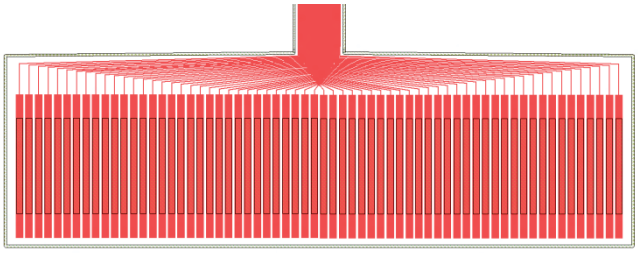


Figure 2.5 - Fanout for bond-pad array showing 5mil width

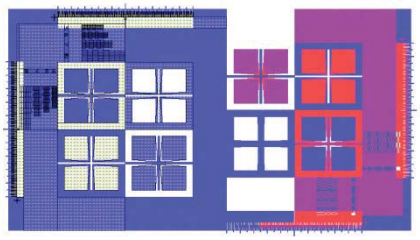


Figure 2.6 - Alignment marks used for10µm alignment

2.3 Process

The surface-micromachining process used to fabricate the µECoG arrays presented in this work is similar to those presented in [12], [26], where lift-off is used to pattern conductor layers between two layers of parylene, and an oxygen plasma etch is used to expose vias on one side of the device and to etch the device outline.

A detailed schematic of the process is presented in Figure 2.7. After cleaning the carrier wafer (Step 1) Parylene C is deposited at a thickness of ~3µm using a Specialty Coating Systems Parylene Deposition System 2010 with the parameters listed in Table 2.2 (Step 2). After coating the wafer with Hexamethyldisilazane (HMDS) in a quick-pump oven process the wafer is the prepared for lift-off using a bilayer photoresist method (Step 3). This step is shown in more detail in Figure 2.7 [35]. First, G-line photoresist was spun at 5000rpm to achieve a thickness of 1.3µm, followed by a 60 second bake on a hot plate at 90°C and 6 seconds on a chill plate. The G-line resist was flood-exposed using a Karl

Table 2.2 - Parylene C Deposition Parameters

Furnace Temperature	690°C
Chamber Temperature	135°C
Vaporizer Temperature	175°C
System Base Pressure	9 mTorr
System Operating Pressure	34 mTorr
Parylene C Mass	13 g

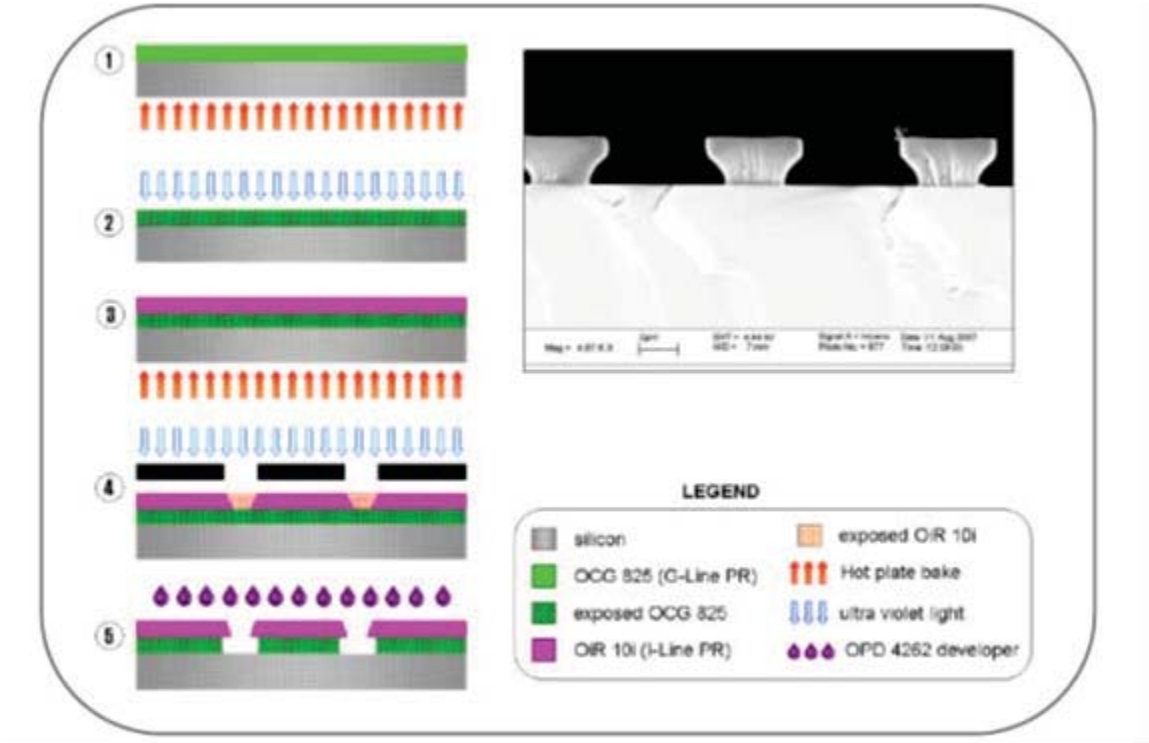
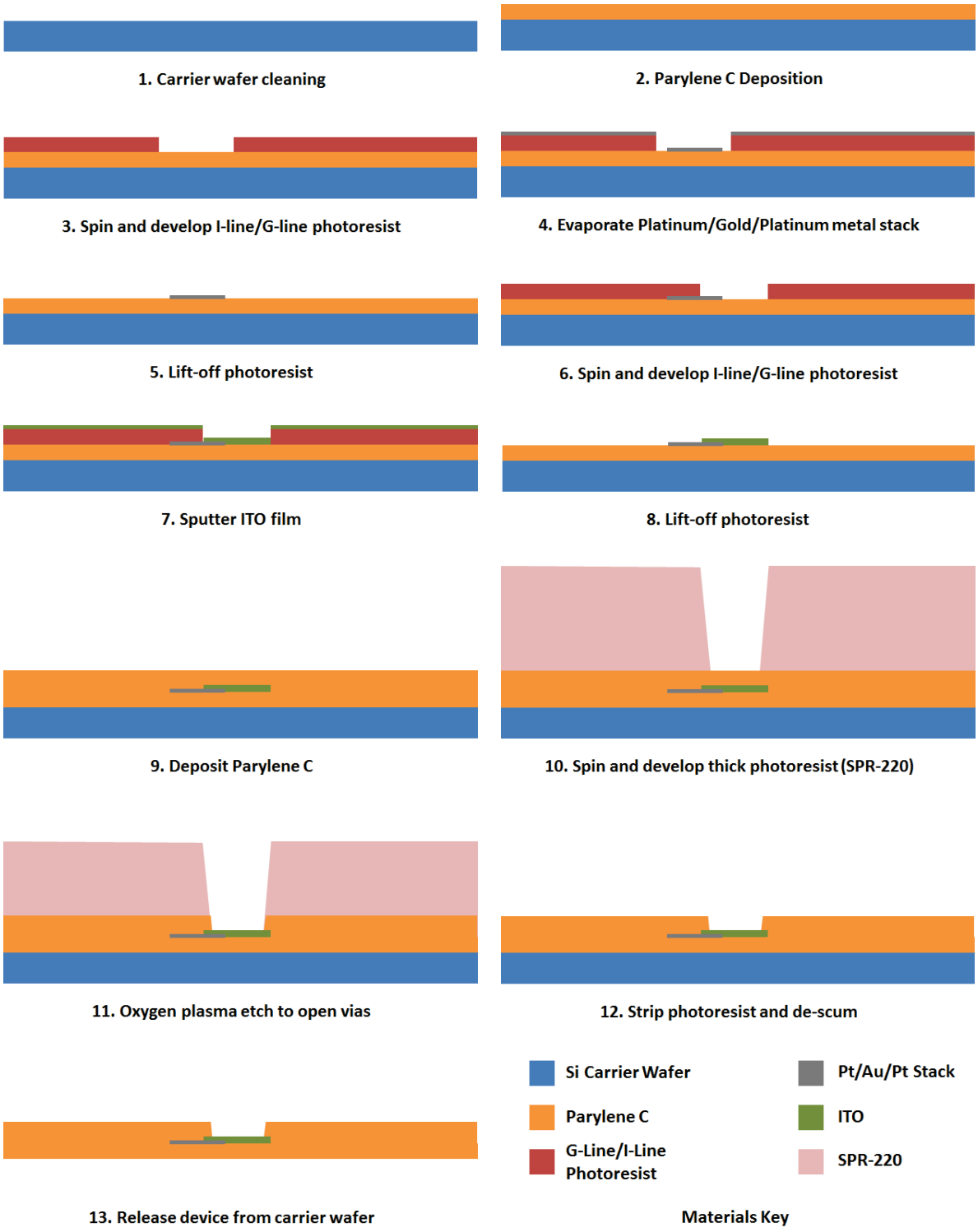


Figure 2.7 - G-line I-line Bilayer Method Process Flow
http://nanolab.berkeley.edu/labmanual/chap1/1.3processmods.pdf

Figure 2.8 - Surface micromachining process for transparent µECoG arrays



Suss MA6 Mask Aligner (KSA). Following this a layer of I-line photoresist was spun on the wafer at 4000 rpm for a thickness of 1.2µm, baked for 60 seconds at 90°C, and chilled for 6 seconds. The I-line photoresist was then exposed through the mask for the metal layer using the KSA. Finally, the photoresist was developed in OPD 4262 developer, which develops both cross-linked I-line and cross-linked G-line photoresist. This is a timed develop, and is the critical step in the process. The timing of the develop varies from 40-50 seconds depending on variations in the process, with the goal of reaching a "scallop" in the G-line resist of 1-2µm (see Figure 2.7). If the wafer is under-developed, then the scallop will be too small and the liftoff will likely be incomplete as metal will adhere to the resist sidewalls. If the scallop is too large, it can interfere and completely eliminate smaller features on the wafer, especially the interconnect tracks between the µECoG array and the bondpads, which have the critical dimension of 10µm. As such, great care must be taken to ensure a correct development time.

Following the preparation of the bilayer photoresist stack and a 20 second descum etch in oxygen plasma (200W RF, 80sccm O_2, Plasma-Thermal Parallel Plate Plasma Etcher), a 10nm/200nm/10nm Pt/Au/Pt stack was evaporated in a single run through a CHA Solution E-beam Evaporator at a base pressure of $1e^{-6}$ Torr (Step 4). The deposition settings used for Au and Pt are shown in Table 2.3. Note that the deposition rate for platinum was set extremely low to 0.1A°/s. This is because the CHA evaporator does not have a cryo-cooled chuck, and in order to keep the parylene C substrate from cracking it was necessary to minimize the temperature allowed inside the chamber, i.e. minimize the deposition rate for platinum. Following deposition the metal was lifted off in a 30 minute ultrasonic acetone bath (Step 5). To deposit the ITO layer, the process described above for bilayer liftoff was repeated, exposing the I-line using the mask for the ITO layer (Step 6). After a descum etch in oxygen plasma, the ITO was sputtered in a Edwards Auto 306 DC and RF Sputter Coater in 2.2mTorr Argon from a base pressure of $4e^{-5}$ torr (Step 7). The deposition took 33 minutes (50W DC, ITO target), and resulted in a layer thickness of 110nm. The ITO was lifted off in a 30 minute ultrasonic acetone bath, followed by another descum etch to get rid of all remaining photoresist residue (Step 8).

Table 2.3 - Deposition settings for metal stack

Setting	*Platinum (Pt)*	*Gold (Au)*
Gun Power	MID	MID
Sweep Pattern	TWO	ONE
Ion Mill	OFF	OFF
Max Deposition Rate	0.1A°/s	10A°/s
Max Power Reached	59.11%	42%

Following the liftoff of the ITO a second layer of parylene C was deposited using the parameters from Table 2.2 (Step 9). This was followed by spinning think (10µm) SPR-220 photoresist onto the wafer, exposing in the KSA using the mask for etching vias, and developing in MA-26 for 5 minutes (Step 10). Spinning thick resist is necessary because the resist has a ~1:1 selectivity for the plasma etch which is used to define vias and etch device outlines (~6µ of parylene C). The procedure for preparing the thick resist begins with coating the wafer with Hexamethyldisilazane (HMDS) in a quick-pump oven process. Next, SPR-220 is spun onto the wafer at 1800rpm, yielding ~10µ of resist. The wafer is then baked on a hot plate for 300 seconds at 115°C before being allowed to cool and exposing using the KSA. After exposure, the wafer is held for 30 minutes prior to performing a post-exposure bake (115°C for 6.5 minutes). The wafer is allowed to completely cool before the tank develop in MA-26. After developing the wafer, the resist is hard-backed at 80°C for 120 minutes to help maintain the critical dimensions and sidewall profiles during etching [35].

To complete the process, the wafer is etched for 20 minutes in oxygen plasma using a Plasma-Thermal Parallel Plate Plasma Etcher (200W RF, 70 sccm O_2) in order to etch vias over the electrodes and bondpads and to etch the device outlines (Step 11). This etch time was reached using a 30 seconds on/30seconds off etch profile in order to keep the wafer from overheating (40 minutes total machine time). Following the etch, the photoresist is stripped from the wafer in a 1 minute acetone bath followed by a IPA rinse and a descum etch in oxygen plasma (Step 12). Finally, the wafer is allowed to sit in an overnight bath of DI water mixed with a few drops of detergent (liquid dish soap) in order to release the devices (Step 13). After release the devices are stored in an IPA bath as shown in Figure 2.9. Note that the devices are too fragile to handle with metal tweezers and are also vulnerable to electrostatic force, and so they must be handled exclusively with plastic anti-static tweezers (pictured in Figure 2.9). The finished devices should be stored in IPA until they are ready to be bonded to the back end assembly in order to minimize damage and keep the devices clean.

Figure 2.9 - Device release and IPA soak. Note that the devices in the photo were from a wafer that was under high stress during the process, and so they are more tightly curled than normal.

Images of finished devices (before final release) are shown in Figure 2.10 - Figure 2.15. The bright areas on the images indicate areas where the parylene has been etched through to bare silicon. All images were taken with an Olympus LEXT OLS3000 3D Laser Confocal Microscope.

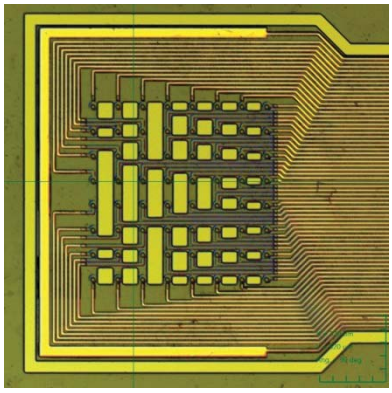


Figure 2.11

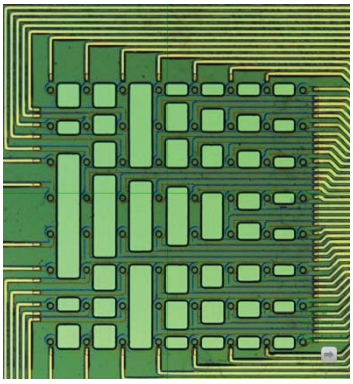


Figure 2.12

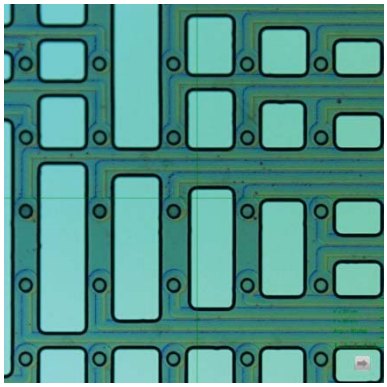


Figure 2.13

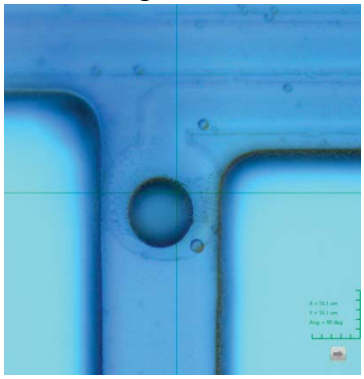


Figure 2.14

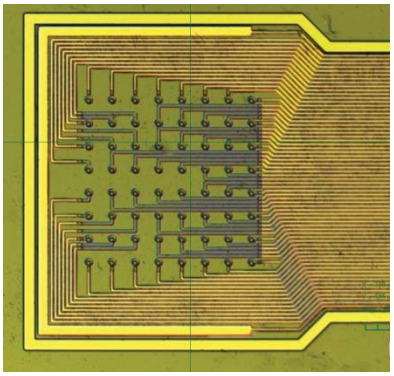


Figure 2.15

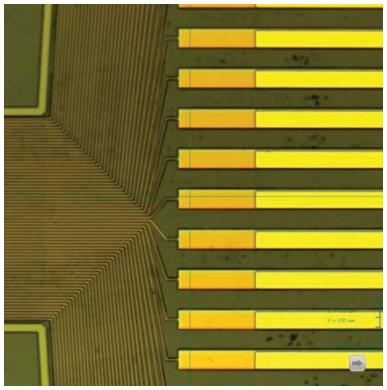


Figure 2.16

2.4 Back-end Fabrication

In order to interface the transparent µECoG arrays with commercial electrophysiology amplifiers it is necessary to develop PCB breakout adapters. For this work, a PCB was designed to interface with a ZC64 or ZC64-LED - 64 Channel ZIF-Clip® head-stage from Tucker Davis Technologies http://www.tdt.com/products/ZIF_heads

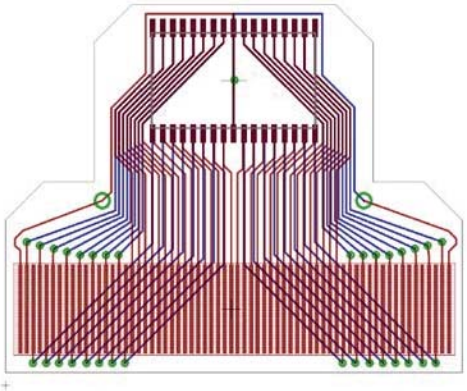


Figure 2.10 - PCB Layout for interfacing with ZIF64 head-stage

tages.htm#ZC64. The finished PCB design utilizes the DF30FC-34DS-0.4V(82) from Hirose and is shown in Figure 2.16 (minimum feature size of 5mil).

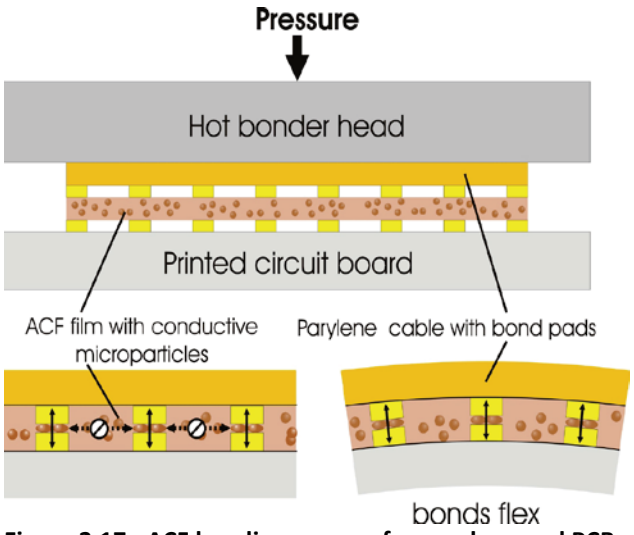


Figure 2.17 - ACF bonding process for parylene and PCBs (image source, Peter Ledochowitsch, personal communication).

The transparent µECoG arrays are bonded to the PCBs using a thermo-compressive anisotropic conductive film (ACF) process. The basic principles of the process are shown in Figure 2.17. A strip of ACF is placed between bond pads on the parylene C cable and the PCB, and with the application of pressure and heat the conductive microparticles in the ACF will form a conductive bond with the bondpads while maintaining an insulating character in between the bonds. Once the bond is formed, it is robust to flexure and egress from moisture and dust particles.

The detailed process of bonding the individual devices to their breakout PCBs is depicted in Figure 2.18 - Figure 2.21 and is similar to the process reported in [26], with differences primarily in the details of the bonding parameters . First, a ribbon of ACF (3M 5552R, 2mm wide) is pre-bonded to the PCB. This is done using an Ohashi HMB-10 table-top bonder equipped with a 2.5mm bond head (5s, 90°C, 5kg/cm^2). Note that, in order to achieve the temperature of 90°C at the bond site, the bond head itself needs to be considerable hotter. For the setup in this work, the temperature setting for the bond head was 120°C. Next, a device is transferred to a glass slide, as show in Figure 2.18 and Figure 2.19. Note that IPA can be used to promote stiction of the device to the slide, and that the device must have its bondpads exposed at this point (i.e. not touching the glass slide) for the process to proceed correctly. Once transferred to the glass slide, the device bondpads can be brought into alignment with the bondpads on the PCB under a microscope. Although this procedure was performed by hand for this work, in practice it could be done using micromanipulators to improve reliability. Once aligned, the device is tacked into place using a hot soldering iron (160°C) glass slide through the as show in Figure 2.20. The glass slide is carefully removed from the device, and the HMB-10 tabletop bonder is once again used to make the final bond (25s, 180°C, 40kg/cm^2).

Figure 2.18 – Removing µECoG array from IPA bath and placing on glass slide

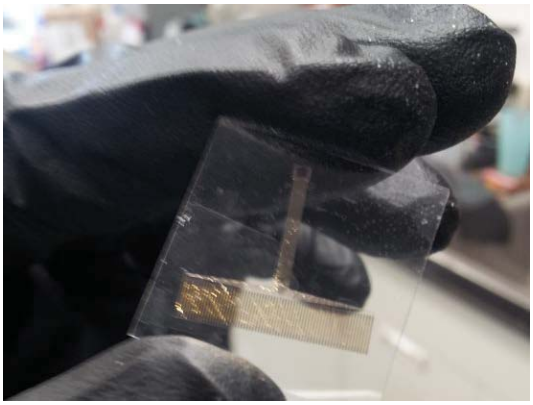


Figure 2.19 – µECoG array mounted on glass slide

Figure 2.20 – Tacking µECoG array to PCB with soldering iron

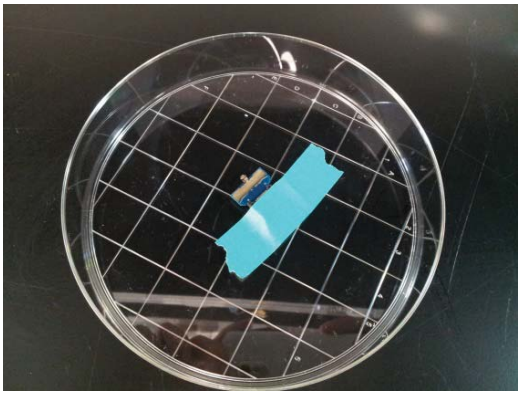


Figure 2.21 – Completed µECoG assembly stored in petri dish

Once bonded to the breakout board, the entire assembly is stored in a plastic petri dish, using tape to prevent the assembly from moving and thus damaging the still-fragile array and cable due to electrostatic forces as shown in Figure 2.21.

3 Experimental Results

3.1 Post-process plating of PEDOT

Indium-tin oxide (ITO) was selected for the electrode material due to its relatively unique combination of transparency, conductivity, and biocompatibility. However, compared to other commonly used electrode materials ITO has a low conductivity [26], which is further exacerbated in this work by the small (~40µm) size of the electrodes. As such, the resulting impedances of the ITO electrodes (shown in subsection 3.2) are high enough to introduce noise into the electrophysiology amplifiers which have an input impedances of around 1Mohm. Plating of platinum black is traditionally used to solve

this problem [9], [12], but is not attractive for this application because it sacrifices transparency.

In order to decrease the impedance of the ITO electrodes, this work utilizes the transparent conductive polymer PEDOT, which has been shown to lower impedances and has been widely explored as a potential electrode material for neural probe applications [27]. The PEDOT can be plated onto the ITO electrodes using a similar setup to that described in subsection 3.2 for measuring electrode impedances. For this work, all PEDOT was plated at 10nA currents for 60 seconds using the NanoZ available from TDT: http://www.tdt.com/products/nanoz.html.

3.2 Impedance Characterization

The electrochemical impedance of the transparent µECoG arrays, with and without PEDOT plating, has been charachterized using the setup shown in Figure 3.1. In this setup, the µECoG (including the breakout PCB) is connected to a NanoZ electrochemical impedance analyzer using a custom adapter. The µECoG array is immersed in a vial containing phosphate-buffered saline (PBS) solution, and a silver wire reference electrode is connected between the reference on the NanoZ and the solution.

The statistical distributions of impedances for electrodes on two µECoG devices are show in Figure 3.2 and Figure 3.3 for ITO electrodes and PEDOT plated electrodes, respectively. All impedances were measured at a test frequency of 1004 Hz. For clarity, electrodes that were classified as "bad" (impedances >2 MΩ) were omitted from the graphs. Of the two devices tested, for the ITO only electrodes, 99 electrodes were classified as good, resulting in a yield of 77% with an average impedance of 524 kΩ. Open (bad) electrodes may be caused at by a variety of failure points, including open traces on the devices due to a failure in the liftoff step of the process, a failure to bond electrodes to PCB pads using ACF, or damage to the electrodes themselves. For the case of the PEDOT plated electrodes, for the single device tested 37 electrodes were classified as good, resulting in a yield of 58% with an average electrode impedance of 628 kΩ.

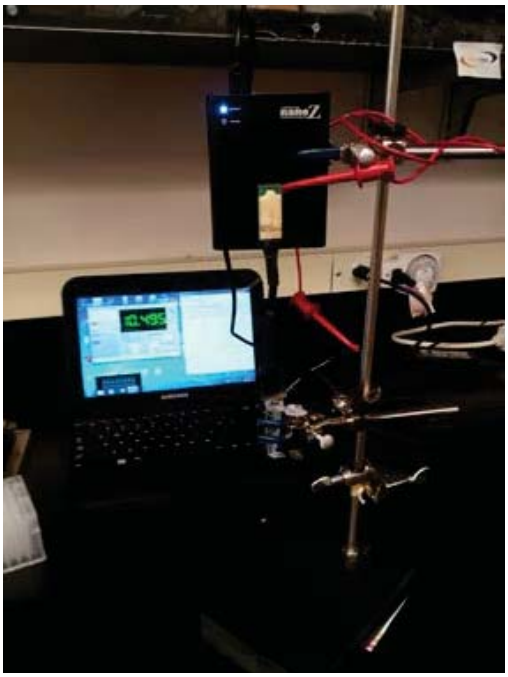


Figure 3.1 - Setup for impedance characterization and DC electroplating

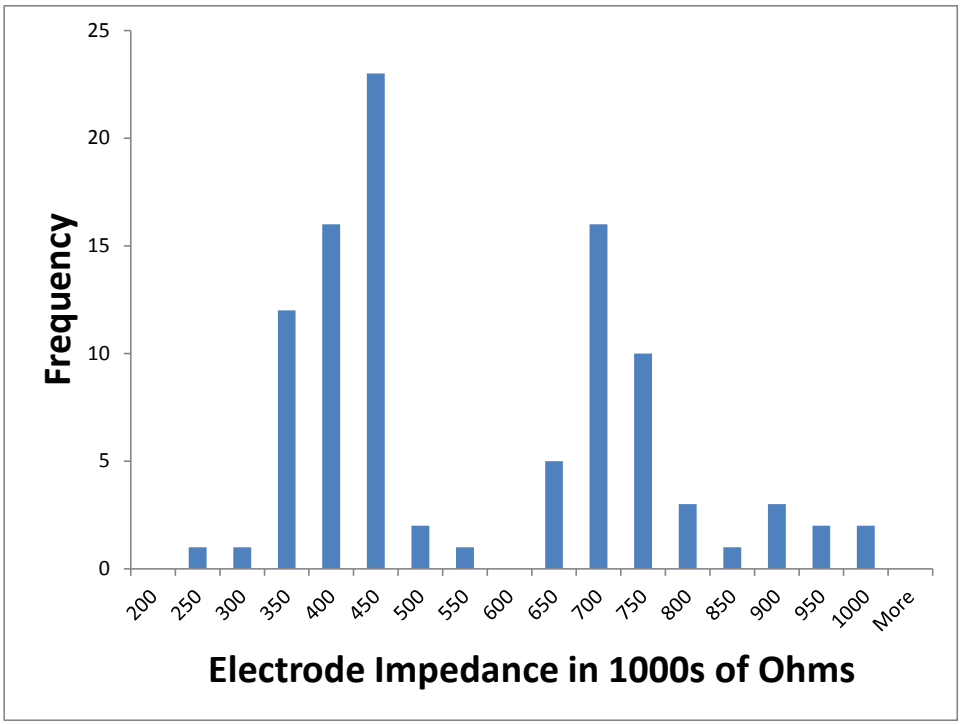


Figure 3.2 - Impedance distribution for ITO electrodes

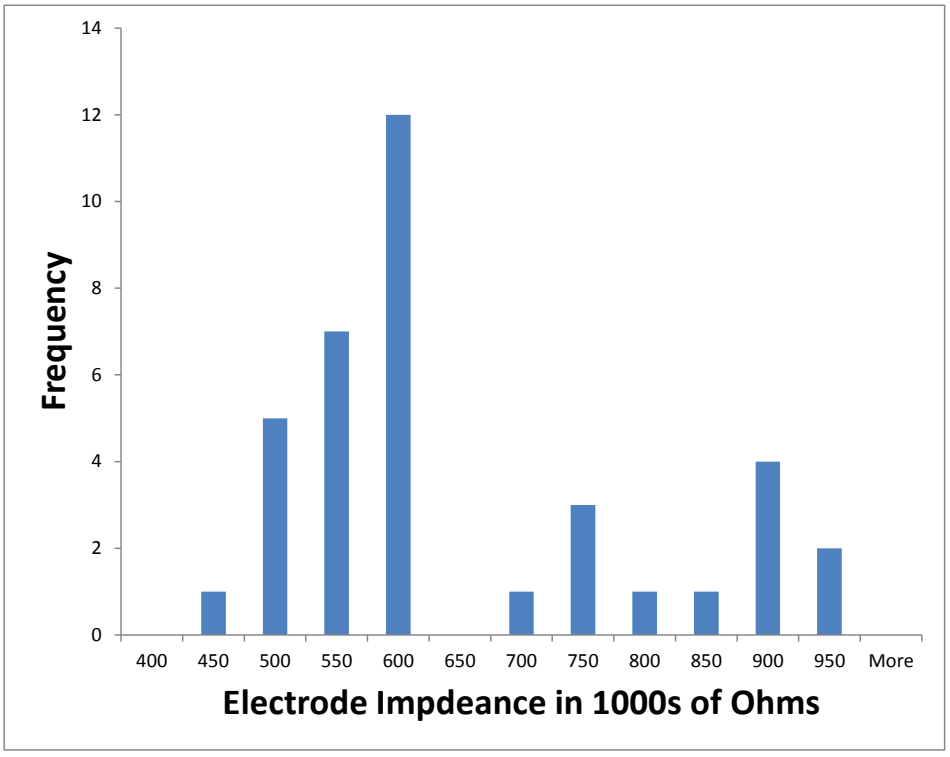


Figure 3.3 - Impedance distribution for PEDOT plated electrodes

3.3 Electrical Test

The µECoG arrays were electrically characterized in a custom test setup where the µECoG arrays were immersed in a saline solution and the solution was interrogated with a 1mV 10 Hz sine wave voltage source via a function generator. The amplifier was grounded such that current passed from the positive electrode of the voltage source through the ECOG array.

Measurements for the ITO-only µECoG arrays are shown in Figure 3.4 - Figure 3.6. Figure 3.4 shows time-domain data for 2 seconds of measurement, sampled at 5000 samples/second. It is easy to see a very strong 60 Hz component of the signal in addition to the 10Hz from in input signal. This is due to the well-known 60 Hz noise of the lab environment, in this case likely originating from the function generator used to produce the 10 Hz source, the amplifier, and the signals processing computer, all of which were plugged into wall power. The presence of 60 Hz noise can be verified by looking at the frequency-domain traces shown in Figure 3.5 (produced via an FFT algorithm in Matlab), which in addition to a strong component at 10 Hz show strong components at 60 Hz and its harmonics. Figure 3.6 shows the time domain and frequency domain data side by side for the best ITO channel. From the figure it can be seen that the SNR for the electrode is only 2.2dB. Note that only 32 channels are shown in Figure 3.4 and Figure 3.5– for this test setup one-half of the adapter stage was malfunctioning such that only half of the 64 channels for a given µECoG device could be recorded from.

Measurements for the PEDOT-plated µECoG arrays are shown in Figure 3.7 - Figure 3.9. Figure 3.4 shows time-domain data for 2 seconds of measurement, sampled at 5000 samples/second. The 60 Hz noise component is still present, but in most channels is highly attenuated compared to the reference case for the ITO only electrodes. This is verified by the frequency domain data shown in Figure 3.8. In addition to a higher overall SNR, the PEDOT electrodes show a much greater variation in SNR compared to the ITO-only electrodes, indicating difference in plating coverage. Figure 3.9 shows the time domain and frequency domain data for the best PEDOT electrode side-by-side. Analyzing the data in the figure shows the PEDOT electrode to have an SNR of ~10db, or approximately 6x higher than the ITO-only electrodes.

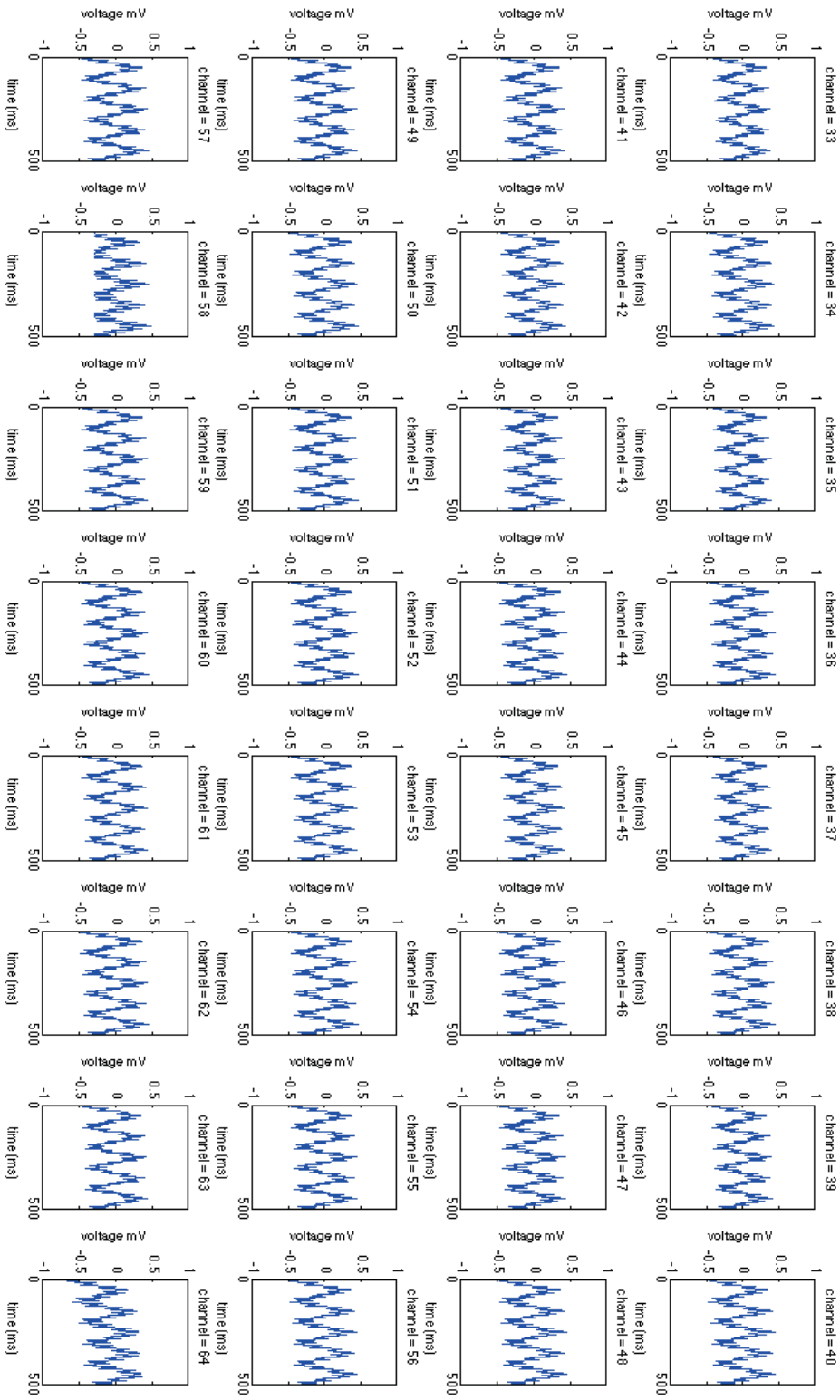


Figure 3.4 – Electrical test recording for 32 ITO electrodes (time domain)

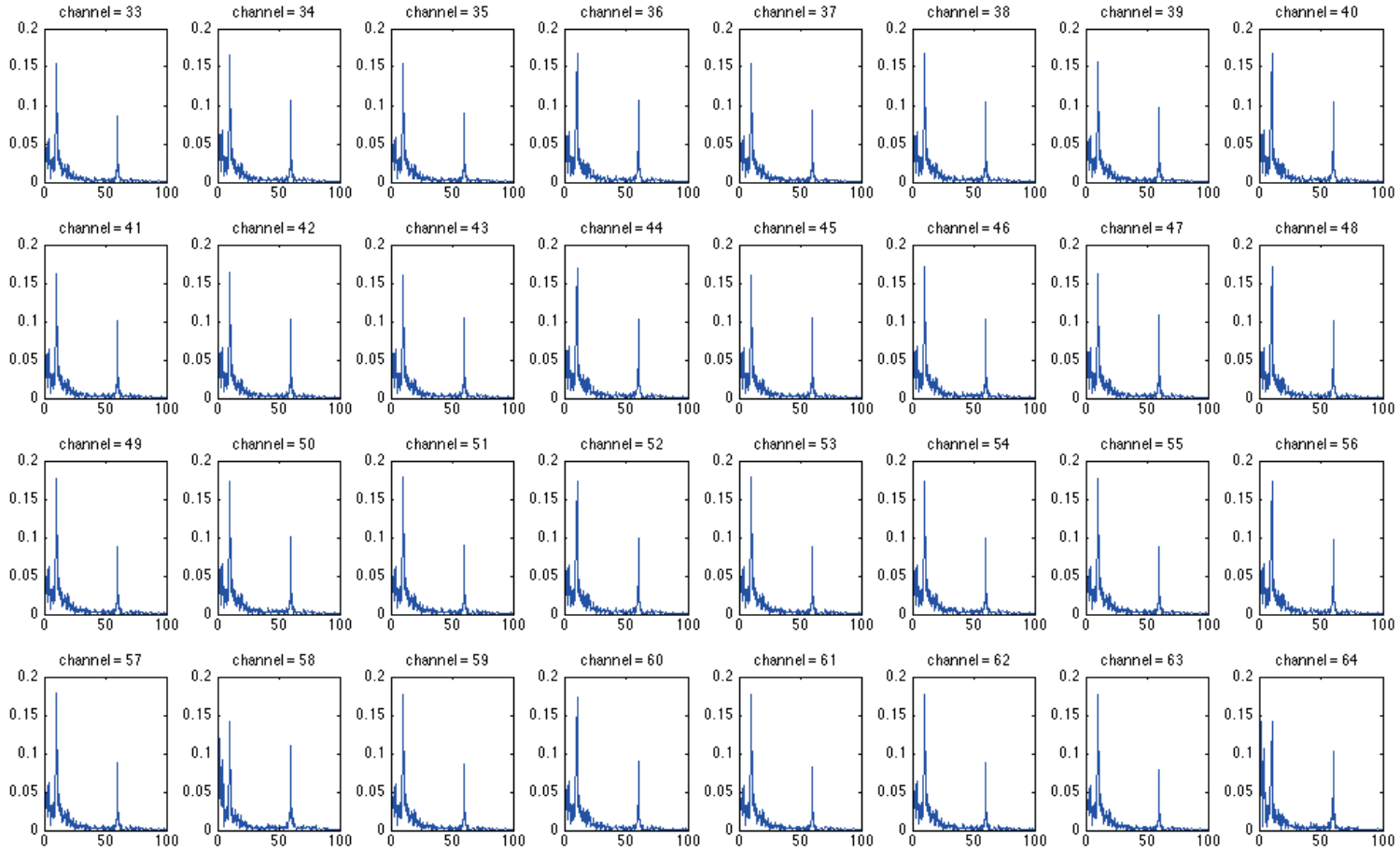


Figure 3.5 - Electrical test recording for 32 ITO electrodes (frequency domain)

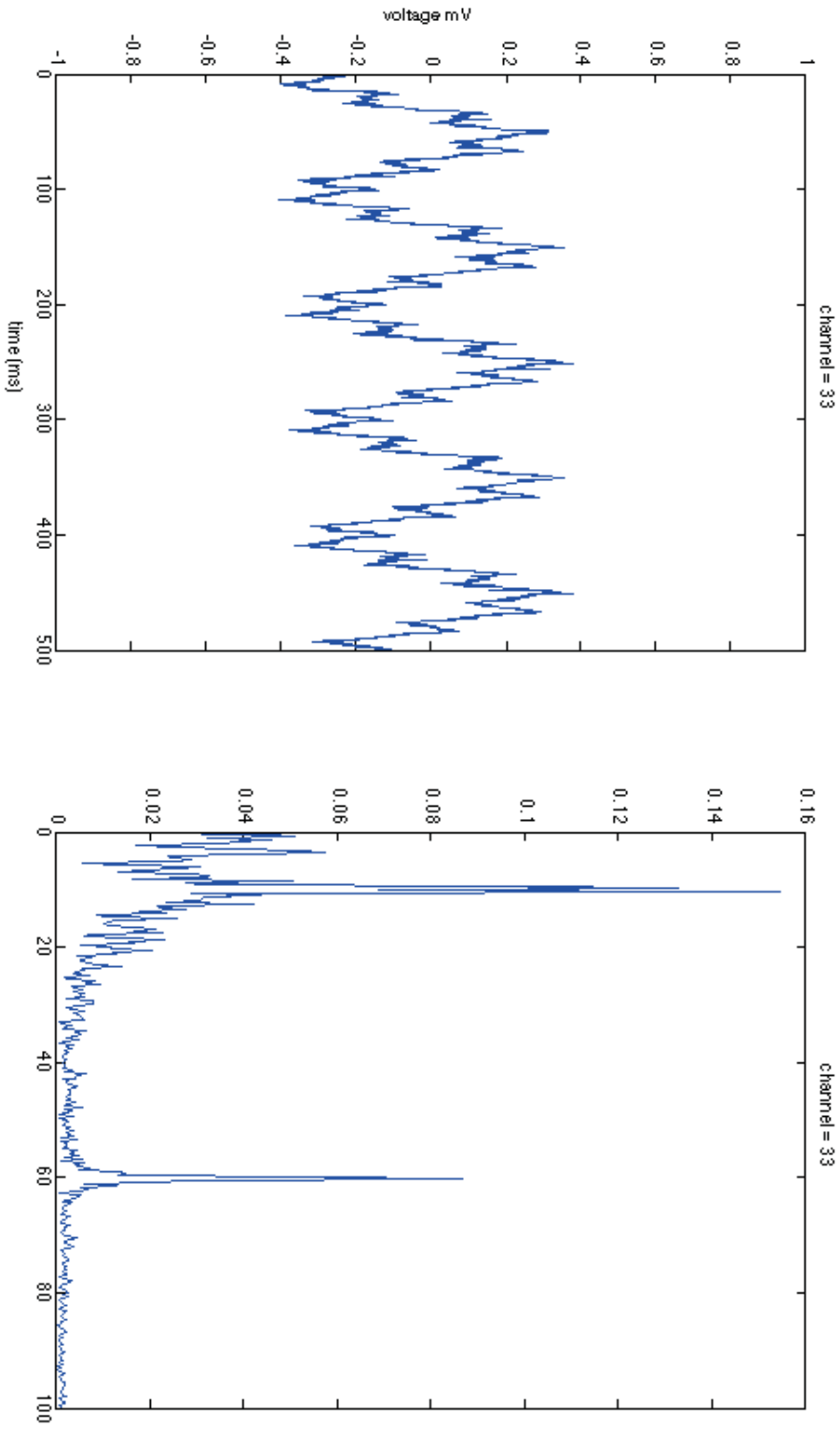


Figure 3.6 – Time and frequency domain data for best ITO channel

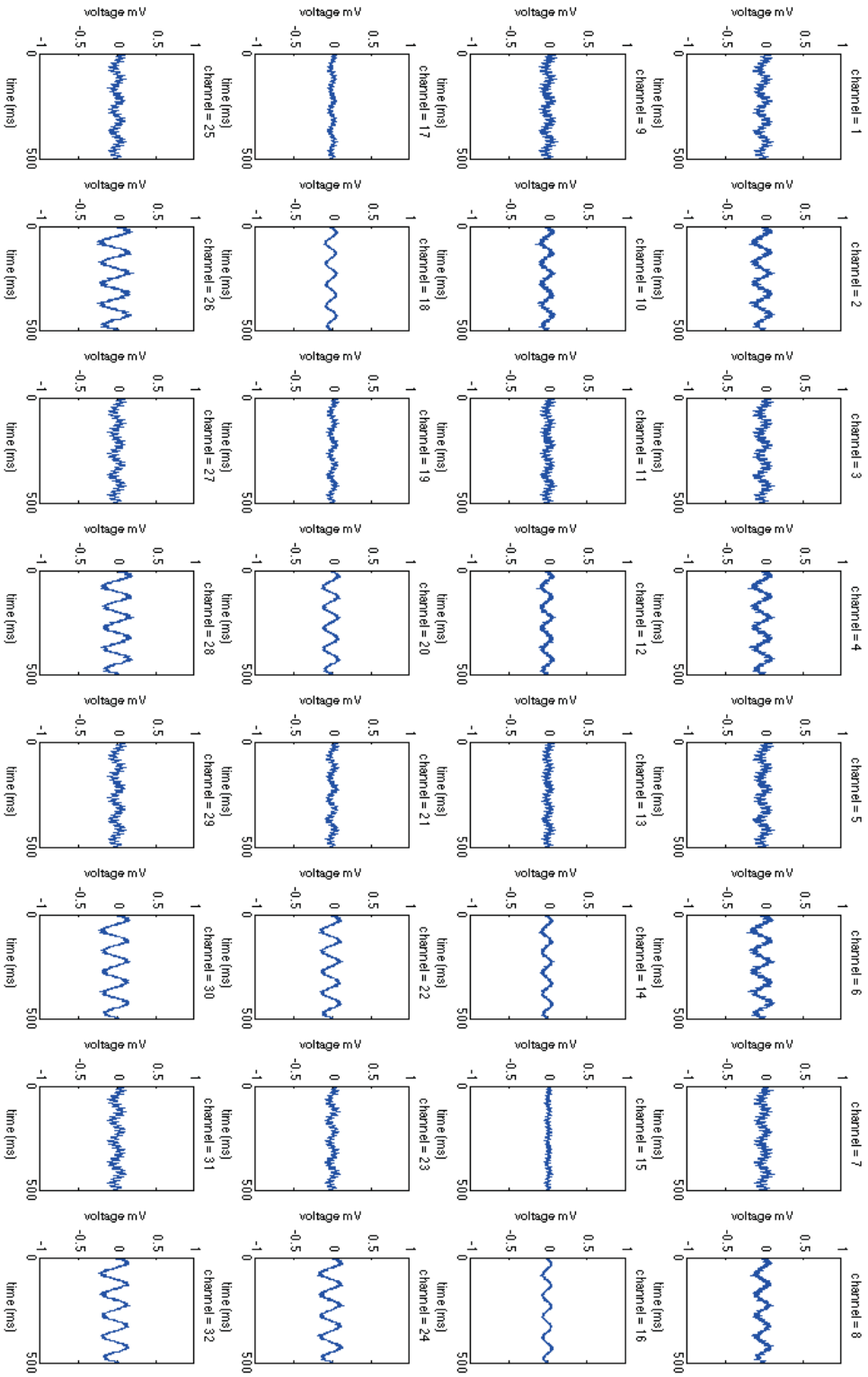


Figure 3.7 - Electrical test recording for 32 PEDOT electrodes (time domain)

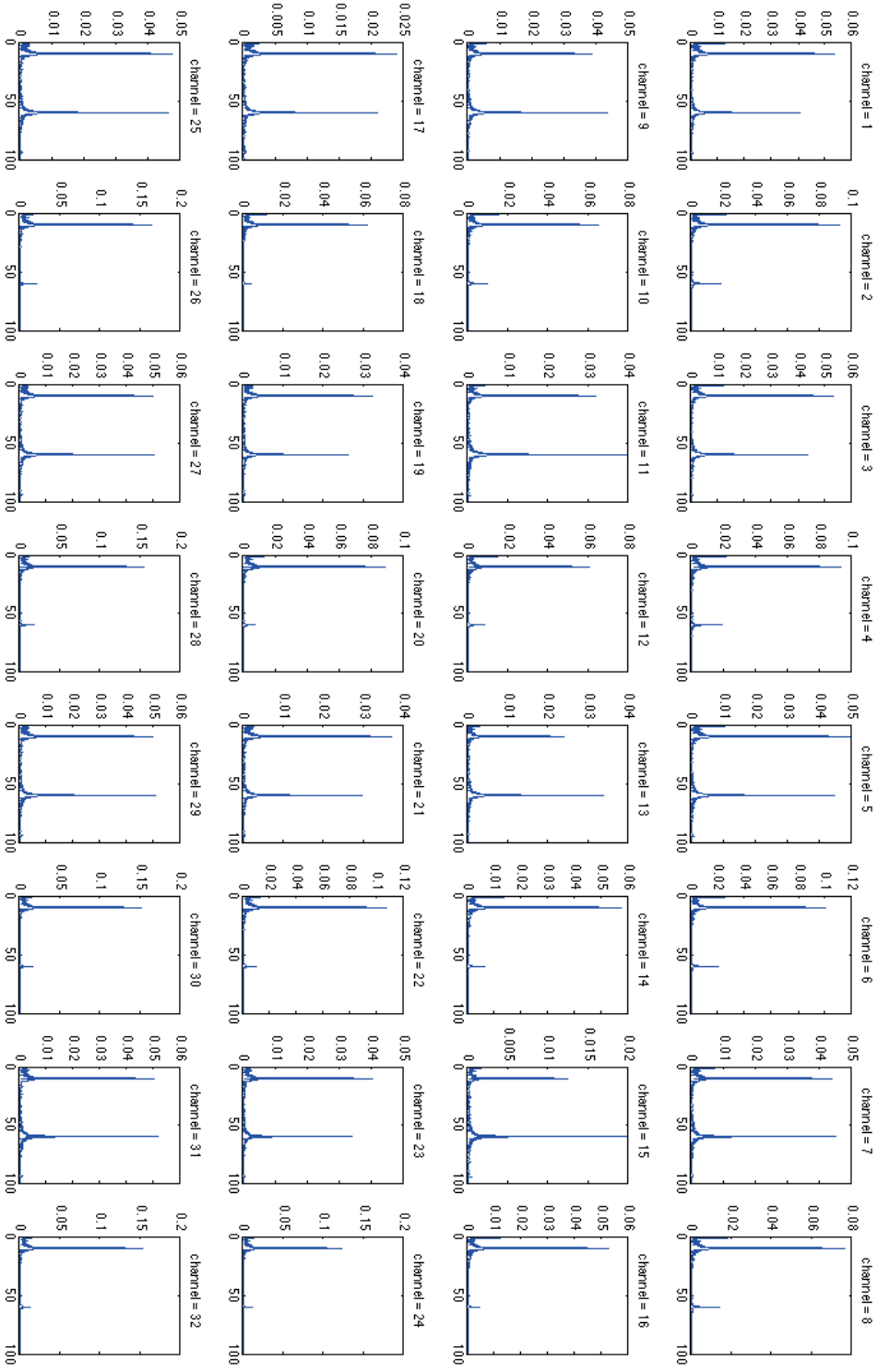


Figure 3.8 - Electrical test recording for 32 PEDOT electrodes (frequency domain)

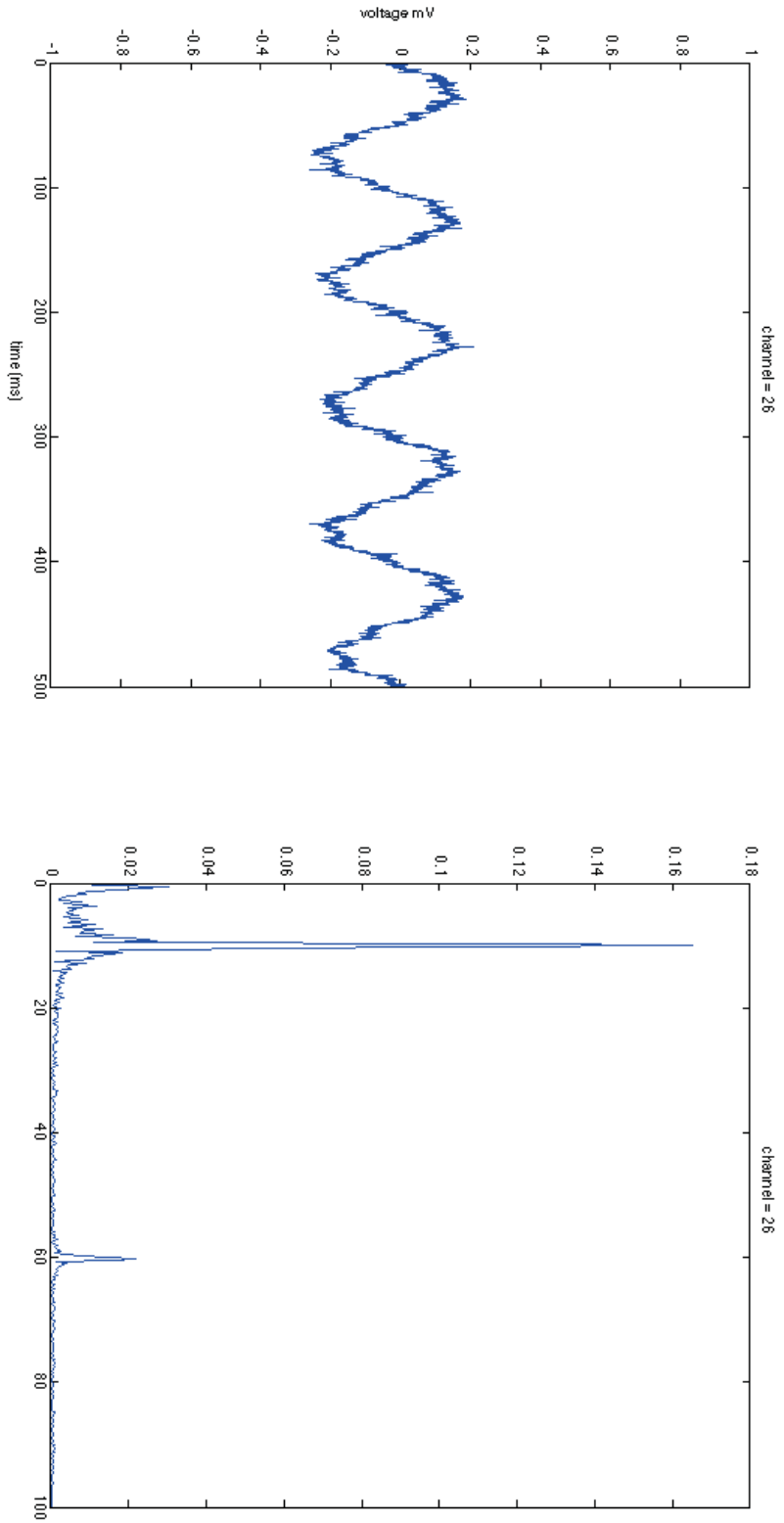


Figure 3.9 - Time and frequency domain data for best PEDOT channel

4 Conclusions and Future Work

This work has described in considerable detail the design, manufacture, and testing of transparent µECoG arrays fabricated in the ITO electrode technology pioneered in [26]. The work extended the results from [26] in two significant areas: plating of electrodes with the conductive electrode polymer PEDOT and reaching new milestones in electrode size and electrode density. While the PEDOT deposition has not yet been fully optimized, results from subsection 3.3 indicate promise for decreasing impedance and lowering noise of ITO electrodes by plating with PEDOT. The exact tradeoffs between transparency and conductivity still need to be established, but it is likely that further optimization of the plating process will lead to a considerable reduction in electrochemical impedance, greatly increasing the viability of ITO electrodes for electrophysiology studies that require low noise levels. Furthermore, inkjet printing PEDOT onto the electrodes at a wafer scale has recently matured into a viable technology option, and will be explored as an alternative to electroplating PEDOT for decreasing impedance of ITO electrodes [36].

Electrical testing described in this work has validated the functionality of µECoG electrodes on the tiny scale (40µm) and large density shown in this work. However, it remains to be shown whether electrodes of this size provide a useful increase in information since decreasing electrode size comes at the cost of increased electrochemical impedance. As described in the introduction to this work, it is suspected based on the literature that decreasing electrode size should result in the ability to image higher-frequency content due to a smaller amount of spatial averaging, but this claim remains to be validated experimentally. Likewise, the usefulness of packing electrodes into such a large density configuration is certainly controversial, as it is unclear if the electrodes will be decoupled from their adjacent neighbors. However, recent work has shown the presence of new phenomena viewable with µECoG arrays as density increases and electrode size decreases [14], and so it is the opinion of the author that a high density of recording sites is probably useful at least for certain experiments. Ultimately, each application will have a unique set of tradeoffs for electrode size and density which trades off bandwidth and specificity for noise and spatial coverage.

Future work will take advantage of the transparent nature of the ITO µECoG arrays to conduct experiments using optogenetic mice while simultaneously recording from the array. The initial goals of these experiments will be to determine optimal parameters for the µECoG array, including PEDOT parameters, electrode size and density, and electrode count. Once optimized, the transparent µECoG arrays can be used in conjunction with optogenetics to probe and elucidate a wide variety of phenomena, including the mechanisms of surface potential gamma band oscillation and oscillatory coupling mechanisms in the cortex.

5 References

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6 Acknowledgments

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7 Appendix

7.1 Process Debugging

One process step that has a large amount of variability is the final oxygen plasma etch to open vias and release the device. This etch varies mostly based on the exact thickness of parylene, but also on the etch timing, since in order to avoid overheating the parylene C substrate the Plasma Etcher must by cycled on and off at 30 second intervals. Figure 6.1 - Figure 6.4 show images charachterteristic of under-etching the parylene. The device outlines still have black residue (partially etched parylene) as do the holes in the electrode array. The vias to open the electrodes are still very small, and the bondpad arrays have not been cleared. These pictures represent an etch that is ~75% complete. Additionally, Figure 6.2 shows some cracking induced by high temperatures in the platinum deposition step.

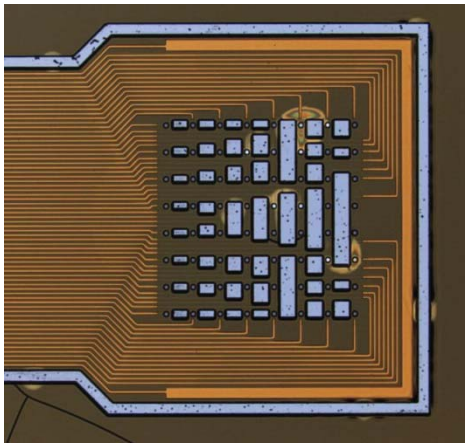

Figure 6.1 – Incomplete etch

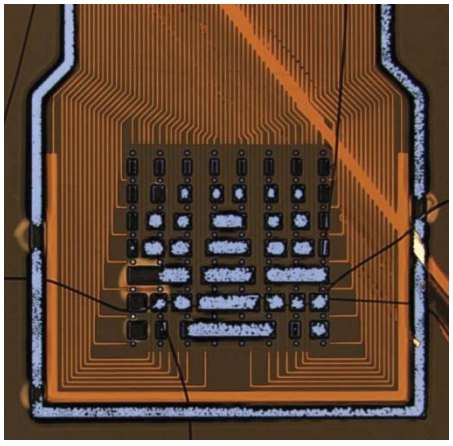

Figure 6.2 – Incomplete etch showing cracking from stress induced by evaporation

Figure 6.3 – Incomplete etch showing bond-pad array

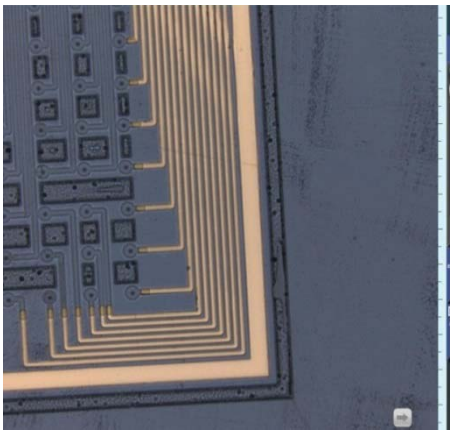

Figure 6.4 – Incomplete etch showing electrode array detail