Gravure-printed Highly-scaled Organic Thin-film Transistors for Low-cost and Large-area Electronics

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By

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Abstract

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Printed electronics using recently developed solution-processed electronic materials and incorporating conventional graphic arts printing presses has been proposed as an emerging technology for low-cost large-area electronic systems on flexible substrates (e.g. disposable RFID tags, flexible displays, and various types of sensors and actuators). For more than a decade, a significant amount of research in printed electronics has been focused on the development of high mobility printable semiconductor materials. Despite the recent achievements of the high mobility semiconductor materials that surpass the performance of amorphous silicon, overall performance of printed transistors on plastic is not adequate for the proposed applications due to the large dimension of the transistors with significant parasitic capacitance, and underperforming semiconductor materials when incorporated with mass-production printing techniques.

In this dissertation, we present a highly-scaled direct-gravure printing technique that allows sub-femtoliter scaling of printed inks, resulting in printed features as small as 4 μm while printed at high speed up to 1 m/s. By using this novel printing technique with the optimization of the high mobility organic semiconductors for the printed device fabrication processes, operation of gravure-printed inverters on plastic at frequencies above 1 MHz is achieved, which satisfies the performance requirements for most of the proposed applications. Along with the demonstration, we discuss how accurate pattern generation in various printing systems can be achieved with the knowledge of using contact angle hysteresis.

In addition, we discuss experimental results on understanding of the origin of 1/f noise in organic thin-film transistors, which particularly affects the performance of the devices in sensor applications. Based on detailed analysis of observed non-idealities in the 1/f noise with respect to various grain sizes, operation regions, and bias conditions, we found that the trapping/de-trapping of carriers within the semiconductor is the dominant mechanism of the low-frequency noise generation in the organic thin-film transistors.

To Boyoung,

my beloved wife, life-long mate and lifetime lover,

who was always with me during my PhD journey.

When I was crying in despair, she was next to me with her warm consolation.

When I struggled, she was in front of me to bravely lead me to go through difficulties.

When I was in success, she was right behind me to lift me up to be more successful.

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Chapter 1

Introduction

1.1 Printed electronics

Printed electronics has been an interesting area where researchers from various fields (e.g. semiconductor devices, mechanical engineering, material/chemical engineering, and also conventional graphic arts industry) came to play major roles. Printed electronic devices and systems have unique benefits that had not been achieved by conventional microelectronics technology: fabrication cost can be significantly reduced in area-constrained applications through additive patterning process; electronics can be built on flexible plastic or even paper substrates; large-area fabrication is possible with no need of vacuum processes; printable electronic materials can be tuned to obtain unique chemical sensitivity; and integration with various biological materials through spatially-specific deposition is possible. With these benefits, various novel applications have been suggested and demonstrated: disposable RFID tags[1]–[3], flexible displays[4], [5], photovoltaics[6], electronic skin[7], braille displays[8], X-ray detectors[9], biological applications[10]–[12] and much more.

In order to realize these applications into products, equally important efforts on various aspects of printed electronics are necessary. First, the performance of printed transistors must be good enough to provide operations that are required for the applications (e.g. RFID tags require data rates in the range of 100 kHz or more, as do fully-integrated displays).[1] With recent development of printable semiconductor materials showing high mobility, the possibility of the high performance operation has grown significantly.[13]–[15] Recently, organic semiconductor materials have shown improved mobility above 1 $cm^2V^{-1}s^{-1}$ (even better than amorphous silicon). In addition, solution processed inorganic semiconductors (e.g. nanoparticle based or sol-gel based) showing much higher mobility than the organic semiconductors have also been demonstrated.[16]

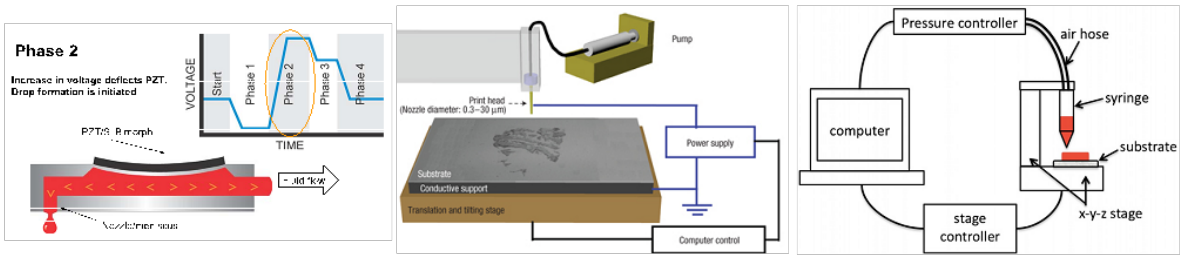
Secondly, mass production-compatible printing processes must be properly integrated with the semiconductor device fabrication processes. Most printable electronic materials have been tested based on processes that either still strongly depend on conventional microelectronics fabrication (e.g. photolithography or vacuum deposition) or are not feasible for mass production (e.g. low throughput laboratory scale inkjet printers). In

particular, for low-cost benefits, it is mandatory that we develop mass-production compatible high-throughput printing processes such as roll-to-roll printing (R2R).

Lastly, printing systems must be understood better and improved further in order to bridge the gap between electronics and graphic arts. While the graphic arts industry is a matured field, required specifications in electronics applications are trickier than in graphic arts printing. For example, since our eyes in general cannot recognize features smaller than a few tens of μm, pixels in printed images do not need to be very small and physically connected. However, in electronics, any kind of disconnections or defects could lead to circuit failure. Therefore, the ultimate goal of printing in printed electronics is to provide impeccable patterns of complex integrated circuits. To do that, better understanding of how printed fluid forms desired patterns is required, and proper design of printers that can deliver the patterns is needed.

1.2 Printing techniques

A number of printing techniques have been suggested for printed electronics. Jet printing techniques such as piezoelectric inkjet printing, electrohydrodynamic (EHD) jet printing, and pneumatic printing have been used.[17]–[19] As shown in **Figure 1.1(a)**, the piezoelectric inkjet printing ejects a droplet by an acoustic wave generated by the deflection of a piezoelectric plate within the inkjet nozzle. The EHD jet printing uses an electric field between the nozzle and the printing substrate to generate a droplet as shown in **Figure 1.1(b)**. The pneumatic printing (also called dispenser printing) uses airflow from a pump to dispense a droplet through a selected syringe needle (see the setup in **Figure 1.1(c)**). Though the physical mechanism of the generation of jetted droplets is different for these printing techniques, desired patterns are built in the same way. Jetted droplets form lines, and the lines form two-dimensional patterns by merging. Advantageously, these non-contact jet-printing techniques provide flexibility in the design of patterns since the printers can be built as a drop-on-demand style printer to jet droplets at any desired location on any substrate in any order. In particular, piezoelectric inkjet printer has been the most widely used because of its multi-nozzle configuration capability and its commercial availability for printed electronics research (such as Dimatix from Fujifilm).



(a) (b) (c)

Figure 1.1 Various jet printing techniques: (a) Piezoelectric inkjet printing (from Fujifilm DMP-2800 user manual), (b) electrohydrodynamic (EHD) jet printing[18], and (c) dispenser printing (pneumatic printing)[19].

However, these jet printing techniques suffer from low printing throughput. In printed electronics, what is very important is its low fabrication cost per unit area instead of the cost per logic (in other words, per transistor); since today's microelectronics based on photolithography can produce billions of transistors in a single chip, the fabrication cost per logic in the case of conventional microelectronics is very low. This is the reason why RFID tags, displays and so on are suggested as appropriate printed electronics applications since the size of RFID tags are determined by the size of their antenna rather than the logic core, and the size of pixels in displays is predefined. In other words, printed electronic systems are likely to have pre-defined sizes that are not very small. Therefore, it is particularly important to be able to print more area in a given time with a given amount of ink. Also, higher throughput of product fabrication is, in general, always helpful for the reduction of fabrication cost. In jetting-based printing, despite the integration of multiple nozzles to increase the production speed, the control of the multiple nozzles without crosstalk and clogging is still a challenge. Moreover, as the printing resolution increases, more nozzles and also more frequent jetting are required, resulting in even slower printing speed.

From the perspective of fabrication cost, high-throughput contact printings (also known as impression printings)—which is used to produce reproductions of an original publication using industrial printing presses—are promising ones for printed electronics applications. There are various impression printing techniques such as flexography, gravure, and offset lithography.[20] Flexography uses a master—typically rubber—that has the image areas (desired patterns) as raised surfaces. The raised surfaces are inked and the inked images are transferred to printing substrates. Flexography printing can be applied to various substrates including metallic films, and it has been popularly used for food package printing. Direct gravure printing, also known as rotogravure, uses a roll-based master with patterns engraved to transfer images directly onto flexible printing substrates. The whole master is inked, and a metal doctor blade wipes only non-image areas such that the engraved patterns (image areas) can only hold the ink. Offset lithography printing uses wetting contrast between image areas (hydrophobic) and non-image areas (hydrophilic); the image areas only hold printing inks, and the non-image areas only hold water. Then, those are transferred to a rubber blanket offset cylinder followed by the transfer of the image onto printing substrates. The printing press setup and the ink transfer process for the three printing techniques are illustrated in **Figure 1.2**.

Due to the fast printing speed (up to 15 m/s) and the master roll size scalability without compromising the printing speed, the roll-based contact printings offer much higher printing throughput than the jet printings. Therefore, these printing techniques are currently used in high-volume printings in graphic arts industry; daily newspapers—which must be very cheap—are offset printed. Among those mass-production printing techniques, direct gravure printing is the most promising one for printed electronics particularly because of its high-resolution capability and good pattern fidelity. Since the roll master in the direct-gravure printing is composed of metal (e.g. chrome plated copper roll), the engraved images on the metal cylinder can be printed with minimized distortion. However, the rubber master used in flexography could cause distortion of the image patterns due to the mechanical deformation of the rubber master during impression. For the offset lithography, the usage of offset cylinder requires additional ink transfer, causing higher chance of

having distorted images and loss of inks. Further, the metal roll used in gravure printing can allow much wider choices of printable inks. The inks that are developed for printed electronics use various chemical solvents that could even dissolve the rubber rolls used in flexography and offset lithography.

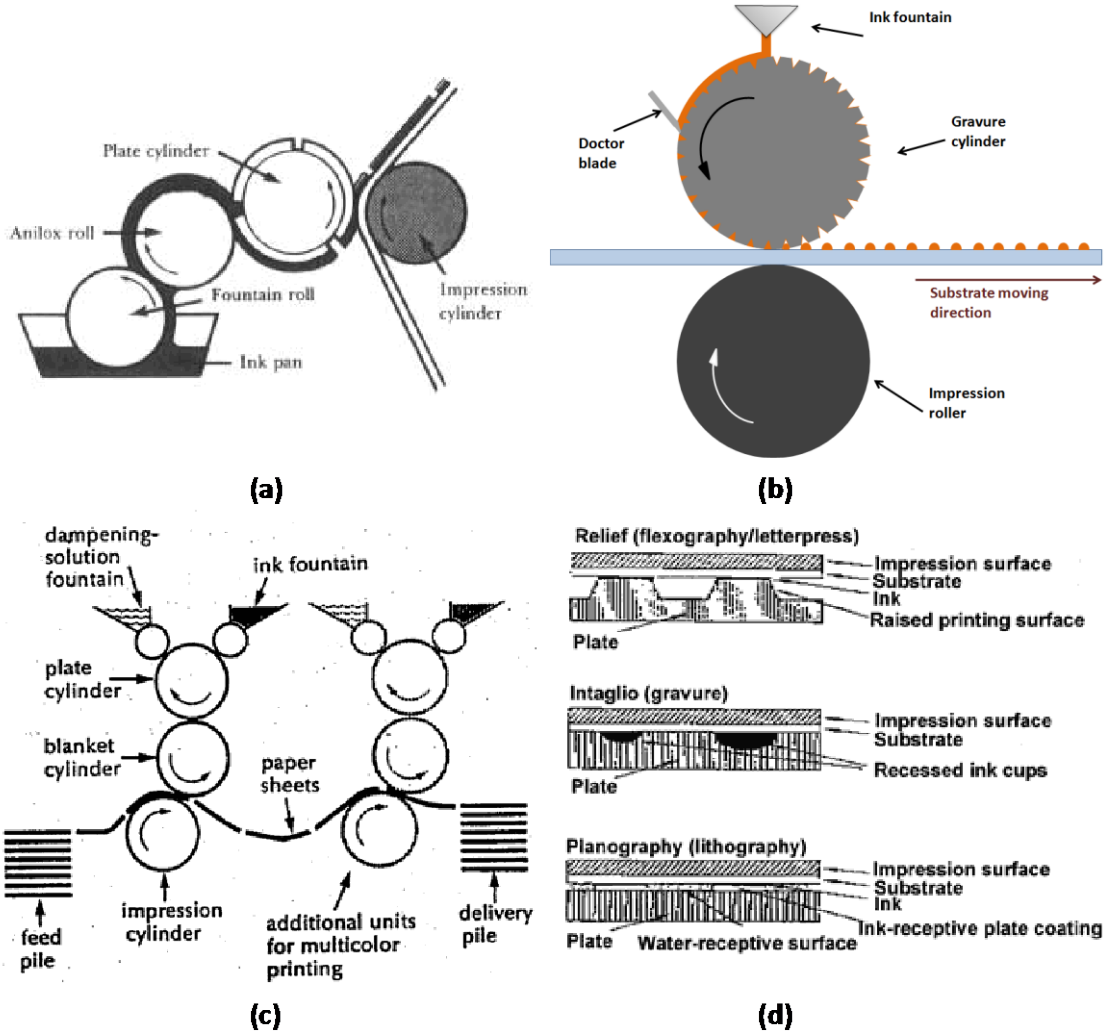


Figure 1.2 Various roll-based impression printing techniques: (a) flexography, (b) gravure, (c) offset lithography, and (d) close-up diagrams of ink transfer. (all the images except (b) are obtained from Printers' National Environmental Assistance Center, http://www.pneac.org/)

Several important properties of the inkjet printing and the gravure printing are summarized for comparison in **Table 1.1**. As mentioned earlier, gravure printing has a significant advantage in printing throughput over inkjet printing. Gravure printing is also less solvent specific and is compatible with a wide range of viscosity of the inks while the piezoelectric inkjet printing requires certain constraints on the inkjet-able ink properties (low viscosity, slow evaporation rate and high boiling point). However, gravure printing is traditionally inferior to the inkjet printing in terms of the printing resolution and printing registration accuracy. The importance of printing resolution will be discussed further in the next section.

Parameters	Inkjet	Gravure
Resolution (typical)	≥ 25 μm from 1 pL droplet	≥ 50 μm
Resolution (State-of-the-art)	≥ 2 μm [21] Multiple passes (10 passes)	≥ 20 μm [22] single pass
Printing speed (throughput)	≈ 10 mm/s (=0.01 m/s) (10 μm drop spacing @ 1 kHz) (scale down with drop size	≥ 1 m/s (regardless of pattern sizes)
Ink compatibility	Non-volatile solvent ≤ 10 cP (low mass-loading)	Not solvent specific 10 ~ 10^5 cP (high mass-loading possible)
Registration accuracy	≥ 10 μm, jetting accuracy [23]	≥ 16 μm in printing direction [24] ≥ 41 μm perpendicular to the printing direction

Table 1.1 Comparison of several key properties between inkjet and gravure printing. [21]–[24]

Among the various printing systems aforementioned, inkjet-printed transistors have been studied the most due to the flexibility in the design of experiments and commercial availability of the inkjet printer. However, for mass production of printed electronics applications, it is vital to be able to investigate electronic devices printed by high-throughput printing techniques—in particular, gravure printing. Further, it is imperative to understand the detailed mechanism of the printing processes for the improvement of the printing quality, and better controllability and optimization of the printing processes.

1.3 Performance improvement by scaling

Compared to the significant amount of effort from the material science and chemistry community focused on the development of high mobility semiconductors, other ways to improve the performance (speed) of printed transistors have relatively not been explored in printed electronics. From the successful history of the semiconductor industry, we know that scaling of the transistor channel length can increase the transistor speed. The transition frequency (f_T)—at which an unloaded transistor shows unity current gain—in saturation mode is given in equation (1) below.

$$f_T = \frac{g_m}{2\pi C_{in}} = \frac{\frac{W\mu C_{ox}}{L} V_{DS,sat}}{2\pi C_{ox} W\left(L_{ch,eff} + L_{SD,overlap}\right)} = \frac{\mu V_{DS,sat}}{2\pi {L_{ch}}^2 \alpha\beta} \quad (1)$$

where $\alpha(=L_{ch,eff}/L_{ch})$ is a constant determined by the operating region to represent more accurate input capacitance, and β is a ratio of S/D overlap area to channel ($L_{SD,overlap}/L_{ch}$). From the equation (1), the reduction of channel length will lead to both increase of transconductance (g_m) and decrease of input impedance, resulting in a quadratic increase of the speed of transistors. Therefore, proper scaling of printed transistors with minimized parasitic capacitance is necessary in addition to the development of high mobility semiconductor. Sekitani et al demonstrated transistors with small channel length down to 2

µm by utilizing sub-femtoliter electrohydrodynamic inkjet-printed droplets.[21] However, as inkjet printing is scaled to finer drops, printing speeds slow unacceptably since the number of drops required to build a pattern increases in correspondence to the reduction in drop size. Furthermore, multiple passes with the inkjet head are required to make lines conductive due to the low metal content, which lowers throughput even more.

The scaling of gravure-printed TFTs is, therefore, of particular interest. As mentioned earlier, the high throughput of the gravure printing makes itself a strong contender for printed electronics applications. Unfortunately, prior to the work herein, the performance of such printed TFTs by gravure or other roll-based printings has been limited by the large dimensions of such printed devices (typical gravure printing produces features > 50 µm), the low mobility of the printed semiconductors, and the poor electrostatic integrity of the realized devices, resulting in poor operating frequencies of demonstrated ring oscillators, 2.5 ~ 150 Hz[25]–[28] and high operating voltages in the range of 50 ~ 100 V.[26]–[30], [22] To make printed electronics a reality, is it critical that orders of magnitude better performance be achieved as mentioned earlier. Additionally, the systems of interest require operation at voltages of <20V.

Unfortunately, very little work has been made to properly scale the channel length of printed organic thin-film transistors (OTFTs). Some reported top-gate OTFTs have achieved reduction of the channel length by placing the printed source and drain closer together, resulting a demonstrated channel length of 10 µm.[28], [30] By using hydrophobic barriers to separate aqueous based source/drain conductive inks, reduced channel lengths have been achieved, and improved ring-oscillator operating frequency of around 150 Hz has been demonstrated.[28] In these devices, unfortunately, performance is limited by the large overlap capacitances resulting from the large width of the gate electrode relative to the source/drain spacing. Additionally, the interactions between the hydrophobic barriers, hydrophilic source/drain electrodes, and the semiconductor typically result in degraded overall carrier transport due to poor semiconductor ordering. Therefore, in order to fully benefit from the reduction of channel length for better AC characteristics, it is vital to reduce the width of the conductive electrodes regardless of the device structure used as illustrated in **Figure 1.3**.

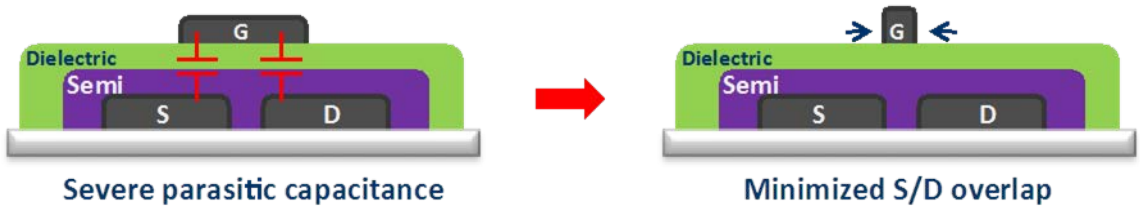


Figure 1.3 Parasitic capacitance from large dimension of printed features limits the speed of printed transistors.

We have previously exploited this to realize high-performance gravure-printed TFTs.[22] de la Fuente Vornbrock et al utilized chemically etched patterns on a gravure cylinder to fabricate 20 µm wide gate electrodes. These were used to realize printed bottom-gate OTFTs with transition frequencies as high as 18 kHz, albeit at relatively high operating voltages. To realize any functional application, however, it is still mandatory to further

scale the channel length, reduce the operating voltage to reasonable range, and optimize carrier transport and overall electrostatic integrity for better mobility and switching. The performance of R2R printed circuits in the literature is summarized in **Figure 1.4**.

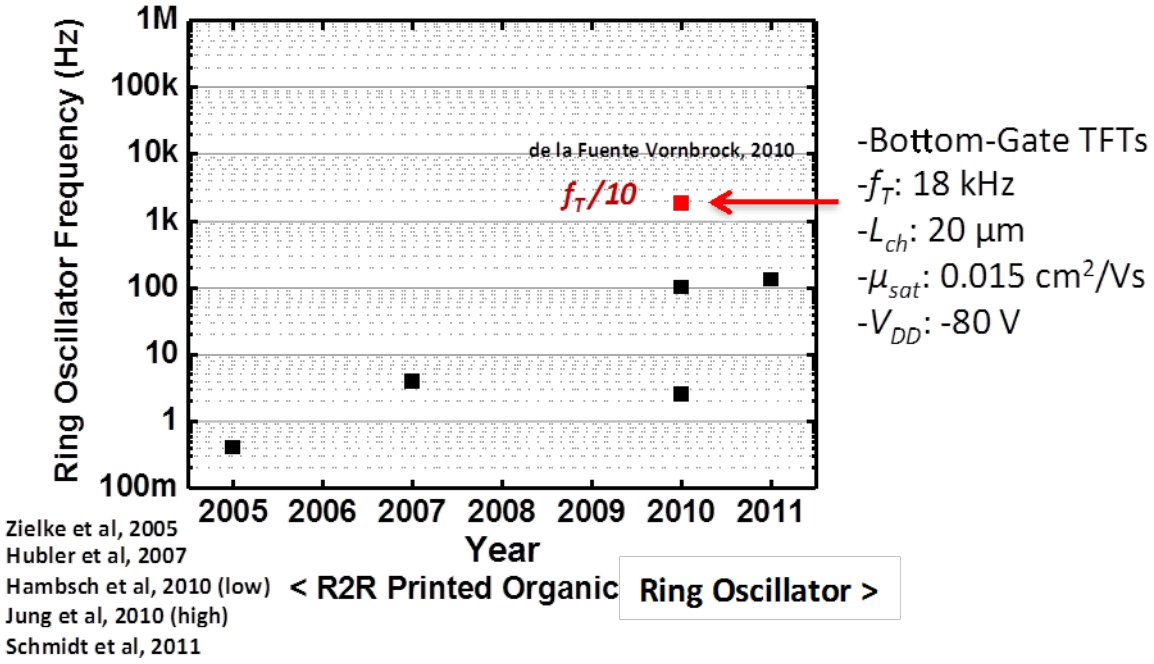


Figure 1.4 Ring oscillator frequency of reported R2R printed ring oscillators.[2], [26]–[28], [31] Red data is from [22] which only showed TFTs. Therefore, 1/10 of f_T is plotted as comparison with circuits.

1.4 Understanding of 1/f noise in OTFTs

The use of organic TFTs has also been suggested for various types of sensors as well. [10], [11], [32]–[36] Many of these applications exploit interactions with the physical world, either through sensing or actuation.[7], [8], [10], [11], [21], [32]–[41] Organic transistors are considered very promising for these applications due to their mechanical flexibility and chemical / physical sensitivity. In the design of those sensor systems, one of the necessary requirements that must be met is noise immunity since this often limits sensitivity—more precisely signal-to-noise ratio (SNR)—of the sensors. Since the current levels in OTFT circuits are generally small (~µA), it is harder to obtain high SNR. Therefore, it is important to know how immune OTFTs are to unwanted noise signals. Since the operating frequency range of OTFTs is typically low (from Hz up to MHz at best), 1/f noise, also called flicker noise, is expected to be dominant in these devices. 1/f noise is a well-known noise signal of which the power spectral density is inversely proportional to the frequency as shown in **Figure 1.5**. At high frequency, thermal noise—that is generated from random Brownian motion of electrons and shows a constant power spectral density—is more dominant than the 1/f noise. 1/f noise is found in almost all electronic devices such as diodes, BJTs, and MOSFETs.[42] Furthermore, given the nature

of the disordered semiconductor system in OTFTs, there are more possible noise sources within the devices. Therefore, it is vital to understand the mechanisms underlying low frequency noise (LFN) in OTFTs and, further, to develop a model that can be integrated into circuit simulations for more accurate estimate of the noise.

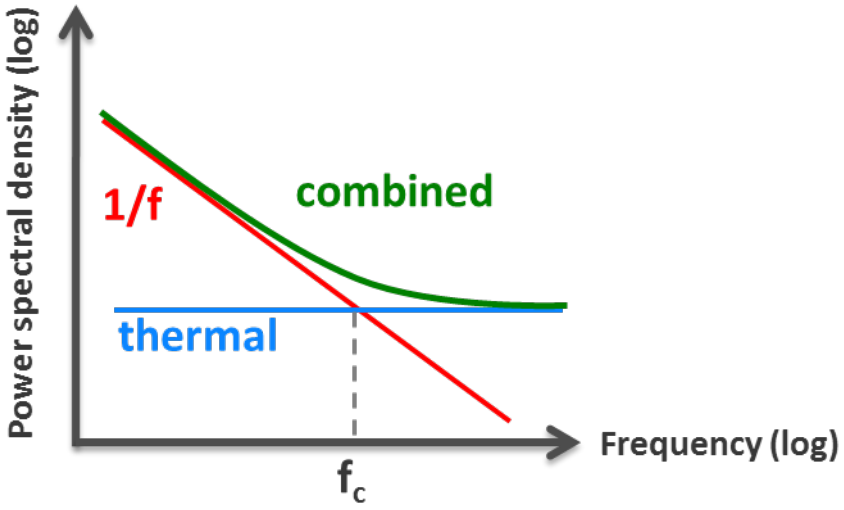


Figure 1.5 Typical frequency spectrum of various noise signals in electronic devices. f_c is defined as corner frequency at which the 1/f noise becomes comparable to the thermal white noise. For conventional silicon MOSFETs, the corner frequency is typically ranged from tens of kHz to a few MHz depending on the technology and the type of transistors.

1.5 Dissertation organization

This dissertation is organized as follows. In Chapter 2, fundamental understanding of desired pattern generation in both inkjet and gravure printing will be presented. Particularly, focus will be made on 2-dimensional (2D) features such as rectangles and squares. Key findings that are found to be governing the quality of printed 2D films will be discussed, and a simple hydrostatic model that can help in the dimensional estimation of the printed film will be developed. In Chapter 3, scaling of gravure-printed lines will be discussed. By introducing a novel pattern engraving system in gravure printing, highly scaled gravure-printed lines below 5 μm will be demonstrated. Along with the demonstration, the effect of printing parameters on the control of printed lines based on a simple hydrostatic model will be discussed. Proper ink optimization for the usage of lines as the electrodes of printed TFTs will be explored. In Chapter 4, successful integration and optimization of the highly scaled lines in Chapter 3 for high performance gravure-printed TFTs/inverters will be presented. With the proper scaling of TFTs, MHz operation of the TFTs and circuits on plastic will be demonstrated. In Chapter 5, the fundamental origin of 1/f noise in OTFTs will be studied. 1/f noise of OTFTs is measured under both DC and AC bias conditions with varied semiconductor film characteristics. From the experimental results, the dominant mechanism of 1/f noise in OTFTs will be elucidated. Finally, some conclusions and directions for future work will be presented in the last chapter.

1.6 References

[1] V. Subramanian, J. M. . Frechet, P. C. Chang, D. C. Huang, J. B. Lee, S. E. Molesa, A. R. Murphy, D. R. Redinger, and S. K. Volkman, "Progress Toward Development of All-Printed RFID Tags: Materials, Processes, and Devices," *Proceedings of the IEEE*, vol. 93, no. 7, pp. 1330–1338, Jul. 2005.

[2] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, J. M. Tour, and G. Cho, "All-Printed and Roll-to-Roll-Printable 13.56-MHz-Operated 1-bit RF Tag on Plastic Foils," *IEEE Transactions on Electron Devices*, vol. 57, no. 3, pp. 571–580, 2010.

[3] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A. K. Tripathi, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "Organic RFID transponder chip with data rate compatible with electronic product coding," *Organic Electronics*, vol. 11, no. 7, pp. 1176–1179, Jul. 2010.

[4] A. C. Arias, Jã¼. Daniel, B. Krusor, S. Ready, V. Sholin, and R. Street, "All-additive ink-jet-printed display backplanes: Materials development and integration," *Journal of the Society for Information Display*, vol. 15, no. 7, pp. 485–490, 2007.

[5] J. Daniel, A. C. Arias, W. Wong, R. Lujan, S. Ready, B. Krusor, and R. Street, "Jet-Printed Active-Matrix Backplanes and Electrophoretic Displays," *Japanese Journal of Applied Physics*, vol. 46, no. 3B, pp. 1363–1369, 2007.

[6] C. J. Brabec, "Organic photovoltaics: technology and market," *Solar Energy Materials and Solar Cells*, vol. 83, no. 2–3, pp. 273–292, Jun. 2004.

[7] T. Someya, T. Sekitani, S. Iba, Y. Kato, H. Kawaguchi, and T. Sakurai, "A large-area, flexible pressure sensor matrix with organic field-effect transistors for artificial skin applications," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 101, no. 27, pp. 9966 –9970, Jul. 2004.

[8] Yusaku Kato, Tsuyoshi Sekitani, Makoto Takamiya, Masao Doi, Kinji Asaka, Takayasu Sakurai, and Takao Someya, "Sheet-Type Braille Displays by Integrating Organic Field-Effect Transistors and Polymeric Actuators," *Electron Devices, IEEE Transactions on*, vol. 54, no. 2, pp. 202–209, Feb. 2007.

[9] R. A. Lujan and R. A. Street, "Flexible X-Ray Detector Array Fabricated With Oxide Thin-Film Transistors," *IEEE Electron Device Letters*, vol. 33, no. 5, pp. 688–690, 2012.

[10] Q. Zhang, L. Jagannathan, and V. Subramanian, "Label-free low-cost disposable DNA hybridization detection systems using organic TFTs," *Biosensors and Bioelectronics*, vol. 25, no. 5, pp. 972–977, Jan. 2010.

[11] L. Jagannathan and V. Subramanian, "DNA detection using organic thin film transistors: Optimization of DNA immobilization and sensor sensitivity," *Biosensors and Bioelectronics*, vol. 25, no. 2, pp. 288–293, Oct. 2009.

[12] L. Jagannathan, "Organic and Printed Electronics for Biological Microfluidic Applications," EECS Department, University of California, Berkeley, 2012.

[13] J. Li, Y. Zhao, H. S. Tan, Y. Guo, C.-A. Di, G. Yu, Y. Liu, M. Lin, S. H. Lim, Y. Zhou, H. Su, and B. S. Ong, "A stable solution-processed polymer semiconductor with record high-mobility for printed transistors," *Sci. Rep.*, vol. 2, Oct. 2012.

[14] H. Chen, Y. Guo, G. Yu, Y. Zhao, J. Zhang, D. Gao, H. Liu, and Y. Liu, "Highly π-Extended Copolymers with Diketopyrrolopyrrole Moieties for High-Performance Field-Effect Transistors," *Advanced Materials*, vol. 24, no. 34, pp. 4618–4622, 2012.

[15] H. Minemawari, T. Yamada, H. Matsui, J. Tsutsumi, S. Haas, R. Chiba, R. Kumai, and T. Hasegawa, "Inkjet printing of single-crystal films," *Nature*, vol. 475, no. 7356, pp. 364–367, Jul. 2011.

[16] S. Jeong and J. Moon, "Low-temperature, solution-processed metal oxide thin film transistors," *J. Mater. Chem.*, vol. 22, no. 4, pp. 1243–1250, Dec. 2011.

[17] D. Soltman and V. Subramanian, "Inkjet-Printed Line Morphologies and Temperature Control of the Coffee Ring Effect," *Langmuir*, vol. 24, no. 5, pp. 2224–2231, Mar. 2008.

[18] J.-U. Park, M. Hardy, S. J. Kang, K. Barton, K. Adair, D. kishore Mukhopadhyay, C. Y. Lee, M. S. Strano, A. G. Alleyne, J. G. Georgiadis, P. M. Ferreira, and J. A. Rogers, "High-resolution electrohydrodynamic jet printing," *Nat Mater*, vol. 6, no. 10, pp. 782–789, Oct. 2007.

[19] C. C. Ho, J. W. Evans, and P. K. Wright, "Direct write dispenser printing of a zinc microbattery with an ionic liquid gel electrolyte," *J. Micromech. Microeng.*, vol. 20, no. 10, p. 104009, Oct. 2010.

[20] N. Board, *Hand Book on Printing Technology (Offset, Gravure, Flexo, Screen)*. National Institute Of Industrial Re, 2002.

[21] T. Sekitani, Y. Noguchi, U. Zschieschang, H. Klauk, and T. Someya, "Organic transistors manufactured using inkjet technology with subfemtoliter accuracy," *Proceedings of the National Academy of Sciences*, vol. 105, no. 13, pp. 4976 –4980, Apr. 2008.

[22] A. de la Fuente Vornbrock, D. Sung, H. Kang, R. Kitsomboonloha, and V. Subramanian, "Fully gravure and ink-jet printed high speed pBTTT organic thin film transistors," *Organic Electronics*, vol. 11, no. 12, pp. 2037–2044, Dec. 2010.

[23] W. S. Wong, E. M. Chow, R. Lujan, V. Geluz-Aguilar, and M. L. Chabinyc, "Fine-feature patterning of self-aligned polymeric thin-film transistors fabricated by digital lithography and electroplating," *Applied Physics Letters*, vol. 89, p. 142118, 2006.

[24] Jinsoo Noh, Dongsun Yeom, Chaemin Lim, Hwajin Cha, Jukyung Han, Junseok Kim, Yongsu Park, V. Subramanian, and Gyoujin Cho, "Scalability of Roll-to-Roll Gravure-Printed Electrodes on Plastic Foils," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 33, no. 4, pp. 275–283, Oct. 2010.

[25] T. Hassinen and H. G. O. Sandberg, "Gravure printed low voltage polymer transistors and inverters," *Thin Solid Films*, vol. 548, pp. 585–589, Dec. 2013.

[26] A. C. Huebler, F. Doetz, H. Kempa, H. E. Katz, M. Bartzsch, N. Brandt, I. Hennig, U. Fuegmann, S. Vaidyanathan, J. Granstrom, S. Liu, A. Sydorenko, T. Zillger, G. Schmidt, K. Preissler, E. Reichmanis, P. Eckerle, F. Richter, T. Fischer, and U. Hahn, "Ring oscillator fabricated completely by means of mass-printing technologies," *Organic Electronics*, vol. 8, no. 5, pp. 480–486, Oct. 2007.

[27] M. Hambsch, K. Reuter, M. Stanel, G. Schmidt, H. Kempa, U. Fügmann, U. Hahn, and A. C. Hübler, “Uniformity of fully gravure printed organic field-effect transistors,” *Materials Science and Engineering: B*, vol. 170, no. 1–3, pp. 93–98, Jun. 2010.

[28] G. C. Schmidt, M. Bellmann, B. Meier, M. Hambsch, K. Reuter, H. Kempa, and A. C. Hübler, “Modified mass printing technique for the realization of source/drain electrodes with high resolution,” *Organic Electronics*, vol. 11, no. 10, pp. 1683–1687, Oct. 2010.

[29] M. M. Voigt, A. Guite, D. Chung, R. U. A. Khan, A. J. Campbell, D. D. C. Bradley, F. Meng, J. H. G. Steinke, S. Tierney, I. McCulloch, H. Penxten, L. Lutsen, O. Douheret, J. Manca, U. Brokmann, K. Sönnichsen, D. Hülsenberg, W. Bock, C. Barron, N. Blanckaert, S. Springer, J. Grupp, and A. Mosley, “Polymer Field‐Effect Transistors Fabricated by the Sequential Gravure Printing of Polythiophene, Two Insulator Layers, and a Metal Ink Gate,” *Advanced Functional Materials*, vol. 20, no. 2, pp. 239–246, Jan. 2010.

[30] T. Fischer, U. Hahn, M. Dinter, M. Bartzsch, G. Schmidt, H. Kempa, and A. C. Huebler, “Novel in-line method for patterned deposition of conductive structures,” *Organic Electronics*, vol. 10, no. 3, pp. 547–550, May 2009.

[31] D. Zielke, A. C. Hubler, U. Hahn, N. Brandt, M. Bartzsch, U. Fugmann, T. Fischer, J. Veres, and S. Ogier, “Polymer-based organic field-effect transistor using offset printed source/drain structures,” *Appl. Phys. Lett.*, vol. 87, no. 12, pp. 123508–3, 2005.

[32] Q. Zhang and V. Subramanian, “DNA hybridization detection with organic thin film transistors: toward fast and disposable DNA microarray chips,” *Biosens Bioelectron*, vol. 22, no. 12, pp. 3182–3187, Jun. 2007.

[33] B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H. E. Katz, A. J. Lovinger, and Z. Bao, “Electronic sensing of vapors with organic transistors,” *Appl. Phys. Lett.*, vol. 78, no. 15, p. 2229, 2001.

[34] L. Torsi, A. Dodabalapur, L. Sabbatini, and P. G. Zambonin, “Multi-parameter gas sensors based on organic thin-film-transistors,” *Sensors and Actuators B: Chemical*, vol. 67, no. 3, pp. 312–316, Sep. 2000.

[35] F. Liao, C. Chen, and V. Subramanian, “Organic TFTs as gas sensors for electronic nose applications,” *Sensors and Actuators B: Chemical*, vol. 107, no. 2, pp. 849–855, Jun. 2005.

[36] J. B. Chang, V. Liu, V. Subramanian, K. Sivula, C. Luscombe, A. Murphy, J. Liu, and J. M. J. Fréchet, “Printable polythiophene gas sensor array for low-cost electronic noses,” *J. Appl. Phys.*, vol. 100, no. 1, p. 014506, 2006.

[37] V. Subramanian, J. B. Lee, V. H. Liu, and S. Molesa, “Printed Electronic Nose Vapor Sensors for Consumer Product Monitoring,” pp. 1052–1059, Feb. 2006.

[38] T. Sekitani, M. Takamiya, Y. Noguchi, S. Nakano, Y. Kato, T. Sakurai, and T. Someya, “A large-area wireless power-transmission sheet using printed organic transistors and plastic MEMS switches,” *Nat Mater*, vol. 6, no. 6, pp. 413–417, Jun. 2007.

[39] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, and T. Sakurai, “Conformable, flexible, large-area networks of pressure and thermal

sensors with organic transistor active matrixes," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 102, no. 35, pp. 12321 –12325, 2005.
[40] T. Someya, A. Dodabalapur, A. Gelperin, H. E. Katz, and Z. Bao, "Integration and Response of Organic Electronics with Aqueous Microfluidics," *Langmuir*, vol. 18, no. 13, pp. 5299–5302, Jun. 2002.
[41] T. Someya, Y. Kato, Shingo Iba, Y. Noguchi, T. Sekitani, H. Kawaguchi, and T. Sakurai, "Integration of organic FETs with organic photodiodes for a large area, flexible, and lightweight sheet image scanners," *Electron Devices, IEEE Transactions on*, vol. 52, no. 11, pp. 2502– 2511, Nov. 2005.
[42] F. N. Hooge, "1/f noise sources," *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 1926–1935, 1994.

Chapter 2

Understanding of Pattern Generation in Printing Processes

2.1 Motivation

In order to realize various printed electronics applications, we must be able to print entire integrated circuits that are much more complex than a single device. As shown in **Figure 2.1** as an example, it requires a combination of various geometries such as lines, elbows, crosses, and rectangles. However, printing such complex layouts is in fact quite challenging because of the different specifications that we have in printed electronics compared to what conventional graphic arts printing requires. In printed electronics, we cannot tolerate any defect or pinhole since any of those can make the entire circuit malfunction. However, in graphic arts printing, even clear disconnections are acceptable as long as those are smaller than what human eyes can recognize. In addition to that, printing in printed electronics requires more precise control because of the substrate's imperviousness to liquids. In graphic arts, the choices of the printing substrates are often various types of paper that absorb the ink and hold the pattern thereafter. However, the printing substrates used in printed electronics typically require no absorption. It thus gives freedom for the printed fluid to reshape itself for surface energy minimization after printing. Therefore, in order to make printing more controllable and technologically feasible for printed electronics applications, it is important to understand the nature of printed features and generate design rules that will allow us to print desired features.

While various types of printing techniques exist, the fundamentals of pattern formation are the same. Patterns are built from primitives. For inkjet printing, the primitives are jetted dots. Dots form a line, and lines form a film by merging. For gravure printing, the primitive is a small volume of the ink which is transferred from an individual cell. There has been significant progress on understanding how the morphology and the stability of inkjet-printed lines change as a function of printing parameters and substrate surface energy.[1]–[3] The same efforts must be put on understanding how to print two-dimensional films.

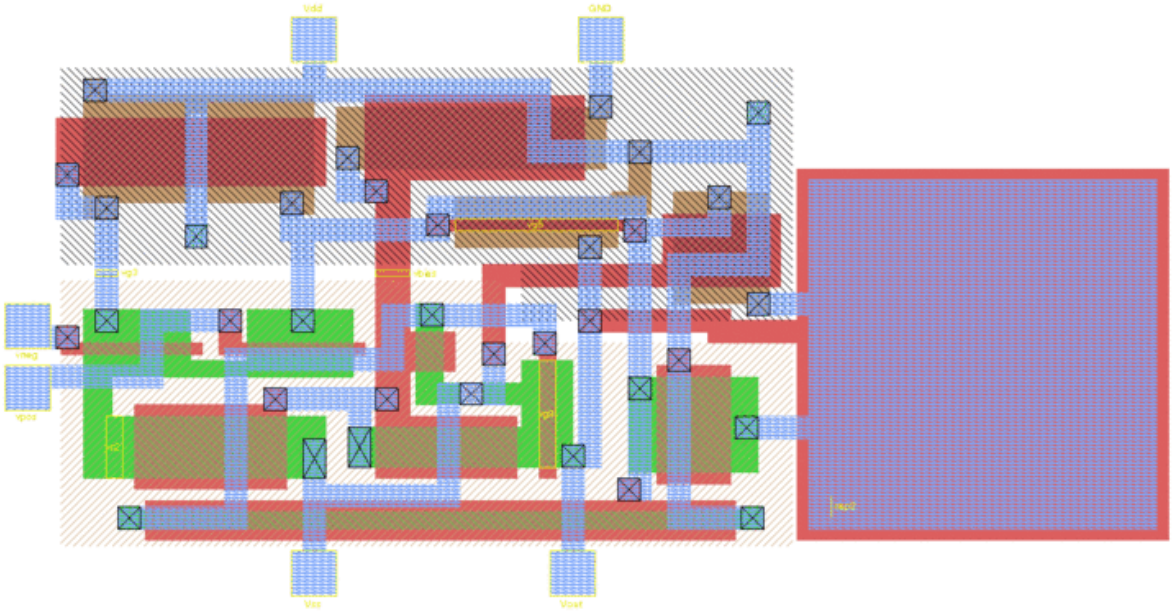


Figure 2.1 An example of a simple circuit layout. It is composed of various geometries such as lines, elbows, crosses, rectangles and squares (found from Google Image search results).

Printed thin films play significant roles in various electronic devices. They are used in thin-film transistors, passive circuit elements, displays, and solar cells. Various aspects of these electrically active printed films need to be understood and controlled in these electronic applications. For example, the size and the thickness of the insulating layer of a transistor or a capacitor have to be controlled for a precise specific capacitance and to avoid leakage. Similarly, for printed light emitting diodes and solar cells, thickness control is required for light emission efficiency and absorption. The surface of printed films needs to be smooth for better field endurance in capacitors and for less carrier scattering in active devices. Therefore, the overall geometry of printed films must be precisely controlled.

An understanding of the various rheological effects that are present during printing of films is thus necessary for the realization of printed devices. Recently, various authors have demonstrated an understanding of drying processes based on the evaporation parameters of inks, causing various surface topographies of printed films to manifest themselves.[4]–[6] To solve some of the observed effects, Tekin et. al. used a multiple-pass inkjet-printing technique to improve homogeneity of a film.[7] The multiple-pass technique, called multilevel matrix in their work, prints matrixes that consist of independent drops and requires back and forth movement of nozzles over the film. They thus offer an experimentally derived solution to film formation challenges in droplet-based printing. Unfortunately, this technique is problematic from a manufacturing perspective, since the multiple passes dramatically reduce throughput and deleteriously impact process cost. It is also not suitable for other printing techniques such as gravure printing in which the patterns must be printed in single pass. What is desired is to obtain a quantifiable understanding of the hydrostatic effects impacting pattern shape control, and to use this understanding to

optimize printing conditions to realize well-controlled shapes. The fundamental understanding can eventually be applied to various types of printing system.

In this chapter, we examine the formation of contiguous film from droplets inkjet-printed in a unitary raster scan, which is more appropriate for faster single-pass printing. We develop a simple analytical framework to establish the limitations imposed by hydrostatic considerations with contact angle hysteresis on pattern formation using the same, thus providing optimization guidelines for formation of films using inkjet printing. This is particularly important, since it established design and printing relationships that determine the limits over which well-defined structures can be printed. This chapter is organized as follows – it begins by explaining the experimental setup in detail, and then establishes the proposed theoretical framework. Then, the implications of the same are examined. After that, experimentally observed phenomena related to film formation are presented, and these are used to develop a quantitative model for film formation. Then the results will be analyzed both qualitatively and quantitatively to form an understanding of the implications of contact angle hysteresis on film formation. Finally, we will discuss how the fundamental understanding can be used to analyze the behavior of gravure-printed films. The concept of contact angle hysteresis which is used throughout this chapter and its general measurement technique are introduced in Appendix 2.7.1.

2.2 Experimental setup, results and qualitative analysis

2.2.1 Experiment setup

To facilitate the development and verification of a model of the hydrostatic considerations in film formation, we study film formation experimentally using droplet-on-demand inkjet printing. Our experiment is conducted with two drop-on demand inkjet printers, a custom-built system based on a Microfab piezoelectric jetting head and the Dimatix Materials Printer DMP-2800. The Microfab system jets 100 pL drops through a single 60 μm orifice at a frequency of about 25 Hz. The Dimatix system jets 10pL drops through up to 16 nozzles at 2 kHz.

For this work, we print a polymer ink, poly(4-vinylphenol), PVP, dissolved in 1-hexanol. PVP is commonly used dielectric material in organic TFTs, with suitable cross-linking.[8], [9] PVP ink usually contains a crosslinker material, but the crosslinker is not included in this experiment to ensure a simpler solvent system. Concentrations of PVP inks used in this experiment are 7.60 wt% and 14.13 wt%. While our experimental data and verification is limited to this important material system, the methodology and modeling developed herein is more generally applicable, provided appropriate parameters are used for different ink systems.

To ensure highly controlled substrate conditions requisite for good modeling, we print on two different glass substrates, Fisher brand No. 12-550C microscope slide (microscope slide) and Corning 1737 (Corning glass) from Corning Inc., a display grade alkaline earth boro-aluminosilicate glass. The glass substrates are cleaned by sequential sonication in soap water, acetone, and isopropyl alcohol for 20 minutes each.

The 7.60 wt% PVP ink on the two glass substrates shows a similar advancing contact angle, but different retreating contact angles, as measured by a Kruss contact angle measurement system. The advancing contact angle for the microscope slide is 27.2±1.5°, and the receding contact angle is close to zero. The advancing contact angle for Corning glass is 26.0±1.5° and receding contact angle is 14.4±0.6°. The advancing and receding contact angles are dynamic contact angle since related to the flow of fluid. The measured diameter of a jetted single drop is about 115 µm for a 100 pL sessile drop and about 45 µm for a 10 pL sessile drop on both substrates.

Printed films, exclusively rectangles in this work, are built up in a raster-scan method with a constant drop spacing. This drop spacing is the same in the slow-print (left-to-right) and fast-print (bottom-to-top) directions as shown in **Figure 2.2**. The PVP films are printed and dried on the printing platen at 30°C. After drying, PVP films are characterized with an optical microscope and a mechanical stylus profilometer.

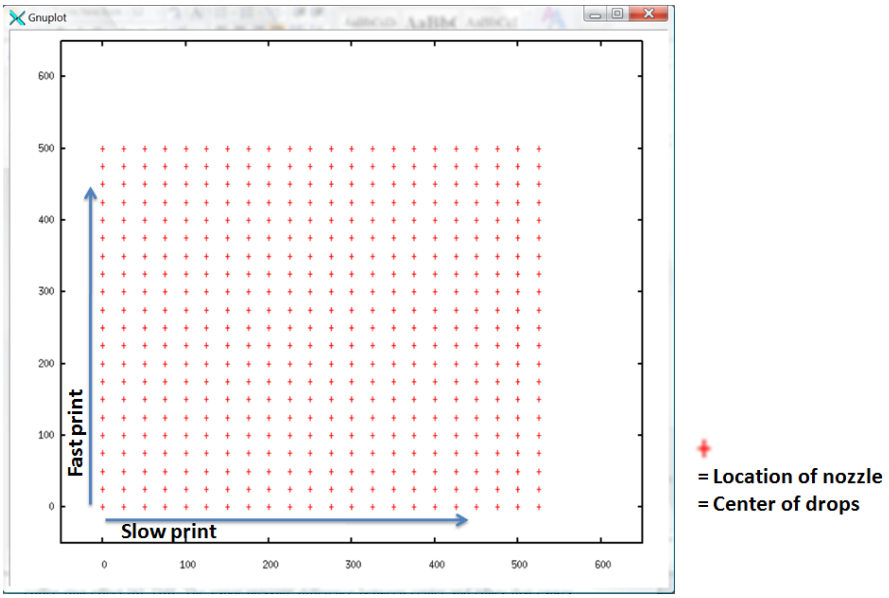


Figure 2.2 A map for inkjet printing drops to form 500 µm square. The red cross mark is where the inkjet nozzle is moved to and jets drops. The jetted drop lands on the spot and spreads to meet equilibrium condition.

Every printed square film in this work shows significant coffee-ring effect around its boundary as shown in **Figure 2.3**. As explained by Deegan et. al., this “coffee ring” is formed due to outward capillary flow caused by pinned contact lines and enhanced evaporate at the edge of a partially wetting film.[10] It has been demonstrated that dual solvent systems with different vapor pressure can suppress the coffee-ring effect [7], [11]. The vapor pressure difference between center and edges, which causes the outward capillary flow, is reduced because the concentration of lower vapor pressure solvent is higher at the edges due to faster evaporation of the solvent with higher vapor pressure. However, the dual-solvent system is not used in this work in order to develop a hydrostatic model based on a single, time-invariant contact angle. Excluding the coffee-ring edges, the

thickness of the films is almost constant since the evaporation rate near the center is constant as shown in **Figure 2.3(b)**. Additionally, we note that the central flat region of dielectric films can be used in organic TFTs despite a coffee ring edge; indeed this structure is advantageous since the central region is extremely flat, unlike the dome-shaped profile commonly observed in films formed using coffee-ring retarding concepts.[12] The average thickness of the central flat region is defined as the thickness of the polymer film in this work. Since the modeling of hydrostatic effects considered in this work is important for timescales before the films dry, the presence of coffee-rings does not influence modeling or verification efforts, nor does it affect the predictive capability of the model. Indeed, the model can be extended to account for multi-solvent systems by introducing time-variant contact angles, but those systems will not be considered here.

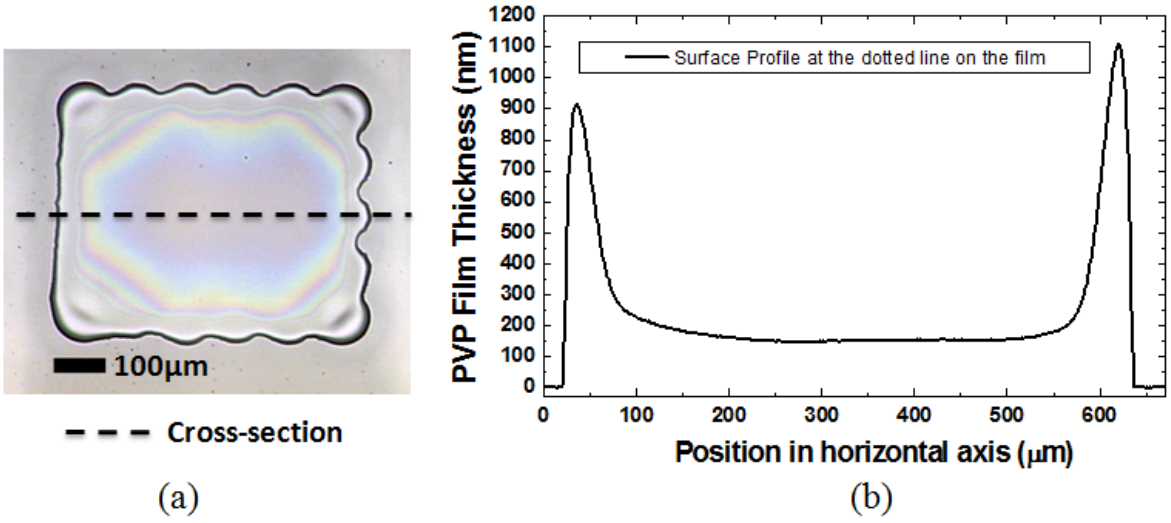


Figure 2.3 (a) Microscope image of a 500 µm square 7.60 wt% PVP film on a microscope slide, which is printed by the custom-built inkjet printer at 100 µm drop spacing (b) Surface profile of this film's cross-section.

2.2.2 Experimental results and qualitative analysis

To collect the requisite data for material development and verification, we investigate how the thickness and pattern fidelity of printed films varies as drop spacing changes. As shown in **Figure 2.4**, the measured thicknesses of 500 µm square films printed by the Microfab system and those of 200 µm square films printed by Dimatix decrease monotonically as drop spacing increases. The minimum thickness in a given ink-substrate system is determined by the spacing required for drop overlap. As shown in **Figure 2.5**, drops do not merge together and the film is separated when drop spacing is larger than the diameter of a single drop. Also the ink concentration affects the thickness of printed films. Doubling the amount of PVP (from 7.6 wt% to 14.13 wt%) yields doubled film thickness. We see the same tendency of monotonically decreasing thickness with increasing drop spacing with the higher concentration ink.

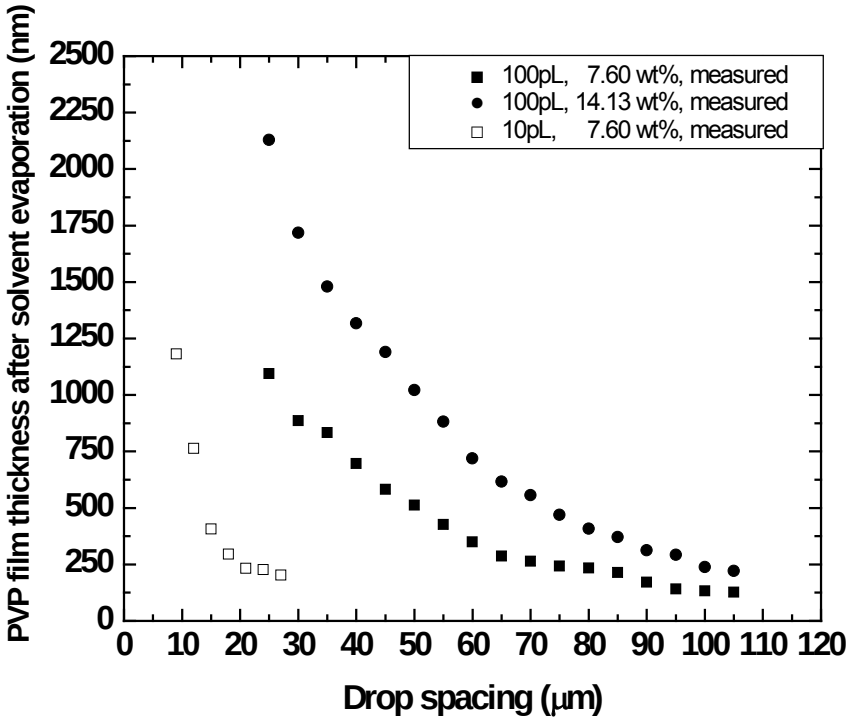


Figure 2.4 Measured PVP film thickness after solvent evaporation. 500 μm square PVP films printed by the Microfab printer (115.5 μm diameter of a circular cap on Corning 1737) and 200 μm by the Dimatix printer (45 μm diameter).

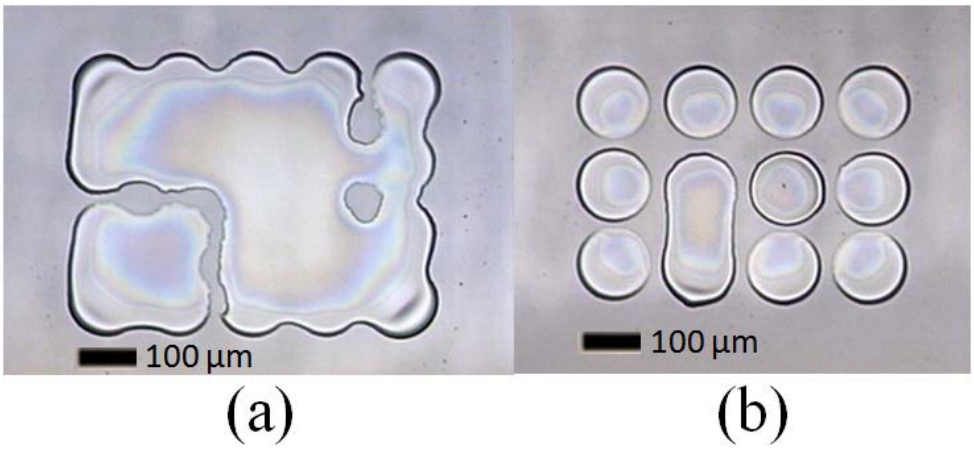


Figure 2.5 Microscope image of 500 μm square 7.60 wt% PVP films on Corning 1737; drop spacing/diameter of a single drop (a) 1.04, (b) 1.21.

In addition to the film thickness, the shape of the formed films also varies as the drop spacing changes. As drop spacing decreases, the square film starts bulging at the left edge and eventually bulges on every edge at sufficiently low spacing, forming a circular shape as shown in **Figure 2.6**.

We observe another interesting phenomenon when we print larger films. The film may separate into smaller beads as we try to print larger film. This results in the pattern breakup

shown in **Figure 2.7**. The top-right corner drops, which are jetted last, are separated from the film with 40 µm drop spacing. Larger drop spacing results in more severe film breakup.

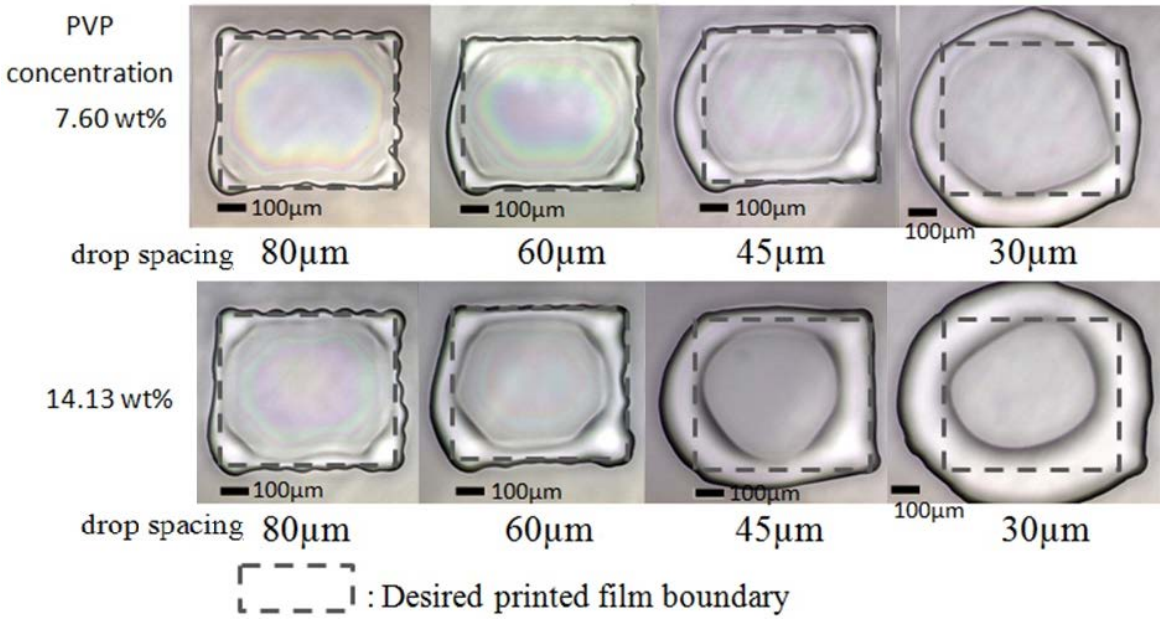


Figure 2.6 Microscope images of 500 µm square 7.60 wt% PVP films on Corning 1737 printed with labeled ink, at labeled drop spacing.

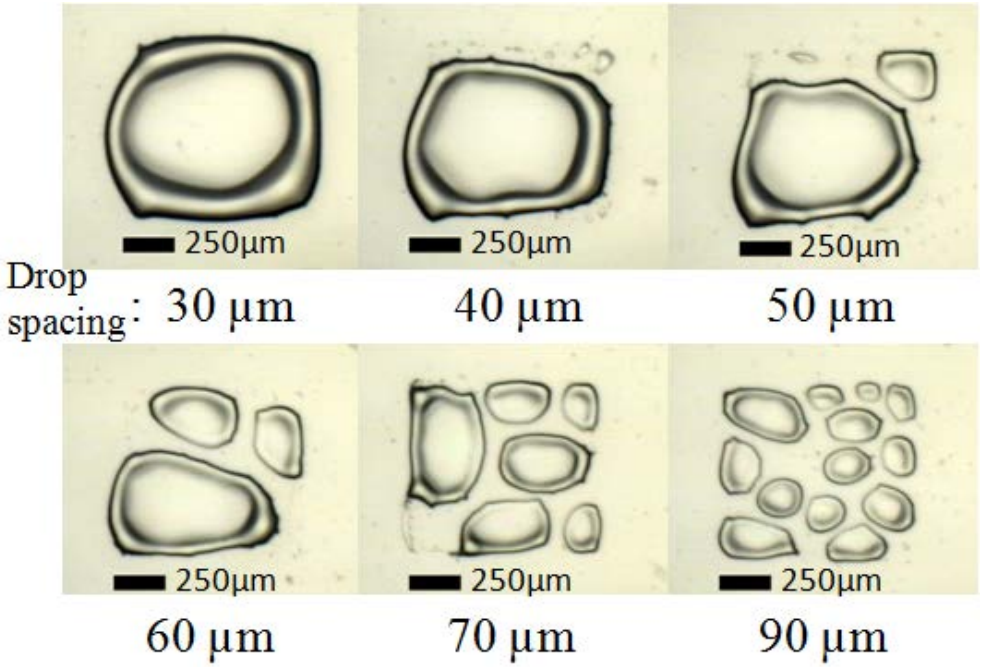


Figure 2.7 Film separation of 1mm square 7.60 wt% PVP film on Corning 1737 as drop spacing increases.

In a uniform film, assumed to be much thinner than the upper limit on film thickness imposed by gravity (see 2.7.2.), the final PVP film thickness is determined by the total volume of PVP ink per unit area. Assuming constant drop spacing in both print directions, the number of jetted drops in printed films of the same size is inversely proportional to this constant drop spacing value. Therefore, the thickness of the film decreases monotonically as drop spacing increases.

If the volume of ink in a film is too much such that contact angle at the edges of the film is higher than the requisite advancing contact angle, then the boundary of the film expands as the excess ink flows outward to form an appropriate advancing contact angle at the edges for surface energy minimization. Since we raster-scan the film from left to right, the contact angle at each edge of the printed bead decreases as more lines are added to the right. Therefore, in **Figure 2.6**, bulging tends to occur on the left hand side when the contact angle is initially higher than advancing contact angle. As the contact angle falls beneath the advancing contact angle, the bulging does not occur any more, resulting no bulging on the right hand side. When more lines are added with relatively large drop spacing, the contact angle continues to decrease and fall beneath the receding contact angle. It then causes the right edge to be pulled to the left, resulting in scalloped morphology.

In order to understand the film breakup, we also need to consider the retreating contact angle. As the wetted footprint of a pattern is expanded through further printing, the growing bead's contact angle may fall due to geometric considerations depending on the volume of ink deposited per increase in substrate area covered. If a growing bead's contact angle falls beneath the receding contact angle as printing proceeds, the contact line will retreat. Thus, the film breakup occurs as we print larger films. If the receding contact angle is near zero which means almost total pinning, then the film breakup does not happen because the bead's contact angle is always higher than the receding contact angle. In case of printed features on the microscope slide whose retreating contact angle is near zero, 2 mm square films are able to be printed with almost no breakup as shown in **Figure 2.8**. Although the film with 100 μm spacing shows small inside breakups, the films maintain their square boundary very well. As shown in **Figure 2.9**, even larger films including 5 mm square film can also be printed on the same substrate, which is impossible on the Corning 1737 glass which has a smaller contact angle hysteresis.

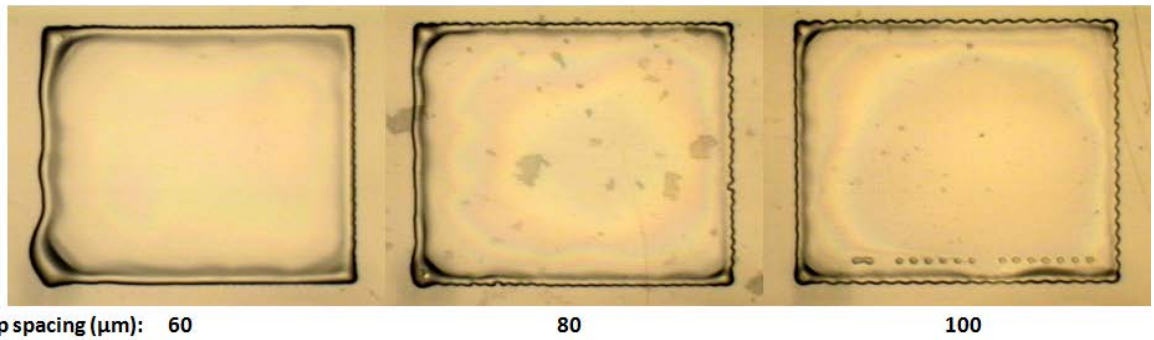


Figure 2.8 2mm square films of 7.60 wt% PVP film on the microscope slide with different drop spacing.

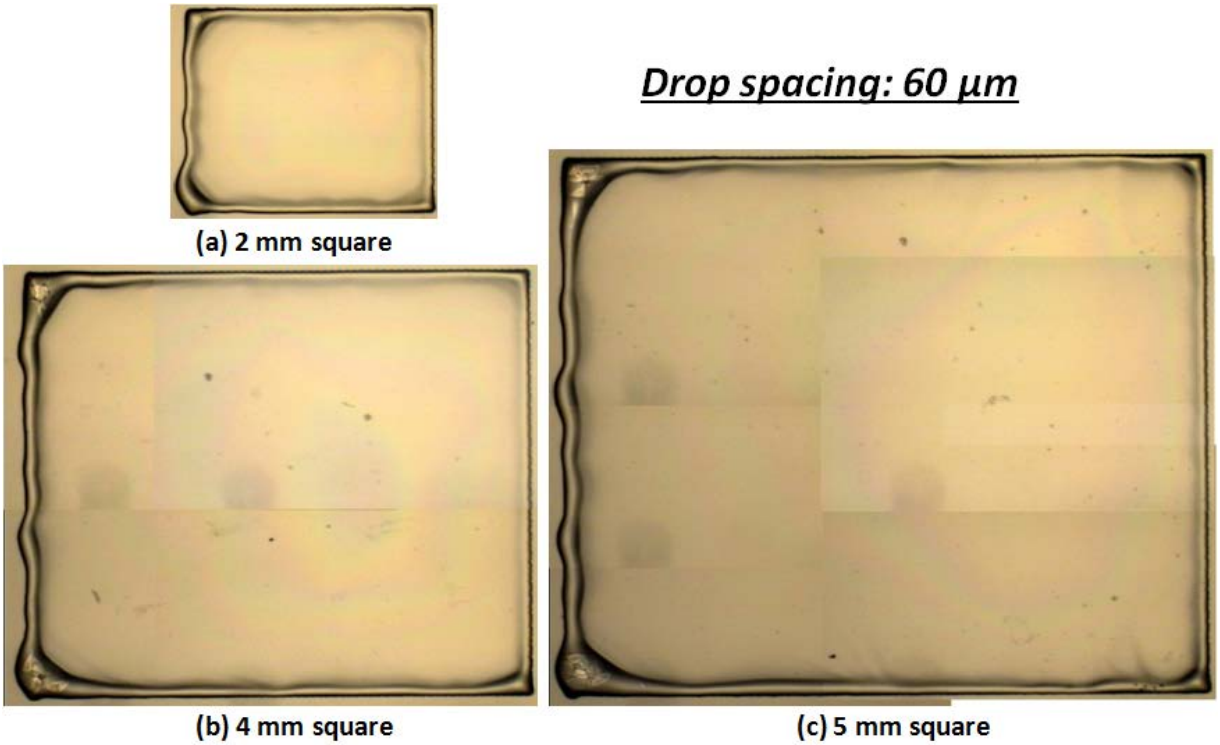


Figure 2.9 Square films of 7.60 wt% PVP on the microscope slide with 60 µm drop spacing; size of (a) 2 mm, (b) 4 mm and (c) 5 mm.

2.3 Quantitative analysis based on 1D hydrostatic model

To proceed with development of analytical models for film formation, we examine film thickness limitations as well as pattern fidelity limitations as a function of hydrostatic considerations.

2.3.1 Inkjet-printed film thickness model

As discussed in the previous section, PVP film thickness is determined by the total volume of PVP ink per unit area. Assuming that a printed film is large compared to the size of a single drop, the final thickness of the dried printed film, h, is proportional to the drying ratio and the total volume of the film and inversely proportional to the area of the film:

$$h = C \times \frac{n^2 V_{drop}}{(nd)^2} = C \frac{V_{drop}}{d^2} \tag{1}$$

where the volume of a single drop is V_{drop}, the drop spacing is d, C is experimentally extracted drying ratio, and the number of lines forming the square is n. However, if the size of a wetting drop approaches the size of the printed film, the size of the drop has to be included in the area of the film. If the center of drop is jetted onto the square of designed size, then the total area of printed square includes the extended boundary of jetted drop

radius, 2*R* on both sides. It is significant when the radius is comparable to the size of the film. Assuming two sides of a rectangle film shown in **Figure 2.10** are a and b, the radius of a single drop is *R*, the volume of a single drop is V_{drop}, the drop spacing is *d* and *C* is experimentally extracted drying ratio, the thickness of the dried printed film, *h*, can be derived in the following way.

$$h = \frac{(drying\ ratio) \times (total\ volume\ of\ a\ film)}{(total\ area\ of\ a\ film\ with\ extended\ boundary)}$$

$$= C \times \left\{ \left(\frac{a}{d} + 1 \right) \times \left(\frac{b}{d} + 1 \right) \times V_{drop} \right\} \div \{(a + 2R) \times (b + 2R)\}$$

$$= C \times \left\{ \frac{a + d}{(a + 2R)d} \right\}^2 V_{drop} \ (\ for\ square\ film, a = b) \qquad (2)$$

$$where\ R = \sqrt[3]{\frac{\sin^3 \theta}{\pi \left(-\cos\theta + \frac{1}{3}\cos^3 \theta + \frac{2}{3} \right)} V_{drop}}$$

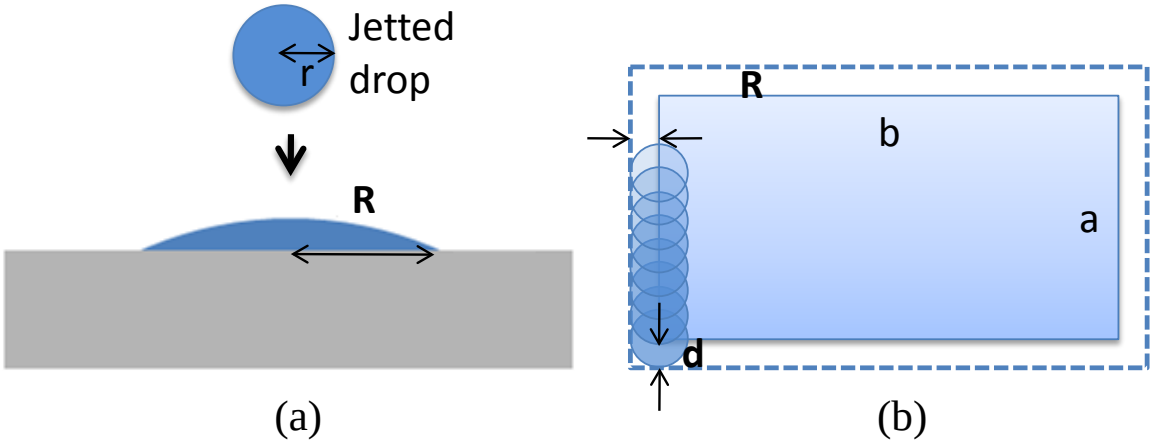


Figure 2.10 (a) Independent drop jetted onto a partial wetting substrate, which has a spherical cap shape with radius, R. (b) Printed rectangle with extended boundary caused by the drop radius, which has a designed size of a and b for each side.

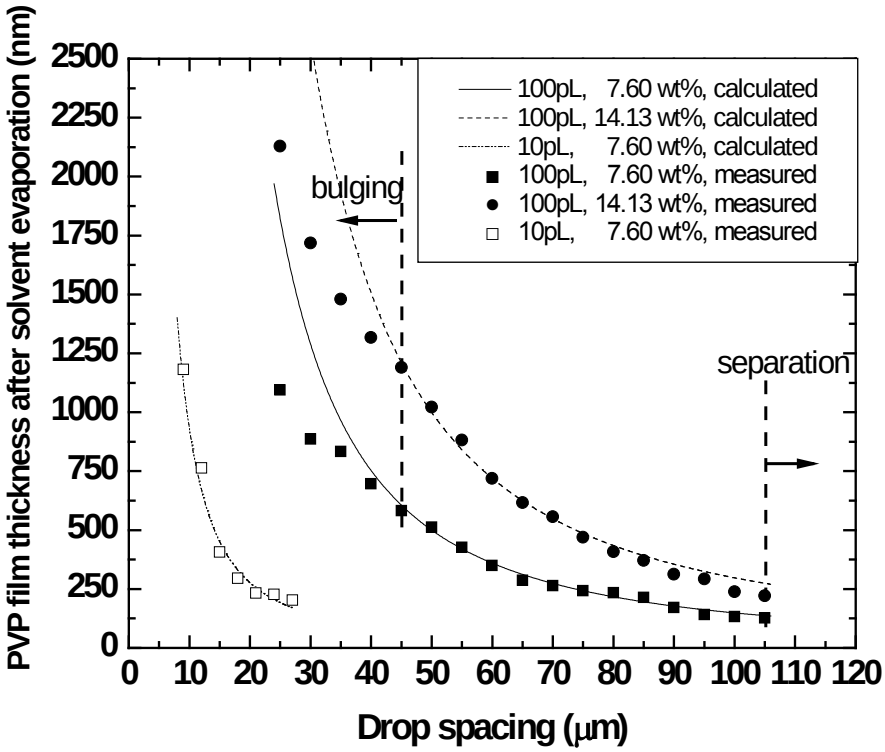


Figure 2.11 Film thickness modeling of equation (2) is fitted to the measurement data presented in Figure 2.4.

The film thickness model including extended boundary shows a good accordance with measured data from both printer systems as shown in **Figure 2.11**. However, at smaller drop spacing the measured film thickness data for the 100 pL drop Microfab system deviates from the model in a bulging phenomenon. The edges of a film bulge when a film is printed with smaller drop spacing. (See **Figure 2.6**) The increased area caused by bulging eventually decreases the ink volume per unit area, resulting in the deviation seen in the measured data at smaller drop spacing in **Figure 2.11**. The bulging phenomenon also distorts the shape of desired patterns. In order to increase the maximum thickness beyond what can be reached due to bulging, the ink concentration can be increased.

2.3.2 Bulging of printed film beyond advancing contact angle

First, we develop a simple hydrostatic model for the width of merged lines to understand the bulging phenomena quantitatively. By comparing the contact angle at the edge of merged lines with advancing contact angle, we can determine whether a bead bulges or not.

2.3.2.1 Two lines impinging

The cross-section of a single line can be assumed as a cylindrical cap (The bond number for our lines is $2 \cdot 10^{-3}$), darker area A1 in **Figure 2.12**. The area A1 can be calculated by subtracting A2, the triangle area, from the sector whose central angle is 2θ.

$$A1 = A_{sector} - A_{triangle} = \frac{R^2}{2}(2\theta - \sin 2\theta) \tag{3}$$

$$W = 2R\sin\theta \tag{4}$$

$$A1 = \frac{W^2}{8\sin^2\theta}(2\theta - \sin 2\theta) \tag{5}$$

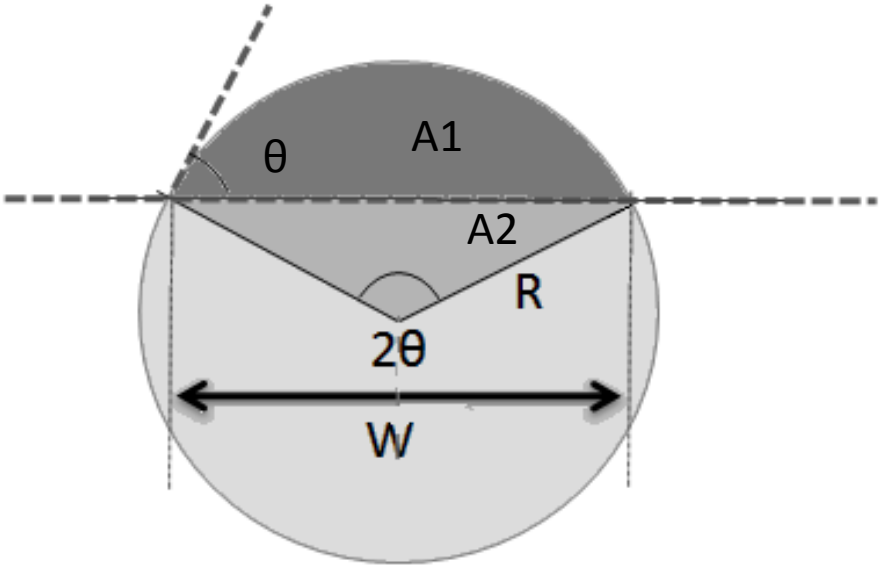


Figure 2.12 Circular segment geometry. The circular segment, A1, can be assumed as a cross-sectional area of a single line. Therefore, θ is equilibrium contact angle and W is the width of a single line.

Thus, its width is determined only by its contact angle and the cross-section area of the cylindrical cap line. Since the cross-section area of a stable line is determined by the total volume of a bead over the line length, the area is simply expressed as (6).

$$A1 = \frac{(number\ of\ drops)\times V_{drop}}{(number\ of\ drops)\times d} = \frac{V_{drop}}{d} \tag{6}$$

By combining (5) and (6), the width of a single cylindrical cap line is given as (7).

$$W_{single} = \sqrt{\frac{8\sin^2\theta V_{drop}}{(2\theta - \sin 2\theta)d}} = K\sqrt{\frac{V_{drop}}{d}} \tag{7}$$

where K is equal to 3.59 for the advancing contact angle of 7.60 wt% PVP ink, 26.0°. After the first line is printed with drop spacing, d, from bottom to top as in **Figure 2.13(b)**, the second line is printed next to the first line with spacing, d, to the right. The cross-sectional view when the second line is printed is shown in **Figure 2.13(c)**. When the spacing between two lines is less than the width of a single line, the second line touches the first printed line, and the two lines merge into a single bead (we ignore evaporation of solvent between printing of successive lines in this analysis; for typical printing speeds and solvent

evaporation rates, this is a good assumption for successively printed lines in our experiment). At that point, the width of two merged lines is the sum of width of the first line and the distance over which the second line spreads as shown in **Figure 2.13(c)** and (8).

$$W_{merged} = W_{\sin gle} + 2\left(d - \frac{W_{\sin gle}}{2}\right) = 2d \tag{8}$$

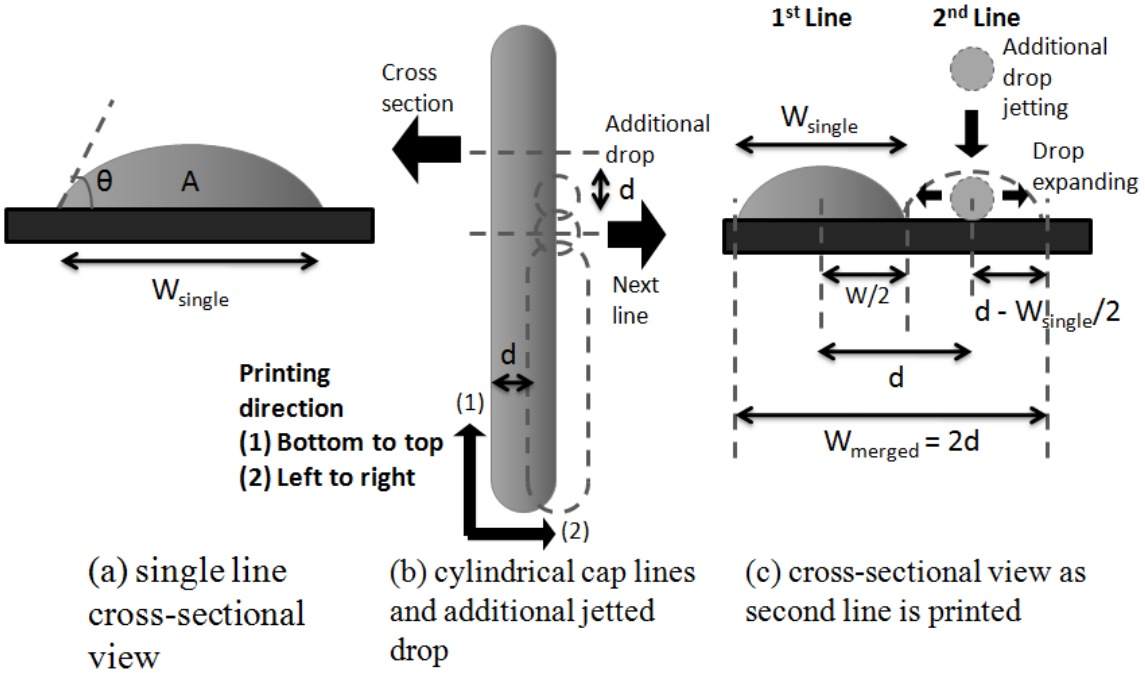


Figure 2.13 Geometry of printed film; (a) single line cross-sectional view (b) cylindrical cap lines and additional jetted drop (c) cross-sectional view as second line is printed.

After the two lines merge, any further spreading is determined by the advancing contact angle for the new bead. We now endeavor to compare the widths of a just-merged bead with that of the same bead spread to its equilibrium width. Substituting twice the ink volume into equation (7) to represent two lines worth of printed drops, we find that the width of the new bead is simply $\sqrt{2}W_{single}$.

If the merged line width, found with equation (8), is smaller than the line width maintaining the advancing contact angle, $\sqrt{2}\ W_{single}$ for two lines, then the contact angle on each side of the merged bead is larger than the advancing contact angle. Consequently the bead will flow until its contact angle is reduced to the advancing contact angle. This outflow is the bulging phenomenon seen in **Figure 2.6**.

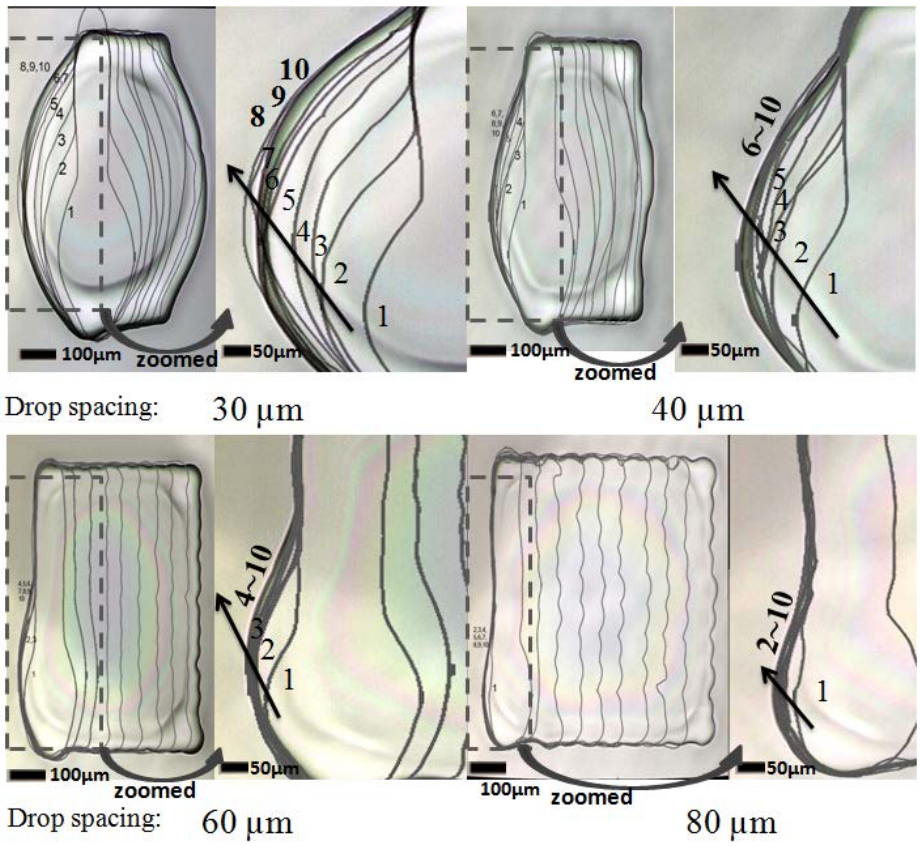
2.3.2.2 Generalization to many printed lines

The same approach can be extended to multiple lines as well. Bulging continues whenever a new line adds fluid such that the new, merged bead would exceed its advancing contact angle. Replacing two lines worth of ink in the case of two lines impinging with n,

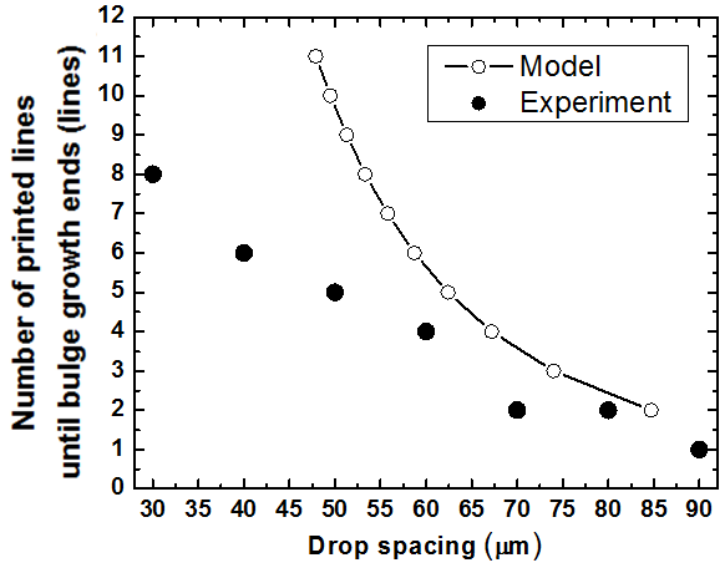
the number of printed lines, it is possible to use the same method to determine the bulging growth when n^{th} line is added, leading to the following inequality (9) for the condition where the contact angle of the merged bead is less than or equal to the advancing contact angle.

$$\frac{d}{W_{single}} \geq \frac{1}{\sqrt{n}} \tag{9}$$

When the inequality (9) is satisfied, the printed bead stops bulging. Therefore, the number of lines that have to be printed to stop bulging for a certain constant drop spacing can be calculated and is shown in **Figure 2.14(b)**. To test the model, ten lines are sequentially printed from the left to the right. The boundary of each dried feature is extracted, aligned, and overlaid in **Figure 2.14(a)**. Since only the left hand side bulging extends beyond the feature's footprint, we look there to view the bulge's growth. At smaller drop spacing, more lines are printed before the film contact angle falls beneath the advancing contact angle. Measured data show a good fit when the drop spacing is large, but it deviates from the model at smaller drop spacing. The model predicts more lines than what are actually observed to grow a bulge. This error is likely due to evaporation losses, which have not been accounted for in the above analysis. Because it takes more time to print the same length of line with smaller drop spacing, more evaporation occurs, removing ink that would otherwise contribute to the bulge. As shown in **Figure 2.14(a)**, the bulging always begins from the bottom of each line. As Duineveld explained the bulging phenomenon in his work, the bulge occurs near the starting point of printing due to the transition from spherical to cylindrical shape. Because the end of a line where drops are added has higher pressure due to extra curvature there, the added liquid flows toward the initial bulge where the pressure is lower, and the initial bulge is enlarged instead of equalizing the width of a line.



(a)



(b)

Figure 2.14 (a) Overlays of one to ten sequentially printed 750 μm 7.60 wt% PVP lines at noted drop spacing on Corning 1737 (100 pL drop volume). Left edge is zoomed 1.5 times horizontally and 3 times vertically from the left full image of beads. The boundary of each step is extracted and overlapped with first printed line. (b) The number of lines until bulge growth ends at different drop spacing for our hydrostatic model and experiment data in (a).

2.3.3 Separation of printed film below receding contact angle

2.3.3.1 Film separation model

The film breakup phenomenon seen in **Figure 2.7** can also be explained by the 1D simple hydrostatic model developed in the previous section. When the equality in (9) is satisfied, the merged bead has the contact angle which defines W_{single}. Based on the 1D hydrostatic model, the width of merged lines which have a contact angle, θ, on each side is determined by the contact angle, drop spacing, drop volume and number of printed lines as in equation (10).

$$\begin{aligned} W_{equilibrium} &= f(d,n,\theta) \\ &= K(\theta)\sqrt{\frac{V_{drop}}{d}}\sqrt{n} \\ &= \sqrt{n}W_{\mathrm{sin}\,gle} \end{aligned} \tag{10}$$

As shown in **Figure 2.13(c)** and (8), the width of merged bead is nd. If $W_{equilibrium}$ in (10) is the same as nd, then the merged bead can stay at the contact angle in (10) and does not require spreading to meet the hydrostatic equilibrium. From this relationship, the width of a bead which has a certain contact angle on each side for certain drop spacing can be obtained as (12).

$$\begin{aligned} W_{equilibrium} &= W_{merged} \\ \sqrt{n}W_{\mathrm{sin}\,gle} &= nd \\ K(\theta)\sqrt{V_{drop}}\sqrt{\frac{n}{d}} &= nd \\ \frac{K(\theta)\sqrt{V_{drop}}}{d^{\frac{3}{2}}} &= \sqrt{n} \end{aligned} \tag{11}$$

$$W_{equilibrium} = \frac{K(\theta)\sqrt{V_{drop}}}{\sqrt{d}}\left(\sqrt{n}\right) = \frac{K(\theta)\sqrt{V_{drop}}}{\sqrt{d}}\left(\frac{K(\theta)\sqrt{V_{drop}}}{d^{\frac{3}{2}}}\right) = \frac{K^2(\theta)V_{drop}}{d^2} \tag{12}$$

where $K(\theta)$ is equal to 3.59 for $\theta_{advancing}$ of 7.60 wt% PVP ink, 26.0° and $K(\theta)$ is equal to 4.87 for $\theta_{receding}$, 14.4°. By using the equation (12), it is possible to set up a framework as shown in **Figure 2.15** to anticipate the contact angle of a printed bead of a given width, printed at a given drop spacing. Based on the established boundaries for bulging, proper shape definition, and bead separation, we can then predict the specific regime within which a pattern will be printed.

Our 1D hydrostatic model has an assumption of infinite length of the bead. Therefore, the model has a limitation to be accurately applied to 2 dimensional square films. However, the framework in **Figure 2.15** is useful to roughly anticipate the behavior of printed square films since the square films consist of merged lines. As shown in **Figure 2.15**, printed square films fit well into the boundaries defined by our 1D hydrostatic model. If drop

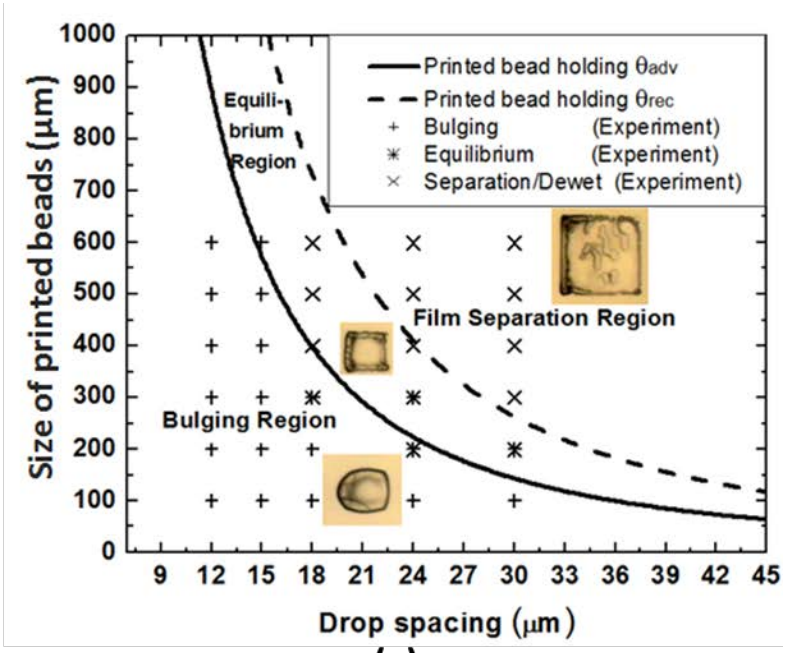
spacing and film size is below the line defined by equation (12) with advancing contact angle (K=3.59), films mostly show bulging behavior. If a film is located above the line defined by equation (12) with receding contact angle (K=4.87), the printed film either dewets or breaks up into smaller beads. Printed films located between those two lines tend to retain a stable square shape. There is a tendency for films to be separated at smaller size or smaller drop spacing than critical values of size or drop spacing. This is likely caused by two issues. Firstly, the 1D model cannot accurately predict the contact angle of square films, and secondly the total volume of the films is reduced due to evaporation of solvent as films are printed. However, despite these errors, we in all cases we clearly see that hydrostatic concerns prove to define the experimental space within which uniform films can be printed.

2.3.3.2 Multiple nozzle printing

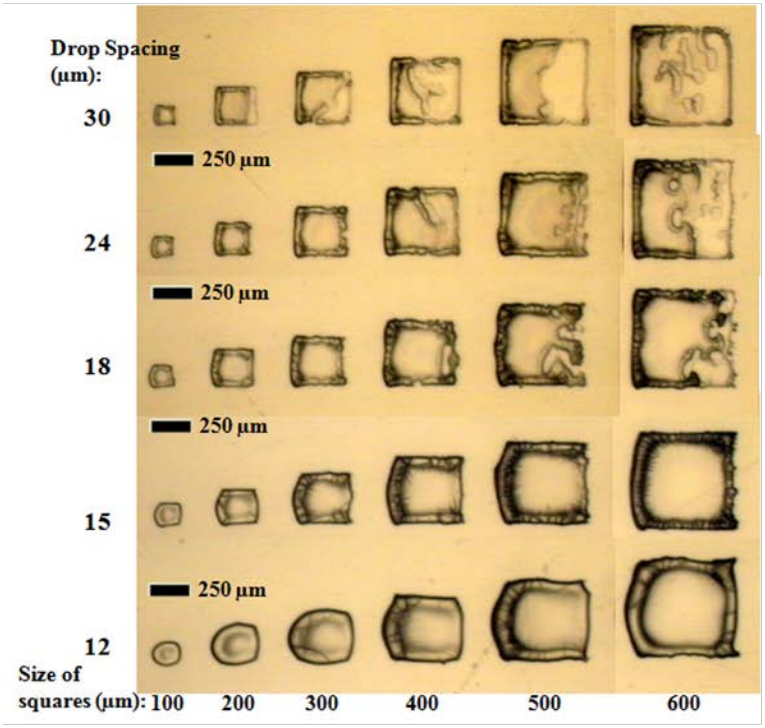
Although much inkjet printing research has been done with single nozzle systems, multiple nozzle printing is desirable for higher throughput. Even if single nozzle printing results show good fitting to the model, unexpected characteristics such as asymmetric edge shape and earlier film-separation tendency have been observed due to unconsidered evaporation in the model. When lines are printed with shorter time intervals or at the same time using multiple nozzles, it is acceptable to ignore evaporation of ink during printing and evaporation-induced pinning.

In A-1 of **Figure 2.16**, the left edge is observed to bulge, but the right edge slightly dewets the surface, showing asymmetry. However, when six nozzles are used to print the same film in A-2 of **Figure 2.16**, bulging is observed on both sides, and therefore the pattern becomes more symmetrical. Based on the hydrostatic condition, the film is also within the bulging region. Since it takes a smaller amount of time to form the pattern when performing multiple nozzle printing, evaporation is suppressed during printing and thus, there is less change of total volume. As shown in B-1,2 of **Figure 2.16**, multiple-nozzle printed films dewet slightly, but do not break up; a single-nozzle printed film of the same size with the same drop spacing is separated, however. However, due to quicker printing, the amount of time taken for forming evaporation-induced pinned line edges is also decreased, resulting in a more surface-energy minimized round shape. This is more clearly observed in (C-1 and 2) of **Figure 2.16**. In C-1, a single nozzle allows enough time for printed lines to be dried and pinned, but the last portion of the printed volume is separated for surface energy minimization. Therefore, the square film still maintains its square boundary. However, in C-2, six-nozzle-printing jets the total volume of ink before the square boundary is formed and the boundary lines recede to minimize the surface energy. These thus form more clearly separated smaller films.

Overall, we see that the same hydrostatic conditions should be also considered in printing films with multiple nozzles in the same way as we did with a single nozzle; considering these, we note that multiple-nozzle printed films have symmetry in their shape and tend to fit the simple hydrostatic model slightly better due to slower evaporation relative to print speed. The tendencies discussed are seen in **Figure 2.17** as well.



(a)



(b)

Figure 2.15 (a) Printed film shape determination based on the size and drop spacing of the film (b) 7.60 wt% PVP films with different size and drop spacing (10 pL drop volume, single nozzle used, on Corning 1737)

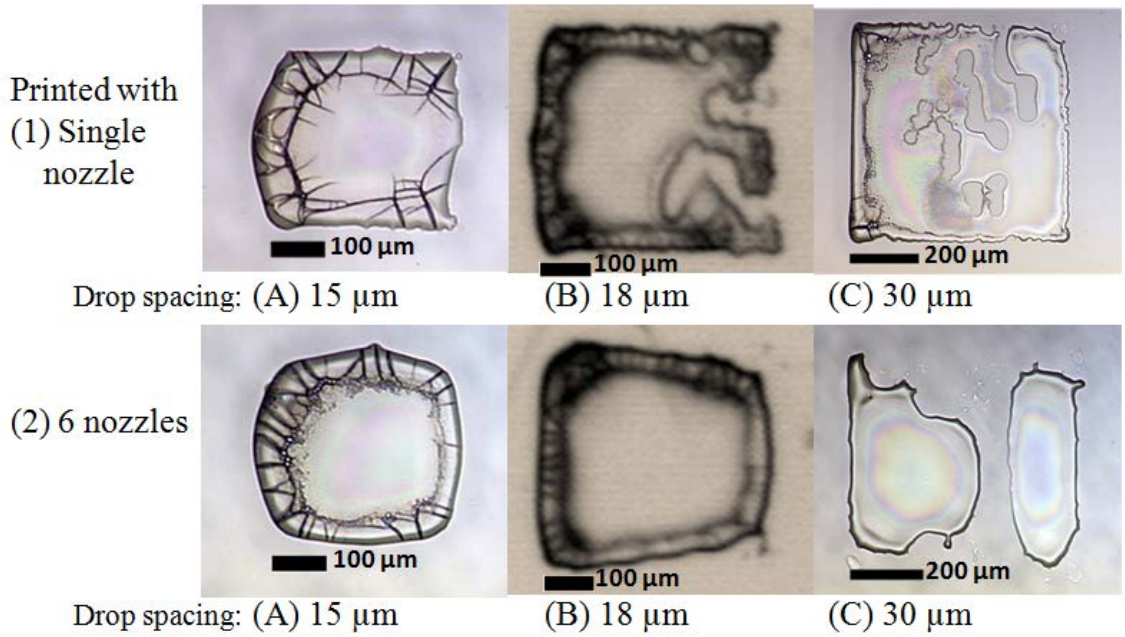


Figure 2.16 Identical films printed with different numbers of nozzles used. (A) 300 µm square is printed with 15 µm drop spacing, (B) 500 µm square with 18 µm drop spacing and (C) 600 µm square with 30 µm drop spacing both by single nozzle (1) and six nozzles (2).

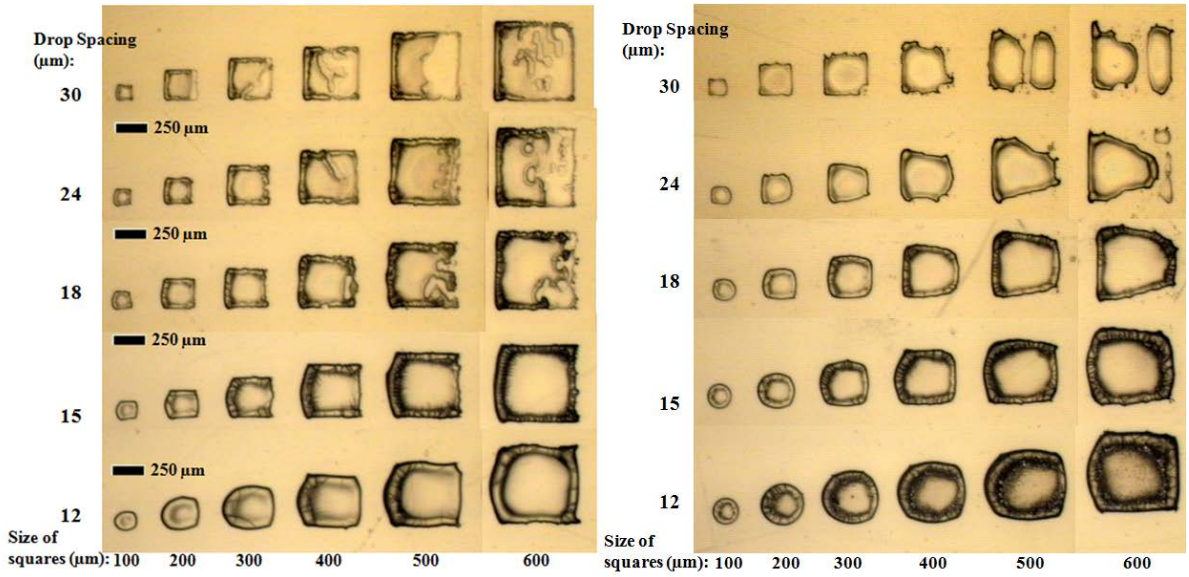


Figure 2.17 Identical films printed with different numbers of nozzles used; (A) printed with single nozzle (B) printed with 6 nozzles.

2.4 Gravure Printed Films

As mentioned in Chapter 1, high-throughput roll-to-roll printing is necessary for many printed electronics applications. Among the various high-throughput printing techniques available, we mentioned gravure printing is of particular interest due to its high resolution printing capability and good pattern fidelity. However, compared to inkjet printing, gravure printing is relatively not studied. In the previous section, we mentioned that the pattern formation of printed fluids is fundamentally similar regardless of the printing techniques. Therefore, the knowledge developed from the inkjet-printed film study above can also be applied to impression printing systems including gravure printing. However, differences exist. For example, the inkjet-printing process is divided into two steps; (1) jetting of droplets, (2) pattern formation after landing on the substrate. However, in gravure printing, the entire process is more complex. The most significant difference is how the ink is transferred to the substrate; (1) filling of engraved cells with ink, (2) wiping of the ink by doctor blade, and (3) the transfer of the ink from the cell to the substrate. After the ink transfer, pattern formation on the substrate is fundamentally the same as in the inkjet printing, which is essentially surface energy minimization within the contact angle hysteresis.

Understanding the complex printing process of gravure printing is challenging particularly because it is hard to separate the three step processes experimentally and hard to theoretically model the processes. While there are both simulation efforts [13] and experimental efforts on simplified systems[14]–[16], bridging the gap between the two approaches is still not established yet. Recently, there have been significant efforts on understanding each step both experimentally and theoretically.[17]–[19] While the importance of the doctor blade wiping process is revealed by the works, accurate estimation or calculation of each step is still an ongoing work.

In this subchapter, the effects of various parameters on gravure printed film formation will be discussed. Differences and similarities between gravure printing and inkjet printing will also be discussed.

2.4.1 Effect of contact angles

Another difference between gravure printing and inkjet printing with respect to pattern formation is the non-possibility of non-zero spacing between the primitives in gravure printing, unlike in inkjet printing. In other words, while the center-to-center drop spacing can be smaller than the size of the droplet or even zero in inkjet printing, the center-to-center spacing between cells will always be larger than the size of the cells. Thus, the pattern formation in gravure-printed features always starts from individual dots. After the dots from cells are transferred, they spread to minimize the surface energy until touching each other to be merged. What determines the size of the dot is the equilibrium contact angle. Therefore, it is important to see the effect of the contact angle on gravure-printed films.

In order to see the effect of the contact angle, gravure printing experiments are designed in the following way. UV/Ozone cleaning time on a chosen plastic substrate is varied to

obtain different contact angles on the substrate. From the inkjet-printed film study above, we learned the importance of receding contact angle. Since lower receding contact angle prevents de-wetting of the film, the plastic substrates with low receding contact angles were chosen for gravure-printing. In this experiment, planarized polyethylene napthalate (PEN) substrates with two different coatings and a polyethylene terephthalate (PET) substrate are used. The two PEN substrates are respectively called PEN-B and PQA1 throughout this thesis. The equilibrium contact angle was varied from 50° down to 20° as shown in **Figure 2.18**. The ink printed here is the same as what was inkjet-printed earlier, poly(4-vinylphenol), PVP, dissolved in 1-hexanol. However, the concentration of the polymer is higher for a higher ink viscosity, which is more suitable for gravure printing. Inks with PVP weight% of 7.6, 14.1 and 19.8 have viscosities of 10, 30 and 90 cP, respectively.

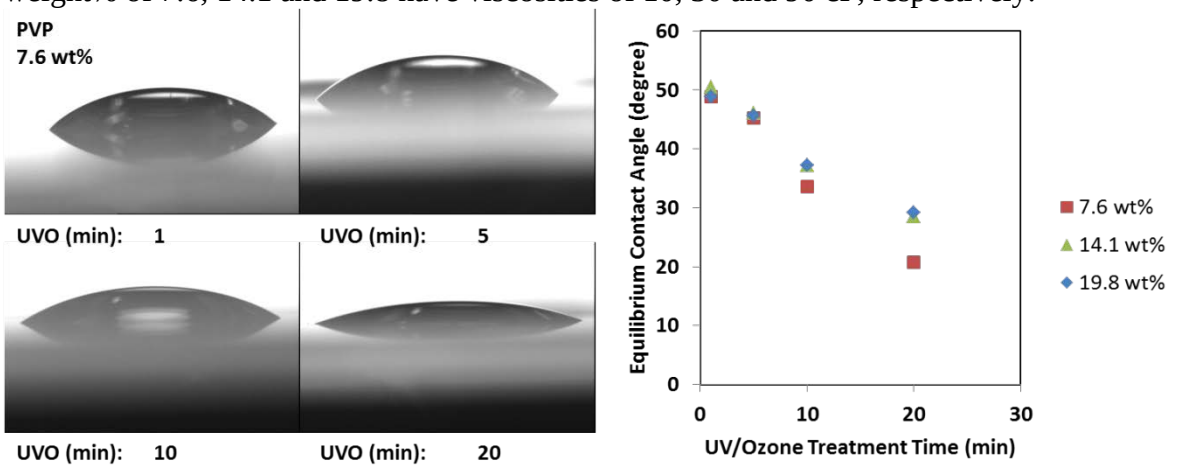


Figure 2.18 Equilibrium contact angle of PVP in 1-hexanol with different concentration on PEN-B substrate treated with different UV/Ozone cleaning time.

Gravure-printed PVP square films with 19.8 wt% of PVP ink on PEN-B are presented in **Figure 2.19**. When the substrate surface is UV/Ozone cleaned for 20 minutes, the printed films are much more complete than the case of 10 minute UV/Ozone treatment. Even when the printed film is almost an array of individual dots in the case of 10 minute UV/Ozone cleaned substrate (CW: 10 μm, CS: 5 μm), the dots are more connected and thus the film is at least partially formed when the substrate is UV/Ozone cleaned for 20 minutes. It is possible to qualitatively explain the observation based on the understanding of the previous inkjet-printed film study. When the contact angle is lower, the printed dots from the engraved cells have larger diameter. Therefore, the printed dots can be more easily connected, forming more complete films. When the dots are large enough to overcome the spacing between cells and thus become connected, the contact angle plays a role to determine the stability of the film. If the surface energy is higher due to longer UV/Ozone cleaning time, then the range of contact angles the ink fluid can have is lower. Therefore, the fluid can maintain the film shape without separation. In other words, the equilibrium region in **Figure 2.15(a)** is thus shifted towards the upper right direction. Thus, for the same amount of ink volume, larger films can be formed without de-wetting. Similar behavior is observed on a different substrate. The same ink is printed on PQA1 substrate as shown in **Figure 2.21**. As the contact angle on the substrate increases, the contact lines of

the printed film around the boundary start receding, thus showing deviation from a perfect square shape.

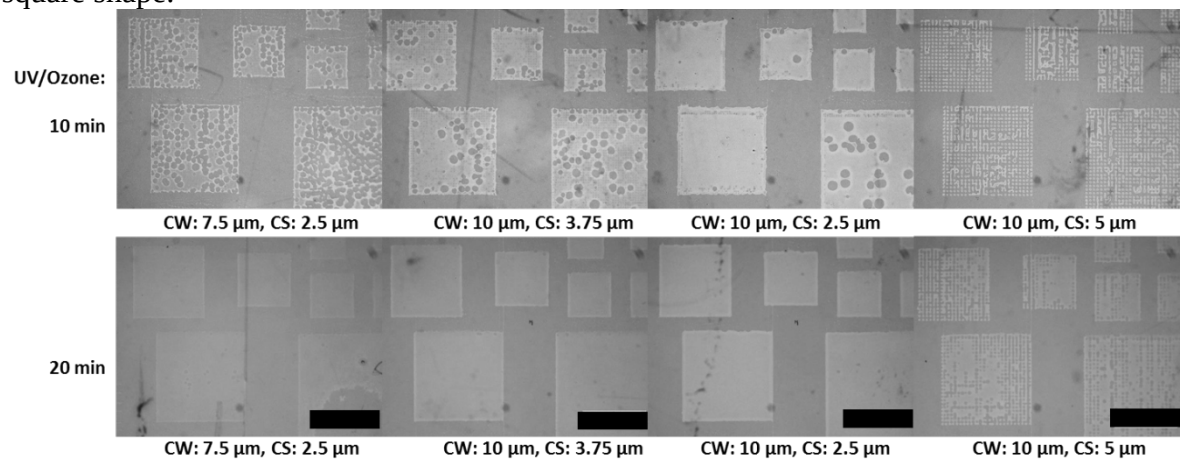


Figure 2.19 Gravure printed PVP square films on PEN-B. UV/Ozone treatment condition and engraved cell parameters are variables. Cell parameters (CW: cell width, CS: side-to-side cell spacing) are defined in Figure 2.20. The black scale bar represents 400 µm.

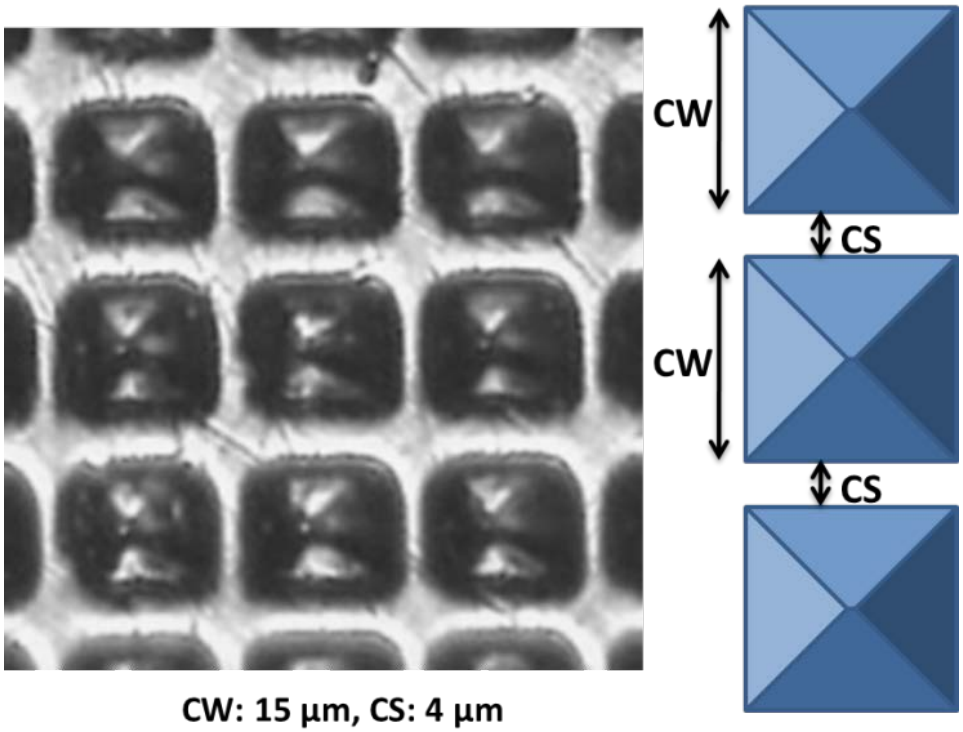


Figure 2.20 Micrograph of electromechanically engraved gravure cells, and the definition of cell parameters. (CW: cell width, CS: side-to-side cell spacing)

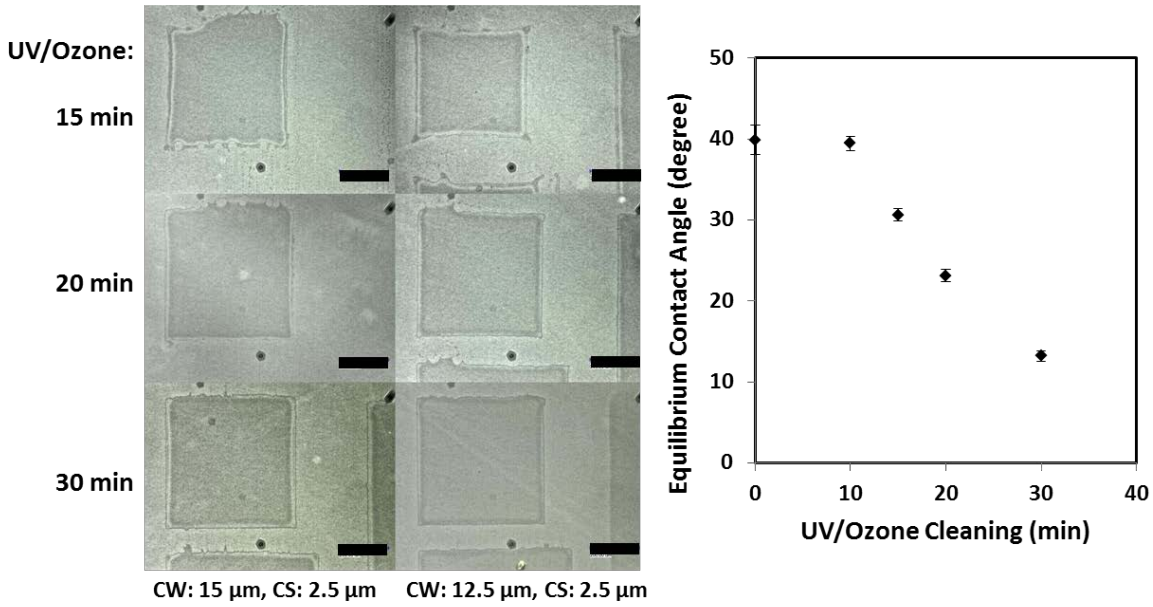


Figure 2.21 Micrographs of gravure-printed 19.8 wt% PVP square films on PQA1, and the effect of UV/Ozone cleaning time on the equilibrium contact angle of the PVP ink on PQA1. The black scale bar represents 200 µm.

2.4.2 Effect of engraved cell parameters

Since the volume of the fluid that forms a square film is largely determined by the areal density of engraved cells, the engraved cell parameters, cell width (CW) and cell spacing (CS), play a major role in forming a complete square shape. As discussed in the previous section, the individual dots must be large enough to be merged together. On the same substrate with the same surface treatment, therefore, large cell spacing results in more incomplete films as shown in **Figure 2.22**. The completeness of the printed films with different cell width and spacing is categorized in **Figure 2.23**. As expected, when the ratio of cell spacing to cell width is smaller, more complete films are formed. The complete film region is widened when the contact angle is lower and thus individual dots are larger. Thus, when the substrate is partially wetting, the cell spacing relative to the cell width needs to be minimized in order to gravure-print complete films.

When the substrate is more wetting, cell spacing must not be too small. The same PVP ink is gravure printed on a PET substrate that has an equilibrium contact angle lower than 10 degrees. Since the contact angle on this substrate is very low, even the printed film with large cell spacing was complete as shown in **Figure 2.24**. However, for smaller cell spacing, the total ink volume is too large so that the contact line around the boundary advances, resulting in a more curved shape, analogous to the previously discussed bulging phenomenon in Chapter 2.3.2.

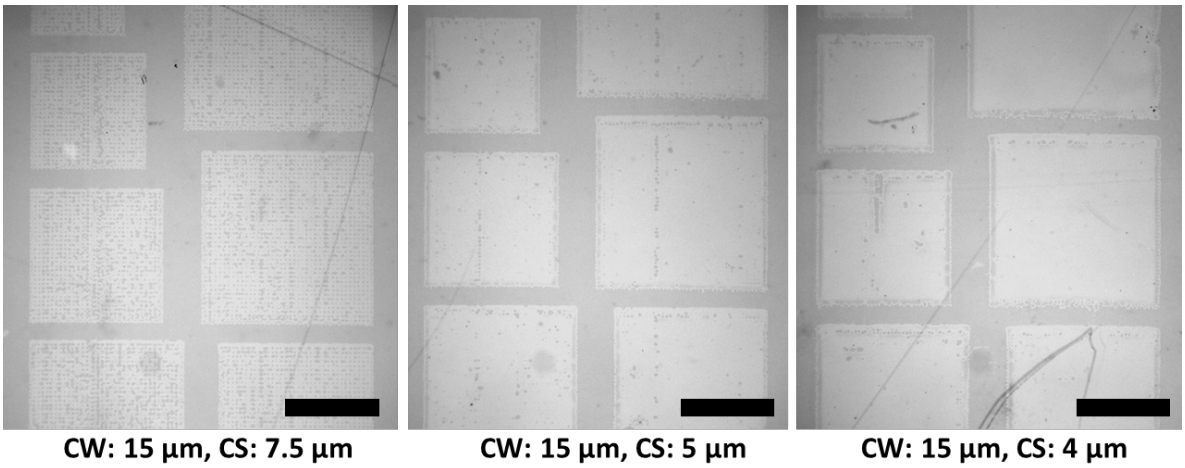


Figure 2.22 Micrographs of gravure printed PVP square films on PEN-B substrate. Cell spacing (CS) is varied. The black scale bar represents 400 µm.

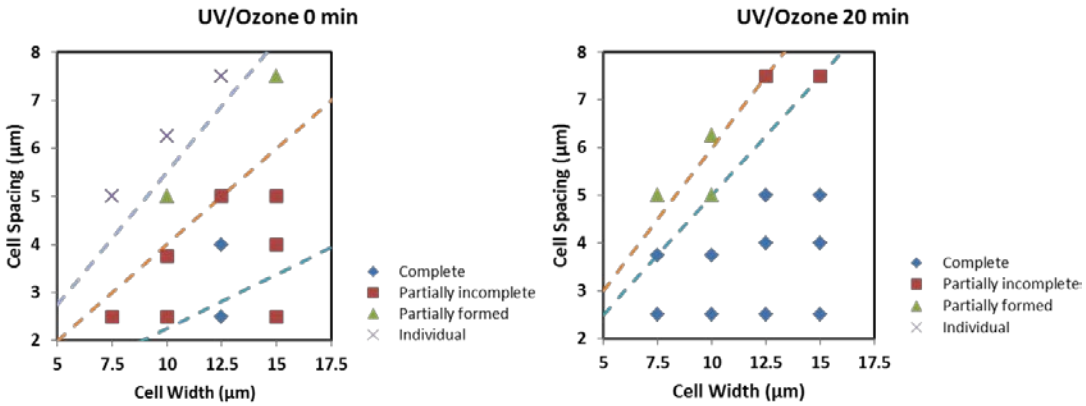


Figure 2.23 Completeness of the gravure-printed square film with different cell width and spacing on two different surface treatments.

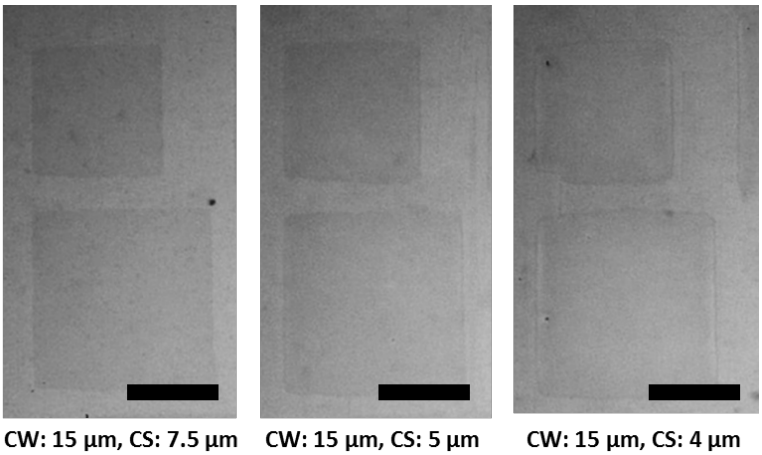


Figure 2.24 Micrographs of gravure printed PVP square films on PET substrate. Cell spacing (CS) is varied. The black scale bar represents 200 µm.

Another important point to note is the way the individual dots are connected. In **Figure 2.25(a)**, two square films are printed with different cell spacing. When the spacing is larger in the upper image, the dots are rarely connected. As the spacing gets smaller as in the bottom image in **Figure 2.25(a)**, dots along the printing direction are first connected and thus lines along that direction are formed. Although the cell spacing is equal in both printing direction and perpendicular direction as shown in **Figure 2.20**, it is interesting to see that the dots tend to be connected more easily along the printing direction than the perpendicular direction. As illustrated in **Figure 2.25(b)**, wiping often leaves excess ink behind the engraved cells from the meniscus formed at the back of the doctor blade. When the ink is transferred, not only the ink confined within the engraved cells, but also the excess ink left behind the doctor blade will be transferred to the substrate. The ink transfer mechanism for the excess ink sitting on the non-engraved area of the roll is different from the ink transfer from the cell to the substrate. It is more similar to the ink transfer in offset printing. As Kang et. al. studied, the contact angle difference between the surface of the substrate and the roll plays an important role in ink transfer during offset printing.[20] When the contact angle of the substrate is lower than that of the master, the ink transfer to the substrate is more favorable. The chrome plated metal cylinder has low contact angle below about 20°. When the substrate has a high contact angle (0 min UVO treatment), the excess ink is not transferred. When the contact angle is lower (20 min UVO treatment), the contact angle is now comparable to the angle on the gravure cylinder, and thus the excess ink is transferred to the substrate, resulting in tails along the printing direction as shown in **Figure 2.25(c)**. Therefore, when the cell spacing is small, the excess ink located between the engraved cells along the printing direction helps connecting the dots particularly when the surface energy of the substrate is comparable to the surface energy of the gravure roll, which is the case in **Figure 2.25(a)**.

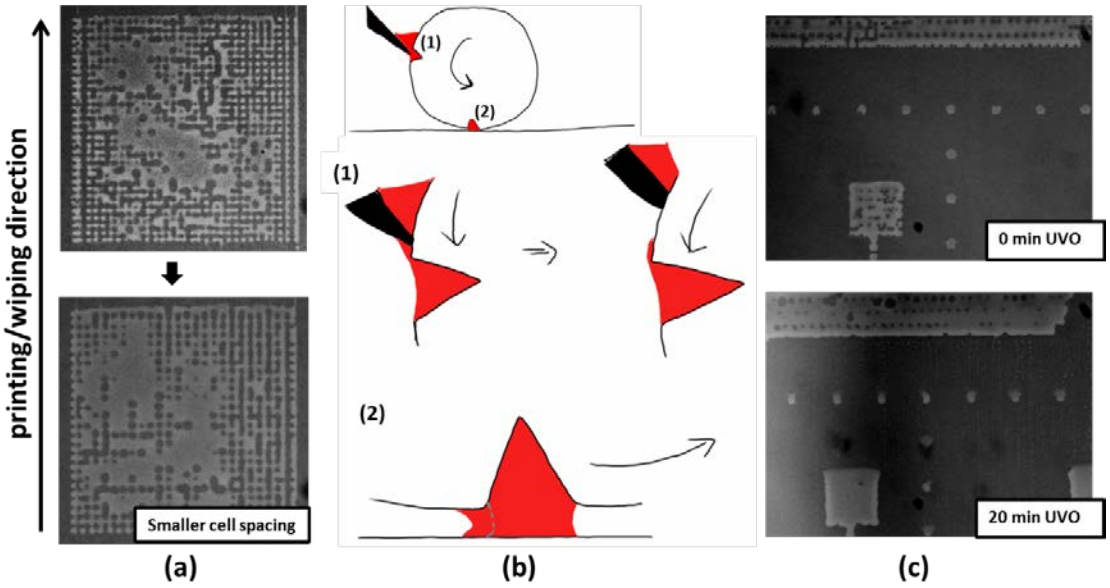


Figure 2.25 (a) Micrographs of gravure-printed partially formed PVP films on PEN-B (b) diagram of the mechanism for the excess ink drag-out by doctor blade and its transfer to the substrate (c) printed individual dots on two different surface conditions.

2.5 Summary

In this chapter, a simple analytic framework for the optimization of printing of two dimensional patterns using droplet-on-demand printing is provided. A simple film thickness model shows a good fit to the printed polymer films. The limitations of the model caused by bulging or unmerged drops are also demonstrated and explained. In order to increase the maximum thickness beyond what can be reached due to bulging, the ink concentration can be increased. This model enabled accurate prediction of the thickness of inkjet-printed films. To develop an understanding of bulging and separation of a film, a one-dimensional hydrostatic model is suggested. A large amount of ink in a given bead, such that its contact angle is higher than the advancing contact angle, causes the bead to advance and wet the substrate. If the amount of ink is not enough to meet the receding contact angle, the film breaks up into smaller films to minimize its surface energy. Therefore, contact angle hysteresis has to be considered carefully for a complete and uniform printed film.

Although the simple 1D hydrostatic model in this chapter helps provide an understanding of the behavior of inkjet-printed films and proves its usefulness, the model is applicable accurately only when the patterns are quasi-1D structures; errors in the 1D approximation manifest themselves as the shape deviates from this regime. When both sides of a pattern become comparable, it is necessary that the entire contact angle around the pattern has to be considered so that the bulging and de-wetting can be anticipated not only at two edges but around the boundary; this is carefully considered and developed further by Soltman et al.[21] What the model in this chapter clearly does establish, however, is the limitations imposed by hydrostatic considerations on films formed using constantly-spaced droplets. Fundamentally, there are finite size regimes for given drop spacing and contact angle conditions over which well-defined patterns without bulging or bead breakup can be achieved. In order to overcome the limitation, varied drop spacing is suggested and demonstrated by Soltman et al in the same work. While the varied drop spacing which decreases the drop spacing as additional lines are printed can be used for drop-on-demand printing system, it is not possible for gravure printing due to the necessity of separation wall between engraved cells.

Gravure printed film formation is found to be fundamentally very similar. The effects of contact angle of the substrate and the engraved cell parameters on the shape of the printed square films are studied. In order to gravure-print good two dimensional patterns, the contact angle and the volume of the printed film must be optimized to ensure merging of the dots while preventing both de-wetting and bulging. With the optimization of those parameters and engraved cell sizes, complete squares of different sizes are gravure printed as shown in **Figure 2.26**. One thing to note here is the sharpness of the corners of the square films and the scalability of the films down to around 60 μm wide squares, which is hard to obtain with conventional inkjet printing.

Electronic devices such as TFTs, OLEDs and solar cells have multilayer structures. Modifying the surface energy of each layer is not always possible because chemical or physical treatments may cause the degradation of the device characteristics such as carrier recombination rate, carrier transport and electric field endurance. Thus, particularly when

the surface energy is inflexible, what has been studied in this chapter can facilitate the printing of good two dimensional films in various printing systems.

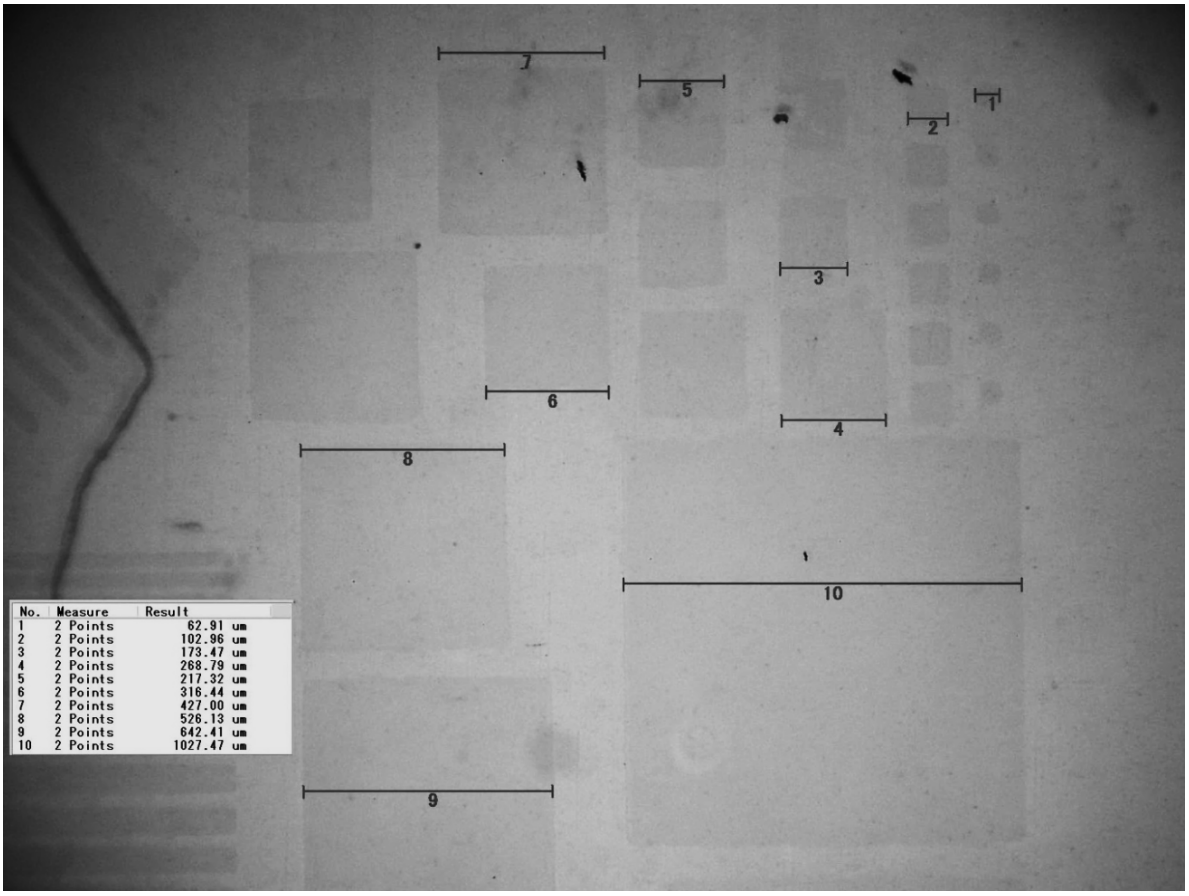


Figure 2.26 Micrograph of gravure printed PVP films on PET substrate. The smallest square film is only about 63 μm wide.

2.6 References

[1] P. C. Duineveld, “The stability of ink-jet printed lines of liquid with zero receding contact angle on a homogeneous substrate,” *Journal of Fluid Mechanics*, vol. 477, pp. 175–200, 2003.

[2] D. Soltman and V. Subramanian, “Inkjet-Printed Line Morphologies and Temperature Control of the Coffee Ring Effect,” *Langmuir*, vol. 24, no. 5, pp. 2224–2231, Mar. 2008.

[3] J. Stringer and B. Derby, “Formation and Stability of Lines Produced by Inkjet Printing,” *Langmuir*, vol. 26, no. 12, pp. 10365–10372, Jun. 2010.

[4] K. Ozawa, E. Nishitani, and M. Doi, “Modeling of the Drying Process of Liquid Droplet to Form Thin Film,” *Japanese Journal of Applied Physics*, vol. 44, no. 6A, pp. 4229–4234, 2005.

[5] Y. Li, C. Fu, and J. Xu, “Topography of Thin Film Formed by Drying Silver Nanoparticle Dispersion Droplets,” *Japanese Journal of Applied Physics*, vol. 46, no. 10A, pp. 6807–6810, 2007.

[6] M. Kaneda, H. Ishizuka, Y. Sakai, J. Fukai, S. Yasutake, and A. Takahara, “Film formation from polymer solution using inkjet printing method,” *AIChE Journal*, vol. 53, no. 5, pp. 1100–1108, 2007.

[7] E. Tekin, B.-J. de Gans, and U. S. Schubert, “Ink-jet printing of polymers – from single dots to thin film libraries,” *J. Mater. Chem.*, vol. 14, no. 17, pp. 2627–2632, Aug. 2004.

[8] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, “High-mobility polymer gate dielectric pentacene thin film transistors,” *Journal of Applied Physics*, vol. 92, no. 9, pp. 5259–5263, Nov. 2002.

[9] M.-H. Yoon, H. Yan, A. Facchetti, and T. J. Marks, “Low-Voltage Organic Field-Effect Transistors and Inverters Enabled by Ultrathin Cross-Linked Polymers as Gate Dielectrics,” *J. Am. Chem. Soc.*, vol. 127, no. 29, pp. 10388–10395, Jul. 2005.

[10] R. D. Deegan, O. Bakajin, T. F. Dupont, G. Huber, S. R. Nagel, and T. A. Witten, “Capillary flow as the cause of ring stains from dried liquid drops,” *Nature*, vol. 389, no. 6653, pp. 827–829, Oct. 1997.

[11] D. Kim, S. Jeong, B. K. Park, and J. Moon, “Direct writing of silver conductive patterns: Improvement of film morphology and conductance by controlling solvent compositions,” *Applied Physics Letters*, vol. 89, no. 26, pp. 264101–264101–3, Dec. 2006.

[12] H.-Y. Tseng and V. Subramanian, “All inkjet-printed, fully self-aligned transistors for low-cost circuit applications,” *Organic Electronics*, vol. 12, no. 2, pp. 249–256, Feb. 2011.

[13] S. Dodds, M. da S. Carvalho, and S. Kumar, “Stretching and slipping of liquid bridges near plates and cavities,” *Physics of Fluids*, vol. 21, no. 9, pp. 092103–092103–15, Sep. 2009.

[14] T.-M. Lee, S.-H. Lee, J.-H. Noh, D.-S. Kim, and S. Chun, “The effect of shear force on ink transfer in gravure offset printing,” *J. Micromech. Microeng.*, vol. 20, no. 12, p. 125026, Dec. 2010.

[15] T.-M. Lee, J.-H. Noh, I. Kim, D.-S. Kim, and S. Chun, “Reliability of gravure offset printing under various printing conditions,” *J. Appl. Phys.*, vol. 108, no. 10, p. 102802, 2010.

[16] X. Yin and S. Kumar, “Flow visualization of the liquid emptying process in scaled-up gravure grooves and cells,” *Chemical Engineering Science*, vol. 61, no. 4, pp. 1146–1156, Feb. 2006.

[17] U. Ceyhan, R. Kitsomboonloha, S. J. S. Morris, and V. Subramanian, “Lubrication analysis of the nanometric coating film deposited during gravure printing,” in *Bulletin of the American Physical Society*, 2012, vol. Volume 57, Number 17.

[18] R. Kitsomboonloha, U. Ceyhan, S. J. S. Morris, and V. Subramanian, “Experimental study of the residue film in direct gravure printing of electronics,” in *Bulletin of the American Physical Society*, 2012, vol. Volume 57, Number 17.

[19] R. Kitsomboonloha, S. J. S. Morris, X. Rong, and V. Subramanian, “Femtoliter-Scale Patterning by High-Speed, Highly Scaled Inverse Gravure Printing,” *Langmuir*, vol. 28, no. 48, pp. 16711–16723, Dec. 2012.

[20] H. W. Kang, H. J. Sung, T.-M. Lee, D.-S. Kim, and C.-J. Kim, “Liquid transfer between two separating plates for micro-gravure-offset printing,” *J. Micromech. Microeng.*, vol. 19, no. 1, p. 015025, Jan. 2009.

[21] D. Soltman, B. Smith, H. Kang, S. J. S. Morris, and V. Subramanian, “Methodology for Inkjet Printing of Partially Wetting Films,” *Langmuir*, vol. 26, no. 19, pp. 15686–15693, Oct. 2010.

2.7 Appendix

2.7.1 Contact Angle Hysteresis and Its Measurement

As well known, a sessile drop on a substrate has a contact angle defined by the Law of Young-Dupré. The surface tensions between gas/liquid, liquid/solid and solid/gas are equilibrated by forming the equilibrium contact angle. When the substrate gets dirty either chemically (defects) or physically (roughened), the contact angle does not only have one value. If there are defects which attract the liquid, more energy is needed to break up the interaction between the defects and the drop. Also, when the surface is rough, the macroscopic contact angle can have a range of values because the rough surface has non-zero angle slope, which changes the macroscopic angle. When the volume of a liquid drop is increased, the angle beyond which the drop starts expanding is defined as 'advancing contact angle'. Also, while the volume of a liquid drop is decreased, the angle below which the drop retreats is 'receding contact angle'. In the case of a dirty or rough surface, the advancing contact angle and receding contact angle are not identical, resulting in nonzero contact angle hysteresis.

Contact angle hysteresis can be measured based on the definitions of the various contact angles. With a supply of ink into a drop to wet the substrate, measured contact angle when the drop just starts advancing can be determined as the advancing contact angle. Similarly, by sucking the ink through a needle to recede the drop, we can measure the retreating contact angle as shown in **Figure 2.A1(a)**. In order to minimize the effect of surface tension between the needle and the liquid, it is desirable to use a needle with low surface energy. Instead of controlling the volume of a drop, a tilted substrate which makes a droplet advance and recede by gravity can be used to measure the hysteresis as shown in **Figure 2.A1(b)**. More methods can be found in other works.[A1-A4]

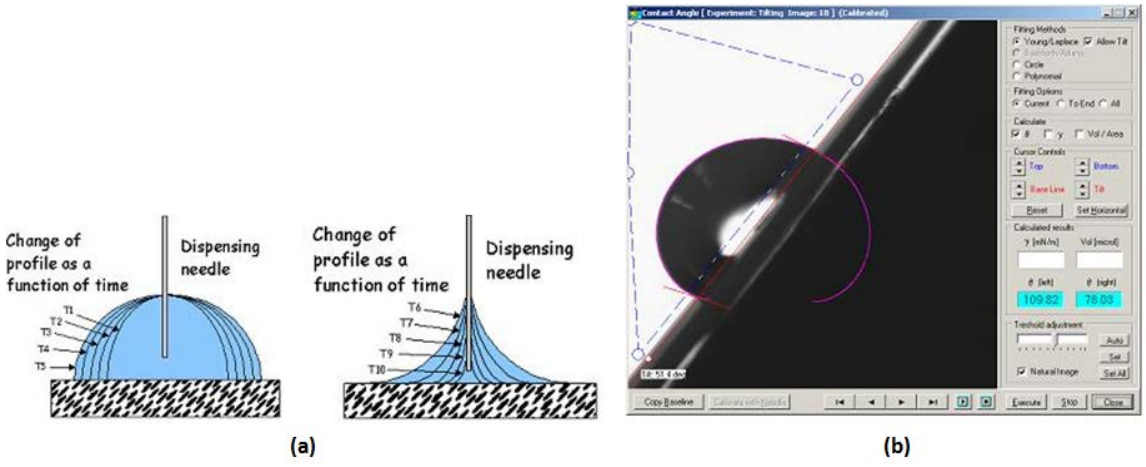


Figure 2.A1 Methodologies to measure dynamic contact angles (source: KSV Instruments Ltd., http://www.ksvltd.com/content/index/keydca) (a) using needle to advance/recede the drop on a flat substrate. (b) Tilting the substrate to advance/recede the drop.

In the hydrostatic models presented in this chapter, the contact angle hysteresis plays the most important role in explaining what we observe and anticipating the pattern shapes. For all the experiments conducted, the former measurement method of using a needle is used to measure the contact angles in the experiments.

2.7.2 Puddle Thickness Limited by Gravity

Gravity flattens partially wetting films to height given below. [A5]

$$e = 2\sqrt{\frac{\gamma}{\rho g}}\sin\left(\frac{\theta_E}{2}\right) \tag{S1}$$

where e is the puddle thickness, γ is the surface tension, ρ is the density of liquid and θE is the equilibrium contact angle. With the parameters of 1-hexanol,[A6] the thickness in (S1) can be calculated to be about 800 μm. The height of printed PVP films before evaporation is from 10 μm to 150 μm, and much smaller than the thickness calculated from (S1). Therefore, we can ignore gravitational effects when calculating shapes of printed films in this work.

2.7.3 References for Appendix

[A1] RULON E. JOHNSON, Jr., and, ROBERT H. DETTRE, “Contact Angle Hysteresis - I. Study of an Idealized Rough Surface.” [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/ba-1964-0043.ch007. [Accessed: 27-Sep-2011].
[A2] ROBERT H. DETTRE and, RULON E. JOHNSON, JR., “Contact Angle Hysteresis - II. Contact Angle Measurements on Rough Surfaces.” [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/ba-1964-0043.ch008. [Accessed: 27-Sep-2011].
[A3] R. E. Johnson and R. H. Dettre, “Contact Angle Hysteresis. III. Study of an Idealized Heterogeneous Surface,” J Phys Chem, vol. 68, no. 7, pp. 1744–1750, Sep. 2011.
[A4] R. H. Dettre and R. E. Johnson, “Contact Angle Hysteresis. IV. Contact Angle Measurements on Heterogeneous Surfaces1,” J Phys Chem, vol. 69, no. 5, pp. 1507–1515, Sep. 2011.
[A5] de Gennes, P.; Brochard-Wyart, F.; Quéré, D., Capillarity and Wetting Phenomena, Drops, Bubbles, Pearls, Waves; Springer, 2004; Chapter 2.
[A6] Piñeiro, M.; García, J.; de Cominges, B.; Vijande, J.; Valencia, J.; Legido, J., Fluid Phase Equilibria, 2006, 245, 32-36.

Chapter 3

Scaling of Gravure-Printed Conductive Lines

3.1 Introduction

As mentioned in Chapter 1, the scaling of printed lines can significantly improve the performance of printed transistors. In particular, using gravure printing for that purpose is ideal due to its high resolution printing capability and high printing-throughput. High pattern fidelity of gravure printing is achieved by using precisely defined well shapes on the roll-based master along with appropriately formulated inks and printing conditions. Therefore, precisely engraved patterns on the master are the most important factor that determines the quality of the gravure printing and further the scalability of the gravure-printed features. In this chapter, the scaling of gravure-printed conductive lines below 5 μm was pursued. Starting with the proper selection of engraving methods for the highly scaled features, the understanding of governing fluid mechanics and the optimization of conductive inks led to successful demonstration of gravure-printed sub-5μm conductive metal lines on plastic substrates.

3.2 Electromechanical engraving

There exist various engraving techniques such as chemical etching, laser engraving, and electromechanical engraving. In order to realize sub-5μm patterns on the master with low variation and excellent fidelity, a novel electromechanical engraving process is chosen over other techniques such as chemical etching engraving shown in **Figure 3.1**. In the electromechanical engraving process, a pyramidal diamond stylus tip moves in and out of a copper gravure roll that rotates to create a digitally-defined pattern. With the precise mechanical control of the diamond stylus and the copper roll, minimized cell-to-cell variation is obtained with the electromechanical engraving compared to chemical etching technique in which inconsistent etch rate and directionality leads to non-uniformity. By the reduction of the engraving depth, scaling down of the patterns is pursued. The electromechanical engraving is processed by Ohio Gravure Technologies (http://www.ohiogt.com). After the engraving, the roll is electroplated with chrome to ensure good resistance to physical damage.

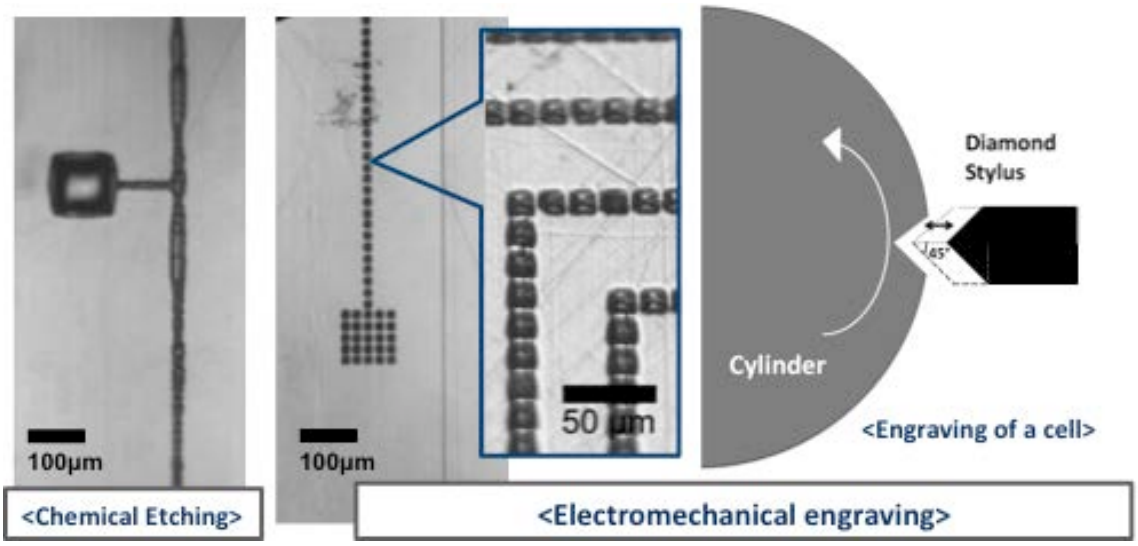
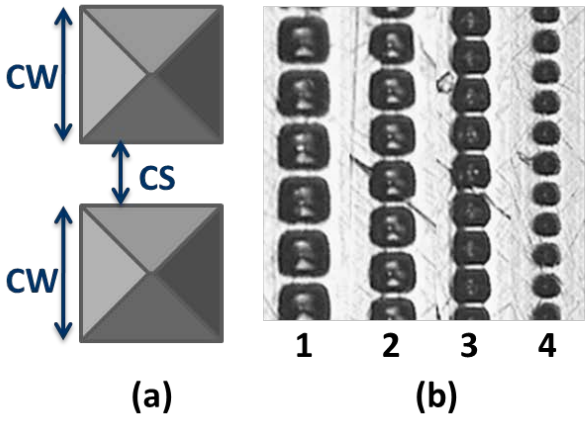


Figure 3.1 Pattern engraving in gravure printing. Optical micrographs of chemically etched and electromechanically engraved patterns are provided and compared. The process of the electromechanical engraving is illustrated on the right.



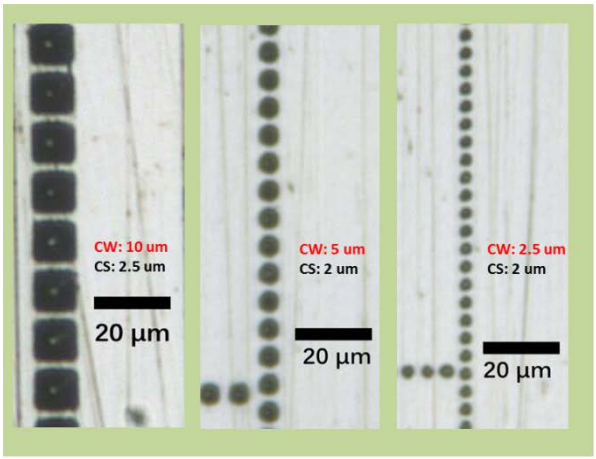
Line #	1	2	3	4
Nominal Cell Width (μm)	15	12.5	10	7.5
Measured Cell Width (μm)	17	15	11.75	9.25

(c)

Figure 3.2 (a) Definition of gravure cell parameters in this work: cell width (CW) and side-to-side cell spacing (CS). (b) Optical micrograph of the engraved cells on our gravure roll with cells as small as 7.5 μm. (c) Nominal and measured cell width of the patterns in (b). Note that CW is controlled by depth of stylus into the Cu roll.

The engraved cells are defined with two parameters: cell width (CW) and side-to-side cell spacing (CS). Engraved cells of which the cell width is ranged from 7.5 μm to 15 μm are shown in **Figure 3.2**. The nominal cell width and the measurement cell width are quite similar. Even smaller cells below 5 μm are shown in **Figure 3.3** along with the associated properties of engraved pyramidal cells. The smallest achieved pattern is a pyramid with a 2.5 μm wide square base and 1.25 μm depth; this feature has a volume of only 2 femtoliters. Since not all the ink filled in the cell is transferred to the substrate during printing, actual ink volume from the 2.5μm cell is even smaller, thus allowing for very aggressive dimensional scaling of printed features. More detail about the ink transfer will be discussed in the next section, but about half of the cell volume is found to be the volume of the transferred ink. For the smallest cell, therefore, the printed ink volume is even sub-femtoliter. The ink transferred from a single cell, analogous to an inkjet-printed droplet, has

thus much smaller volume than the typical volume of a single inkjet-printed droplet, 1-10 picoliters (e.g. Dimatix inkjet printer designed for printed electronics by FUJIFILM). The volume level is even comparable to the most aggressively scaled subfemtoliter inkjet printer.[1] Advantageously, gravure printing proceeds at very high-speeds, independent of feature scaling, unlike inkjet printing. Since scaling down of printed patterns benefits from the reduced ink volume, gravure printing is a promising technology for scaling of features.



(a)

Cell Width [µm]	Cell Volume [fL]	Transferred Ink Volume* [fL]	Ink Volume per Unit Length** [fL/µm]
15	562.5	253.1	14.5
12.5	325.5	146.5	9.8
10	166.7	75.0	6.0
7.5	70.3	31.6	3.2
5.0	16.4	7.4	1.05
2.5	2.0	0.92	0.23

(b)

Figure 3.3 (a) Micrograph of the engraved cells on our gravure roll with cells as small as 2.5 µm. (b) Properties of engraved pyramidal cells on the gravure roll. The cell width is the side length of a square base of the pyramid. The ratio of cell width to depth is determined to be 2 by the shape of the diamond stylus used for engraving.
*The volume of transferred ink onto the substrate is about 45 % of the volume of the engraved cells. (see supporting information)
**Values are calculated assuming the spacing between cells is 2.5 µm.

3.3 Scaling of gravure-printed lines

To realize properly scaled devices, it is necessary to gravure print both scaled metallic electrodes and polymer materials (e.g. for gate dielectrics). Therefore, we begin by examining both of these from here. Using the gravure-printing master, lines are gravure-printed on the planarized PEN substrate introduced in Chapter 2. This substrate was selected due to its good thermal stability and wide contact angle hysteresis due to near zero receding contact angle. As studied in the previous chapter, low receding contact angle minimizes de-wetting of printed 1D and 2D features, resulting in more complete features. Thus, the small receding contact angle of the planarized PEN substrate used in this work helps ensure completeness of gravure-printed patterns.

3.3.1 Line width

We firstly studied the behavior of gravure-printed patterns by printing 20wt% poly-4-vinylphenol (PVP) (Mw ≈ 11,000 from Sigma Aldrich) dissolved in 1-hexanol (99.0%, from Sigma Aldrich) which has been successfully used to understand the fundamentals of printed features in Chapter 2 and [2]. As shown in **Figure 3.4**, changing the size (CW) and spacing (CS) of gravure cells enables reduction of the width of gravure-printed lines down to 6.3 µm. Measured width of the gravure-printed lines is in good agreement with the

hydrostatically determined theoretical relationship (modified from equation (7) in Chapter 2),

$$W_{single} = \sqrt{\frac{8\sin^2\theta}{2\theta - \sin 2\theta}\beta V_{perlength}} = K(\theta)\sqrt{\beta V_{perlength}} \quad (1)$$

where θ is the equilibrium contact angle of the ink on substrate; $K(\theta)$ is thus a function of contact angle; β is ink print ratio from the master to the substrate; and $V_{perlength}$ is the volume of the cells per unit length. Good accordance with the equation proves good controllability of the printing process.

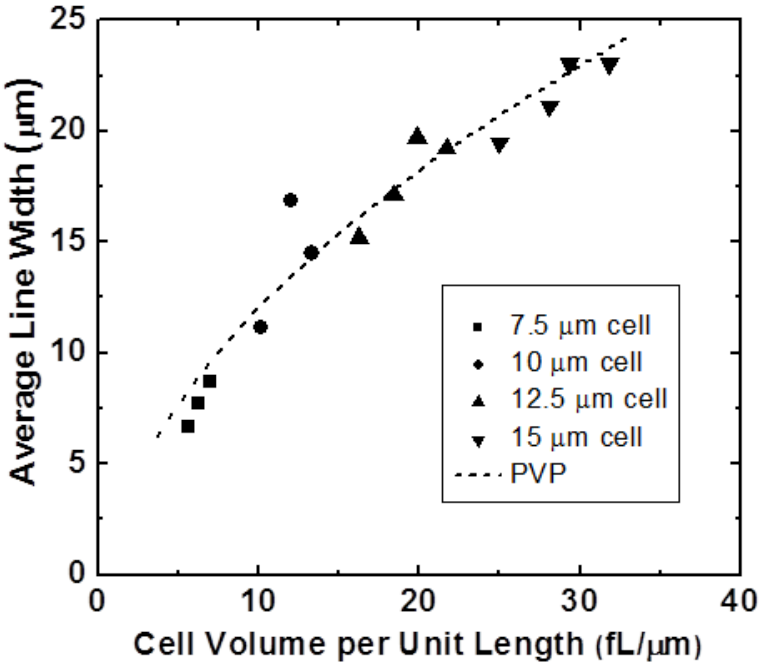


Figure 3.4 Scaling of gravure-printed PVP lines on 20 min UVO treated PEN (contact angle 30°). Gravure cell sizes ranged from 7.5 μm to 15 μm with four different spacing from 2.5 μm to 7.5 μm. ($W_{single,\ 20min\ UVO}$ = 2.87*(volume)$^{0.5}$-2.89)

3.3.2 Ink transfer

Since it is important to know how much volume of the ink is printed compared to the volume of the engraved cell when estimating the line width, experiments are designed to obtain the print ratio, β in equation (1). The experiment is designed in the following way. The same ink is gravure-printed with the same roll on the PEN substrates with different surface treatment (UV/Ozone treatment time). Other printing parameters such as printing speed, roll to substrate pressure, and doctor blade pressure are kept the same as well. Since the PEN substrate surface energy does not affect the ink filling and the ink drag-out by doctor blading, it is assumed that the only parameter that could be affected by the different surface energy of the PEN substrate is the ink transfer. For the calculation of the transferred ink volume, firstly the volume of the dried printed feature is measured from the 3D surface profile obtained by white-light-interferometry, and the volume before drying is calculated based on the mass loading of the ink. For the verification of the dried feature volume

calculation, polymer ink droplets are inkjet printed on the PEN substrate, and the volume of the droplets is analyzed. As shown in **Figure 3.5**, even with significant coffee ring edges, this method is able to measure the volume of the droplets quite well based on the fact that the volume of the droplets is linearly proportional to the number of droplets, and the volume of a single droplet is about 5.6 pL which is reasonable given the fact that 10pL inkjet cartridge is used for this experiment.

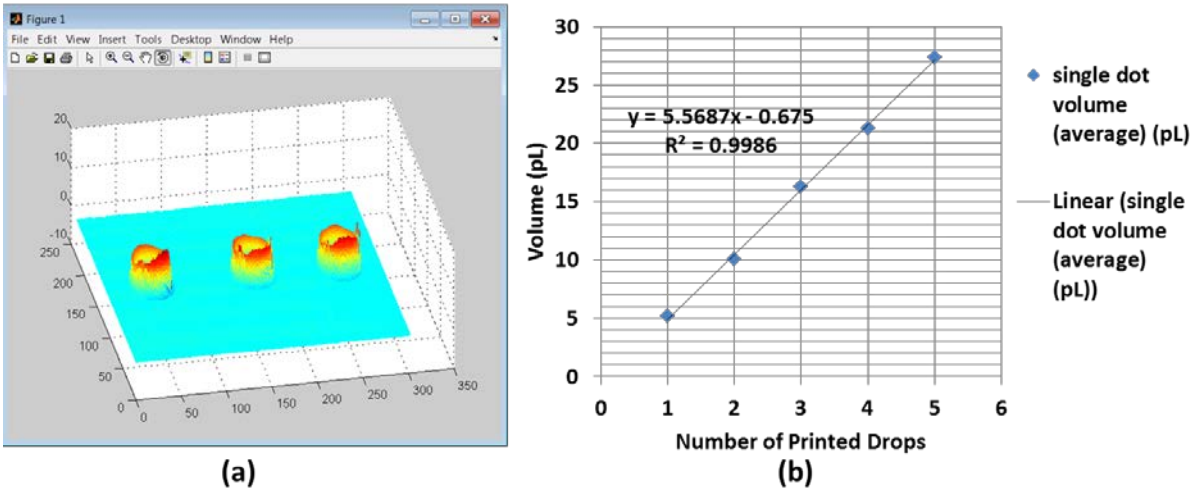


Figure 3.5 (a) Surface profile of inkjet printed PVP dots on PEN substrate. (b) The measured volume of the printed dots before drying.

With the same method, the print ratio (β) of the gravure-printed individual dots with different UV/Ozone time on PEN substrate is measured and calculated as shown in **Figure 3.6**. β was calculated to be around 45 %. The print ratio is however slightly increased as more UV/Ozone treatment is applied (lower contact angle).

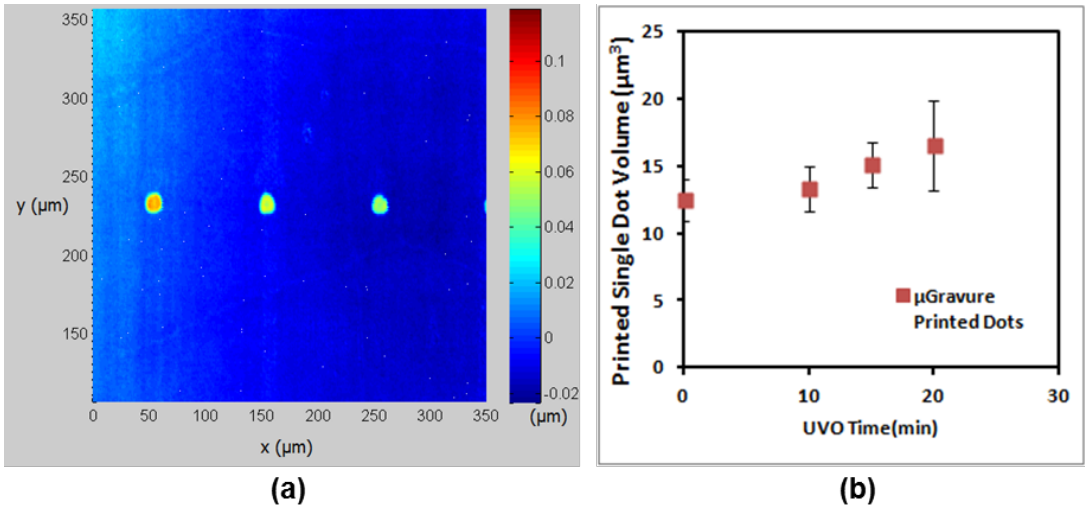


Figure 3.6 (a) Surface profile of gravure-printed dots on plastic substrate obtained by white-light-interferometer. (b) Measured volume of the gravure-printed dots from the surface profile in (a) with respect to different surface treatment on PEN substrate.

As discussed in the previous chapter, the consequences of the doctor blade wiping are different for a single cell and for multiple dots that form a line. Thus, as a next step, the ink print ratio (β) for lines is measured in the same way. As shown in **Figure 3.7**, the cross-sectional area of the line is calculated from the profile, and the area is integrated along the direction of the line to obtain the volume of printed lines.

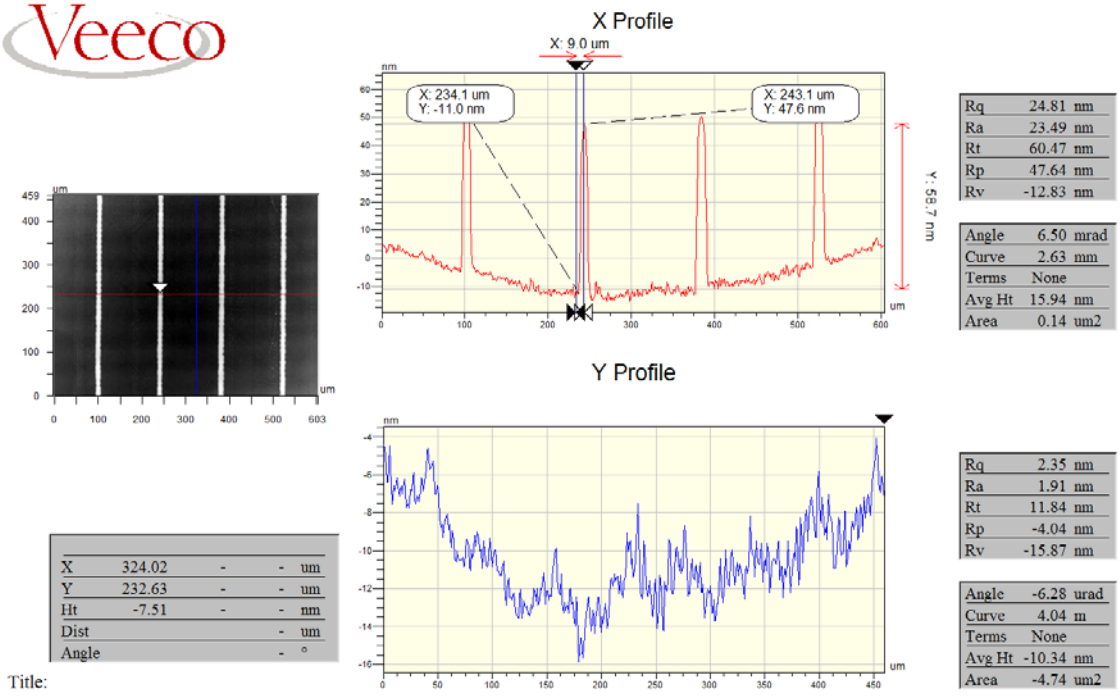


Figure 3.7 Cross-sectional view of printed lines after drying. The cross-sectional area obtained in this graph is integrated to obtain the volume of printed lines.

Gravure printed lines on PEN substrates with different UV/Ozone time are analyzed in **Figure 3.8**. Cell width and cell spacing are varied to cover a wide range of the total cell volumes. The printed line volume after drying is linearly proportional to the volume of the total cells, meaning almost identical print ratio regardless of the CW and CS. The print ratio is not significantly affected by size of the cell and the surface treatment. β is still near 50% for the range of the cell widths used in the experiment. While the print ratio of lines is similar to that of a single dot, the effect of the surface energy of substrates is different. It may be because of the different effect of the drag-out volume by doctor blading (Chapter 2). Since the ink dragged out can be more easily transferred when the contact angle on the substrate is lower, the print ratio increases as the UV/Ozone time increases in the case of a single dot. When the cells are spaced closely, the ink dragged out is moved to the next cell, and thus there is not much tail left behind the cell, which can be transferred to the PEN substrate. Thus, for printed lines, there is no significant effect of the surface energy of PEN on the print ratio.

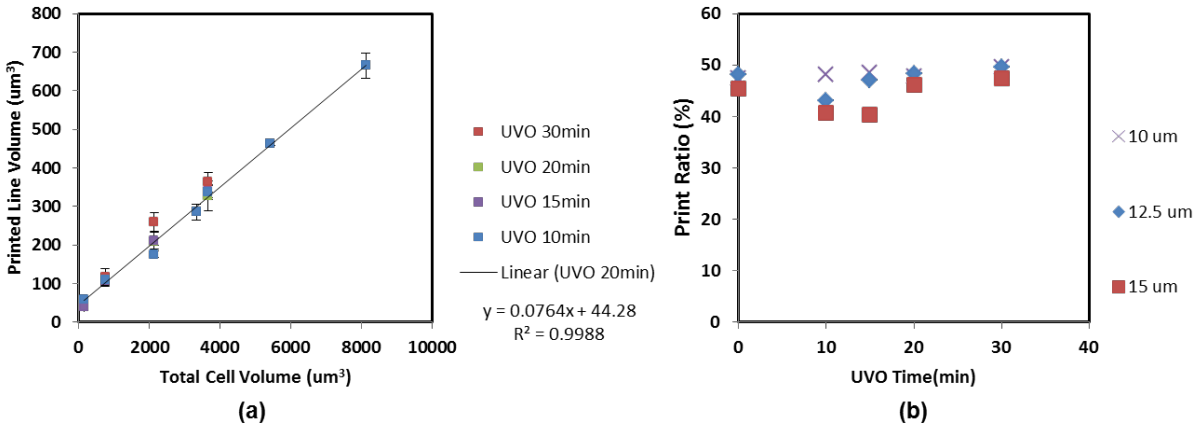


Figure 3.8 (a) Relationship between the volume of the printed lines after drying and the total volume of the cells used for printing the lines of the same length (b) The effect of different surface treatment on the print ratio (β) of the gravure roll. Three different CW groups are used.

The result of print ratio experiment leads to more accurate estimates of printed line width. According to the equation (1), since the print ratio, β, is independent of the contact angle, θ, within the range of our experiments, the width of the printed lines will be determined by the cell volume per length and $K(\theta)$ which is easily calculated. Micrographs of gravure-printed lines on the substrate with different surface treatments are given in **Figure 3.9**. The average width of the lines in **Figure 3.9** is compared with the calculated line width based on the equation (1) with all the needed parameters (see **Figure 3.10**). Except the case of no UV/Ozone treatment, the actual line width matches quite well with the theoretically calculated line width. Again, it proves a good controllability of our gravure printing thanks to excellent quality of engraved cells. The possible reason for the deviation of 'non-UVO treated condition' is because of the cleaning of the surface by UV/Ozone treatment that alters the receding contact angle on the substrate. Since the UV/Ozone treatment is a surface cleaning process, it not only increases the surface energy of the substrate, but also cleans the surface so that the cleaned surface has smaller contact angle hysteresis. Thus, the lines on 10 minute UV/Ozone treated PEN tend to de-wet due to the incapability of maintaining cylindrical cap geometry.

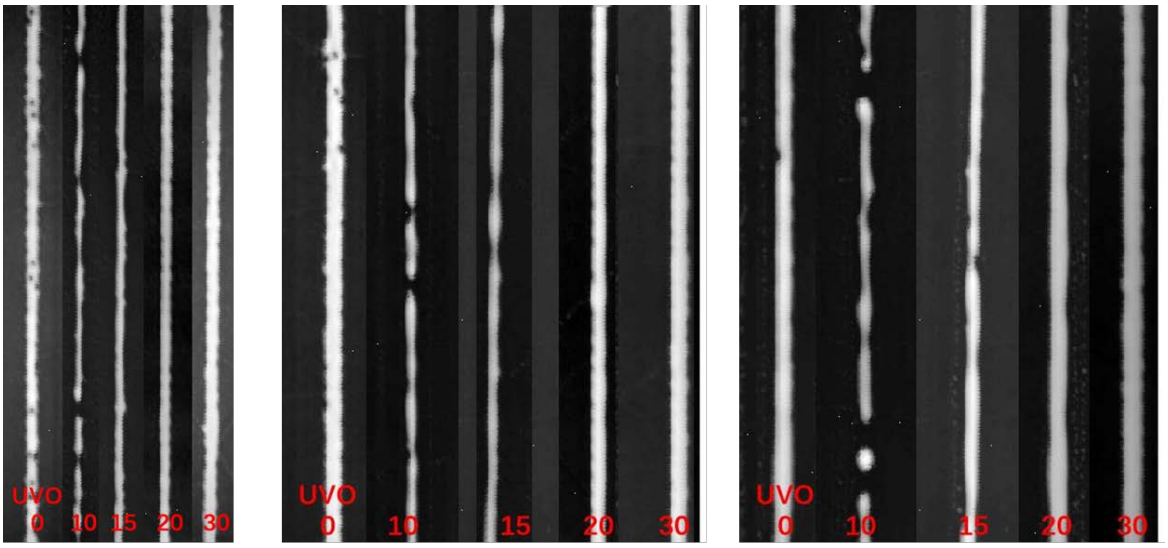


Figure 3.9 Gravure-printed PVP lines on PEN substrate with different UV/Ozone time; (a) CW: 10 μm, (b) CW: 12.5 μm, and (c) CW: 15 μm.

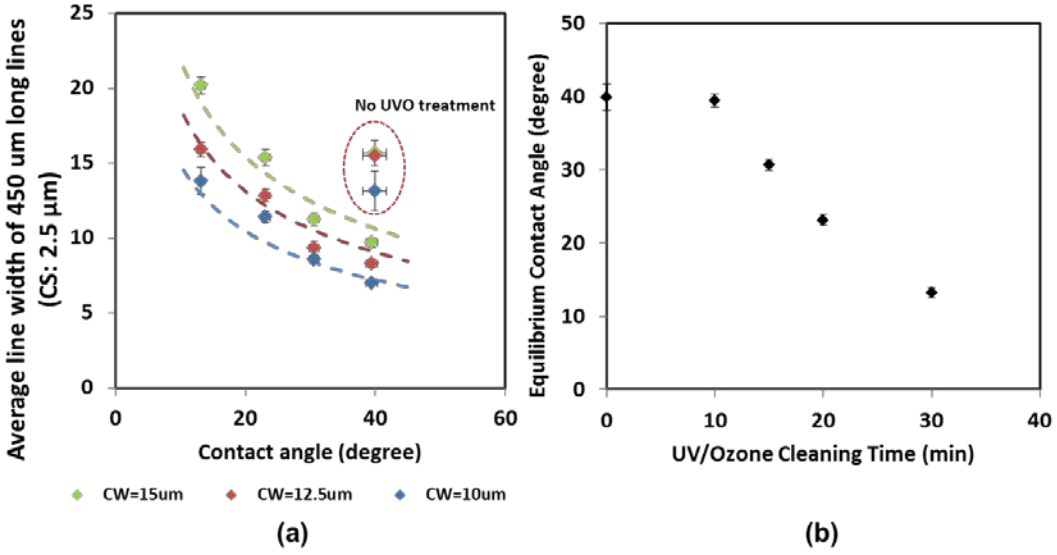


Figure 3.10 (a) Average width of the lines in Figure 3.9. The dotted lines are the estimated line width calculated based on the equation (1) with cell parameters and measured print ratio (b) The equilibrium contact angle of PVP inks on the PEN substrate.

Printed lines with the sub-5μm engraved cells shown in **Figure 3.3** were even further scaled down to around 4 μm as shown in the following **Figure 3.11** while keeping the line edge roughness (LER) below 2 μm. While these LER values are rather large, the achieved resolution attests to the possibility of significant scaling of gravure printing through appropriate optimization.

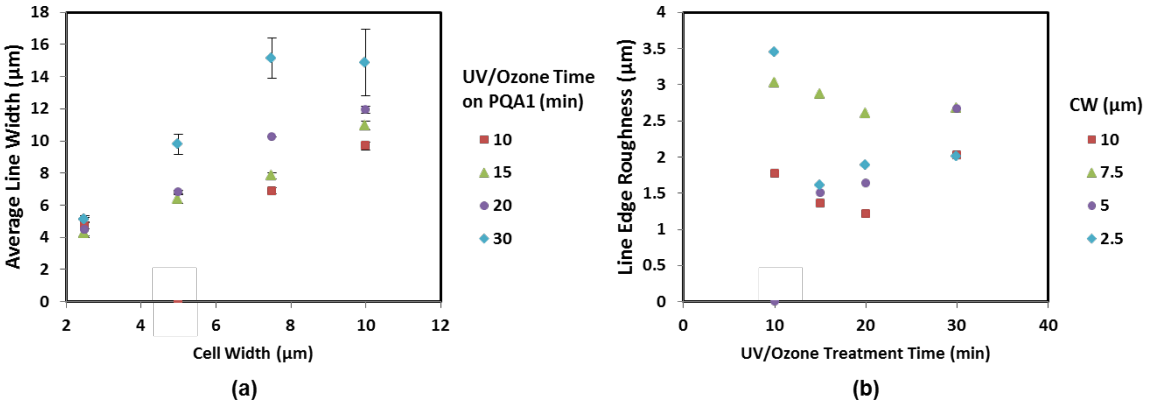


Figure 3.11 (a) Scaling of the PVP line width by the change of cell width and surface treatment condition. (b) Line edge roughness of the lines in (a).

3.4 Optimization of conductive inks for highly scaled gravure printing

Printed transistors are multilayer devices. Thus, the three-dimensional morphology of printed lines is of critical importance in device formation. For example, the thickness of conductive lines determines the resistance of the same, which can limit operating speed of circuits. Additionally, the smoothness of printed conductive lines is critical for their use as gate electrodes in bottom gate TFTs since rough underlying gates will tend to cause defects such as pinholes, etc., in overlying gate dielectric layers. The surface roughness of the gate line affects not only the leakage current and breakdown characteristics of the dielectric layer, but also the mobility of the semiconductor.[3] Therefore, in addition to the printed line width studied in the previous section, we studied the materials-process-structural relationships of printed conductive lines in order to allow for proper materials and process optimization. Firstly, the optimization of conductive inks for the highly scaled gravure printing will be presented herein.

3.4.1 Organometallic ink

Conducting polymers such as poly(3,4-ethylene dioxythiophene) doped with poly(styrene sulfonate) (PEDOT:PSS) have been previously printed with roll-to-roll printers.[4]–[7] However, the resistance of this conducting polymer is unacceptably high for use in high-speed circuits. To overcome this, we have previously studied the use of an organometallic silver precursor ink, Inktec PR-010.[8] One advantage of the organometallic silver ink was that there was no coffee-ring in the printed features. However, the low metal content (~ 10 wt%) of this system limits scalability due to the absence of conductive paths for thin films; thus the gravure-printed silver lines in **Figure 3.12** are not only resistive, but also are semi-transparent which is an indication of its thinness. To overcome the problem of low conductivity, metal inks with much higher metal content such as metallic nanoparticle based inks are tried in the following section.

Figure 3.12 Micrograph of the gravure printed organometallic silver ink.

3.4.2 Nanoparticle inks

3.4.2.1 Effect of nanoparticle size

Firstly, we studied the printing of two high metal content nanoparticle-based metal inks with different particle sizes. One is DGP silver nanoparticle ink with 50 nm nanoparticle size, purchased from Advanced Nano Products (ANP). As-received metal content of the ink is 75 wt% with viscosity of 100 P; this is diluted to tune the viscosity of the ink by addition of isopropyl alcohol while maintaining the metal content above 50 wt%. The other ink is NPG-J gold nanoparticle ink purchased from Harima Chemicals. This ink has an average particle size of 5 nm. In spite of its low viscosity (~10 cP), it has a high metal content of ~50 wt%, and shows good printability in our gravure system, by increasing printing speed and thus keeping capillary number still high.

Both of the inks are able to produce sub-10μm wide lines with reasonable thickness (35-60 nm) as shown in **Figure 3.13**. However, the characteristics of the lines are quite different depending on the size of the nanoparticles. Although the ink containing 50 nm Ag nanoparticles prints thicker lines, the lines become very resistive as feature sizes are scaled below 10 μm due to the loss of continuous conduction paths. As the thickness of the lines approaches the nanoparticle diameter (~50 nm), a near-monolayer printed structure is formed, preventing the formation of good conductive percolative networks. Also, the surface roughness of 50 nm nanoparticle lines is significantly higher due to the large size of the particles as shown in **Figure 3.13**. On the other hand, 5 nm gold nanoparticle based ink leads to much better conductivity in spite of reduced film thickness, and much improved surface roughness (RMS 2.31 nm). The improvement in conductivity can be attributed to the densely packed structure, offering well-connected paths for percolation-based conduction. The low surface roughness improves the endurance of dielectric layer built upon the metal lines. PVP capacitors printed on the metal lines show very low leakage current density, 1 A/cm^2 at 2 MV/cm even when PVP layer thickness is also significantly scaled, which will be discussed in detail in Chapter 4.

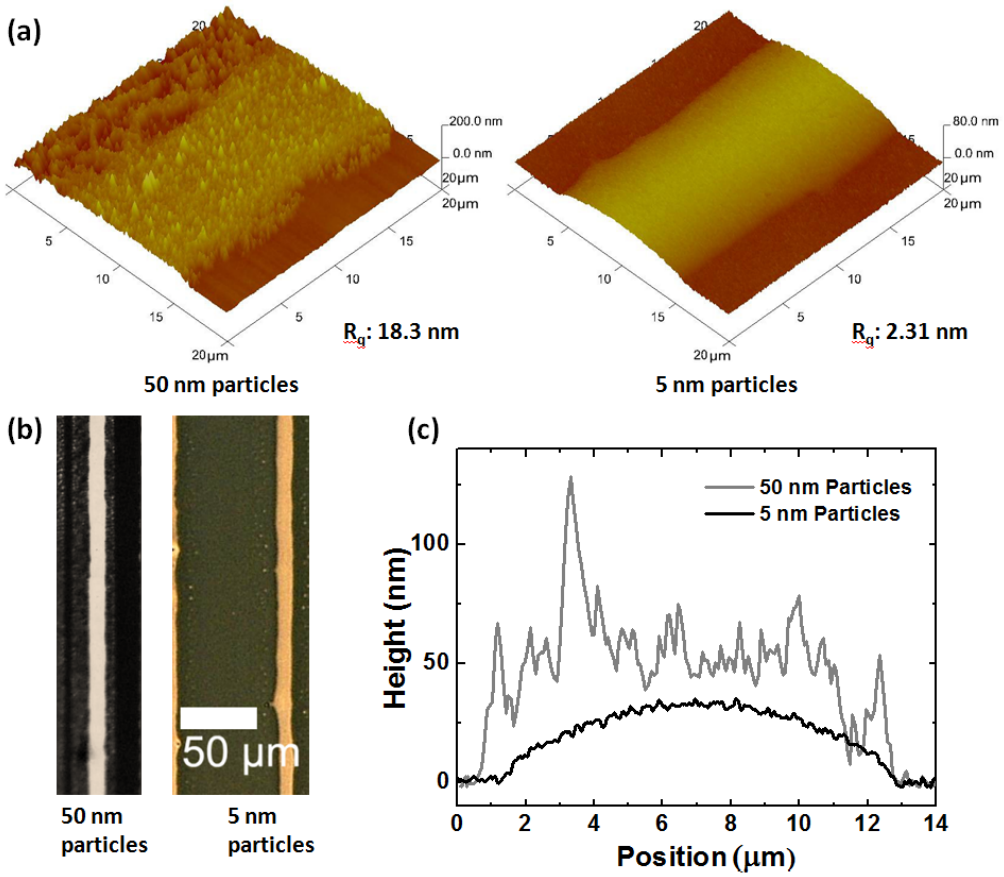


Figure 3.13 (a) AFM images of gravure printed metal lines with different nanoparticle sizes. The scan area is 20 µm x 20 µm. RMS roughness of the lines (R_q) is provided. (b) Optical images of the gravure printed metal lines (from 10 µm square cells with 3.75 µm cell spacing), showing excellent pattern fidelity. (c) Surface profile of the printed metal lines.

3.4.2.2 Effect of mass loading and viscosity

With the optimization of the size of nanoparticles, highly scaled gold lines are demonstrated. However, further scaling below 5 µm does not seem promising with this NPG-J gold ink because the thickness of the lines drops below 15 nm which makes the lines hard to be conductive. Therefore, increase of the thickness is pursued by further increase of the metal content while keeping the size of particles small. The ink selected is a silver nanoparticle ink, NPS, purchased from Harima Chemicals. This ink also has an average particle size of 5 nm, and has high metal content, 75~80 wt%. NPS ink is particularly designed for screen printing, and thus it has high viscosity of around 1,500 P. The ink is diluted by its non-aromatic matching solvent, AF5, to reduce the viscosity for being compatible with the gravure printing. 7.6 wt% of AF5 is added to the as-received ink, and thus the viscosity is decreased to 100 cP while keeping the metal content as high as 74 wt%. As a result of the higher mass loading and viscosity of the diluted NPS ink than the previous NPG-J gold ink, the gravure-printed lines get thicker even when the line width is decreased to about 4 µm as shown in **Figure 3.14**. Thanks to the small nanoparticle size, the coffee-ring-less printed lines are still fairly smooth. The material switch from gold to

silver might give negative results for some applications due to the change of workfunction and the difference of intrinsic material characteristics (e.g. bio compatibility). However, in terms of the fabrication cost, silver is preferred over gold. For the purpose of using these highly scaled lines as electrodes in low-cost electronics applications, usage of silver is more appropriate.

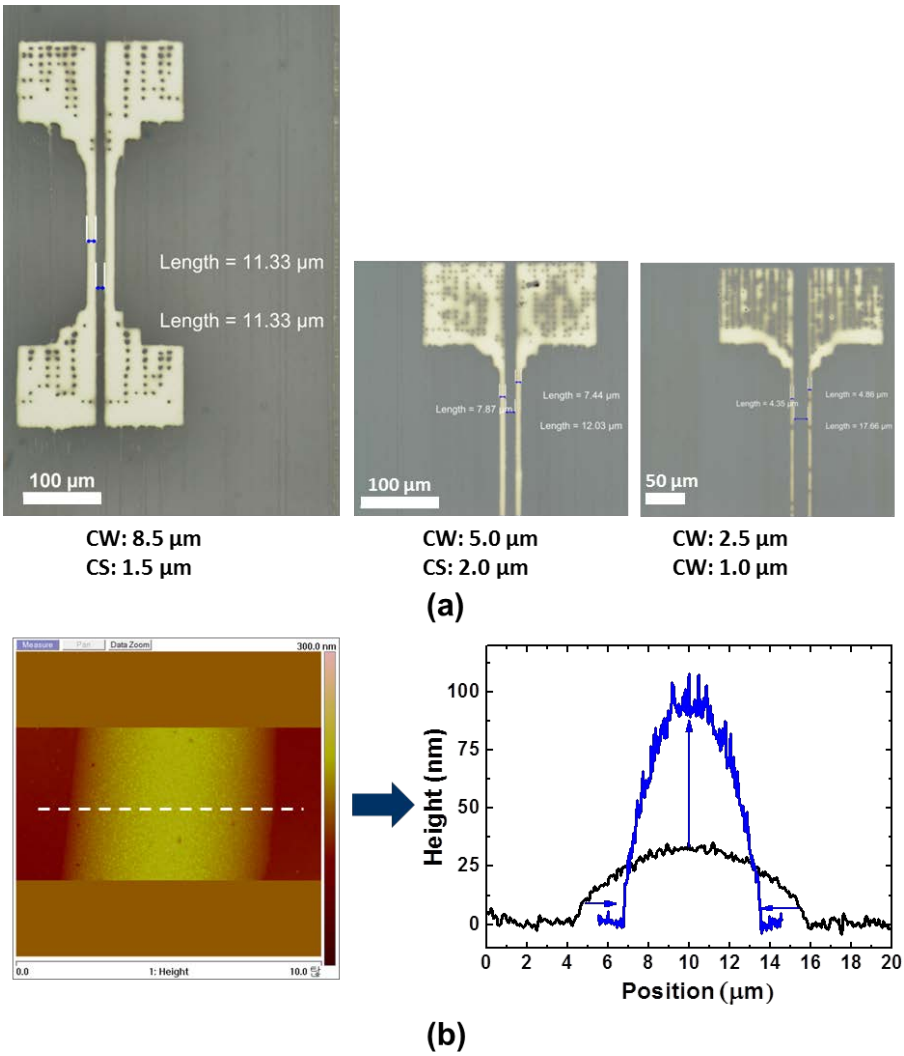


Figure 3.14 (a) Gravure-printed silver lines with NPS ink from different cell widths. (b) Surface profile of the gravure printed lines (blue: NPS silver line, black: NPG-J gold line shown in the previous section).

In addition to the benefit of scalability of the lines by the optimization of the mass loading of the ink, higher viscosity leads to more uniform width of the lines as shown in **Figure 3.15**. As commonly observed in the inkjet printing of low viscosity inks, printed lines typically have larger circular bulges at the starting point of the printing. This is because of the hydrostatic pressure difference during the transition of the shape of fluid from a spherical cap to cylindrical cap.[9] When the viscosity is increased, the fluid is reluctant to be drawn towards the end of the lines. Due to the smaller amount of solvent, lines also dry quickly, resulting in nearly no bulge. Therefore, the uniformity of the line

width is improved when a higher viscosity ink is used. This is particularly beneficial for placing the lines closely. For example, when using these lines as source and drain of TFTs, channel length can be reduced more with better uniformly of the lines.

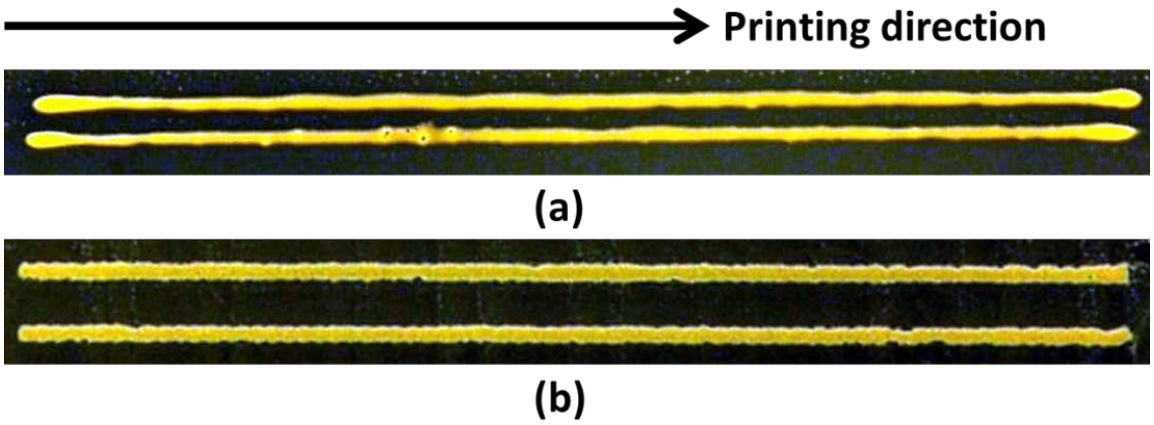


Figure 3.15 The effect of viscosity on the uniformity of the line width (a) when viscosity is lower than 10 cP (NPG-J) (b) when viscosity is 100 cP (diluted NPS).

Printing velocity also has a significant effect on the printed patterns. As shown in **Figure 3.16(a)**, for the same ink, incomplete dots are printed when printed at low speed compared to well-formed circular dots realized during high-speed printing. High printing speed leads to the increase of capillary number of the ink. Thus, it is found that relatively high capillary number is required to improve the printability of the inks in our gravure printing. The same behavior is also observed in more complex ink systems. When the NPS silver nanoparticle ink with viscosity of ~100 cP is used to print lines at different printing speeds, the low-speed printed lines show significant pinholes along the line as shown in **Figure 3.16(b)**. The number of pinholes decreases as the printing speed increases.

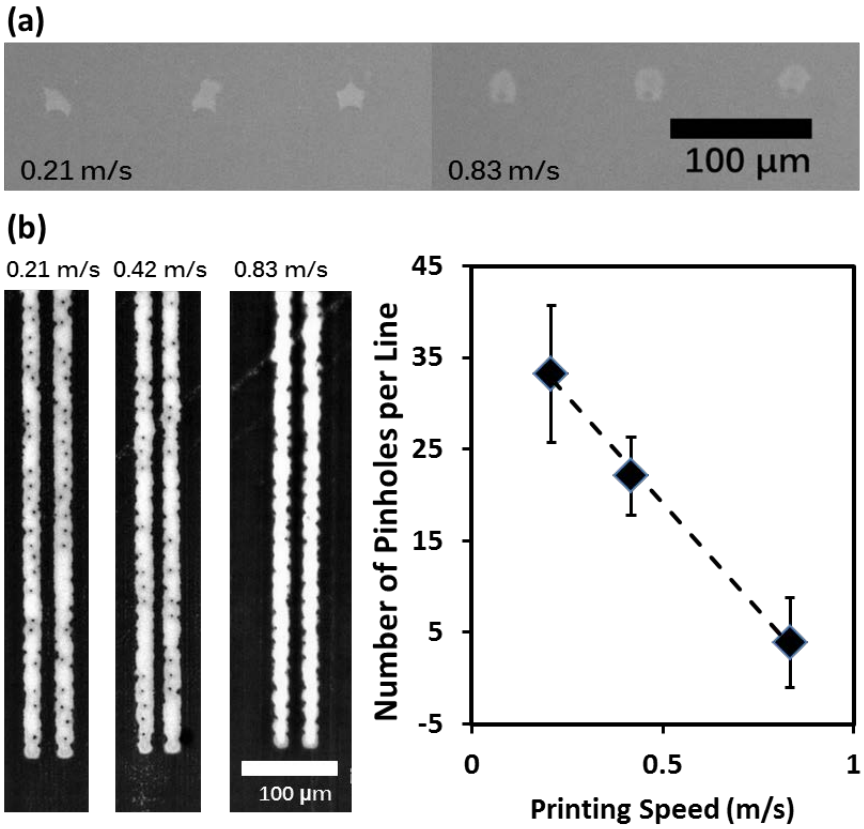


Figure 3.16 (a) Individual dots of PVP from 15 µm wide cells are printed at different printing speeds. The viscosity of the PVP ink is 90 cP. (b) Gravure printed 5 nm silver nanoparticle ink at different printing speeds. Viscosity of the ink is 100 cP and the cells are 12.5 µm wide with 2.5 µm spacing. The capillary number is calculated from the viscosity and printing speed; the accuracy of this value is limited by shear-thinning effects in the ink at high speeds. Average number of pinholes per a 900 µm long line is measured from 16 printed lines printed at different printing speeds.

3.5 Properties of the gravure-printed highly scaled metal lines

More detailed geometrical and electrical properties of the highly scaled gravure-printed gold and silver lines are summarized in this section. The gravure-printed gold and silver lines based on the optimized ink properties show good scalability and controllability.

3.5.1 Gold lines (sub 10 µm)

Although the metal ink has a complex fluid system due to additional surfactants, the printed metal lines obeyed the same trends as shown with the PVP ink shown in a previous section. Controlling the volume per unit length by changing the width and spacing of gravure cells enables precise scaling of the width of gravure-printed gold lines down to 8 µm as shown in **Figure 3.17**. Measured width of the gravure printed lines is in good agreement with the hydrostatically determined theoretical relationship in equation (1). Good accordance with the equation proves again good controllability of our printing process even for the metal nanoparticle ink. As the ratio of cell spacing (CS) to cell width (CW) is decreased (thus resulting in more volume per unit length), line edge roughness

(LER) is decreased (**Figure 3.18**). The LER as low as 2 μm allows for the realization of very tight gaps between adjacent printed lines.

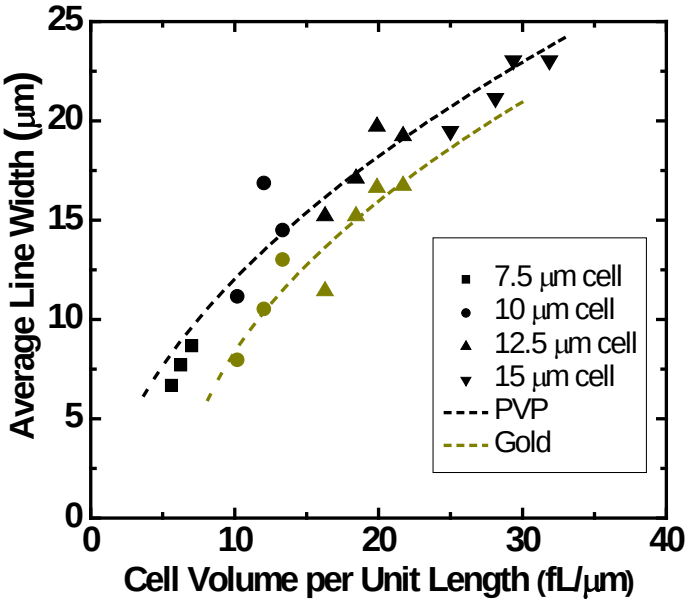


Figure 3.17 Scaling of gravure printed PVP (black) and gold (gold) lines on PEN substrate. Gravure cell sizes ranged from 7.5 μm to 15 μm with four different spacing from 2.5 μm to 7.5 μm.

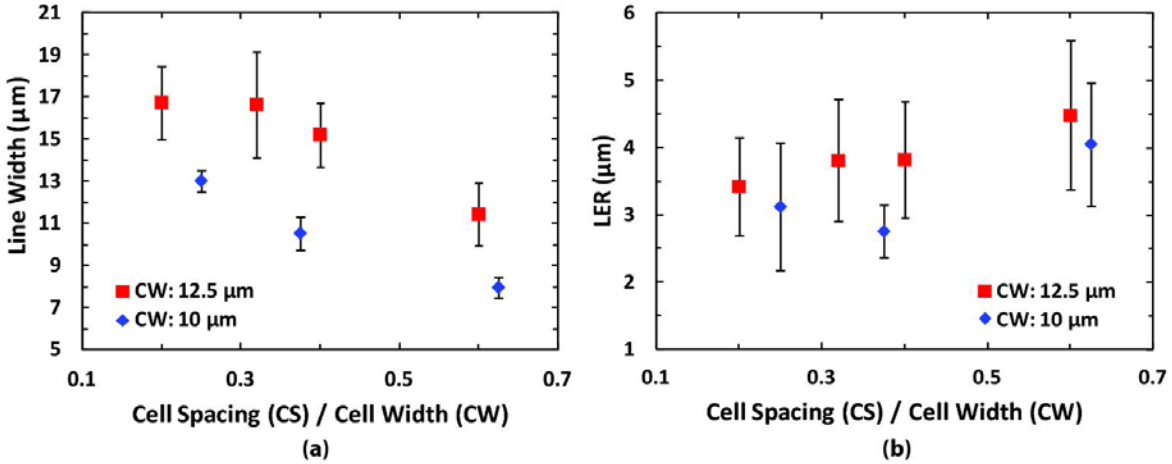


Figure 3.18 Scaling of gravure printed gold lines on 10 min UVO treated PEN. Line width and line edge roughness (LER) are plotted with respect to the ratio of cell spacing (CS) to cell width (CW) for 12.5 μm and 10 μm cells. Decrease in the ratio of CS to CW indicates an increase in the ink volume per unit length. (Whisker: standard deviation)

Highly scaled metal lines still deliver low sheet resistance of about 40 Ω/□, which is several orders of magnitude lower than commonly gravure-printed PEDOT:PSS lines,[7] and is more than adequate for use in OTFT electrodes. The line width, LER and sheet resistance of the lines printed using 10 μm cells with 3.75 μm spacing are shown in **Figure 3.19** below. The average line width is 10.5 μm, and average LER is 2.5 μm, attesting to the fidelity of the gravure printing process. The average sheet resistance is ~40Ω/□, which is more than adequate for use in OTFT electrodes.

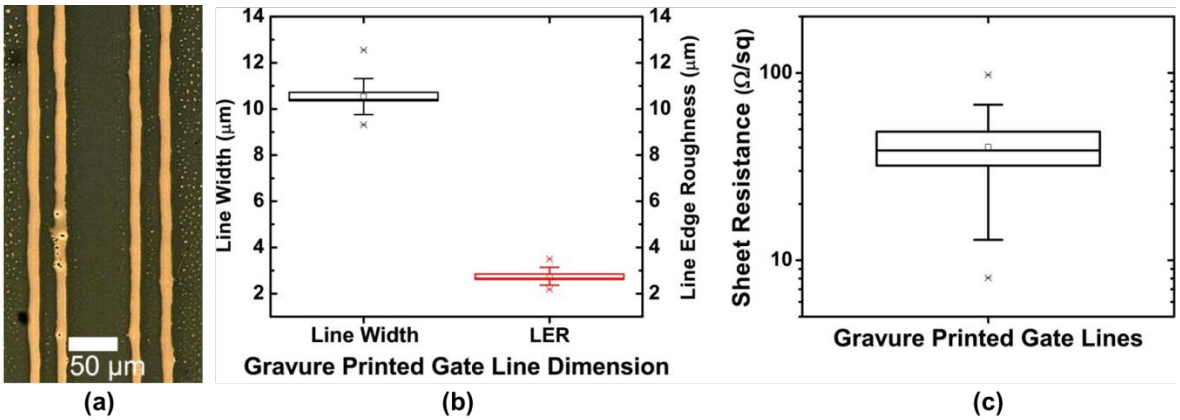


Figure 3.19 (a) Micrographs of gravure printed gold lines from cells (CW: 10 μm, CS: 3.75 μm) (b) Dimensional analysis of the gravure printed lines in (a) (total number of lines analyzed, 18) (c) Sheet resistance of gravure printed gate lines from two-point measurement. (Box: standard error, Whisker: standard deviation, star: minimum and maximum)

3.5.2 Silver lines (sub 5 μm)

Gravure-printed NPS silver lines also showed good controllability and even better scalability. With the usage of the smaller engraved cells down to 2.5 μm, the gravure printed silver lines showed line width below 5 μm as shown in **Figure 3.14** and **Figure 3.20**. The LER of the NPS lines are even smaller than 1 μm which potentially allows us to print multiple lines with very tight gap.

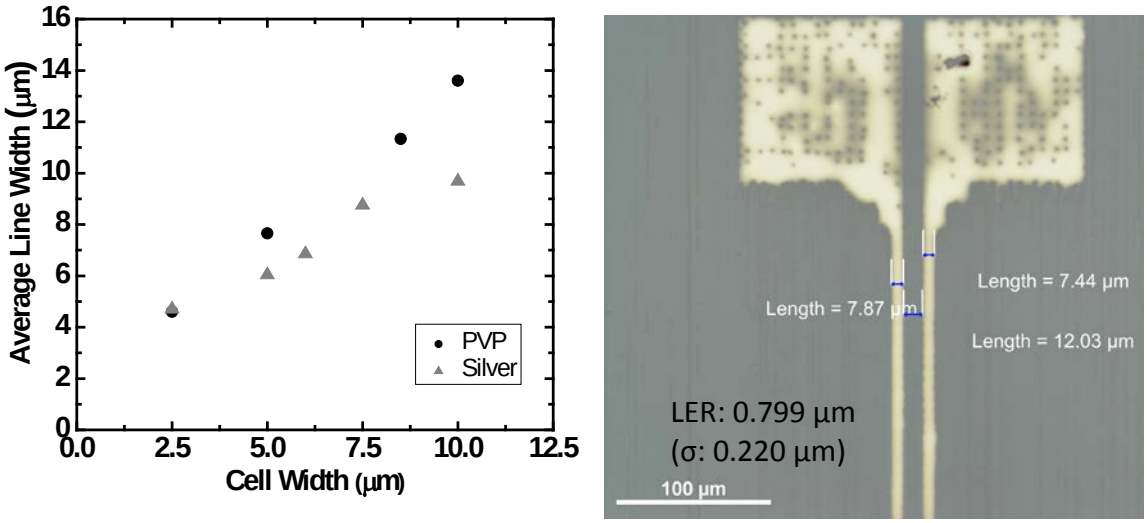


Figure 3.20 (a) Scaling of the gravure printed PVP and silver lines on PEN substrate below 5 μm. (b) Optical micrograph of gravure printed silver lines with 5 μm cells.

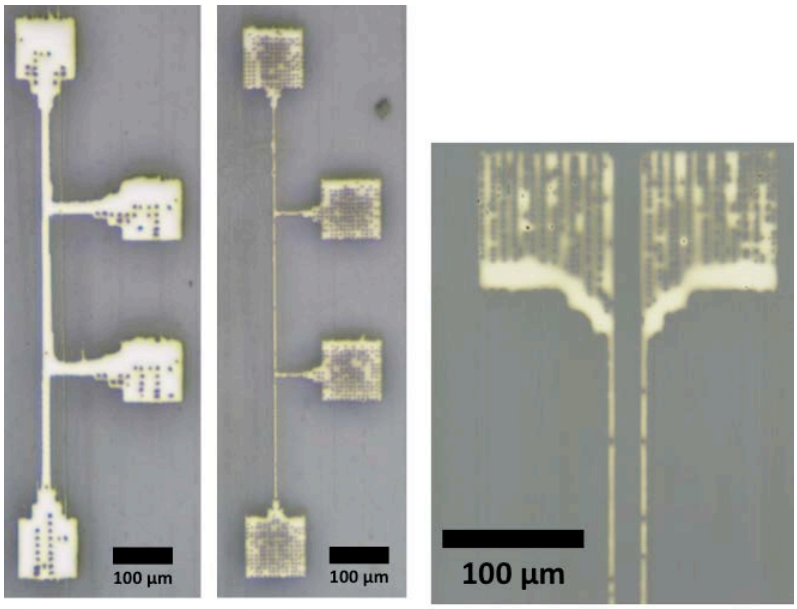
3.5.2.1 Sintering condition optimization

In order for the silver lines to be used in TFTs on plastic, good conductivity must be obtained using a processing temperature that is compatible with low-cost plastic substrates.

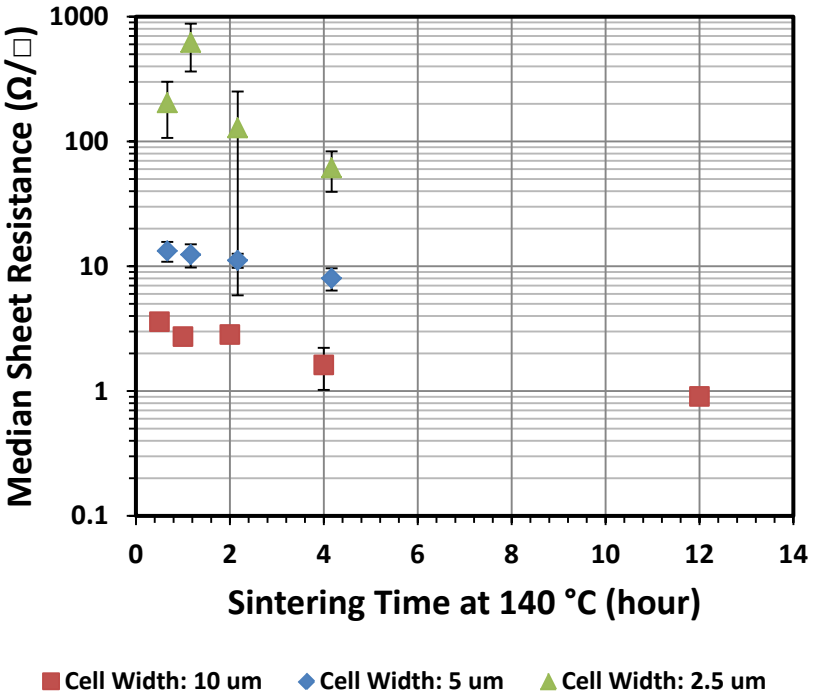
For the measurement of sheet resistance of the gravure printed silver lines, 4-point probe structures were gravure-printed with the NPS silver ink as shown in **Figure 3.21(a)**. One observation with this nanoparticle silver ink is its low temperature sintering capability when the features are highly scaled. The manufacturer-suggested sintering temperature for this ink is 220~230 °C for 1 hour, which agrees with the experimental data obtained from studies on thick films. However, when the printed features are highly scaled such that the film or feature thickness is around 100 nm, the printed features become conductive even after a sintering process at low temperature, 140°C as shown in **Figure 3.21(b)**. The low temperature sintering of the same or similar ink system has been reported by others as well.[10], [11] The thicker lines printed from larger cells show lower sheet resistance, and the resistance decreases as the sintering time is increased. For even the narrowest lines (from 2.5μm cells), the sheet resistance was as low as 60 Ω/□ which is still low enough for the printed TFTs while keeping the process temperature even compatible with the cheapest PET substrate. The lowest sheet resistance was even lower than 1 Ω/□. The broad range of electrode resistance obtained from one printed sample shows that our gravure printing can provide various options to meet interconnect specifications needed for building large-area electronics systems (e.g. display applications).

3.5.2.2 Doctor blade optimization

While the nature of contact printing allows good pattern reproduction in printing, ink transfer from non-patterned areas often happens because of the same nature of contact printing. For printed electronics applications, any printing or ink transfer in the non-patterned area will harm the printed circuits or devices due to possible circuit shorting or degradation of visual quality for display applications. Therefore, for the gravure printing to be more promising, it is important to eliminate residues on the roll during wiping process. It is found that the optimization of the doctor blade condition leads to significant improvement as shown in **Figure 3.22**. When the doctor blade pressure is increased from 20 psi to 50 psi, ink residue is clearly wiped better, leading to much clearer distinction of the printed features.



(a)



(b)

Figure 3.21 (a) Micrographs of the gravure-printed silver 4 point probe structures (b) The effect of sintering time on the sheet resistance of printed silver lines in (a).

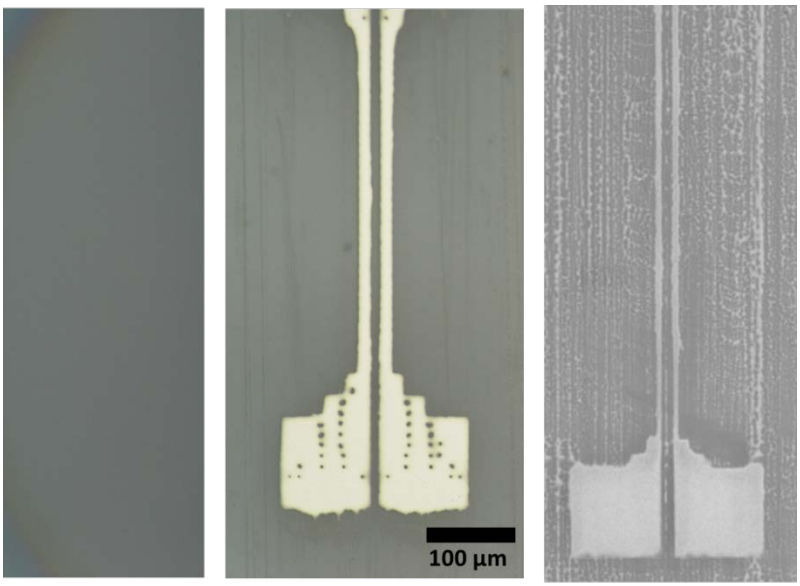


Figure 3.22 (a) Micrograph of PEN substrate before printing (b) Doctor blade pressure: 50 psi (c) Doctor blade pressure: 20 psi.

3.6 Summary

In this chapter, the scaling of gravure-printed lines is studied with the introduction of a novel electromechanical engraving technique. By reducing the size of the engraved cells down to 2.5 μm, unprecedented scaling to sub-5μm regime for both polymer and conductive lines is achieved. Minimized cell-to-cell variation in the electromechanically engraved patterns leads to very good controllability of the printed line dimension with accurate theoretical estimation. In addition to the scaling of the engraved cells, the conductive inks are optimized so that the printed lines are very conductive while having good surface morphology, which is critical for the usage in multilayer electronic devices (e.g. TFTs). The concentration of metal in the ink, size of metal nanoparticle, and the viscosity of the ink are found to be very critical in printing good highly scaled gravure-printed metal lines that can be used for TFTs. The sintering condition of the conductive ink is optimized, and thus post-annealing process is done at no higher than 140 °C, which is even compatible with very low-cost plastic substrates such as PET and PEN. The highly scaled gravure-printed metal lines will be used to build high performance thin-film transistors on plastic in the following chapter.

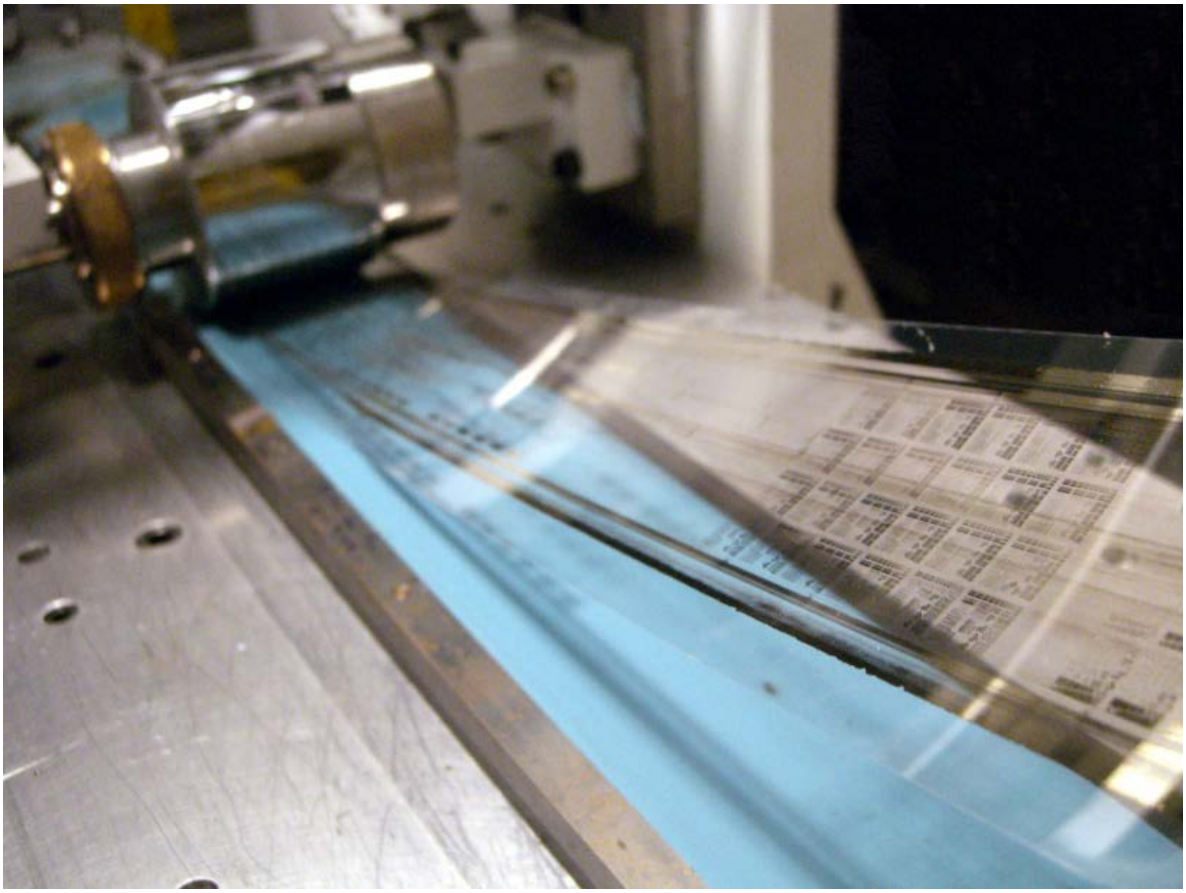


Figure 3.23 Highly-scaled gravure printing of silver inks on plastic substrate with custom-built gravure printer.

3.7 References

[1] T. Sekitani, Y. Noguchi, U. Zschieschang, H. Klauk, and T. Someya, “Organic transistors manufactured using inkjet technology with subfemtoliter accuracy,” *Proceedings of the National Academy of Sciences*, vol. 105, no. 13, pp. 4976 –4980, Apr. 2008.

[2] D. Soltman, B. Smith, H. Kang, S. J. S. Morris, and V. Subramanian, “Methodology for Inkjet Printing of Partially Wetting Films,” *Langmuir*, vol. 26, no. 19, pp. 15686–15693, Oct. 2010.

[3] Y. Jung, R. J. Kline, D. A. Fischer, E. K. Lin, M. Heeney, I. McCulloch, and D. M. DeLongchamp, “The Effect of Interfacial Roughness on the Thin Film Morphology and Charge Transport of High- Performance Polythiophenes,” *Advanced Functional Materials*, vol. 18, no. 5, pp. 742–750, Mar. 2008.

[4] A. C. Huebler, F. Doetz, H. Kempa, H. E. Katz, M. Bartzsch, N. Brandt, I. Hennig, U. Fuegmann, S. Vaidyanathan, J. Granstrom, S. Liu, A. Sydorenko, T. Zillger, G. Schmidt, K. Preissler, E. Reichmanis, P. Eckerle, F. Richter, T. Fischer, and U. Hahn, “Ring oscillator fabricated completely by means of mass-printing technologies,” *Organic Electronics*, vol. 8, no. 5, pp. 480–486, Oct. 2007.

[5] T. Fischer, U. Hahn, M. Dinter, M. Bartzsch, G. Schmidt, H. Kempa, and A. C. Huebler, “Novel in-line method for patterned deposition of conductive structures,” *Organic Electronics*, vol. 10, no. 3, pp. 547–550, May 2009.

[6] M. Hambsch, K. Reuter, M. Stanel, G. Schmidt, H. Kempa, U. Fügmann, U. Hahn, and A. C. Hübler, “Uniformity of fully gravure printed organic field-effect transistors,” *Materials Science and Engineering: B*, vol. 170, no. 1–3, pp. 93–98, Jun. 2010.

[7] G. C. Schmidt, M. Bellmann, B. Meier, M. Hambsch, K. Reuter, H. Kempa, and A. C. Hübler, “Modified mass printing technique for the realization of source/drain electrodes with high resolution,” *Organic Electronics*, vol. 11, no. 10, pp. 1683–1687, Oct. 2010.

[8] A. de la Fuente Vornbrock, D. Sung, H. Kang, R. Kitsomboonloha, and V. Subramanian, “Fully gravure and ink-jet printed high speed pBTTT organic thin film transistors,” *Organic Electronics*, vol. 11, no. 12, pp. 2037–2044, Dec. 2010.

[9] P. C. Duineveld, “The stability of ink-jet printed lines of liquid with zero receding contact angle on a homogeneous substrate,” *Journal of Fluid Mechanics*, vol. 477, pp. 175–200, 2003.

[10] T. Yokota, T. Sekitani, Y. Kato, K. Kuribara, U. Zschieschang, H. Klauk, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, and T. Someya, “Low-voltage organic transistor with subfemtoliter inkjet source–drain contacts,” *MRS Communications*, vol. 1, no. 01, pp. 3–6, 2011.

[11] E.-U. Kim, K.-J. Baeg, Y.-Y. Noh, D.-Y. Kim, T. Lee, I. Park, and G.-Y. Jung, “Templated assembly of metal nanoparticles in nanoimprinted patterns for metal nanowire fabrication,” *Nanotechnology*, vol. 20, no. 35, p. 355302, Sep. 2009.

Chapter 4

Highly-Scaled Gravure-Printed OTFTs and Circuits

4.1 Fabrication process and transistor structure

Given the high quality and scalability of the gravure-printed lines in Chapter 3, we proceed to demonstrate their integration into high-performance gravure-printed OTFTs and simple test circuits in this chapter. In order to fully utilize the benefit of highly scaled lines, bottom-gate (BG) TFTs are pursued (see the device structure in **Figure 4.1**). To realize BG TFTs on PEN, metal gate lines and polymer dielectric layer were gravure-printed as illustrated in **Figure 4.2**. It is necessary to have minimized overlapping of the source and drain electrodes on the gate electrode to ensure good AC characteristics. Though significant effort has been devoted to improve the layer-to-layer alignment of roll-to-roll printing processes, the overlay printing registration accuracy of these processes is still typically worse that 15 μm,[1] which is not adequate for the targeted OTFTs with 5~10 μm channel length. Therefore, in this work, silver source and drain electrodes were deposited by inkjet printing; note that inkjet printing can be easily integrated into roll-to-roll processes, and can be combined with high-speed gravure printing to realize high-speed overall layer printing. As a last step, organic semiconductor film is deposited. As a choice of the semiconductor, two organic materials, supplied by EMD Chemicals, are investigated herein: a polymer semiconductor, poly(2,5-bis(3-alkythiophen-2-yl)thieno[3,2-b]thiophene) also widely known as pBTTT; and a recently developed high-performance organic semiconductor, S1200. Our group has previously shown that pBTTT can be gravure-printable with good stability and uniformity.[2] Although not yet widely used, S1200 is also a good candidate for our process since the material is particularly designed to be compatible with various types of printing processes while improving field-effect mobility. Detailed optimization of the fabrication processes for both material sets will be provided in this chapter. In particular, we will focus on proper electrostatic integrity of printed short channel TFTs ($L_{ch} \leq 10$ μm).

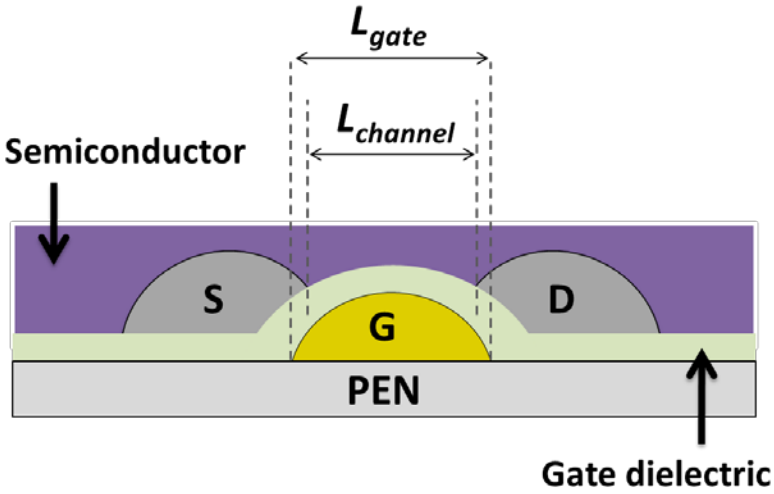


Figure 4.1 Cross-sectional diagram of the bottom-gate TFT structure. $L_{overlap}$ is defined as the difference between L_{gate} and $L_{channel}$.

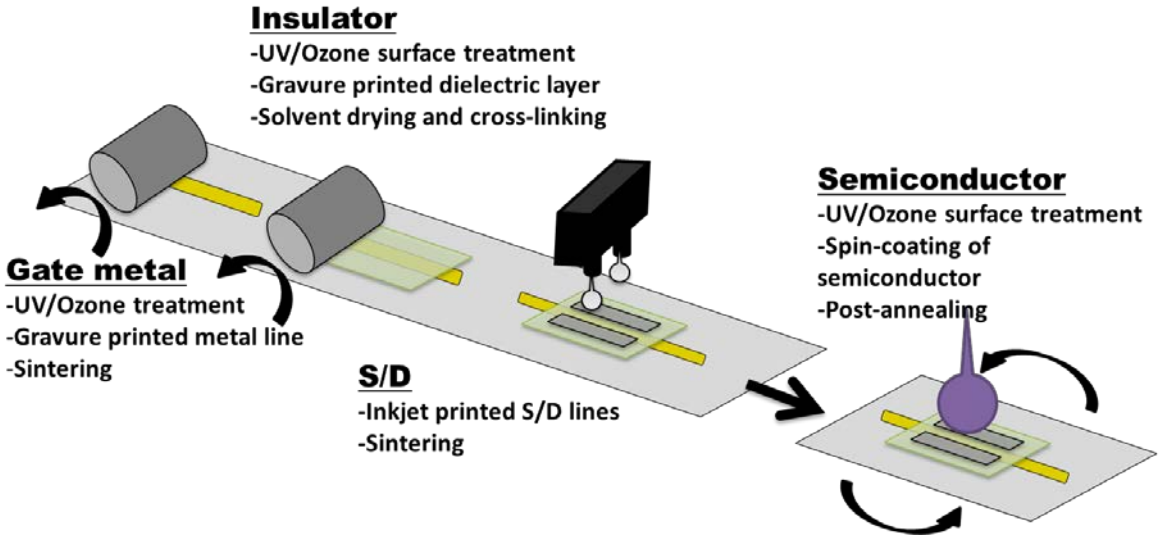


Figure 4.2 Fabrication process flow for the gravure and inkjet-printed highly scaled TFTs in this chapter.

4.2 pBTTT TFTs (L_{ch}=10 µm)

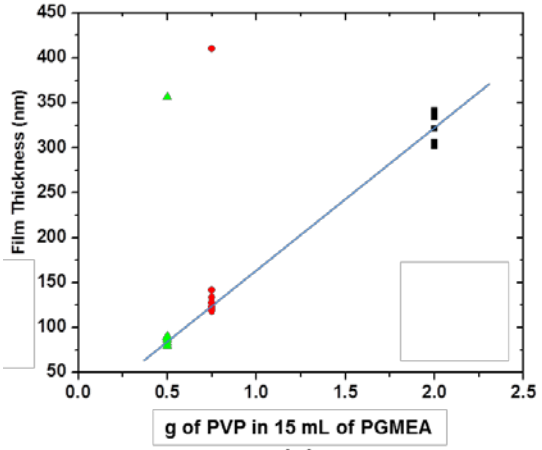
Firstly, pBTTT based transistors will be discussed. In the case of pBTTT, gravure-printed NPG-J gold lines scaled below 10 µm (see Chapter 3.4.1) are used as gate electrodes. As gate dielectric, PVP with poly(melamine-co-formaldehyde) as a cross-linker is used due to its excellent performance and printability. S/D electrodes are inkjet-printed with CCI-300 silver ink. pBTTT layer is spin-coated as a last step. This section is organized as follows. PVP gate capacitors with gravure-printed bottom electrode will be first characterized. Then, the semiconductor layer will be optimized for our device structure.

Afterwards, electrical characteristics of fully fabricated pBTTT TFTs on PEN will be discussed.

4.2.1 Capacitors

Not only do we have to obtain good electrical insulation properties of the dielectric layer, but also the gate capacitors must be properly designed to obtain enough gate controllability for minimization of short-channel effects in our highly scaled TFTs. In the same way that inkjet-printed film thickness is controlled by changing inkjet printing parameters in Chapter 2, the thickness of the gravure printed film can be controlled by the gravure printing parameters: cell width, cell spacing, and ink concentration as shown in **Figure 4.3**. With the precise thickness control, PVP MIM (metal-insulator-metal) capacitors with 4 different thicknesses are fabricated as shown in **Figure 4.4**. Here, the bottom electrodes are gravure-printed NPG-J gold rectangles instead of lines so that the area of the capacitors is large enough to provide measurable capacitance values (at least a few pF). Inkjet-printed CCI-300 silver ink is used as top electrodes. In general, larger capacitors are more vulnerable to defects, leading to lower yield. In addition, since larger gravure printed rectangles show tall coffee-ring edges around the boundary, it may lead to even worse electrical insulation characteristics than when narrower coffee-ring-free lines are used as bottom electrodes. Thus, it is worthy to note that the characteristics of the gate capacitor with highly scaled lines as bottom electrode might actually be better than those of the capacitors in **Figure 4.4**. As shown in **Figure 4.5**, it is found that the PVP films thinner than 160 nm failed to provide good insulating properties. PVP films thicker than 160 nm showed good electrical insulating properties. However, as the film gets thinner than 160 nm, most of the capacitors broke down. The failure plot in **Figure 4.6(a)** also confirms the minimum PVP film thickness limitation. Therefore, PVP films with thickness equal to or larger than 160 nm will only be used as gate dielectric of pBTTT TFTs. More investigation on further reduction of the PVP film thickness is a subject of future work; however, 160 nm thick gate dielectric is adequate to have good electrostatic scaling in the short channel devices herein. This thinner dielectric layer allows for reduced TFT operation voltage as well.

One important point to note is the improved insulation characteristics of the PVP film with our gravure-printed bottom electrodes. Due to the smoothness of the gravure-printed gate lines (RMS roughness of 2.31 nm; see Chapter 3.3.2.1), we are able to deliver low leakage of 100 nA/cm^2 at 1 MV/cm (10 times lower than our previous result when organometallic inks were used [2] and more than two orders of magnitude lower than when evaporated silver is used as both bottom and top electrodes). High breakdown field (>2 MV/cm, **Figure 4.7**) is also achieved. Here, the breakdown field is defined as the electric field at which the current density is equal to 1 $\mu A/cm^2$. Such a current-defined limit was used due to the dominance of soft breakdown, rather than hard breakdown, in PVP dielectrics. Good electrical characteristics of the gravure-printed PVP film are very encouraging; thus, the PVP film will be used for the highly scaled pBTTT TFTs in the next section.



(a)

PVP in 15 mL of PGMEA (g)	PVP concentration (wt%)	Film thickness (nm)	Volume of cross-linker (µL)
2	15.2	320	800
0.75	5.7	102	300
0.5	3.8	71	200

(b)

Figure 4.3 (a) Gravure-printed PVP film thickness as a function of the concentration of the PVP polymer ink. (b) Data for the PVP films in (a).

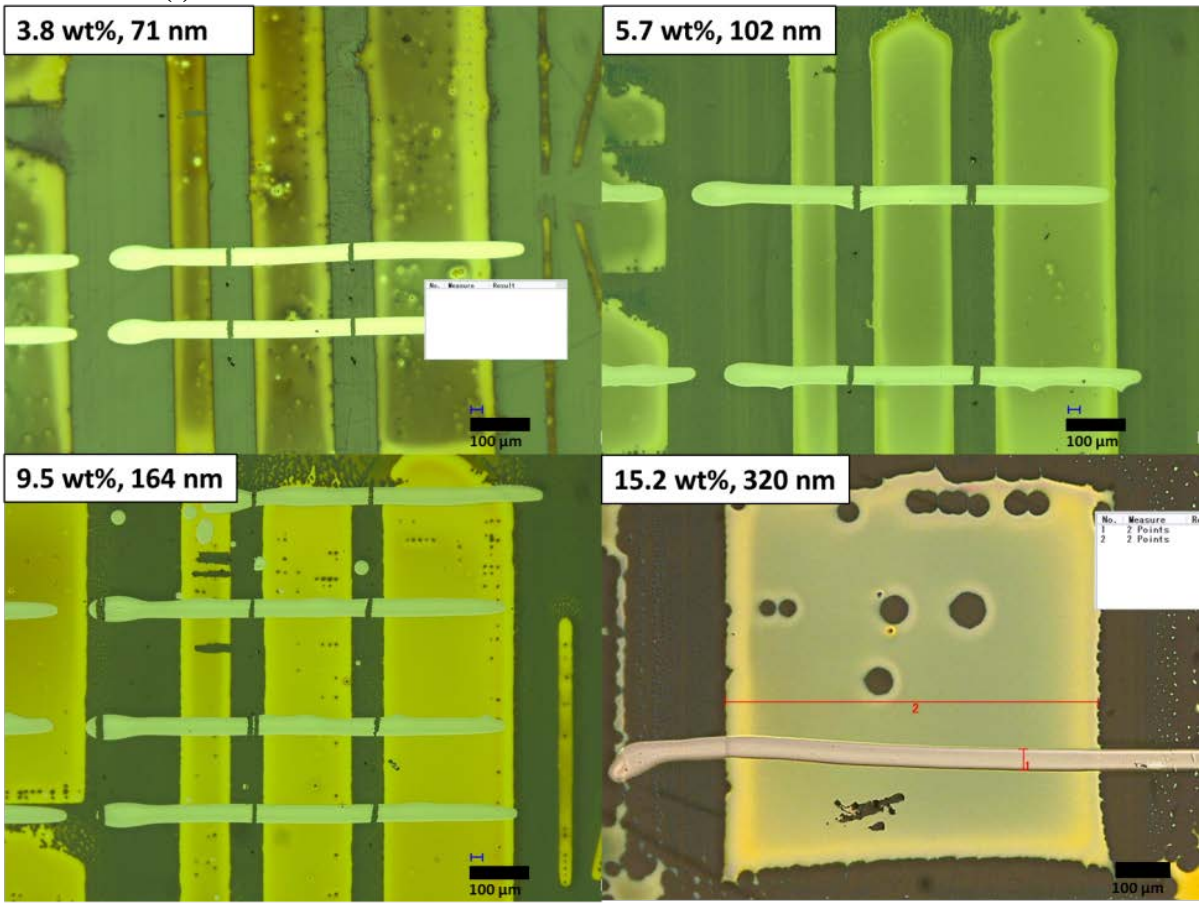


Figure 4.4 Gravure-printed PVP capacitors on PEN substrate with different PVP film thicknesses. Bottom electrodes (rectangles or squares) are gravure-printed NPG-J gold electrodes on PEN, blanket dielectric layer films are gravure printed, and horizontal top CCI-300 silver electrode lines are inkjet-printed.

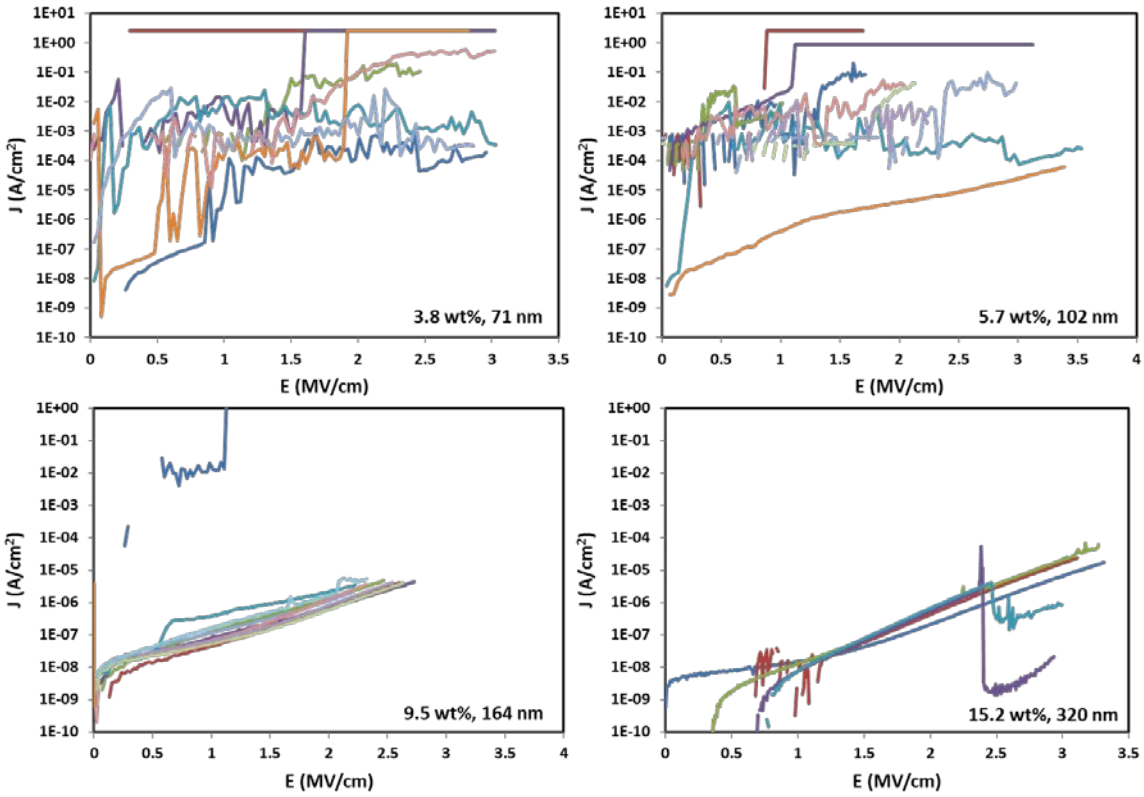


Figure 4.5 Current density and electric field characteristics of the gravure-printed PVP capacitors in Figure 4.4.

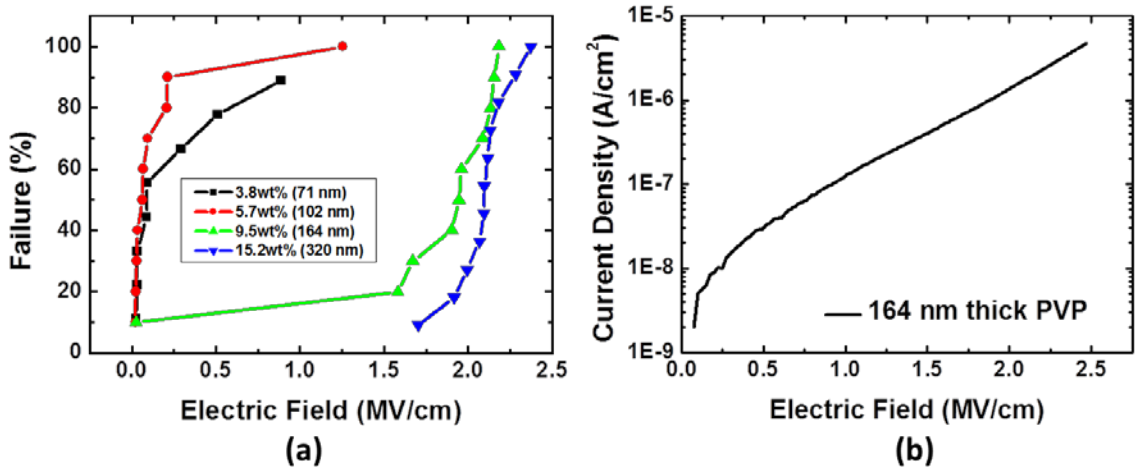


Figure 4.6 (a) Breakdown characteristics of the cross-linked PVP with different thickness. Capacitors show excellent yield for thicknesses >164nm; which was used to fabricate the devices herein. Breakdown field is defined as the field at which the current density is 1 μA/cm^2. (b) Representative current density through the cross-linked PVP layer.

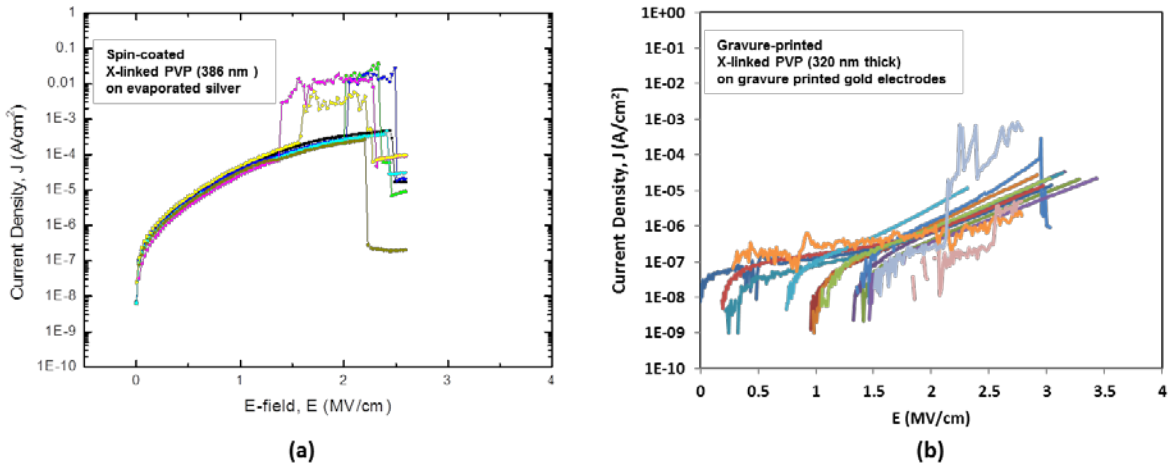


Figure 4.7 (a) Current density of spin-coated PVP capacitors on evaporated silver bottom electrode. Both bottom and top electrodes are evaporated silver through shadow masks. Corning 1737 display grade glass substrate is used as a substrate. (b) Current density of gravure-printed PVP capacitors on PEN substrate. As explained within the graph, the bottom electrodes are gravure-printed NPG-J gold, and top electrodes are inkjet-printed CCI-300 silver.

4.2.2 pBTTT

4.2.2.1 Effect of annealing and cooling condition on pBTTT

In this section, optimum-processing condition for the pBTTT film deposition and follow-up treatment will be investigated. Because pBTTT forms isotropic liquid crystals when annealed above a certain temperature, uniform heating provides uniform crystalline structure of the semiconductor, resulting in minimized device-to-device variation. Thus, it is easy to expect the effect of different annealing temperature on the characteristics of the pBTTT layer. In addition, the cooling speed of the pBTTT film after annealing is known to affect the quality of the film.[3], [4] In those works, it was found that the saturation mobility is significantly increased as the annealing temperature increases in response to the bulk liquid crystalline transition. Also, slow cooling of the pBTTT film after annealing results in smoother films and higher mobility because fast cooling prevents enough release of heat for the recrystallization of the polymer. Thus, it is found that the cooling rate below 15 °C/min is required in order to achieve the best performance. However, the device structures employed in these works are different from those of the proposed printed devices here. Firstly, we propose using inkjet-printed silver S/D electrodes for fabrication cost benefit whereas evaporated gold electrodes are used in their works. In addition, bottom S/D contacts are proposed here instead of top contact structure. Secondly and perhaps more importantly, the semiconductor/dielectric interface at which the channel of the TFTs is formed is different. For the previous works mentioned above, octyltrichlorosilane (OTS) treated silicon dioxide is used as gate dielectric layer. However, due to the incompatibility of those materials with printing processes, we choose to use polymer dielectric. The effect of annealing and cooling conditions on the carrier transport of the pBTTT film on PVP dielectric layer is therefore not known yet. Lastly, side chain groups of the pBTTT materials in both references and ours are slightly different although the different side chain groups are expected to have more significance on the solubility of the polymer than

mobility. Thus, in this experiment, both annealing and cooling temperatures are properly chosen as variables as organized in **Table 4.1**. Cooling speed is controlled by varying the set temperature of a cooling metal on which the TFT samples are cooled down after annealing. For fast cooling, the samples are moved to a cooling metal plate that is kept at room temperature. For slow cooling, a metal block that is preheated to the annealing temperature of pBTTT is naturally cooled down to room temperature after TFT samples are moved onto it. It approximately took about 10 minutes to cool down to room temperature, which gives us approximately 8~14 °C/min cooling rate. pBTTT film thickness is also varied by altering spin-coating speed.

Sample #	Spin speed (RPM)	Annealing temperature (°C)	Annealing time (minute)	Cooling speed (no unit)
PVP3	3000	100	10	Slow
PVP4	3000	100	10	Fast
PVP5	3000	130	10	Slow
PVP6	3000	130	10	Fast
PVP7	3000	160	10	Slow
PVP8	3000	160	10	Fast
PVP9	6000	100	10	Slow
PVP10	6000	100	10	Fast
PVP11	6000	130	10	Slow
PVP12	6000	130	10	Fast
PVP13	6000	160	10	Slow
PVP14	6000	160	10	Fast

Table 4.1 Design of experiment for the optimization of the deposition and post-annealing of pBTTT film.

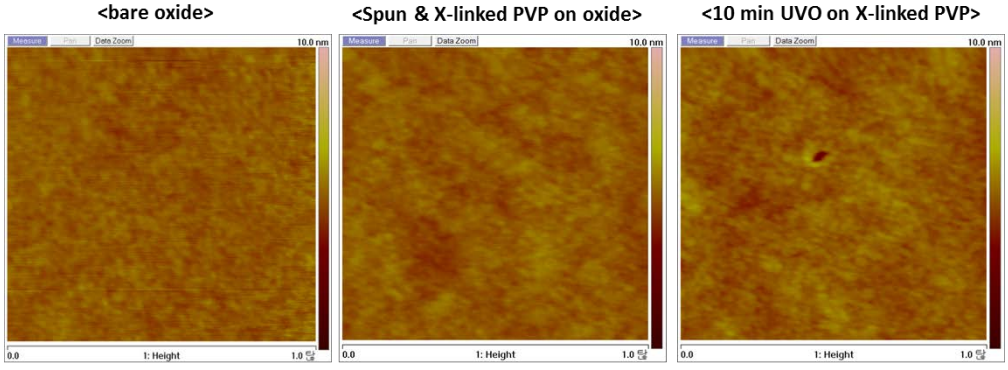


Figure 4.8 Surface roughness of substrates on which pBTTT is deposited. AFM images have a scan size of 1 μm by 1 μm. The vertical scale of the scan is 10 nm.

Before running experiments, the surface roughness of the dielectric layer interface is determined since it has been previously observed that the interfacial roughness of the dielectric layer plays a significant role in the pBTTT thin film morphology and thus transport performance.[5] In **Figure 4.8**, surface roughness of three different interfaces is given: bare oxide on which PVP film is deposited; PVP film after crosslinking; and crosslinked PVP film after 10 min UV/Ozone treatment for surface energy modification which is necessary for proper deposition of pBTTT film. For all the conditions, it is found that the RMS roughness is below 0.3 nm, below the thickness beyond which the degradation of saturation mobility is observed in [5]. Therefore, the effect of interfacial roughness is insignificant in this experiment.

The gate electrode of the test devices is heavily doped n-type silicon. A spin-coated PVP film on top of 100 nm thick SiO_2 was used as the gate dielectric. S/D contacts are inkjet-printed CCI-300 silver lines with channel lengths from 100 μm down to 10 μm. Lastly as mentioned above, the pBTTT film is spin-coated, annealed, and cooled under nitrogen. In this section, one kind of pBTTT formulation, SP210 supplied by EMD Chemicals Inc., is used. All the electrical measurements are done under N_2. Typical characteristics of the fabricated back-gated pBTTT TFTs are provided in **Figure 4.9** for both long and short channels. Overall, the transistors operated very well. Field dependent mobility is also presented. Saturation mobility increases as gate bias increases. However, linear mobility is degraded at high gate bias. One thing to note is that the linear mobility is much lower in short channel devices because of more significant contact resistance as shown in the output characteristics of the devices.

Long channel device results are summarized in **Figure 4.10**. Unfortunately, the maximum field-effect mobility achieved throughout the samples is lower than what has been previously reported, possibly due to the un-optimized S/D contact barriers and the PVP polymer dielectric material used herein. Fabricated TFTs showed the following characteristics. Firstly, there is a clear difference between slow cooling (blue) and fast cooling (red). For all the spin-coating and annealing conditions, slow cooling always gave higher mobilities as expected from a previous report.[4] Secondly, the overall mobilities are slightly higher in the case of faster spin coating at 6000 rpm. Lastly, the mobility in our samples decreases as annealing temperature increases, which is an opposite trend compared to the previous report.[3] A similar trend was also observed in short channel devices as shown in **Figure 4.11**. Other device parameters including on/off ratio, subthreshold swing (SS), and V_{ON} are also shown in **Figure 4.12**. Though on/off ratio is similar throughout the samples, SS and V_{ON} seemed to be dependent upon the annealing temperature. As annealing temperature increases, SS decreases, and V_{ON} decreases. The improvement of SS, in general, suggests that the semiconductor film quality (e.g. trap density) is improved as the annealing temperature increases. Based on surface morphology of the pBTTT films measured by AFM in **Figure 4.13**, as the annealing temperature increases, bigger and flatter domains are obtained, which could possibly indicate lower trap densities within the pBTTT film and thus lower SS. It is, however, not clear why the V_{ON} (or threshold voltage) shifts toward more negative values and why the mobility decreases as the annealing temperature increases.

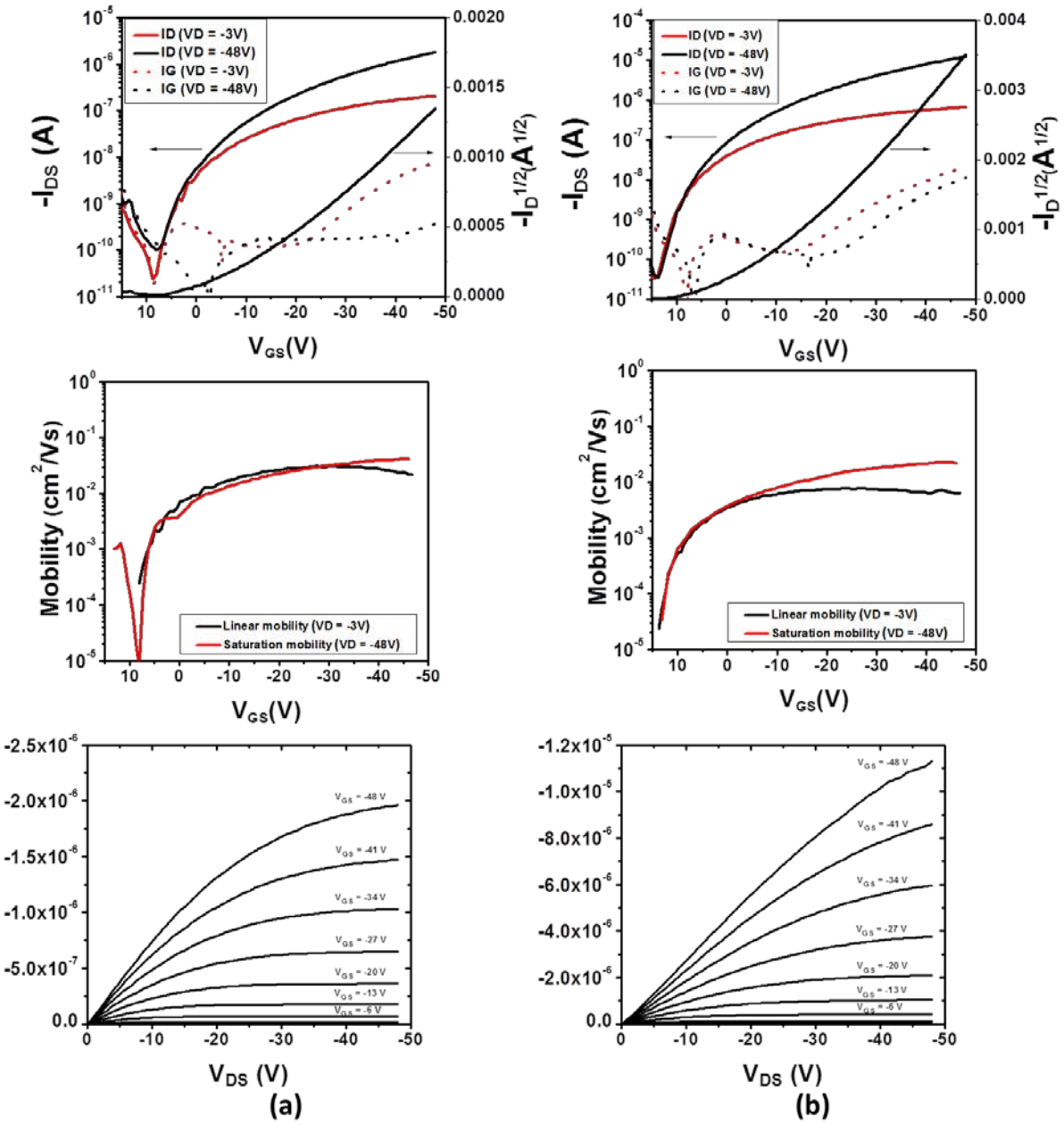


Figure 4.9 Transfer and output characteristics, and field-dependent mobilities of the back-gated pBTTT TFTs (a) L_{ch} ≈100 μm, (b) L_{ch} ≈10 μm

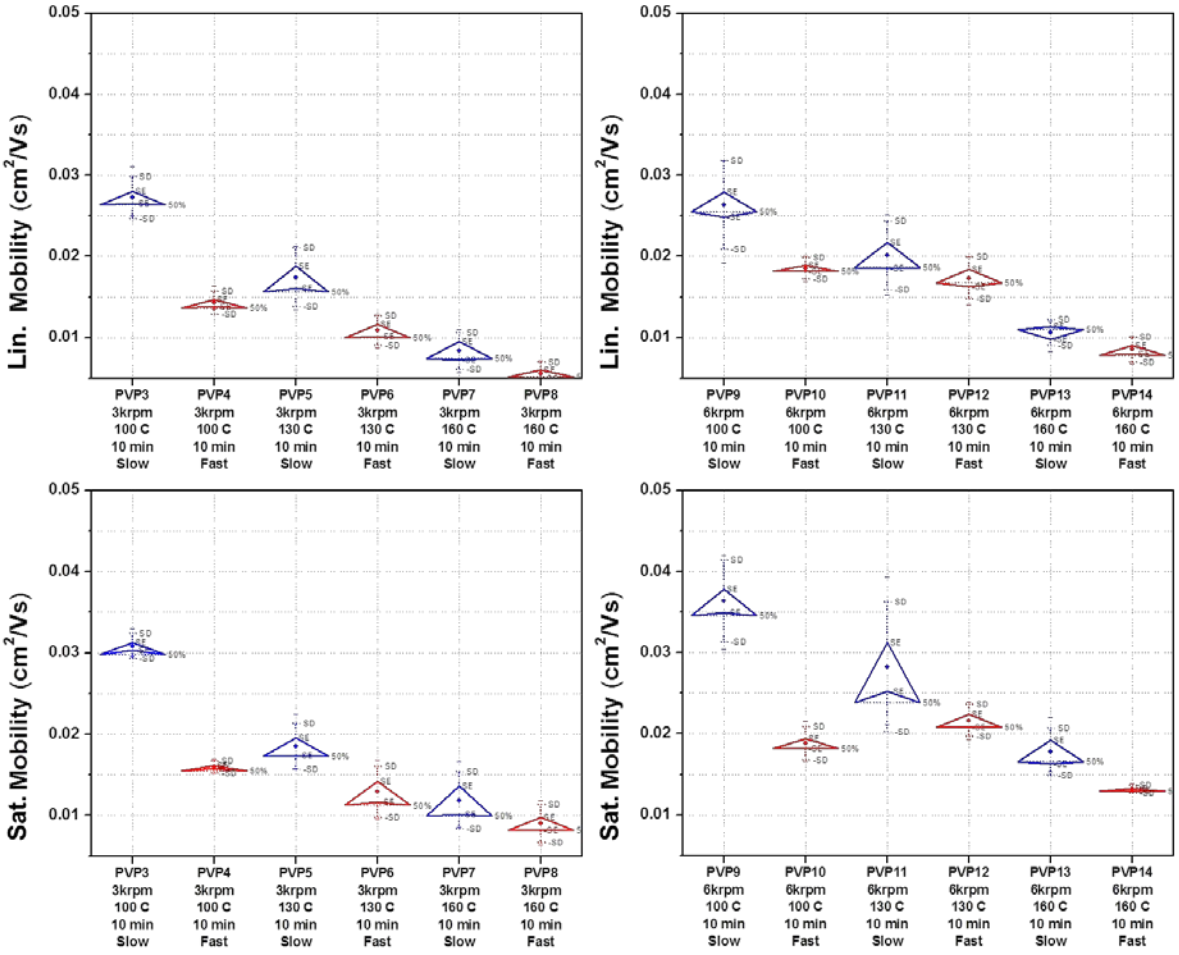


Figure 4.10 Field-effect mobilities of the back-gated pBTTT TFTs (long channel devices, $L_{ch} \geq 40$ µm, $t_{pvp,eff} = 311$ nm)

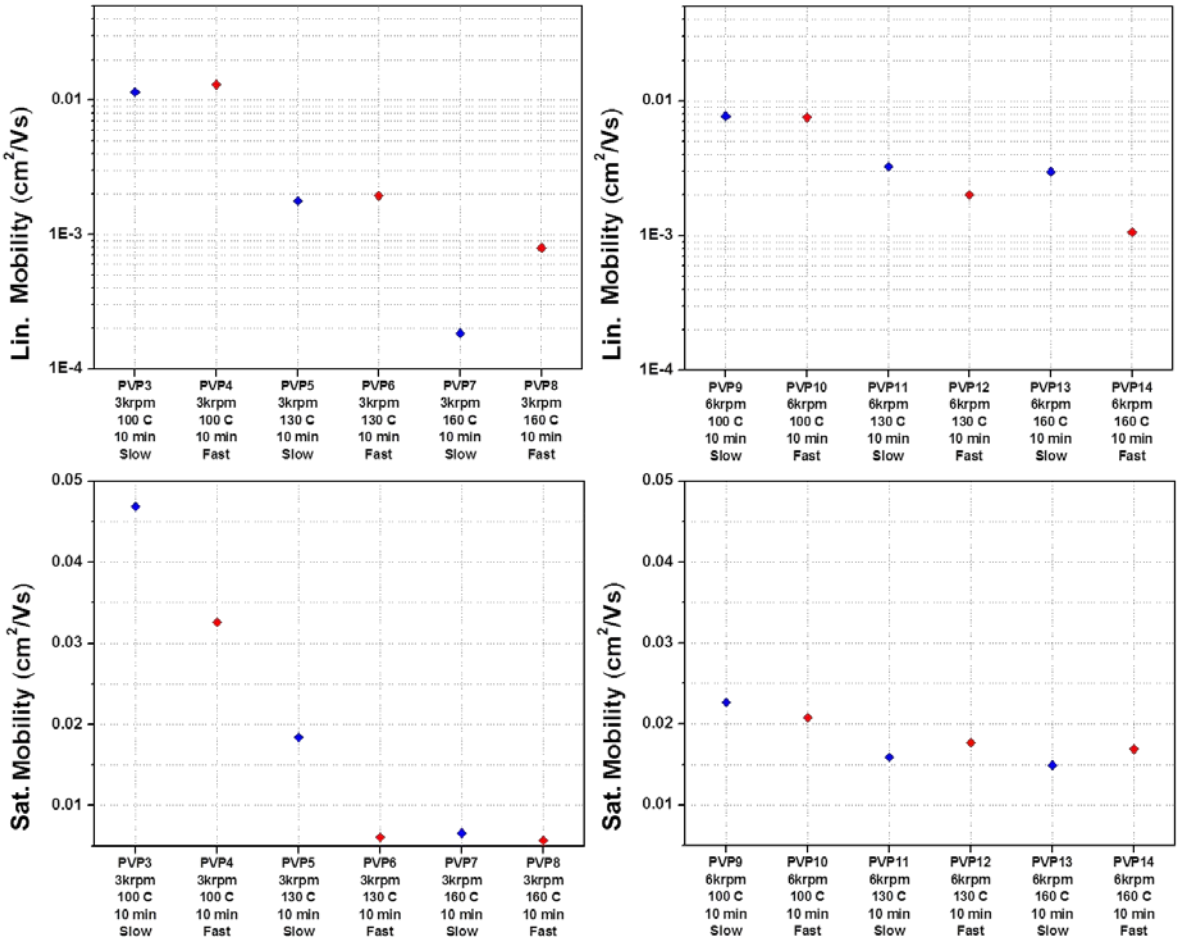


Figure 4.11 Field-effect mobilities of the back-gated pBTTT TFTs (short channel devices, $L_{ch} < 10$ µm, $t_{pvp,eff} = 311$ nm)

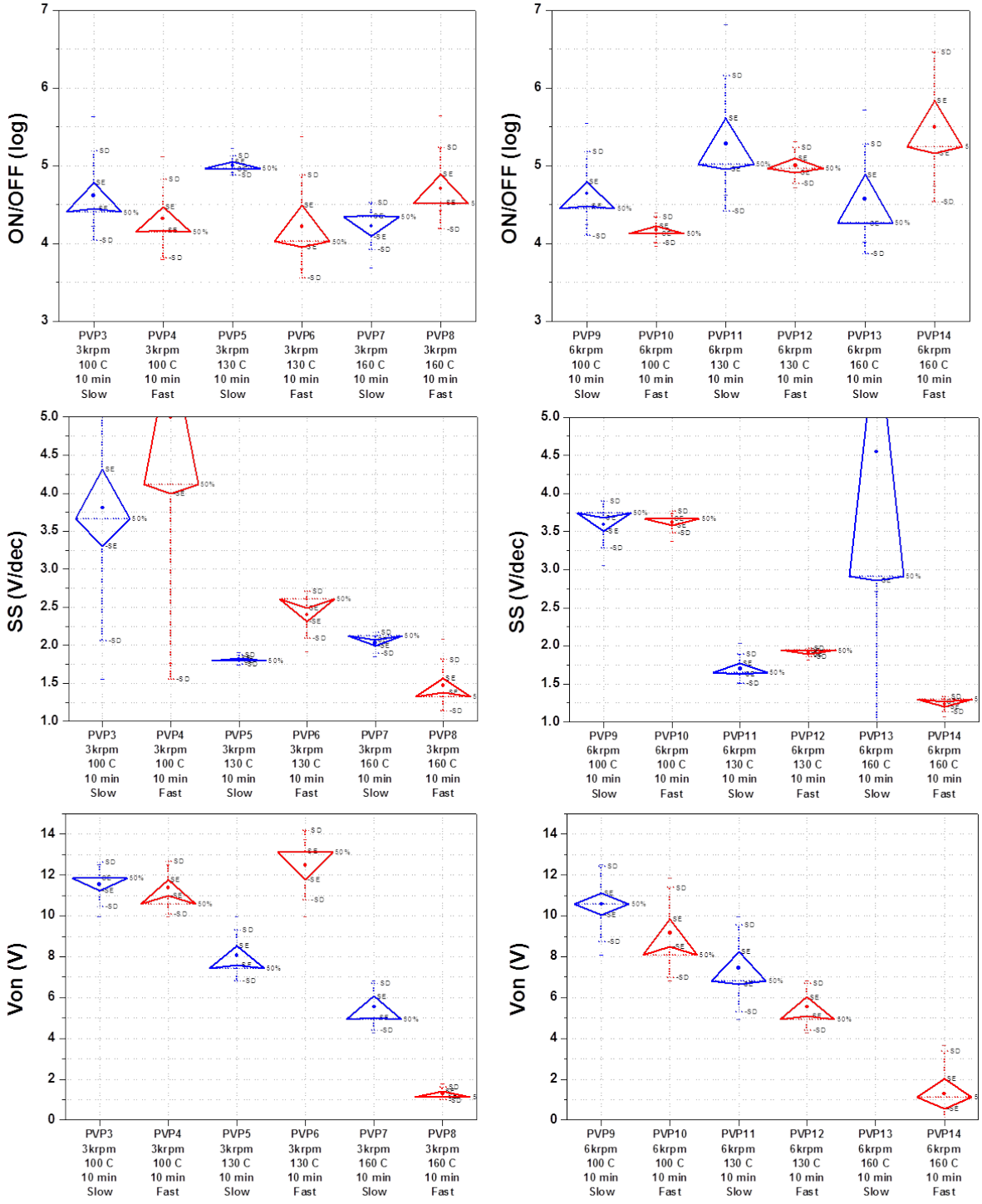


Figure 4.12 Summary of other TFT parameters of the back-gated pBTTT TFTs. (long channel devices, $L_{ch} \geq 40$ µm, $t_{pvp,eff} = 311$ nm)

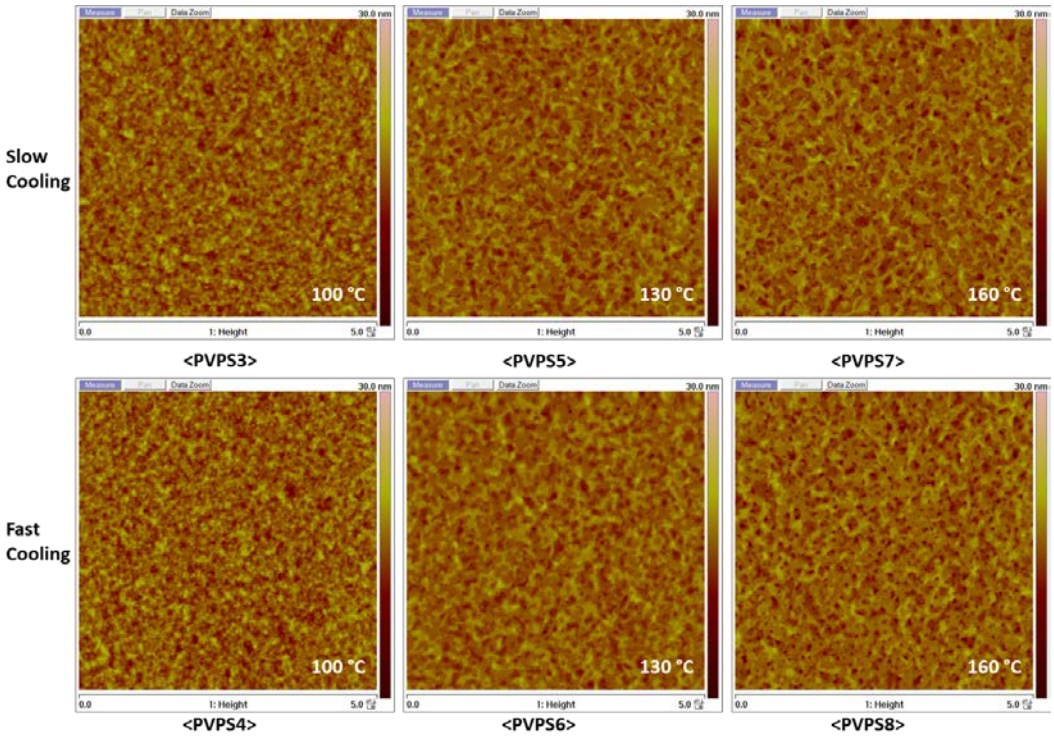


Figure 4.13 Effect of annealing temperatures and cooling rate on the surface morphology of pBTTT films.

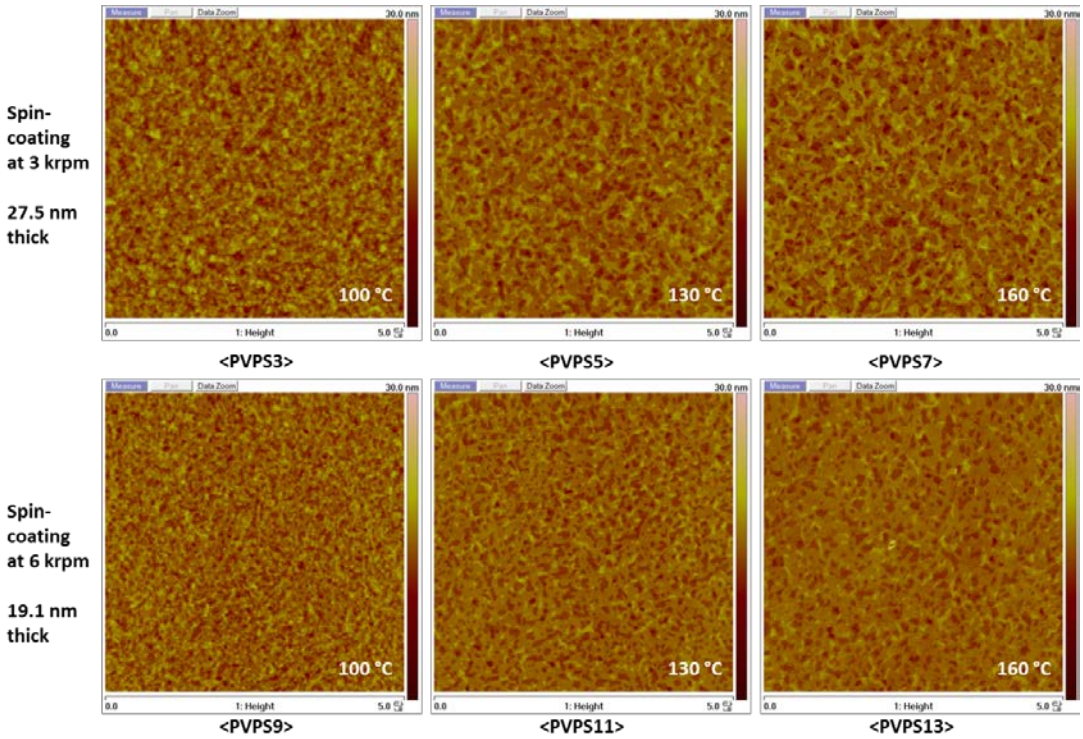


Figure 4.14 Effect of the thickness of pBTTT film on the surface morphology of pBTTT films.

4.2.2.2 Contact resistance and short channel behavior

As observed from the output characteristics of the pBTTT TFTs, there is clear S/D contact resistance and the presence of an injection barrier. In this section, the contact resistance will be analyzed based on the commonly used transmission line method (TLM). The samples in the previous section are used for this analysis since various channel lengths are obtained by inkjet printing. In order for the TLM to be properly applied, the uniformity of the channel resistance must be maintained regardless of the channel length. Since polymer semiconductors such as pBTTT show good uniformity compared to small molecule organic semiconductors, TLM was well applied to our samples as shown in **Figure 4.15**. Good linear fitting is obtained for various gate bias conditions. Extracted data are presented in **Figure 4.16** based on the following equation (1) where R_S is channel sheet resistance and R_{cont} is contact resistance.

$$R_{total} = \frac{V_{DS}}{I_{DS}} = R_S\left(\frac{L}{W}\right) + 2R_{cont} \quad (1)$$

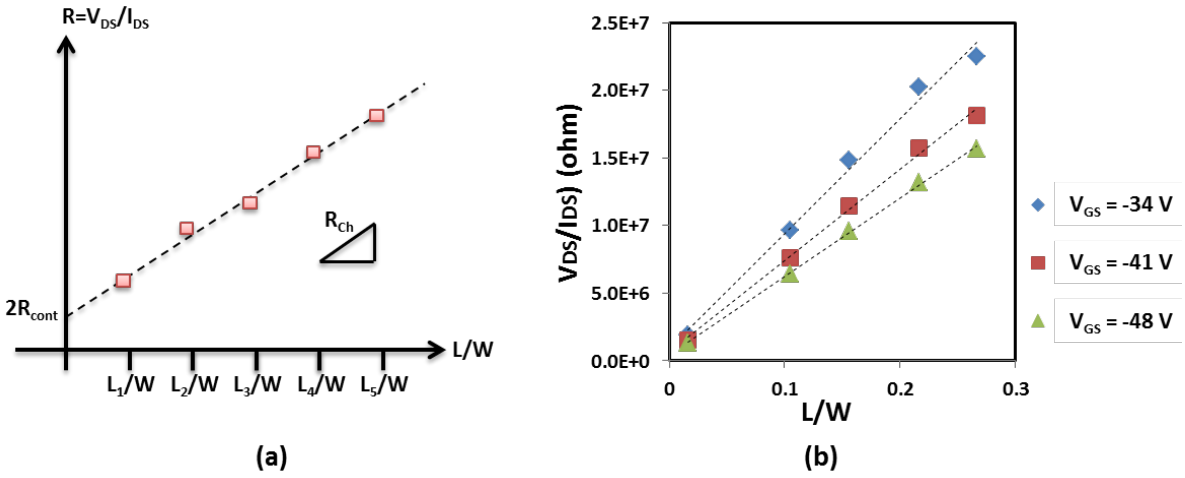


Figure 4.15 (a) Transmission-line method (TLM), (b) measured data from the pBTTT TFTs at different gate bias.

On average, the contact resistances, R_{cont}, are on the order of 10^6 Ω, and channel sheet resistance, R_S, is 10^8 Ω/sq. Based on that, in short channel devices (L/W ≤ 10/200 = 0.05), channel resistance, R_{ch} (=R_S×(L/W)), is about 5×10^6 Ω and it is comparable to the contact resistances. Thus, it is no surprise that we observed significant contact resistances in the output characteristic of the short channel pBTTT TFTs.

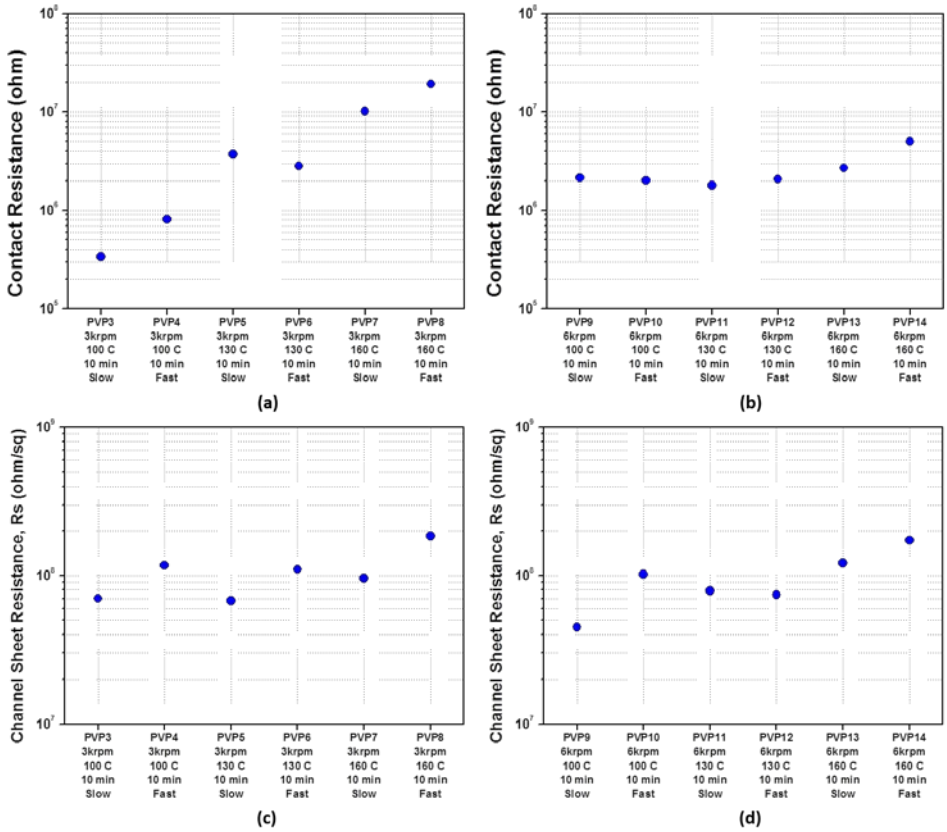


Figure 4.16 Contact resistances for pBTTT TFTs (W=200 μm) of spin-coating speed (a) at 3000 rpm and (b) at 6000 rpm. Channel resistances for pBTTT TFTs of spin-coating speed (c) at 3000 rpm and (d) at 6000 rpm.

4.2.3 Printed pBTTT TFTs

In this section, pBTTT semiconductor will be integrated with gravure printed capacitors to fabricate highly scaled pBTTT TFTs on plastic substrates. While we adopt the optimized conditions for SP210 from the previous section, another formulation of pBTTT which has shorter side chain groups is also introduced in order to increase a chance of having higher mobility. Therefore, the new pBTTT will be called pBTTT(A) and SP210 used in the previous section will be called pBTTT(B) from now on. Post annealing of pBTTT is 10 min at 160°C for pBTTT(A) and 100°C for pBTTT(B) under nitrogen in order to maximize the field-effect mobilities.

pBTTT TFTs were fabricated based on the process in **Figure 4.2**. In order to ensure good device reliability, firstly, a relatively thick dielectric layer (320 nm) was utilized, as previously used in [2]. Transfer and output characteristics of the TFTs are shown in **Figure 4.17**. The pBTTT(A) TFT characterized in **Figure 4.17** has a channel length(L_{ch}) of about 8 μm but has approximately 10 μm S/D overlap($L_{overlap}$), which certainly limits switching speed. As shown in **Figure 4.17,** the device shows good saturation mobility of 0.134 and ON/OFF ratio of above 10^5. However, the device output characteristic, shown in **Figure 4.17(b),** shows significant short-channel-effect (SCE). The saturation region is not clearly

defined even at small gate bias. Near quadratic increase of drain current as drain bias increases was observed when the gate bias is high; it is reported as space-charge-limited current (SCLC).[6]–[8] This clearly attests to the need for proper electrostatic scaling via the use of an appropriately scaled gate dielectric; despite the fact that the device here has the same thickness of dielectric layer as in [2], better gate controllability is clearly required in these aggressively scaled devices to suppress SCE and SCLC. In order to improve the gate controllability, the scaling of the thickness of the dielectric layer is necessary. As expected from the previous section, due to more significant contact resistance in these short channel devices, linear mobility is much lower than saturation mobility as shown below.

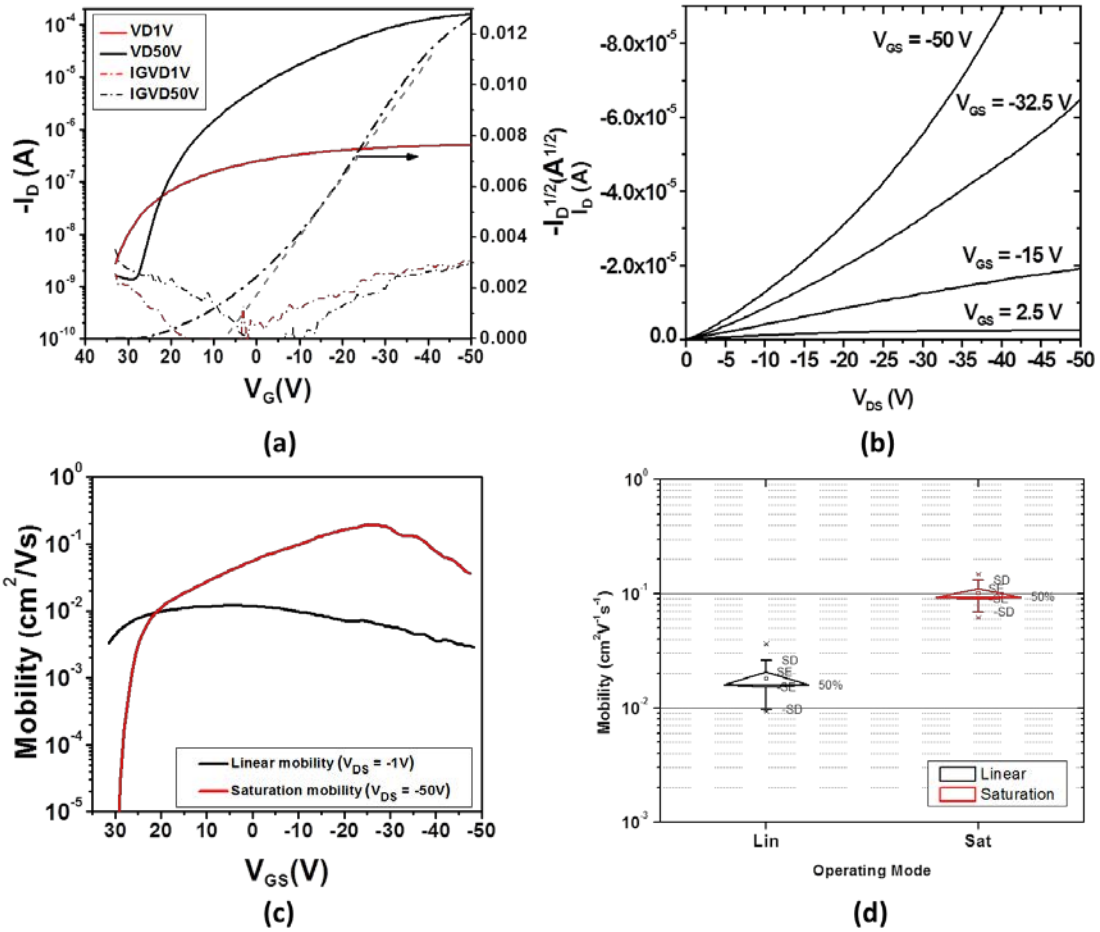


Figure 4.17 (a) Transfer and (b) output characteristics of a gravure printed pBTTT(A) TFT with thick PVP dielectric layer (320 nm). L = 8.3 μm with 10.2 μm of S/D to Gate overlap and W = 428 μm. (see optical micrograph of the TFT in Figure 4.18(a)). (c) Field-dependent mobilities of the pBTTT(A) TFTs. (d) Statistical data of the maximum field effect mobilities.

In order to confirm the benefit of scaling in terms of the speed of TFTs, AC characteristics of the pBTTT(A) TFTs are performed by the measurement of transition frequency (f_T)—the frequency at which an unloaded transistor shows unity current gain. The measurement method was based on the method described in [2]. Its formulation in saturation mode is

$$f_T = \frac{\mu V_{DS,sat}}{2\pi L^2 \alpha \beta} \quad (2)$$

where α is a constant determined by the operating region to represent more accurate input capacitance, and β is a ratio of S/D overlap area to channel ($L_{overlap}/L_{ch}$).

As observed in **Figure 4.18**, the unity gain is obtained around 800 kHz. If the S/D overlap capacitance is optimized even further down to, for example, about 20% of the channel length, then the f_T can be increased beyond 1 MHz. However, due to the significant SCE and SCLC in this device, low output resistance, r_o, could reduce f_{max} significantly. Thus, further effort on better electrostatic scaling is necessary. Lastly, hysteresis in the I-V characteristic of the TFTs is provided in **Figure 4.19**.

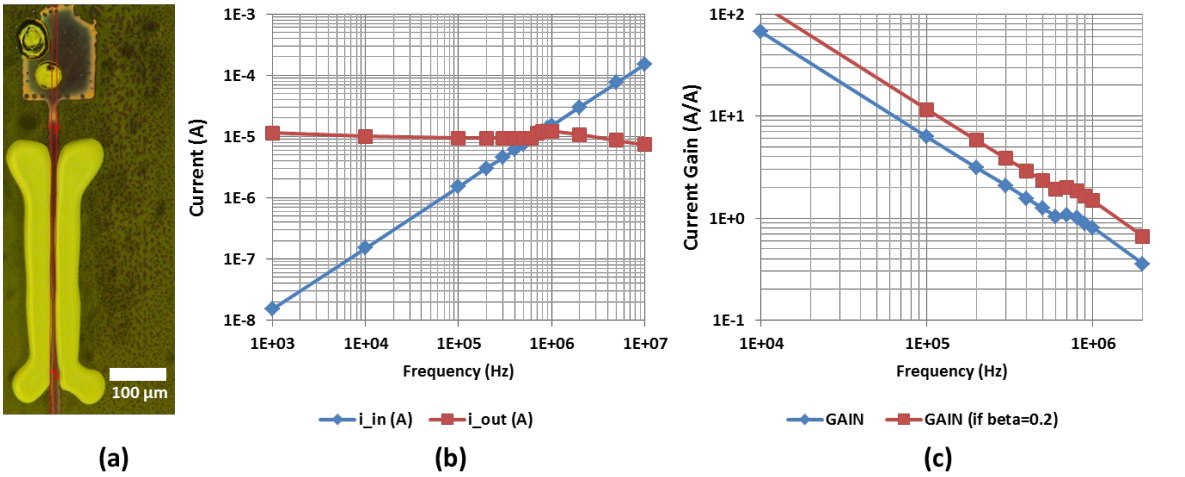


Figure 4.18 (a) Optical micrograph of the highly-scaled pBTTT(A) TFT measured in Figure 4.17. L = 8.3 µm with 10.2 µm of S/D to Gate overlap and W = 428 µm. (b) Input and output current, and (c) current gain during the f_T measurement of the pBTTT(A) TFT in (a).

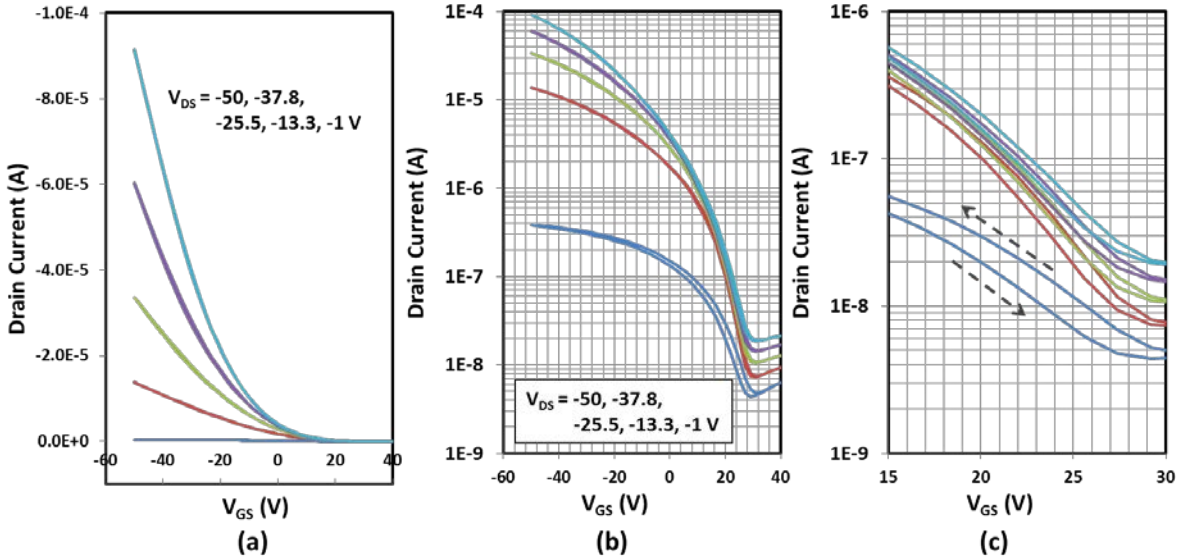


Figure 4.19 Hysteresis in the transfer characteristic of the pBTTT(A) TFTs of Figure 4.18 in (a) linear scale (b) semi-log scale (c) sub-threshold region in the semi-log scale.

Transfer and output characteristics of two pBTTT(A and B) TFTs with thinner dielectric layers are shown in **Figure 4.20** and **Figure 4.21**. The thickness of PVP film is reduced to 160 nm as studied in Capacitors. The pBTTT(A) device in **Figure 4.20** has a channel length of 10 μm with less than 2 μm of S/D overlap, showing excellent performance of the overall gravure printing process. Device parameters and statistics of the two groups of pBTTT TFTs are given in **Table 4.2** and **Table 4.3**. pBTTT(A) TFT has better ON characteristics, having saturation mobility of about 0.1 $cm^2V^{-1}s^{-1}$ and thus higher ON current. pBTTT(B) TFT has better OFF characteristics. The device is almost completely off at zero gate bias and shows better subthreshold swing (SS) of less than 2 V/dec. Compared to the TFTs with thick dielectric, these properly scaled TFTs have a reduced operating voltages of -25 V and significantly suppressed SCE and SCLC. The pBTTT(A) TFT in this work has ten times higher mobility and two times smaller channel length than our previous work [2] while its operating voltage has also been reduced significantly.

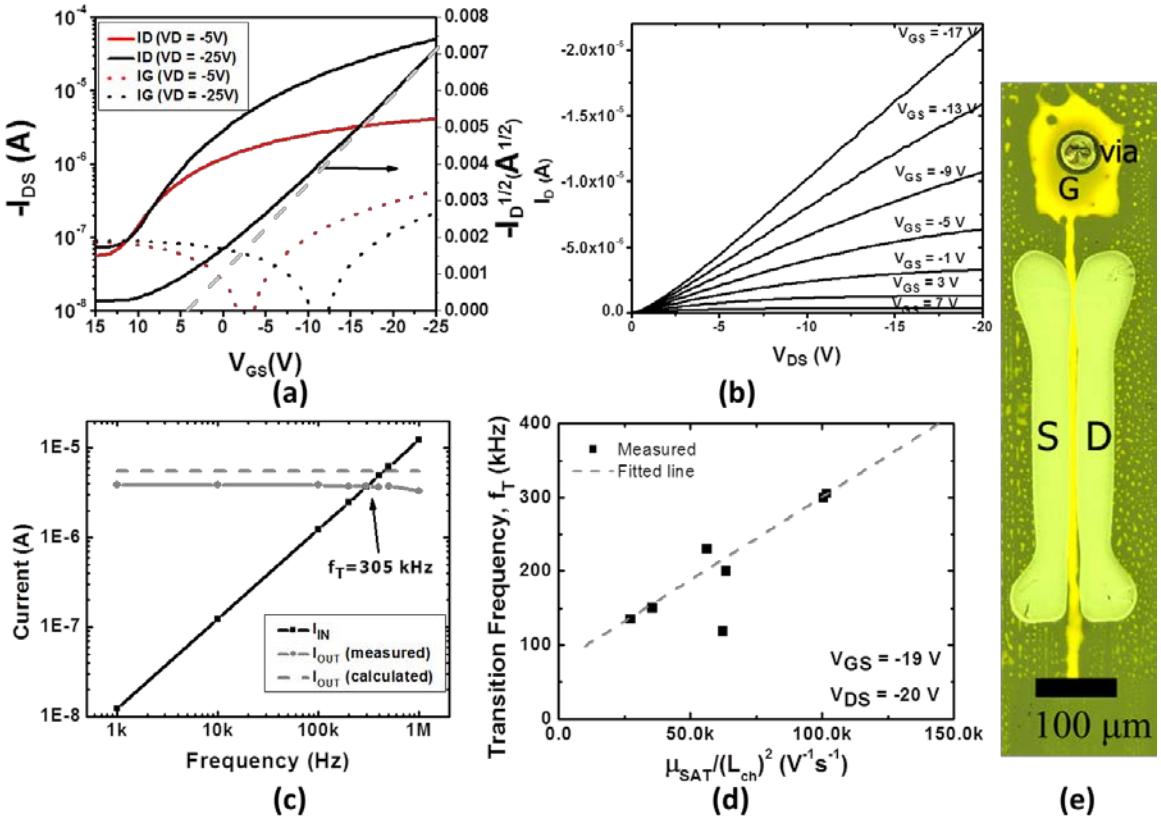


Figure 4.20 (a) Transfer and (b) output characteristics of a representative highly-scaled μGravure-printed TFT with μ_{LIN}= 0.025 $cm^2V^{-1}s^{-1}$, μ_{SAT}: 0.105 $cm^2V^{-1}s^{-1}$ (c) AC characteristics of the representative TFT. Grey dashed line indicates theoretically calculated output current based on measured transconductance (g_m), load resistance, and input signal, showing good agreement with the experimentally observed data. (grey solid line) (d) The trend of fT with respect to mobility/(channel length)^2. As theoretically expected, f_T is linearly proportional to mobility/(channel length)^2. One significant deviation is due to significant overlapping area from a wide gate line (23 μm), resulting in increased parasitic capacitance. (e) Optical micrograph of the representative pBTTT TFT (W = 416 μm, $L_{channel}$ = 10 μm with minimal gate overlap)

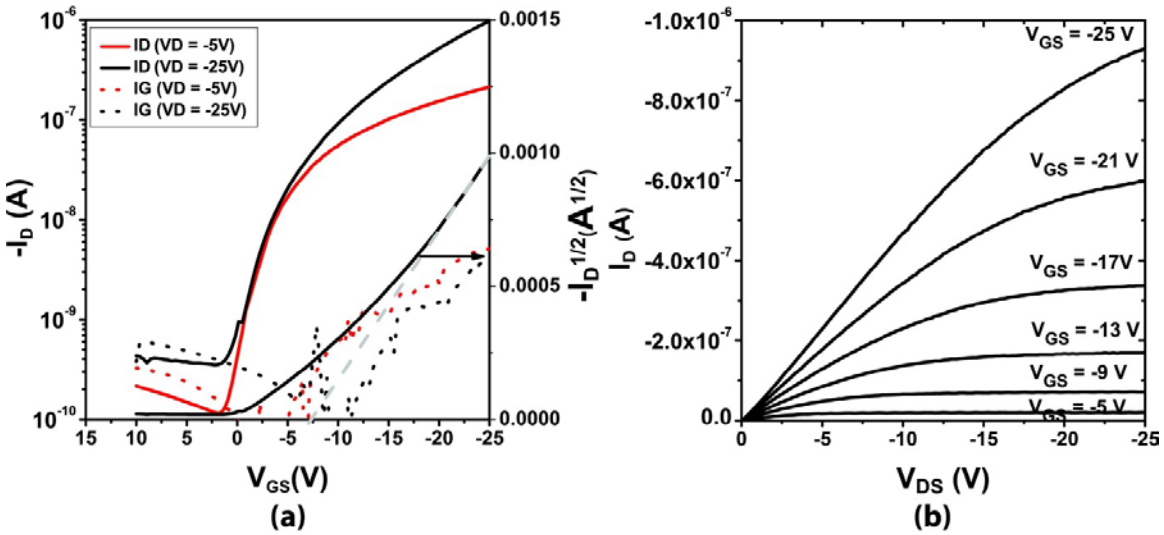


Figure 4.21 (a) Transfer and (b) output characteristics of a representative gravure printed pBTTT(B) TFT. L = 18 μm, W = 422 μm.

Parameters	pBTTT A	pBTTT B
μ_{LIN} [$cm^2V^{-1}s^{-1}$]	$2.50x10^{-2}$	$3.88x10^{-3}$
μ_{SAT} [$cm^2V^{-1}s^{-1}$]	0.105	$1.15x10^{-2}$
ON/OFF [A/A]	$7.16x10^{2}$	$5.03x10^{3}$
SS_{SAT} [V/dec]	5.84	1.89
V_T [V]	5	-7

Table 4.2 Device parameters of the representative pBTTT (A) and (B) based gravure-printed TFTs shown in Figure 4.20 and 4.21, respectively.

Parameters	pBTTT A	pBTTT B
μ_{LIN} [$cm^2V^{-1}s^{-1}$]	$(3.19 \pm 0.21)x10^{-2}$	$(2.98 \pm 0.94)x10^{-3}$
μ_{SAT} [$cm^2V^{-1}s^{-1}$]	$(7.35 \pm 0.90)x10^{-2}$	$(5.90 \pm 1.43)x10^{-3}$
ON/OFF [A/A]	$(6.96 \pm 1.05)x10^{2}$	$(4.25 \pm 1.59)x10^{3}$
SS_{SAT} [V/dec]	5.48 ± 0.22	2.37 ± 0.12

Table 4.3 Statistics of device parameters for both pBTTT (A) and (B) based gravure-printed TFTs. The device A showed about 10 times higher mobility, but the device B showed higher ON/OFF ratio and smaller subthreshold swing.

The transition frequency (f_T) of the higher performance pBTTT(A) TFTs was measured in a similar way. Instead of using a low input capacitance operational amplifier to measure the output signal,[2] a high impedance active probe, Picoprobe Model 18C with 20 fF input capacitance by GGB Industries Inc., was used to minimize coupling. This was necessary due to the dramatic improvement in device performance relative to our previous work, and indeed, relative to all other reported gravure printed devices. As shown in **Figure 4.20(c)**, the transition frequency when a pBTTT(A) TFT was biased at V_{GS} = -19V and V_{DS} = -20V

was measured to be 305 kHz which is by far the highest switching speed reported to date for any roll-printed process (see Chapter 1). Though this is lower than that of the thicker PVP device in **Figure 4.18**, it is more practically useful due to lower operating voltage and higher output resistance. The theoretical f_T calculated based on the extracted trans-conductance (g_m) from I-V, input small signal and load resistance is also plotted in **Figure 4.20(c)** and shows good agreement with the measured value. The measured f_T of TFTs with various channel lengths and μ_{SAT} values are plotted in **Figure 4.20(d)**. f_T is linearly proportional to the parameter, $\mu_{SAT}*L^{-2}$, which is in agreement with expectations shown in Equation (2). Some deviations result from the source/drain overlap parasitic capacitance, which increases β in (2).

The highly scaled gravure-printed pBTTT TFTs showed significant improvement from previously reported roll-to-roll printed devices mentioned in Chapter 1. In addition to the optimized mobility up to 0.1 $cm^2V^{-1}s^{-1}$ in saturation, channel length scaling down to 10 μm with minimized parasitic capacitance is proved to be very important. However, it still left room for more improvement. Firstly, further channel length reduction is possible by adopting more highly scaled silver lines provided in Chapter 3. Secondly, field-effect mobility can be further improved. Various organic semiconductors showing higher mobility than pBTTT have been recently developed.[9]–[12] Thus, those higher performance semiconductors must be integrated with our gravure-printed process. Lastly, more optimization of the device parameters such as output resistance and contact resistance is needed. Those improvements will be discussed in the following section.

4.3 S1200 TFTs (L_{ch}=5 μm)

While the polymer based organic semiconductors such as pBTTT provide good solubility, easier printability, and thus less variation in characteristics, overall performance is poorer than small molecule based organic semiconductors.[13], [14] In order to utilize all the benefits from both types of the organic semiconductors, EMD Chemicals have recently developed a new semiconductor series, Lisicon S1200, which provides higher mobility than their polymer group, SP family including SP210, while maintaining good printability not only for inkjet, but also for various roll-to-roll printing.[12] S1200 has been designed for both bottom-gate and top-gate structures with matching dielectric materials. In this section, bottom-gate S1200 TFT material set will be applied to the highly scaled gravure-printed lines.

4.3.1 D207 Capacitors

S1200 is designed to be used with a matched gate dielectric, D207. This gate dielectric material and its fabrication process are investigated first. As a matching dielectric material for a bottom-gate TFT process, 2-Heptanone (also called, methyl amyl ketone, MAK) based UV cross-linkable polymer dielectric material, D207, is provided by EMD Chemicals. As-received 18wt% D207 ink is appropriately diluted by additional MAK solvent in order to obtain the desired film thickness. D207 ink is easily gravure-printed on UV/Ozone surface-treated PEN substrates (up to 10 min). As shown in **Figure 4.22(a)**, gravure-printed NPS silver line is used as a bottom electrode for D207 capacitors. The D207 film is cross-linked by UV light (365nm, 3 J/cm^2 intensity, supplied by Spectroline SB-100P). A CCI-300 silver top electrode is inkjet-printed on D207 after 2-minute UV/Ozone treatment in order to ensure good wettability. The dielectric constant of D207 is measured to be 2.9. 18wt% D207 is diluted with a volume ratio of 1:1. Then, it is gravure-printed with a commercial gravure roll, IGT 402.150.43 (stylus angle 120°, cell depth: 50 μm, and areal volume: 13.5 ml/m^2) followed by solvent drying at 120°C for 2 min. The printed D207 film has an average film thickness of 288 nm.

Compared to the PVP dielectric layer used in the previous section, D207 showed much more improved insulation characteristics. Rarely did hard breakdown happen even up to 100 V (≈3.5 MV/cm). Breakdown field defined as the electric field at which the current density is 1 μA/cm^2 is beyond 3 MV/cm as shown in **Figure 4.22** (50% improvement from the PVP capacitors). Scalability of the D207 film thickness is also explored in **Figure 4.23**. Changing the dilution ratio of the ink varies film thickness linearly. The good insulation characteristic was well maintained down to 150 nm thick films although yield becomes worse.

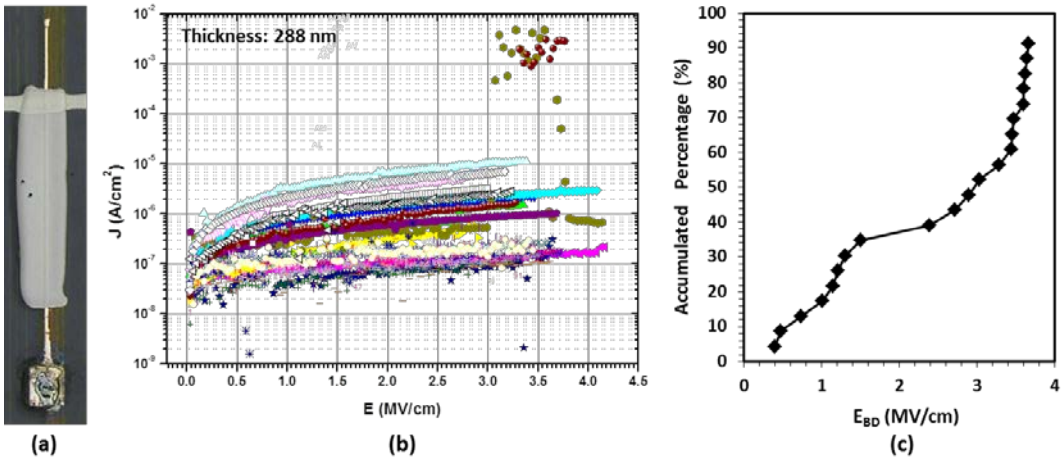


Figure 4.22 Insulation characteristics of gravure-printed D207 capacitors (288 nm thick): (a) current density – electric field plot, (b) failure statistics of the breakdown field. The breakdown field is defined as the electric field at which the current density is 10^{-6} A/cm^2.

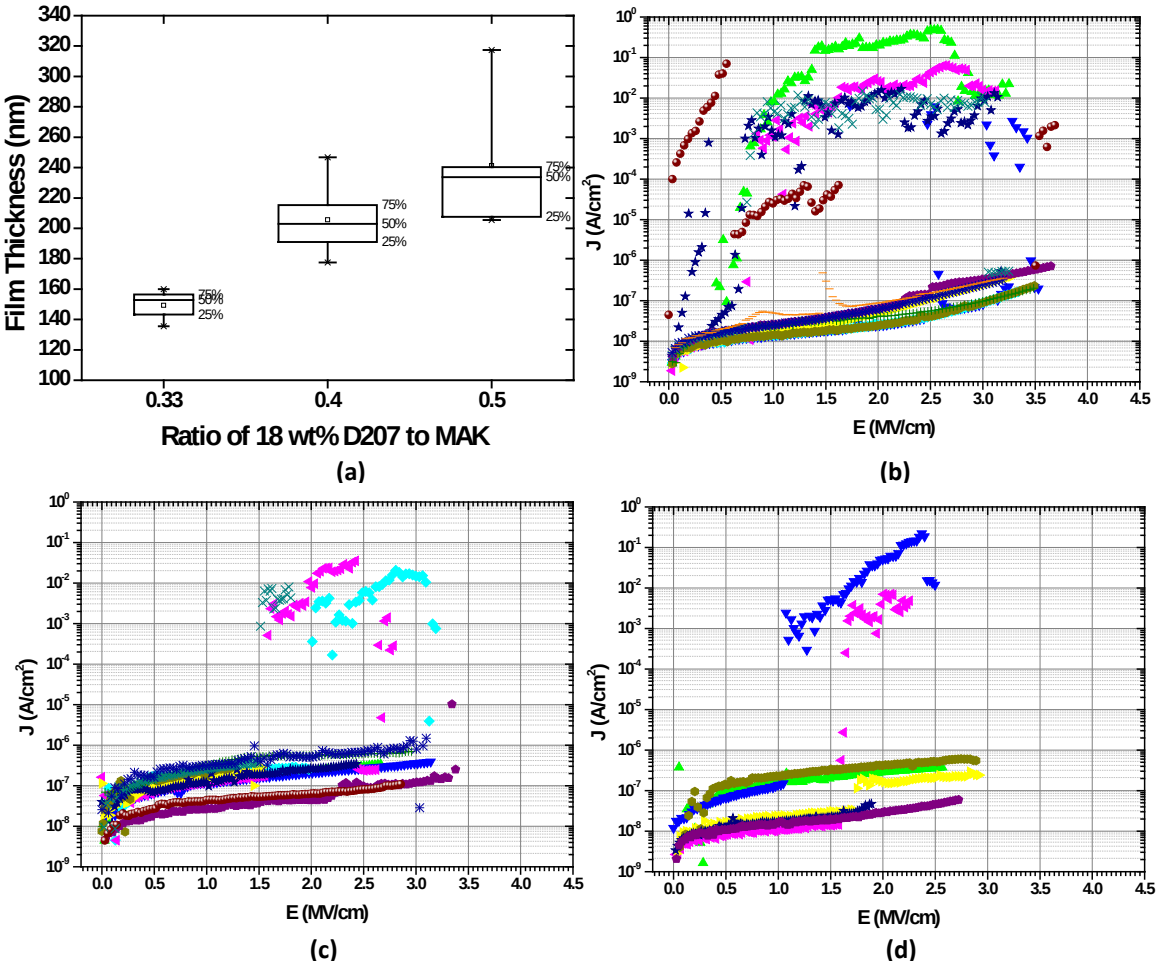


Figure 4.23 Scaling of the gravure-printed D207 film thickness. (a) film thickness is varied by different dilution ratio of D207 ink ratio: (b) 0.33, (c) 0.4 and (d) 0.5.

While in practice it is desired to pattern D207 to only insulate the device area, blanket-coated D207 film is gravure-printed for experimental convenience. The use of a blanket dielectric necessitates the creation of a via to make contact to the gate. In order to easily probe the gate electrodes under the D207 layer and form interconnects through the D207, the via is formed by inkjet printing. Propylene glycol monomethyl ether acetate (PGMEA) is inkjet-printed using a Dimatix inkjet printer in order to etch the D207 film before it is UV cross-linked. PGMEA generally exhibits good inkjet printability except for its relatively low viscosity (0.8 cP). Other parameters are suitable for inkjetting: surface tension of 26.9 dynes/cm; slow evaporation rate of 0.33; and relatively high boiling point of 146°C. On a Dimatix inkjet printer with a 10 pL cartridge, it is found that the pure PGMEA ink can be jetted, but single drop jetting cannot be obtained. Due to the low viscosity, the tail of the jetted droplet is separated from the main droplet during flight. However, since the two drops land on the same spot, it is usable for etching of the D207 in this work. In **Figure 4.24**, the profile of etched via holes with varying number of droplets is provided. Etch rate is about 88 nm per drop when a 10 pL nozzle is used. Thus, it is necessary to print multiple droplets to fully form a via hole through the gravure-printed D207 films.

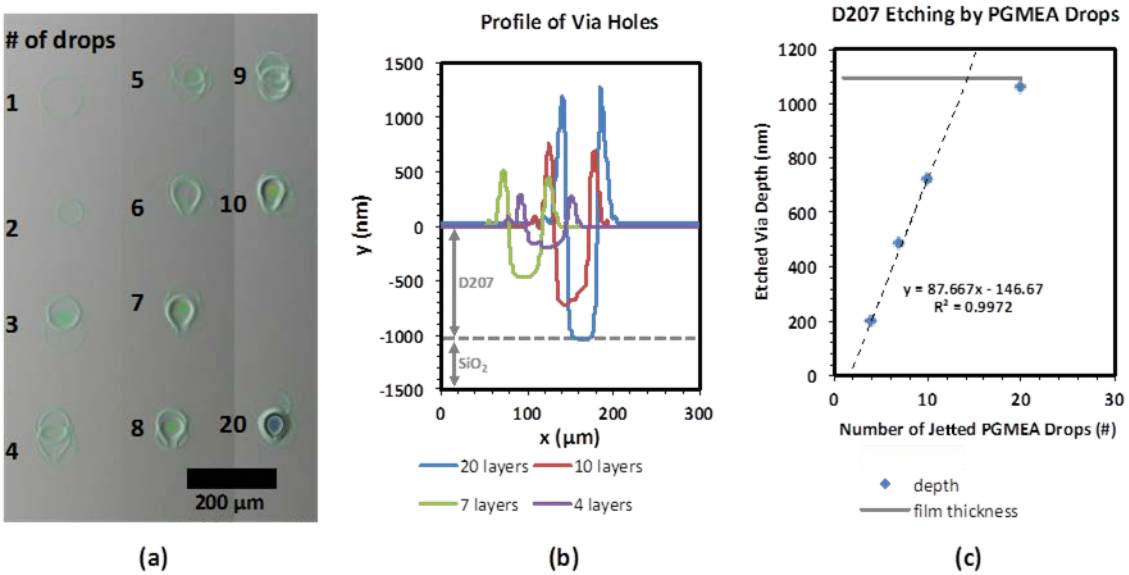


Figure 4.24 (a) Optical micrographs of D207 (≈1.1µm thick) with inkjet printed PGMEA droplets. 20-droplet case shows blue region in the middle, which is the color of oxidized silicon wafer under the D207 film. (b) Profile of printed via holes (c) Etched via depth as a function of the number of jetted PGMEA droplets.

4.3.2 S1200

Due to the wide bandgap with low HOMO level of the organic semiconductor, in general, gold S/D contacts are ideal for better carrier injection. However, the high cost of gold is not feasible for mass production particularly in low-cost electronics applications as discussed in Chapter 1. Therefore, EMD Chemicals also developed surface treatment materials for various types of alternative S/D contacts such as ITO, silver, and copper in order to provide low contact barriers. Lisicon M001 is designed for silver electrodes. In this

section, our efforts on the optimization of the short channel S1200 TFTs including the reduction of S/D contact barriers are presented.

4.3.2.1 Effect of S/D work function

Firstly, M001 treatment was tested with evaporated silver S/D electrodes as shown in **Figure 4.25**. These serve as reference devices for our printed TFTs. A heavily-doped silicon wafer is used as a back-gate. 310 nm thick D207 (ε_r=2.9) is spin-coated on 100 nm thick SiO_2 to maintain the same gate dielectric/semiconductor interface. Effective D207 thickness overall is therefore 385 nm. S/D silver electrodes are evaporated through a shadow mask. M001 is applied to the silver electrodes immediately after the S/D evaporation. M001 solution totally wets D207. Thus, a small volume of M001 dropped on D207 completely wets both silver electrodes and D207 surface. After 1 min of the application, M001 is spun-dried at 1000 rpm for 30 sec, followed by a rinse with isopropyl alcohol for at least 30 seconds. After the IPA rinse, the sample is spun-dried again at 1000 rpm for 30 sec. As-received S1200 is spin-coated at 4000 rpm (with 500 rpm/s) for 30 sec. After the deposition of S1200, the sample is dried at 100°C for 1 min. During the drying, crystallization of the S1200 film is observed. Fully fabricated TFTs are shown below. Measured electrical characteristics of the TFTs are on par with the data provided by EMD Chemicals and ref. [12]: both linear and saturation mobilities are around 1 cm^2/Vs; high on/off ratio (>10^6); and small subthreshold swing (SS) (<600 mV/dec).

While M001 is proven to be effective on evaporated silver, the effectiveness on printed silver electrodes must be confirmed since the printed silver electrodes are still not as pure as evaporated silver due to residual ligands. To clean these off, we use a weak RF forming gas plasma. The change of work function is measured by Kelvin probe force microscopy (KPFM) for our two different nanoparticle silver inks, CCI-300 and NPS. As shown in **Table 4.4**, regardless of the type of inks and sintering condition, the final work function of M001 treated electrodes with RF plasma in 4.5% forming gas is shifted to ~5.4 eV.

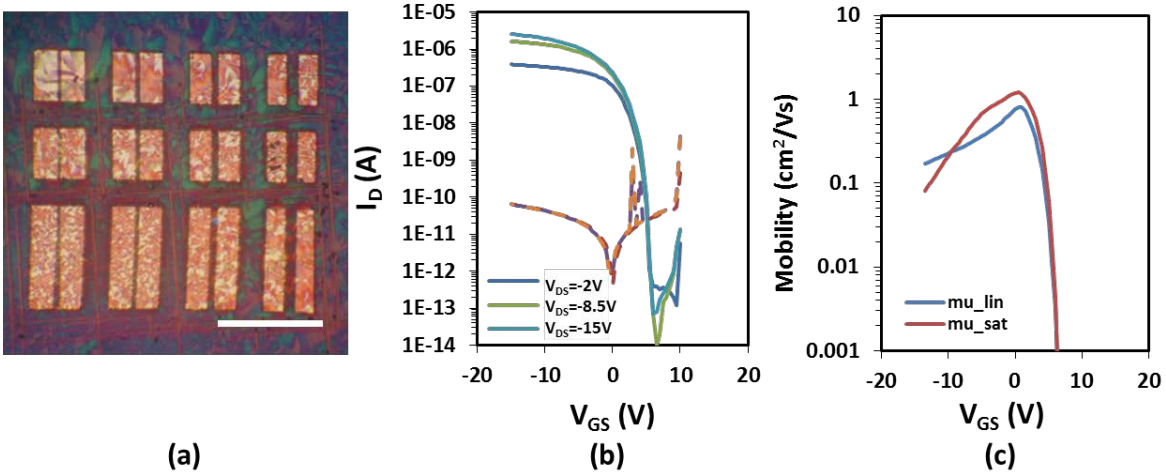


Figure 4.25 (a) Optical micrograph of S1200 TFTs with evaporated S/D silver electrodes. Scale bar represents 400 µm. (b) Transfer characteristic and (c) mobilities of a TFT in (a). (W: 400 µm, L: 100 µm).

S/D silver ink	Sintering Condition	Work function (eV)		
		As sintered	After RF plasma 4.5% H_2/N_2, 40W, 30s	After M001 treatment
CCI-300	at 120°C for 20 min	4.34	4.87	5.42
CCI-300	at 150°C for 30 min	4.38	5.02	5.40
NPS	at 140°C for 2 hour	4.47	4.52	5.36
NPS	at 250°C for 30 min	4.71	5.02	5.49

Table 4.4 The effect of RF plasma and M001 on the work function change of printed silver electrodes of different ink and sintering condition. 1cm×1cm electrodes are prepared on glass (by inkjet for CCI-300, and by spin-coating for NPS).

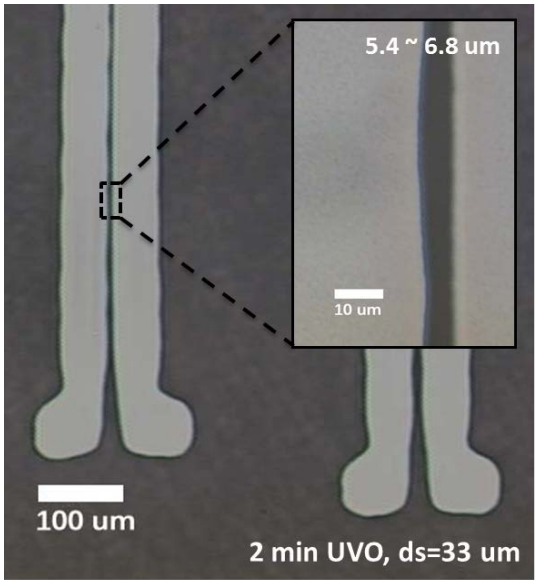


Figure 4.26 Inkjet printed S/D electrodes on UV cross-linked D207 film. 2-minute UV/Ozone treatment is done before printing. Drop spacing for the printed lines is 33 µm with 10 pL droplets. Guide droplets are pre-printed to prevent lines from being merged.

To further confirm that the S/D treatment by M001 delivers good characteristics for S1200 TFTs with inkjet printed silver electrodes, S1200 TFTs were fabricated on silicon back-gates by replacing the evaporated silver electrodes of the TFTs in **Figure 4.25** with inkjet-printed CCI-300 lines (sintered at 150°C for 30 min). Inkjet printing of CCI-300 S/D on D207 is optimized to provide channel length down to 5 µm as shown in the optical micrograph above.

Transfer characteristic and mobilities of the TFTs are provided in **Figure 4.27**. 4 different S/D treatments were conducted: (a) no RF plasma, (b) RF plasma in only N_2, (c) in 5% forming gas, and (d) in 10% forming gas. Without RF plasma treatment, the TFTs did not work well, showing lower mobilities and poorer off characteristics. Although the different RF plasma chamber gas formulations did not cause significant difference, 5% H_2/N_2 condition gave the best performance. Mobility was the highest while having good off

characteristics (low SS and fully off around zero bias). The benefits of the plasma cleaning prior to M001 deposition are clear.

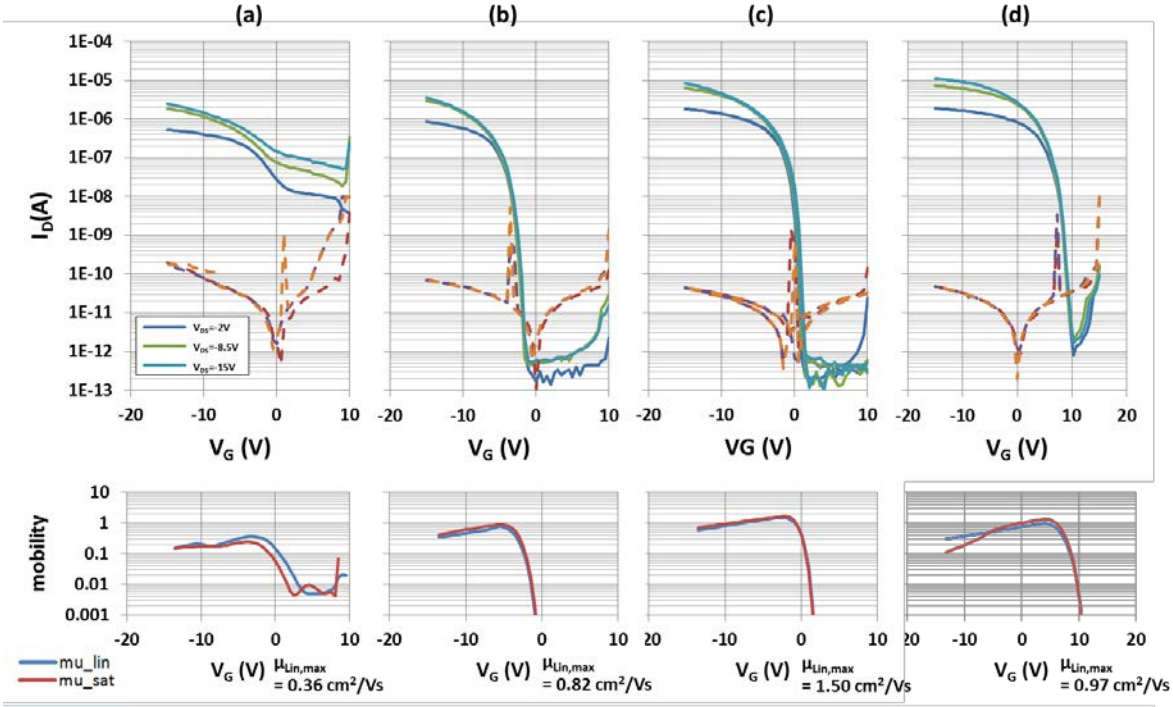


Figure 4.27 The effect of plasma on the characteristics of S1200 TFTs with inkjet-printed CCI-300 S/D electrodes. (W=1 mm, L_{ch}=94μm) (a) No plasma treatment, (b) 40 sccm N_2 only (c) 5% forming gas (H_2/N_2=5/100 sccm) (note the double sweep in transfer characteristics) (d) 10% forming gas (H_2/N_2=10/100 sccm). Linear region is when V_{DS} is -2 V, and saturation region is when V_{DS} is -15V.

S1200 TFTs also showed more advantages over pBTTT TFTs. With the optimized S/D contacts, measured mobilities in linear and saturation regions are almost identical whereas the linear mobility—which has more physical meaning—of pBTTT TFTs was about an order of magnitude lower than saturation mobility. It is also important to note that the operation voltage is much smaller than that of the pBTTT TFTs, even though the gate capacitance is much lower due to lower dielectric constant and thicker film than the PVP capacitors in pBTTT TFTs. Good qualities of the semi/dielectric interface and semiconductor itself lead to more efficient carrier accumulation. Therefore, for the same amount of accumulation carrier concentration, the required voltage is lower in the case of S1200 on D207.

4.3.2.2 Optimization for short channel TFTs

The optimized S/D treatment is applied to TFTs with various channel lengths even below 10 μm. **Figure 4.28** shows channel length dependence of the transfer characteristic of the S1200 TFTs. As seen from the plot, short channel devices below 20 μm or so show degradation in off-state characteristics. SS starts increasing as the channel length decreases

below 30 μm, and the transistors eventually do not turn off properly. Extracted device parameters are given in **Table 4.5**. As shown from the output characteristics of the TFTs in **Figure 4.29**, the drain current does not saturate in short channel TFTs. The shortest channel TFT does not show significantly different contact resistance from that of long channel devices. It also does not show SCLC behavior as was observed from the pBTTT TFTs in **Figure 4.17**. Therefore, the poor off characteristics and low output resistance might be the indication of an additional conduction path that is not controlled by gate bias. Since the semiconductor film was spin-coated over the inkjet-printed S/D lines, the S1200 film thickness will be nonplanar.[15], [16] The film thickness in the channel could be affected more when the channel length is smaller due to the film coverage over the profile of the printed S/D lines. If the film is thicker than what gate field can control, then the conduction path that is far from the channel is always on, leading to lower output resistance. Therefore, S1200 film thickness needs more optimization.

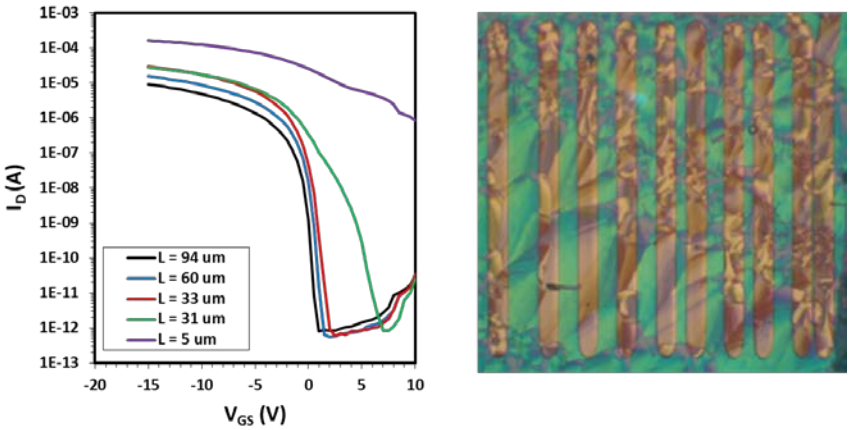


Figure 4.28 (a) Transfer characteristics of S1200 TFTs with different channel lengths. (b) Optical micrograph of 5 TFTs measured in (a). Width of the transistors is 1 mm.

L (μm)	94	60	33	31	5
W (μm)	1000	1000	1000	1000	1000
ON/OFF (lin) (A/A)	6.16E+06	1.37E+07	2.55E+07	3.29E+07	5.34E+02
ON/OFF (sat) (A/A)	1.12E+07	2.77E+07	5.01E+07	3.29E+07	1.98E+02
μ_{lin} (cm^2/Vs)	1.50	1.62	1.63	1.46	1.08
μ_{sat} (cm^2/Vs)	1.61	1.86	2.01	1.66	0.84
SS_{lin} (V/dec)	0.36	0.36	0.39	0.60	3.46
SS_{sat} (V/dec)	0.39	0.38	0.42	0.75	3.97
V_{on} (V)	1	2	2.5	7.5	10

Table 4.5 Extracted device parameters of the S1200 TFTs in Figure 4.28.

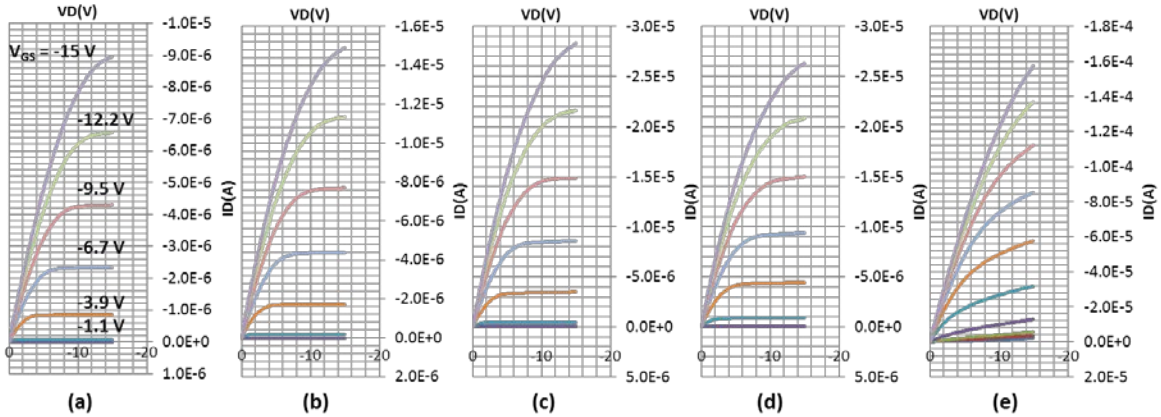
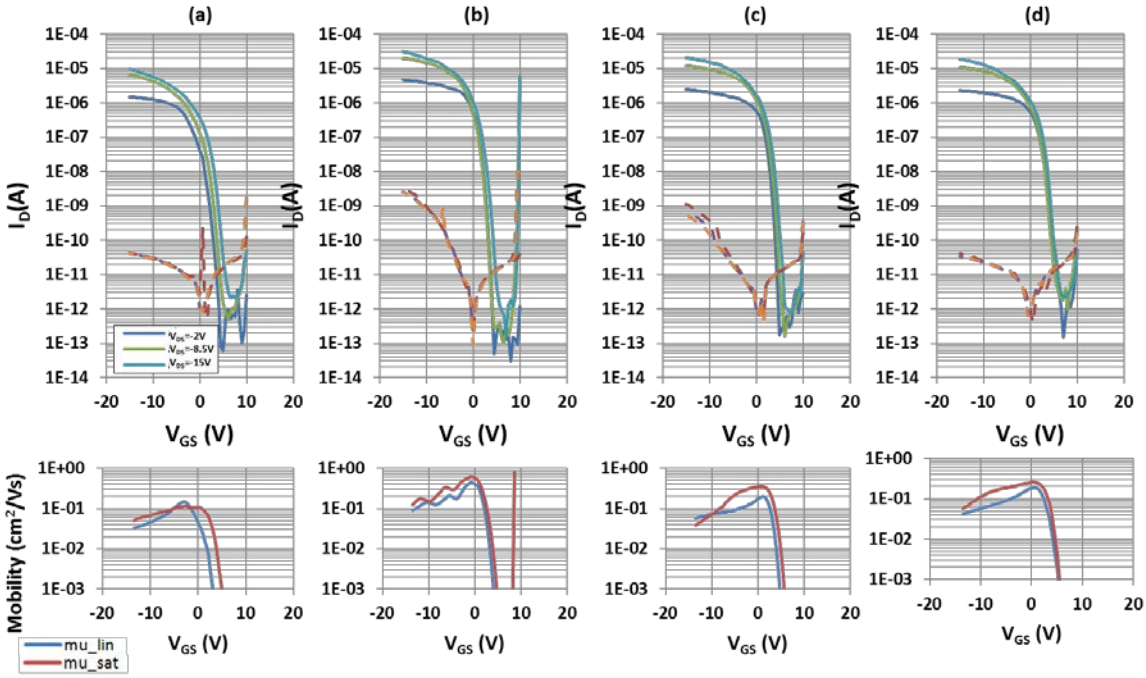


Figure 4.29 Output characteristics of S1200 TFTs with various channel lengths in Figure 4.28. (a) L_{ch}=94 µm, (b) 60 µm, (c) 33 µm, (d) 31 µm, and (e) 5 µm.

While keeping all the other process steps the same, the spin-coating condition for the S1200 film was varied. Since both spin speed (rpm) and spin acceleration (rpm/s) affect the final spin-coated film thickness, both parameters are chosen to be more intense than the previous condition (4000 rpm with 500 rpm/s acceleration). Therefore, the resultant S1200 film thickness is varied from 50 nm down to about 26 nm. After the film thickness is reduced, the TFTs in short channels (below 10 µm) are able to turn off as shown in **Figure 4.30** and **Figure 4.31**. Statistical data of the extracted device parameters are plotted in **Figure 4.32** (long channels: L_{ch} > 60 µm) and **Figure 4.33** (short channels: $L_{ch} \leq$ 10 µm). For long channel TFTs, it is clear that the thinnest S1200 film (6 krpm with 6 krpm/s) gave the best performance: higher mobility, larger on/off ratio, and smaller SS. While the effect of the film thickness is not that significant in short channel TFTs, the fastest spin-speed and acceleration still deliver better overall performance. Therefore, for the highly scaled gravure-printed TFTs, this spin-coating condition will be used to ensure good operation of the transistors.

However, one thing to mention here is that the mobility is dropped in short channel TFTs (median is around 0.25 cm^2/Vs) possibly due to a larger S/D contact factor. It could set the maximum mobility that can be achieved in gravure-printed TFTs unless the fabrication process is optimized further. More study on how the mobility can be improved will be discussed in later. Lastly, in order to see the variability of the material system, the results of 59 TFTs characterized in **Figure 4.32** and **Figure 4.33** are plotted in **Figure 4.34**. Though variation between S1200 recipes is observed, overall device variation was reasonably good.



Sample #	(a)	(b)	(c)	(d)
S1200	4000 rpm, 1000 rpm/s	4000 rpm, 4000 rpm/s	6000 rpm, 1000 rpm/s	6000 rpm, 6000 rpm/s

Figure 4.30 Transfer characteristics of representative S1200 TFTs ($L_{ch} \leq 10$ µm) with different S1200 film spin-coating conditions.

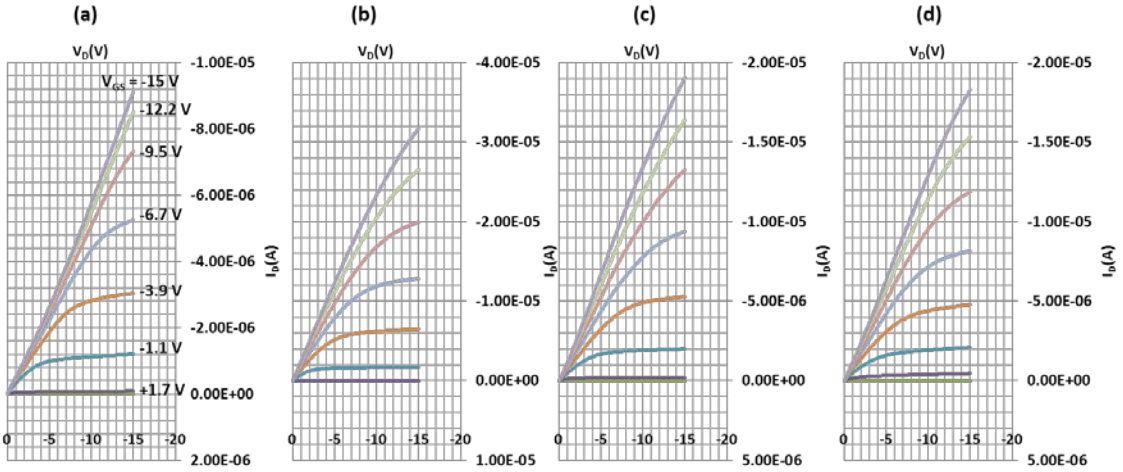


Figure #	(a)	(b)	(c)	(d)
S1200	4000 rpm, 1000 rpm/s	4000 rpm, 4000 rpm/s	6000 rpm, 1000 rpm/s	6000 rpm, 6000 rpm/s

Figure 4.31 Output characteristics of representative S1200 TFTs ($L_{ch} \leq 10$ µm) with different S1200 film spin-coating conditions.

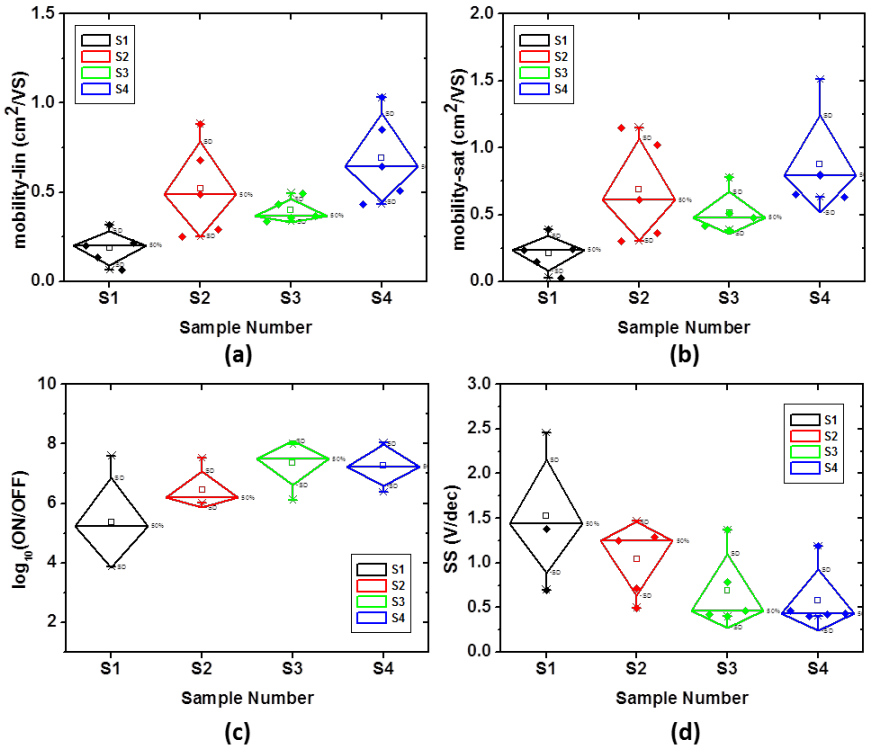


Figure 4.32 Box plot of extracted device parameters of long channel (L_{ch} > 60 µm) S1200 TFTs with different spin-coating condition. S1: 4 krpm, 1 krpm/s, S2: 4 krpm, 4 krpm/s, S3: 6 krpm, 1 krpm/s, and S4: 6 krpm, 6 krpm/s.

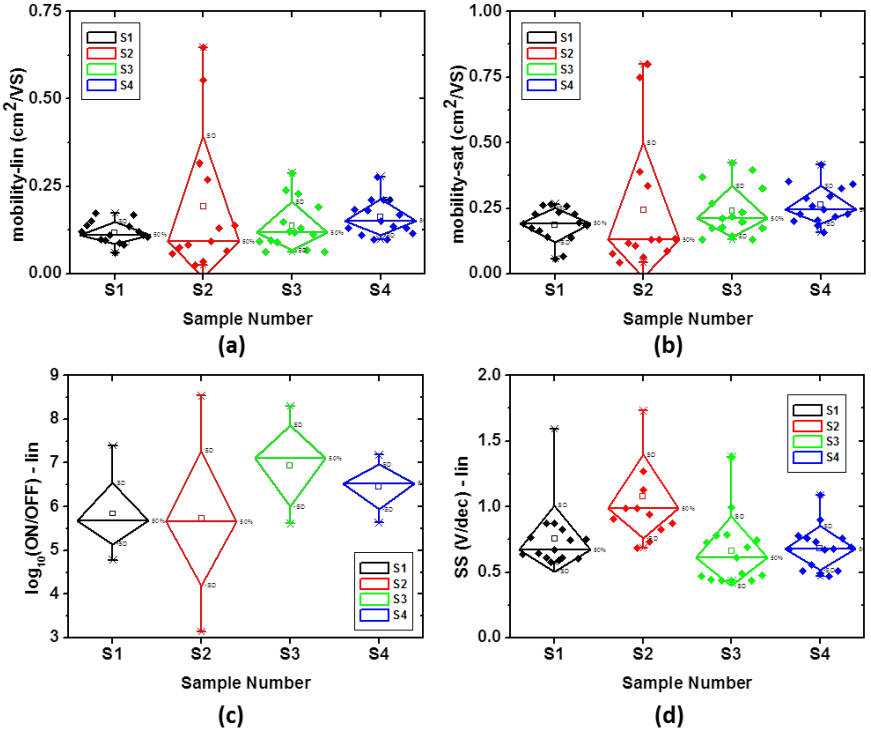


Figure 4.33 Box plot of extracted device parameters of short channel ($L_{ch} \leq 10$ µm) S1200 TFTs with different spin-coating condition. S1: 4 krpm, 1 krpm/s, S2: 4 krpm, 4 krpm/s, S3: 6 krpm, 1 krpm/s, and S4: 6 krpm, 6 krpm/s.

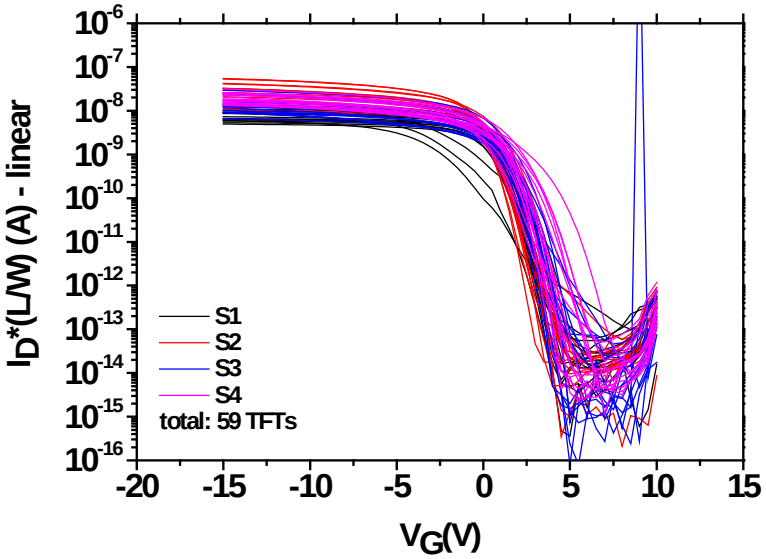


Figure 4.34 59 TFTs characterized in Figure 4.32 and 4.33 are presented here with normalized drain current in order to show the variation in this process. Different colors represent different spin-coating conditions explained in Figure 4.32.

4.3.3 DC characteristics of S1200 TFTs

By combining the gravure-printed D207 capacitor with optimized silver S/D and S1200 in the previous sections, highly scaled gravure-printed S1200 TFTs are fabricated on PEN substrates. The overall process flow for the bottom-gate S1200 TFTs is again identical to the description in **Figure 4.2**. The detail process steps are explained in the figure below along with an optical micrograph of an exemplar printed TFT.

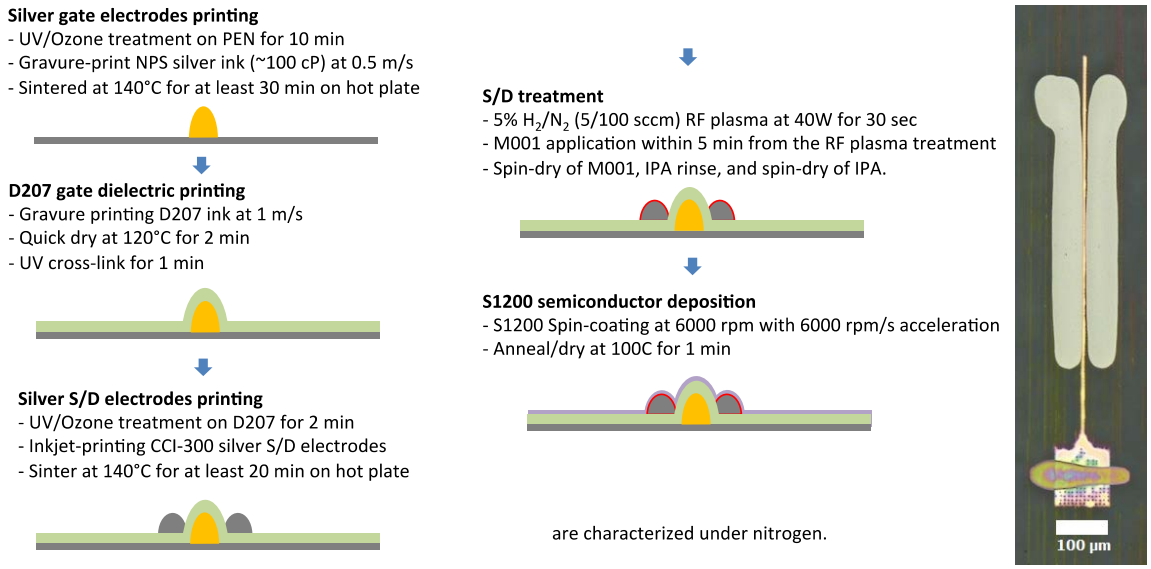


Figure 4.35 Basic fabrication flow of the gravure-printed highly scaled S1200 TFTs in detail. The optical micrograph is a fabricated TFTs without S1200 layer (L_{gate}=7.5 µm, L_{ch}=5.0 µm, and W=500 µm).

The initial TFTs on PEN based on the process above had severe device-to-device variation as shown in **Figure 4.36**. This could be due to a number of factors, including substrate non-uniformities, printing-induced non-uniformities, and non-uniform heating due to the plastic substrate. It is important to note that the initial process transfer to PEN substrate was very promising. One of the best TFTs in the sample showed overall much better characteristics than pBTTT TFTs. (See **Figure 4.37** and **Table 4.6**). The TFT showed mobility maximized at 0.22 cm^2/Vs that is similar to the average mobility shown in **Figure 4.33** with good on/off ratio (>10^6) and small SS (< 1V/dec). While the operating voltage is only up to 15V, calculated transition frequency (f_T)—based on the extracted transconductance (g_m) of 1.5×10^{-6}(A/V) and calculated other parameters including overlap capacitance from geometry—is 1.07 MHz. Increased field-effect mobility and further scaling of channel length down to 5 µm facilitate the increase of transition frequency into the MHz range.

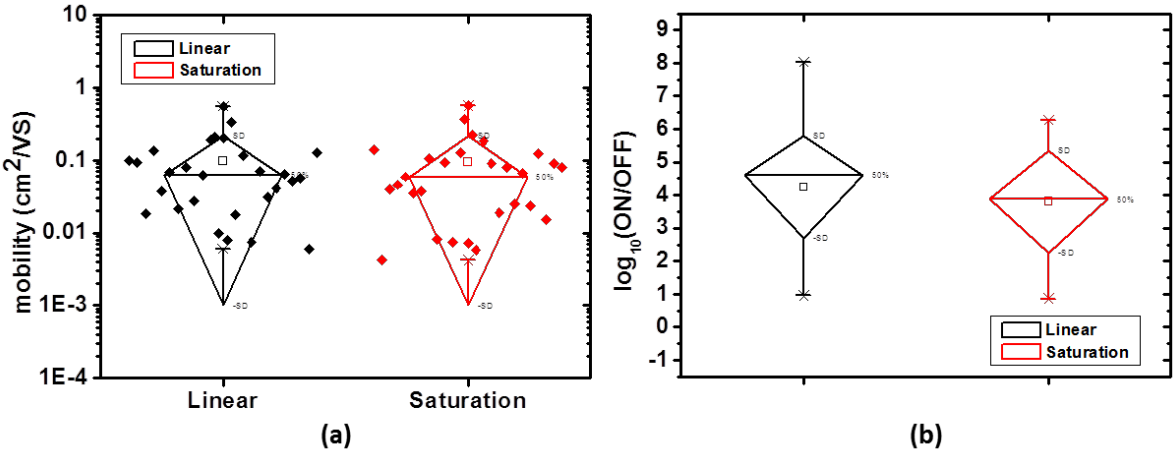


Figure 4.36 Box plot of extracted device parameters of gravure-printed S1200 TFTs fabricated based on the process in Figure 4.35. S1200 film is dried and annealed at 100°C by placing PEN substrate directly onto hotplate. Median thickness of gravure printed D207 film is 336 nm. Channel lengths are from 5 to 15 µm.

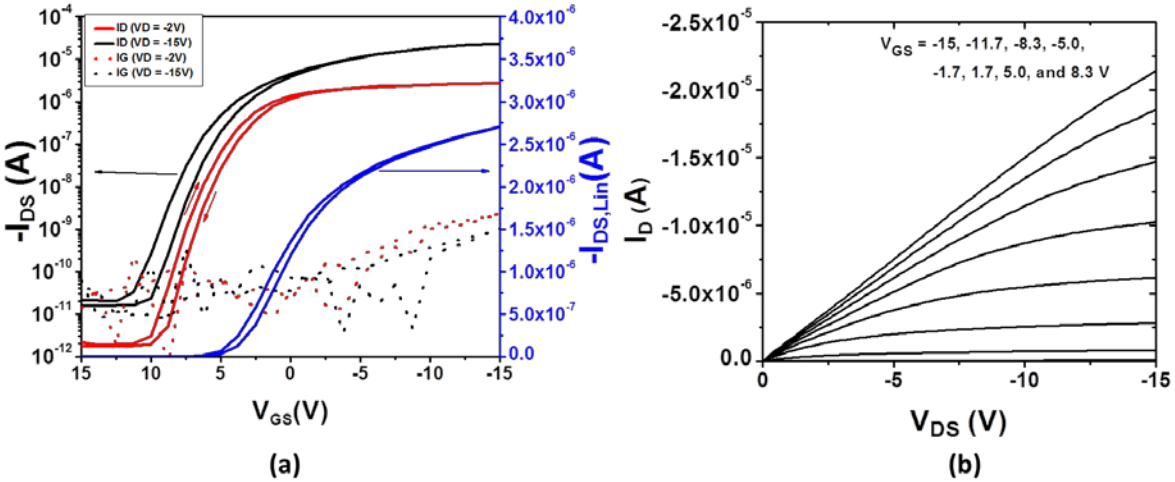


Figure 4.37 (a) Transfer and (b) output characteristics of the S1200 TFT shown in the optical micrograph in Figure 4.35. One of the best TFTs among the devices in Figure 4.36 (L_{gate}=7.5 µm, L_{ch}=5.0 µm, and W=500 µm).

Measured parameters	Values
μ_{LIN} [$cm^2V^{-1}s^{-1}$]	0.22
μ_{SAT} [$cm^2V^{-1}s^{-1}$]	0.23
ON/OFF [A/A]	$1.05x10^6$
SS_{LIN} [V/dec]	0.72
SS_{SAT} [V/dec]	1.21
V_{ON} [V]	10

Table 4.6 Extracted device parameters of the S1200 TFT in Figure 4.37.

In order to reduce device-to-device variation, a rigid substrate carrier is used for handling the flexible PEN substrate. We used a gel material (WF Gel-Film from Gel-Pak®) that can be attached to a rigid substrate on one side and can have PEN substrate stick to the gel film uniformly on the other side. This substrate carrier ensures uniform heat transfer throughout the substrate.

The fabrication process in **Figure 4.35** is modified to include the rigid substrate carrier after the gravure-printing steps. The TFTs with the substrate carrier operate well as shown in **Figure 4.38**. The device-to-device variation is particularly improved as seen from the box plot in **Figure 4.39**. However, overall mobility was degraded (median $\mu_{sat} \approx 0.05$ cm^2/Vs), likely due to non-optimized annealing of the S1200. Due to the thermal insulation characteristic of both the plastic PEN substrate and the Gel-Film, the actual temperature at the top surface of PEN is much lower than the set temperature of hotplate (see **Figure 4.40**). When the PEN substrate is carried with Gel-Film carrier, the surface temperature is about 50°C lower than the temperature of the hotplate. It means in order to apply drying temperature of 100°C that has been used for the previous S1200 TFTs, the hotplate temperature must be set to 150°C. However, when the hotplate temperature is increased to 150°C, the mobility of TFTs drop even more as shown in **Figure 4.41** (nearly two orders of magnitude lower than the S1200 TFTs fabricated on heavily doped silicon wafer. **Figure 4.42** shows average crystallites of S1200 film in previous three TFT groups. From the images taken through a polarizer, it is clear that larger crystallites deliver higher mobility. Therefore, finding a condition that allows formation of larger crystallites in our system is necessary for improving the performance of S1200 TFTs.

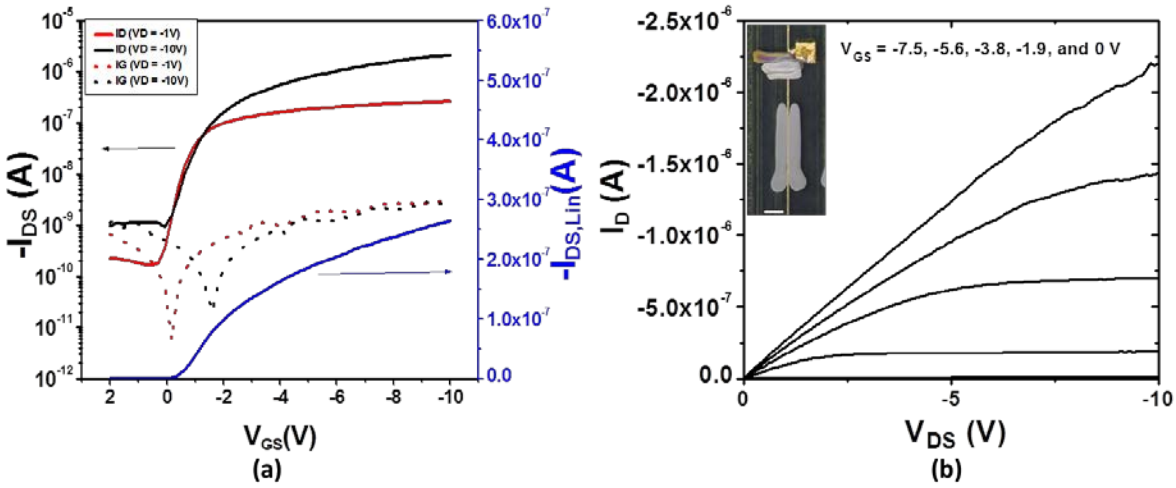


Figure 4.38 (a) Transfer and (b) output characteristics of a printed S1200 TFT on PEN substrate. Fabrication process is based on the process described in Figure 4.35 except the usage of Gel-Film substrate carrier. The gate line in (b) is printed from 6 µm wide cells. The scale bar represents 100 µm. Median thickness of D207 gate dielectric layer is 153 nm.

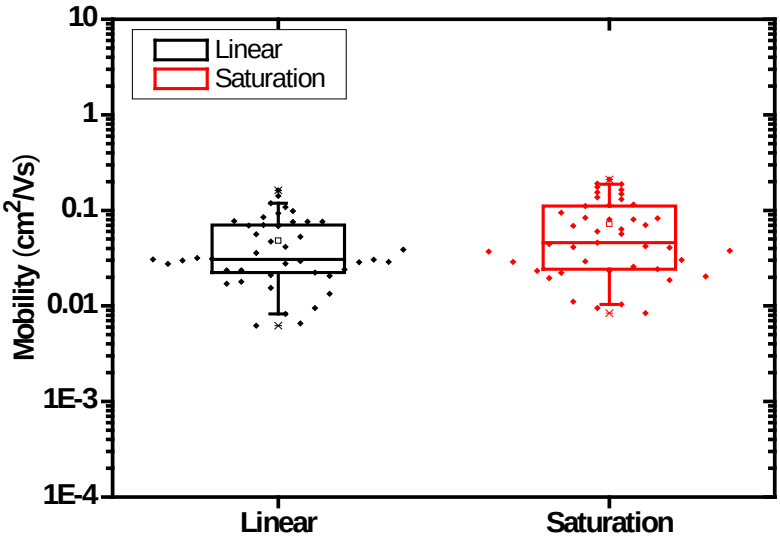


Figure 4.39 Box plot of extracted mobilities from gravure-printed S1200 TFTs in Figure 4.38. Fabrication process is based on the process described in Figure 4.35 except the usage of Gel-Film substrate carrier. Median thickness of gravure printed D207 film is 153 nm, and $L_{ch} \leq 15$ µm.

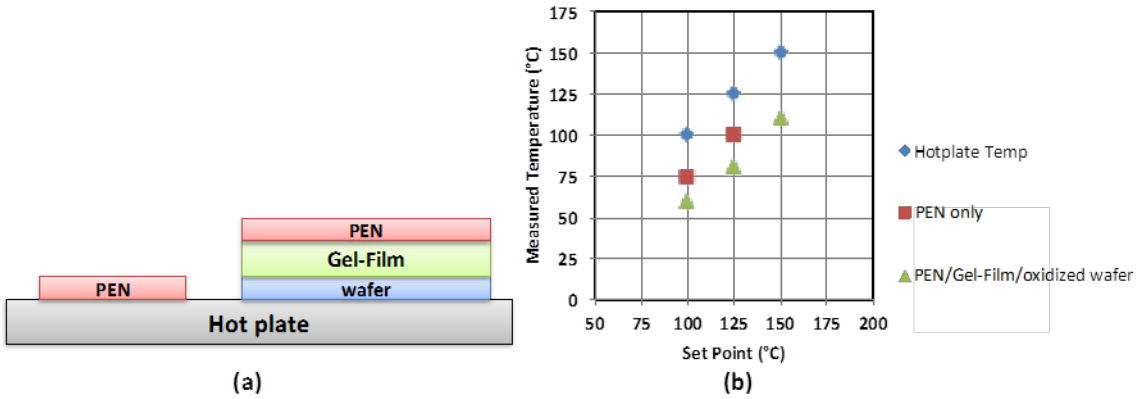


Figure 4.40 (a) PEN substrates with and without a rigid substrate carrier on hotplate during annealing. (b) Surface temperature of PEN substrate with respect to the set temperature of hotplate.

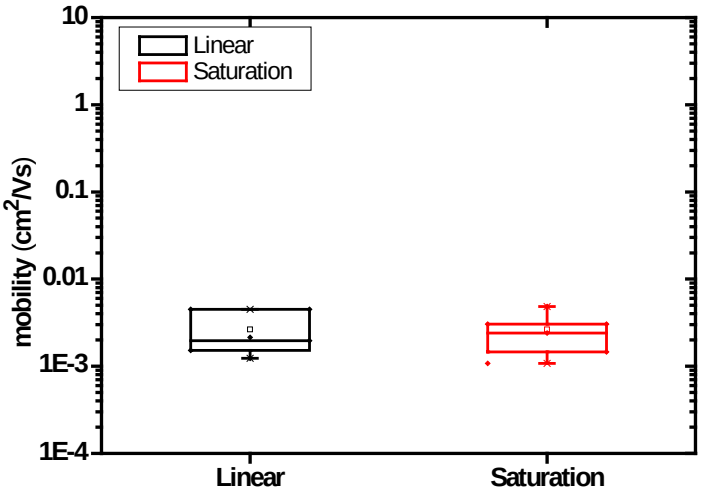


Figure 4.41 Box plot of extracted mobilities of gravure-printed S1200 TFTs on PEN with the rigid substrate carrier. S1200 film in this sample is dried/annealed at 150°C. Median thickness of gravure printed D207 film is 203 nm, and $L_{ch} \leq$ 15 µm.

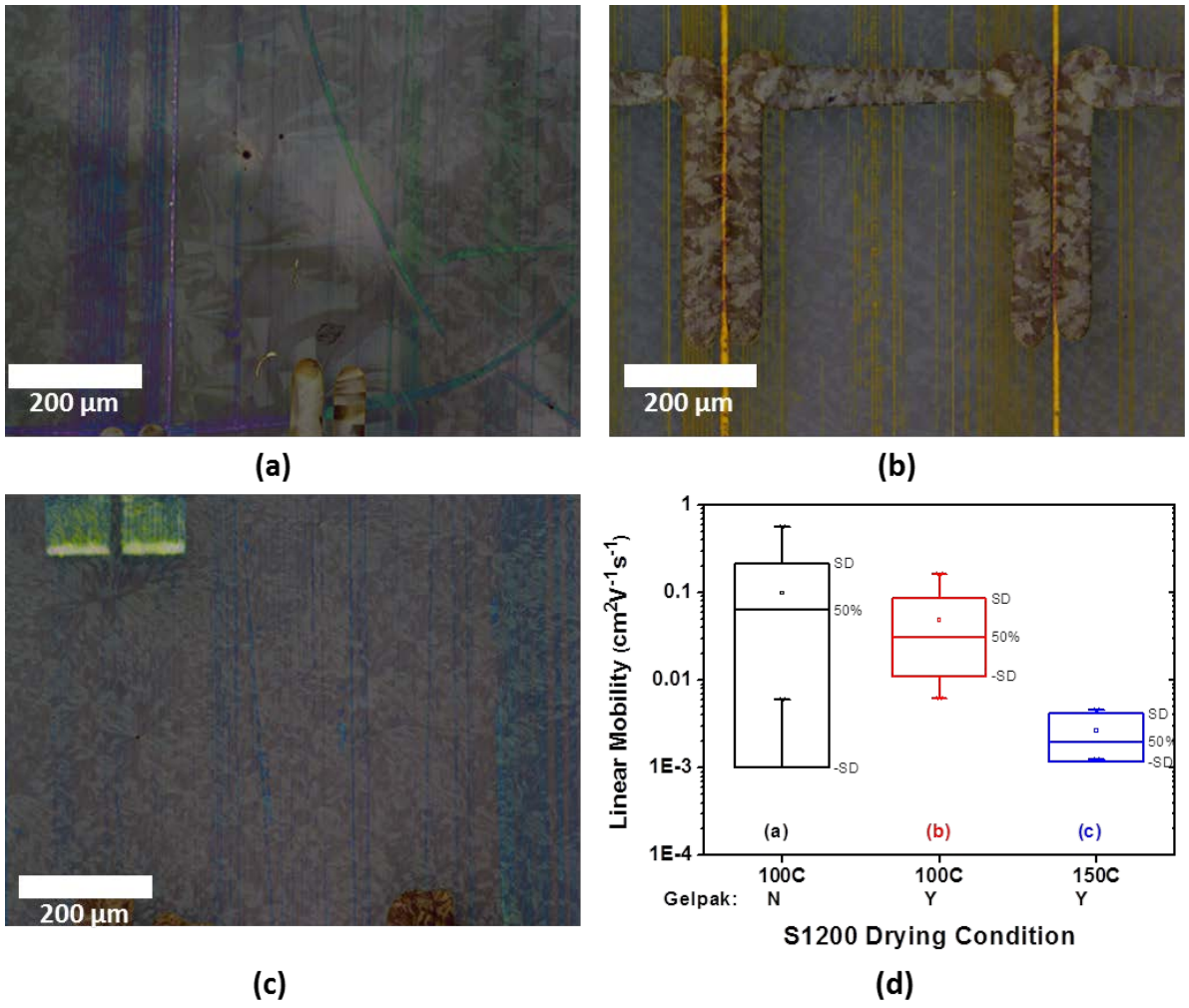


Figure 4.42 Crystallites of S1200 in three different samples above. Fabrication condition: (S1200 drying temperature, rigid substrate used) (a) (100°C, No), (b) (100°C, Yes), and (c) (150°C, Yes). (d) Box plot of linear mobility of the TFTs.

We investigated the effect of drying temperature on the formation of crystallites based on the observation that higher drying temperature in fact resulted in even smaller crystallites and thus lower mobility. Crystallites of S1200 film on PEN/Gel-Film/glass slide are compared when the hotplate temperature is varied from 50°C to 160°C. Unlike pBTTT which shows formation of larger crystal domain at higher annealing temperature, larger crystallites of S1200 are formed at lower temperature as shown in **Figure 4.43**. Further research on the crystallization of the S1200 film is needed to understand the mechanism, but it is therefore expected that the S1200 TFTs dried at lower temperature deliver higher mobility.

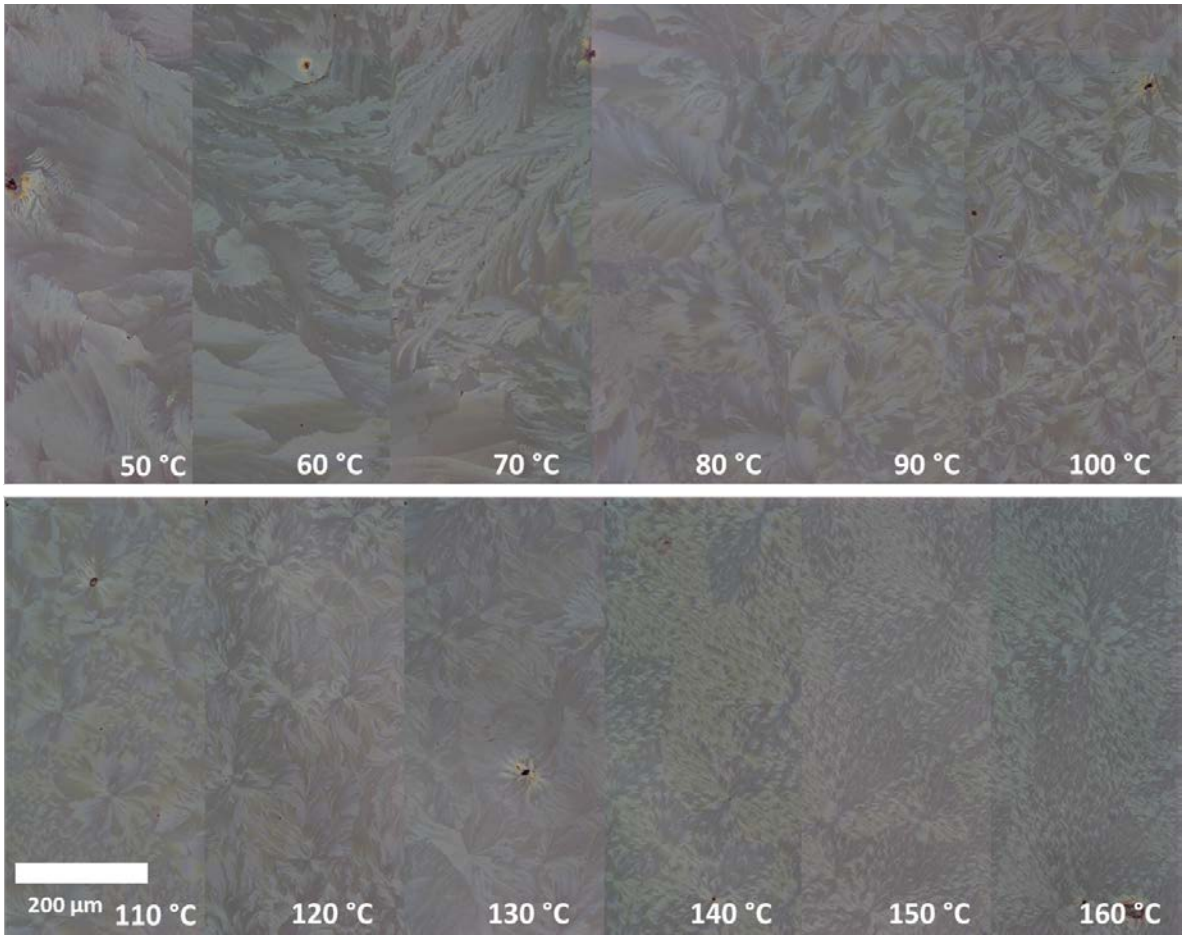


Figure 4.43 The effect of drying temperature on crystallization of S1200 film. S1200 film is spin-coated on UV cross-linked D207 film that is also spin-coated on PEN substrate. Microscope glass slide (1 mm thick) with Gel-Film is used as a PEN carrier.

The TFT fabrication process is modified from **Figure 4.35**: Gel-Film rigid carrier is used, and S1200 film is dried at 60°C. As a result, significantly improved performance of S1200 TFTs is observed in **Figure 4.44**. Average mobility is increased to 0.5 cm^2/Vs which is the highest in these short channel TFTs we have fabricated so far. Device-to-device variation is also improved. Although poorer on/off ratio and worse swing than previous devices are the shortcomings, much improved mobility can lead to significantly faster transistor operation. Lastly, post-annealing at higher temperature (at 100°C for 5 min) in air was tried to hopefully improve the quality of S1200 semiconductor film, but the effect on these TFTs was not very significant.

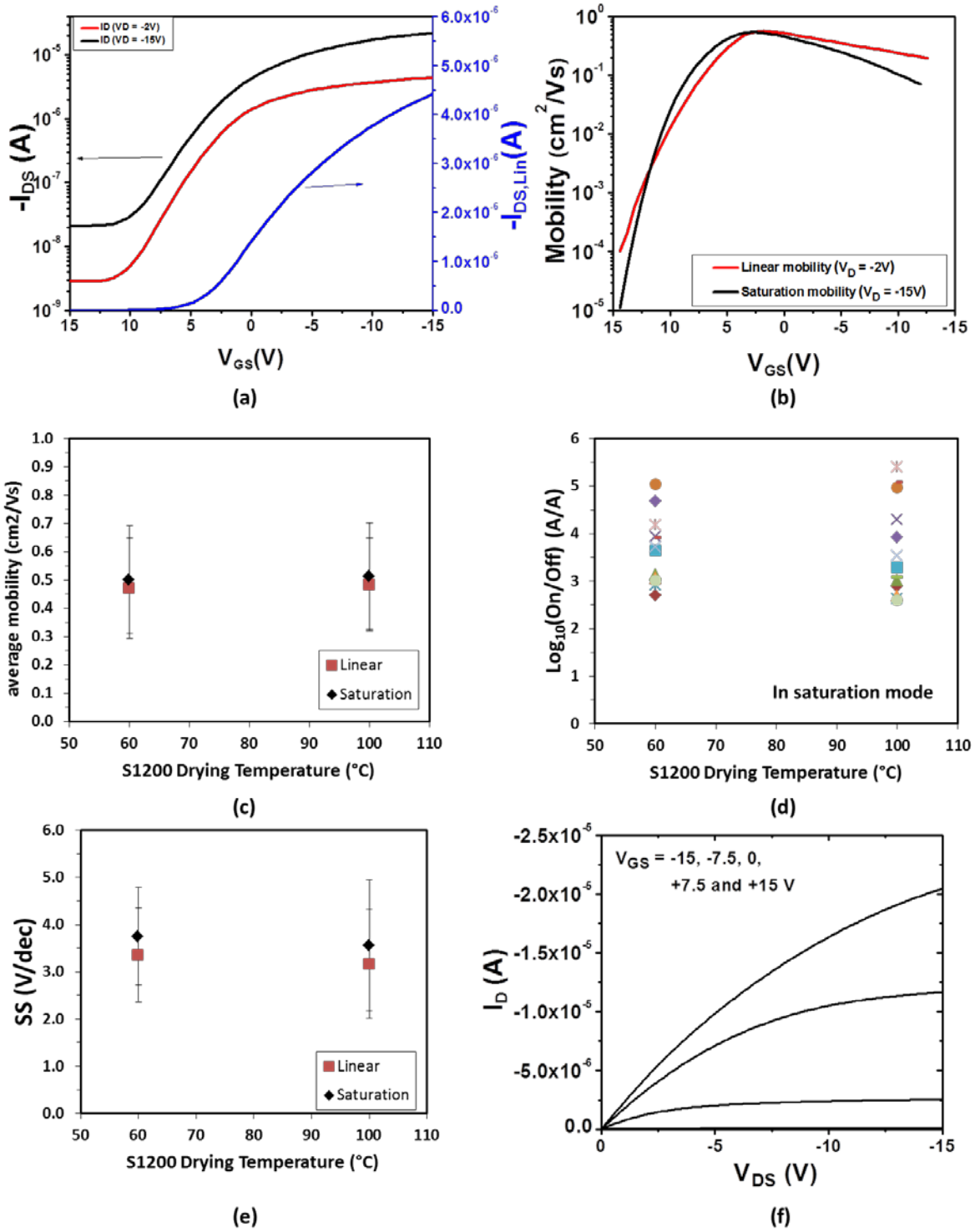


Figure 4.44 Extracted device parameters of the S1200 TFTs dried at 60°C. Microscope glass slide (1 mm thick) with Gel-Film is used as a PEN carrier. Median thickness of gravure printed D207 film is 296 nm, and L_{ch} is from 5 µm to 15 µm. Error bars represent standard deviation of the data.

4.4 High performance gravure-printed inverters

Using the S1200 TFTs in the previous section, inverters are fabricated in order to verify how the scaling and optimized mobility can benefit the speed of transistors and circuits. Since the S1200 is a p-type semiconductor, p-type only inverters were printed, using a PMOS active load. To account for load transistor variations, the load transistor is controlled by separate gate bias (V_{REF}) instead of making a choice between enhancement load (gate is tied to drain) and depletion load (gate is tied to source)(see **Figure 4.45**). In addition, the channel resistance ratio of the two TFTs is controlled by V_{REF} instead of proper sizing between load and drive TFTs. Interconnects between the two TFTs are inkjet-printed during the S/D electrode printing step.

A fully fabricated PMOS inverter is shown in **Figure 4.45**. This inverter is fabricated with the rigid substrate carrier and drying temperature of 100°C (the same as the TFTs in **Figure 4.38)**. Gate lines in the picture are printed from 2.5 μm wide cells, resulting in only about 4.5 μm wide lines. Drive and load TFTs show almost identical behavior with maximum saturation mobility ~0.2 cm^2/Vs. Calculated transition frequencies for the driver and load TFTs are ~350 and 320 kHz, respectively. Voltage transfer characteristic (VTC) and voltage gain of the inverter is presented in **Figure 4.46**. Typical single-type transistor based inverter characteristic is observed. Due to the thin gate dielectric layer (~160 nm), the operation voltage (V_{DD}) is reduced to even 3 V while the maximum voltage gain is still above 1 V/V. Transient characteristic of the inverter is also measured. For simplicity, a high-impedance probe, Picoprobe® MODEL 18C (input capacitance of 20 fF, and up to 15V operation), is used to measure the output signal of the inverter. Since the input capacitance of the inverter is around 400 fF, fan-out of the operation is only about 0.05 which indicates that the propagation delay measured in this setup can be only slightly longer than the intrinsic delay of the inverter. As shown in **Figure 4.47**, much improvement compared to previous reports discussed in Chapter 1 is observed. Propagation delay observed here is as low as 2.5 μsec (t_p) at V_{DD} of only -5V and 2.75 μsec at -10V. t_{pLH} is only 1.5 μsec which is close to MHz operation.

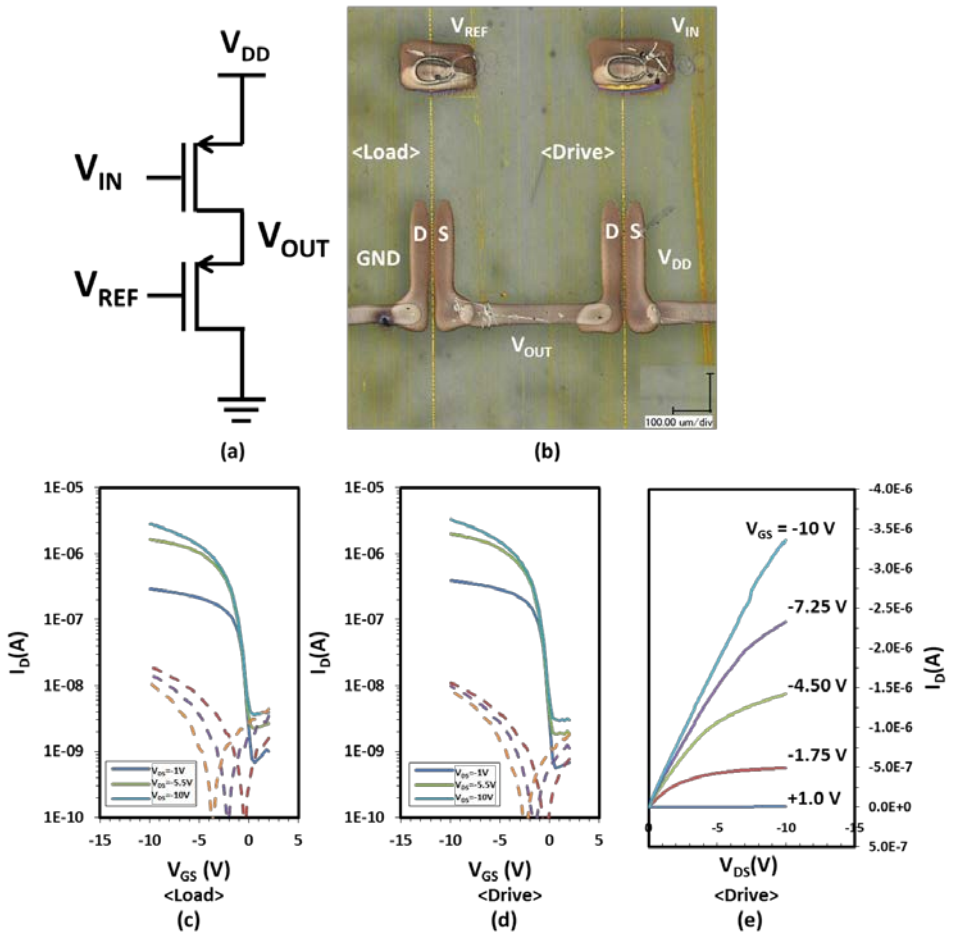


Figure 4.45 Printed PMOS inverter using TFTs from the sample in Figure 4.39. (a) Circuit diagram of the PMOS inverter. (b) Optical micrograph of the inverter without polarizer. (c-e) I-V characteristics of the TFTs in (b).

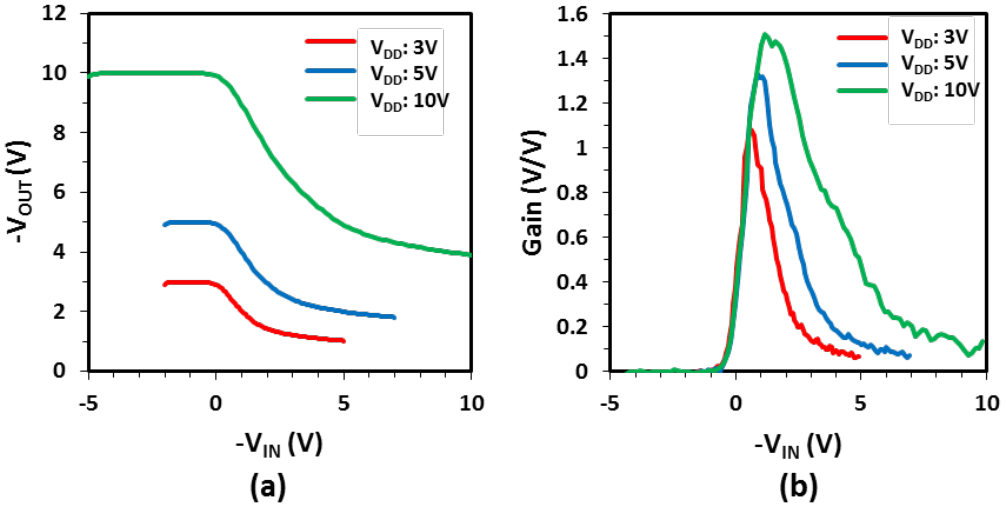


Figure 4.46 (a) Voltage transfer characteristic and (b) voltage gain of the inverter in Figure 4.45. Extracted parameters of the inverter is given in the following Table 4.7.

V_{DD} [V]	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [V]	NM_L [V]	Swing [V]	Maximum voltage gain [V/V]
3	3.00	-0.80	0.8	0.45	2.20	1.25	3.80	1.08
5	4.90	-0.02	1.5	0.50	3.40	0.52	4.92	1.33
10	9.98	-1.07	2.8	0.50	7.18	1.57	11.05	1.50

Table 4.7 Extracted parameters of the inverter in Figure 4.46. It is important to note that the input and output voltage range in this measurement is not symmetric due to no optimization of turn-on voltage. V_{OL} values given are represented in input voltage (x-axis). When in output voltage (y-axis), minimum input voltage must be subtracted.

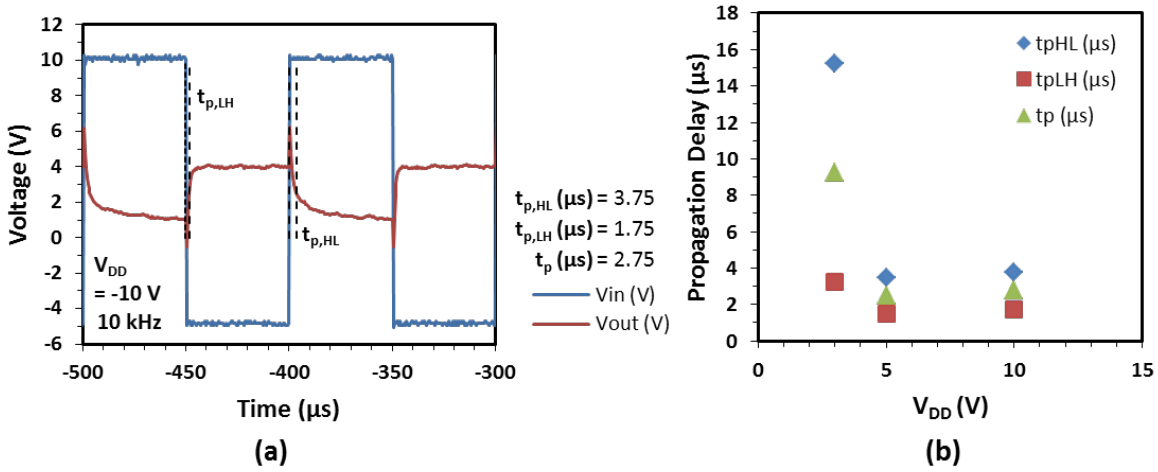


Figure 4.47 (a)Transient response of the inverter in Figure 4.45 when operation voltage is 10V (from -5V to +5V). (b) Extracted propagation delay. $t_p = (t_{pHL} + t_{pLH})/2$.

Lastly, the low-temperature drying condition for the S1200 film discussed in the previous section is applied to the inverters for further speed enhancement. These inverters are therefore fabricated with the rigid substrate carrier and drying temperature of 60°C as in **Figure 4.44**. Good crystallization of S1200 is observed in **Figure 4.48**. Due to the thicker D207 layer (~290 nm) than the previous inverter, operation voltage is slightly higher, but still the inverter can operate at V_{DD} of 10V. Although the inverters here are not as highly scaled as the inverter in **Figure 4.45** due to the wider gate lines, the speed of the inverter is faster than the previous one due to the higher field-effect mobility (**Figure 4.44)**. Propagation delay measured at V_{DD} of 10V shows >1MHz operation. Measured t_{pLH} is as low as 350 nsec. Due to the asymmetrical performance of the TFTs in inverters of this sample, t_{pHL} is much larger than t_{pLH}. However, it is enough to prove that the benefit of high mobility is represented in the improvement of the speed of inverters.

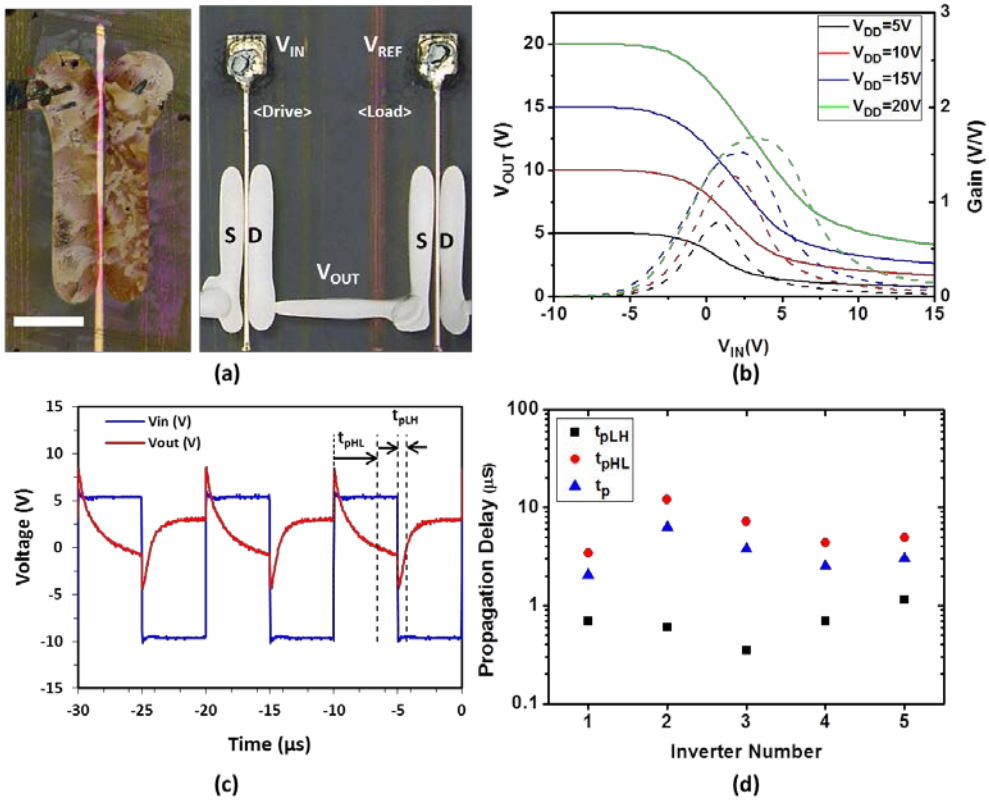


Figure 4.48 PMOS inverters with optimized mobility of S1200 as in Figure 4.44. (a) Optical micrographs of the devices with S1200 under polarizer (left) and without S1200 (right). Scale bar represents 100 µm. (b) Voltage transfer characteristic of the inverter with voltage gain (dotted lines) (c) Extraction of propagation delay when V_{DD} is 10V (from -5V to +5V). (d) Extracted propagation delay of five different inverters printed within the same sample. The inverter in (c) is inverter #1 in (d).

V_{DD} [V]	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [V]	NM_L [V]	Swing [V]	Maximum voltage gain [V/V]
10	10.00	-7.95	3.23	0.25	6.77	8.20	17.95	1.27
15	14.99	-7.36	4.63	-0.75	10.36	6.61	22.35	1.52
20	19.99	-6.39	6.73	-0.85	13.26	5.54	26.38	1.68

Table 4.8 Extracted parameters of the inverter in Figure 4.48. It is important to note that the input and output voltage range in this measurement is not symmetric due to no optimization of turn-on voltage. V_{OL} values given are represented in input voltage (x-axis). When in output voltage (y-axis), minimum input voltage (-10V) must be subtracted.

4.5 Summary

In this chapter, highly scaled gravure-printed organic TFTs on plastic are investigated. By using the highly scaled metal electrodes introduced in Chapter 3 as gate electrodes, channel length of the TFTs have been reduced to 5 μm while minimizing parasitic capacitances. Two different material systems, pBTTT and S1200, have been explored. While the polymer semiconductor, pBTTT, shows a benefit of low device-to-device variation, S1200 system surpasses the performance of pBTTT system in many aspects: higher mobility in both linear and saturation (0.5 cm^2/Vs), low operation voltage (as low as only 3 V), faster operation speed (beyond 1MHz), easier fabrication (all in air), and lower processing temperature (only 60°C for S1200 and 140°C including metal layers). With all those benefits observed from the fabricated S1200 TFTs and inverters, it is demonstrated that our highly scaled gravure-printed metal lines below 5 μm are successfully integrated with a state-of-the-art organic semiconductor, resulting in enormously improved speed of the printed transistors, delivering >1MHz operation.

4.6 References

[1] Jinsoo Noh, Dongsun Yeom, Chaemin Lim, Hwajin Cha, Jukyung Han, Junseok Kim, Yongsu Park, V. Subramanian, and Gyoujin Cho, "Scalability of Roll-to-Roll Gravure-Printed Electrodes on Plastic Foils," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 33, no. 4, pp. 275–283, Oct. 2010.

[2] A. de la Fuente Vornbrock, D. Sung, H. Kang, R. Kitsomboonloha, and V. Subramanian, "Fully gravure and ink-jet printed high speed pBTTT organic thin film transistors," *Organic Electronics*, vol. 11, no. 12, pp. 2037–2044, Dec. 2010.

[3] L. A. Lucas, D. M. DeLongchamp, B. M. Vogel, E. K. Lin, M. J. Fasolka, D. A. Fischer, I. McCulloch, M. Heeney, and G. E. Jabbour, "Combinatorial screening of the effect of temperature on the microstructure and mobility of a high performance polythiophene semiconductor," *Applied Physics Letters*, vol. 90, no. 1, p. 012112, Jan. 2007.

[4] E. S. H. Kang and E. Kim, "Effect of non-isothermal recrystallization on microstructure and transport in poly(thieno-thiophene)thin films," *Organic Electronics*, vol. 12, no. 10, pp. 1649–1656, Oct. 2011.

[5] Y. Jung, R. J. Kline, D. A. Fischer, E. K. Lin, M. Heeney, I. McCulloch, and D. M. DeLongchamp, "The Effect of Interfacial Roughness on the Thin Film Morphology and Charge Transport of High‐Performance Polythiophenes," *Advanced Functional Materials*, vol. 18, no. 5, pp. 742–750, Mar. 2008.

[6] J. N. Haddock, X. Zhang, S. Zheng, Q. Zhang, S. R. Marder, and B. Kippelen, "A comprehensive study of short channel effects in organic field-effect transistors," *Organic Electronics*, vol. 7, no. 1, pp. 45–54, Feb. 2006.

[7] S. Locci, M. Morana, E. Orgiu, A. Bonfiglio, and P. Lugli, "Modeling of Short-Channel Effects in Organic Thin-Film Transistors," *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2561–2567, Oct. 2008.

[8] M. Koehler and I. Biaggio, "Space-charge and trap-filling effects in organic thin film field-effect transistors," *Phys. Rev. B*, vol. 70, no. 4, p. 045314, Jul. 2004.

[9] J. Li, Y. Zhao, H. S. Tan, Y. Guo, C.-A. Di, G. Yu, Y. Liu, M. Lin, S. H. Lim, Y. Zhou, H. Su, and B. S. Ong, "A stable solution-processed polymer semiconductor with record high-mobility for printed transistors," *Sci. Rep.*, vol. 2, Oct. 2012.

[10] H. Chen, Y. Guo, G. Yu, Y. Zhao, J. Zhang, D. Gao, H. Liu, and Y. Liu, "Highly π-Extended Copolymers with Diketopyrrolopyrrole Moieties for High-Performance Field-Effect Transistors," *Advanced Materials*, vol. 24, no. 34, pp. 4618–4622, 2012.

[11] H. Minemawari, T. Yamada, H. Matsui, J. Tsutsumi, S. Haas, R. Chiba, R. Kumai, and T. Hasegawa, "Inkjet printing of single-crystal films," *Nature*, vol. 475, no. 7356, pp. 364–367, Jul. 2011.

[12] Y. Fujisaki, H. Ito, Y. Nakajima, M. Nakata, H. Tsuji, T. Yamamoto, H. Furue, T. Kurita, and N. Shimidzu, "Direct patterning of solution-processed organic thin-film transistor by selective control of solution wettability of polymer gate dielectric," *Applied Physics Letters*, vol. 102, no. 15, p. 153305, 2013.

[13] S. K. Park, T. N. Jackson, J. E. Anthony, and D. A. Mourey, “High mobility solution processed 6,13-bis(triisopropyl-silylethynyl) pentacene organic thin film transistors,” *Applied Physics Letters*, vol. 91, no. 6, p. 063514, 2007.
[14] H. Minemawari, T. Yamada, H. Matsui, J. Tsutsumi, S. Haas, R. Chiba, R. Kumai, and T. Hasegawa, “Inkjet printing of single-crystal films,” *Nature*, vol. 475, no. 7356, pp. 364–367, Jul. 2011.
[15] L. M. Peurrung and D. B. Graves, “Film Thickness Profiles over Topography in Spin Coating,” *J. Electrochem. Soc.*, vol. 138, no. 7, pp. 2115–2124, Jul. 1991.
[16] D. B. LaVergne and D. C. Hofer, “Modeling Planarization With Polymers,” 1985, vol. 0539, pp. 115–123.

Chapter 5

Mechanism of Low-Frequency Noise in OTFTs

5.1 Background

In the previous sections, we have provided an in-depth study of pattern printing processes, and have realized significant performance improvement of gravure-printed transistors by substantial scaling of the gravure printed lines. In Chapter 1, various types of sensor and actuator applications are introduced. The high-speed operation (MHz) of the printed transistors is also beneficial for sensing applications because the temporal resolution of the sensing operation can be improved.[1] What is also very critical is the noise immunity of the printed transistors since it limits the bandwidth of the sensing operation. As mentioned in Chapter 1, 1/f noise is of particular importance in OTFTs due to the low current level and slow operation speed. However, 1/f noise in OTFTs is relatively unknown. Therefore, in this chapter, the detail of 1/f noise in OTFTs is presented.

For more than four decades, *1/f* noise in conventional MOSFETs has been studied intensively, and it is generally believed that there are two dominant sources of *1/f* noise – fluctuations in the number of carriers due to carrier trapping by oxide traps and in the carrier mobility due to phonon scattering.[2] Not only are theories about the physical mechanism of noise suggested, but several analysis methods to verify the physical mechanism have been introduced.[3]–[5] In previous work on low-frequency noise (LFN) in OTFTs, there has been disagreement regarding which mechanism is more applicable to OTFTs. Some authors concluded that the mobility fluctuation is dominant in OTFTs by using Hooge's empirical equation in Equation (1) to analyze their experiment results.[6]–[9]

$$\frac{S_I}{I^2} = \frac{\alpha_H}{fN_{total}} \tag{1}$$

where S_I represents power spectral density of drain current, I is drain current, α_H is Hooge number, f is frequency, and N_{total} is the total number of carriers. Unfortunately, since this model is purely empirically derived, it is difficult to explain the physical origins of observed deviations from ideal 1/f behavior. On the other hand, others have speculated that

the McWhorter's number of carrier fluctuation is the dominant origin of noise in OTFTs.[10]–[13] In these works, the active traps that are considered to be important in OTFTs are not the oxide traps, but traps within semiconductor. This model, being physically derived, is able to explain observed non-idealities. To date, none of the reported studies have performed detailed analysis on the non-idealities observed in the LFN characteristics of TFTs. Therefore, it has not been possible to establish the relative dominance of the various mechanisms due to a lack of comprehensive experimental data and related modeling. This detailed analysis was performed and is presented in this chapter. The earlier part of this chapter will show the LFN measurement of OTFTs under dc bias. Drain current noise measurements on evaporated pentacene-based OTFTs having different grain size, pentacene film thickness and operating region are conducted. The effects of semiconductor grain size, semiconductor film thickness and operating region on LFN will be presented and analyzed. The latter part of this chapter will show the LFN measurement of OTFTs under ac bias. Drain current noise measurements on solution-processed polymer semiconductor-based OTFTs during gate switching will be presented and analyzed.

5.2 Low-frequency noise under dc bias

5.2.1 Experiment setup

5.2.1.1 Evaporated pentacene TFTs

In order to control the characteristics of semiconductor accurately, thermally evaporated pentacene TFTs with bottom gated structure were chosen for the drain current noise measurement in this experiment. Pentacene was selected as the semiconductor of choice due to the high degree of control of grain structure that is achievable, allowing for precise correlation of physical structure to noise properties. A heavily doped n-type silicon wafer was used as the bottom gate, 100 nm thermal oxide was used as the gate insulator, and 100 nm thermally evaporated lithographically patterned gold was used for the source and drain electrodes. An HMDS layer was deposited on the oxide before the pentacene deposition to ensure deposition of high-quality semiconductor films. The morphology and thickness of pentacene film were controlled precisely via a method published previously.[14] The device structure is illustrated in **Figure 5.1(a)**. Five different samples were prepared for measurement as shown in **Figure 5.1(b)**. Two different thicknesses of 14 nm and 26 nm were used, with varying grain size from 0.48 μm^2 to 3.92 μm^2. TFTs with large pentacene grains had μ_{Lin} of 3×10^{-3} $cm^2V^{-1}s^{-1}$, on/off ratio of 10^4, and ON current of 1 μA. The TFTs with small grains had around 1 order of magnitude lower in linear mobility. DC characteristics of devices were measured under nitrogen ambient with temperature controller used to precisely control the substrate temperature during measurement. The transfer and output characteristics of the measured TFTs are shown in **Figure 5.2**.

5.2.1.2 Low-frequency noise measurement under dc bias configuration

The low-frequency noise characteristics of these devices were measured with a dynamic signal analyzer, HP 35670A after amplification using a low noise transimpedance amplifier, BTA9812B. The measurement configuration is shown in **Figure 5.3**. The dc bias of the device under test (DUT) was provided by Agilent 4156 semiconductor parameter analyzer (SPA) through low pass filters. Therefore, the dc component of the drain current (I_{DS}) is supplied from the SPA. The ac component of the drain current (i_{DS}), the LFN signal, will only pass the transimpedance amplifier that is connected to the drain terminal of the DUT. The BTA9812B transimpedance amplifier has a gain of 1 *mV/nA*. The range of frequency for measurement is selected from 1 Hz to 100 Hz since lower frequency makes the measurement interval too long and unreliable. At frequencies higher than 100 Hz, the measured noise becomes comparable to the chamber noise which is measured when the DUT is connected without any dc bias. The LFN measurements are conducted in both linear and saturation operation modes.

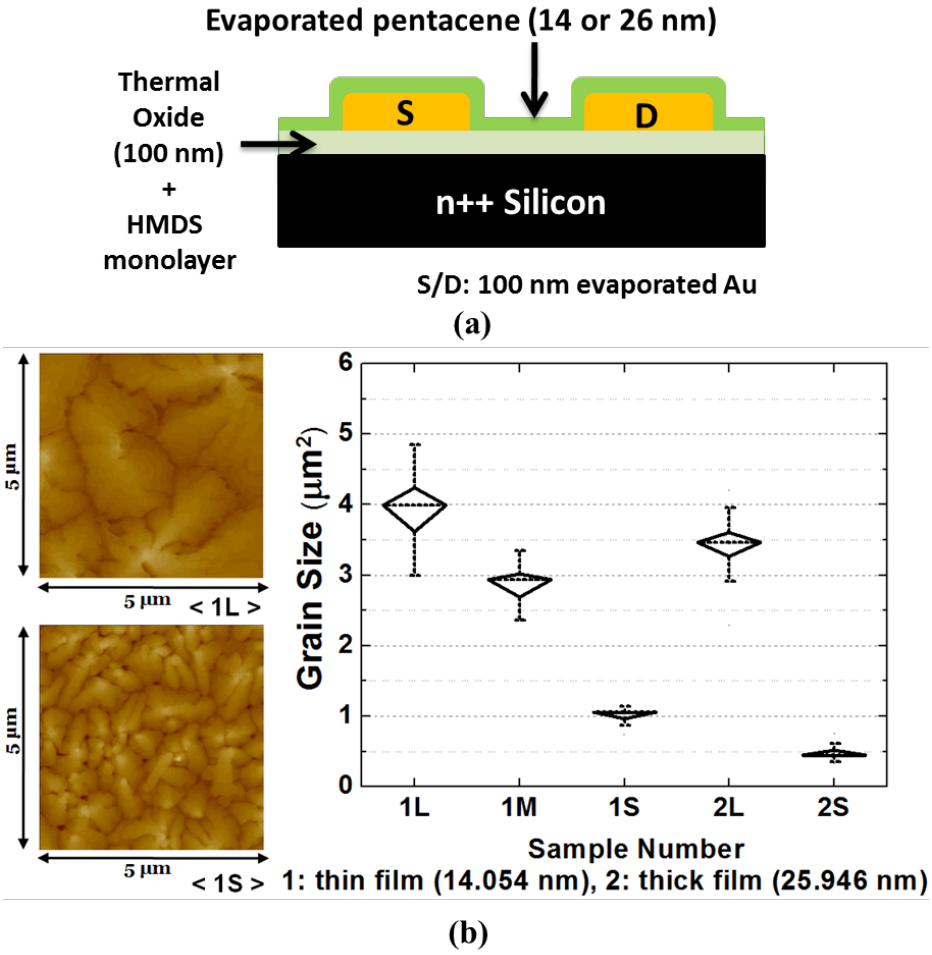


Figure 5.1 (a) Device structure (b) Grain size of pentacene film samples used in this experiment and AFM images: thickness of pentacene film: 1 (14 nm), 2 (26nm), grain size: L (large), M (middle), S (small).

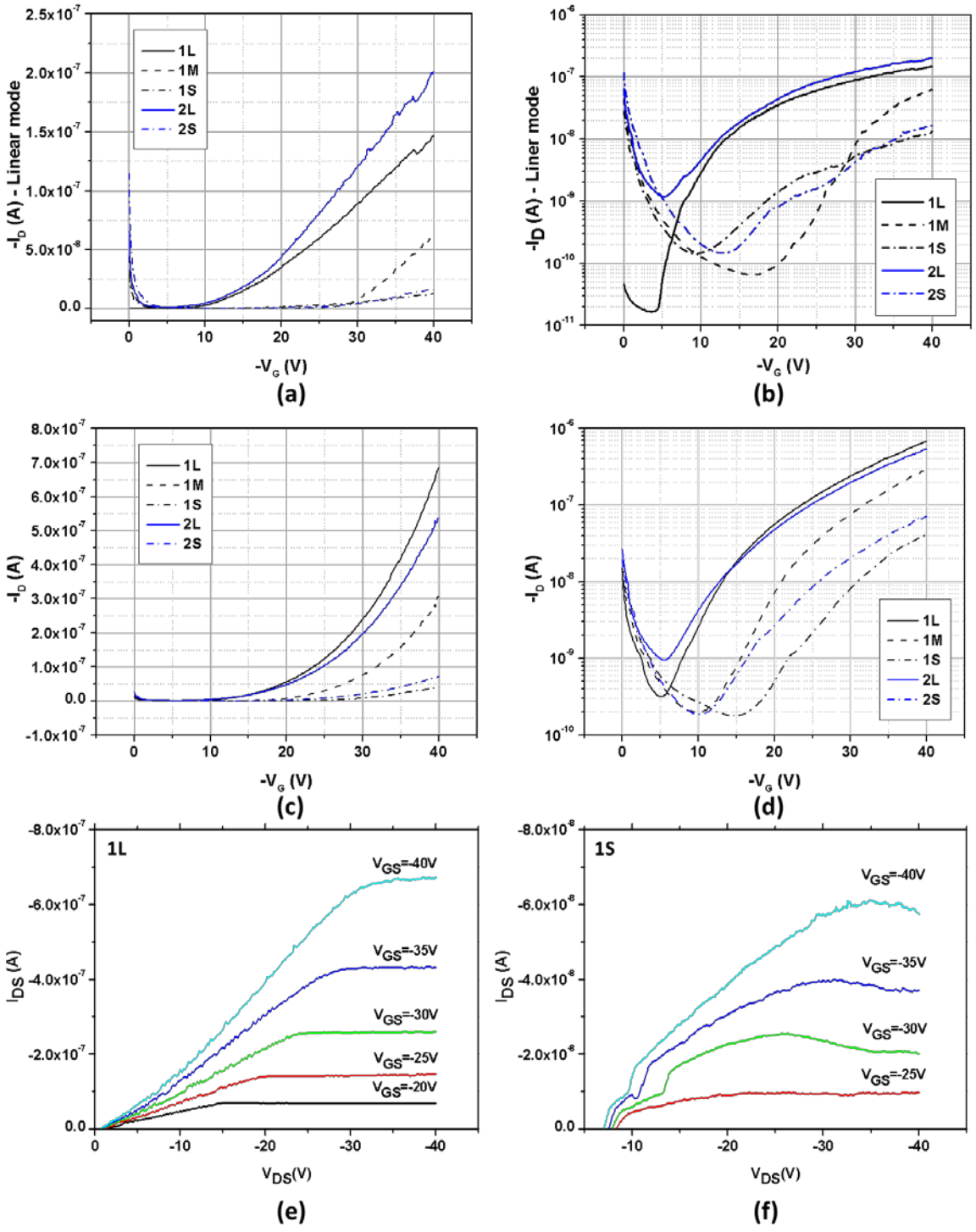


Figure 5.2 Transfer characteristics of the measured transistors (a) and (b) in linear mode, and (c) and (d) in saturation mode. Output characteristics of (e) 1L and (f) 1S.

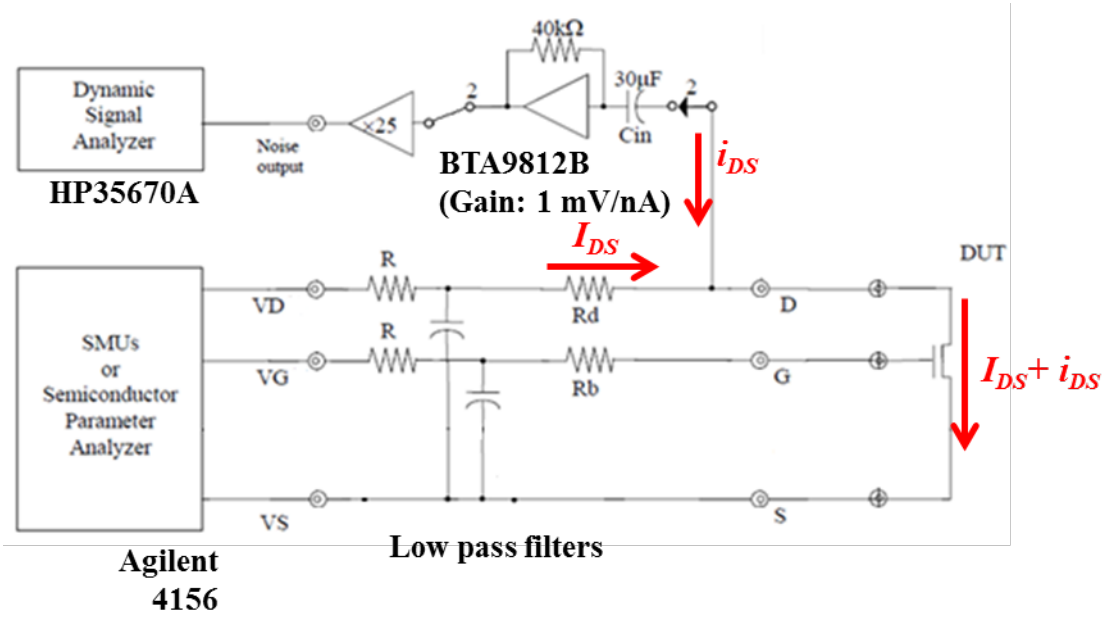


Figure 5.3 Noise measurement setup. BTA9812B (transimpedance amplifer) and HP35670A are provided by the Device Characterization Laboratory (DCL) in UC Berkeley. This image is obtained from the user manual of BTA9812B with modification.

5.2.2 Experiment results

5.2.2.1 Correlation of non-ideality in 1/f noise to band structure

Figure 5.4(a) and **(b)** show representative data of normalized drain current spectral densities for all the samples under linear and saturation modes. All spectra show a monotonic decrease as frequency increases, and become constant beyond a certain frequency. This is a typically observed characteristic of transistor noise, where *1/f* noise is dominant in the low frequency region and it is flattened by the limitation of background chamber noise (or thermal noise if the chamber noise is much smaller). It confirms that the measurement is conducted properly. Importantly, not all devices follow exact *1/f* dependence. Instead, the exponent values (γ) in $1/f^{\gamma}$ behavior vary depending on the sample type and operating region. As shown in **Figure 5.4(c)**, in linear mode, samples with relatively large pentacene grains (1L, 1M and 2L) have γ close to 1. However, the exponent γ values for samples with small grains (1S and 2S), are much larger than 1. When devices are operated in saturation, all the devices have γ larger than 1 and close to 1.4 ~ 1.5. However, no significant effect of semiconductor film thickness on noise characteristics was observed. I believe it is because the carriers are mostly located near the semiconductor/insulator interface and are thus not significantly affected by the additional semiconductor layers present in thicker channel films.

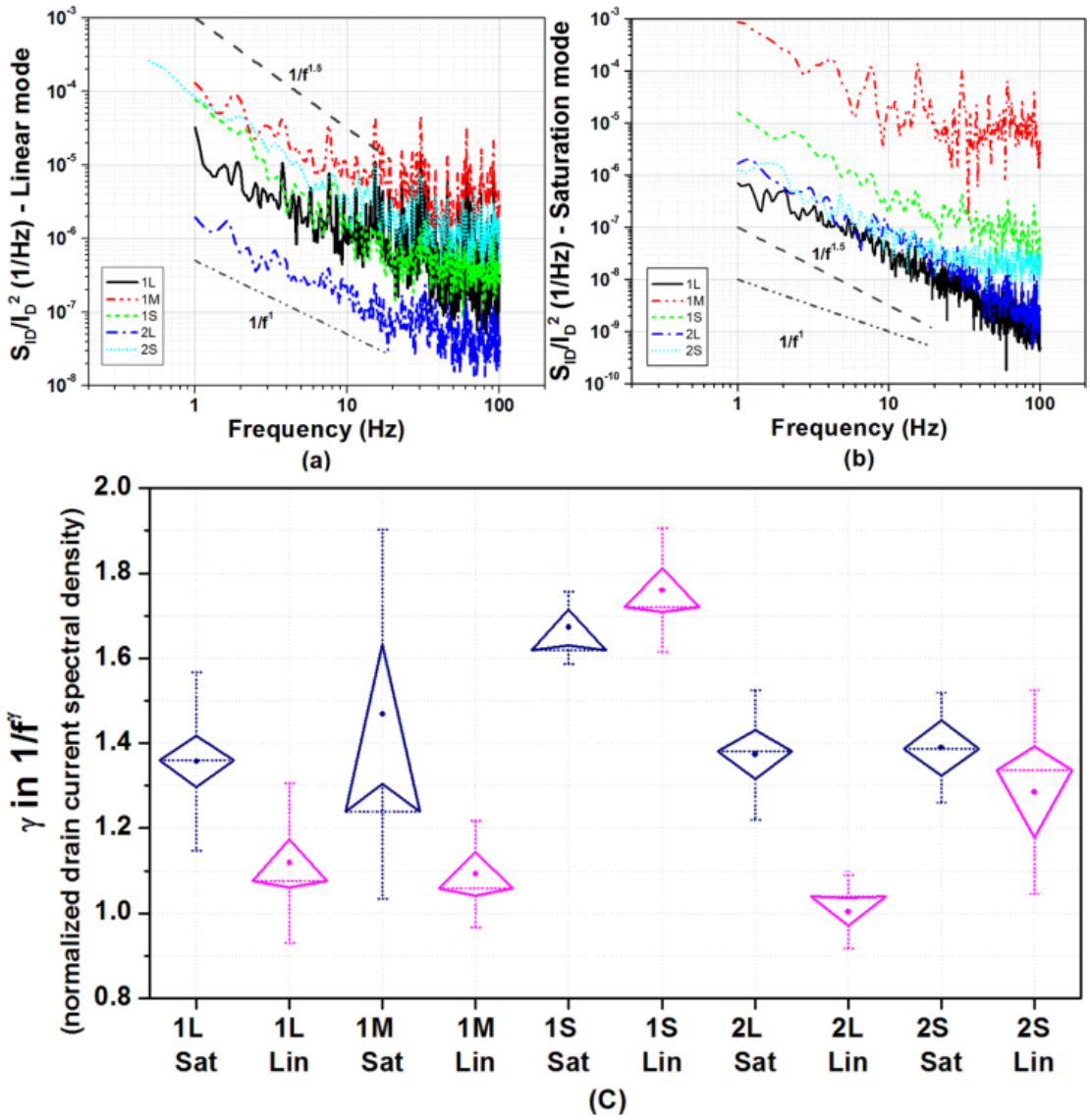


Figure 5.4 Normalized drain current spectral density for all the samples under (a) linear region (b) saturation region. For the slope comparison, 1/f and $1/f^{1.5}$ relationships are also plotted alongside of measured data. The spectral density above 100 Hz is constant due to thermal noise. (c) Distribution of exponent values of $1/f^{\gamma}$ in (a) and (b), (Sat: saturation, Lin: Linear). Diamond boxes in the graph define the boundary of standard errors, and whiskers in the graph show boundary of standard deviations.

It has been known that the exponent of $1/f^{\gamma}$ behavior in drain current spectral density is closely related to the location of the Fermi level, trap distribution and available energy states within the energy gap of the semiconductor [4], [15], [16]. Since the trapping and de-trapping of carriers by/from traps are based on Shockley–Read–Hall (SRH) process, the multiplication of the probability of finding electrons, *f(E)*, and the probability of finding empty states, *1-f(E)*, is maximized at the Fermi level (E_F) as shown in **Figure 5.5(a)**. When only a single trap plays a role in generating low-frequency noise, the power spectral density (PSD) of the noise will show Lorentzian spectrum in **Figure 5.5(b)**. The PSD is constant

below the corner frequency that is inversely proportional to the average time to take during the trapping and de-trapping by/from the single trap, and the PSD rolls off with $1/f^2$ relationship above the frequency. It has been observed in sub-micron MOSFETs and called random telegraph noise (RTN). When multiple traps with different roll-off frequencies exist in a single device, the PSD of the noise in the device is thus the sum of the PSD of the Lorentzian spectrum with different roll-off frequencies, resulting in the 1/f like PSD of the noise in the device as shown in **Figure 5.5(c)**.

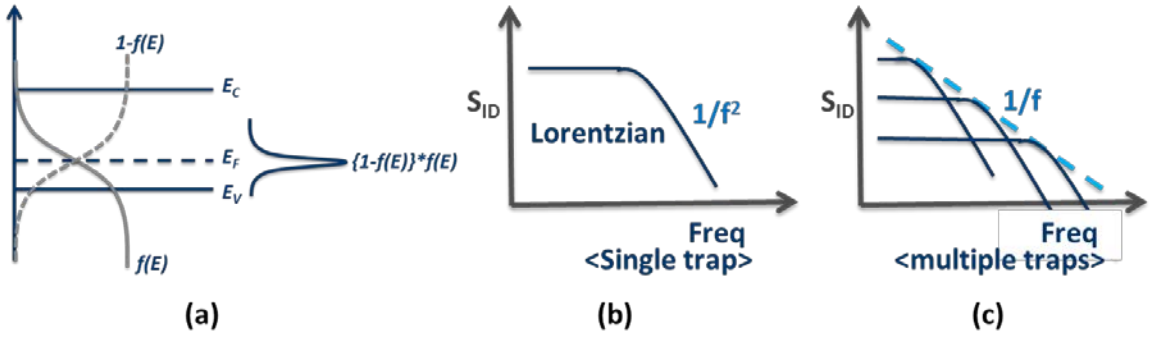


Figure 5.5 (a) Possibility of the carriers to be trapped by empty states within the band gap (b) Power spectral density of the noise when only a single trap is involved (c) Power spectral density of the noise when multiple traps are involved.

Christensson et al. explained that the PSD of the flicker noise in conventional MOSFET shows exact 1/f behavior only if the dominant oxide traps have uniform distribution over space and energy because in that case traps with different lifetimes are equally distributed.[4] However, if the distribution of traps is not uniform, the PSD will deviate from the ideal *1/f* behavior. In polycrystalline silicon TFTs, for example, the exponent value was observed to be smaller than 1 due to the presence of band-tail states, which require shorter time for trapping and de-trapping.[15] Therefore, carrier trapping/de-trapping correlated with shorter lifetime becomes more dominant, and thus noise levels in the high frequency region increase, resulting in an exponent less than 1.

Our experimental results can also be explained in the same way. When the TFTs operate in the saturation mode, the channel region near the drain is not in accumulation due to the high drain bias. Since organic semiconductors are generally semi-insulating, the Fermi level near the drain region is thus located near mid-gap. Because the traps near the Fermi level are the dominant active traps for noise generation as explained in **Figure 5.5(a)**, only deep traps at the grain boundaries (GBs) will then participate in the fluctuation of the number of carrier. Since trapping by deep level traps is known to be slower process than by shallow traps, the noise level at low frequency will be enhanced with increasing number of deep traps as illustrated in **Figure 5.6(a)**. Thus, it is measured that the slope in drain current spectral density becomes steeper. This is thus the reason why we observed a larger exponent when the TFTs operate in saturation as confirmed in **Figure 5.4**. This result is consistent with previous observations by Ke et al.'s work shown in **Figure 5.6(b)**, which show an increasing exponent value with increasing drain bias.[13] Note that the exponent distinction between operating modes was not observed in the samples with smaller grains such as 1S and 2S. In fact, in both operation modes, steeper slope of the flicker noise was

observed. Due to the smaller grain size, those devices have more GBs, and therefore the effect of the deep traps at the GBs on the exponent is still present even in the linear mode of operation.

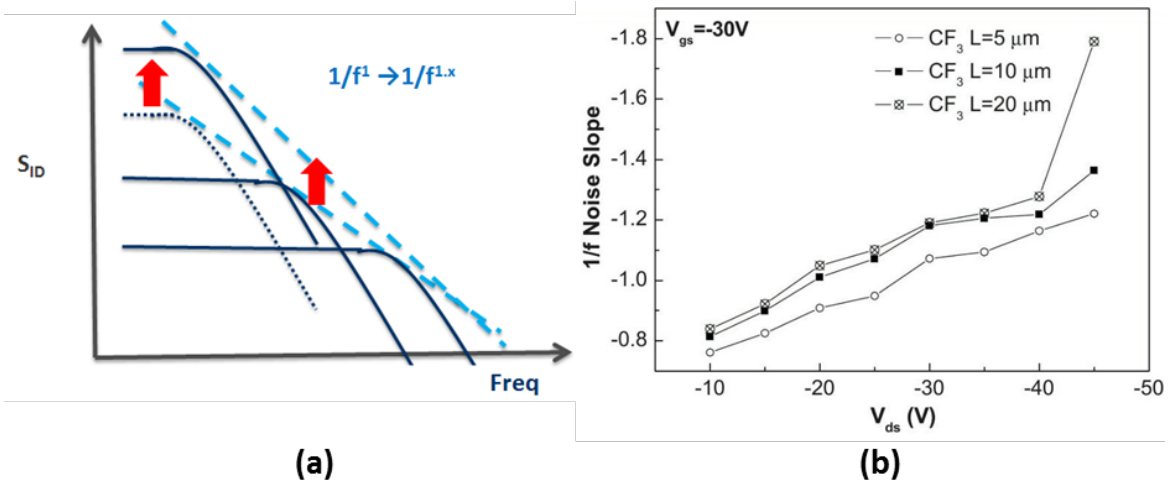


Figure 5.6 (a) Change of drain current power spectral density when slower traps are more dominant (b) Figure 5 in Ke et al.'s work[13].

5.2.2.2 Density of states (DOS)

Since the difference in the noise behavior between large grain and small grain samples is explained based on the differences in the number of deep traps at grain boundaries, it is important to confirm that the sample with smaller grains has a higher density of deep level traps or states by comparing the density of states. Thus, we conducted a density of state measurement based on Horowitz's method which assumes a double exponential distribution of states.[17], [18] Based on the method, the information about traps or available states at different energy levels within the bandgap can be obtained from I-V characteristics at different temperatures because carriers that were trapped at different energy levels can be activated and become free carriers with the additional thermal energy. Since we are interested in differences in deep trap levels, we extracted the DOS information from I-V measurements at high temperatures up to 100 °C, which are shown in **Figure 5.7**. The DOS of large and small grains is shown in **Figure 5.8**. $N_{t0,1}$=10^{13} cm^{-2}, $T_{c,1}$=100 K, and $N_{t0,2}$=5×10^{12} cm^{-2} are the common parameters for both samples in the double exponential distribution equation written as

$$N_t(E) = \sum_{i=1}^{2} \frac{N_{t0,i}}{kT_{c,i}} \exp\left(-\frac{E_t - E_V}{kT_{c,i}}\right). \quad (2)$$

$T_{c,2}$, which determines the slope of deep states, is 700 K for 1L and 1100 K for 1S. Thus, we can clearly observe that the sample 1S, which has smaller grains that the large grain sample 1L, has a similar tail state distribution, but has a higher concentration of deep states. Therefore, these results are consistent with expectations based on the aforementioned noise measurements. All the detail parameters are listed in **Table 5.1**.

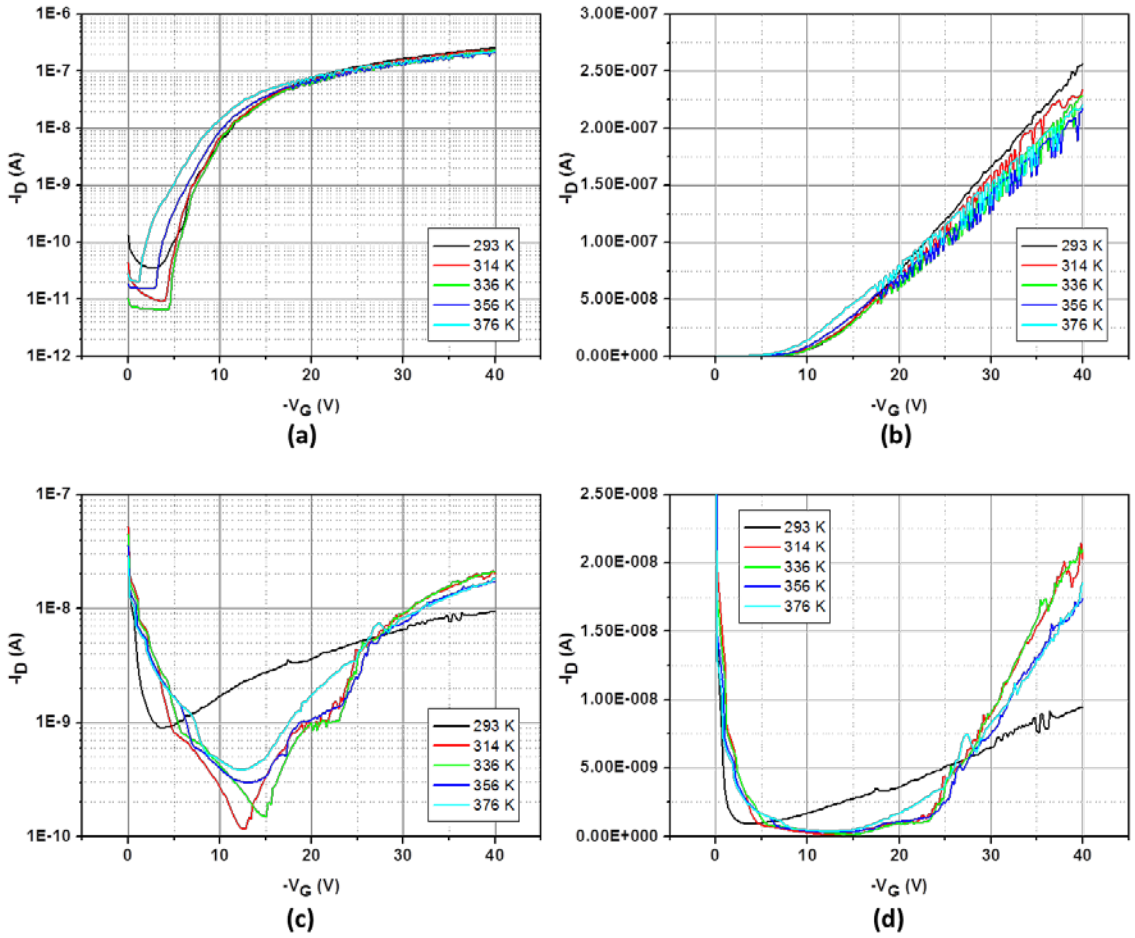


Figure 5.7 Transfer characteristics of TFTs (1L: (a) and (b), 1S: (c) and (d)) at different substrate temperatures.

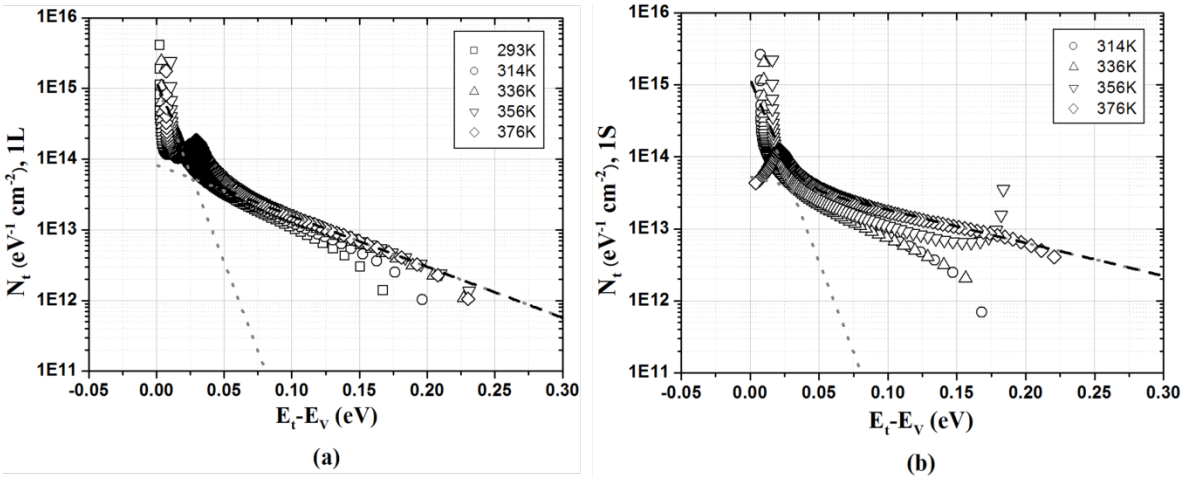


Figure 5.8 Density of states in pentacene for (a) 1L (large grain) and (b) 1S (small grain) based on Horowitz's method. For the plot, I-V characteristics of TFTs were measured at different temperatures from room temperature to 100 °C. Dotted lines represent double exponential distribution of traps; two gray dotted lines for each exponential distribution, and one black dashed line for the sum of the two distributions.

	1L	*1S*
$\mu_0 N_c$ ($V^{-1}s^{-1}$)	**2.5E10**	**2E9**
$N_{t0,1}$ (cm^{-2})	1E13	
$T_{c,1}$ (K)	100	
$N_{t0,2}$ (cm^{-2})	5E12	
$T_{c,2}$ (K)	**700**	**1100**

Table 5.1 Parameters used in Equation (2) for good fitting of the model. As a fitting parameter, $\mu_o N_c$ is selected as 2.5×10^{10} $V^{-1}s^{-1}$ for (a) and 2.0×10^{9} $V^{-1}s^{-1}$. The one order difference is reasonable considering that the mobility of 1L is one order higher than 1S.

5.3 Low-frequency noise under ac bias

5.3.1 Background

In addition to 1/f noise measurement under DC bias, it has been known that the measurement of 1/f noise under switched gate bias is a very useful method to both estimate the behavior of the flicker noise during actual operation and to gain further insight into the physical underpinnings of the flicker noise. The noise signal under AC gate bias is especially important for OTFTs since pass transistor logic based designs (in which a square wave clock signal is applied to the transmission gate terminal) are suggested to be beneficial for OTFTs because lower number of transistors are required. Additionally, the resulting reduced depth layouts result in faster circuit operation compared to logic gate based design.[19]–[21] 1/f noise under switched bias is also known to affect the phase noise in RF applications, which is very important when considering OTFT usage in low-cost radio-frequency identification tags (RFID).[22], [23]

Since switching the channel of the transistors on and off affects the mechanism of the 1/f noise generation, the actual noise signal generated under switched bias is in fact often found to be different from the noise measured under DC bias. Previous studies on flicker noise under switched signals in conventional MOSFETs showed that 1/f noise below the frequency of the switching gate signal (f_{switch}) decreases and deviates from ideal 1/f behavior observed under dc bias.[23]–[26] In some cases, the noise level below f_{switch} has been observed to flatten, and finally, at still lower frequencies, has been found to approach 1/f like behavior.[23]–[25] In other cases, instead of flattening, the noise level below f_{switch} has been observed to remain 1/f noise, but with a lower slope.[25], [26] It has been concluded for both cases that the deviation is due to the reduction of the carrier number fluctuation (Δn), caused by the disappearance of carriers when the transistor channel is turned off. This hypothesis was further confirmed in deep-submicron MOSFETs. When a Lorentzian distribution of random telegraph signal noise (RTS)—the trapping-emission signal that is due to a single trap—is observed in deep-submicron devices, the Lorentzian curve below f_{switch} is almost completely flattened[25], [27], [28] This indicates that the traps can be deactivated when the gate signal switches and removes carriers faster than the capturing process. To our best knowledge, the measurement of 1/f noise in OTFTs under

switched gate bias has not yet been conducted and analyzed, leaving an important gap in our knowledge to this point. To address this shortcoming, in this section, we present our observation of flicker noise in OTFTs under AC gate bias.

5.3.2 Experiment setup

5.3.2.1 Solution-processed polymer TFTs

Solution-processed OTFTs were used in this work to be consistent with expected target application processes. The solution processed OTFTs used in this experiment were fabricated as follows. For convenience and to assure good reproducibility, a heavily doped n-type silicon wafer was used as the bottom gate contact. The gate insulator of the OTFTs consists of a bilayer structure of thermally oxidized silicon dioxide (100 nm) and spin-coated poly-4-vinylphenol (PVP) (170 nm), ensuring excellent reproducibility while mimicking the polymer gate dielectric interface typically seen in fully-printed devices. The PVP polymer dissolved in propylene glycol monomethyl ether acetate was pre-mixed with poly(melamine-co-formaldehyde) as a cross-linker, and cross-linked at 210 °C for 10 min after spin-coating. The PVP layer is used to replicate the interface between polymer dielectric layer and organic semiconductor, which is common in fully printed OTFTs.[29]–[32] The source and drain contacts were inkjet printed with silver nanoparticle based ink, Cabot CCI-300, followed by a sintering process at 150 °C for 20 min. The channel length and width of the OTFTs are defined as 100 µm and 400 µm, respectively. Lastly, a solution processed polymer organic semiconductor, pBTTT (used in Chapter 4), was used as the semiconductor material in the OTFTs. The pBTTT layer was spin-coated and annealed under nitrogen at 130 °C for 10 min. After the annealing, the OTFTs were slowly cooled down to room temperature at a rate of -10 °C per min. The fabricated OTFTs show field-effect mobilities in linear and saturation of 0.025 and 0.028 respectively, consistent with other reports for this material system.[30], [31], [33], [34] The transfer and output characteristics of the OTFTs are provided in **Figure 5.9** along with an AFM image of the pBTTT semiconductor layer.

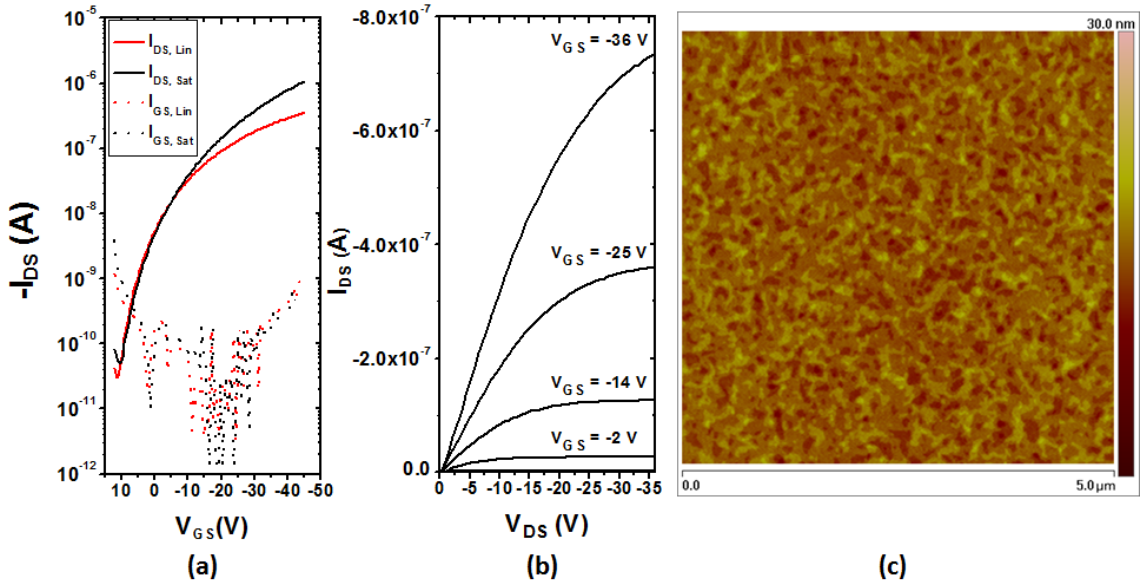


Figure 5.9 (a) Transfer and (b) output characteristics of pBTTT OTFTs measured. (c) An AFM image of the deposited pBTTT layer in the OTFTs (scan area: 5 µm by 5 µm; z range: up to 30 nm).

5.3.2.2 Low-frequency noise measurement under ac bias configuration

The 1/f noise measurement configuration used in the previous section cannot be used for the measurement under ac bias since (1) the input gate bias must be replaced to ac signal and (2) the low pass filter used will remove the ac signal. Therefore, a different noise measurement configuration is set up. The 1/f noise of the OTFTs was measured as the voltage fluctuation across a load resistor in the drain current path. As shown in **Figure 5.10**, DC bias was applied between the source and drain of the OTFTs. A square wave voltage signal generated by a function generator with amplification by an op-amp was applied to the gate terminal of the OTFTs. The drain current noise generated within the channel of the OTFTs is converted to the fluctuation of the voltage across a 10 kΩ load resistor. The voltage fluctuation is then amplified by a low noise amplifier, BTA9812B with a gain of 500 V/V, and monitored by a dynamic signal analyzer, HP 35670A.

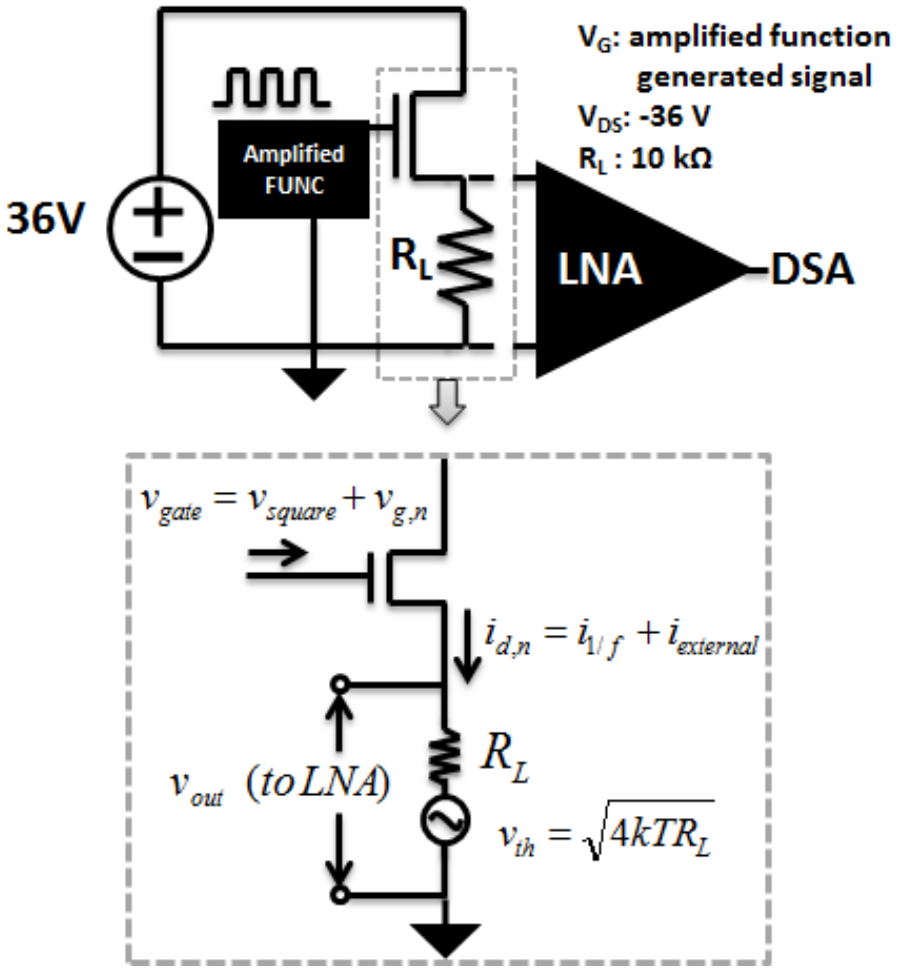


Figure 5.10 The configuration of the 1/f noise measurement under switched gate bias.

5.3.3 Experiment results

The results of the LFN measurement of the OTFTs under switched bias are provided in **Figure 5.11(a)**. The source and drain voltages, V_S and V_D, are set to 36 V and 0 V respectively. The square wave gate voltage (V_G) with f_{switch} of 300 Hz has a peak-to-peak voltage (V_{pp}) varied from 0V to maximum 36 V while keeping the minimum peak value as 0 V. When the OTFTs were operated under purely DC conditions, the measured power spectral density (PSD) of the drain current noise showed typical 1/f like behavior. However, as the switching gate bias is applied by increasing V_{pp}, the noise at lower frequencies decreases while the noise at higher frequency increases.

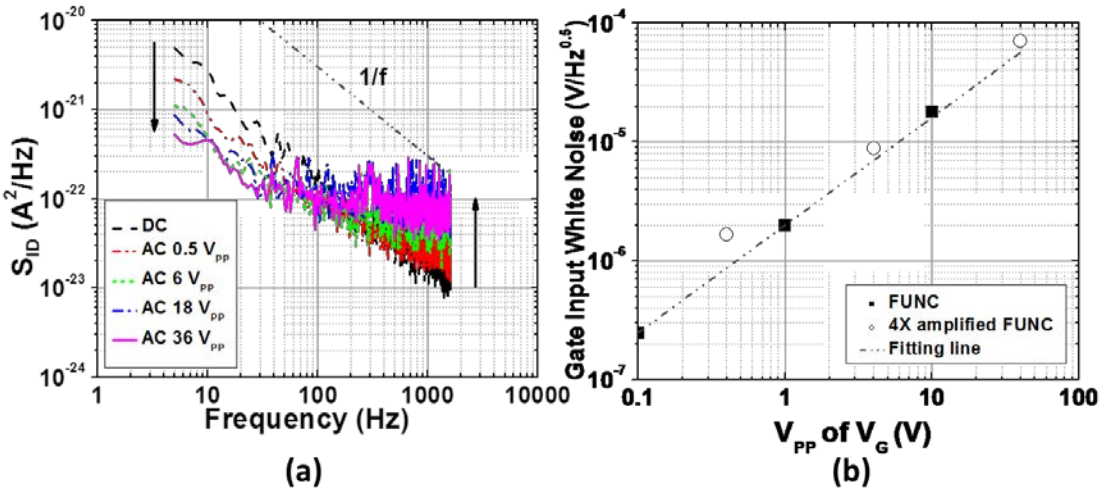


Figure 5.11 (a) The power spectral density of the drain current when the pBTTT TFTs are under switching gate bias. For the switched bias, the peak-to-peak voltage (V_{PP}) is varied from 500 mV to 36 V. The measured PSD is averaged from 20 data. (b) The background white noise of the input switching gate signal generated from the amplified function generator. The white noise increases as the peak-to-peak voltage of the input gate signal increases.

The increase of the noise in the higher frequency range is believed to be caused by the background noise within the input AC signal. Although the input square wave voltage signal has a reasonably high SNR, background white noise always exists. The background noise of the gate input signal adds additional drain current noise through transconductance (g_m). Therefore, in this measurement setup, the voltage noise measured across the load resistor is,

$$\begin{aligned} v_{R_L} &= R_L \cdot i_{DS,noise} + v_{thermal} \\ &= R_L (i_{1/f} + g_m v_{G,noise}) + \sqrt{4kT \cdot R_L} \end{aligned} \tag{3}$$

where R_L is the resistance of load resistor, k is Boltzmann constant, and T is absolute temperature. The thermal noise ($v_{thermal}$) generated from the 10 kΩ load resistor can only generate about 1 pA white noise which is orders of magnitude smaller than the other sources. As the amplitude of the square wave gate signal increases, the background white noise that is coupled by g_m also linearly increases as shown in **Figure 5.11(b)**. Considering the range of g_m is 6×10^{-9} ~ 8×10^{-8} (A/V) for the gate voltage biases during this measurement, the PSD of the drain current noise coupled with the input white noise can increase up to an order of 10^{-22} (A^2/Hz). This can thus explain the increase of the drain current noise at higher frequencies when the amplitude of the gate input signal increases.

The decrease of the drain current noise in the lower frequency range, however, can only be explained by the change of the flicker noise component ($i_{1/f}$) in equation (3) since other components in (3) are either small or showing the opposite trend. More importantly, the decrease of the 1/f noise under switched gate bias provides strong evidence that the dominant mechanism of the flicker noise in OTFTs is the fluctuation of the number of carriers. Of the two possible sources of 1/f noise, Δμ and Δn, if Δμ due to the grain

boundaries were to be the dominant source of the 1/f noise in our OTFTs as reported by others,[8], [9] then the noise level would have increased because the switching to weaker gate bias in fact makes the energy barriers formed at grain boundaries even higher than when strong gate bias is applied.[35] Therefore, the stronger disturbance of the carrier transport by the energy barriers and thus increased mobility fluctuation would be expected when the OTFTs are under switched gate bias. On the other hand, as the input gate voltage switches from accumulation to depletion, the carriers accumulated within the channel disappear. Thus, the number of carriers that could potentially be trapped by the various traps within the semiconductor should also decrease, resulting in a decrease of the 1/f noise. This hypothesis based on the Δn model agrees with our observation in **Figure 5.11(a)**. This observation and the analysis based upon the Δn model also agree with the previously discussed works on conventional MOSFETs. It is important to note that from this experiment, it is not clear why the resurgence of 1/f like behavior in much lower frequency domains is observed instead of showing a complete plateau. It has been suggested that this could be caused by a different mechanism of 1/f noise, such as Δμ model which was shadowed by the Δn mechanism.[24], [25] Others have proposed that it is because the carriers and traps that are farther from the channel are less affected by the change of the gate bias.[36] Further in-depth investigation is needed to understand the residual noise below f_{switch}.

To date, it has not been possible to clearly prove that the Δμ model does not play a main role since DC measurements do not allow for unequivocal discrimination between the Δμ and Δn effects. Since the Δμ model in equation (1) is an empirical model from experiments with homogeneous materials, an application of the model to different device structures is challenging. However, in this 1/f noise measurement under switched gate bias, the Δn model and the Δμ model can be experimentally compared since the outcomes are expected to be different.

5.4 Low-frequency noise of printed OTFTs

For further confirmation of the dominance of the Δn mechanism and its applicability to fully printed OTFTs, the 1/f noise of gravure-printed pBTTT TFTs shown in Chapter 4 was measured in both linear and saturation regions, and the exponent values in $1/f^{\gamma}$ of the two regions are compared as suggested in the earlier part of this chapter. As similarly observed previously in the vacuum-processed pentacene TFTs above, the exponent values are higher in saturation mode than in the low drain bias linear region as shown in **Figure 5.12**. Note that the difference is smaller than in the case of the pentacene TFTs due to the better quality of the semiconductor crystalline structure, which leads to possibly lower deep trap state concentration and thus orders of magnitude higher field-effect mobility.

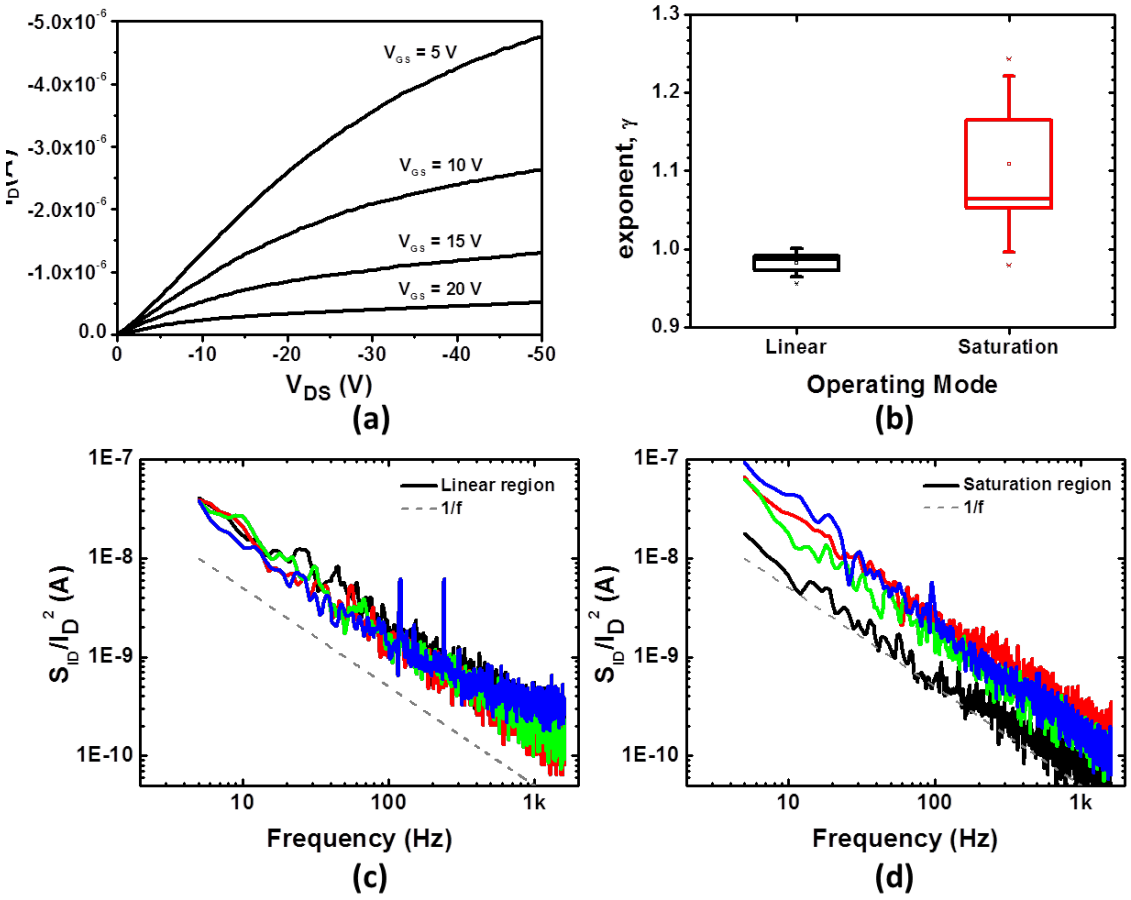


Figure 5.12 (a) Output characteristic of the gravure printed pBTTT TFTs in [31]. (b) Distribution of exponent values of $1/f^{\gamma}$ in the LFN of the TFTs in (a). The exponent values are extracted within the frequency range of 5 Hz to 100 Hz in order to minimize the effect of the chamber noise (c) PSD of the LFN in the TFTs of (a) in linear region and (d) in saturation region.

5.5 Application of the unified noise model

To allow for the deployment of organic transistors in noise-sensitive applications, it is important to develop an analytical noise model to enable more accurate simulation. Hung et al. developed a unified flicker noise model for MOSFETs as shown in

$$\frac{S_{I_D}}{I_D^{\,2}} = \left(1 + \alpha\mu_{eff} C_{ox} \frac{I_D}{g_m}\right)^2 \frac{g_m^{\,2}}{I_D^{\,2}} S_{V_{fb}}, \tag{4}$$

where $S_{Vfb}=S_{Qss}/(WLC_{ox}^{\,2})$ and $S_{Qss}=A/f^{\gamma}$, A is constant [3]. Although there is a method to distinguish the origin of the noise by comparing the slope in $S_{ID}/I_D^{\,2}$ – I_D plot [5], our observed results cannot be explained by either only the phonon induced mobility fluctuation or carrier number fluctuation. However, the model in (4) with appropriate fitting parameters can explain our results, as shown in **Figure 5.13**. The steep slope in the plot was

well fitted by the model when $\alpha\mu_{eff}C_{ox}I_D/g_m$ in (4) is close to -1. This factor represents mobility fluctuation that is caused by trapped charges through coulombic scattering. Since there are acceptor-like traps at the GBs of pentacene [37] and the traps become neutral with stronger gate field [35], the mobility fluctuation due to coulombic scattering is reduced and thus the total noise also becomes smaller. After the exponent, γ, is determined by the operating mode and the experimentally measured DOS of the semiconductor, the drain current spectral density can be modeled by the equation in (4).

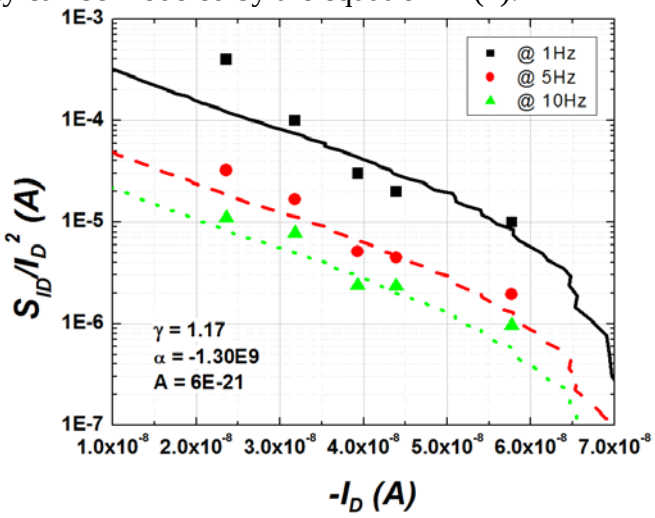


Figure 5.13 Application of the Unified Noise Model to the normalized drain current spectral density of the sample 1L in the linear region. γ is from the spectral density measurement, and other constants in (4) are fitting parameters.

5.6 Summary

Firstly, the effects of pentacene grain size, thickness, and device operating region on the low frequency noise of organic TFTs under dc bias are studied. It is found that significant differences in the slope of the drain current spectral density for different operating regions and for different channel grain sizes. These experimental results can only be explained by fluctuations in carrier concentration. Unlike conventional MOSFETs, various types of traps within the disordered organic semiconductor are the main source of the carrier trapping/de-trapping. Specifically, acceptor-like deep traps at grain boundaries lead to a steeper slope in the drain current spectral density when the traps are unfilled. Thus, we observed and explained a difference in the noise characteristics between linear and saturation mode. For devices with higher deep trap concentrations, a steeper slope was observed even in the linear mode due to the greater effect of trapping by these deep states.

Secondly, the 1/f noise of polymer based OTFTs was measured under switched gate bias conditions. The 1/f noise decreases as the gate switches between accumulation mode and depletion mode. This observation supports the hypothesis that the number of carrier fluctuation is the main source of 1/f noise in OTFTs. This is further confirmed by 1/f noise measurement under DC bias as well.

Further, it is shown that the unified noise model which has been analytically derived for conventional MOSFETs can be applied to OTFTs with a notable feature which reveals that there is an additional mobility fluctuation induced by acceptor-like traps in the semiconductor through coulombic scattering. Thus, we suggest that a structure-dependent exponent term that describes the carrier density fluctuation and coulomb scattering-based mobility fluctuation should be used to explain and estimate the low frequency noise of OTFTs.

5.7 References

[1] J. K. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard, "Integrated nanopore sensing platform with sub-microsecond temporal resolution," *Nat Meth*, vol. 9, no. 5, pp. 487–492, May 2012.

[2] A. van der Ziel, "Unified presentation of 1/f noise in electron devices: fundamental 1/f noise sources," *Proceedings of the IEEE*, vol. 76, no. 3, pp. 233–258, 1988.

[3] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *Electron Devices, IEEE Transactions on*, vol. 37, no. 3, pp. 654–665, 1990.

[4] S. Christensson, I. Lundström, and C. Svensson, "Low frequency noise in MOS transistors--I Theory," *Solid-State Electronics*, vol. 11, no. 9, pp. 797–812, Sep. 1968.

[5] D. Rigaud, M. Valenza, and J. Rhayem, "Low frequency noise in thin film transistors," *Circuits, Devices and Systems, IEE Proceedings* -, vol. 149, no. 1, pp. 75–82, 2002.

[6] L. K. J. Vandamme, R. Feyaerts, G. Trefán, and C. Detcheverry, "1/f noise in pentacene and poly-thienylene vinylene thin film transistors," *J. Appl. Phys.*, vol. 91, no. 2, p. 719, 2002.

[7] Zhang Jia, I. Meric, K. L. Shepard, and I. Kymissis, "Doping and Illumination Dependence of \hbox {1}/f Noise in Pentacene Thin-Film Transistors," *Electron Device Letters, IEEE*, vol. 31, no. 9, pp. 1050–1052, 2010.

[8] O. Marinov, M. J. Deen, J. Yu, G. Vamvounis, S. Holdcroft, and W. Woods, "Low-frequency noise in polymer thin-film transistors," *Circuits, Devices and Systems, IEE Proceedings* -, vol. 151, no. 5, pp. 466–472, 2004.

[9] B. R. Conrad, W. G. Cullen, W. Yan, and E. D. Williams, "Percolative effects on noise in pentacene transistors," *Appl. Phys. Lett.*, vol. 91, no. 24, p. 242110, 2007.

[10] S. Martin, A. Dodabalapur, Z. Bao, B. Crone, H. E. Katz, W. Li, A. Passner, and J. A. Rogers, "Flicker noise properties of organic thin-film transistors," *J. Appl. Phys.*, vol. 87, no. 7, p. 3381, 2000.

[11] O. D. Jurchescu, B. H. Hamadani, H. D. Xiong, S. K. Park, S. Subramanian, N. M. Zimmerman, J. E. Anthony, T. N. Jackson, and D. J. Gundlach, "Correlation between microstructure, electronic properties and flicker noise in organic thin film transistors," *Appl. Phys. Lett.*, vol. 92, no. 13, p. 132103, 2008.

[12] Lin Ke, S. Bin Dolmanan, C. Vijila, Soo Jin Chua, Ye Hua Han, and Ting Mei, "Investigation of the Device Degradation Mechanism in Pentacene-Based Thin-Film Transistors Using Low-Frequency-Noise Spectroscopy," *Electron Devices, IEEE Transactions on*, vol. 57, no. 2, pp. 385–390, 2010.

[13] L. Ke, S. B. Dolmanan, L. Shen, C. Vijila, S. J. Chua, R.-Q. Png, P.-J. Chia, L.-L. Chua, and P. K.-H. Ho, "Low frequency noise analysis on organic thin film transistors," *J. Appl. Phys.*, vol. 104, no. 12, p. 124502, 2008.

[14] L. Jagannathan and V. Subramanian, "DNA detection using organic thin film transistors: Optimization of DNA immobilization and sensor sensitivity," *Biosensors and Bioelectronics*, vol. 25, no. 2, pp. 288–293, Oct. 2009.

[15] C. A. Dimitriadis, J. Brini, G. Kamarinos, and G. Ghibaudo, “Characterization of Low-Pressure Chemical Vapor Deposited Polycrystalline Silicon Thin-Film Transistors by Low-Frequency Noise Measurements,” *Jpn. J. Appl. Phys.*, vol. 37, no. Part 1, No. 1, pp. 72–77, Jan. 1998.

[16] C. T. Sah, “Theory of low-frequency generation noise in junction-gate field-effect transistors,” *Proceedings of the IEEE*, vol. 52, no. 7, pp. 795–814, 1964.

[17] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, “Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors,” *J. Appl. Phys.*, vol. 87, no. 9, p. 4456, 2000.

[18] G. Horowitz, R. Hajlaoui, and P. Delannoy, “Temperature Dependence of the Field-Effect Mobility of Sexithiophene. Determination of the Density of Traps,” *J. Phys. III France*, vol. 5, no. 4, pp. 355–371, Apr. 1995.

[19] B. Yoo, B. A. Jones, D. Basu, D. Fine, T. Jung, S. Mohapatra, A. Facchetti, K. Dimmler, M. R. Wasielewski, T. J. Marks, and A. Dodabalapur, “High-Performance Solution-Deposited n-Channel Organic Transistors and their Complementary Circuits,” *Advanced Materials*, vol. 19, no. 22, pp. 4028–4032, 2007.

[20] B. Crone, A. Dodabalapur, Y.-Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, and W. Li, “Large-scale complementary integrated circuits based on organic transistors,” *Nature*, vol. 403, no. 6769, pp. 521–523, Feb. 2000.

[21] B. Crone, A. Dodabalapur, J. Rogers, S. Martin, R. Filas, Yen-Yi Lin, Z. Bao, R. Sarpeshkar, Wenjie Li, and H. Katz, “Novel fabrication methods and characteristics of organic complementary circuits,” in *Electron Devices Meeting, 1999. IEDM Technical Digest. International*, 1999, pp. 115–118.

[22] H. Tian and A. El Gamal, “Analysis of 1/f noise in switched MOSFET circuits,” *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 48, no. 2, pp. 151–157, 2001.

[23] S. L. J. Gierkink, E. A. M. Klumperink, A. P. van der Wel, G. Hoogzaad, E. A. J. M. van Tuijl, and B. Nauta, “Intrinsic 1/f device noise reduction and its effect on phase noise in CMOS ring oscillators,” *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 7, pp. 1022–1025, 1999.

[24] I. Bloom and Y. Nemirovsky, “1/ f noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation,” *Applied Physics Letters*, vol. 58, no. 15, pp. 1664–1666, Apr. 1991.

[25] B. Dierickx and E. Simoen, “The decrease of ‘“random telegraph signal”’ noise in metal-oxide-semiconductor field-effect transistors when cycled from inversion to accumulation,” *J. Appl. Phys.*, vol. 71, no. 4, p. 2028, 1992.

[26] A. P. van der Wel, E. A. M. Klumperink, S. L. J. Gierkink, R. F. Wassenaar, and H. Wallinga, “MOSFET 1/f noise measurement under switched bias conditions,” *Electron Device Letters, IEEE*, vol. 21, no. 1, pp. 43–46, 2000.

[27] A. P. van der Wel, E. A. M. Klumperink, and B. Nauta, “Effect of switched biasing on 1/f noise and random telegraph signals in deep-submicron MOSFETs,” *Electronics Letters*, vol. 37, no. 1, pp. 55–56, 2001.

[28] A. P. van der Wel, E. A. M. Klumperink, L. K. J. Vandamme, and B. Nauta, “Modeling random telegraph noise under switched bias conditions using cyclostationary RTS noise,” *IEEE Transactions on Electron Devices*, vol. 50, no. 5, pp. 1378 – 1384, May 2003.
[29] H.-Y. Tseng and V. Subramanian, “All inkjet-printed, fully self-aligned transistors for low-cost circuit applications,” *Organic Electronics*, vol. 12, no. 2, pp. 249–256, Feb. 2011.
[30] A. de la Fuente Vornbrock, D. Sung, H. Kang, R. Kitsomboonloha, and V. Subramanian, “Fully gravure and ink-jet printed high speed pBTTT organic thin film transistors,” *Organic Electronics*, vol. 11, no. 12, pp. 2037–2044, Dec. 2010.
[31] H. Kang, R. Kitsomboonloha, J. Jang, and V. Subramanian, “High-Performance Printed Transistors Realized Using Femtoliter Gravure-Printed Sub-10 μm Metallic Nanoparticle Patterns and Highly Uniform Polymer Dielectric and Semiconductor Layers,” *Advanced Materials*, vol. 24, no. 22, pp. 3065–3069, 2012.
[32] F.-C. Chen, C.-W. Chu, J. He, Y. Yang, and J.-L. Lin, “Organic thin-film transistors with nanocomposite dielectric gate insulator,” *Applied Physics Letters*, vol. 85, no. 15, pp. 3295–3297, Oct. 2004.
[33] N. Zhao, Y.-Y. Noh, J.-F. Chang, M. Heeney, I. McCulloch, and H. Sirringhaus, “Polaron Localization at Interfaces in High-Mobility Microcrystalline Conjugated Polymers,” *Advanced Materials*, vol. 21, no. 37, pp. 3759–3763, 2009.
[34] Y. Takeda, Y. Yoshimura, Y. Kobayashi, D. Kumaki, K. Fukuda, and S. Tokito, “Integrated circuits using fully solution-processed organic TFT devices with printed silver electrodes,” *Organic Electronics*.
[35] A. B. Chwang and C. D. Frisbie, “Temperature and gate voltage dependent transport across a single organic semiconductor grain boundary,” *J. Appl. Phys.*, vol. 90, no. 3, p. 1342, 2001.
[36] M. Miguez and A. Arnaud, “A Study Of Flicker Noise In MOS Transistor Under Switched Bias Condition,” *ECS Trans.*, vol. 9, no. 1, pp. 313–322, Sep. 2007.
[37] S. Yogev, R. Matsubara, M. Nakamura, and Y. Rosenwaks, “Local charge accumulation and trapping in grain boundaries of pentacene thin film transistors,” *Organic Electronics*, vol. 11, no. 11, pp. 1729–1735, Nov. 2010.

Chapter 6

Conclusions and Future work

6.1 Summary and key contributions

In this dissertation, significant technological improvement and in-depth understanding of various important aspects of printed electronics were presented. Key contributions are as follows. In Chapter 2, how contact angle hysteresis affects printed pattern formation is studied. It is both experimentally and theoretically confirmed that the contact angle hysteresis puts a limitation on the size of the achievable printed films. If the contact angle of the printed films is larger than the advancing contact angle, then bulging is observed. On the other hand, if the contact angle falls below the receding contact angle, then the films are separated into smaller films. A simple hydrostatic model is developed to anticipate the completeness of inkjet-printed films, and its effectiveness is experimentally confirmed with inkjet-printed polymer films. Based on the lesson we have learnt, the effects of printing parameters on the shape of gravure-printed films were also studied. With the optimization of the contact angles of the ink on a chosen plastic substrate, high-quality polymer films of various sizes with sharp corners are successfully gravure-printed. In Chapter 3, gravure-printed conductive lines are scaled down below 5 μm by using a novel electromechanical engraving method. Minimized cell-to-cell variation of the engraved patterns led to small line edge roughness (<1μm) as well. High metal concentration and small size of nanoparticles in the metal inks are found to be very critical for highly scaled gravure-printed metal electrodes to be used in printed TFTs. In Chapter 4, high-performance gravure-printed TFTs are demonstrated by using the high-resolution gravure-printed metal lines developed in Chapter 3 as bottom-gate electrodes. In addition to the scaling of the channel length down to 5 μm with minimized parasitic capacitances, proper electrical scaling is pursued to reduce the operating voltage down to 5 V. The mobility of the organic semiconductors in the gravure-printed TFTs is optimized to deliver 0.5 $cm^2V^{-1}s^{-1}$ on average, resulting in the operation of the transistors and inverters beyond 1 MHz. In Chapter 5, the origin of 1/f noise in OTFTs was studied under both dc and ac operating conditions. Non-ideal behaviors of the observed 1/f noise with respect to the various semiconductor qualities and bias conditions suggest that the dominant mechanism of the 1/f

noise in OTFTs is the trapping/de-trapping of carriers by/from the traps within the semiconductor film.

The technology developed in this dissertation certainly provides significant improvement in the performance of demonstrated printed electronics. As shown in **Figure 6.1**, orders of magnitude higher speed of roll-to-roll printed transistors and circuits are demonstrated. In addition to the technology improvement, the in-depth knowledge discovered in the printing processes and the low-frequency noise of OTFTs would certainly help printed electronics become more matured.

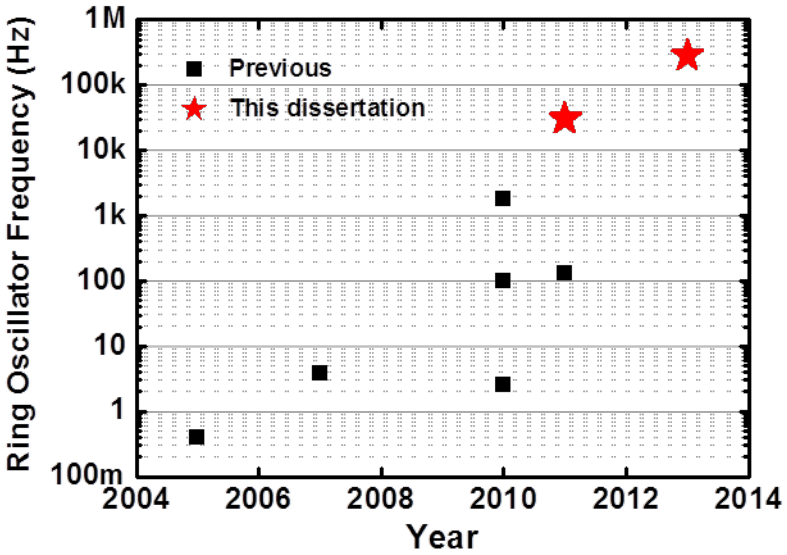


Figure 6.1 Ring oscillator frequency of reported R2R printed ring oscillators.[1]–[6] Our data only showed TFTs or inverters. Therefore, 1/10 of f_T and $1/t_p$ are plotted as comparison with circuits.

6.2 Future work

While significant progress has been made toward fully gravure-printed integrated circuits in this dissertation, there are still many tasks left for further improvement. First of all, better understanding of the gravure-printing process is needed. Gravure printing is a much more complex process than the inkjet printing that is well studied. Therefore, in order to develop more generalized models that can accurately estimate how much ink is printed and further anticipate the completeness of printed patterns, every step in the entire gravure-printing process such as ink filling, doctor blading or ink transfer must be fully understood. To do that, it is important to study each mechanism both experimentally and theoretically.

Secondly, further scaling of the gravure-printed lines can be pursued. As demonstrated in this dissertation, high-quality engraving of the patterns is the key for the scaling of the gravure-printed features. Therefore, developing other engraving techniques that can pattern even smaller features than 2.5 μm would enable further scaling of the printed TFTs. However, as the printed patterns become smaller, the thickness of the features becomes comparable to the thickness of residue generated during printing. Therefore, the reduction of the undesired residue must be accompanied by the further scaling of the gravure-printed

lines. To do so, the physical mechanism of the residue generation must be understood. Especially, the doctor blade wiping in gravure printing is found to be very important.[7]–[9] Better surface polishing of the gravure roll master can also help minimization of the undesired residue formation.

For the printed transistors in this dissertation, S/D electrodes are inkjet-printed in order to obtain good alignment to the gate electrodes. However, for fully gravure-printed ICs, it is necessary to overcome the poorer alignment of roll-to-roll printing.[10] While further improvement of the registration accuracy of the R2R printings can be pursued by better precision mechanics, perfect alignment to our highly scaled lines is very challenging. The self-alignment technique developed by Tseng et al can possibly be integrated with R2R printing since the technique only requires surface energy modification only on the channel area. Therefore, the adoption of the self-alignment technique to our highly scaled gravure-printed features could be a solution to overcome the alignment issue. The change of the transistor structure can also establish entirely R2R compatible fabrication processes. Instead of using the highly scaled lines as the gate electrode, the lines can be used as S/D electrodes for both bottom and top gate TFTs. Then, wide gate electrodes (larger than the registration inaccuracy) can be gravure-printed to fully overlap the highly scaled S/D lines to ensure good gate control in the transistors. Though the full S/D overlap slows down the transistor operation, the highly scaled S/D lines still provides much smaller parasitic capacitances than when S/D electrodes are also wide as seen from previous reports. In addition, the semiconductors need to be optimized to be compatible with the gravure-printing process. High mobility n-type semiconductors must also be introduced for our printing processes in order to fabricate CMOS circuits instead of the p-type only configurations demonstrated in this dissertation. Lastly, both dielectric and semiconductor layers must be properly patterned by gravure printing for better isolation of the devices.

For the study of the noise in printed transistors, a broader spectrum of the noise signal in OTFTs needs to be studied. For wide bandwidth applications (e.g. high temporal resolution), how the noise signal in the OTFTs changes in higher frequency ranges is important since it determines the bandwidth of the printed sensors. More specifically, the corner frequency—at which the 1/f noise becomes comparable to the thermal noise—needs to be characterized. The characteristics of the noise signal beyond the corner frequency, which can be affected by the parasitic of the printed transistors, must be characterized as well.[11] Moreover, how 1/f noise affects the phase noise of the oscillators in organic transistors and circuits needs in-depth analysis for their usage in various applications.[12], [13]

In sum, more studies can be done in the near future for the realization of fully printed electronics applications mentioned in Chapter 1. This dissertation can thus drive greater innovation to reach the goals of the printed electronics community.

6.3 References

[1] D. Zielke, A. C. Hubler, U. Hahn, N. Brandt, M. Bartzsch, U. Fugmann, T. Fischer, J. Veres, and S. Ogier, "Polymer-based organic field-effect transistor using offset printed source/drain structures," *Appl. Phys. Lett.*, vol. 87, no. 12, pp. 123508–3, 2005.

[2] G. C. Schmidt, M. Bellmann, B. Meier, M. Hambsch, K. Reuter, H. Kempa, and A. C. Hübler, "Modified mass printing technique for the realization of source/drain electrodes with high resolution," *Organic Electronics*, vol. 11, no. 10, pp. 1683–1687, Oct. 2010.

[3] M. Hambsch, K. Reuter, M. Stanel, G. Schmidt, H. Kempa, U. Fügmann, U. Hahn, and A. C. Hübler, "Uniformity of fully gravure printed organic field-effect transistors," *Materials Science and Engineering: B*, vol. 170, no. 1–3, pp. 93–98, Jun. 2010.

[4] A. C. Huebler, F. Doetz, H. Kempa, H. E. Katz, M. Bartzsch, N. Brandt, I. Hennig, U. Fuegmann, S. Vaidyanathan, J. Granstrom, S. Liu, A. Sydorenko, T. Zillger, G. Schmidt, K. Preissler, E. Reichmanis, P. Eckerle, F. Richter, T. Fischer, and U. Hahn, "Ring oscillator fabricated completely by means of mass-printing technologies," *Organic Electronics*, vol. 8, no. 5, pp. 480–486, Oct. 2007.

[5] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, J. M. Tour, and G. Cho, "All-Printed and Roll-to-Roll-Printable 13.56-MHz-Operated 1-bit RF Tag on Plastic Foils," *IEEE Transactions on Electron Devices*, vol. 57, no. 3, pp. 571–580, 2010.

[6] A. de la Fuente Vornbrock, D. Sung, H. Kang, R. Kitsomboonloha, and V. Subramanian, "Fully gravure and ink-jet printed high speed pBTTT organic thin film transistors," *Organic Electronics*, vol. 11, no. 12, pp. 2037–2044, Dec. 2010.

[7] R. Kitsomboonloha, U. Ceyhan, S. J. S. Morris, and V. Subramanian, "Experimental study of the residue film in direct gravure printing of electronics," in *Bulletin of the American Physical Society*, 2012, vol. Volume 57, Number 17.

[8] R. Kitsomboonloha, S. J. S. Morris, X. Rong, and V. Subramanian, "Femtoliter-Scale Patterning by High-Speed, Highly Scaled Inverse Gravure Printing," *Langmuir*, vol. 28, no. 48, pp. 16711–16723, Dec. 2012.

[9] U. Ceyhan, R. Kitsomboonloha, S. J. S. Morris, and V. Subramanian, "Lubrication analysis of the nanometric coating film deposited during gravure printing," in *Bulletin of the American Physical Society*, 2012, vol. Volume 57, Number 17.

[10] Jinsoo Noh, Dongsun Yeom, Chaemin Lim, Hwajin Cha, Jukyung Han, Junseok Kim, Yongsu Park, V. Subramanian, and Gyoujin Cho, "Scalability of Roll-to-Roll Gravure-Printed Electrodes on Plastic Foils," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 33, no. 4, pp. 275–283, Oct. 2010.

[11] J. K. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard, "Integrated nanopore sensing platform with sub-microsecond temporal resolution," *Nat Meth*, vol. 9, no. 5, pp. 487–492, May 2012.

[12] H. Tian and A. El Gamal, "Analysis of 1/f noise in switched MOSFET circuits," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 48, no. 2, pp. 151–157, 2001.

[13] S. L. J. Gierkink, E. A. M. Klumperink, A. P. van der Wel, G. Hoogzaad, E. A. J. M. van Tuijl, and B. Nauta, “Intrinsic 1/f device noise reduction and its effect on phase noise in CMOS ring oscillators,” *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 7, pp. 1022–1025, 1999.