Thin Body InAs on Insulator Transistors

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by

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Abstract

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Described in the following report are a series of design decisions and experiments towards demonstrating a prototype bilayer InAs Tunneling Field Effect Transistor (TFET), a new type of transistor which could exhibit a steeper sub-threshold slope and could enable lower-power electronics. In the process of designing and fabricating this device, n-channel InAs on insulator MOSFETs were fabricated and characterized to better inform the TFET design and fabrication. While in this work, a TFET with the desired characteristics was never realized, others were able to demonstrate similar tunneling devices with poor subthreshold slopes. A simple model is presented which explains the sensitivity of the performance of the TFET to interface traps.

Contents

Chapter 1

Introduction

1.1 The Need for a Lower-Voltage Replacement to the Transistor and The Physics Governing the Voltage Sensitivity of Transistors

Over the history of digital computing, reduction of energy consumption per operation has been enabled by the miniaturization of components in integrated circuits. Another reason for this reduction in energy consumption per operation, which is maybe not as well-known, has also been the reduction in circuit power supply voltage.

However, in recent history this reduction in power supply voltage V_{dd} has slowed, as shown in Table 1.1. At the end of the roadmap, the power supply voltage for high performance logic is projected to be 0.57 V [1].

Technology Node	0.25 µm	0.18 µm	0.13 µm	90 nm	65 nm	45 nm	32 nm	22 nm	14 nm	10 nm
Supply Voltage V_{dd} (V)	2.5	1.8	1.3	1.2	1.1	1.0	0.97	0.9	0.8	0.71

Table 1.1: Supply Voltage scaling has slowed since 0.13 µm node. From the International Technology Roadmap for Semiconductors [1], High Performance Logic Technology Requirements.

While there are many technological challenges in practice which make lowering the supply voltage below 0.57 V difficult while maintaining the cost and performance of current digital integrated circuits, a fundamental challenge to lowering the supply voltage has to do with the basic physics of the transistor. This physics limits the voltage sensitivity of the transistor and prevents transistor-based digital circuits from operating at arbitrarily low supply voltages with both high throughput and low standby power levels.

Shown in Figure 1.1 is an energy band diagram of a transistor showing the Fermi distribution of carriers in the source of the transistor and the potential barrier to the channel seen by the source electrons. Lowering the barrier by applying a gate voltage of $\frac{kT}{q}$ at best can only increase the carrier density in the channel, and thus the drain current, by a factor of e. This sensitivity of drain current of the transistor to gate voltage is called the *sub-threshold slope* and at room temperature requires 60 mV of applied gate voltage to increase the drain current by one decade.
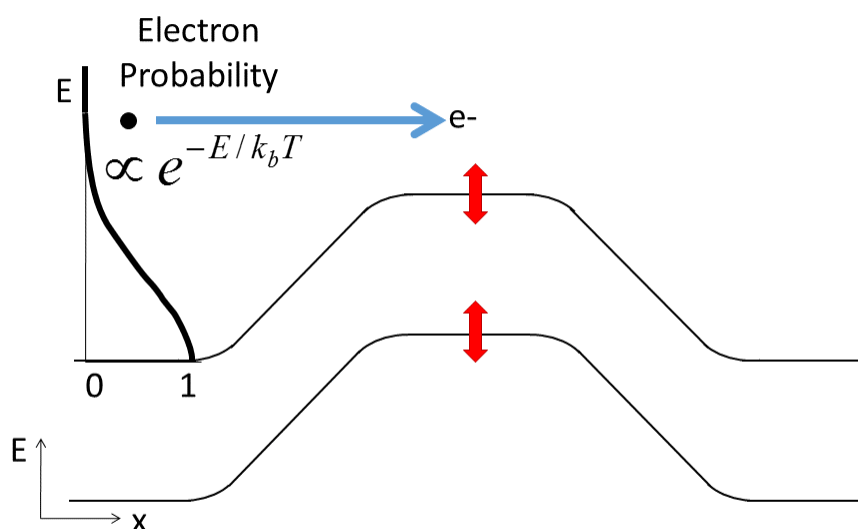

Figure 1.1: Lowering the barrier by applying a gate voltage of $\frac{kT}{q}$ at best can only increase the carrier density in the channel, and thus the drain current, by a factor of e. From [2].

Doing better than this sensitivity would either mean operating the circuit at lower temperatures, which would require expensive, bulky, and energy-consuming refrigeration, or moving away from the concept of modulating transistor conductivity by raising and lowering a potential barrier for thermally excited electrons.

1.2   The Tunneling Field Effect Transistor

The Tunneling Field Effect Transistor (TFET) is one scheme for a steep sub-threshold slope device. The main idea is to inject charge carriers from the source into the channel via quantum-mechanical band-to-band tunneling, avoiding the physics of thermal generation

of electrons over the source-channel barrier. The hope is that the physics permits charge injection using band-to-band tunneling to be engineered to produce a steeper sub-threshold slope device.

The TFET is not a new idea, and many papers on this device have been published. However there tends to be a huge discrepancy between simulation and experiment, with simulation predicting steep subthreshold slopes and on-currents, and experiments falling short [3]. Part of the reason for this discrepancy has to do with overlooked physics of the TFET turn-on. Proposed in this report is a TFET device which was designed while keeping those physics in mind.

Chapter 2

TFET Physics and Design

2.1 Two TFET Switching Mechanisms

Two possible mechanisms have been identified [4] by which TFETs could exploit to potentially achieve a steep sub-threshold slope. The two mechanisms are shown in Figure 2.1.

Barrier Thickness Modulation

Density of States Switching

E_C
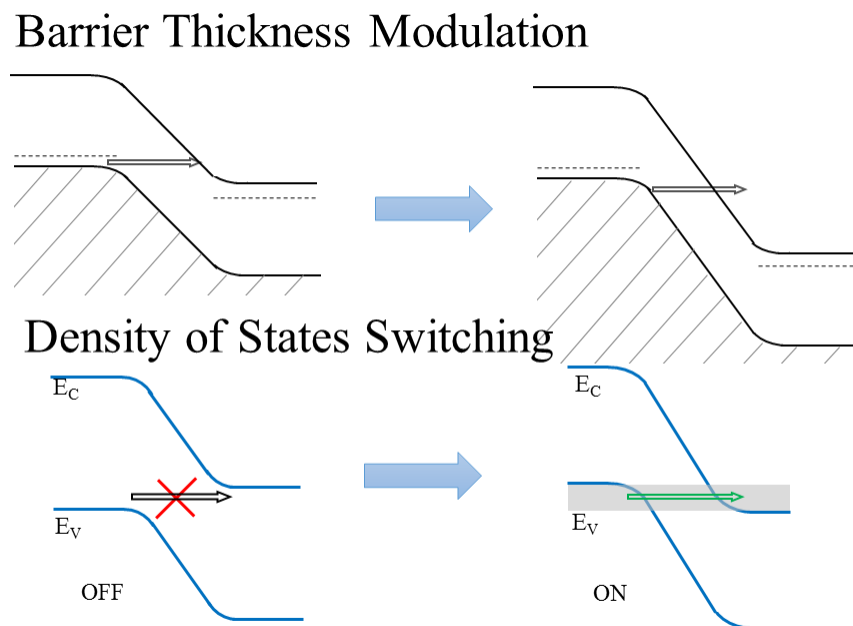
E_C

E_V

E_V

OFF

ON

Figure 2.1: Two possible switching mechanisms in TFETs. From [4].

The first mechanism is called *barrier thickness modulation*, which is when the gate potential acts to modulate the thickness of the source-channel p-n junction depletion region,

thus modulating the band-to-band tunneling probability. While this mechanism has been demonstrated to produce sub-60mV/decade sub-threshold swings at low conductances [5], at high conductances the sub-threshold slope is typically worse. This was explained in the following report [4], where, using Kane's model of band-to-band tunneling [6], the author derived the following equation relating the point sub-threshold slope S to the potential drop across the source-channel junction ϕ and the band-to-band tunneling probability T.

$$S = \left| \frac{\phi}{\log(T)} \right|$$

For the conduction and valence band to line up on opposite sides of the homojunction, we need the potential drop ϕ to be greater than the bandgap. For $T = 1\%$ which is what is required for a good on-state conductance density competitive with state-of-the-art MOS-FETs, $S = 560$ mV/decade for silicon, which is a much worse sub-threshold slope than that of a well-engineered MOSFET.

The second mechanism is called *density of states switching* which is when the gate potential aligns and misaligns the valence and conduction bands opposite the source-channel junction, turning the junction on and off. This is the same mechanism which creates the negative differential resistance region in a tunnel diode [7]. Right away, without looking carefully at the engineering details or the microscopic physics, one realizes the following: *this switching mechanism is only as sensitive to the degree that the conduction and valence band-edges are abrupt.* Also, something which is less obvious is that if one wants to use the alignment and misalignment of band-edges as a switching mechanism, one ought to pay attention to the joint band-edge density of states and recognize that the dimensionality of the source-channel junction plays a role in modifying the joint band-edge density of states.

2.2   Band-Tails and Dimensionality: Two Important Design Considerations for TFETs

While naively, one might think that the semi-conductor band-edge is perfectly sharp, optical measurements of the semi-conductor band-edge [8] reveal that the band-edge is not perfectly sharp. When plotting the optical absorption coefficient versus optical frequency, instead of the expected step function with abrupt turn-on at photon energy equal to the bandgap energy, $\hbar\omega = E_g$, measurements show a more gradual turn-on near the band-edge with absorption $\alpha = \alpha_0 \exp\left[-\frac{\hbar\omega - E_g}{E_0}\right]$, where its abruptness is characterized by the so-called "Urbach parameter" E_0.

Measurements of the optical absorption coefficient of gallium arsenide [9] at different doping concentrations show that the Urbach parameter becomes larger and the absorption edge becomes more broad at higher doping concentrations. One makes the following conclusion, at least to the degree that the physics of optical absorption in semi-conductors translates to

the physics of band-to-band tunneling (both are commonly modeled as being proportional to the integral of the joint density of states over energy): *to see the sharpest TFET turn-on, one must eliminate doping in the tunneling junction.* This is a rather startling conclusion which says that TFET designs ought to move away from the usual technique of preparing tunneling junctions, which is to use heavy chemical doping of both sides of a homojunction to achieve the desired band alignment.

A consequence of the joint density of states determining the TFET turn-on is that the dimensionality of the source-channel junction of the TFET is an important design parameter and should not be neglected. In semiconductor lasers, the dimensionality of the optical gain medium is commonly engineered in order to reduce the joint density of states, which reduces the transparency and threshold current densities of semiconductor lasers [10]. In the referenced report [4], Harrison's tunneling theory [11] is applied to p-n tunnel junctions of different dimensionalities, shown in Figure 2.2 and for each case the tunneling current turn-on is calculated.
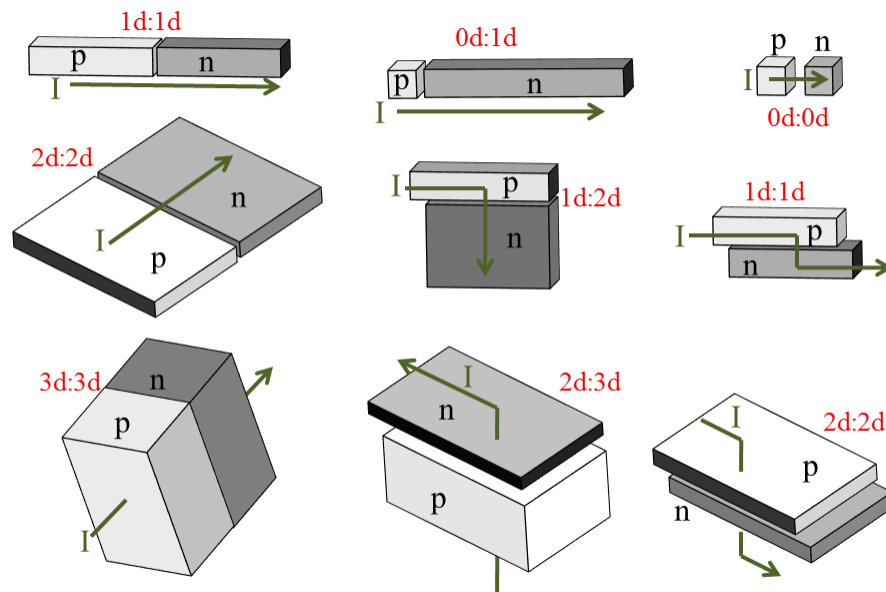

Figure 2.2: Nine possible tunnel p-n junction configurations in TFETs. From [4].

An important conclusion of the calculation is that the 2D-2D face overlapped junction, shown in Figure 2.2, is promising for TFETs. The calculation, using the ideal step-function 2D-2D joint density of states, predicts a sharper turn-on and higher conductance density at low voltages than that of the 3D-3D or 2D-3D tunneling junctions.

2.3 Putting It all Together: The Bilayer Tunneling Field Effect Transistor

The bilayer tunneling field effect transistor or bilayer TFET, is a novel TFET design, first proposed in 2011 [12], which possesses the preferred 2D-2D tunnel junction dimensionality and band alignment prepared via electrostatic gating and not chemical doping. Shown in Figure 2.3 is a cartoon showing the bilayer TFET structure and cross-section energy band diagram. Of central importance to the device is the tunnel junction at the region of the overlap of the staggered top and bottom electrodes, which is formed by accumulation and inversion layers on either side of the semiconductor film induced by the top and bottom gates, respectively. Either by the application of the appropriate voltages to the gate electrodes or by work function control, the conduction band minimum and valence band maximum can be brought into near-alignment and then aligned and misaligned by the application of voltage to the top gate.
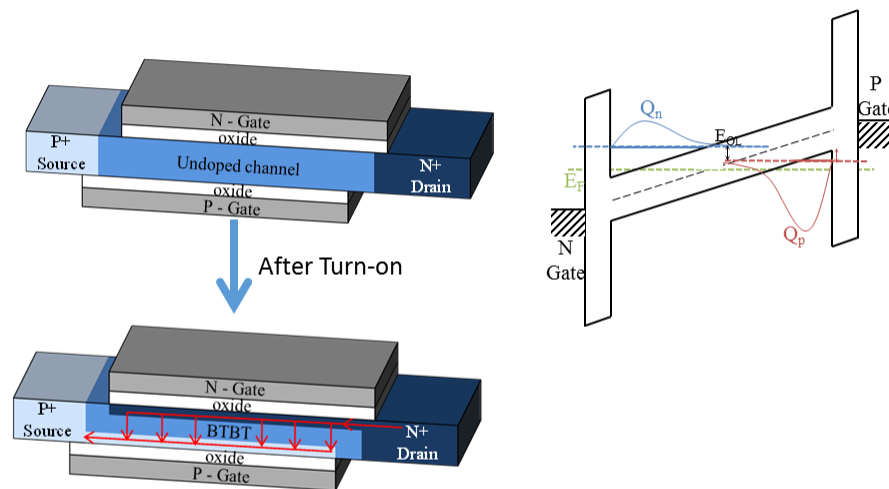

Figure 2.3: Bilayer TFET structure showing current path upon transistor turn-on and the off-state energy band diagram of tunnel junction cross-section. From [13].

There are a few theoretical drawbacks to this device structure. One is that the ideal, no-interface traps, gate efficiency is actually less than one (an easy way to see this is to notice that application of voltage to the top gate works to lower the conduction band minimum energy level of the accumulation layer as well as to slightly lower the valence band maximum

level in the inversion layer through the capacitive coupling of the layer of thin semiconductor film). This is to be contrasted with state-of-the-art multi-gate or fully-depleted silicon-on-insulator MOSFETs, where the gate efficiency is unity. Another drawback is that the device has at least four terminals per device, and suffers from the area penalty of having at least four instead of three terminals, and a shared bulk terminal. A huge practical challenge with this design is the question of how to achieve self-alignment between the staggered gates on opposite sides of the film, in either a fin-based or planar double-gate structure, with self-alignment being a necessary requirement for the manufacturability of this device. Even with these drawbacks, this bilayer TFET device can be viewed as a good experimental 'test-bed' for studying the physics of the density of states switching mechanism.

Chapter 3

Fabrication Processes for InAs TFETs and FETs

3.1   Introduction

Described in this chapter is a micro-fabrication process flow for an planar InAs TFET. InAs was chosen as the transistor body material over the more usual transistor material, silicon, for two reasons:

- The physics of band-to-band tunneling is much like the physics of optical absorption in that the electron momentum is conserved when going from valence band to conduction band. Therefore, for higher band-to-band tunneling rates and thus, higher current densities, a direct-gap semiconductor is preferred.

- Although this was not attempted in the experiment, the small band-gap of InAs (0.3 eV) permits the quiescent band alignment between conduction band minimum and valence band maximum to be achieved by work function control of the top and bottom gates. In larger band-gap semi-conductors, like in silicon, the required work function difference is larger than the range of work functions permitted by metals typically used in micro-fabrication processes. [13]

The bilayer TFET possibly could be realized in two configurations—either as a fin-based transistor, or in a planar, double-gated structure. The planar, double-gated structure was chosen because it was more compatible with the existing process capability at Berkeley. That is, a process for van der Waals bonding epitaxially grown InAs onto insulator-coated substrates was already developed at Berkeley [14], while no process existed for the RIE etching of thin InAs fins at high aspect ratios, which would be required for a fin-based structure.

In order to better understand and design the TFET fabrication process flow, n-type InAs MOSFETs were designed and fabricated as well. Therefore in addition to the bilayer TFET fabrication process flow, an InAs nFET fabrication process flow is described as well.

3.2 TFET Fabrication Process Flow

Shown in Figure 3.1 is a cross-section diagram of a fabricated bilayer TFET. The bilayer TFET fabrication can be broadly separated into three steps. First, the silicon wafer is processed to form the local back gate electrodes and back gate insulator. Next, InAs is bonded onto the silicon die using a process developed by the Javey Research Lab at Berkeley [14]. Finally, the InAs films are processed to form the top gate and source and drain contacts of the transistors.
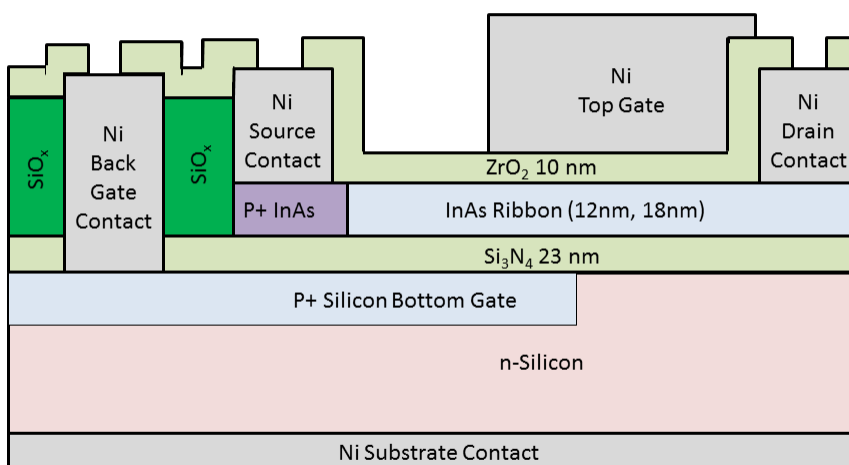

Figure 3.1: Cross-section diagram of an InAs bilayer TFET.

Silicon Back Gate Processing

Shown in Figure 3.2 is a cross-section diagram of the silicon wafer after forming the back gate electrode and back gate insulator. Notice that the back gate electrode is actually a heavily-doped p++ silicon layer implanted into the n-type wafer. While this design choice easily gives us a smooth and flat service upon which to bond the InAs, a consequence of this design is that this particular bilayer TFET does not scale to deep sub-micron dimensions. The tunnel junction length defined by the lateral overlap of the top and bottom gates must be larger than the depletion length of the p++-n junction in the silicon.

The fabrication process is as follows. We start with phosphorus-doped silicon wafers with resistivities of $\sim 5\,\Omega\,\mathrm{cm}$. Then, photo-lithographically patterned fiducials are etched into the
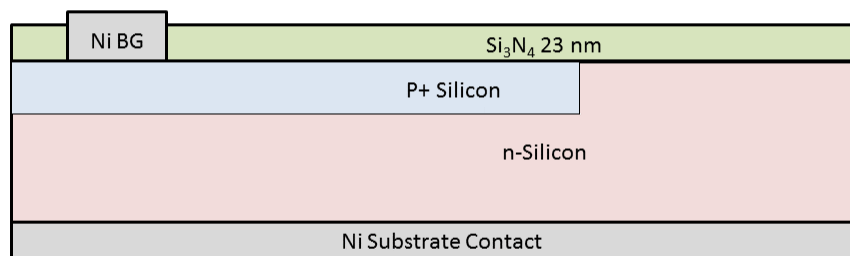
Figure 3.2: Cross-section diagram of the silicon wafer, after silicon processing steps and prior to bonding InAs films onto wafer.

wafer using a chlorine-based chemistry. Next, to tailor the background n-type doping level, blanket phosphorus implants with an implantation energy of 200 keV and doses of $10^{13}/\mathrm{cm}^2$ or $10^{14}/\mathrm{cm}^2$ were implanted through a 15 nm thick dry screen oxide grown on the wafers. Next, the wafers were annealed in a nitrogen ambient for 7 hours at $1050\,^\circ$C to activate and diffuse the dopants to create $\sim 1\,\mu$m thick n-type layers with doping concentrations of $\sim 10^{17}/\mathrm{cm}^3$ and $\sim 10^{18}/\mathrm{cm}^3$, respectively. Following that step, patterned boron implants, through a 15 nm thick dry screen oxide grown on the wafers and using $\sim 2\,\mu$m thick photo-resist as an implant mask, were performed with implantation energies of 30 keV or 90 keV and doses of $3 \cdot 10^{15}/\mathrm{cm}^2$ or $6 \cdot 10^{15}/\mathrm{cm}^2$. Following stripping the photo-resist mask in an oxygen plasma and stripping the screen oxide in diluted HF, a 3 nm dry oxide was grown on the wafers followed by the deposition of an 18nm LPCVD stoichiometric nitride to form the back gate dielectric. During the oxide growth and nitride deposition, the boron-implanted p++ layers which form the back gate electrodes are activated and are designed to have doping concentrations of $\sim 10^{20}/\mathrm{cm}^3$ and junction depths of 400 nm and 800 nm, respectively.

Next, the back-gate dielectric is etched off of the back-side of the wafer using a fluorine-based RIE etch chemistry and then on the front-side, vias were photo-lithographically patterned and then etched through the back gate oxide/nitride dielectric using the same dry etch chemistry. Following this step, nickel electrodes are evaporated and patterned using

the lift-off process with photo-resist to create ohmic contact to the p++ silicon back-gate electrodes through the etched vias. This is followed by the evaporation and patterning via lift-off of Ti/Au fiducials for later electron beam lithography steps. Finally, the back-side of the wafer is metallized with evaporated nickel to ensure electrical contact with the n-type silicon substrate, and the wafer is sawed into dies. Shown in Figure 3.3 is a top-down scanning electron micrograph of a processed silicon die. Notice the clearly visible contrast between the p++ and n-type silicon.
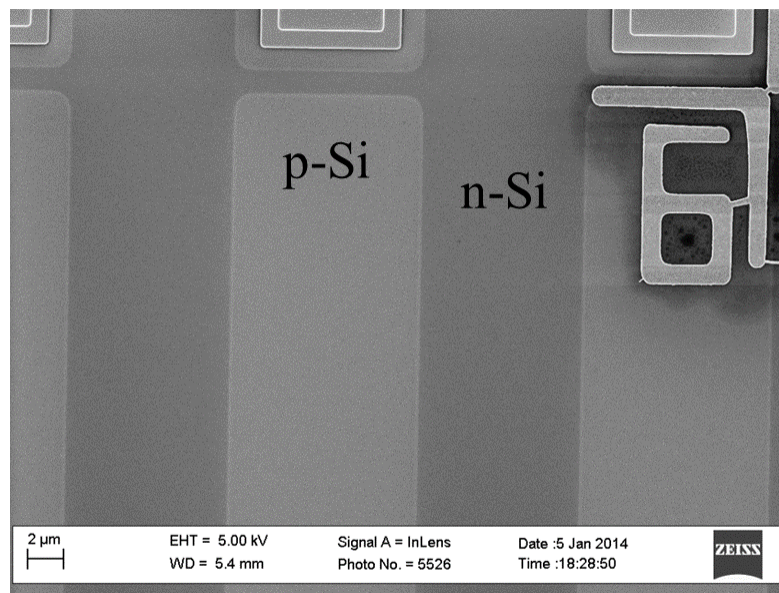

Figure 3.3: Top down SEM of processed silicon die.

van der Waals Bonding of InAs onto Silicon Die

Shown in Figure 3.4 is a cross-section diagram of the silicon die with bonded InAs film straddling the p-n junction boundary. Described below is the fabrication process, developed in [14], used to bond the InAs to the silicon. Figure 3.5 shows the steps used in the bonding process.

First, we start with the processing of the InAs film on its native III-V substrate. Unintentionally doped InAs was pseudomorphically grown by molecular beam epitaxy on top of an unintentionally doped 60 nm $Al_{0.4}Ga_{0.6}Sb$ layer on a 2-inch GaSb substrate by the Krishna Group at the University of New Mexico. The wafer is then cleaved into 1 x 1 cm dies. Next, following an imprint lithography step to pattern 0.5 µm wide polymethylmethacrylic
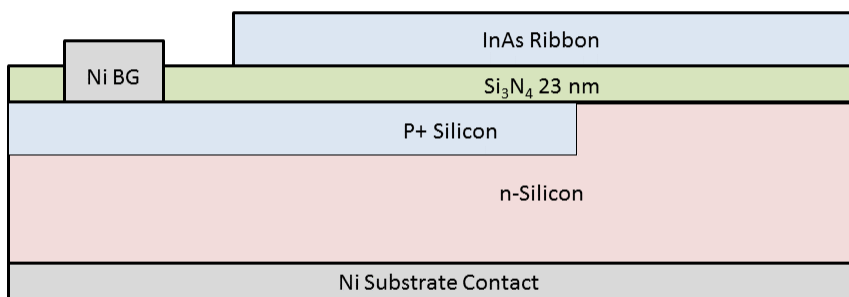
Figure 3.4: Cross-section diagram of the silicon wafer, after bonding InAs films onto wafer.

(PMMA) lines with $1\,\mu m$ pitch on the GaSb subtrate, the InAs film is etched with a 1:20 citric acid/hydrogen peroxide solution to transfer the lines into the InAs. The PMMA is then stripped and the die is further cleaved into 2 x 2 mm dies. Next, a timed etch is performed using a 3% ammonium hydroxide solution, which etches the $Al_{0.4}Ga_{0.6}Sb$ with a high selectivity to InAs, and the InAs lines are undercut. When the InAs lines are barely attached to the GaSb substrate by a narrow $Al_{0.4}Ga_{0.6}Sb$ stub, the die is taken out of solution, rinsed in water, and dried with an nitrogen gun, and a polydimethylsiloxane (PDMS) substrate is brought into intimate contact and then detached from the GaSb substrate. This transfers the InAs film onto the PDMS substrate.

Next, the $Al_{0.4}Ga_{0.6}Sb$ remnants are etched off of the backside of the InAs films on the PDMS substrate with dilute HF. After rinsing and drying, the PDMS substrate is brought into contact with a silicon die and then detached. After this step, the InAs films are detached from the PDMS substrate and are bonded onto silicon. Shown in Figure 3.6 is an optical microscope image of a small portion of the silicon die with a particularly good InAs transfer yield. As this InAs bonding process only has a rough angular alignment between InAs lines and the patterns on the silicon, the silicon die must be inspected either optically or using scanning electron microscopy to be able to locate positions of the InAs lines relative to gold electron beam fiducial markers so that the InAs lines can be processed into transistors.
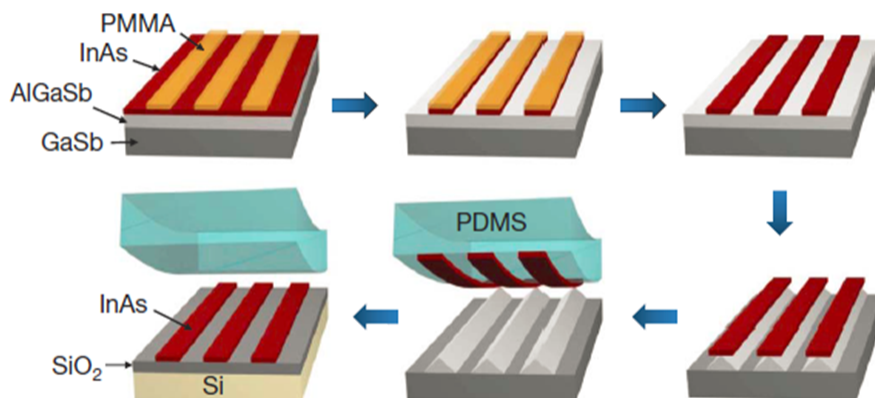
Figure 3.5: Process for bonding InAs onto silicon. InAs strips are epitaxially lifted off of the GaSb substrate and bonded onto silicon with the help of a PDMS stamp. From [14].

InAs Top Gate, Source, and Drain Processing

With the InAs films bonded to the silicon die, the next steps are to do the processing for the source, drain, and top gate of the InAs transistors. The first mask step is the p-type doping of InAs using a zinc vapor-phase diffusion to create the p-type source in the natively n-type InAs. First, oxide is evaporated and then windows in the oxide are etched in a buffered HF solution with an electron beam lithographically defined PMMA mask. Next, the InAs is doped p-type through the windows in the oxide using a Zn vapor phase diffusion doping process $400\,^{\circ}C$ developed in [15].

After stripping the oxide mask in buffered HF, another layer of oxide used for the isolation of the source and drain leads from the substrate, is evaporated and windows in the oxide exposing the active area and back gate contact of the transistor are patterned via etching in a buffered HF solution using a lithographically defined PMMA mask. Next, the nickel source and drain electrodes, as well as the leads to the back gate electrode are evaporated and patterned using the liftoff process, followed by a 1 min anneal at $300\,^{\circ}C$ to improve the nickel-InAs contact resistance. Prior to the evaporation of the nickel, a quick dip in dilute HF is used to remove the native oxide from the surface of the InAs.

Then, the top gate dielectric, ZrO_2 is deposited using a thermal atomic layer deposition process at $130\,^{\circ}C$ using tetrakis (ethylmethylamido) zirconium and water precursors. Follow-
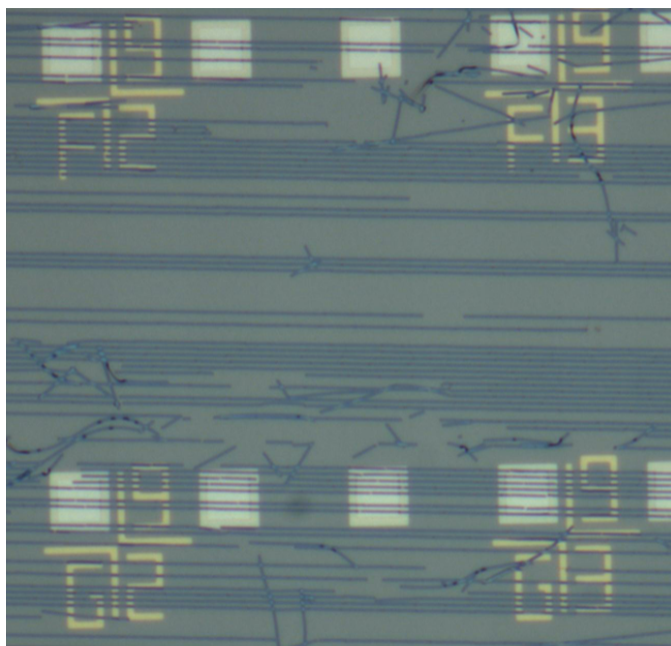
Figure 3.6: An optical microscope image of a small portion of the silicon die with a good InAs transfer yield.

ing the deposition of the film, a forming gas anneal is performed at $170\,^\circ$C, which has been shown to reduce interface trap densities at the InAs ZrO$_2$ interface [16]. Next, nickel gate electrodes are evaporated and patterned using the lift-off process, followed by the etching of vias through the ZrO$_2$ to the source and drain pads using buffered HF solution through a lithographically patterned PMMA etch mask. A scanning electron micrograph showing a finished device is shown in Figure 3.7.

3.3   nFET Fabrication Process Flow

The nFET fabrication process flow is much simpler and recycles a lot of the steps from the TFET process flow. Shown in Figure 3.8 is a cross-section diagram of an InAs nFET.

The nFET fabrication process generally proceeds as that of the TFET in that first the silcon wafer is processed and sawed into dies, followed by the bonding of InAs onto the silicon die and then the electron beam lithography processing of the bonded InAs films into transistors. Here, the silicon wafer processing is much simpler, consisting of only the growth and deposition of the thermal oxide and LPCVD nitride films on the p++ silicon wafer with resistivity of $< 1\,\text{m}\Omega\,\text{cm}$, followed by the backside RIE etching of the dielectric film in a fluorine-based chemistry and nickel metallization of the backside, and then finally the
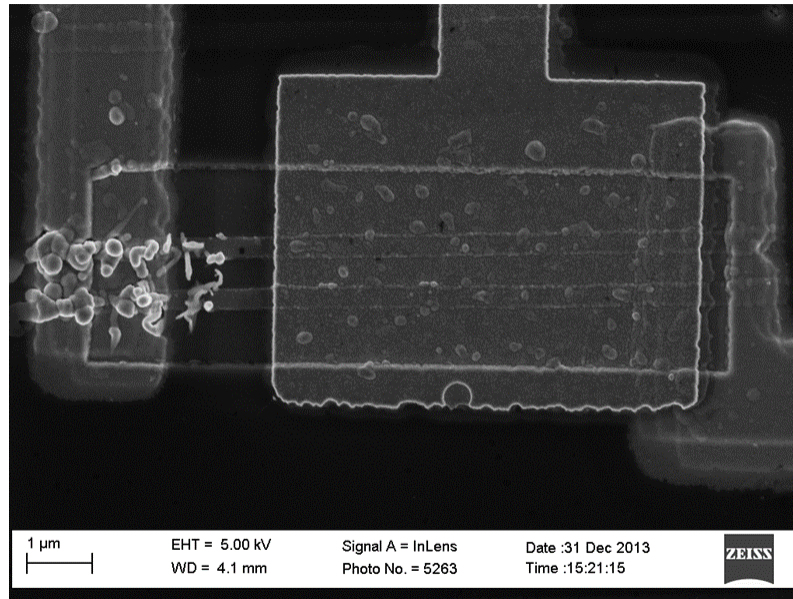
Figure 3.7: A top-down SEM of a finished TFET device.

evaporation and lift-off of Ti/Au fiducial markers for electron beam lithography and sawing the wafer into dies. The bonding of the InAs to the silicon die proceeds in the same way except that the bonding yield requirement is relaxed since nFET transistors do not need to straddle a lateral p-n junction in the silicon. The InAs nFET transistor processing is a lot simpler as well, mostly because there is no need to create a p-type source. The nFET transistor processing required is only the fabrication of the nickel source and drain electrodes, followed by the top gate dielectric and electrode processing and source/drain via opening for probing. Shown in Figure 3.9 is an optical image of a completed nFET.
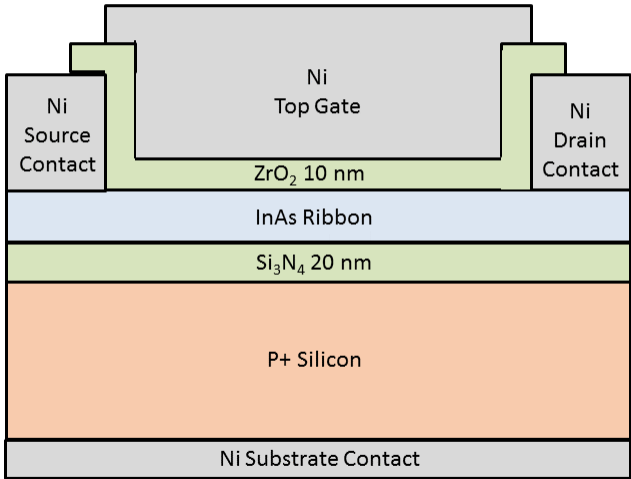
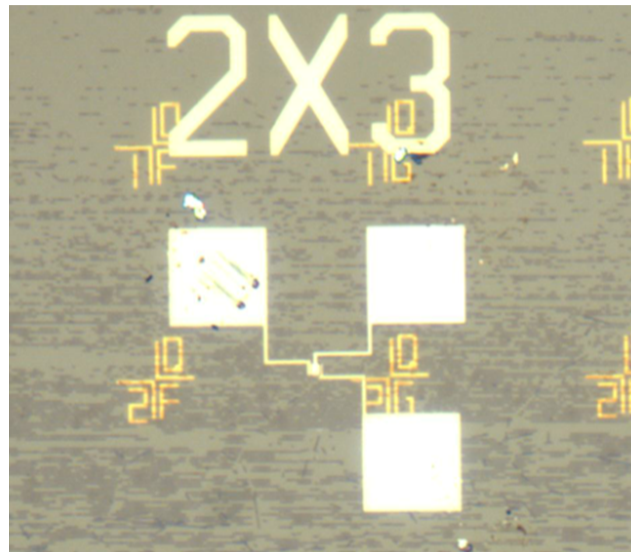Figure 3.8: A cross-section diagram of an nFET device.

Figure 3.9: Optical image of a completed nFET.

Chapter 4

Measurement Results and Interpretation

4.1 TFET Measurement Results

One run of TFET devices was able to be completed. No trend in transfer characteristics was found across the fabricated devices. High leakage currents were measured from substrate to probe pads. Plotted in Figure 4.1 is a 2 terminal I-V measurement from drain probe pad to the substrate of a TFET device. In the desired operation of the TFET device, the drain voltage is higher than the grounded substrate, and this measurement shows a drain current level comparable to, or maybe higher than the on state current for a few micro-meter wide TFET device.

This leakage was later attributed to an oversight in the fabrication process which was predicated on two false assumptions. The first bad assumption was the etch rate of ALD ZrO_2 in 5:1 buffered HF for clearing the gate dielectric from the source and drain probe pads for probing. Ellipsometry measurements pre- and post-etching on silicon dies with blanket ALD ZrO2 films, along with checking the die's 'hydrophobicity' post etching were used to calibrate the BHF etch rate. However, ellipsometry can only measure an average film thickness. It was later discovered that the ZrO_2 does not etch uniformly in BHF, and the condition used in the process lead to a huge overetch of portions of the ZrO_2 film. The second bad assumption was that the nickel probe pads would be a good etch-stop layer for BHF. Under this unintended overetch condition, BHF was found to form pinholes in the nickel film, allowing the BHF to seep through and attack the field oxide and back gate dielectric underneath the probe pad. Shown in Figure 4.2 is a nickel probe pad with pinholes from prolonged exposure to BHF.
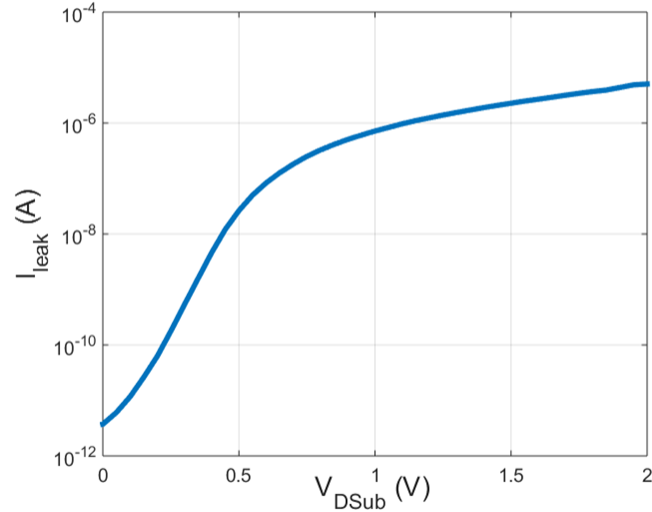
Figure 4.1: Drain probe pad to substrate leakage plotted for a first run TFET device.

4.2 nFET Measurement Results

InAs nFETs were able to be fabricated with interpretable electrical characterization data. Plotted in Figure 4.3 is the measured transfer characteristic of a typical nFET. Common to all of the measured nFETs is a poor subthreshold slope. This poor gate efficiency was attributed to the high interface trap density D_{it} at the InAs/ZrO$_2$ interface. Electrons attracted to the surface of the semiconductor become captured by the interface traps and cannot participate in conduction. This means that more voltage needs to be applied to the gate to increase the mobile channel charge and thus, the drain current. From the sub-threshold slope, D_{it} is estimated to be $3 \times 10^{13} \, \mathrm{eV}^{-1} \, \mathrm{cm}^{-2}$.

4.3 Extraordinary Sensitivity of TFET Subthreshold Slope to Interface Traps

The high D_{it} not only degrades the sub-threshold slope by reducing the gate efficiency. The interface traps also provide a conduction path in parallel to the direct band-to-band tunneling from valence to conduction band edges. The turn-on of this conduction path occurs prior to alignment of conduction and valence band edges and is believed to be responsible for
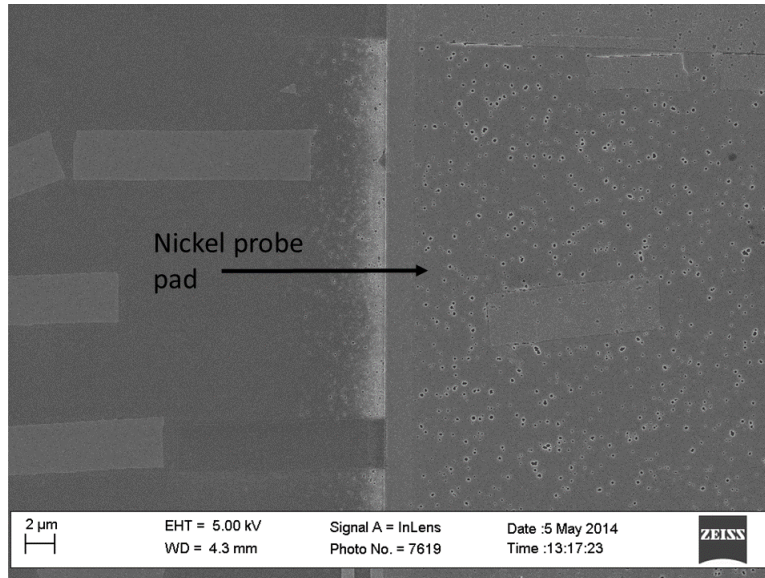
Figure 4.2: Top-down SEM showing pinholes in nickel film formed by BHF etching. Notice the 'un-holey' border on the edges of the probe pad. This is where the PMMA via etch mask protected the nickel.

the smeared-out, and temperature dependent [17] turn-on for TFETs which operate by the density of states switching mechanism.

Figure 4.4 explains this undesired parallel conduction path in a TFET. The source-channel junction in a TFET, with interface traps throughout the bandgap, is shown. The two-step process of tunneling into the traps and then the thermal generation from the trap and into the band provides a shunt current path in the TFET. When the tunneling rate is larger than the thermal generation rate, the current density in the junction is proportional to the thermal generation rate from the traps to the conduction band, which, like the normal generation over the source-channel barrier, is governed by the Boltzmann factor.

Assuming that the tunneling probability to an interface trap is the same as the tunneling probability to a conduction band energy state, engineering out this parallel conduction path would require a huge reduction in the density of interface traps. The extracted D_{it} and the 2D density of states at the conduction band edge of InAs are both $3 \times 10^{13} \, \text{eV}^{-1} \, \text{cm}^{-2}$. To achieve an on-off ratio of 10^4, which barely would meet the minimum requirement for transistors used in digital logic, we'd roughly need to reduce the interface trap density by the same amount to $3 \times 10^9 \, \text{eV}^{-1} \, \text{cm}^{-2}$, which is comparable to or even lower than the best interface trap densities for the silicon/thermal oxide interface. Engineering interface trap densities to such low levels is very challenging and not very practical for this InAs bilayer TFET device, where great chemical control of the InAs-dielectric interfaces is not obtainable with this fabrication process.
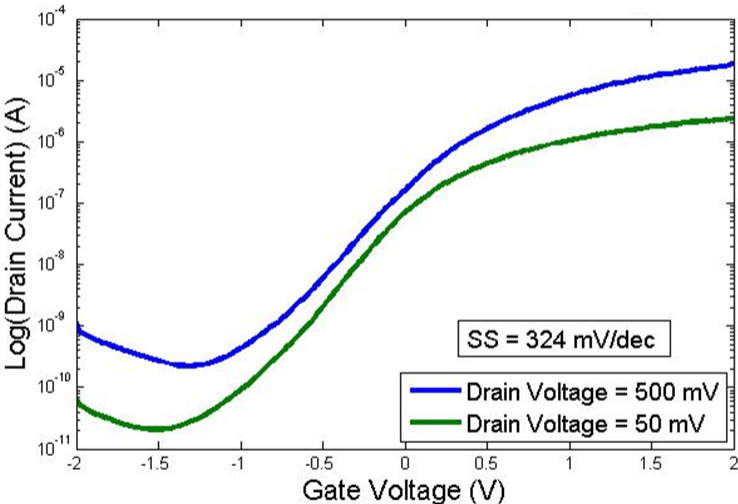
Figure 4.3: Transfer characteristic of InAs nFET with 2 μm gate length, and 1.5 μm width.
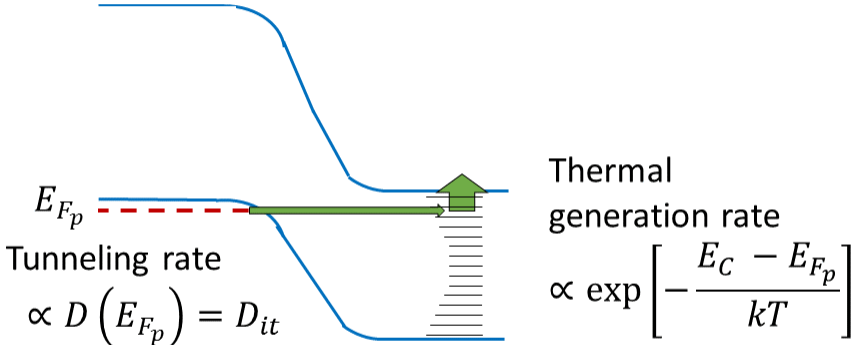
Figure 4.4: The source-channel junction in a TFET, with interface traps throughout the bandgap, is shown. The two-step process of tunneling into the traps and then the thermal generation from the trap and into the band provides a shunt current path in the TFET.

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