Improved Nanowire Sensor for pH Measurements in solution

Maria Pace Pace

Electrical Engineering and Computer Sciences
University of California at Berkeley

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By

Maria Pace

Research Project

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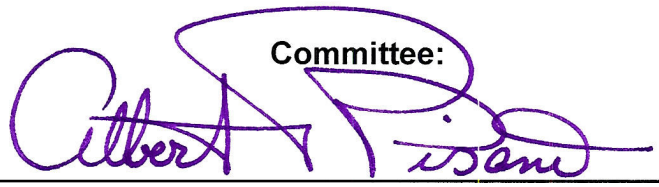

Professor Albert P. Pisano
Research Advisor

15 DEC 2014

(Date)

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Professor Ali Javey
Second Reader

12/15/2014

(Date)

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1. Introduction

1.1 Chemical Sensing:

Industries raging from medical to environmental, automotive and homeland security have a wide interest in chemical sensors. Miniaturized sensors, that are cost-effective, high performance (high sensitivity and speed), portable and CMOS (Complementary Metal Oxide Semiconductor) integrable are advantageous to a more optimum sensor platform.

Nanotechnology facilitates the fabrication of Silicon Nanowires (SiNW) with high surface area to volume ratio, which leads to higher sensitivity with shorter response times in detection of charged species [1]. This work overcomes several shortcomings in previous sensor designs.[2, 3]. Park's work on a nanowire sensor focused on pH measurement and functionalization of the nanowire sensor for biological applications.

Nanowires can be fabricated primarily by two methods: bottom up and top down fabrication techniques.

In the bottom up fabrication process, nanowires are formed by atom-by-atom deposition, with process conditions dictating the final structures. This method can produce very small nanowires. The principal drawback of this fabrication method is the integration with microelectronic components and external circuitry, because it is difficult to control the location and exact dimensions of the resulting nanowire.

The top down fabrication process consists of selective removal of layered material to form the nanowires, similar to a thin-film semiconductor fabrication process. The main advantage of this method is the use of existing semiconductor fabrication tooling. The principal limitation is the achievable small dimensions, limited by the available lithography tool. The patterning method used in this approach is nanolithography using direct-write electron beam patterning, using a photoresist mask and silicon etching techniques to fabricate the nanowires as discussed in section 3. A second limitation specific to electron beam patterned nanowires is the time required to generate the pattern. The nanowires themselves are not particularly time consuming, but the necessary ancillary connecting wires and bond pads take an inordinate amount of time to write.

Park and Choi use a top down fabrication method. From their previous research work [1], three main challenges are identified and improved in this work:

i) Line Edge Roughness (LER)

ii) Sensor Response Drift over time

iii) Passivation pin hole density

These three limitations and their improvements are discussed in sections 3 through 5.

2. Fundamentals of Silicon nanowires (Si NW) and electrochemical sensing mechanism

2.1 Physics of Depletion Region

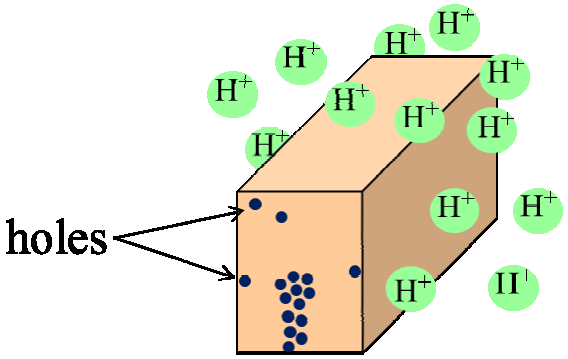

Figure 1. Silicon Nanowire cross-section in ionic solution.

Given an ionic fluid under test that contains for example hydrogen ions, a p-doped semiconductor nanowire is immersed within as a sensing element. When the hydrogen ions approach the semiconductor, then positive electrical charges (eg. hydrogen ions (H+)) in solution cause positive majority carriers (holes) in the semiconductor nanowire to be electrostatically repelled around the periphery of the nanowire, forming a region depleted of positive majority carriers, thus causing an increase in electrical resistance since fewer carriers are available for electrical conduction. There is also a region depleted of H+ ions on the solution side of the interface, the so-called Debye region. Conversely, a decrease in the positive ion concentration in solution, or increase in negative ion concentration will cause an accumulation of positive charge carriers in the semiconductor, which will decrease electrical resistance of the nanowire. This electrical resistance is the sensed quantity that is used for pH measurement.

A complementary device is also possible, where the majority carriers are electrons (-), and the response is opposite. This work uses only a p-doped nanowire.

2.2 Electrochemistry and pH sensing

The pH in a fluid can be detected using Ion Sensitive Field Effect Transistors (ISFET) [4]. However, one disadvantage is that the sensing area is limited to the electrical channel of the ISFET, which is necessarily very small to provide higher transistor performance. This limitation reduces the overall sensitivity of the sensor made from an ISFET.

In this work, the sensor element uses a long silicon nanowire to achieve high sensitivity. No amplification is achieved within the element, however high sensitivity is achieved by appropriate dimensional scaling. In general, having a high aspect (perimeter to area) ratio in cross-section leads to the highest sensitivity because the charge depletion region covers a larger percentage of the cross-section of the nanowire for a given solution ionic concentration. Making the sensor wire long increases the collection volume in the fluid, and increases the baseline electrical resistance. It is desired for the ions in solution to cause the maximal perturbation in electrical resistance in the nanowire, within the resistance measurement limitations of the external circuit.

2.3 Fabrication

Using a top down fabrication method with electron beam lithography and optical lithography, SiNW can achieve small dimensions (50 nm wide), high reproducibility and reliability. Silicon on insulator (SOI) wafers are used to fabricate the nanowire sensors. SOI wafers are fabricated with a thin monocrystalline silicon layer bonded on top of an insulator having very low defect density.

Line Edge Roughness: The hardmask

One of the challenges in this work is to achieve the fabrication of small and large features using a single photomask. Electron beam lithography write time is directly proportional to the area on the wafer being written (exposed). This limitation does not exist in optical (visible light) lithography because the exposure is a flood exposure, but optical lithography has a limitation of diffraction limited resolution. This challenge is overcome by using a combination of electron beam lithography and optical lithography integrated into one etch step. The electron beam is used to form the small features (nanowire sensors) and the optical lithography is used to form the large features (leads and pads). In this way, the e-beam write time is short, used only as needed for high resolution, while necessarily large features are pattered more crudely by optical lithography, yet they are etched in the same step. Since the optically-sensitive film used is different for optical and e-beam exposures, the patterns must be combined in a separate masking layer under the film before being transferred to the silicon to form the nanowire.

A pattern can be transferred by liftoff or by using a hard mask. In a lift off process, the nanowires can be formed by deposition of metal (Chromium) mask followed by lift off. This process is repeated twice, once for the large features using optical lithography, and again for small nanowire features using ebeam lithography. This is the method employed by both Park and by Choi.

Disadvantages of this method are that it requires an additional mask and it also leads to line edge roughness (LER). As a result of the LER, the sensor response measured is not as accurate or consistent from nanowire to nanowire. A further problem with this approach is that the introduction of Cr early in the process leads to a contamination that

renders the samples as “non-CMOS compatible”, limiting future processing and integration.

A better approach is to use a hard mask to form the nanowire sensors. For instance, a silicon oxide (SiO_2) is thermally grown on top of the Silicon as a sacrificial hardmask layer. Once the nanowires are exposed with an e-beam pattern and developed, then this pattern is transferred to the oxide layer using an oxide etch. Subsequently, optical lithography is used to pattern large features (wires, bondpads), while grossly protecting the previously etched nanowire region. This pattern is transferred to the oxide hardmask as well. After removing the photoresist, the silicon is etched using the oxide as a hardmask, and both large and small features are formed simultaneously in the silicon (SOI) layer.

Straight side walls are achieved using a silicon etch, with oxide mask, eliminating the poor LER and the need for an additional mask. One additional advantage of this approach is making this process truly CMOS compatible by eliminating the use of metals as the hardmask material.

Pin hole density in the dielectric

After forming the nanowire, a dielectric film is deposited around the wire, encapsulating it and electrically insulating it from the surrounding fluid. This prevents charge recombination at the wire-solution interface. This dielectric is necessarily very thin (a few nm) so that the electric field penetrates from the solution into the nanowire, causing charge depletion. Plasma Enhanced Chemical Vapor Deposition (PECVD) is used by both Park and Choi for depositing the dielectric film surrounding the nanowire. PECVD provides good adhesion, and uniformity and most importantly for their process, low

deposition temperatures (~350 C) compared to other CVD (Chemical vapor deposition) methods. PECVD allows a large choice of materials to be deposited such as silicon nitride, silicon oxide etc. However, PECVD generally produces a film with higher pin hole density when compared to other deposition methods such as Low Pressure Chemical Vapor Deposition (LPCVD), which is performed at higher temperatures (~800C).

A synergistic result of the redesigned process in this work is that by eliminating the Cr hardmask (which was done principally to imporove LER) the process remains CMOS-compatible at this point. This allows high temperature processing, and thus, the use of LPCVD nitride as the dielectric material.

3. Si NW Design and Fabrication

3.1 Motivation of work:

Three fabrication improvements are discussed in this section.

i) Line edge roughness (LER) results from double chromium deposition and lift off. Liftoff is a process whereby the metal mask shape is formed by "tearing", leading to a jagged edge. A contribution of this work is a redesigned process using a double mask to combine gross and nano features without jagged edges. This work eliminates the need to do a

chromium deposition and lift off making this process truly CMOS compatible and improving on the line edge roughness.

ii) Another contribution is the improved drift over time. This is achieved by using an AC voltage and it is explained in more detail in section 4.

iii) This work also improves on the pin hole density (traps) by using LPCVD (Low Pressure Chemical Vapor Deposition) instead of PECVD (Plasma Enhanced Chemical Vapor Deposition) made possible, in part, by making the process CMOS compatible and high temperature compatible.

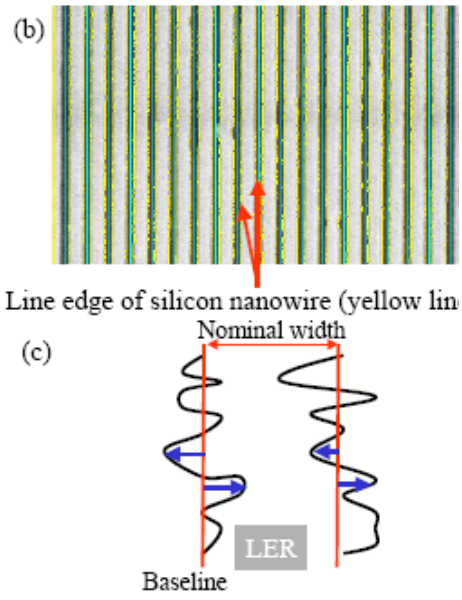

Figure 2. Line edge roughness as viewed in a CD-SEM [Park]

3.2 Novel Fabrication Process

A novel fabrication process is used to improve on these three challenges mentioned above. Using SOI (Silicon on insulator) wafer, a thin thermal oxide (30 nm) is grown as the sacrificial hardmask layer. A further improvement in the process is that it can be made wafer-scale, saving development time for rapid short-loop development. Thus, alignment marks are placed at the wafer level using optical lithography. One additional improvement is the addition of a patterned heavy Boron ion-implantation to improve ohmic contact and reduce parasitic resistance outside of the nanowire region. This improves sensor sensitivity, since the majority of the resistance is now in the nanowire rather than parsitics. Once the wafer is diced, e-beam lithography is used to form the nanowire sensor (small features) shape into the silicon oxide hard mask. Optical lithography is then employed to form the leads and pads (large features) shape using photoresist as a mask and this shape is transferred into the silicon oxide with an etch (while grossly protecting the nanowire region). Once both large and small features are formed in the oxide hardmask, the aggregate pattern is etched into the SOI layer, forming the nanowire and all associated leads and pads. A layer of silicon nitride dielectric is deposited as passivation layer. Silicon nitride is used as an ion blocking electrical insulator. Holes are etched in the nitride on the pads, and finally bondpad contact metal is deposited followed by liftoff.

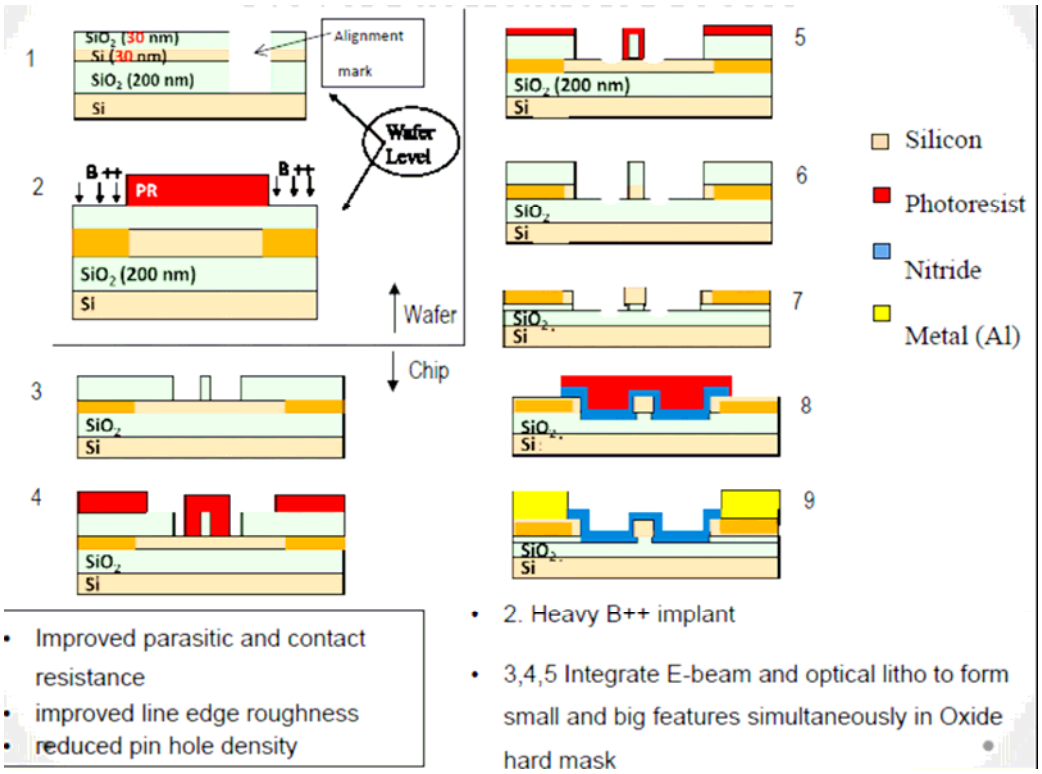

Figure 3. Novel fabrication process

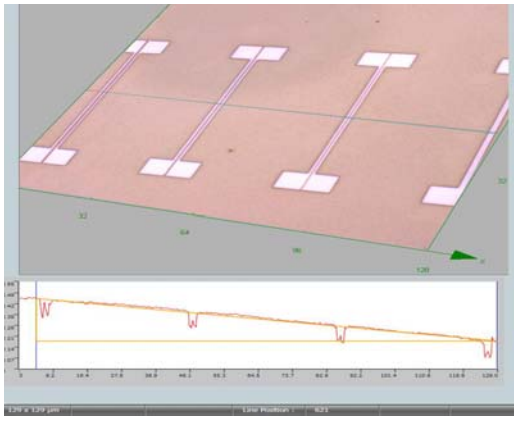

Figure 4. Array of fabricated nanowire sensors

4. Driving Mechanism Improvements:

Beyond process improvements, additional improvements to the nanowire sensor of Park and Choi have been made in the driving mechanism. This work explores a novel driving mechanism to reduce the sensor drift over time that was reported by Park: instead of using a DC voltage to drive the nanowire, an AC voltage is used. The principal cause of sensor drift over time is the accumulation of charge at the nanowire-solution interface. This was partially mitigated by the use of a higher quality dielectric, described above. But independent of pinholes in the dielectric, charge still accumulates on the surface of the nanowire.

One aspect of the AC driving mechanism is that a periodic reversal of the field causes charge to be driven away, thus performing a clean on the sensor. This effect can be amplified by using a periodic large field, above the normal sensing potential, for the purposes of charge cleaning.

Another aspect of using AC is achieved by careful selection of the frequency of the driving potential. Ions in solution will migrate in response to the applied potential. Any charge that is attached to the nanowire will remain so. Therefore, the sensor can be re-baselined, or calibrated on each cycle when the mobile ions are repelled. Any charge present during the repulsion phase are assumed “fixed” and therefore ignored. As the potential reverses, and ions are attracted, the net change in charge is assumed to be the charge in solution, and that charge is measured as the true pH. By operating the sensor in this way, the drift over time is nullified.

The mechanism described herein for driving the sensor with AC to improve drift can be further extended to functionalized surface nanowire sensors to detect the amount of attached biomaterial. In this case, the operation is reversed and the quiescent charge is the signal of interest, and the periodic charge (in solution) is discarded.

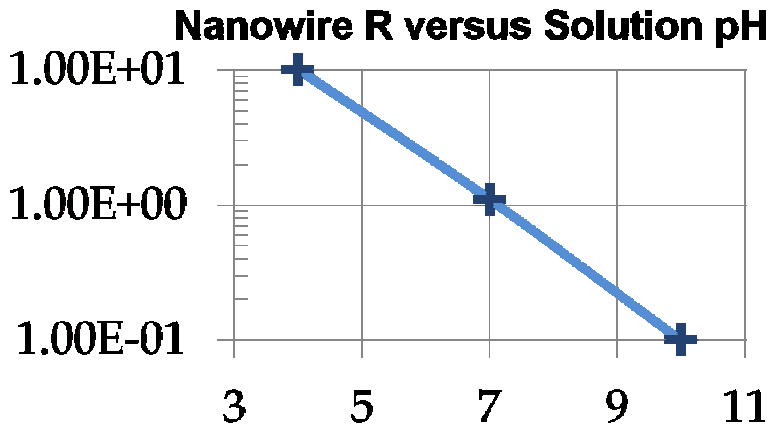

Figure 5. Measured nanowire resistance versus solution pH from new improved devices

5. Conclusion

In this work, the pH nanowire sensor of Park and the sensor of Choi have been improved by two principal changes: A completely redesigned process and a novel driving mechanism. These changes target three disadvantages as reported by both Park and by Choi: Line Edge Roughness, Sensor Drift over time, and passivation pinhole density. By

employing a complete redesign, other improvements, such as reduced parasitics and faster development cycles are obtained as well.

The changes to the process include:

- The use of a two-stage oxide hardmask to reduce line edge roughness and to maintain CMOS compatibility.
- The use of LPCVD nitride as passivation to reduce pinhole density
- The addition of a selective heavy boron implantation to reduce parasitics
- The use of wafer-level alignment marks to allow wafer-scale processing for par t of all of the process, simplifying the development cycle dramatically.

The second main improvement is to the driving mechanism of the device. By employing AC drive instead of DC, the sensor drift over time is eliminated. The use of AC causes a periodic cleaning of the ions attached to the nanowire. Additionally, through careful selection of the frequency, allows re-calibration or re-baselining of the sensor on each cycle to distinguish charge that has become permanently attached from charge that remains mobile in the solution.

6. Bibliography

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