

Time-Division Duplexing Solutions for Wireless Transcievers

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Time-Division Duplexing Solutions for Wireless Transceivers

by

Amanda Pratt

A thesis submitted in partial satisfaction of the
requirements for the degree of
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University of California, Berkeley

Time-Division Duplexing Solutions for Wireless Transceivers

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Abstract

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Professor Borivoje Nikolic, Chair

The wireless age poses an unprecedented strain on global spectrum resources. As such, the available frequency spectrum is becoming more segmented, creating a need for wireless front-ends with wide bandwidths and unpaired spectrum capabilities. The features of time-division duplexing (TDD) lend themselves to this current and future need, making it a growing means of wireless communication across the mobile spectrum.

Integrating a high-power transmitter and a highly sensitive receiver on the same antenna, as is desired in TDD, remains a difficult problem for time-division duplexing transceivers. This work describes wide-band TDD solutions which enable the integration of a power amplifier (PA) on the same antenna as a sensitive low-noise amplifier (LNA).

The first part of this work discusses the design of a transmit/receive (Tx/Rx) switch, a solution for transceiver integration, implemented in bulk CMOS. The simulation results from the extracted layout of this design show improved insertion loss performance and power tolerance over the state-of-the-art Tx/Rx switches in CMOS.

The second part of this work presents the design of a second TDD solution, which implements device re-use, a novel approach to the TDD power tolerance problem. This solution overcomes some of the inherent non-idealities of a CMOS Tx/Rx switch, such as insertion loss, by embedding an LNA within the devices of a digital PA. The results from an extracted layout of this device are also presented.

The end result of this work is two different, novel approaches to integrating transmit and receive circuitry on the same antenna, each achieving state-of-the-art performance. We also provide a discussion of the benefits and drawbacks of each solution.

This thesis is dedicated to my teachers, mentors, managers, friends, and family members
who could see a future for me before I could imagine it and
who showed me the way before I knew there was somewhere to go.
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Chapter 1

Introduction

It is no surprise to note the increased global presence of mobile devices. Since 2000, mobile traffic has risen to a level 18 times the total traffic rate of the internet in 2000 [1]. The economic interest in mobile devices is obvious.

However, with the proliferation of wireless devices, the radio frequency spectrum has become increasingly cluttered. In new standards, such as LTE, related communication bands are disjoint in the frequency domain. In addition, wireless devices must generally support a large number of protocols, such as legacy and country-specific protocols. This has increased the need for more integrated radios in handsets.

The RF-FPGA project will integrate a number of different frequency band transceivers on the same silicon chip in order to support the varied bands and varied protocols required in modern mobile systems. Accordingly, the RF-FPGA project, as designed here at UC Berkeley, will support both frequency-division duplexing (FDD) protocols and time-division duplexing (TDD) protocols. FDD requires a pair of spectrum: one channel to transmit and one channel to receive. TDD does not require paired spectrum, but instead transmits and receives data at alternating time intervals, as shown in Figure 1.1. TDD dominates WiFi, Bluetooth, and government radios.

While LTE-FDD is currently the more common protocol, with a penetration rate 8.3

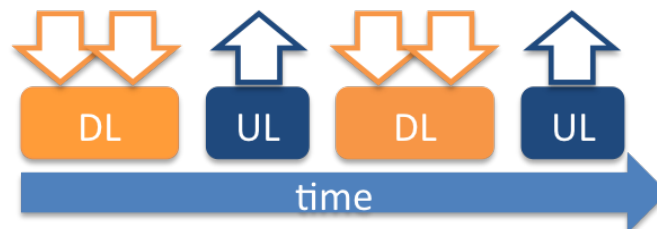


Figure 1.1: A simplified diagram of the TDD downlink and uplink division in the time domain.

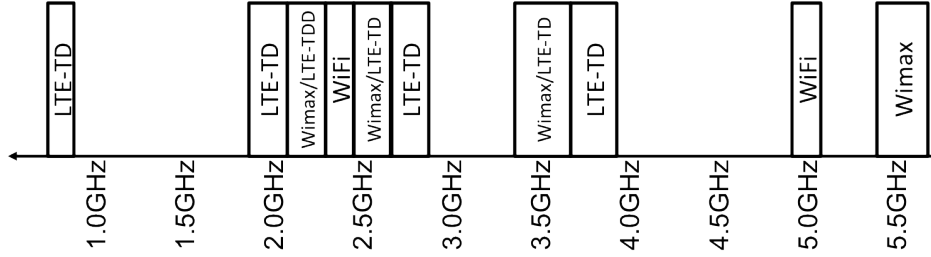


Figure 1.2: A simplified diagram indicating spectrum used for some form of mobile TDD communication. Exact spectrum allocations may be found in [3, 4].

times that of LTE-TDD, TDD is still a major player in both LTE and other mobile solutions [2]. For example, LTE-TDD covered a population 500 million in China alone last year [3].

In addition, LTE-TDD's lack of paired spectrum and ability to change downlink (DL) to uplink (UP) ratios is beneficial as compared to LTE-FDD [3]. The ability to change downlink to uplink ratios will become more important as mobile video traffic, already exceeding 50% of data usage in 2013, increases popularity [1].

Finally TDD solutions are also used in the WiFi and WiMax protocols. With 45% of mobile data being off-loaded to WiFi or femtocells [1], which can use WiMax, TDD represents an important portion of current and future mobile traffic. Finally, TDD is the protocol used in most government transceivers.

Figure 1.2 shows the areas of the frequency spectrum in which a TDD mobile system may operate. The spread of the spectrum in this diagram and the interwoven protocols illustrate the clear need for a wide-band, configurable, TDD transceiver.

In this introduction, we present background information on common TDD architecture topologies and outline the problems of interest in TDD transceivers.

1.1 TDD Transciever Architecture Overview

Given that in a TDD system, transmit and receive transmissions happen at the same frequency, the transmitting power amplifier (PA) and the receiving low-noise amplifier or low-noise transimpedance amplifier (LNA/LNTA) are connected, in general, to a single antenna through the same transformer network. A diagram of such a system may be seen in Figure 1.3.

RF-FPGA Architecture Description

In the final implementation of the RF-FPGA, each band will have a dedicated PA and LNA connected to a transformer. Each transformer will be connected to the single antenna, which will use an interposer to create the appropriate antenna size.

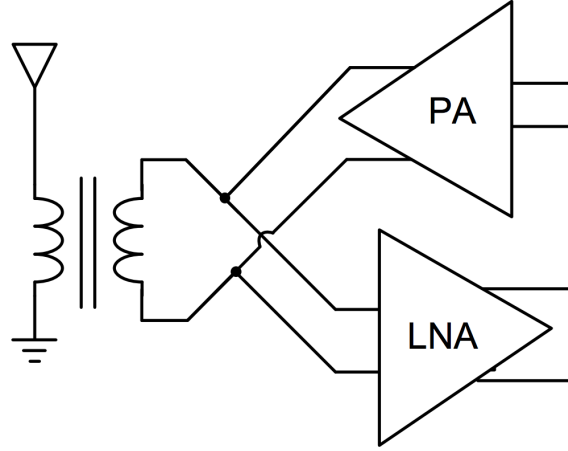


Figure 1.3: A simplified diagram of the PA and LNA receive pair connected at one transformer and antenna.

Additionally, the RF-FPGA will use an inverse class D PA as the front-end of the transmit circuitry. The class D^{-1} PA is chosen for the transmit architecture as it is efficiently scaled to support different frequency bands, allowing for the reuse of the design in all of the RF-FPGA bands.

Much of the following TDD solutions relies on at least some of the characteristics of an class D^{-1} PA. Relevant digital class D^{-1} PA characteristics will be described in Section 2, while other details go beyond the scope of this research and may be found in [5–9].

1.2 TDD Design Limitations

The focus of this work is on a fundamental issue with TDD coexistence. Attaching the transmit and receive circuitry to the same antenna exposes the sensitive receive circuitry to the high output power of the transmitter. Commonly, the power amplifier (PA) outputs a peak power of 30dBm differentially on the antenna when transmitting. Exposing the thin-oxide devices of the LNA input to this type of voltage swing will damage them. However, these cannot be changed to a more power-tolerant device without compromising efficiency of the LNA and reducing the bandwidth due to the addition of parasitic capacitors.

One solution to this ‘coexistence’ issue is a transmit/receive (Tx/Rx) switch. A conceptual image of the Tx/Rx switch is shown in Figure 1.4.

Tx/Rx switches generally perform the following functions:

1. Isolate the LNA from the large PA output power.
2. Create a high impedance node at the PA output during receive mode.

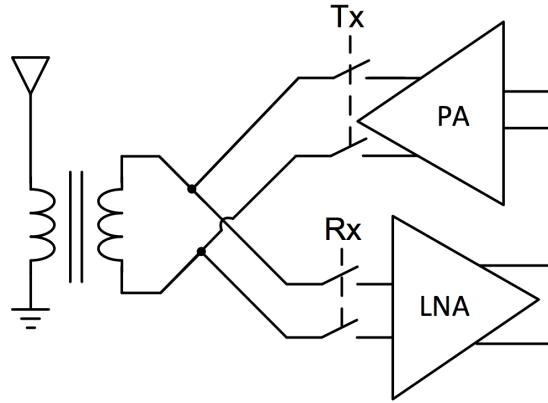


Figure 1.4: Location of Tx/Rx switch in simplified transceiver diagram. When ‘on,’ a switch connects its respective device to the antenna. When ‘off,’ the switch is open and isolates its respective device from the antenna.

3. Create a high impedance node at the LNA input during transmit mode.

PA Output Power Isolation Figure 1.3 shows how the PA output power is incident directly to the LNA. At 30 dBm or 1 Watt of output power, the PA creates a voltage of about 20 V peak-to-peak on the 50 Ω antenna. The LNA input devices cannot withstand more than a few volts across any of their terminals. In order to isolate the LNA from the PA and prevent damage to the LNA during transmit mode, a Tx/Rx switch is implemented.

PA Output Impedance Tx/Rx switches are also used to create a high-impedance node at the PA output during receive mode. For the LNA to absorb maximal receive power, its input impedance should match that of the antenna output impedance. And because the PA output and the LNA input appear in parallel to the antenna, the PA output impedance should be infinite. Thus, an isolation switch is often implemented at the PA output to create a high impedance point in receive mode.

LNA Input Impedance A high-impedance node at the LNA input is necessary in transmit mode for the same reasons the PA needs be high impedance during receive mode. However, unlike in receive mode where unretrievable signal is lost, a low impedance node during transmit mode only results in decreased PA efficiency. In addition, a capacitive low impedance node at the LNA during transmit mode may also be able to be tuned out in the matching network. For these reasons, in this discussion, we divorce the LNA input impedance during transmit mode from most of the Tx/Rx Switch design discussion.

	[10]	[11]	[12]
Loss (dB) (near 2GHz)	0.5	0.6 - 0.8	0.55
Isolation (dB) (near 2GHz)	-27	-28	-17
Power Tolerance (dBm)	34	35	34.5
Bandwidth	0-3GHz	2.4-2.5GHz/4.9-6.0GHz	0.1-2.5GHz
Technology	GaAs MESFET	GaAs pHEMT	GaAs pHEMT
Voltage	5V	3V	3V

Table 1.1: Commercially available discrete Tx/Rx switch solutions.

1.3 Prior Art

Creating a Tx/Rx switch is a challenging task. These switches impact the performance of the receiver and transceiver and still need to withstand the output power of the PA. The switch design must balance the need to protect itself and the LNA, create the desired impedance nodes, and minimally impact the performance of the overall transceiver. The focus of this work is in improving the performance of CMOS Tx/Rx switches.

Tx/Rx switches can either be outside the transceiver die and package or integrated into the same CMOS as the transceiver. A sampling of the commercially available external Tx/Rx switches is presented here first for comparison.

Discrete Tx/Rx Switches

External Tx/Rx switches can offer somewhat better performance than CMOS Tx/Rx switches and are common commercial solutions for mobile applications. Table 1.1 lists the performance and technology of several of these switches. External Tx/Rx switches generally see better performance than CMOS switches due to their ability to use exotic semiconductor processes for fabrication. For example, an external Tx/Rx switch might use gallium arsenide (GaAs), which is more power tolerant and has better device resistance and isolation properties than bulk CMOS. Unfortunately, this type of technology cannot be integrated into the same die as the CMOS transceiver.

There are additional drawbacks to these switches, including additional die pins, printed circuits board (PCB) area, and component cost. Performance of these switches depreciates from the stated value once integrated due to the loss due to loss in the I/O pads and PCB routing. Thus, it is preferable to find an on-chip solution for Tx/Rx switches.

Bulk CMOS Tx/Rx Switches

The traditional CMOS Tx/Rx switch architecture includes a series-shunt transistor arrangement on both the Tx and Rx path. This design creates a high impedance node and isolates the unused element when the opposite element is working [13], [14], [15], [16]. This design suffers from several drawbacks, such as insertion loss and poor power tolerance in

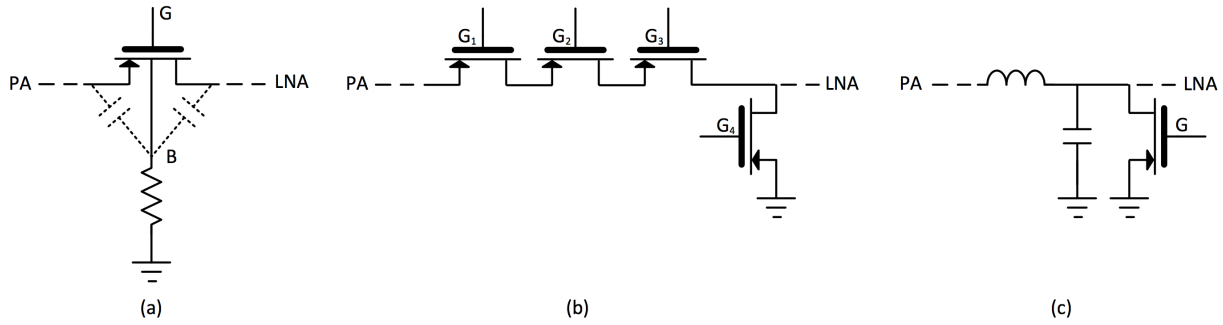


Figure 1.5: Tx/Rx bulk CMOS design strategies. (a) Floating wells allow for increased power tolerance. (b) Stacked transistors in the series leg of a series-shunt switch help to increase power tolerance. (c) Inductors act as frequency-dependent resistors when connected to ground during transmit mode, but are resonated out in receive mode when the capacitor is in use. Additional matching network components not shown.

standard CMOS. Most designs use the series-shunt topology with some application specific modifications, such as the elimination of the shunt transistors [17] to overcome these drawbacks. Switch structures which differ from this topology have been proposed [18]. However, many such designs require appreciable transceiver-level architectural consideration, and their use must be anticipated well before the design of the matching and transformer network.

Most Tx/Rx switch designs, series-shunt and otherwise, achieve the desired isolation, power tolerance, and other design metrics through at least one of three strategies.

1. Floating Wells
2. Stacked Transistors
3. Inductive Tuning

A diagram of each of these strategies may be seen in Figure 1.5. Further innovation of Tx/Rx switch design generally builds off one of these three themes.

Floating Wells Floating wells facilitate higher power tolerance. This manifests itself in two ways. First, in the case of a series switch on the transmit side, the switch transistor with a floating well is able to withstand a higher PA output power before forward-biasing source/drain to body diodes than a transistor without floating wells. This is measured as an increase in Tx mode linearity and directly corresponds to power output. [17] and [13] use this methodology. Second, floating wells allow for a the potential to have non-zero body voltages, which increases or to changes the source to body coupling capacitance, as in [14]. The change in capacitance increases isolation and subsequently, power tolerance.

Floating wells have the drawback of adding parasitic diodes and capacitances. The parasitic diodes require close attention to ensure that reverse-bias is preserved under worst-case PA output powers. The increased capacitances can impact both isolation and insertion loss, depending on the biasing technique. Thus, it is important to balance the benefits of transmit linearity, LNA isolation, and receive insertion loss.

Stacked Transistors Stacked Transistors also allow for an increased power tolerance. Stacked transistors divide the output power across several transistors, reducing the stress on each individual transistor. Effectively, the power tolerance of the switch is the power tolerance of a single transistor multiplied by the number of transistors [13, 16]. The stacked transistor method requires floating gates and source/drain regions, if not floating bodies, to achieve the increased power tolerance.

Feed-forward capacitors can be used to balance the power dissipated across each transistor and subsequently increase power tolerance [13]. This increased performance comes at the cost of die area.

In addition, the stacked methodology also comes at the cost of either increased insertion loss or increased parasitic capacitance. The insertion loss increase is due to the increased series resistance. To mitigate this, larger transistors may be used, which increases parasitic capacitances.

Inductive Tuning Inductive tuning is the most varied methodology of Tx/Rx switch design. It can vary from tuned switches, such as in [19], [15], and [20], to dedicated transformers for the receive mode which may be shorted during transmit mode [18]. Some of these techniques may create very low insertion loss and power handling. However, as the tuned switches have a reduced bandwidth, we will not consider this methodology here.

Scope of Research

The current bulk CMOS switches are almost uniformly non-ideal solutions for TDD. The series on resistance incurs loss in the receive mode and increase the LNA noise. The additional capacitance of large switch devices can also negatively impact matching in both the transmit and receive modes. An off-chip solution represents a similar amount of performance depreciation as well as other costs associated with pins and PCB area.

In the subsequent chapters, a design methodology for Tx/Rx switches and the resulting performance metrics and tradeoffs will be discussed. The floating well, stacked transistor, and feedforward capacitor techniques are used in the design of this switch, which approaches a more ideal series switch solution for low gigahertz frequencies.

Following the discussion of the Tx/Rx switch, another coexistence solution without a traditional Tx/Rx switch is proposed. Though this work is specific to the TDD solutions for the RF-FPGA project, the design methodology could be used on other PAs with similar topologies.

Extracted layout results will be reported for both designs. Comparison to the state-of-the-art in both Tx/Rx switch solutions and other front-end metrics will illuminate the trade-offs within each design methodology and between these two approaches.

Chapter 2

General Tx/Rx Definitions

It is important to understand the metrics by which we measure the performance of these coexistence solutions. In this chapter, we discuss the metrics of both receive and transmit mode of the transceiver¹. After reading this chapter, the reader should be able to easily contextualize the performance of the coexistence design discussed herein.

2.1 Tx/Rx Metrics

If the reader is familiar with amplifiers and radio frequency communications, the concepts described below will be a review. If not, this section will serve as a brief introduction to RF metrics and will provide information on the use of these metrics in this application. It is expected that the reader has at least a basic understanding of analog, transistor-level circuit design.

Receive

The primary circuit element used in receive mode is the LNA. In order to evaluate the performance of a coexistence solution, we measure the impact of the switch on the LNA metrics: gain, noise figure, linearity, and matching. To the highest degree possible, we want to make the TDD solution ‘disappear’ in receive mode, allowing the LNA to perform as if isolated from the PA. Here we introduce the metrics of interest in receive mode.

Gain and Loss

Gain In an LNA, the gain (A) is the amount by which the signal is amplified from input to output. In this case, the gain of amplifiers discussed is always voltage gain (A_v).

$$A_v = \frac{V_{out}}{V_{in}} \quad (2.1)$$

¹The theory behind these metrics and other details may be found in more completeness in [21–24].

Loss Loss measures the amount of signal removed from the signal path due to a series circuit element. It is measured as the inverse of gain across the element in question. While voltage gain can be used, it does not account for matching in the system. Thus, loss is more commonly reported as the inverse of S_{21} , or forward voltage gain, of the device under test (DUT) as it accounts for matching, making it congruent with the change in noise figure due to a passive element.

S_{21} parameter is given by the equation

$$S_{21} = \frac{V_2^-}{V_1^+}, \quad (2.2)$$

where V_1 is the wave at the input of the circuit element, V_2 is the wave out of the circuit element, and the $+$ and $-$ indicate whether the wave is incident or reflected. In this topology, loss indicates how much of the signal from the antenna reaches the LNA, and one would like loss to be near unity.

Both gain and loss metrics are often represented in their decibel form. The conversion from gain to decibels is

$$A_{dB} = 20\log(A_v). \quad (2.3)$$

Noise Figure

Noise figure gives an indication of the amount of noise a circuit element injects into the signal path. The amount of noise present at any point in a circuit may be represented by the signal-to-noise-ratio (SNR) equal to $\frac{P_{Signal}}{P_{Noise}}$, where $P \propto V^2$, P is power, and V is voltage. A representation of the amount of noise injected by a circuit element along the signal path looks at the SNR between two points: the input and output of the circuit. The equation for noise factor is

$$NF = \frac{SNR_{in}}{SNR_{out}}. \quad (2.4)$$

Noise figure, which is used in this paper, is the decibel representation of NF:

$$NF_{dB} = 10\log(NF). \quad (2.5)$$

The noise figure of a circuit can be found analytically; some examples will be seen in later chapters. However, the noise factor of a completely passive element is directly related to the behavior of the passive element, such that its noise factor is equal to the power loss.

The noise factors of cascaded elements interact. The Friis Equation provides the relationship for this interaction:

$$NF_{eff} = NF_1 + \frac{NF_2 - 1}{A_{P1}} + \frac{NF_3 - 1}{A_{P1} \times A_{P2}} + \dots + \frac{NF_i - 1}{A_{Pi-1} \times \dots \times A_{P1}}, \quad (2.6)$$

where A_p is the power gain of a stage. Thus, one can see that it is important to keep the loss of the switch low to keep its noise figure and impact on the overall system noise figure low. Increased noise figure reduces the sensitivity of the overall system and negatively affects receiver performance.

Linearity

An ideal linear circuit element has the same linear transfer function for any input power. In other words, the linear equation which maps the input to the output should be the same regardless of the input value. In CMOS circuits, there are no perfectly linear circuit elements. Physical systems exhibit different behaviors at different power levels. Most non-linear functions, however, can be approximated using a Taylor series polynomial expansion.

Two metrics are then used for linearity in this work. The first is the 1dB compression point and the second is the 3rd Intercept Point.

1dB Compression Point The 1dB compression point (P1dB) is the input value at which the transfer function differs from an extrapolated linear function by 1dB.

3rd Order Intermodulation Intercept Point The 3rd order intermodulation intercept point (IIP3) is the input value where the extrapolated 3rd order term in the Taylor series polynomial expansion overtakes the 1st order term.

The higher each of these metrics, the less of an impact the non-linearity of the circuit has on the signals of interest. If the solution is a series switch, for example, the switch should have a linearity markedly higher, no less than double, the succeeding LNA, in order to preserve the LNA's linearity.

Matching

The input impedance of a circuit element determines how much signal is absorbed and how much signal is 'reflected' off of that element ². To maximize the transmitted power and

²This idea of reflection is often explained through transmission line theory. Dissimilar impedances in series will result in some loss of signal, due to the wave-like properties of voltage and current. To elaborate, the solution to the differential equation describing transmittance of electromagnetic waves allows for both a forward and a reverse component of voltage and current. In system with a open-circuit boundary condition, the reflected wave is positive and equals the forward wave, resulting in a voltage level of a constant positive value. In an short-circuit condition, the reflected wave is negative and equals the forward wave, resulting in a voltage level of 0V. When the termination is some other impedance value, the value of the reflected wave is between the negative and positive of the incident wave value. In a condition of matched impedance, no reflection occurs.

minimize the reflected power, all input impedances in the circuit should match the output resistance of the previous series circuit element.

The two measures of matching used in this work are S_{11} and Z_{in} .

S_{11} - Input Voltage Reflection Coefficient The equation for S_{11} is

$$S_{11} = \frac{V_1^-}{V_1^+}, \quad (2.7)$$

where V_1 is the wave at the input of the circuit element and the $+$ and $-$ indicate whether the wave is incident or reflected. Thus, S_{11} is a measure of the input matching accuracy. This value should be as close to zero (or negative infinity in decibels) as possible. Because these parameters are ratios, they are inherently unit-less.

Z-Parameters Z-Parameters are a measure of the frequency dependent impedance of the circuit element in relation to the source impedance.

Z_{11} parameters are given by the equation

$$Z_{11} = Z_0 \frac{1 + S_{11}}{1 - S_{11}}, \quad (2.8)$$

where Z_0 is the frequency dependent source impedance. If S_{11} is small, this value should be nearly the value of the source impedance. Similar equations exist for relating any S_{xy} and Z_{xy} .

The Z-parameters are also used to find Z_{in} , which is similar, but not equivalent to Z_{11} , as it depends on the load. This value, instead of Z_{11} , is used to find the input impedance in a passive device.

$$Z_{in} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} + Z_L} \quad (2.9)$$

Z_{in} is used in this work.

Transmit

The primary circuit element used in transmit mode is the PA. Similarly to the LNA, the PA should function as ideally as possible, as if no coexistence solution were used. However, in transmit mode, unlike receive mode, the effects of the coexistence solution on PA performance are somewhat secondary to the protection the switch provides the LNA in transmit mode. The assumption is that it is more important to ensure the LNA survives the transmit mode than to ensure the transmit mode is optimized.

Thus, in this section, we present basic measures of PA performance and introduce the metrics that measure how well the switch isolates the LNA from the PA signal.

Output Power

Output power is the total power supplied by an amplifier. In general, the output power is calculated by

$$P_{out} = \frac{V_{rms}^2}{R_{load}}, \quad (2.10)$$

where V_{rms} is the root-mean-square of the voltage at a given node and R_{load} is the load resistance.

Drain Efficiency

Drain efficiency is a measure of how well the DC power is converted to AC power at the output of an amplifier. In general, the metric is simply

$$\eta_D = \frac{P_{out}}{P_{total_{DC}}}, \quad (2.11)$$

where DC power is the average power which flows out of the DC supply.

Power Tolerance

Power tolerance is the power level which the switch can withstand before damaging the switch transistor devices. This parameter is determined by architecture, topology, and CMOS technology. The PA output power is measured in decibel-milliwatts (dBm). In the RF-FPGA design, the PA output power seen at the LNA must be at least 12dBm single-ended before the maximum allowed voltages are seen at the transistors.

Isolation

Isolation indicates the degree to which a signal is blocked by a circuit element. The amount of signal which passes through a series circuit element is measured as the inverse of S_{21} or voltage gain across the circuit element (See A_v in 2.1). In a Tx/Rx switch, this measures the amount of the PA signal which reaches the input of the LNA. One would like isolation to be near zero, indicating that the signal is completely blocked; no signal passes through. In this case, isolation should be less than -20dB, as is standard in literature.

PA Output Waveform

It is important to note that power level and differential voltage levels across the switch depend upon the waveform incident at the switch. A common assumption for RF signals is that the signal is perfectly sinusoidal and that the initial conditions are the common mode. This, however, may not be the case. A sinusoid and the true PA output with similar common mode and power levels may be seen in Figure 2.1. As one can see, the voltage difference from common mode is greater in the true PA output than in the sinusoidal output.

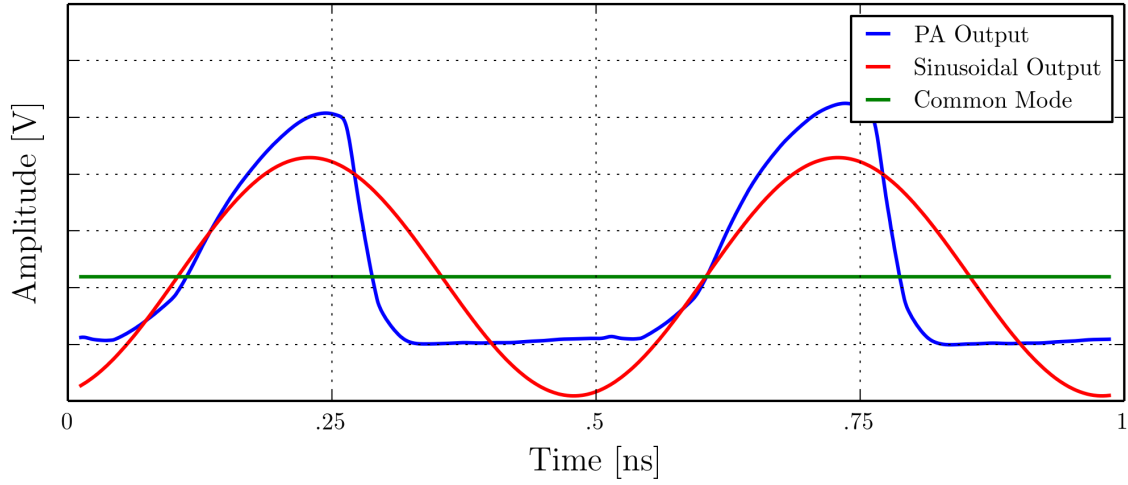


Figure 2.1: PA output and sinusoid of equal power and common-mode voltages with common-mode voltage labeled. The known inverse class D PA output and a sinusoid with similar power and common-mode levels are shown in order to illustrate the difference between the two signal shapes and their resulting voltage levels. Switch design should accommodate the worst-case PA output scenario.

In the case of an incident sinusoid, the common mode voltage is the arithmetic mean of the maximum and minimum voltage levels. For increasing power levels, the voltage levels increase identically above the common mode. If the waveform is not a sinusoid, this may not be true. In fact, as the waveform approaches a series of impulses, the common mode drops, but the voltage difference from common mode for a given power output increases. Thus, it is important to understand both the output power and signal waveform of the PA to ensure tolerable voltage levels are not violated.

Chapter 3

RF-FPGA Series Tx/Rx Switch Design and Results

The last chapters discussed both the metrics by which our switch design is measured and prior switch designs. With this context, we present the design of the RF-FPGA Tx/Rx Switch.

3.1 Tx/Rx Switch Design

Architecture Selection

The first step in designing the Tx/Rx switch is to choose an overall architecture for the switch. The architecture should specify how the switch is situated relative to the PA and LNA, how the switch creates an AC ground at the LNA input, and how the PA affects the input signal during receive mode.

A simple image of the chosen architecture may be seen in Figure 3.1. The selected architecture has only a shunt switch at the input to the LNA and series transistors to separate the PA signal from the input of the LNA.

We situate the switch between the antenna AC coupling capacitance and the LNA for isolation and biasing. The AC coupling capacitance separates the voltages of the switch drain and source regions from the PA DC voltage and allows these regions to be biased separately from the PA. In the transmit mode, the antenna side of the switch sees the AC voltage of the PA output, and the switch isolates the receiver from the transmitter output signal.

The AC ground at the LNA input is created by exploiting the differential input of the RF-FPGA LNTA. Putting a standard shunt transistor between the two differential lines shorts the input nodes of the LNA, creating a DC voltage equal to the average voltage of the two differential lines at the input to the LNA.

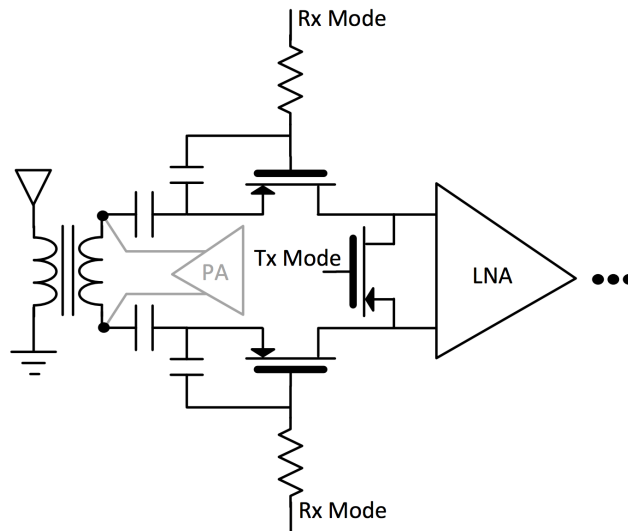


Figure 3.1: A simple differential series switch with shunt transistor. One method for creating an AC ground at the input to the LNTA is to connect the two differential inputs of the LNA with a shunt transistor. Series transistors are used to isolate the AC ground from the PA signal at the antenna.

In the RF-FPGA architecture, any single PA is in a high impedance state when not in use. This keeps the receive signal from leaking away through the PA. Thus in this design, the Tx/Rx switch is only required on the receiver side for isolation. In standard designs, the switch often is needed both on the PA and LNA side for high impedance creation and isolation respectively.

Technology Voltage Requirements and Bias Voltage Selection

Given the selected topology, the next step is to determine the bias voltages and swing limits needed to ensure that the switch survives the PA output power and operates in receive mode.

Transmit Mode

The same thick-oxide devices as the RF-FPGA PA were used in the Tx/Rx switch design to ensure compatibility with the transceiver during integration. A cross-section of a deep-Nwell device is shown in Figure 3.2. Deep-Nwell devices are used to float the device body and increase power tolerance. The acceptable DC and an AC voltage levels between each node of the device must be considered in order to ensure that the device is not damaged during ‘worst-case’ usage.

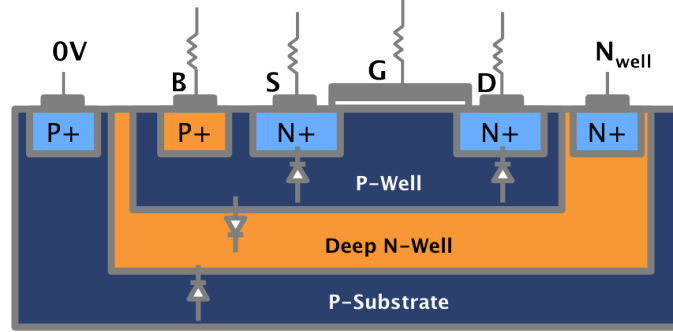


Figure 3.2: Cross-section of the deep-Nwell Devices. Thick-oxide deep-Nwell devices are used for the switch's series transistors. The deep-Nwell is set to a fixed voltage while the Pwell, gate, and source/drain nodes are free to oscillate with the incoming signal, preventing the differential voltages from exceeding the requirements of the silicon technology.

Tx	
$S, D > B$	To ensure reverse bias diodes
$B < N_{well}$	To ensure reverse bias diodes
$G < S, D$	To ensure device is off
$S_{dc} = D_{dc}$	To ensure V_{sd-max} is minimized
$V_{sd-max} < V_{ac-max}$	As per DRM
$V_{sb-max} < V_{ac-max}$	As per DRM
$V_{s-swing} - V_{d-swing} < V_{ac-max}$	
Rx	
$G > S, D + V_t$	To ensure device is on
$S, D > B$	To ensure reverse bias diodes

Table 3.1: Differential node requirements

The voltages required for this device are listed in Table 3.1.

Given the waveform of the PA output, discussed in 2.1, $V_{s-swing} - V_{d-swing} < V_{ac-max}$ is not achieved with a single transistor.

Thus, two switches must be used in series to withstand the output power of the PA, while allowing for the creation of an AC ground at the input to the LNA. Again, the bodies of these switches must be allowed to swing to achieve this increased power tolerance. The resulting topology is shown in Figure 3.3.

The bias voltages of the source and drain regions of all the devices are set by the input bias voltage of the LNA. In order for the source/drain to body diodes to remain reverse-biased and minimize the difference between the source and body voltages, the body bias conditions are set such that $B_{dc} - V_{B-swing} = S_{dc} - V_{s-swing}$, where B_{dc} is DC body voltage

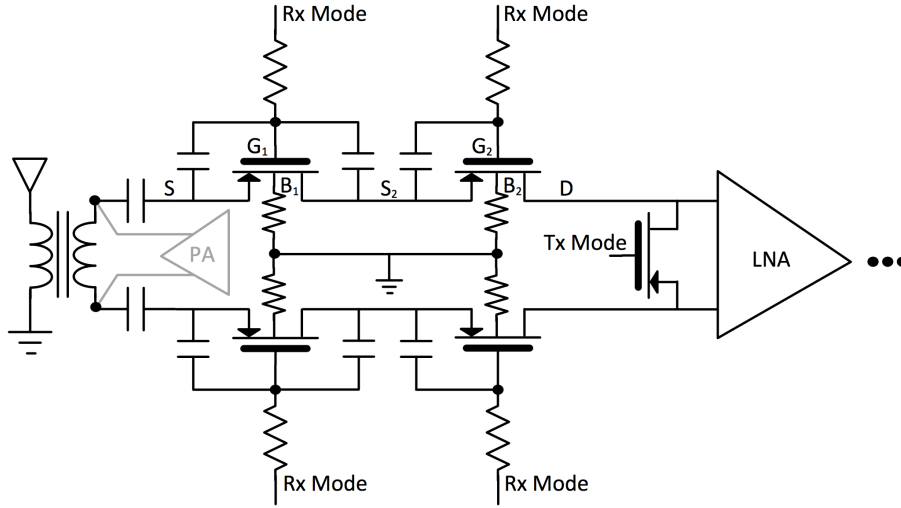


Figure 3.3: Complete switch topology. The switch uses two series transistors with floating Pwells to ensure that the differential node voltage limits are satisfied under worst-case PA output powers and waveforms.

and $V_{B-swing}$ is the amount the body voltage swings.

Now, because the body voltage is ensured to be less than both the source and drain voltages, the gate voltage is set to the body voltage as well. This keeps the device ‘off’ in transmit mode.

Given that all of the DC voltages are now set, one needs to set only the swing at each node. There are three nodes between the input node and the LNA input, for a total of five nodes. The easiest way to divide the voltage drop is by a quarter of the input voltage between each node. Figure 3.4 shows how the difference in node voltage amplitude is 25% of the input voltage.

Receive Mode

In receive mode, the conditions for functionality are more easily maintained. The devices simply need to remain completely ‘on.’ The input voltage is not expected to exceed 2V. Thus, $G_{dc} > S_{dc} + \frac{1}{2}V_{s-swing} + V_t$ and $B_{dc} = 0V$ is all that is required.

Receive Mode Noise Figure Requirements and Transistor Sizing

Once the architecture and topology is selected, one must size the transistors appropriately. The first step to determine the size of the series transistors is to analyze the impact these

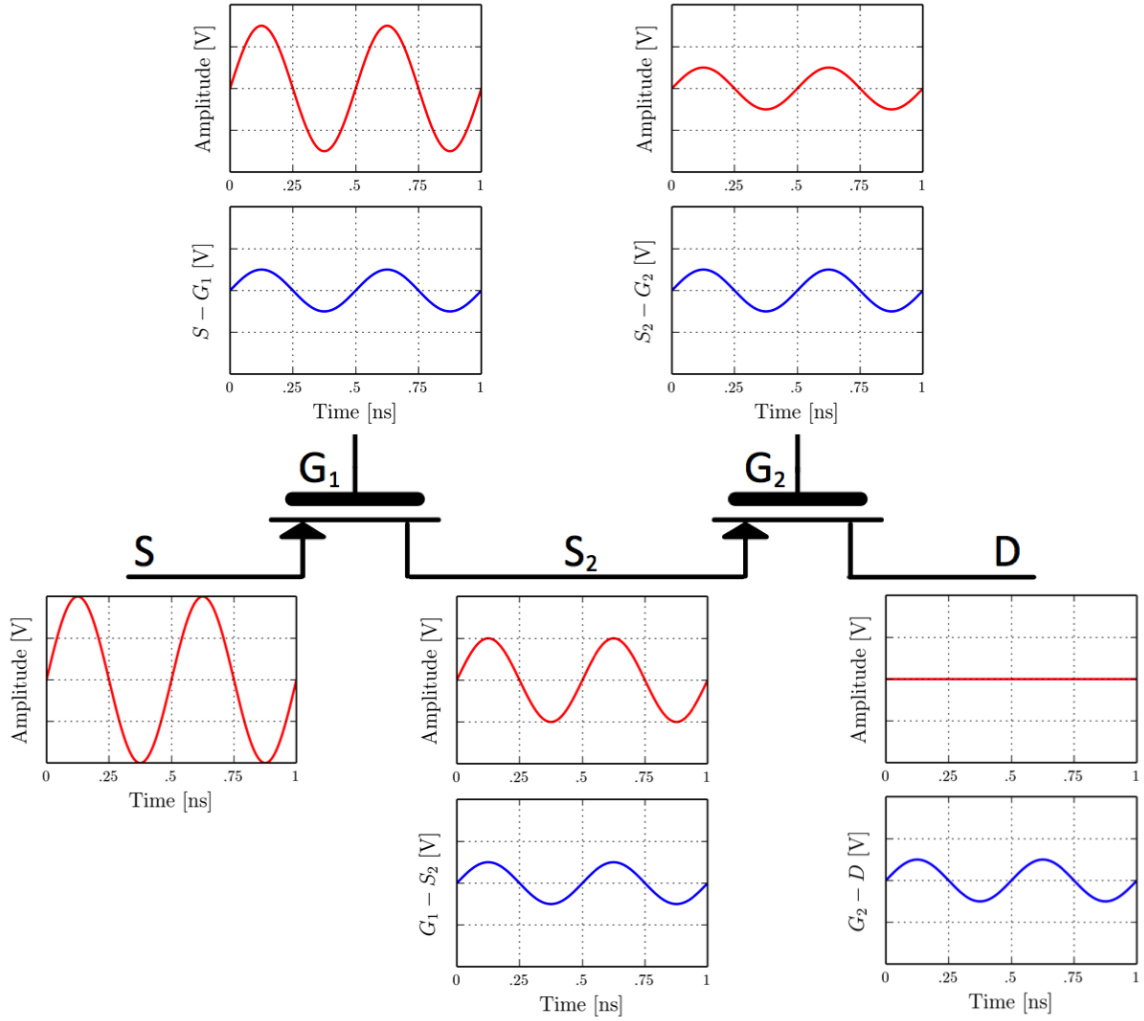


Figure 3.4: Desired node voltages at each gate, source, and drain in one series leg of the Tx/Rx Switch. The amplitude of the voltage at each node during transmit mode is represented in red. The difference in amplitude between each node is represented in blue.

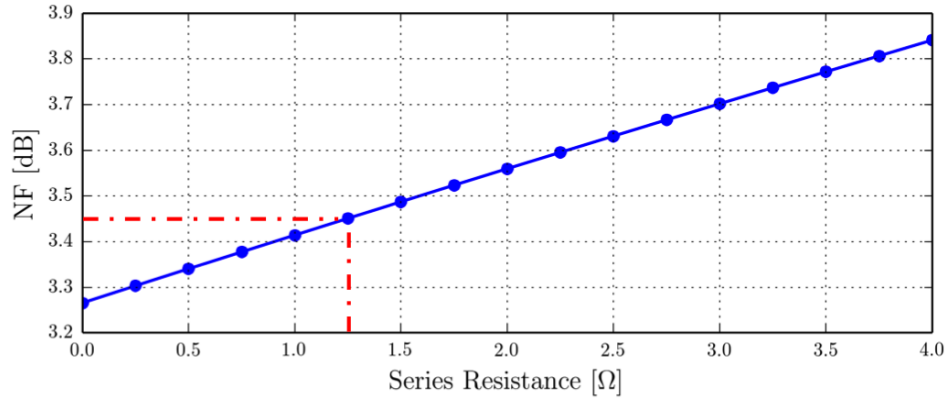


Figure 3.5: Noise figure in relation to series resistance at 2 GHz. The noise figure is sensitive to the series resistance at the input of the LNTA. A parametric sweep reveals the relation between resistance and noise figure.

transistors have on the noise figure of a potential receive system¹.

We start with noise figure, as opposed to insertion loss, because, the effects of insertion loss manifest themselves as an increase in noise figure, see Equation 2.6, and those effects help to determine the insertion loss requirement. Assuming the switch attenuation, or $\frac{1}{A_1}$, is approximately equal to its noise figure, an approximation that takes the liberty of assuming the switch is a passive device, one can see how the insertion loss both adds directly to the overall noise figure and causes an increase in the noise contribution of all further elements in the receive chain.

Thus, we characterize the impact of a resistance in series, between the transformer and LNTA, on the noise figure to determine the maximum series resistance that would deliver the desired noise figure performance. Specifications of the RF-FPGA stipulate that the simulated schematic noise figure should only be 0.2 dB greater than the NF of the LNTA without any series resistance. This is believed to give margin for an increase in noise figure due to layout.

Figure 3.5 shows noise figure in relation to various on-resistances at the input of the LNTA over a range of input frequencies. Given the NF requirement, the input resistance was capped at 1.25 Ω.

After determining the maximum series resistance, we determined the transistor size that yields no more than the maximum series resistance. Figure 3.6 shows the generalized parametric analysis performed to compare the size of the thick-oxide deep N-well device to its on-resistance. Note that because two series devices are used, the on-resistance of a single device must be half the resistance limit of 1.25 Ω.

¹The receive test structure is a version of the LNTA used on the RF-FPGA chip, designed by Charles Wu. This structure is also used in Section 3.2.

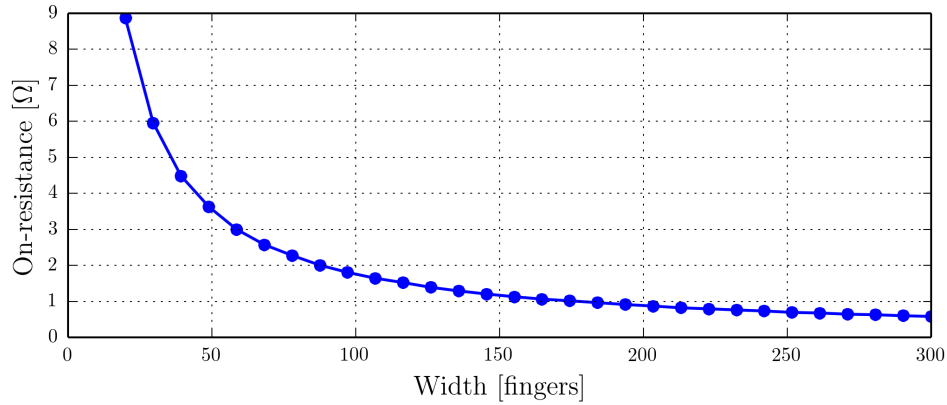


Figure 3.6: Generalized device on-resistance in relation to width. Device on-resistance is directly related to insertion loss and thus drives the selection of device width.

Isolation Requirements and Passive Selection

Given an architecture and the the size of the transistors in the architecture, we select passive components to help satisfy the isolation requirements and ensure the technology requirements, discussed in 3.1.

In this architecture, the parasitic capacitances associated with the transistors form a capacitive network, shown in Figure 3.7. From 3.1, we know the node voltages should be reduced by 25% between each node. In order to ensure these voltage requirements are met, the capacitance values must form a voltage divider accordingly.

One can determine the necessary capacitance values between each node by first determining the value of the impedance between the node closest to AC ground, G_2 and ground bottom node.

The impedance from G_2 to AC ground is

$$Z_{gg2} = \frac{1}{C_{gd2}s} \parallel \left(\frac{1}{C_{gb2}s} + \frac{1}{C_{bg2}s} \parallel R_{B2} \right) \quad (3.1)$$

$$= \frac{sR_{B2}(C_{gb2} + C_{bg2}) + 1}{C_{gd2}s(R_{B2}C_{gb2}C_{bg2}s + R_{B2}C_{gb2}s + R_{B2}C_{bg2}s + 1)}, \quad (3.2)$$

where R_{B2} is the resistor used to bias the body voltage.

One can then determine the necessary impedance value between S_2 and G_2 . The voltage ratio between G_2 and S_2 should be one half and is given by the equation

$$G_2 = \frac{Z_{gg2}}{Z_{gg2} + Z_{sg2}} \times S_2. \quad (3.3)$$

Thus, the impedance between S_2 and G_2 , called Z_{sg2} , should equal Z_{gg2} to create the voltage division equation.

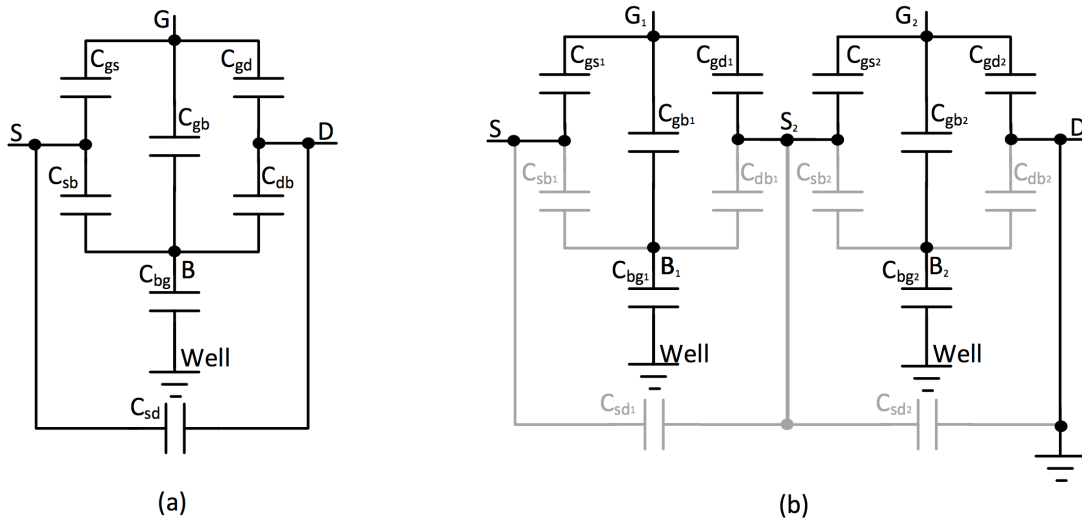


Figure 3.7: (a) Transistor parasitic capacitors. The parasitic capacitances between each node of a transistor form a capacitive network, coupling signal between each node. (b) Full parasitic capacitance network for switch topology. The signal coupled between each node is exploited to ensure the differential node voltage limits are met, as per the technology requirements. Capacitors in grey are small enough that they do not impact the coupling between nodes.

The necessary impedance value between G_1 and S_2 can be found in a similar manner. The voltage ratio between S_1 and G_2 must be two-thirds and is given by the equation

$$S_2 = \frac{Z_{gg2} + Z_{sg2}}{Z_{gg2} + Z_{sg2} + Z_{gs1}} \times G_1. \quad (3.4)$$

Thus, Z_{gs1} should equal Z_{gg2} as well.

The final impedance is more complicated. The voltage ratio between G_1 and S_1 should be three-fourths. However, the voltage division equation is given by

$$G_1 = \frac{(Z_{gg2} + Z_{sg2} + Z_{gs1}) \parallel (\frac{1}{C_{gb1}s} + \frac{1}{C_{bg1}s} \parallel R_{B1})}{(Z_{gg2} + Z_{sg2} + Z_{gs1}) \parallel (\frac{1}{C_{gb1}s} + \frac{1}{C_{bg1}s} \parallel R_{B1}) + Z_{sg1}} \times S_1 \quad (3.5)$$

From this equation, $Z_{sg1} = \frac{(Z_{gg2} + Z_{sg2} + Z_{gs1}) \parallel (\frac{1}{C_{gb1}s} + \frac{1}{C_{bg1}s} \parallel R_{B1})}{3}$.

The capacitances needed to create the voltage divider should have the impedances found in Table 3.2. The capacitance values that create the necessary impedances are likely not the same as the parasitic capacitance values. Figure 3.8 shows how the existing capacitance values may be modified by adding additional capacitors in parallel with the parasitic ones to meet the impedance requirements.

With the choice of capacitance values, the switch design is complete.

External Cap	Impedance Value
C_{gsex_1}	$\frac{(Z_{gg_2} + Z_{sg_2} + Z_{gs_1}) (\frac{1}{C_{gb_1}s} + \frac{1}{C_{bg_1}s} R_{B_1}))}{3} - \frac{1}{C_{sg_1}}$
C_{gdex_1}	$\frac{\frac{1}{C_{gd_2}s} (\frac{1}{C_{gb_2}s} + \frac{1}{C_{bg_2}s} R_{B_2}) - \frac{1}{C_{gd_1}}}{\frac{1}{C_{gd_2}s} (\frac{1}{C_{gb_2}s} + \frac{1}{C_{bg_2}s} R_{B_2}) - \frac{1}{C_{sg_2}}}$
C_{gsex_2}	$\frac{\frac{1}{C_{gd_2}s} (\frac{1}{C_{gb_2}s} + \frac{1}{C_{bg_2}s} R_{B_2}) - \frac{1}{C_{sg_2}}}{\frac{1}{C_{gd_2}s} (\frac{1}{C_{gb_2}s} + \frac{1}{C_{bg_2}s} R_{B_2}) - \frac{1}{C_{sg_2}}}$

Table 3.2: External Capacitance Values

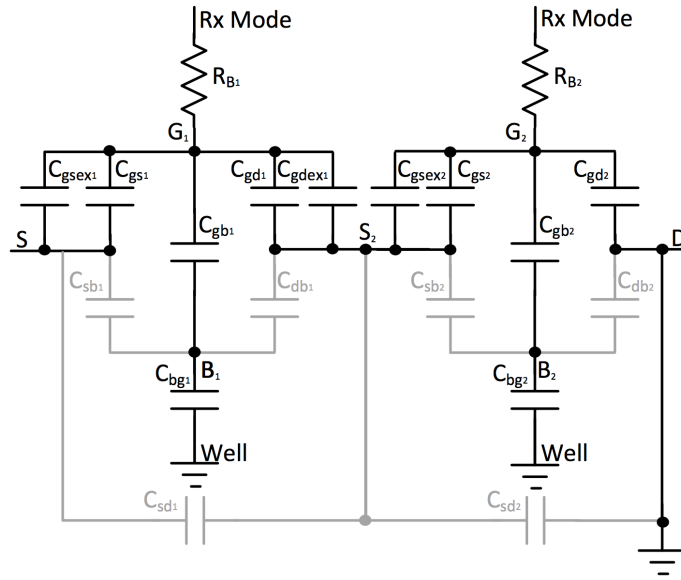


Figure 3.8: Capacitive network with external capacitances added. The external capacitances ensure the voltage divider caused by the capacitive network divides the PA output voltage down to AC ground with allowable resulting differential node voltages.

3.2 RF-FPGA Series Tx/Rx Switch Results

Section 2.1 discussed the metrics used to characterize Tx/Rx switch performance. In this section, we present the performance from layout-extracted simulations of this Tx/Rx switch.

Functionality Verification

The first step in testing the Tx/Rx switch is to look at metrics that demonstrate the primary functionality of the Tx/Rx Switch. This section discusses functionality tests from two different perspectives.

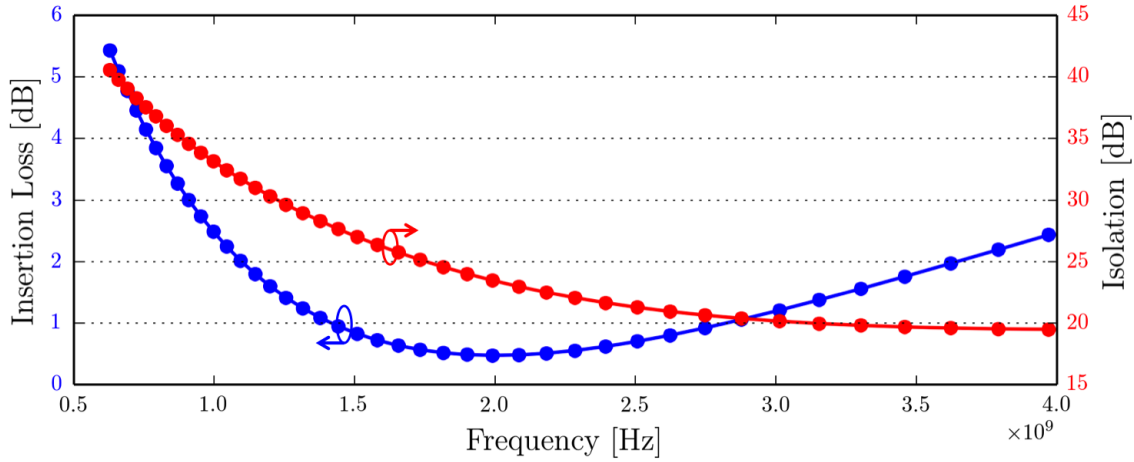


Figure 3.9: Loss and isolation of simulated extracted switch using the S_{21} parameter. The simulated loss and isolation of the extracted switch, when placed between two ideal $50\ \Omega$ ports is shown. The loss and isolation are comparable to the state of the art, discussed in Table 3.3.

The first perspective is to look at the isolated Tx/Rx switch, which provides the best perspective from which to compare the Tx/Rx switch to other works. This is accomplished by placing the switch between two $50\ \Omega$ ports.

The second perspective is in-situ. A schematic representation of a state-of-the-art LNTA, designed to function in this band, is used to understand the behavior of the switch with non-ideal loading and with respect to noise figure. This test set-up is also be used to understand the impact the Tx/Rx switch has on overall front-end performance.

In the following discussion, the input capacitance of the switch was resonated out with an ideal inductor. Inductance was placed between the two differential legs of the Tx/Rx switch, acting as the transformer inductance and creating a parallel resonant tank with the parasitic capacitance.

Loss and Isolation

The measured loss and isolation of the extracted switch between two ideal ports may be seen in Figure 3.9. These results use the S_{21} parameters of the two ports to obtain the power gain of the system, the standard by which to compare switch performance. The loss at 2 GHz in extraction is 0.48 dB and the isolation is 23 dB.

Loss and isolation performance both decrease with increasing frequency due to the capacitance in the system. As the frequency increases, the amount of signal that the parasitic capacitances shunt to ground increases, in turn, increasing insertion loss. Also as frequency increases, the amount of signal coupled to the LNTA side of the switch increases, decreasing

the effective isolation. At low frequencies, loss performance is poor due to the inductor used to tune out the input capacitance. Despite this decrease, the switch performance still falls below -20 dB of isolation and less than 1 dB of insertion loss across the entire matched frequency range, as is standard in literature.

Power Tolerance

While the isolation and insertion loss in Figure 3.9 show that the switch provides adequate attenuation in transmit mode, we need to verify that the Tx/Rx switch is capable of providing this attenuation across a large input power range in transmit mode. With a 2 GHz input frequency, the extracted transmit voltage gain was measured over input power.

Figure 3.10 shows that, in fact, to input powers up to at least 30 dBm, the Tx/Rx switch provides a constant, adequate gain of -29 dB when placed between two ideal 50 Ω ports. Voltage gain over the switch is used instead of S_{21} as this simulation is done using a periodic steady state (PSS) analysis, not an s-parameter analysis. In addition, voltage gain over the switch is a sufficient metric of isolation for our design, as isolation serves only to ensure voltage values do not damage the LNTA, not overall power values. This value is expected to differ from S_{21} as it does not account for matching in the system.

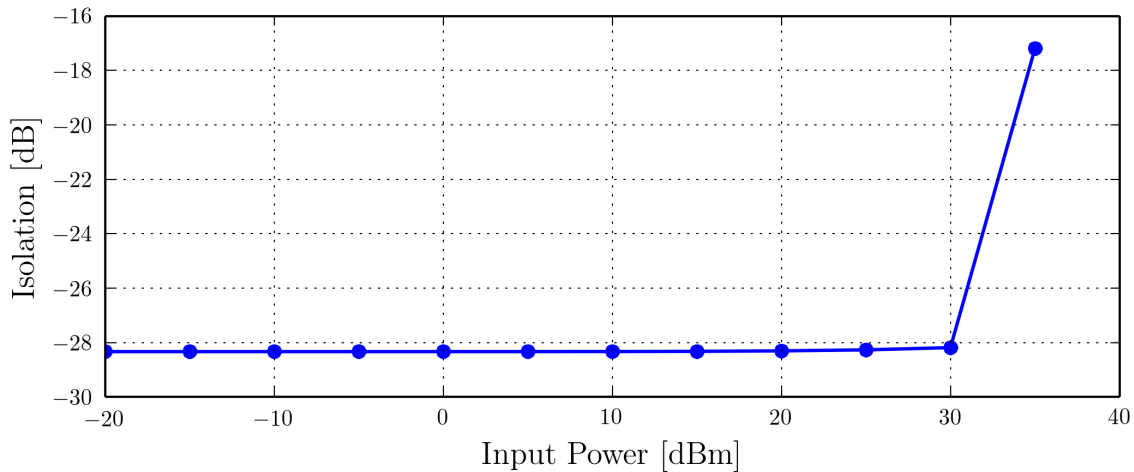


Figure 3.10: Power sweep using PSS at 2 GHz in transmit mode. The isolation (measured as voltage gain over switch) does not deviate until greater than 30 dBm of input power, showing that the Tx/Rx switch achieves the specified power tolerance.

Figure 3.11 shows that the differential node voltages during an AC simulation are proportioned as expected. Simulations were run on purely sinusoidal signals for simplicity. The AC voltage magnitude at each node in the Tx/Rx switch was measured to ensure the capacitive voltage divider worked as expected. The voltages step down from the incident voltage by

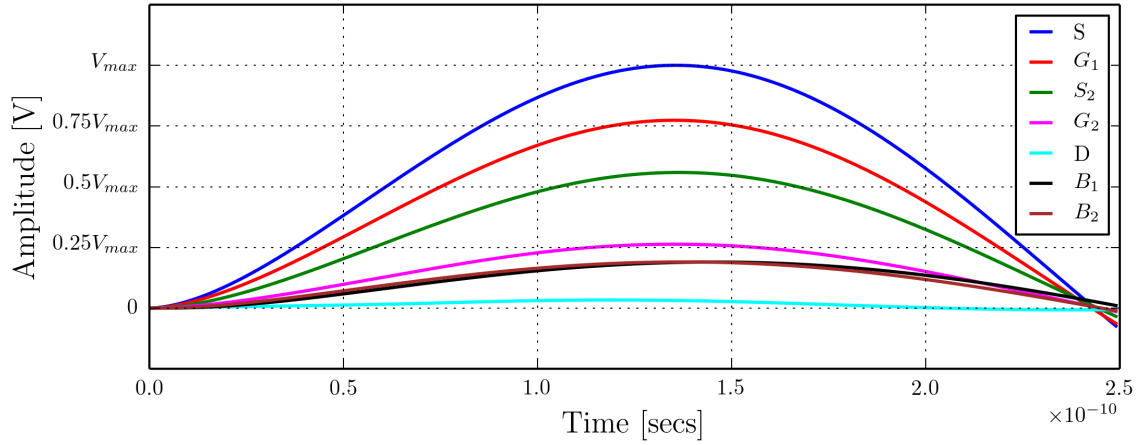


Figure 3.11: Extracted AC Node Voltages at 2 GHz, scaled to maximum input voltage and plotted with common-mode at 0 V. The voltage division works between nodes, with each node stepping down in voltage by about 25% of the total.

25% of the incident voltage at each node. It appears that the body voltage does not track the gate voltage. However, the differential node analysis shows that the voltage requirements are still satisfied, and no further coupling was implemented.

Thus, we can be assured that the Tx/Rx switch will function as a Tx/Rx switch, with adequate isolation over frequency and power and minimum insertion loss over frequency.

Input Impedance, Matching, and Noise Figure

Besides functionality, it is important to verify the matching and input impedance of the Tx/Rx switch. In this design the matching and input impedance take on special meaning because part of the Tx/Rx switch functionality is to create high-impedance/matched impedances in transmit and receive modes, respectively.

In addition, the determinant of usable bandwidth is generally not a functionality requirements, but the S_{11} and Z_{in} parameters. It is generally accepted that matching must achieve at least -10 dB of S_{11} or too much of the signal is lost for the interface to work properly.

Input Impedance Figure 3.12 shows the Z_{in} of the switch in receive and transmit mode with the same tuning inductance at the input of the Tx/Rx switch. The insert shows a magnified plot of the Z_{in} in transmit mode with the impedance on a logarithmic scale.

From this plot, one can see that the receive mode has approximately a $50\ \Omega$ impedance at the resonant point of the tank. This indicates that, in fact, matching should be adequate over at least some bandwidth.

This plot also shows the impedance the Tx/Rx switch provides to the PA. One can see that, without the loading of the PA, the high impedance range is not the same range

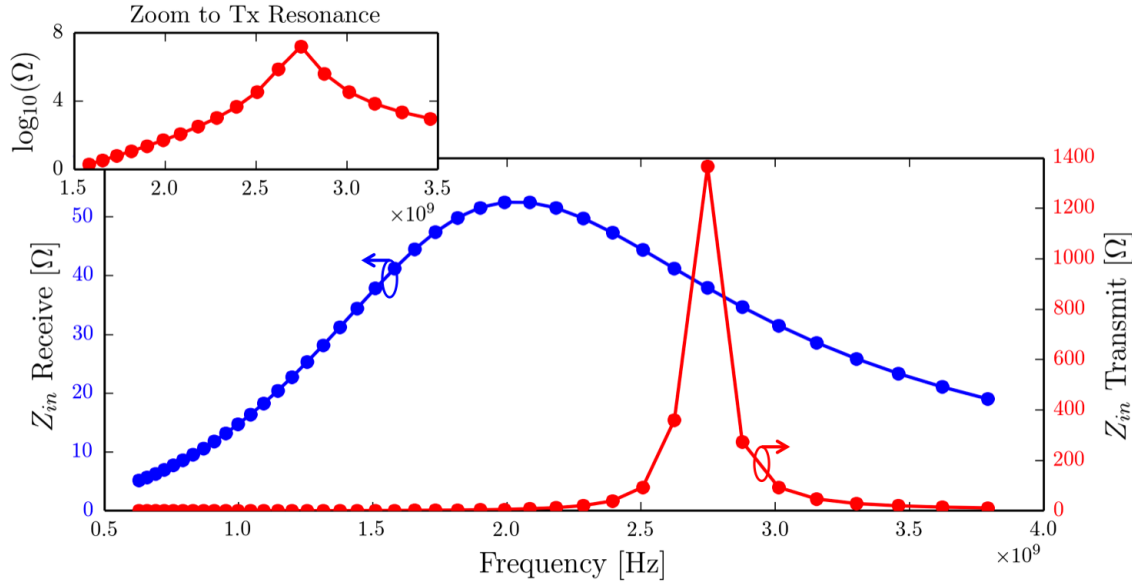


Figure 3.12: Input impedance of the Tx/Rx Switch in transmit and receive modes. The input impedance is important for proper power transfer. In transmit mode, the Tx/RX switch should have a high input impedance in order to ensure the PA output power is conveyed to the antenna and not shunted to ground. In receive mode, it is important to have a input impedance that matches that of the antenna, in order to ensure that there are not reflections of the signal.

over which the receive mode sees good matching. A change in the resonant frequency of the input tank between modes is not unexpected, however. The input capacitance of the Tx/Rx switch in transmit mode is a series combination of the coupling capacitances and the parasitic source and drain capacitances, as described in 3.1. However, the input capacitance in the receive mode is a parallel combination of the parasitic source and drain capacitances. Thus, in receive mode, the input capacitance is larger than transmit mode.

This differential in impedance matching could be a drawback if the designer wants a truly ‘drop-in’ solution for Tx/Rx isolation. However, in the case of a class D^{-1} amplifier, which is the expected application of this switch, a similar change in capacitance occurs when the PA switches to transmit mode. In receive mode, the PA will have all the transistors turned ‘off.’ But in PA mode, the cascode transistors of the PA are turned ‘on,’ exposing an additional source and drain capacitance not seen in receive mode. Thus, we present this impedance differential here to show that, in fact, both impedances may be achieved from the same switch, and leave it to the designer to ensure that the transmit high-impedance and receive matched impedances are well aligned.

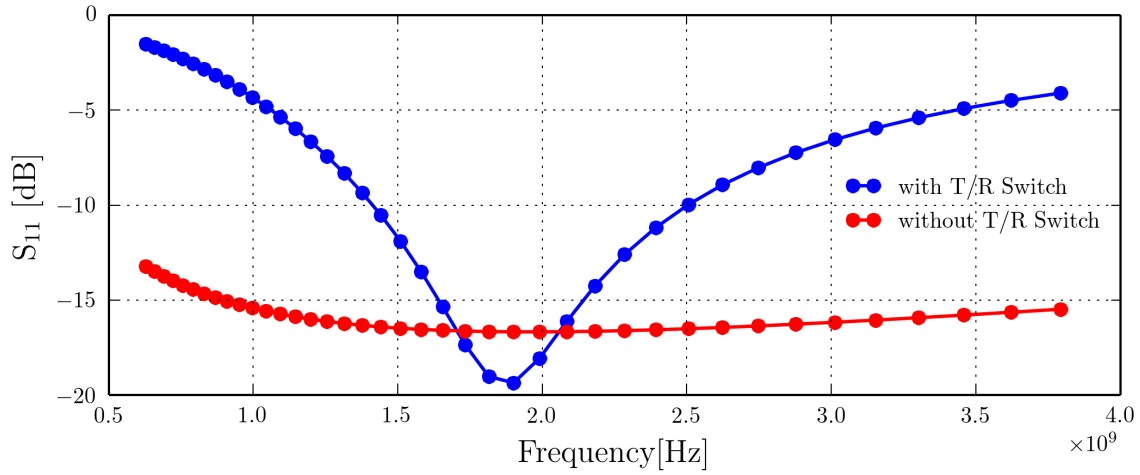


Figure 3.13: S_{11} of LNTA with and without Tx/Rx Switch. The -10 dB mark delineates the edge of the matched band, making the bandwidth 1.4-2.5 GHz

Matching Figure 3.13 shows that the input impedance is matched only from 1.4 to 2.5 GHz with the LNTA attached.

As can be seen, the amount of capacitance at the input node significantly depreciates the usable band of this LNTA. The capacitance at this node is high both because of the capacitors added for the voltage division and because of the size of the switch devices. These switch devices must be large to reduce insertion loss and mitigate increases to noise figure. As can be seen in Figure 3.6, the sensitivity of the on-resistance to device width drops after about $1\ \Omega$ of on-resistance. In this system, insertion loss was optimized. However, this small sensitivity means relatively large changes in device size may cause relatively small increases in insertion loss and may allow for increased matched bandwidth.

Noise Figure The effects of poor matching are also evident in the noise figure. The poor matching acts like an additional loss in the system and increases the overall noise figure of the front-end. Figure 3.14 illustrates how the poor matching at the Tx/Rx switch degrades the noise performance of the LNTA.

In the band where S_{11} is less than -10 dB, the noise performance is at an acceptable level, less than 4.5 dB, and with only a .42 dB increase from the LNTA without the switch. However, the overall noise figure performance follows from the matching performance. Poor matching acts similarly to additional loss in the system. Thus, when the matching is poor, the noise figure also increases.

The Tx/Rx switch's impact on matching is a design drawback of the switch.

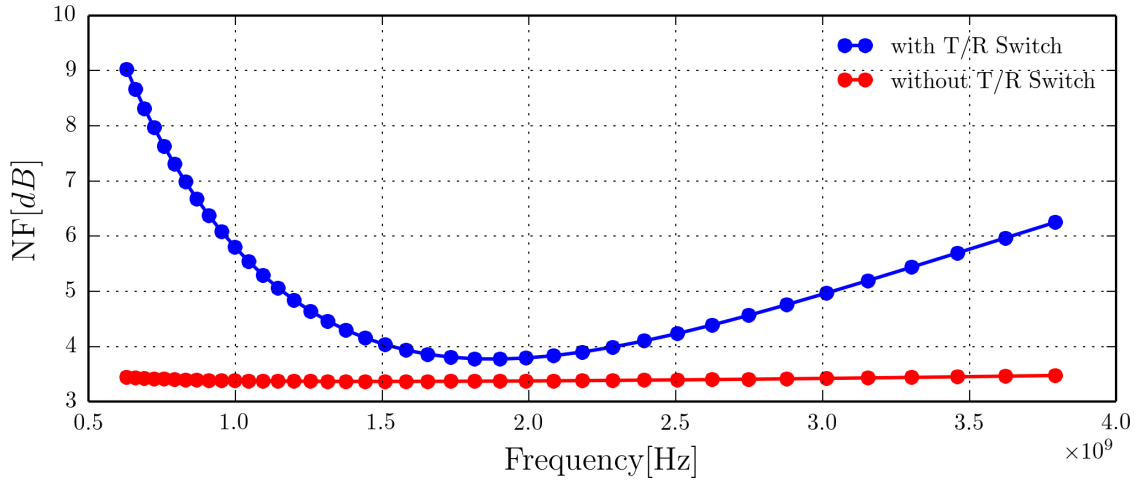


Figure 3.14: The noise figure of the schematic LNTA and the LNTA with the extracted switch.

	[17]	[13]	[14]	This Work
Loss (dB) (near 2 GHz)	0.9	1.2 ^a	2.8	0.48
Isolation (dB) (near 2 GHz)	-43	-25	-19	-23
Power Tolerance (dBm) ^b	30	28	18	30
Isolation Bandwidth	20 GHz	3 GHz	30 GHz	3 GHz
Technology	130 nm	130 nm	130 nm	65 nm
Voltage	2 V	3.3 V	1.2 V	2.5 V

Table 3.3: Comparison of Tx/Rx simulated extracted switch performance with prior art.

^awithout cap

^bTx P1dB

Comparison to Prior Art

Table 3.3 presents metrics by which to evaluate this Tx/Rx switch's performance. In comparison to other works, this switch performs well in receive mode, with one of the lowest insertion losses and an isolation comparable to that of other switches.

From Table 3.3, we can see that, with the exception of isolation bandwidth, the extracted simulation results of the Tx/Rx switch meet or exceed the current state-of-the-art in Tx/Rx CMOS functionality. The isolation bandwidth is lower in this design than other designs due to the trade-off between device size and loss. Larger devices provide less isolation but also less loss than a smaller device. As this switch is not designed to be used beyond about 3 GHz, isolation was not optimized for higher frequencies.

Parameter	No Switch	Extracted
NF (@2 GHz)	3.38 dB	3.80 dB
S11 (1.4-2.5 GHz)	<-15 dB	<-10 dB
Linearity (P1dB)	11.97 dBm	13.90 dBm ^a

Table 3.4: Comparison of simulated LNTA performance with and without the Tx/Rx switch.

^aSchematic only

Comparison to a System without a Tx/Rx Switch

While Table 3.3 shows the performance of the Tx/Rx switch in relation to other Tx/Rx switches, it is important to consider the absolute measure of the Tx/Rx switch performance: how the Tx/Rx switch impacts the performance of the overall front-end of a system.

Tables 3.4 presents the impact of the Tx/Rx switch on the receive mode of the LNTA test structure. As expected, the performance depreciates from the performance of the LNTA alone. However, the overall results show an acceptable level of performance degradation within the matched band. The matched band, however, is more narrow than desired.

The reader may wonder why linearity actually improves between the LNTA and the LNTA with a switch. This is due to the loss across the switch as well as some loss from poor matching. These two losses combine to keep the LNTA incident power lower for a given input power, and thus, increase the amount of input power the LNTA can tolerate. The Tx/Rx switch has a P_{1dB} of 25.3 dBm, more than twice that of the LNTA alone, preventing any negative impact to the main signal linearity from the switch itself.

3.3 Conclusion

In conclusion, the Tx/Rx switch design achieves the power tolerance, isolation, and insertion loss of the state-of-the-art. Taken as is, it provides a high power tolerance with minimal insertion loss. In fact, this performs quite well as a narrow-band, power tolerant, CMOS switch.

However, the input capacitance of the Tx/Rx switch has a detrimental effect on the usable bandwidth of the transceiver. Additionally, AC coupling capacitors, used in this design to allow for different common-mode biases between PA and the Tx/Rx switch in transmit mode, are troublesome. They need to be off-chip and require I/O pins.

Thus, while the Tx/Rx switch provides a generalized solution to coexistence in time-division duplexed systems, it does become impractical. Further chapters will discuss other solutions to the TDD coexistence problem.

Chapter 4

Principle of Device Reuse between LNA and PA

The Tx/Rx switch structures in CMOS do not offer the desired performance at high frequencies. The RF-FPGA project needs a TDD solution beyond 3 GHz. Though not a drop-in solution, an alternative is to eliminate an explicit Tx/Rx switch completely while satisfying the requirements:

1. Isolate the LNA from the large PA output power.
2. Create a high impedance node at the PA output during receive mode.
3. Create a high impedance node at the LNA input during transmit mode.

The first requirement offers some insight into what might be done to eliminate the Tx/Rx switch. The PA is able to withstand its own output power. Thus, the LNA may be able to take on some or all of the PA characteristics which enable this power tolerance, in order to eliminate the Tx/Rx switch.

4.1 The PA's Inspiration for Switch Design

Each of the the PA unit cells are not necessarily operational while the PA is transmitting. The devices within the PA are able to withstand the output power of the PA because the cascode device is biased such that approximately half of the PA output power is dropped across that device and half across the driver device at the bottom of the stack, keeping the total voltage drop across any node (gate-drain, gate-source, drain-source) below the technology limits.

Designing a switch with the voltage division paradigm in the PA requires devices which are prohibitively large. Due to the static gate bias, this design may also suffer from linearity limitations in receive mode. Instead, the front-end of the LNA can be designed with the

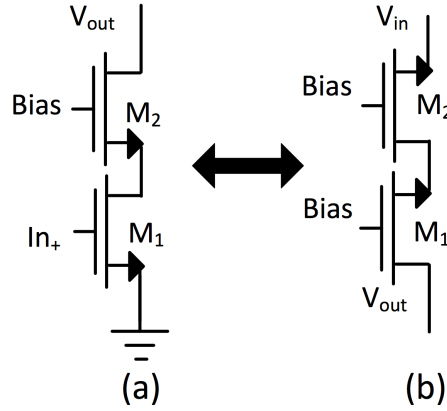


Figure 4.1: (A) Leg of class D^{-1} PA (B) Simple common gate amplifier with cascode.

same devices PA, allowing for this biasing without the corresponding loss. Figure 4.1 shows the topology from the PA which would be required for the input of the LNA.

One may recognize the devices in Figure 4.1 as the basis of the standard common-gate amplifier with a cascoded output. This is a common device used in wide-band LNAs for its ability to be matched across a wide range of input frequencies. Thus, we propose using the two device topology for the LNA as well as the PA.

4.2 Device Reuse between PA and LNA Functionality

One may notice that, as this is a TDD system, the LNA and PA operation is orthogonal. Therefore, instead of supporting additional circuitry for the LNA on the same transformer, the PA can simply be reused as an LNA when the system is in receive mode. This cannot be accomplished without modifications to the PA. However, these changes can be made simply by placing switches in the system.

Figure 4.2 show the location of each switch necessary to support the PA and LNA functionality using the same devices.

PA Ground Switch Switch A in Figure 4.2 grounds the source of the PA driver devices when transmitting and allows the LNA signal to pass out of the common gate LNA when receiving. We call this the PA Ground Switch in the following discussions.

LNA Load Switch Switch B in Figure 4.2 connects the power source to the LNA load when receiving and opens to allow for a ground node during transmit mode. This switch is the LNA Load Switch in the following discussions.

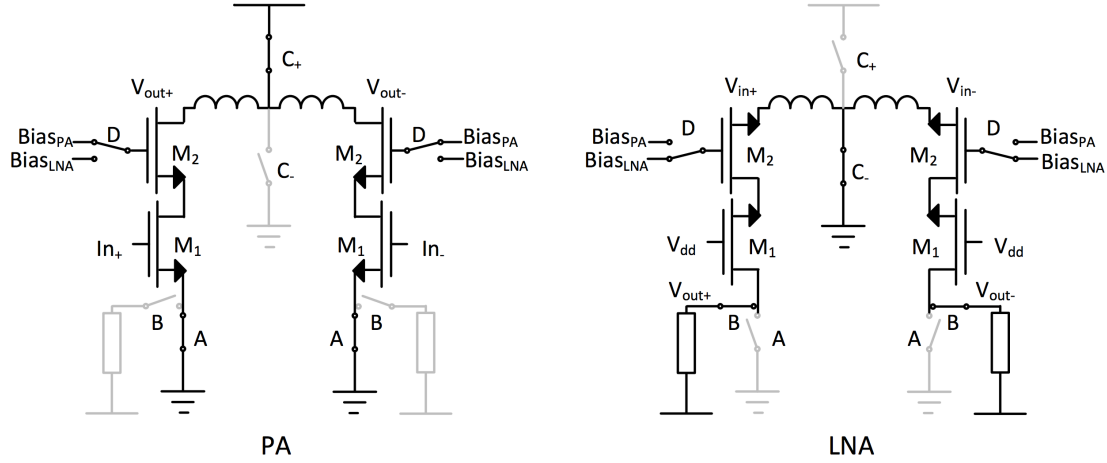


Figure 4.2: Device reuse between a class D^{-1} PA and a common-gate LNA. A series of switches, notated A-D, allow the class D^{-1} PA to share the same transistors as a common-gate LNA.

Center Tap Switch Switches C+ and C- in Figure 4.2 connect the power source to the PA transformer during transmission, while providing ground to the LNA while receiving. This switch is the Center Tap Switch in the following discussions.

Cascode Bias Switches Switch D in Figure 4.2 changes the functionality of device M_2 in Figure 4.2 from the cascode of the PA to the common-gate input of the LNA. This switch is called the cascode bias switch. Further discussion will reveal that, in implementation, the cascode bias switch is a collection of different switches. But, for conceptual purposes, it can be considered one switch unit.

PA and LNA Design Considerations

Traditionally, PAs and LNAs are designed independently. One is able to choose the device sizes, output impedances, and other parameters of the two designs with little to no consideration of the other device's performance.

However, the shared devices in this design cause the PA and LNA performance to be inextricably linked. In this case, the design paradigm was to preserve, to the greatest extent possible, the class D^{-1} behavior of the PA. Thus, this work assumes that the LNA will occupy one or more unit cells of the PA and that the LNA will not play a role in sizing the PA unit cells. Further discussion of the performance trade-offs and the design around them will be addressed in the following chapter.

Chapter 5

Design of LNA and PA with Device Reuse

The previous chapter introduced the concept of device reuse between a digital PA and a common-gate LNA. This chapter provides the background and design details necessary for implementation of the LNA and PA.

5.1 Inverse Class D PA Background

Though the class D^{-1} PA is not the focus of this work, background on the operation and topology of the device is necessary to understand the overall design. In this section, we cover some basics of operation, the number and content of the unit cells, and a high-level overview of the final layout.

Basics of Operation

The class D^{-1} PA used in the RF-FPGA design is a digital PA which uses discrete codewords to create the varied amplitudes the PA requires for RF transmission. Codewords are fed serially into the chip and deserialized for implementation in the PA. Each deserialized bit corresponds to a single PA unit cell. If a unit cell is operational, the two legs of the cell alternate state, from ‘on’ to ‘off’ and vice-versa. This alternation draws current through the transformer, which acts as a power combiner for all of the unit cells.

The Unit Cell

The unit cell of this class D^{-1} PA contains only the legs of the PA and the drivers for these legs. See Figure 5.1 for a unit cell schematic. The positive and negative drivers in a particular unit cell switch with opposite phase to produce the output frequency of the PA, if a unit cell is operational at any given time. Unit cells increase the output amplitude of the

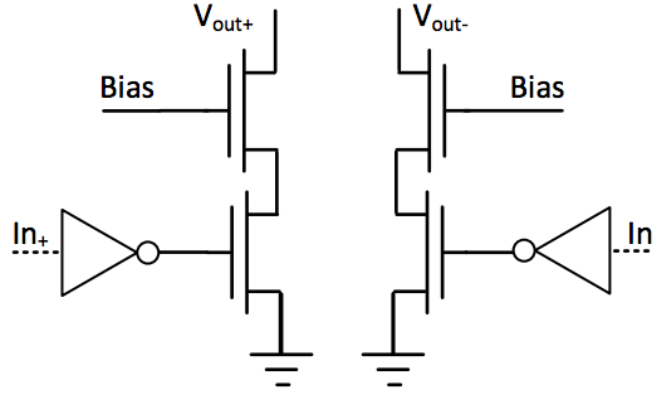


Figure 5.1: PA unit cell schematic. A single digital PA unit cell contains only the positive and negative driver devices, their corresponding cascode devices, and driving inverters.

PA either linearly or by a power of two, depending on function. There are 15 linear unit cells in this implementation, called thermometer cells. There are 4 unit cells which each double the prior's output power, called binary cells. Together, these 19 cells form a single PA array.

Two vs. One PA

The PA should have a low output impedance in order to maximize PA efficiency. However, the LNA should have a higher input impedance, in order to keep g_m low and minimize power consumption while still achieving input matching. As such, this design uses two PAs on the same power combiner. A power combiner divides down the output impedance of the PA by the number of instances in the combiner. In this case, two stages were used, making the impedance seen at the output of a single PA equal to half the antenna impedance.

Each PA has a unit cell sized half that of a full PA. This creates a PA which functions identically to a full class D⁻¹ PA, but divides the transformer to better support the LNA functionality. A diagram of the two PAs and the power combiner may be seen in Figure 5.2.

5.2 Common Gate LNA Design

Several common common-gate LNA topology choices were made in the design of this LNA to increase efficiency, maintain the desired bandwidth, and facilitate noise performance and input matching. This section touches on each of those choices and the purpose for these choices. Finally, this section provides a procedure for designing LNAs from the unit cells of digital PAs.

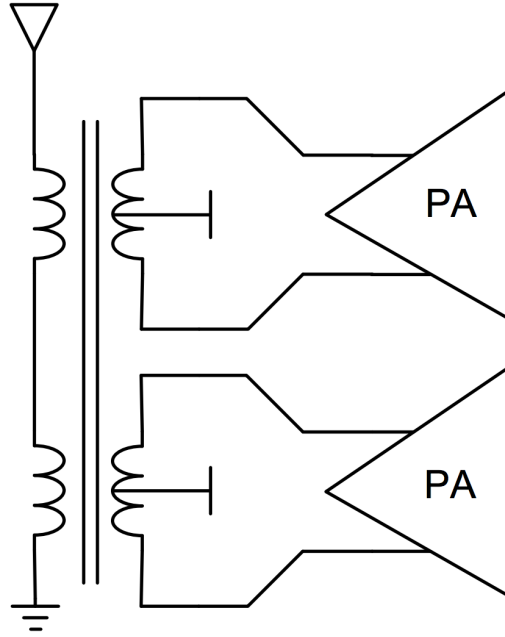


Figure 5.2: Two class D^{-1} PAs on the same power combiner. With a power combiner, the unit cells of each PA may be half the size of a unit cell in a standard digital PA and will see half the output impedance. This topology allows the PA and LNA to have differing input impedances. It also reduces noise in the LNA design, discussed in the following parts of this chapter.

Gm-boosting

A increases the efficiency of a differential common-gate LNA is to capacitively couple the inputs of the LNA to the gate of the device with opposite polarity input, increasing the effective g_m [25], but without increasing the DC drain current. The effect of gain boosting on the is g_m :

$$g_m = \frac{\delta I_d}{\delta V_{gs}} \quad (5.1)$$

$$G_m = \frac{\delta I_d}{\delta V_{in}} \quad (5.2)$$

$$V_{gs} = 2V_{in} \quad (5.3)$$

$$G_m = \frac{\delta I_d}{\frac{1}{2}\delta V_{gs}} = 2g_m \quad (5.4)$$

However, this factor of two is not perfect. The capacitive coupling is subject to a capac-

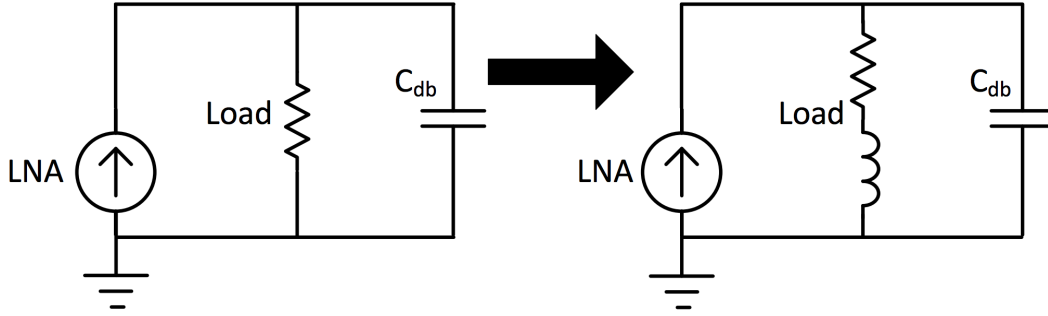


Figure 5.3: The current low-pass filter created by the g_m stage of the LNA, the restive load of the LNA, and the parasitics at the output of the LNA. This low-pass filter may be transformed to a band-pass filter through the use of a series load inductance; the resulting topology is called shunt-peaking.

itive voltage division between the coupling capacitor C_c and the gate capacitance C_g of the transistor. Instead, the effective G_m maybe found in Equation 5.5.

$$G_m = \left(1 + \frac{C_c}{C_c + C_g}\right) g_m \quad (5.5)$$

In this case, the target G_m was 1.5, where $C_c = C_g$.

Shunt-Peaking

The output of an LNA is inherently limited by the low-pass parallel RC filter created between the load resistance and the load capacitance at the output of the LNA. By placing an inductor also in parallel with these, one resonates out the capacitance. Selecting the inductor to resonate with the capacitor will effectively center the LNA gain at the desired center frequency, as opposed to being limited by the cut-off frequency of the RC filter. A diagram of this effect may be seen in Figure 5.3.

The resonant frequency is set by

$$\omega_o = \sqrt{\frac{1}{LC} \left(1 - \frac{CR^2}{L}\right)}. \quad (5.6)$$

The resistance and inductance value should also be selected while accounting for bandwidth and maximum impedance, which can both be found through the overall transfer function of this circuit.

$$Z(j\omega) = R \frac{1 + j\omega \frac{L}{R}}{1 - \omega^2 LC + j\omega CR} \quad (5.7)$$

One can find the optimal inductance and resistance for shunt peaking by solving these equations for the 3dB points and the desired center frequency.

Input Tuning

Impedance Matching and Noise

The standard noise figure equation for a common-gate amplifier where all impedances are matched is

$$NF = 1 + \frac{\gamma}{2} + \frac{2}{g_m R_L} \quad (5.8)$$

However, the equation for noise figure with unmatched impedances becomes [26]

$$NF = 1 + \frac{\gamma}{2} \frac{R_{in}}{R_s} + \frac{\left(\frac{R_{in}}{R_s} + 1\right)^2}{g_m R_L \frac{R_{in}}{R_s}}. \quad (5.9)$$

If one assumes $g_m R_L \gg 1$ and if the impedance from the antenna side of the transformer is slightly higher than the input impedance, the noise figure can be reduced. Thus, care was taken to make the input impedance of the LNA lower than the antenna impedance by about 20%, in order to take advantage of this property while still preserving reasonable input matching.

Tank Noise

It can be shown that the transformer causes the noise contribution of all LNA elements to scale approximately as a function of

$$|V_n|^2 \left(1 + \frac{C \times R_{par} \times R_s}{L}\right)^2, \quad (5.10)$$

where R_{par} represents both inductor parasitic resistance and series routing resistance.

As such, it is important to lower the capacitance at the LNA input and increase the inductance as much as possible. We were able to achieve this through strategically picking center tap locations for the PA and LNA. This strategy is shown in Figure 5.4.

This use of the power combiner to support the LNA allows for the LNA to maintain a large input impedance, as mentioned in 5.1. It also allows for the inductance seen at the input of the LNA to be large, as compared to the inductance of a single transformer on the power combiner.

It might be worthwhile at this point to note that the capacitances seen at the input node in PA and LNA mode differ. This is due to the nature of the PA, where the cascode devices are always on, exposing the two drain capacitances and a source capacitance to the input

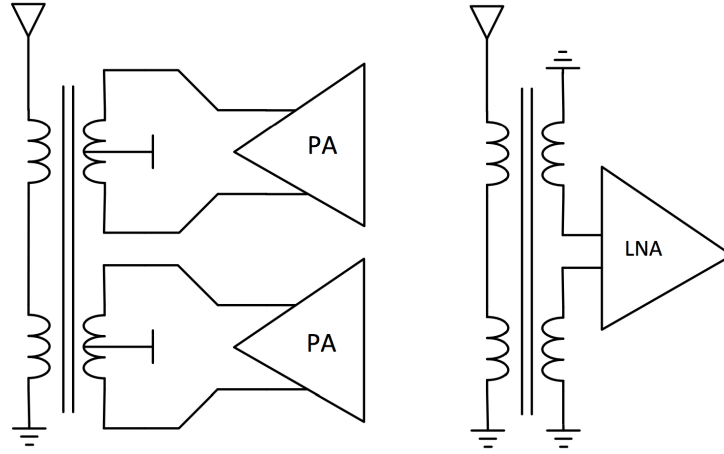


Figure 5.4: The PA and LNA center tap locations. By making the center tap locations different depending on mode, the input impedance and parallel inductance can be optimized for each mode.

node. However, this is not the case in LNA mode, where the PA cascode devices may be off when not in use. Thus, changing the inductance between modes may actually help recenter the two resonant points, as opposed to pull them apart, as would be the case if the PA and LNA had identical input capacitances.

Capacitive Tuning

The bandwidth of the input impedance of the LNA is limited by the Q of the transformer network. Unfortunately, it is difficult to broaden this Q without sacrificing noise figure. Instead, if one is able to add or subtract capacitance from the input of the LNA, one can effectively tune the resonance frequency of the tank, such that with two or more tuning points, the entire band of interest sees a well matched input impedance.

$$\omega_0 = \frac{1}{\sqrt{L_{eff}C_{eff}}} \quad (5.11)$$

$$C_{eff} = C_{static} + C_{tuning} \quad (5.12)$$

In this implementation, additional C_{tuning} is added to the input tank by turning ‘on’ the cascode devices in the unused legs of the PA, the legs in which the devices were otherwise biased ‘off’ to create an open node. Turning the cascaded devices ‘on,’ the tank input sees both the source and drain capacitance of these devices and the drain capacitance of the driver devices. With the cascode devices ‘off,’ the tank only sees the cascade’s drain capacitance.

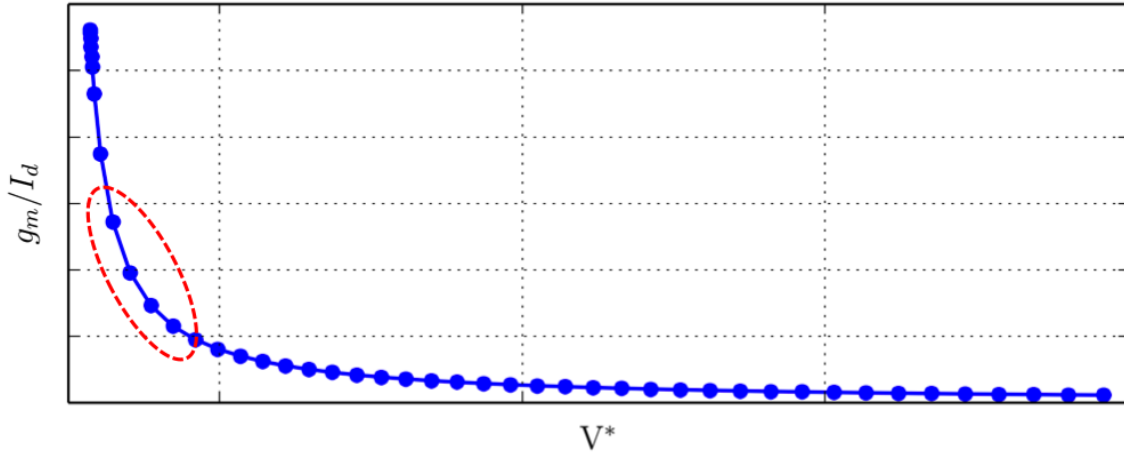


Figure 5.5: Unit cell efficiency where $V^* = \frac{2I_d}{g_m}$, a measure of saturation in short-channel devices.

The extra $C_{db} + C_{ds}$ is used to shift ω_0 and increase the overall impedance bandwidth of the LNA input.

Unit-cell Selection Procedure

While this LNA design follows a mostly standard design procedure, there are some slight differences, given that the LNA must correspond to some discrete number of PA unit cells. Thus, the design procedure is described herein.

Single Unit Cell Efficiency

The first step to designing the LNA from PA unit cells is to characterize the extracted devices within the PA. From there, the efficiency or $\frac{g_m}{I_d}$ vs. V^* curve is used to find an optimal point of efficiency. $V^* = \frac{2I_d}{g_m}$ and is used in place of $V_{od} = V_{gs} - V_{th}$ for short channel devices in order to determine the depth of saturation in the device. It is important to select a point on this curve where efficiency is maximized, but also a point which is well in saturation to avoid large performance variations over bias voltage variation. Figure 5.2 shows the approximate location of the the optimal efficiency.

Once the point of optimal efficiency is found, one correlates that V^* back to a g_m value.

Input Matching with Discrete Unit Cells

The input impedance of a common-gate LNA is approximately $\frac{1}{g_m}$. However, with the described g_m boosting method, the required input impedance was not equal to $\frac{1}{g_m}$ but $\frac{1}{G_M} =$

$$\frac{1}{1.5g_m}.$$

In this case, a single leg of the LNA could have a single-ended impedance of somewhere between 15 and 20 Ω in order to minimize the noise figure and still achieve adequate input matching over the band.

With g_m boosting, the required total LNA g_m then becomes equal to .033S-.04S. Thus, the number of PA unit cells required is simply $\frac{.04}{g_{m-cell}}$, biased at the V_{gs} corresponding to the V^* found in 5.2.

Before finalizing the number of unit cells and the bias voltage, it is important to verify that the corresponding current with the number of unit cells used is acceptable. This can be easily found by corresponding the V^* used to a current value, multiplying by the number of unit cells, and then multiplying by 2 for both legs of the LNA.

Coupling-Cap Determination

The final note about unit cell selection is that the C_{gb} of each unit cell is an important parameter to characterize in addition to g_m , I_d , and V^* . The C_{gb} multiplied by the number of unit cells determines the size required for C_c .

Cell Location in PA

The LNA devices, such as the PA Ground switch and g_m boosting, will have an impact on the performance of the PA. Most importantly, it will cause these unit cells to behave differently than the other cells, reducing the cell matching and linearity of the PA.

In order to have the minimal effect on the PA, the LNA cells were chosen to be the two PA cells which are turned-on as the last and second to last bit in the PA output scale. These cells are activated when the PA already sees some compression from the ideal input to output transfer function. And in effect, the mismatch due to the added LNA elements will be masked by this compression.

Finally, the physical location of the location of the cell needs to be selected. The PA unit-cell assignment is generally dithered in order to mitigate linearity issues due to gradients across the PA core which change performance between unit cells. This arrangement, however, placed the unit cells corresponding to the last and second to last bit in the PA output scale a part from each other and somewhat far from the PA array edge. In the PA for this LNA implementation, these two cells were brought to the center of the complete PA array, where the two PA devices connected to separate turns of the transformer meet. This facilitated the LNA output routing and was necessary to preserve the bandwidth of the LNA. A diagram of the PA layout with the LNA unit cells may be seen in Figure 5.6.

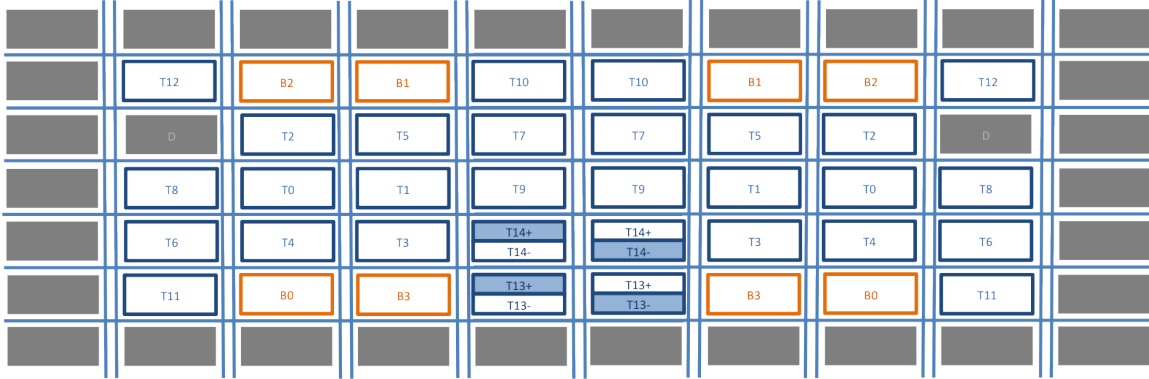


Figure 5.6: The PA layout with designated LNA, thermometer, binary, and dummy cells. One can see how the LNA cells are located adjacent to one another, facilitating layout and minimizing variation. In addition, these cells are the thermometer bits of the PA used for the two largest amplitudes, a mode of operation which already sees compression in the PA output, masking non-idealities from the addition of the LNA bits.

5.3 Switch Design for Device Reuse

PA Ground Switch

The PA Ground Switch was implemented as a single standard transistor, as may be seen in Figure 5.7. The LNA voltage and load impedances were designed to ensure that the AC and DC voltages on all nodes of the switches are tolerable.

Of the switches, the PA ground switch has some of the most rigorous constraints upon it. The parasitic capacitance of this switch limits the bandwidth of the LNA output. In addition, it must be robust enough to survive the DC and AC currents and voltages at its drain node. And, despite only being used in two PA unit cells, the PA ground switch was added to each unit cell, though shorted-out, in order to preserve matching to the greatest degree possible between cells.

In effect, the PA Ground switch needs to achieve all of this without greatly impacting the the performance of the PA or the PA unit cell size.

Resistance, capacitance, and current tolerance switch design requirements were optimized in layout, and a brief qualitative explanation is provided here.

Resistance

The on-resistance of the PA Ground Switch has a direct impact on the PA efficiency. The simplest approximation of the impact of the switch resistance is that the resistance will reduce output power by $(\frac{I}{16})^2 R$ for each cell. This overestimates the impact on efficiency because it fails to consider the impact that the switch resistance will have on the overall

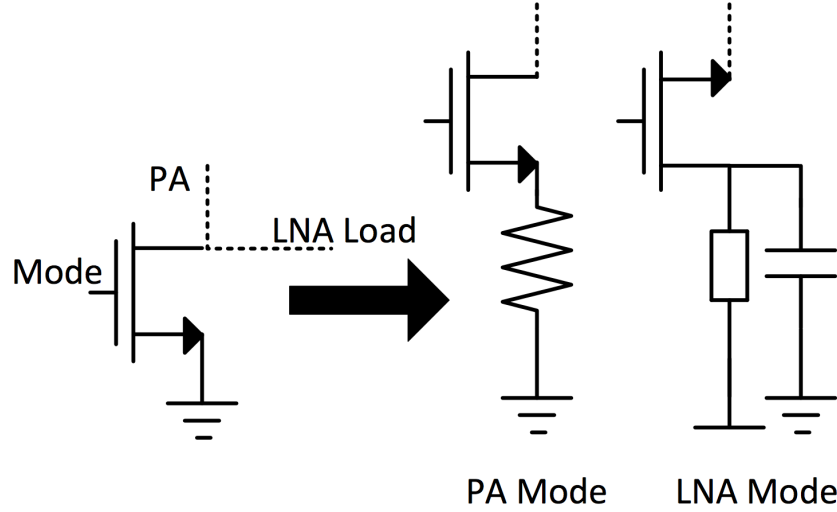


Figure 5.7: The PA Ground Switch and passive equivalents in transmit and receive mode respectively. The PA ground switch provides a low-impedance path to ground for the PA legs in transmit mode. The PA ground switch is open in receive mode, but does add parasitic capacitance to the LNA output node.

current. In fact, the current is somewhat lessened by the reduced V_{gs} and V_{ds} of the device. However, the above model is used for simplicity. Care was taken to choose resistance values that made the total drop in efficiency over all affected cells less than 5%.

Capacitance

To the first order, drain capacitance is minimized by maximizing the number of fingers on a device. This decrease is because the physical area of the drain is reduced, while maintaining the width of the device. However, at a certain point two things occur, the routing capacitance to reach the distant fingers increases and the device becomes impractically proportioned.

In addition to optimizing finger count, high metal layers were used for routing in order to reduce parasitic capacitance. And, vias to the source and drain were kept at oblique angles, respectively minimize parallel plate capacitance in the switch. All of these considerations resulted in a switch with less than the tolerated parasitic drain capacitance.

Current tolerance

Given the PA output power, the AC current tolerance of the PA Ground switch needs to be substantial. Given that there are approximately 16 evenly sized cells within a single PA, the current tolerance for a PA ground switch is $\frac{1}{16}$ of the overall current output of the PA. In this design, this results in a requirement of approximately 20mA of peak current.

Widened source and drain connections minimize parasitic resistance and increase the current tolerance of the PA Ground Switch. The source and drain regions were widened in conjunction with the finger selection for capacitance minimization. The additional fingers also keep the routing wire lengths short in the direction of current travel, increasing current tolerance.

LNA Load Switch

The LNA load switch is implemented as a single thick-oxide device, which allows it to tolerate the V_{ds} that it sees when the PA is transmitting: its source will be at the LNA V_{dd} while the drain on the PA side will be at ground. The design requirements of the LNA Load Switch first depend on the location one selects for the switch. At its most basic level, the LNA load switch needs to create an open circuit between the PA Ground switch and the LNA V_{dd} . This can be achieved by placing the LNA load switch at any one of the locations shown in Figure 5.8.

Each one of these locations comes with certain benefits and limitations. Several of these options would allow for the LNA load switch to be used as part of the LNA output impedance. However, the on-resistance of this device is simply not linear enough to allow for this to work. In order to preserve linearity, the nominal on-resistance of the LNA Load switch is kept to approximately 5% of the total load resistance.

Creating a switch with only a small fraction of the load resistance requires a large switch device. This switch device will have a large amount of parasitic capacitance. The LNA is bandwidth limited, which calls for the shunt-peaking output method described. A large amount of parasitic resistance on the source and drain of this switch will have an impact on the effectiveness of the shunt peaking equations. Figure 5.8 shows how equivalent circuit used for shunt peaking analysis will change with the addition of a low-on resistance switch. As the on-resistance of the switch is small, the switch can simply be modeled as a capacitance equal to the source and drain capacitance of the switch.

In all but case (c) shown in Figure 5.8, the capacitance will add to the capacitance which must be resonated out by the inductor, requiring a larger inductance, taking up area on the chip, decreasing bandwidth, and increasing the gain peaking. Even if one models the switch with some parasitic series resistance between the source and drain capacitances, there will only be a drain capacitance seen at the V_{dd} side of the inductor in option (c). Plus, instead of shorting out the inductance, as in the other options, this capacitance shorts out the resistance to create an AC short across the resistance, a benefit to the shunt-peaking method.

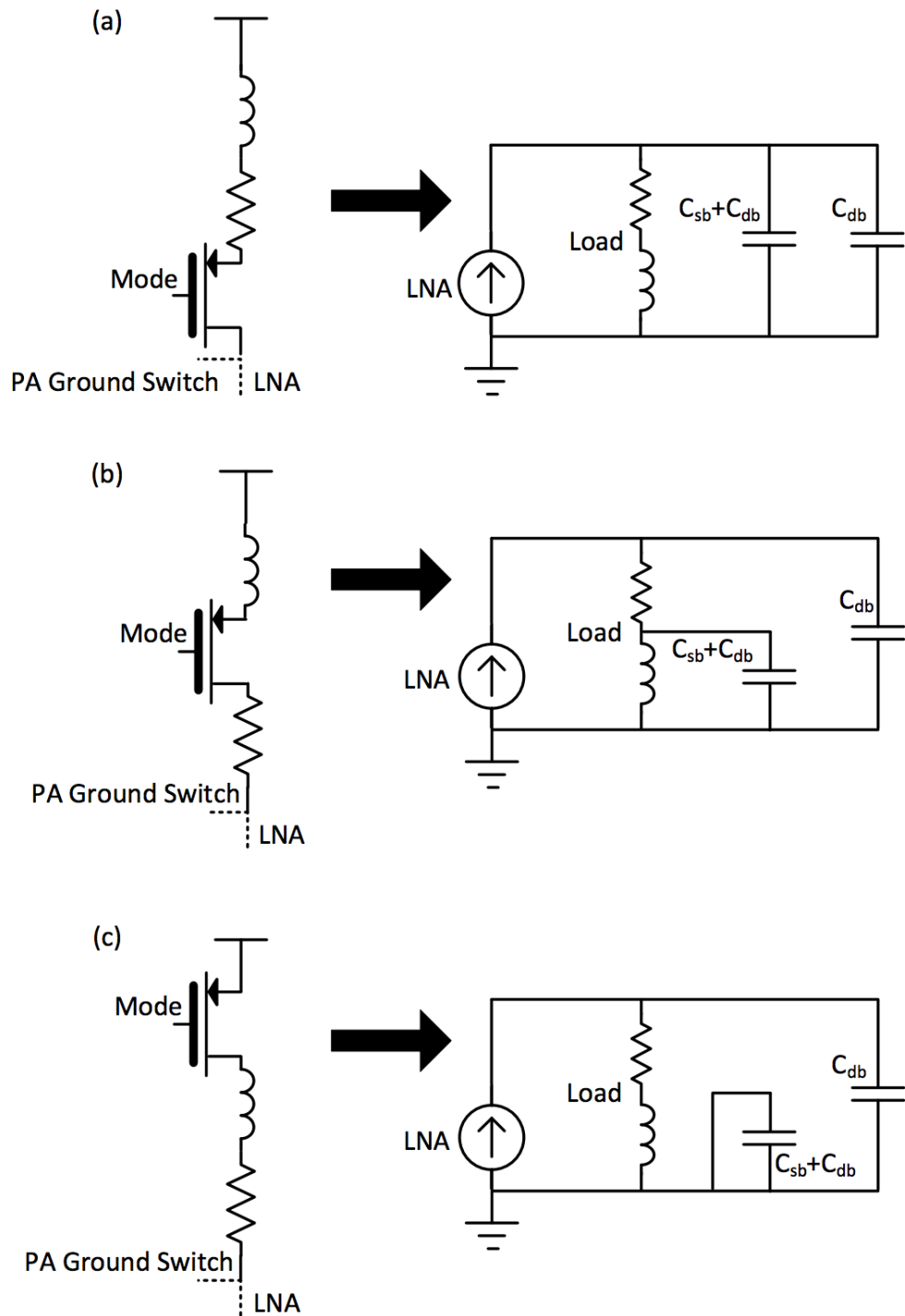


Figure 5.8: Different potential placements of the LNA load switch with respect to the load and the resulting effect on the shunt-peaking equivalent circuit. The equivalence assumes that the on-resistance of the load switch is low and that the switch can thus be modeled primarily as capacitance. This is valid as it is less than 5% of the output load.

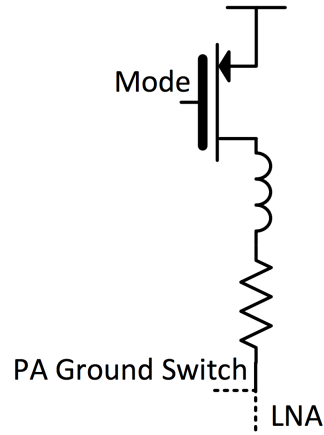


Figure 5.9: The LNA load switch. This switch connects the LNA output to power. It is a thick-oxide device in order to tolerate the V_{dd} of the LNA.

Thus, in order to maximize the LNA output bandwidth, the device is placed between V_{dd} and inductor and is used as a power switch where the drain voltage should change as little as possible when the LNA is receiving. A diagram of the LNA Load Switch may be seen in Figure 5.9.

Center Tap Switch

The Center Tap switch is implemented in two parts. The center tap for the PA, which connects to V_{dd} is implemented as a single thick-oxide device. The center tap for the LNA, which connects to ground is formed by legs of the PA on the side of the transformer opposite the LNA connections.

LNA Center Tap

There are fewer requirements on the LNA center tap, as there is less current, less than 7mA, of current flowing through these legs while the LNA is receiving. In addition, it is desirable to leave the PA legs as-is. Thus, no design changes were made for the LNA center tap.

PA Center Tap

The PA center tap's requirements, however, are more rigorous. The resistance of the PA center tap directly affects PA efficiency. With a desired output power greater than 23 dBm, the current through a single center tap can be over 250 mA. The target resistance was .5

Ω in order to keep the total efficiency over 40%. Such a low on-resistance in thick-oxide requires an unusually wide device, resulting in large parasitic capacitances and area usage.

In isolation, without the described LNA topology, the center tap switch could have unlimited parasitic capacitance without effecting the PA performance. However, due to the location of the center tap switch, the capacitance has a negative effect on the LNA input impedance. The capacitance at that node effectively shorts out the transformer between the PA center tap and the LNA center tap when the LNA is receiving.

The effect of this capacitance can be mitigated in several ways. Figure 5.10 shows three different configurations of inductors around the center tap and transformer which either isolate the capacitance from the RF path or resonant out the capacitance.

Parallel Inductor Resonance - Option (a) In the first option, an inductor is placed in parallel with the parasitic capacitance in order to resonate out the capacitance. The fundamental problem with this solution is that the bypass capacitance, required to allow for the drain of the center tap to be either V_{dd} or ground, ends up being prohibitively large.

Modified Parallel Inductor Resonance - Option (b) The Modified Parallel Inductor Resonance takes advantage of the differential nature of the voltages at the drain of each center tap in LNA mode and the common mode nature of the drain of each center tap in PA mode. To further explain, an AC ground is located at the node between the inductors, which is all that is required for resonance in LNA mode. In addition, this node will be self-biased to the common mode voltage at the drain of the PA Center Tap switch during each mode of operation, eliminating the need for a bypass cap.

This options requires that one carefully design the inductor Q to present an inductance in the series-to-parallel conversion that resonates with the capacitance. The amount of resistance also needs to be on the order of an Ohm in order to provide the Q necessary to support both the wide band operation of the LNA both in general and the potential process variation of the parasitic cap.

The small resistance in the inductor, though small, has a large impact on the noise of the LNA. This resistance injects noise at the input of the LNA, which then sees the entire gain of the LNA. Even the small resistance of a few Ohms, when transformed through the tuning network, can cause appreciable changes in the noise figure of the LNA.

Series Inductor Resonance/Choke Inductor - Option (c) The third and final option is to use a series inductor to resonant out the signal, which if done at a frequency well below the frequency of interest, makes a common mode choke by placing an inductor in series with the PA Center tap switch.

The full PA current will need to flow through this device, and the resistance will theoretically have an effect on PA efficiency. The inductance would need to be large enough to both cancel out the center tap cap and not reduce the effective transformer inductance by a parallel operation. Achieving a low-resistance and high-inductance inductor is difficult

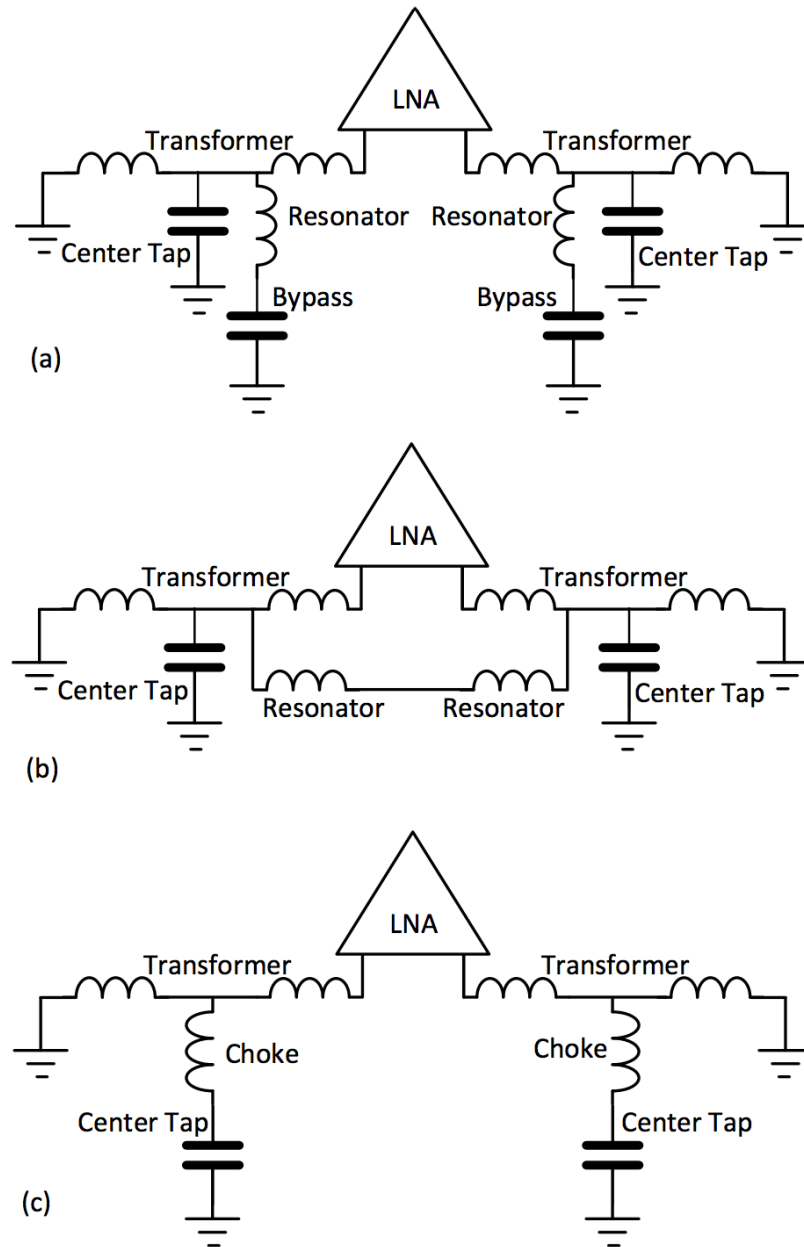


Figure 5.10: Center tap capacitance mitigation solutions. Options (a) and (b) show methods for resonating out the parasitic from the PA center tap switch. Option (c) proposes a common-mode choke in order to isolate the capacitance from the RF path.

in CMOS. Instead, one can get a ‘low’ resistance inductor with a high inductance in LNA mode by using both center tap inductors as a set of coupled inductors. Coupled inductors, follow the property:

$$v_1 = L_1 \frac{di_1}{dt} - M \frac{di_2}{dt} \quad (5.13)$$

where M is the mutual inductance $k\sqrt{L_1 L_2}$, $v_1, L_1, \frac{di_1}{dt}$ are the voltage, inductance, and derivative of the current on the side of interest, and $\frac{di_2}{dt}$ is the current on the opposite side.

Assuming that $\frac{di_1}{dt} = -\frac{di_2}{dt}$, as is the case in differential signals, the effective inductance of a single side in receive mode is

$$L_{1eff} = L_1 + M. \quad (5.14)$$

In transmit mode, where the currents are flowing in the same direction, the effective inductance becomes

$$L_{1eff} = L_1 - M. \quad (5.15)$$

Thus, this method allows for an increased inductance in receive mode, where the current i_1 and i_2 are differential. The reduced inductance in transmit mode simply returns the system somewhat closer to the design without the inductor in series with the center tap switch.

However, the system is not completely returned to an inductor less state, as M never equals L_1 due to the physical limitations of k , the coupling factor which determines M . This residual inductor has an additional interesting side-effect. The inductor makes the center tap in transmit mode look somewhat more like a current source, as opposed to a DC voltage source. The resulting AC open at the center tap node helps to provide proper termination of the second order harmonics in the system [6].

A final image of the center tap design with the coupled choke inductor may be seen in Figure 5.11.

Cascode Bias Switches

The Cascode Bias Switches are implemented as a collection of switches, pass-gates, and a resistive DAC. The different elements of this system may be seen in Figure 5.12.

PA Cascode Device Bias

For the purposes of the PA, the PA cascode devices, which act as the LNA input devices, could be left in an ‘on’ state at all times. These devices do not need to change gate bias, if operated solely in PA mode.

Similarly, some of the PA cascode devices, specifically those not used in the LNA, but in the leg of the PA which forms the LNA center tap, can be left in an ‘on’ state at all times.

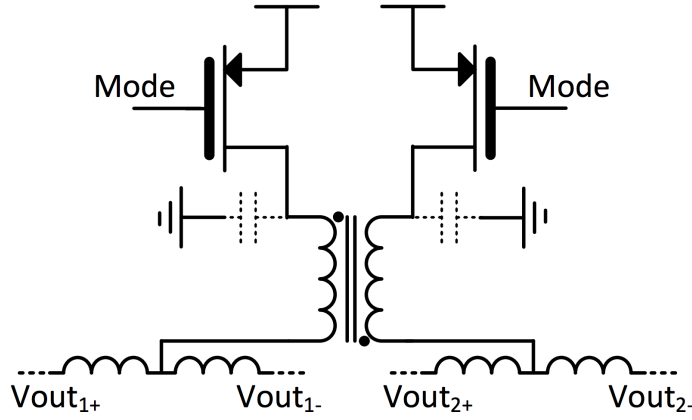


Figure 5.11: The complete center tap switch. The final center tap switch solution used supportive passive elements to compensate for the large capacitance of the switch. The coupled inductor at the output of the center tap switch increases inductance in receive mode and decreases in inductance in transmit mode. This allows for the capacitance to be well isolated in receive mode without increasing the inductor noise and helps keep resonance in transmit mode out of band.

In this implementation, the only time during which these devices are turned ‘off’ is when switching between receive and transmits mode, in order to avoid current shunting. This ‘on’/‘off’ functionality simply requires that the inverter driver of the cascode device provide a low impedance path to the source, as to not reduce the efficiency of the PA through gate-to-drain coupling.

However, other PA cascode devices need to be turned into other states during receive operation. The branch which does not form the LNA center tap is used to create 1 bit of input capacitance tuning, as described in 5.2. Again, this simply requires a low-impedance inverter (and the appropriate digital logic) to drive the cascode device.

LNA Input Bias Node

Finally, the LNA input device gates need to see a precision bias voltage, coupled to the source of the opposite polarity input devices, with a large impedance between the bias voltage and the gate node to allow for g_m boosting. This implementation is somewhat more difficult than the simple ‘on’ and ‘off’ switches.

Firstly, one must generate a precision voltage. In this implementation, the voltage is generated using a resistive DAC. The DAC output is isolated from the gate input by several pass-gates and some additional resistance.

In PA mode, it is somewhat important that this node not swing. While this cross-coupling should, due to the effective g_m boost of the coupling, actually help efficiency, it

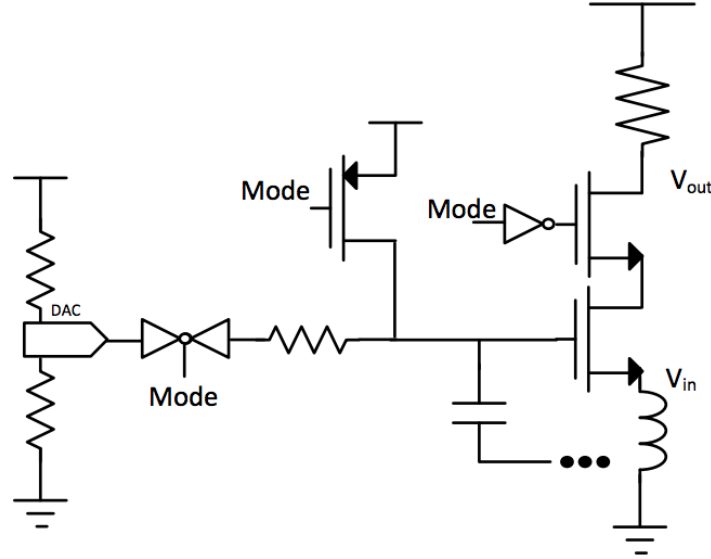


Figure 5.12: Complete bias circuitry for both the transmit and receive modes, including g_m cross-coupling capacitance. In transmit mode, the cascode device of the PA must be connected to V_{dd} , which is done through a PMOS switch. In receive mode, the cascode device in the PA becomes the input device to the LNA. This device then needs a precision gate bias, which is provided by the DAC. In order to achieve good g_m cross-coupling, there must be sufficient impedance between the DAC and the device gate. This is provided by a pass-gate and real resistance. The pass-gate also isolates the DAC from V_{dd} in transmit mode.

causes stability issues. A cross-coupled g_m stage, effectively the PA with the LNA cross-coupling implementation, is a well known, potentially unstable element: a negative resistance generator, often used in oscillators. Thus, the PMOS switch to V_{dd} on the LNA bias node should have a low on-resistance.

However, there is an additional design requirement, the PMOS switch must leak as minimally as possible when in the ‘off’ state. Any leakage current from this device will be shunted through the DAC, causing error in the output voltage of the DAC. Thus, one must find a balance between on-resistance of the device and leakage current. In this implementation, a high-threshold device enabled simultaneous satisfaction of both requirements.

Full PA/LNA Architecture with Device Reuse

The previous sections described the design of the PA, LNA, and mode switches. Figure 5.13 shows a schematic of the complete PA and LNA architecture. Some switches are represented as ideal switches, as opposed to their full transistor realization. However, this should

provide the reader contextualization for the design described.

5.4 Coexistence via Device Reuse PA/LNA Simulated Results

The described PA and LNA coexistence solution has been taped-out as of the writing of this document. This section presents partially extracted simulation results from that chip.

PA

As the PA is not the main focus of this work, we use simulations results merely to prove that the PA meets power and efficiency specifications. In other words, we want to confirm that the PA performance was not greatly reduced due to the modifications made to the PA to support the LNA. Partially extracted simulation results for output power and efficiency may be seen in Figure 5.14.

In these partially extracted simulation results, the performance meets specification with greater than 23dBm output power across the band and a peak efficiency greater than 40%. This indicates that the PA modifications work as designed and do not interfere with the PA performance more than expected.

LNA

The LNA designed by reusing PA devices is the main focus of the is work. As such, this section provides details of the partially extracted simulation results. We start by covering the matching of the LNA, which implemented 1-bit of capacitance tuning to increase the bandwidth. We will follow with noise figure and gain.

Input Impedance and Matching

As was described in 5.2, the input matching of the LNA needs to be about 20% lower than the antenna impedance while achieving a minimal power consumption. In Figure 5.15, one can see the input impedance over frequency. At the maximum point, the Z_{in} value is approximately 38Ω , on target for the 20% differential. One is also able to see how the input impedance Z_{in} increases more rapidly towards resonance when the varactor is ‘on.’ This was achieved with a power consumption of only 8.6 mW.

Given that the impedance is optimized for noise, the matching is not expected to be much below the standard -10 dB for S_{11} . Figure 5.16 shows the matching parameter, S_{11} , for this design. Due to the amount of parasitic capacitance from the PA which is found at the input node of the LNA, it was somewhat difficult to achieve broadband performance with this LNA. The 1-bit of tuning capacitance benefits the bandwidth in the lower range of the LNA by adding an additional 500 MHz of bandwidth to the lower end of the band.

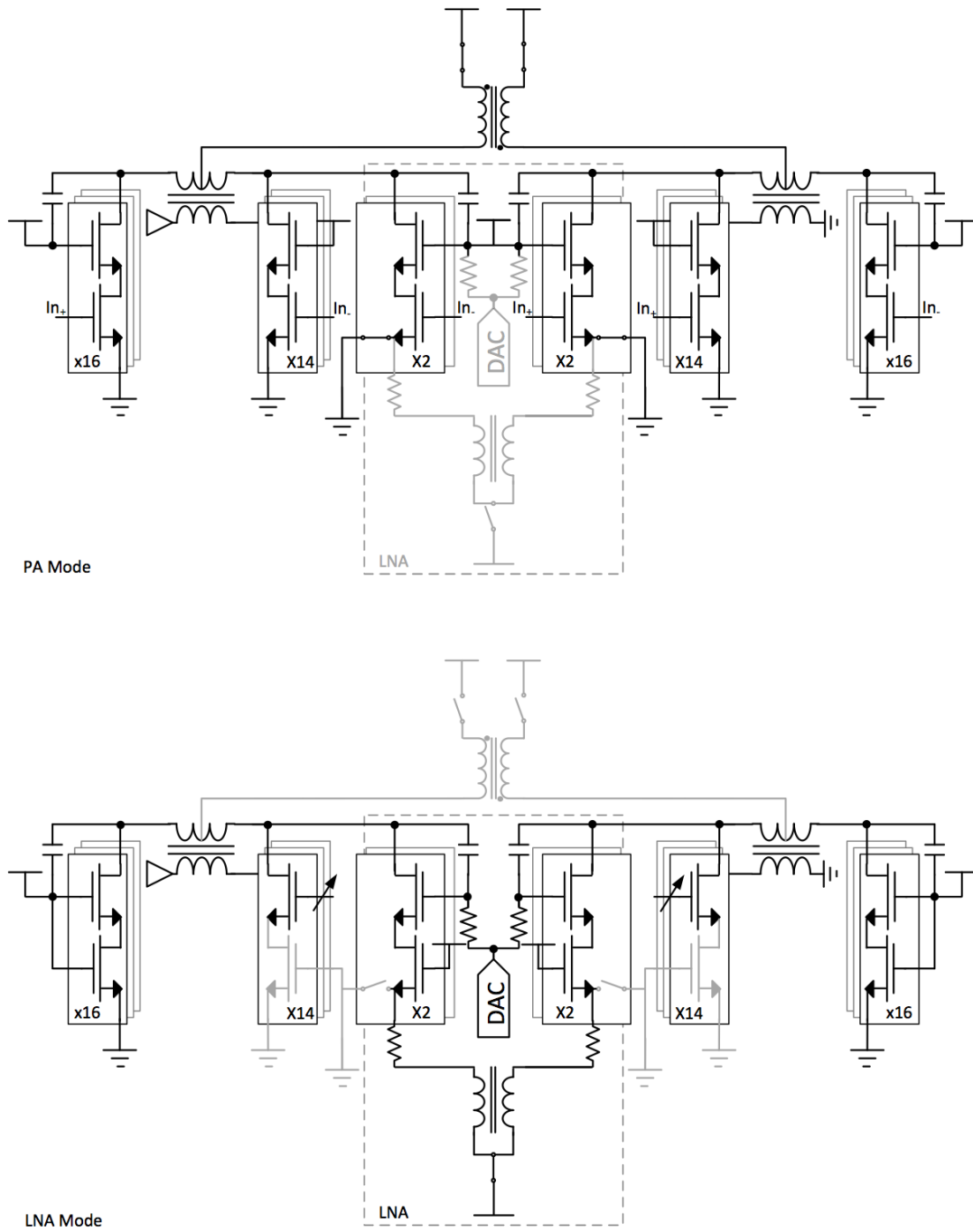


Figure 5.13: Full PA and LNA mode schematics. Though some switches are represented as ideal, this diagram represents the full architecture of the PA and LNA in this coexistence solution. In addition, binary cells are compressed and represented as one thermometer unit cell.

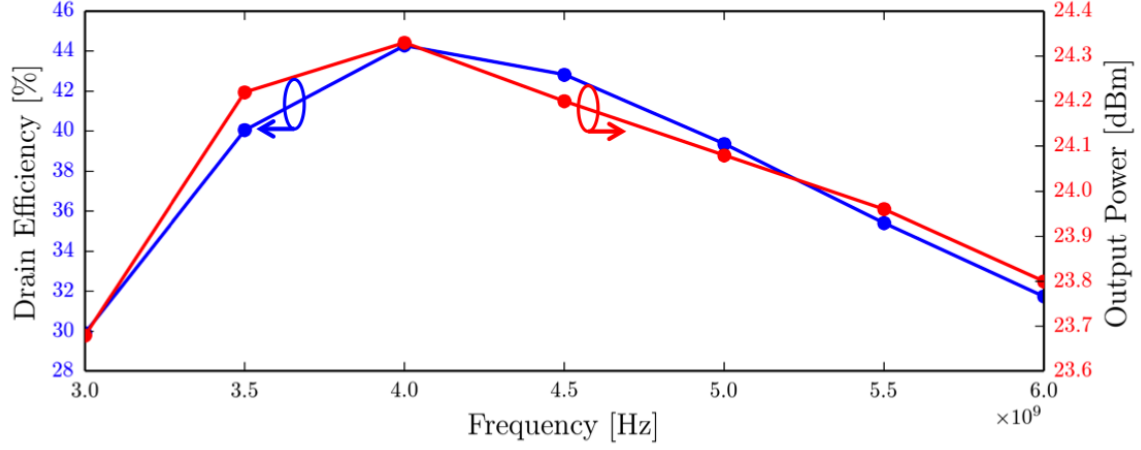


Figure 5.14: Partially extracted PA efficiency and output power simulation results across frequency. The output power of the PA is about 23 dBm across the band. The peak efficiency is about 40%.

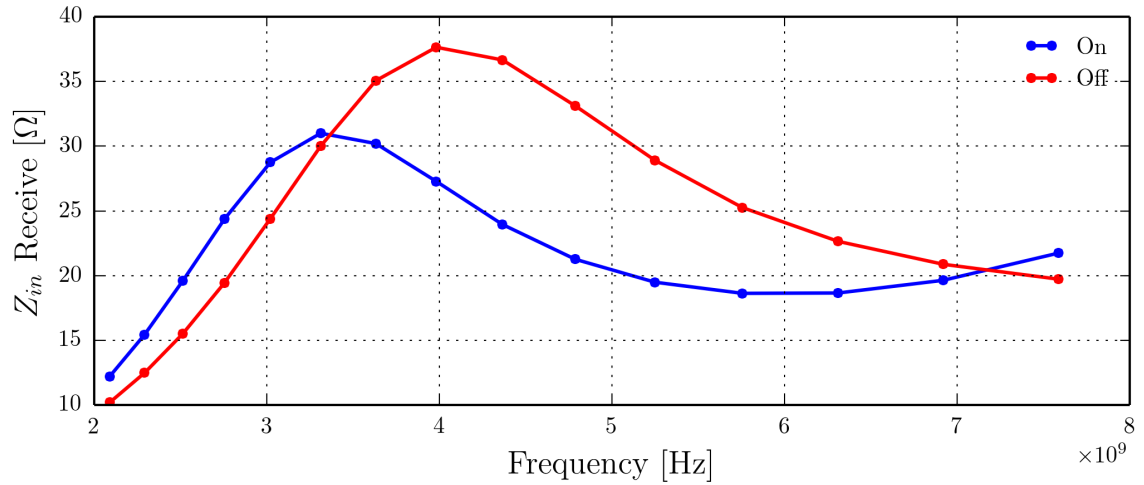


Figure 5.15: Z_{in} of the LNA with and without the additional bit of capacitive tuning.

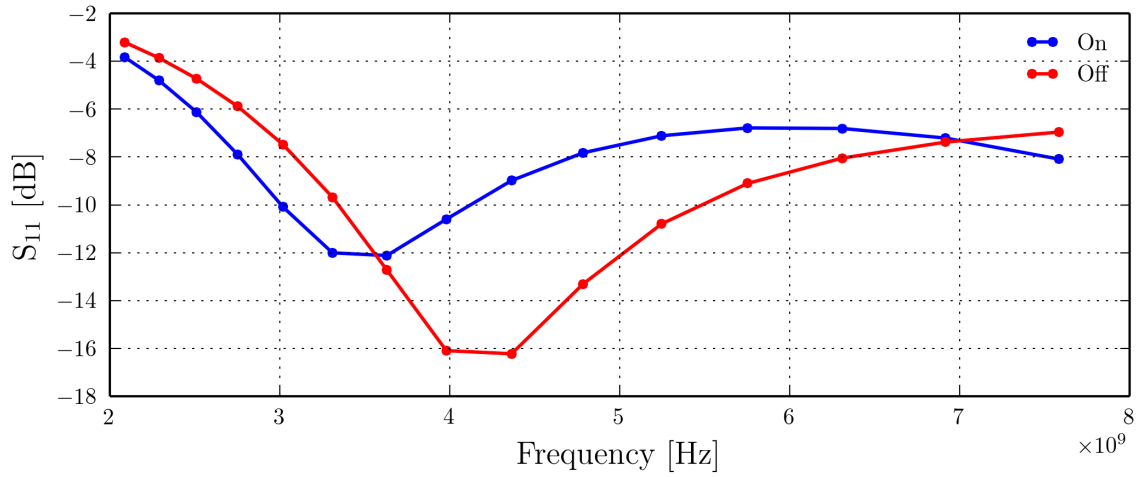


Figure 5.16: S_{11} of the LNA with and without the additional bit of capacitive tuning.

The resulting bandwidth for the LNA is 3 GHz to 5.5 GHz.

Gain and Noise Figure

In order to keep noise figure low, the gain of the LNA was kept above 20 dB. Figure 5.17 shows that the gain is stable around 22 dB throughout most of the matched band. As this is a low power LNA with a resistive load, a high gain negatively impacts linearity. However, even at 8.6 mW of power consumption and 22 dB of gain, a linearity of -4.3 dBm P_{1dB} and 6.5 dBm IIP_3 was achieved in schematic simulations.

Though gain is high, the overall poor input matching has a negative effect on noise figure. In addition, the topology of the LNA is highly sensitive to resistance seen at the input of the LNA. Figure 5.18 shows the noise figure performance of this LNA. The minimum noise figure crests at 4.0 dB. Again, the 1-bit of input tuning capacitance does add about 500 Mhz of bandwidth where the noise figure is less than 5 dBm.

The reader will note that the minimum and overall noise figure can be improved by increasing the power consumption. However, there is very little margin on the 10 mW power consumption specified, and noise figure will be sacrificed.

Comparison to State of the Art

Having discussed the metrics of LNA performance above, there is sufficient information with which to compare this LNA performance to similar LNAs in the literature. Table 5.1 shows current work in the field as compared to the semi-extracted results of this LNA.

Looking across the state-of-the-art in wide-band LNA performance in this frequency range, this design is superior in gain, linearity, and power consumption. This design, similarly

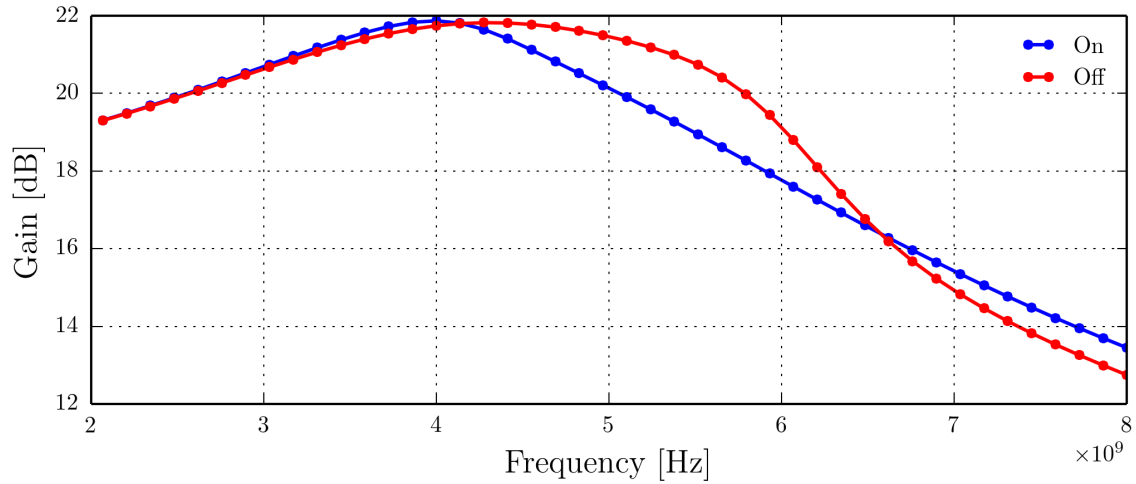


Figure 5.17: Gain of the LNA with and without the additional bit of capacitive tuning.

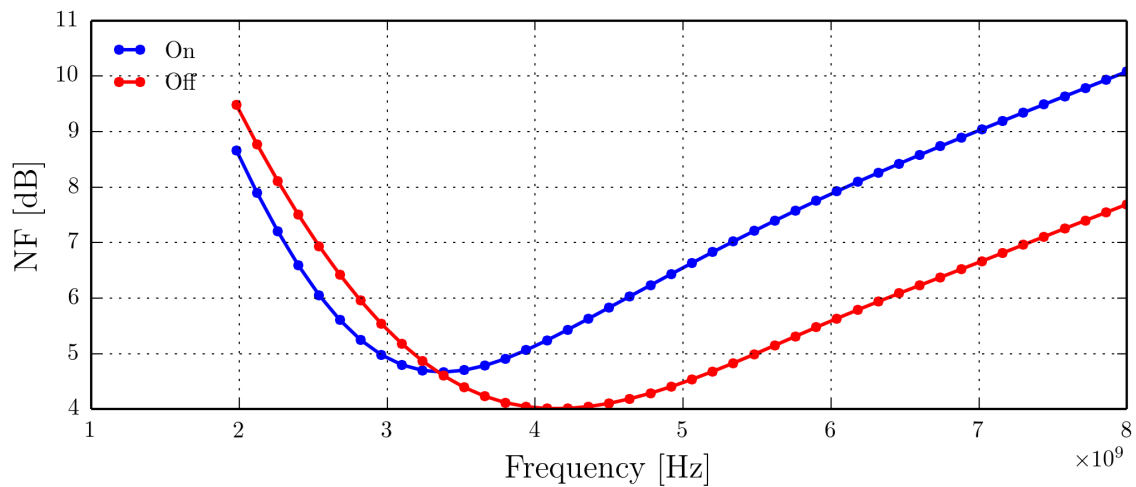


Figure 5.18: Noise Figure of the LNA with and without the additional bit of capacitive tuning.

	Freq (GHz)	NF min (dB)	Gain (dB)	IIP3 (dBm)	S11 (dB)	Power (mW)	Tech	Sw?	Xfmr?
This	3-5.5	4.0	22	6.5 ^a	<-10	8.6	65nm	Y	Y
[27]	1.4-3.8	>3	16	-4	-	6	45nm	Y	Y
[28]	DC-10	4	13	-1.5	>-5	NA	65nm	Y	N ^b
[29]	DC-9.5	3.8 ^c	12	4	<-10	18	65nm	N	N
[30]	1.2-6.6	4.8 ^c	14	1.8	<-10	13.2	.13um	N	Y
[31]	1-8	3.65 ^c	13.5-16.5	3	<-10	10.8	.18um	N	Y
[32]	DC-10	3.9 ^c	10.7	-3.5	<-8	13.7	65nm	N	N

Table 5.1: Wide band LNAs in the low GHz found in literature as compared to the LNA herein. The works appearing above the horizontal line are complete transceivers, while works below the line are LNAs only.

^aSchematic Only

^bWiMedia

^cComputed using 1 dB of attenuation and the Friis Noise Equation.

to the Tx/Rx switch is bandwidth limited. In addition, the noise figure is somewhat higher than desired, though this is a trade off with power consumption.

The reader may ask why this solution was not directly compared to the Tx/Rx switch solution found in the first half of this work. Primarily, the two designs operate in two slightly different frequency bands and at two different output power levels. Thus, an outright comparison is unfair in both cases. In addition, the Tx/Rx simulations were done using only a schematic version of the LNTA and an ideal transformer. This given the Tx/Rx switch simulations an obvious unfair advantage over the LNA described here. Instead, the adjusted noise figure of the LNA-only prior art is meant to orient the reader to how a Tx/Rx switch solution would compare to the LNA described.

5.5 Conclusion

In conclusion, simulations show that it is possible to produce a functional and competitive LNA and PA which uses device reuse as the TDD coexistence solution. The amount of capacitance from the PA does limit the bandwidth of the device. In addition, there is a tradeoff between noise figure and power consumption. However, this device performs well as compared to the state of the art in gain, linearity, and power consumption. It is also a scalable solution for inverse class D power amplifiers, which might save on future design time. Final chip testing and fabrication will be able to determine the true viability of this device as a TDD solution.

Chapter 6

Conclusion

6.1 Summary of Work

In this work, we presented the problems faced in TDD coexistence. Through analysis of the problem from a generalized and implementation-specific perspective, we developed two different coexistence solutions: a power tolerant Tx/Rx switch and a PA-embedded LNA. From layout-extracted simulations, it was shown that both solutions provide the basic requirements of a TDD system: power tolerance and high-impedance isolation nodes. However, the cost in design time and in performance differs between the two solutions.

The Tx/Rx switch achieves lower insertion loss than the state-of-the-art and comparable isolation, though the isolation bandwidth is lower than other bulk CMOS designs. The trade-off between insertion loss and bandwidth is a function of device size, which begins to illuminate the inherent trade-offs and limitations of bulk CMOS Tx/Rx switches.

The PA-embedded LNA achieves comparable performance, with better gain, linearity, and power consumption than other solutions, but again suffers from a small bandwidth and comparable noise figure. The bandwidth and noise limitations are largely due to the resistance sensitive routing and capacitance at the LNA input node. The switches which support the change between PA and LNA functionality are not the main contributors to the performance limitations. In effect, the PA-embedded LNA has potential for further iterations and development.

6.2 Future Work

Future work includes measurement of the results from both chips, which have been taped-out. Upon analysis of the measured results, one will be able to analyze the true efficacy of each solution and determine if the design costs of the application-specific solution outweigh the performance gains provided.

If the application-specific solution is found to be viable, several additional steps should be taken and avenues of applications should be researched. First, the described solution should

be implemented within the full context of a TDD transceiver, eliminating non-production peripherals, such as the resistive DAC. Second, work should be done to understand the costs and benefits of taking the opposite design paradigm described here and choosing to form the PA unit cells around a strategically design LN(T)A. This approach would help to illustrate the full performance capabilities of the device reuse concept and could help pave the way to an industrial implementation.

Bibliography

- [1] “Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2013-2018,” Cisco Systems Inc., www.cisco.com, White Paper, 2014.
- [2] “Evolution to LTE Report,” Global mobile suppliers association, www.gsacom.com, Market/Technology Update, 2014.
- [3] X. Chen and C. Xie, “TDD Spectrum White Paper,” Global TD-LTE Initiative, www.lte-tdd.org, White Paper, 2013.
- [4] R. Womersley, “Spectrum for WiMAX in Europe,” InterConnect Communications, <http://www.icc-uk.com/download/papers/Spectrum-for-WiMAX-in-Europe.pdf>, Tech. Rep., 2006.
- [5] D. Chowdhury, “Efficient Transmitters for Wireless Communications in Nanoscale CMOS Technology,” PhD thesis, University of California at Berkeley, <http://www.eecs.berkeley.edu/Pubs/TechRpts/2010/EECS-2010-168.html>, 2010.
- [6] L. Ye, “Design and Analysis of Digitally Modulated Transmitters for Efficiency Enhancement,” PhD thesis, University of California at Berkeley, 2013.
- [7] D. Chowdhury, L. Ye, E. Alon, and A. Niknejad, “An Efficient Mixed-Signal 2.4-GHz Polar Power Amplifier in 65-nm CMOS Technology,” *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 8, pp. 1796–1809, 2011, ISSN: 0018-9200. DOI: 10.1109/JSSC.2011.2155790.
- [8] D. Chowdhury, S. Thyagarajan, L. Ye, E. Alon, and A. Niknejad, “A Fully-Integrated Efficient CMOS Inverse Class-D Power Amplifier for Digital Polar Transmitters,” *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 5, pp. 1113–1122, 2012, ISSN: 0018-9200. DOI: 10.1109/JSSC.2012.2185555.
- [9] L. Ye, J. Chen, L. Kong, P. Cathelin, E. Alon, and A. Niknejad, “A digitally modulated 2.4GHz WLAN transmitter with integrated phase path and dynamic load modulation in 65nm CMOS,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 330–331. DOI: 10.1109/ISSCC.2013.6487756.
- [10] “GaAs SPDT Switch DC - 3.0 GHz,” MA-COM Technology Solutions Inc., MASW2000 Datasheet.

- [11] “SPDT Switch for Single-band and Dual-band, 802.11a/b/g Systems,” TriQuint Semiconductor WLAN Products, TQS5200 Datasheet, 2003.
- [12] “PHEMT GaAs IC High-Linearity 3 V Control SPDT 0.1 – 2.5 GHz Switch Chip,” Skyworks Solutions, Inc., AS193-000 Datasheet, 2008.
- [13] H. Xu and K. O, “A 31.3-dBm Bulk CMOS T/R Switch Using Stacked Transistors With Sub-Design-Rule Channel Length in Floated p-Wells,” *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 11, pp. 2528–2534, 2007, ISSN: 0018-9200. DOI: 10.1109/JSSC.2007.907201.
- [14] T. Zhang, V. Subramanian, and G. Boeck, “Comparison of regular and floating bulk transistors in ultra-wideband CMOS T/R switches,” in *Microwave Radar and Wireless Communications (MIKON), 2012 19th International Conference on*, vol. 1, 2012, pp. 293–296. DOI: 10.1109/MIKON.2012.6233540.
- [15] W. Lerdsitsomboon and K. Kenneth, “Technique for Integration of a Wireless Switch in a 2.4 GHz Single Chip Radio,” *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 2, pp. 368–377, 2011, ISSN: 0018-9200. DOI: 10.1109/JSSC.2010.2090089.
- [16] A. Madan, M. McPartlin, Z.-F. Zhou, C.-H. Huang, C. Masse, and J. Cressler, “Fully Integrated Switch-LNA Front-End IC Design in CMOS: A Systematic Approach for WLAN,” *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 11, pp. 2613–2622, 2011, ISSN: 0018-9200. DOI: 10.1109/JSSC.2011.2166216.
- [17] Q. Li and Y.-P. Zhang, “CMOS T/R Switch Design: Towards Ultra-Wideband and Higher Frequency,” *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 3, pp. 563–570, 2007, ISSN: 0018-9200. DOI: 10.1109/JSSC.2006.891442.
- [18] Y. Wang, H. Wang, C. Hull, and S. Ravid, “A transformer-based broadband I/O matching-balun-T/R switch front-end combo scheme in standard CMOS,” in *Custom Integrated Circuits Conference (CICC), 2011 IEEE*, 2011, pp. 1–4. DOI: 10.1109/CICC.2011.6055284.
- [19] Y. Han, K. Carter, L. Larson, and A. Behzad, “A low insertion loss, high linearity, T/R switch in 65 nm bulk CMOS for WLAN 802.11g applications,” in *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, 2008, pp. 681–684. DOI: 10.1109/RFIC.2008.4561529.
- [20] E. Adabi and A. Niknejad, “A mm-wave transformer based transmit/receive switch in 90nm cmos technology,” in *Microwave Conference, 2009. EuMC 2009. European*, 2009, pp. 389–392.
- [21] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2004, ISBN: 9780521835398. [Online]. Available: <http://books.google.com/books?id=io1hL480qBsC>.
- [22] A. M. Niknejad, *Electromagnetics for High-Speed Analog and Digital Communication Circuits*. Cambridge University Press, 2007, ISBN: 9781139462242. [Online]. Available: <http://books.google.com/books?id=o80zzb4AUNYC>.

- [23] B. Razavi, *RF Microelectronics*, ser. Prentice Hall International Series in the Physical and Chemical Engineering Sciences. Pearson Education, 2011, ISBN: 9780132901055. [Online]. Available: <http://books.google.com/books?id=zTnD1RgHbbkC>.
- [24] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. Wiley, 2001, ISBN: 9780471321682. [Online]. Available: <http://books.google.com/books?id=-VmVQgAACAAJ>.
- [25] D. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2004. Digest of Papers. 2004 IEEE*, 2004, pp. 97–100. DOI: 10.1109/RFIC.2004.1320538.
- [26] X. Xiao, "Low-Power Spectrum Sensing for Cognitive Radio Applications," Master's thesis, University of California at Berkeley, <http://www.eecs.berkeley.edu/Pubs/TechRpts/2012/EECS-2012-146.pdf>, 2012.
- [27] S. Goswami, H. Kim, and J. Dawson, "A frequency-agile RF frontend for multi-band TDD radios in 45nm SOI CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE*, 2013, pp. 331–334. DOI: 10.1109/RFIC.2013.6569596.
- [28] D. Leenaerts, R. van de Beek, J. Bergervoet, H. Kundur, G. Van Der Weide, A. Kapoor, T. Y. Pu, Y. Fang, Y. J. Wang, B. Mukkada, H. S. Lim, M. Kiran, C. S. Lim, S. Badiu, and A. Chang, "A 65nm CMOS inductorless triple-band-group WiMedia UWB PHY," in *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, 2009, 410–411, 411a. DOI: 10.1109/ISSCC.2009.4977482.
- [29] J. Zhu, H. Krishnaswamy, and P. Kinget, "A DC-9.5GHz noise-canceling distributed LNA in 65nm CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE*, 2013, pp. 177–180. DOI: 10.1109/RFIC.2013.6569554.
- [30] H. F. Leung and H. Luong, "A 1.2V - 6.6GHz LNA using transformer feedback for wideband input matching and noise cancellation in 0.13 μ m CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE*, 2012, pp. 17–20. DOI: 10.1109/RFIC.2012.6242222.
- [31] R.-F. Ye, T.-S. Horng, and J.-M. Wu, "Wideband common-gate low-noise amplifier with dual-feedback for simultaneous input and noise matching," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE*, 2011, pp. 1–4. DOI: 10.1109/RFIC.2011.5940667.
- [32] K.-H. Chen and S.-I. Liu, "Inductorless Wideband CMOS Low-Noise Amplifiers Using Noise-Canceling Technique," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, no. 2, pp. 305–314, 2012, ISSN: 1549-8328. DOI: 10.1109/TCSI.2011.2162461.