Exploration of surface states in a monolayer MoS2 transistor by pulsed gating

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Exploration of surface states in a monolayer MoS_2 transistor by pulsed gating

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Research Project

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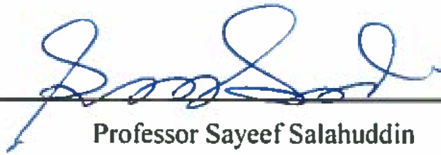

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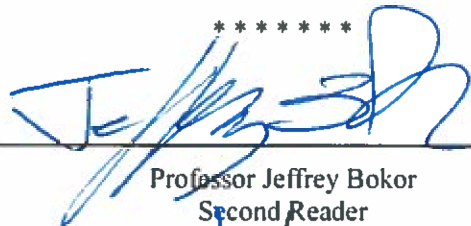

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Abstract

Two-dimensional (2D) materials have interested researchers all over the world for years due to their unique properties. Their ultra-thin thicknesses, lack of dangling bonds, and excellent thermal stabilities make them promising material candidates for use in next generation nanoelectronic devices. Graphene was the first 2D material discovered and has extremely high carrier mobility (>10^5 cm^2/V-sec). However, it lacks a finite band gap, restricting its potential use in field-effect transistors (FETs) to only the channel. Alternatively, MoS_2 is a compound 2D material with a finite band gap and low dielectric constant. As a result, it has recently been generating great interest in both academia and industry for its potential use in switchable devices.

In this work, we have explored the interface states that form between the channel of a monolayer MoS_2 transistor and a high-k gate dielectric. These interface states result in a large hysteresis in the transfer characteristic (i.e. drain current versus gate voltage) of the transistor. By applying carefully designed pulses to the gate of the transistor, we show that it is possible to both understand the nature of the interface states and minimize the hysteresis. This allows for reliable extraction of material parameters such as mobility from the transfer characteristics.

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Chapter 1. Introduction

1.1 Transition Metal Dichalcogenides

Transition metal dichalcogenides (TMDs) have recently garnered much attention for their potential to enable development of new and highly efficient two-dimensional (2D) electrical and optical devices [1-11]. Unlike graphene, TMDs have finite band gaps in the 2H phase (i.e. hexagonal symmetry, two layers per repeat unit, and trigonal prismatic coordination) [1, 3]. This is critical for transistor applications, and, indeed, excellent switching behavior with high ON/OFF ratio has been demonstrated for a number of different TMDs. Schematics of the 2H TMD crystal structure are shown below in Figure 1 [2]:

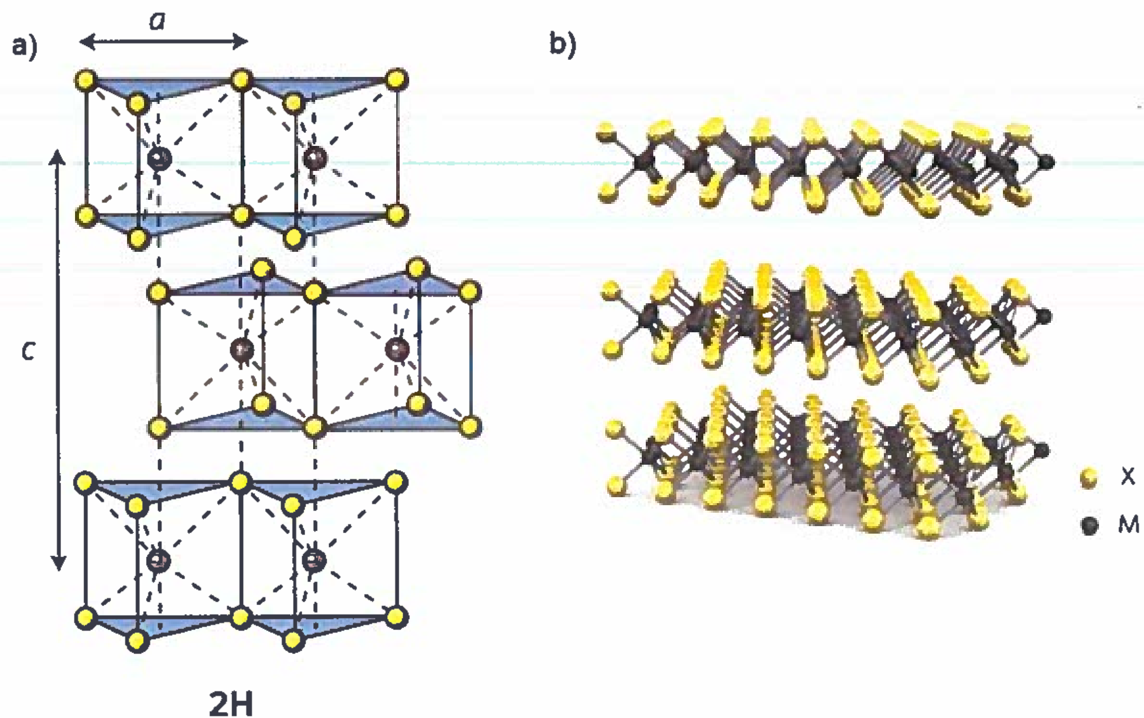

Figure 1. a) Schematic of the 2H TMD compound structure. b) 3-dimensional schematic of TMD, with the chalcogen atoms (X) in yellow and the metal atoms (M) in grey.

1.2 MoS_2 Transistor

Molybdenum disulfide (MoS_2) is the most widely used compound in the TMD family due to its stable chemical properties and high exfoliation yield. A transistor structure (Figure 2) is typically used to probe material properties such as dielectric permittivity and mobility.

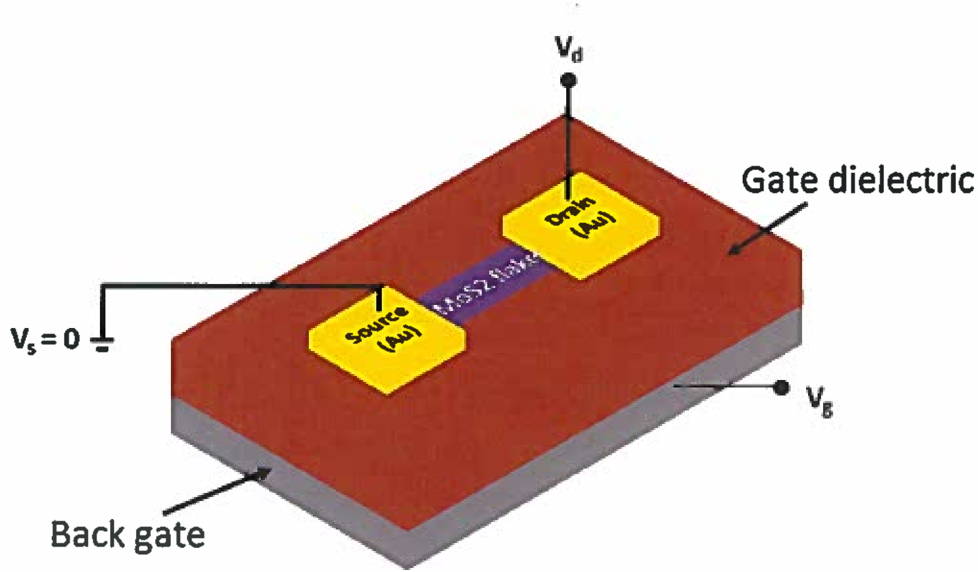

Figure 2. Schematic of a back gate MoS_2 transistor.

In a traditional transistor structure, the relationship between channel current I_d and gate voltage V_g can be modeled as

$$I_d = \frac{W}{L} C_{ox} \mu_{FE} (V_g - V_t - \frac{m}{2} V_d) V_d \quad (1)$$

where W and L are the channel width and length respectively; C_{ox} is the gate oxide capacitance per unit area; μ_{FE} is the carrier mobility; V_t is the threshold voltage; V_d is the drain bias voltage; and m is the "bulk-charge factor" corresponding to the body effect. Note that additional complicating factors such as contact resistance have been neglected for simplicity. For small V_d, $\frac{m}{2} V_d$ is negligible, and the relationship between I_d and V_d becomes approximately linear:

$$I_d = \frac{W}{L} C_{ox} \mu_{FE} (V_g - V_t) V_d \quad (2)$$

This shows that the field-effect mobility value can be extracted directly from measurement data by computing the slope of the I_d-V_g curve in the linear region:

$$\mu_{FE} = [I_d / (V_g - V_t)] / (\frac{W}{L} C_{ox} V_d) \quad (3)$$

1.3 Hysteresis Induced by Adsorbates

When these transistor structures are characterized under typical ambient conditions,

molecules such as oxygen, water vapor, etc. can adsorb at the interface between the channel and the gate oxide. This typically results in the formation of trapping centers at the interface [12-17]. The trapping mechanism can be understood from the schematics shown in Figure 3. The thermal average occupancies of these interface states are described by the Fermi-Dirac distribution:

$$f(E)=\frac{1}{1+e^{(E-E_f)/kT}} \tag{4}$$

Consequently, interface states with energies above the Fermi level are less likely to trap electrons while states with energies below the Fermi level are mostly full of trapped electrons. When a negative voltage is applied to the gate, the energy bands in the channel bend upwards near the oxide-channel interface as depicted in Figure 3a. This results in previously occupied states to rise in energy above the Fermi level, resulting in detrapping of electrons and increased channel current. On the other hand, when a positive gate bias is applied (Figure 3b), states previously unoccupied will decrease in energy below the Fermi level, resulting in trapping of electrons and reduced channel current.

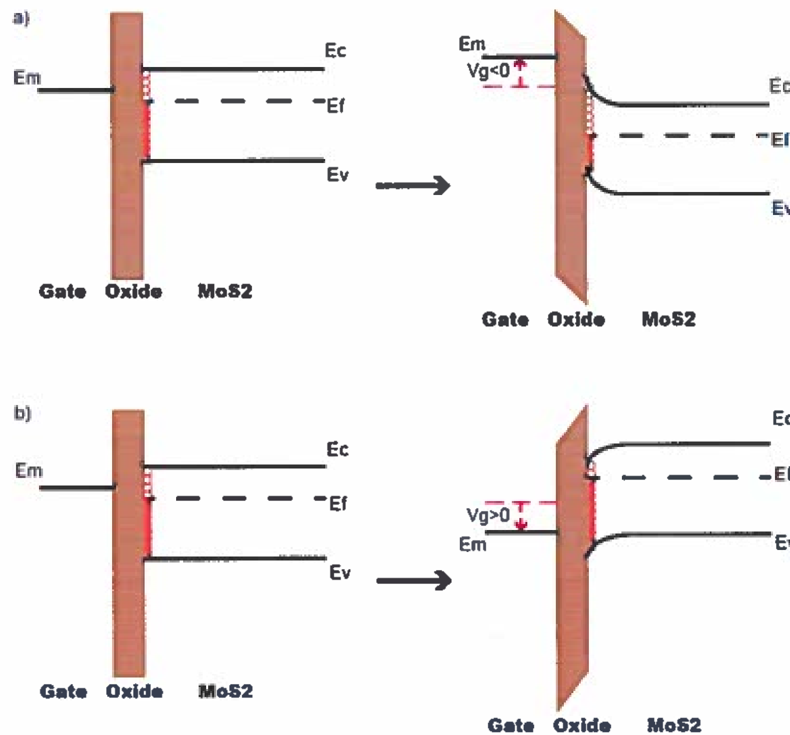

Figure 3. Schematics of interface trapping states changing occupancy when a gate bias is applied in the a) negative direction and in the b) positive direction.

As a result, nearly all experiments consisting of a DC sweep of the gate voltage show large hysteresis in the drain current.

The trap states and resultant hysteresis are highly undesirable. For example, the traps can continuously change the threshold voltage as a function of gate bias, and they can also significantly reduce ON current. Furthermore, the two branches of the hysteresis loop are typically different and usually depend on the initial condition, sweep rate, etc. Therefore, critical parameters such as mobility—which is extracted from the slope of the transfer characteristic (I_d-V_g)—can no longer be reliably estimated.

Later in Chapter 4.2, we will show that the hysteresis depends on different parameters that can be exploited to quantify the nature and density of the trap states. Such information can provide important insight for engineering the oxide-channel interface to optimize device performance. We will then show that by applying carefully designed pulses to the transistor gate, the effect of the trap states can be completely removed. This eliminates the hysteresis and reveals the intrinsic nature of the material itself.

Chapter 2. MoS_2 Transistor Fabrication

2.1 MoS_2 Film Exfoliation and Thickness Identification

Nanoscale thin films of MoS_2 were required to fabricate the transistors. While different methods exist for obtaining those films, mechanical exfoliation with scotch tape is the most popular method since it is easy to perform and produces high quality films. After exfoliation, atomic force microscopy (AFM) can be used to identify flakes that are of appropriate thicknesses. Unfortunately, however, this approach is time-consuming, especially when dealing with the numerous flakes produced by exfoliation. As an alternative approach, optical images can be used to rapidly and non-destructively identify flakes of appropriate thicknesses by using substrates with appropriate color contrasts. For example, MoS_2 monolayer flakes (~0.65 nm in thickness) exhibit a ~30% contrast (Figure 4b, [18]) when exfoliated onto light brown SiO_2 (270 nm) (Figure 4a, [18]).

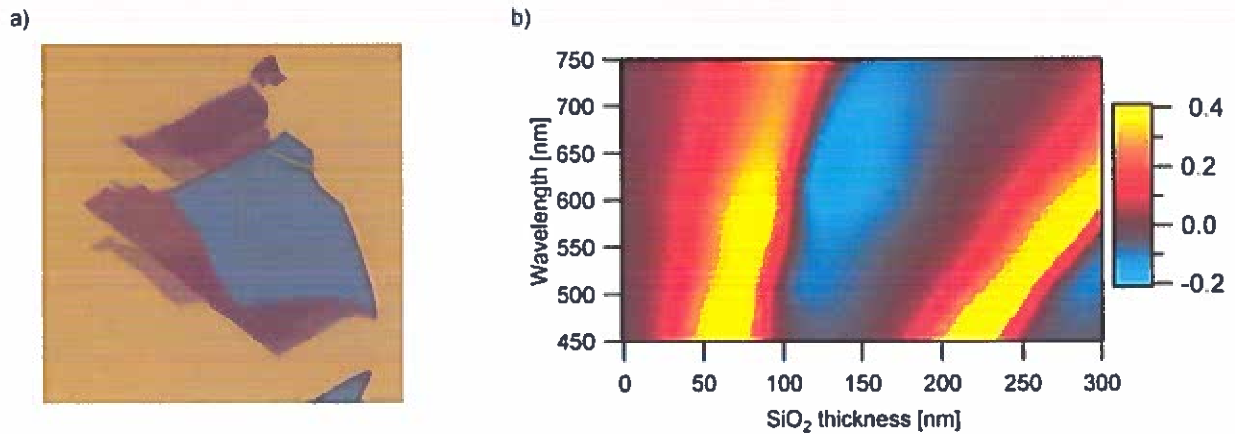

Figure 4. a) Microscope image of an MoS_2 flake. b) Plot of color contrast calculated as a function of incident light wavelength and SiO_2 layer thickness.

2.2 Transistor Fabrication Processes

The MoS_2 back gate transistor used here was fabricated using the following process flow (Figure 5):

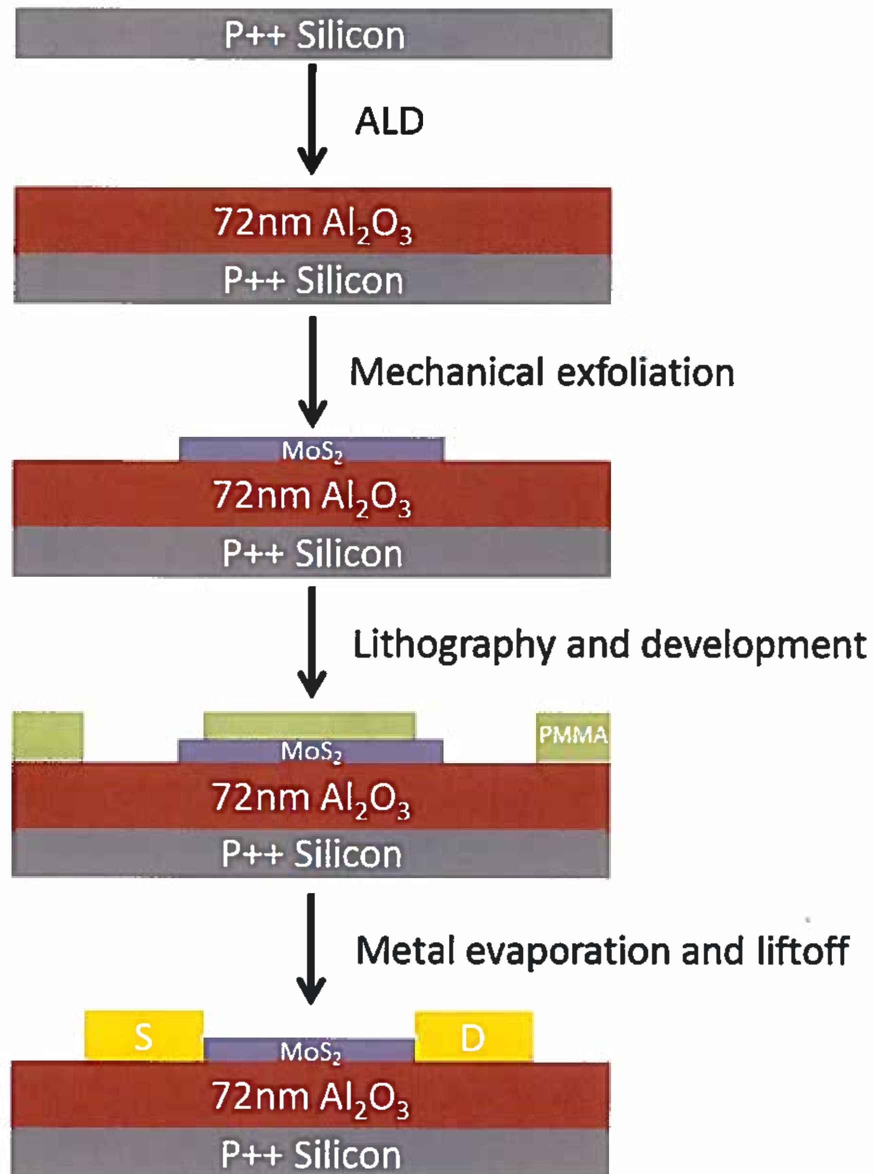

Figure 5. Transistor fabrication process flow.

First, 72 nm of aluminum dioxide (Al_2O_3) were deposited as the gate dielectric onto a heavily doped p-type Si substrate via atomic layer deposition (ALD). The thickness was chosen to ensure sufficient color contrast with MoS_2 in light brown color (Figure 6a) [19]. Next, a monolayer MoS_2 flake was exfoliated onto the Al_2O_3 from a bulk MoS_2 crystal (SPI Supplies). The electrodes were patterned by e-beam lithography. An Au (60 nm)/Ti (10 nm) bi-layer was chosen as the electrode metal (Figure 6a). AFM was used to confirm the flake's thickness (Figures 6b and 6c).

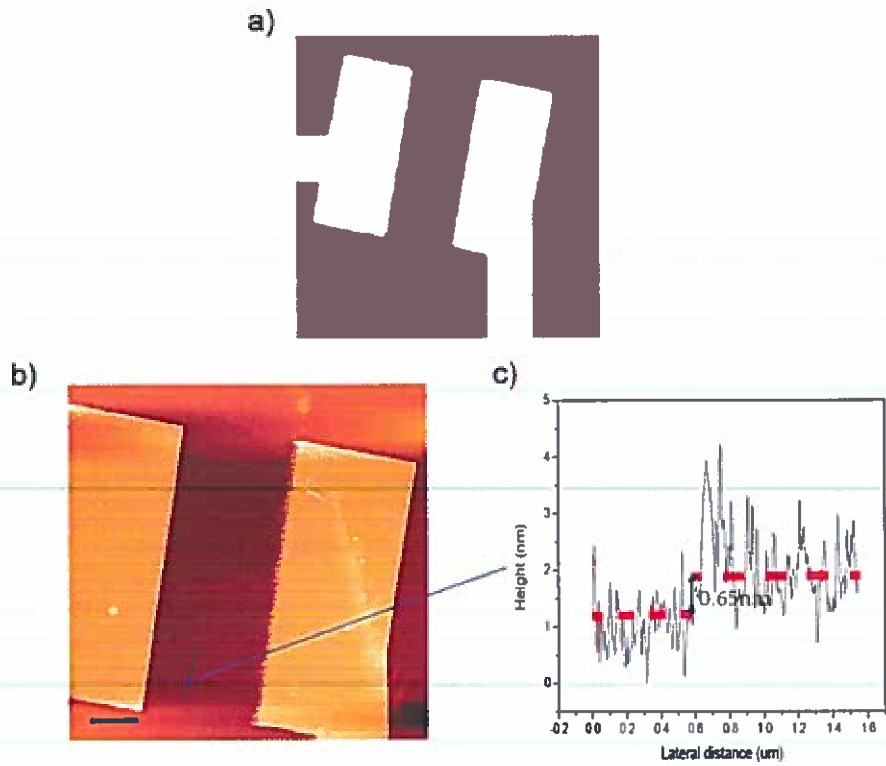

Figure 6. a) Optical image. b) AFM image of fabricated device. Scale bars are both 2 um.
c) Corresponding flake thickness measurement.

Chapter 3. Measurement Setup for Hysteresis Analysis

3.1 Pulsed Measurement

Pulsed measurement was introduced to analyze the transistor's *I-V* characteristics. Instead of applying DC voltages to the gate, a sequence of voltage pulses with equal durations but different amplitudes was applied. The delay between pulses provided a relaxation period during which trapping/detrapping states could recombine. By varying parameters such as pulse width (t_{on}) and pulse delay (t_{off}), the hysteresis loop induced by adsorbates was minimized, and the ON-current was optimized. A Keithley 2612B SourceMeter controlled by a LabVIEW program was used to generate a series of V_g and V_d bias voltages while simultaneously measuring I_d.

Two different pulse series were used for the measurement. In the "normal" pulse series (Figure 7a), the pulse amplitude gradually decreases or increases in magnitude, but the polarity only switches after half the waveform period [20]. In contrast, in the "zigzag" pulse series (Figure 7b), each voltage pulse is followed by a pulse of equal amplitude and duration but opposite polarity to offset trapping/detrapping effects [21, 22]. The pulses of opposite polarity help to equilibrate the interface states. For example, electrons detrapped by a negative V_g pulse are retrapped by the subsequent pulse of opposite polarity (a positive V_g pulse). Thus, the two effects cancel each other, and the hysteresis nearly disappears. This will be discussed again with more details and data later in Chapter 4.2.

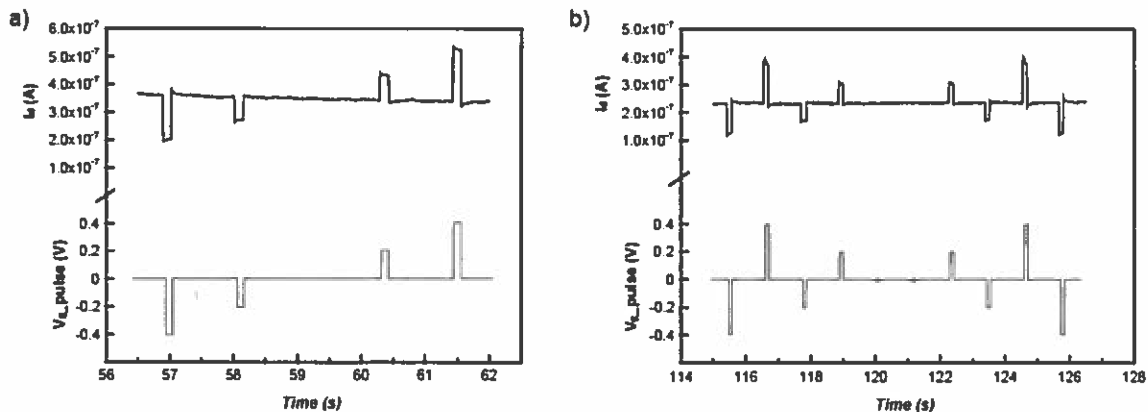

Figure 7. a) Part of the normal pulse series and the corresponding I_d-*Time* sweeping curves. b) The zigzag pulse series setup and the corresponding I_d-*Time* sweeping curves.

3.2 Real-Time Detection

To detect the real-time response of the channel current to the voltage pulses generated in the pulsed measurement, a function generator (Agilent 81150A) was combined with a semiconductor device analyzer (Agilent B1500A). The setup is shown schematically in Figure 8. The device analyzer connects the source/drain terminals of the transistor and records changes in current induced by changes in gate voltage. The function generator and device analyzer are started simultaneously by a LabVIEW program.

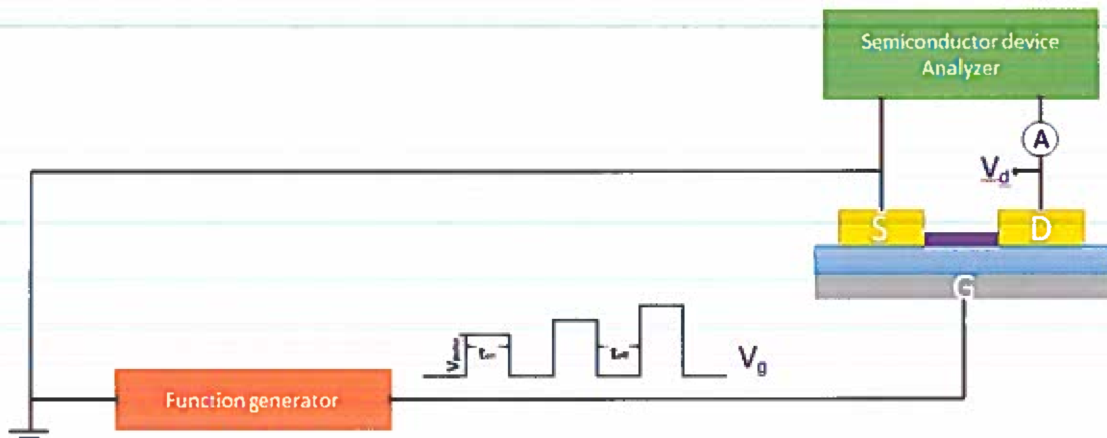

Figure 8. Setup for real-time detection of changes in channel current induced by pulsed gate voltage.

Chapter 4. Results and Interpretation

4.1 Transistor Electrical Characteristics

All DC electrical characterizations were performed under dark conditions in the ambient environment. The transfer characteristics of the monolayer transistor are shown in Figure 9. The transistor shows n-type transfer behavior (Figure 9a) with an ON/OFF ratio of ~10^8, a subthreshold swing of 127 mV/dec, and negligible gate leakage. As shown in Figure 9b, the current density reaches around 15 uA/um in the saturation region. Schottky behavior is observed in the low V_d region and limits the total current attainable by this transistor.

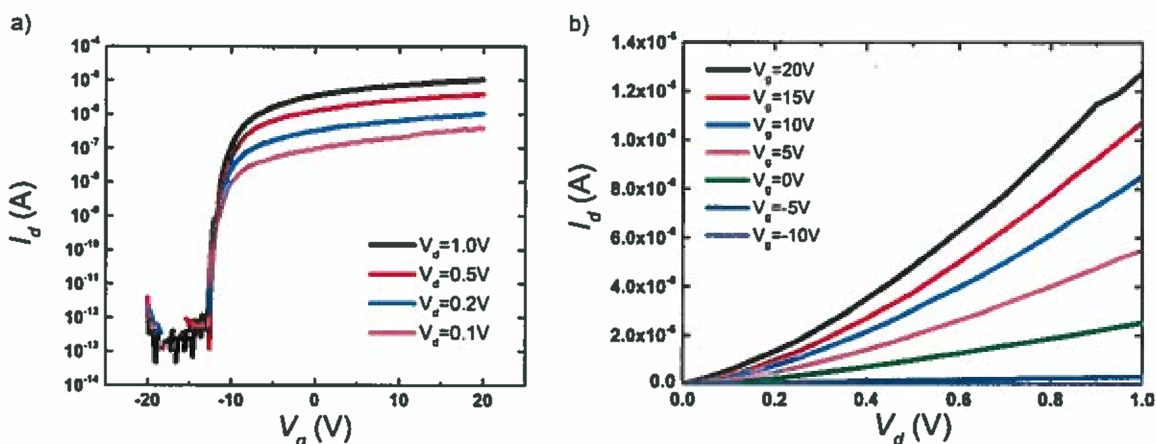

Figure 9. a) Transfer curves with gate voltage sweeping from -20V to 20V and drain bias voltage ranging from 0.1V to 1V. b) Source/drain electrical characteristics for different gate bias voltages.

4.2 Hysteresis Analysis Depending on Different Parameters

As the gate voltage is swept back and forth, a clear hysteretic behavior is observed (Figure 10). We have characterized this hysteresis by varying different test parameters. Figure 10a shows the I_d-V_g behavior when gate voltage is swept from -20V to +20V and then back to -20V with different sweeping intervals. Notice that with higher sweeping interval values (i.e. fewer sweeping points), the hysteresis window is narrower, and the ON current at 20V is higher. Figures 10b and 10c show the transfer characteristics for different starting voltages while keeping the sweeping interval unchanged. It is clear that

a more negative starting voltage leads to a negative shift in threshold voltage. We can now use this observation to understand the nature and distribution of the trap centers.

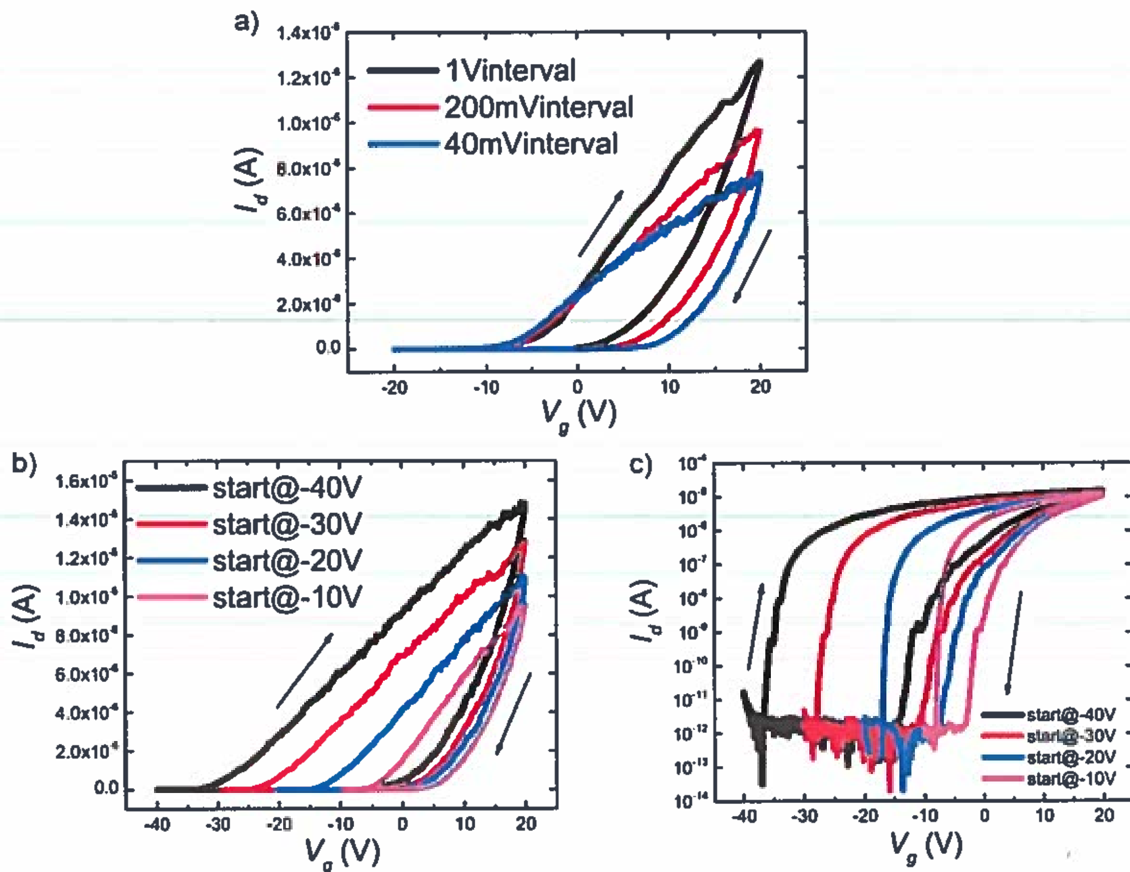

Figure 10. a) I_d-V_g curves with different sweeping intervals ranging from 40mV to 1V. b) and c) I_d-V_g curves in linear axes (b) and in log y axis (c) with different starting voltages from -40V to -10V, with the same ending voltage (20V). The sweeping interval is kept unchanged at 200mV. Drain voltages are all 1V.

Note that once the trapping/detrapping occurs, a reasonably long relaxation period is needed before the interface states can return to their initial conditions, even after the gate bias has been removed. This is responsible for the speed-dependent and scale-dependent hysteresis seen in Figures 10a and 10b.

	SS@10nA(V/dec)
-40V start	1.50
-30V start	1.36
-20V start	1.12
-10V start	0.653

Table 1. *SS* values at 10 nA channel current for different starting voltages.

From Figure 10c, we see that the subthreshold swing (*SS*) degrades as the DC sweeps are started at increasingly negative voltages (Table 1). This observation allows us to estimate the effective density of interface states from [23]:

$$SS = \ln(10)\left(\frac{kT}{q}\right)\left[1+\frac{q}{C_{ox}}\left(\sqrt{\frac{\varepsilon_{ch}N_a}{4\varphi_B}}+qD_{it}\right)\right] \tag{5}$$

Here we neglect the effect of channel depletion capacitance since the changes in *SS* value due to different starting voltages are significantly larger than the ideal *SS* value of 60 mV/dec. Table 1 considers the *SS* at a fixed channel current of 10 nA for different sweeping parameters while keeping all other channel conditions constant. The calculated D_{it} results are shown in Table 2. The interface traps are found to have an energy-dependent distribution; there are more interface states at higher energies. Our results are consistent with those of previous studies that used optical techniques [24].

	D_{it}@10nA(10^{12}/cm^2.eV)
-40V start	17.3
-30V start	15.7
-20V start	12.9
-10V start	7.53

Table 2. Density of interface states for different starting voltages.

Now that we have quantified the nature and distribution of the trap states, we can move on to analyzing the hysteresis that results from these trap centers. To achieve this, we use

the "pulsed measurement" technique mentioned in Chapter 3.1.

The real-time changes in current versus sweeping gate bias are shown in Figure 11a. The current clearly decays after each pulse, corresponding to the trapping/detrapping mechanism. In Figure 11b, the normal pulsed measurement mode results are compared with the DC transfer curve for the same sweeping scale and interval (200 mV). The time needed to capture one point in DC measurement is ~100 ms without any relaxation period between consecutive points. With 100 ms pulse width and 100 ms relaxation period, the effects of interface trapping are dramatically reduced, and the ON current increases. When reducing the pulse width to 1 ms—thereby decreasing the time during which trapping/detrapping can occur—the interface effects are further minimized, leading to an enhancement of channel current by nearly 4 times compared to that of the DC mode. 1 ms pulse width and 100 ms relaxation period appear to be the optimal measurement parameters. No further enhancement was observed for longer relaxation periods within the limit of our measurement instruments. This indicates that time needed for detrapping is significantly long.

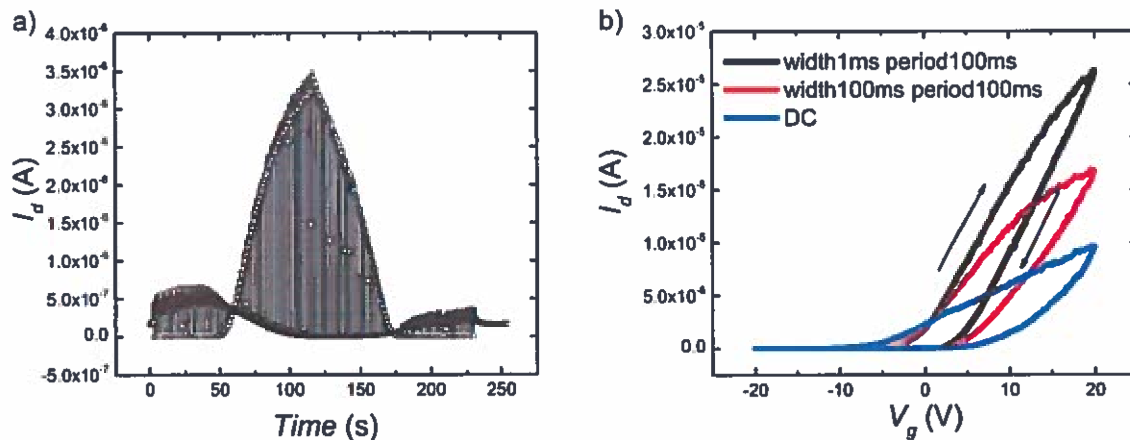

Figure 11. a) Complete I_d-*Time* curve produced by the normal pulse series. b) Normal pulsed measurement *I-V* curves compared with DC mode. Drain voltages are all 1V.

Next, the zigzag pulse series was set up in which a voltage pulse follows another one with the same amplitude but opposite polarity (e.g. -20V, 20V, -19V, 19V, ..., 19V, -19V, 20V, -20V). Figure 12a shows the time domain behavior of the drain current. The result is

fairly symmetrical, especially in the low voltage region (100 s ~ 150 s). Figure 12b shows a comparison of the I_d-V_g behavior measured by the normal pulse mode and the zigzag pulse mode. Notably, for the zigzag mode, the hysteresis is significantly smaller. In fact, the hysteresis completely disappears in the linear region (0V ~ 10V). Moreover, the curves with 1 ms pulse width and 100 ms relaxation period nearly overlap each other. The curves with different sweeping scales ranging from ±10V to ±30V also nearly overlap each other as shown in Figure 12c. The threshold voltage stays at ~ -1.5V for all measurements done in the zigzag mode, showing a lightly n-doped MoS_2 property. Thus, the zigzag pulse mode is a robust method for measuring the *I-V* characteristics. It eliminates the negative effects of the trap states for the most part and reveals the intrinsic nature of the material itself.

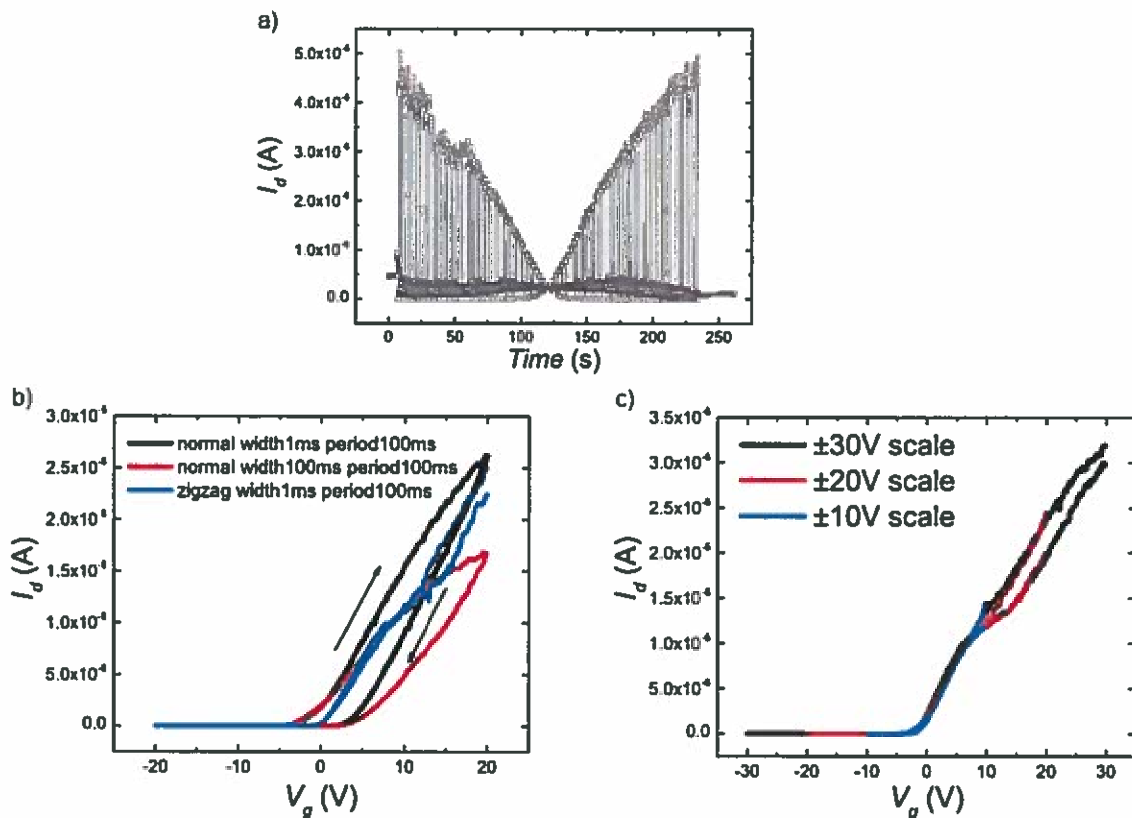

Figure 12. a) Complete I_d-*Time* curve generated by the normal pulse series with 10V amplitude and 200mV sweeping interval. b) Zigzag pulsed measurement *I-V* result compared with normal pulse series mode. c) Zigzag pulsed measurement with different sweeping scales. Drain voltages are all 1V.

Using Equation 3 from Chapter 1.2, the mobility extracted from the DC sweeps is 1.74 cm^2/V-sec for the forward sweep and 3.14 cm^2/V-sec for the reverse sweep. Therefore, there is nearly a 100% difference between the results from the two branches of the hysteresis loop. By contrast, mobility extracted from the zigzag pulse mode data is almost identical for both branches (5.91 cm^2/V-sec for the forward sweep and 5.59 cm^2/V-sec for the reverse sweep). Note that even in the presence of pulsed gating, some of the states can be filled/empty in the steady state (pulsed gating only removes the dynamic trapping/detrapping), which can adversely affect the mobility.

4.3 Conclusion

In summary, we have explored the interface states in a monolayer MoS_2 transistor. We have shown that the hysteresis in the DC sweeps can be exploited to quantify the nature and density of the interface trap states that are created by adsorption of various contaminant molecules. Such trap states severely affect device behavior such as ON current and mobility. We have shown that by applying carefully designed pulses to the gate, the effects of the trap states can be removed, revealing the intrinsic properties of the channel material. The techniques shown here are applicable in general to all other emerging channel materials.

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