An Energy-Efficient Triple-Channel UWB-based Cognitive Radio

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Acknowledgement

Working and studying with brilliant people in the superb environment at UC Berkeley was one of the most fortunate and honorable opportunities in my whole life. Most of all my gratitude to my research advisor, Prof. Jan M. Rabaey is so sincere and deep that I can't even find proper words to express it. Without the dedication, insight, and tolerance he showed me during my stay, I could not have reached this point, much less conducted proper research. I also would like to convey my deepest thanks to Prof. Ali M. Ninejad for the discussion and his devotion to the field of research. It was also my honor to have Prof. Paul K. Wright as my qualification committee.

An Energy-Efficient Triple-Channel UWB-based Cognitive Radio

By

Nam-Seog Kim

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Committee in charge:

Professor Jan Rabaey, Chair

Professor Ali M. Niknejad

Professor Paul K. Wright

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The proposed triple-channel UWB-based cognitive radio exploits spectral crowding and coexistence of other wireless devices as the number of sensors and wearable computing devices increases in 3.1GHz to 10.6GHz ISM band to achieve energy efficient 1Gb/s short-range wireless communication. A dual-resolution analog wavelet-based spectrum performs bandwidth-and frequency-agile band pass filter (BPF) to detect narrowband and wideband interferers with low power consumption. A charge-pump-based triangular waveform generators and a source follower type low pass filter (LPF) generates basis function for the spectrum sensing with 132MHz sensing resolution. A Low power integer-N QPLL with reduced reference spur by digital calibration on mismatch of the charge pump current supports the tuning frequencies with a linear tuned wide range two stage ring-VCO and a low power programmable true-single-phase-clock (TSPC) divider. The proposed Triple-channel UWB-based cognitive radio was fabricated in 1V 65nm CMOS GP process. The test chip size is 2.3×2 mm^2, and the active area is $2.1mm^2$. The data rate by using triangular shaped BPSK data is 1Gb/s at 1m communication. The lowest FoM of the energy/bit is 61pJ/bit, and the highest FoM is 102pJ/bit. It achieves BER from 9.2×10^{-7} to 1.1×10^{-4} according to frequency allocation of the triple-channels. The triple-channel UWB-based cognitive radio can provide energy efficient high-data rate wireless communication even with over 20% channel occupation.

Dedicated to my Family…

Contents

List of Figures

List of Tables

Acknowledgments

Working and studying with brilliant people in the superb environment at UC Berkeley was one of the most fortunate and honorable opportunities in my whole life. Most of all my gratitude to my research advisor, Prof. Jan M. Rabaey is so sincere and deep that I can't even find proper words to express it. Without the dedication, insight, and tolerance he showed me during my stay, I could not have reached this point, much less conducted proper research. I also would like to convey my deepest thanks to Prof. Ali M. Ninejad for the discussion and his devotion to the field of research. It was also my honor to have Prof. Paul K. Wright as my qualification committee.

The Berkeley Wireless Research Center (BWRC) was the ideal place to study, discuss, and make chips. I've been proud of being a member of this great facility from the first day. I still vividly remember my hard feeling of pride when I first got my cubicle at BWRC. In the center, Brian helped me how to do tape out, and Fred had done his all effort for my chip testing. Other BWRC staff gave me a lot of support that I can focus on my research work.

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Chapter 1. Introduction

1.1 High-Data-Rate and Short-Range Radio

With the rapid evolution of wireless technologies, ubiquitous and always-on wireless system in homes and enterprises are expected to emerge in the near future as shown in Fig. 1.1. A wide range of heterogeneous systems, including wireless personal area networks (WPAN), wireless local area networks (WLAN), cellular, WiMAX, and satellite systems will be present together to meet consumer demand for wireless data capacity [1].

Figure 1.1: Ubiquitous wireless systems

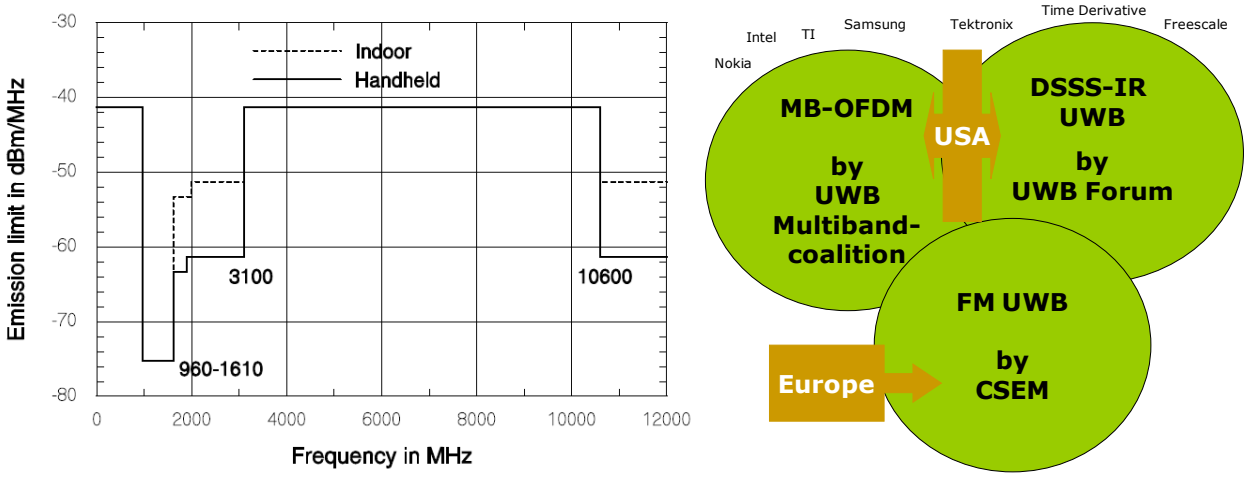


Figure 1.2: UWB spectrum mask as defined by FCC and various type of UWB radios

The ultra-wideband (UWB) and 60 GHz millimeter-wave based radios are expected to play a vital role in emerging WPAN for high-data-rate wireless applications. UWB technology, proposed for high-speed short-range applications, is one of the more active areas of focus in academia, industry, and regulatory circles. UWB technology affects the basic policy of spectrum regulation by using both the occupied and the unoccupied spectrum across the 3.1–10.6 GHz band as shown in Fig. 1.2. The -10dB bandwidth (BW) is greater than 500MHz and the transmitted power density is limited to be less than -41.3dBm/MHz in the UWB band. After allowance of commercialized UWB radio in United States from FCC [2], IEEE802.15.3a was an attempt to provide high rate UWB PHY based on multiband orthogonal frequency domain multiplexing (MB-OFDM) and direct sequence spread spectrum (DSSS) by industry mainly. However, the members of the task group were not able to come to an agreement choosing between two technology proposals.

In the meantime, Impulse radio systems have received much attention as a possible architecture for UWB transceivers from academia and research institute due to the large data bandwidth, low spectral interference with nearby channels, and simplicity of UWB transmitter/receiver

architectures with mostly digital implementations. Because of the low emitted power spectral density of -41.3dBm MHz mandated by the FCC, impulse radio is especially well suited for low-cost, low power, and short-range wireless communications [3].

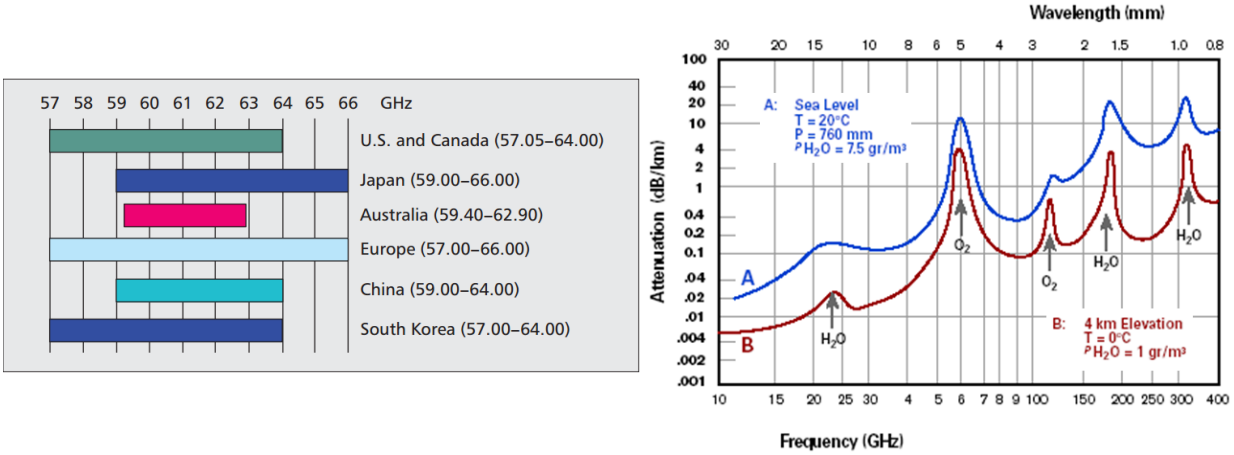


Figure 1.3: Worldwide spectrum availability at the 60 GHz band and Atmospheric propagation attenuation versus frequency.

There is also an ongoing effort to migrate indoor WLAN and WPAN networks toward less congested higher frequency unlicensed spectrum bands of 60 GHz (Fig. 1.3) to provide high data rates of up to several gigabits per second for indoor applications. Their interest in this frequency band stems from a phenomenon of nature: the oxygen molecule (O2) absorbs electromagnetic energy at 60GHz. Several standardization bodies have been working on the 60-GHz PHY and MAC protocols approaching 10Gb/s service rate. These include the IEEE 802.11ad and Wireless Gigabit Alliance (WiGig) for WLAN, and IEEE 802.15.3c, and Wireless HD for short-range PANs. The IEEE 802.15.3c standard defines a central controlled network topology and TDMA-based MAC protocol for 60-GHz wireless PANs [4]. The IEEE 802.11ad draft standard introduces a new

network architecture named Personal Basic Service (PBSS) without an access point in which each station can serve the role of a central coordination point which supports a combination of random access CSMA access and scheduled TDMA access modes. There are still a number of open research issues related to 60-GHz networks such as MAC-layer support for beam switching, diversity techniques to overcome propagation impairments, cooperative relaying [5]. Overall, 60-GHz technology is expected to mature during the next three to five years and will provide an important option for high-speed indoor connectivity associated with applications such as device docking and HD video.

1.2 Comparison between UWB Radio and 60GHz Radio

The plot in Fig. 1.4 compares the energy/bit of recently published UWB and 60GHz transceivers [6-15]. Energy/bit is a popular figure-of-merit (FoM) for wireless transceivers because it directly relates to the energy required to transmit and receive a single bit of data, or the efficiency of the radio. All results are measurements from fabricated custom integrated circuits. The highest data rate of the UWB radio and 60GHz radio goes up to 2Gb/s and 6.5Gb/s respectively. UWB radio output power (-41dBm/MHz) is much lesser than that of 60GHz radio. Thus, there is limitation to get the data rate of larger than 2Gb/s.

On the other hand, the lowest data rate of the 60GHz radio is 1 or 2Gb/s since average power consumption of the 60GHz radio is higher than that of the UWB radio mainly due to the difference of the carrier frequency. Two radio technology has the same dependence on the data rate as the FoM generally decreases with increasing data rate. Comparison on 2Gb/s data rate shows that UWB radio is more efficient than 60GHz radio in terms of energy consumption. This two

observations verify that UWB radio is more efficient less than 2Gb/s data rate wireless communication than 60 GHz transceivers.

Fig 1. 5 shows the required data rate with the resolution of the screen for uncompressed wireless data communication that is one of the example of high data rate short range wireless communication. In case of mobile devices like 4~5 inch smart phones and head-mount displays, around 1Gbps data rate is enough to provide the uncompressed data application.

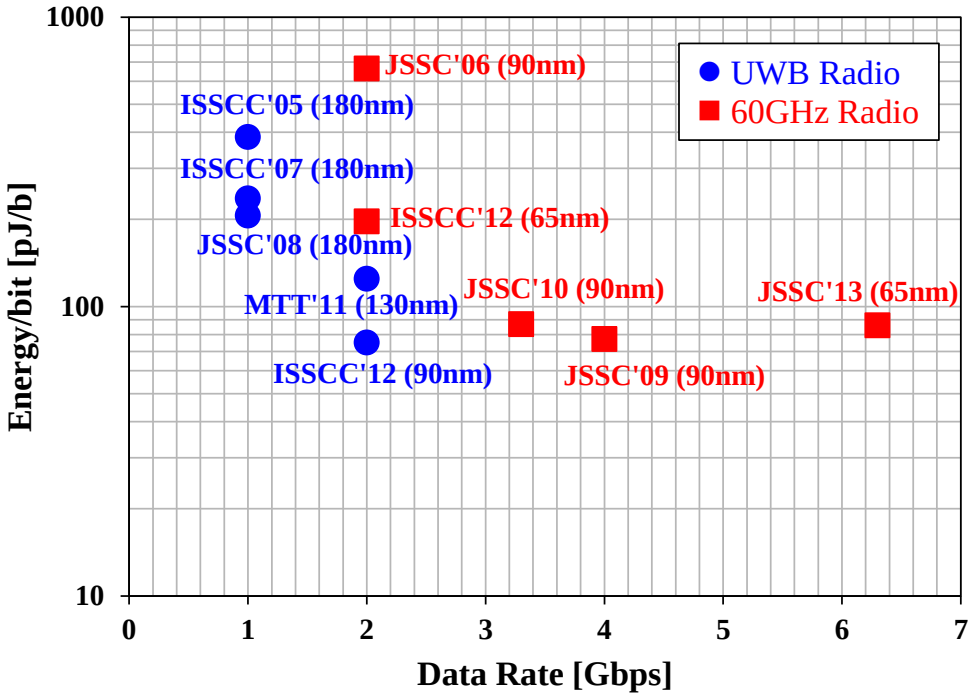


Figure 1.4: UWB and 60GHz transceivers FoM (Energy/bit) relative to data rate and process

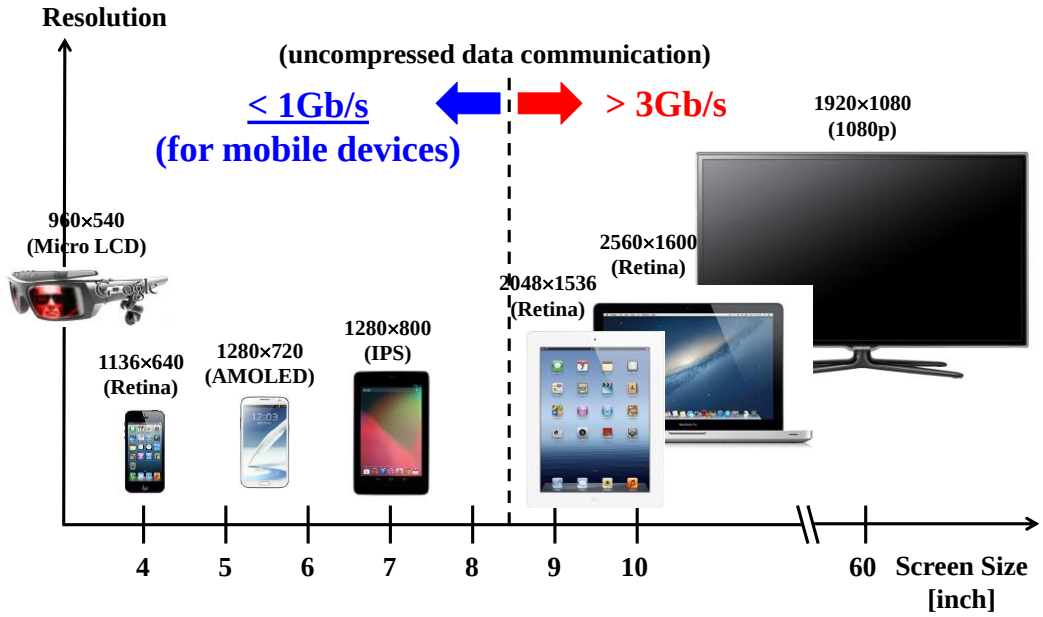
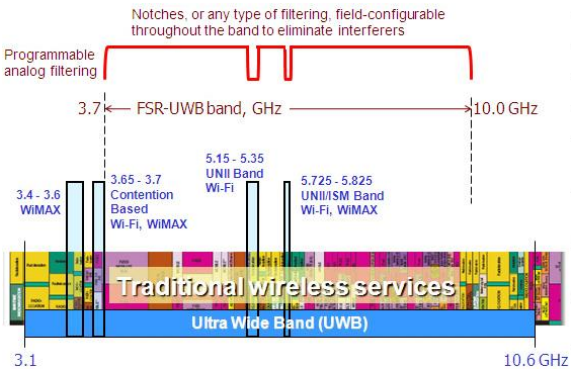


Figure 1.5: Required data rate with the resolution of the screen for uncompressed wireless data communication.

1.3 Interferers in UWB band

Potentially a large number of UWB devices may operate in close proximity of an indoor wireless application such as Wireless Local Area Network (WLAN). The UWB signal is a very low power signal and therefore the power of any single UWB device can be compared to that of a noise floor. But when a number of such devices operate simultaneously then the interference level could rise significantly above the level of the noise floor [16]. In addition to UWB interferers, Fig. 1.6 shows the narrow band licensed interferes like IEEE 802.11a and WiMax that operate in the UWB band also increases noise level of the desired UWB signals [17, 18].



	Frequency [GHz]	System	Power into Receiver
1	2.7~2.9	Airport surveillance radar (ASR-9)	-11.2 dBm
2	2.7~2.9	Next generation weather radar (NEXRAD)	-17.3 dBm
3	2.9~3.1	Maritime radio-navigation radar	-14.7 dBm
4	2.3~2.69	IEEE 802.16e mobile system (only shown terminal)	-36.9 dBm
5	3.4~3.8		-11.3 dBm
6	3.7~4.2	Geo-stationary orbit(GSO) fixed satellite service(FSS) downlink	-110.7dBm
7	4.2~4.4	FMCW and pulsed radar altimeter (only pulsed system shown)	-27.3 dBm
8	5.1~5.35 5.725~5.825	IEEE 802.11a and IEEE 802.11n systems	-15.2dBm
9	5.031~5.091	Microwave landing system (only shown worst case)	-23.5 dBm
10	5.6~5.65	Terminal Doppler weather radar (TDWR)	12.9 dBm
11	9.2~9.5	Maritime radio-navigation radar	11.6 dBm
12	10.95~11.2	GSO FSS and Non-GSO FSS downlink	-95.7 dBm

Figure 1.6: Services licensed to operate in the UWB band.

The traditional regulatory mechanism to handle interference is to separate contenders in space or in frequency. Thus regulators would impose artificial limits on transmissions to minimize interference. This approach precludes dynamic spatial/temporal reuse of the spectrum. Furthermore, with all frequency bands being allocated multiple times over, new spectrum is not readily available for such allocation.

UWB regulations in Japan, Europe, Korea and China has introduced Detect and Avoid (DAA) Schemes, in which UWB systems will first check whether there are NB systems existing in the environment and if it exists, NB avoidance techniques can be applied [19]. Thus, by declaring that all new users of the spectrum are secondary users and requiring that they must detect and avoid (DAA) the primary user, the regulators are opening up spectrum for opportunistic use. In the absence of DAA functionality, UWB devices would have to forfeit the band designated as 'DAA required' which would greatly reduce the spectrum available for communication.

1.4 UWB-based Cognitive Radios

The general idea behind Cognitive Radio is that performance can be improved by reducing interference if wireless systems were aware of other RF signals in the band. While communication engineers have historically thought of channel capacity and Shannon's Law simply in terms of bandwidth, Cognitive Radio considers an expanded view of the wireless channel by managing various dimensions of time, frequency, space, power, and coding [20].

Since UWB faces severe interference from narrowband system nearby, it will surely benefit more from utilizing Cognitive radio techniques implementing the collaborative coexistence process than will the non-UWB systems [21]. UWB is highly competent in satisfying many basic requirements of cognitive radio. Therefore, employing UWB in cognitive radio networks could be very instrumental for the successful penetration of cognitive radio into the wireless world. Nevertheless, since today's spectrum regulations prohibit employing UWB systems in the overlay mode, UWB based implementation of cognitive radio might not become a reality in the near future. However, besides being a strong candidate for practical cognitive radio implementation, UWB can be considered as a supplement to cognitive radio systems that are realized by means of other wireless technologies. Therefore, it can be concluded that this way or the other, UWB will be an inseparable part of cognitive radio applications. UWB can offer various kinds of support to cognitive radio network. These include sharing the spectrum sensing information via UWB, locating the cognitive nodes in a cognitive network by means of IR-UWB, and sensing the physical environment channel with IR-Spectrum Sensing.

1.5 Dissertation Outline

Chapter 2 discusses architecture level design for short-range high-data rate radio. UWB radio and 60GHz millimeter wave radio are compared in terms of energy efficiency with their data rate. Interference issue in UWB band is addressed with cognitive radio technique. Statistical analysis helps to define UWB-based cognitive radio architecture like modulation method and pulse shaping. Another investigation is done with a multi-channel UWB-based cognitive radio and a single-channel one. The analysis also gives high energy efficiency of the triple-channel UWB-based cognitive radio in over 20% channel occupancy cases.

Low power spectrum sensing algorithms are discussed with architecture level and circuit level approach in Chapter 3. Several algorithms are investigated to find out proper spectrum sensing solution for energy efficient, short-range, and high data rate UWB-based cognitive radios. Moreover, dual-resolution analog wavelet-based spectrum sensing is introduced to detect narrowband and wideband interferers together with low power consumption. This chapter also deals with the implementation of the proposed spectrum sensing, and the test chip results verify the efficiency.

In Chapter 4, the wide lock range and low power QPLL is introduced to utilize whole bandwidth of the UWB band and to accommodate higher capacity and data rates. Low power and wide lock range can be achieved with the proposed two stage ring oscillator having highly linear tuning characteristics over whole UWB frequency range. Digitally spur reduction technique on the charge pump mismatch is also introduced to reduce spur level, which causes malfunction in spectrum sensing operation. This chapter also deals with the implementation of the proposed QPLL with the spur reduction technique, and the test chip results verify the efficiency.

Low power programmable divider is addressed with true-single-phase-clock logic in chapter 4. Gated inverter technique is adopted for wide frequency range operation. Proper frequency range can be defined by the maximum cycle with timing analysis and the minimum cycle with sub-threshold leakage current analysis. This chapter also deals with the implementation of the proposed QPLL with the spur reduction technique, and the test chip results verify the efficiency.

Chapter 5 describes circuit details and demonstrates functionality of the proposed triple-channel UWB-based cognitive radio with the test chip. This approach can be shown to be optimal to avoid unknown narrowband and wideband interferers. The best and the worst cases of the channel allocation in the proposed radio according to channel occupancies are described, and the measurement results show the energy efficiency of the radio. Finally, this chapter summarizes performance of the chip and compares it with other recently published high data rate UWB and 60GHz radios.

Conclusions and contributions are given in Chapter 6.

Chapter 2. Multi-Channel High-Data-Rate UWB-based Cognitive Radio

2.1 Modulation Schemes of the UWB Radio

In UWB radio, simple modulation schemes are used such as pulse amplitude modulation (PAM) [22], on-off keying (OOK) [23], pulse position modulation (PPM) [24], binary frequency shift keying (BFSK) [25], binary phase shift keying (BPSK) [26], and transmitted reference [27]. BPSK outperforms PAM and PPM due to an inherent 3dB increase in separation between constellation points. The high data rate transmitters use BPSK modulation with a coherent receiver. BPSK can minimize losses in the link budget and can obtain the maximum distance with more than hundreds Mb/s.

2.2 Pulse Shaping of the UWB Radio

The time domain pulse shapes considered are the square, triangle, cosine, Gaussian, and Hann. These pulses are BPSK modulated with 1000 random bit sequence in time domain, and corresponding power spectral densities are shown in Figure 2.1 with MATLAB simulation. The carrier frequency is 7GHz. First, the null-to-null bandwidth (BW) for 1Gb/s data rate is examined. Hann and cosine require the minimum null-to-null BW of 2GHz, and Gaussian pulse has the maximum null-to-null BW of 6GHz. Second, each pulse requires different carrier amplitude to get -41dBm/MHz spectral density. The magnitude is normalized to the amplitude of the square pulse

case, which is defined as A in the figure. The parameter A is strongly related with power consumption of the transmitter. Gaussian pulse needs high power consumption since it has the largest BW. Third, side-lobe leakage is examined. Small side lobe leakage is desirable to get high spectral efficiency. Hann and Gaussian pulses have the lowest side-lobe leakage, and square pulse has the highest one. Finally, implementation complexity should be considered since the complexity is highly proportional to circuit power consumption. It is hard to generate Gaussian and Hann pulses in CMOS technology.

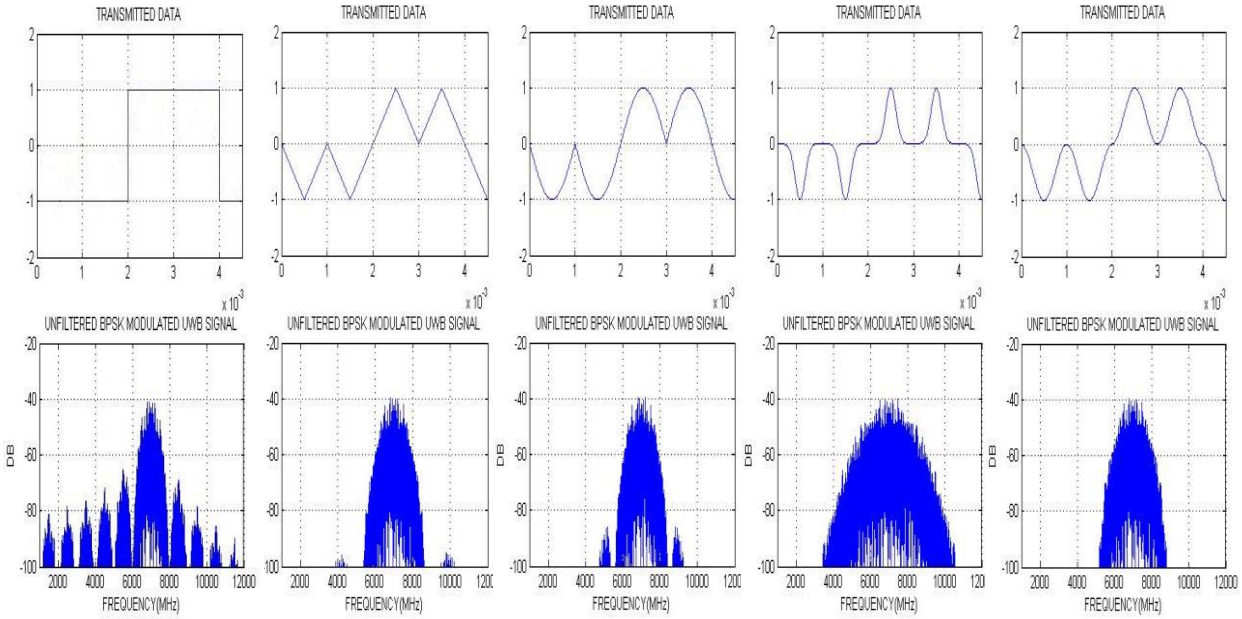


Figure 2.1: Time domain pulse shapes modulated with 1000 random bit sequence and power spectral density of the (a) square, (b) triangle, (c) cosine, (d) Gaussian, and (d) Hann for 1Gb/s data rate. The null-to-null bandwidth (BW) for 1Gb/s and the carrier amplitude (A) to get -41dBm/MHz spectral density are included.

Triangular pulses do not show the best results in terms of BW, A, and side-lobe leakage. However, if all design parameters including BW, A, side-lobe leakage, and complexity, are considered, triangular pulses can provides optimal performance among the five candidates. Triangular pulse shaping requires 2.8GHz null-to-null BW, 2.1 relative carrier frequency amplitude to square pulse, and about -54dBc/MHz side-lobe magnitude to main-lobe magnitude. Moreover, design complexity can be simplified even with CMOS technology, which leads to low power consumption.

2.3 Single-Channel UWB-based Cognitive Radio

Statistical analysis is done with the help of MATLAB for estimating the performance of the UWB-based Cognitive radio (CR). Fig. 2.2(a) shows an example of randomly decided interferers that takes 30% channel occupation of the UWB band, 3.1GHz to 10.6GHz. Contiguous 2.8GHz null-to-null frequency range is searched with the interferers' environment in order to accommodate the spectrum of the 1Gbps random triangular BPSK pulses. Fig. 2.2(b) shows the allocated at the vacant channel after searching 2.8GHz contiguous bandwidth where does not have interferers. Energy/bit is calculated at the allocated center frequency. The allocated channel carrier frequency is at around 9GHz in this example.

This operation is done repeatedly by 1000 times as changing the location of the interferers. The resolution of carrier frequency of the interferers is 10MHz from 3.1GHz to 10.6GHz. The random variables are generated with uniform distribution. On the other hand, the number of interferers is fixed during the 1000 iteration, which defines channel occupancy in the UWB band.

Energy/bit is one of the figure of merits (FoM) to characterize the performance of a device, system or method. However, it does not count communication reliability, so it is not proper quantity parameter for measuring the CRs' performance. Thus, alternative quantity parameter of energy per useful bit (EPUB) is used to characterize the UWB-based CR. EPUB can be expressed as equation (2.1).

$$EPUB = P / (R*(1-BER)) \quad (2.1)$$

where P is power consumption, R is data rate, and BER is bit error rate of the system.

The EPUB of the single channel UWB-based CR can be estimated with specific channel occupation rate by averaging the 1000 different EPUB values.

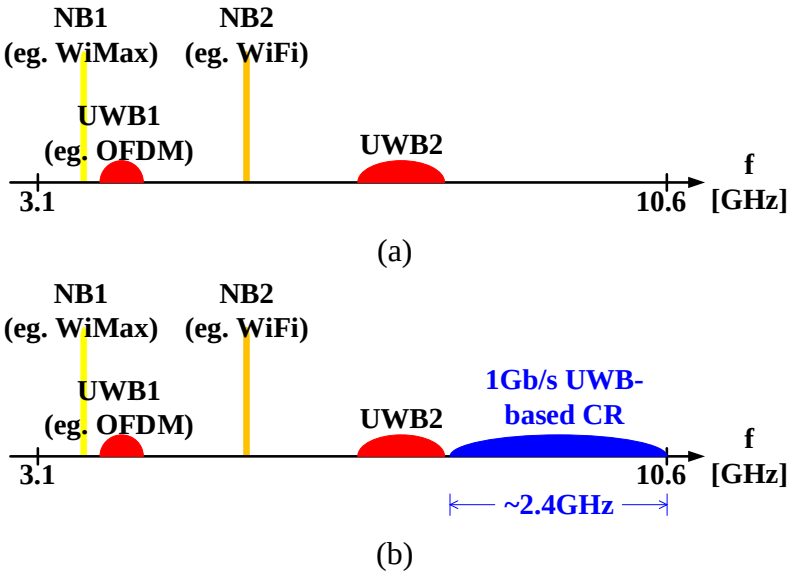
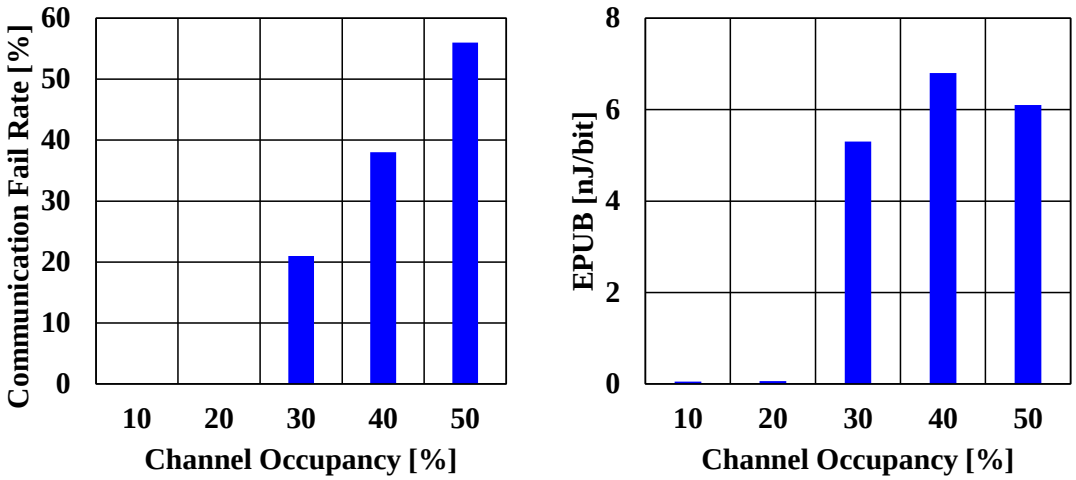


Figure 2.2: (a) An example of the interferers with 30% channel occupation in MATLAB simulation (The carrier frequency is randomly decided with 10MHz resolution from 3.1GHz to 10.6GHz) and (b) a single-channel 1Gb/s UWB-based CR with triangular BPSK pulses.

Fig. 2.3 (a) shows the communication fail rate with different channel occupancy cases. When the interferes takes frequency range by over 20% of the whole band, the probability that there is no contiguous 2.8GHz BW to accommodate the spectrum of the 1Gbps random triangular BPSK pulses is increased. The case of no 2.8GHz BW in the band is defined as communication fail since desired signal will be corrupted with interferes.



(a) (b)

Figure 2.3: (a) Communication fail rate due to non-contiguous 2.8GHz BW and (b) EPUB except communication fail cases for the single-channel UWB-based CR along with channel occupancy rate.

Fig. 2.3(b) shows the average EPUB with various channel occupancy except the communication fail cases. The average EPUB value starts increasing over 20% channel occupancy even if the communication failure cases are not counted. If the interferers are located at lower frequency range, the center frequency of the UWB-based CR is allocated at higher frequency as shown in Fig. 2.2(b). If the carrier frequency is high, free space path loss is getting higher than that

of the low frequency. The loss reduces SNR of the received signal and increases bit error rate (BER) as shown if Fig. 2.4. Thus, transmitter should send the same data repeatedly in order to receive a big data like high definition pictures or movies, which increases energy consumption on the communication.

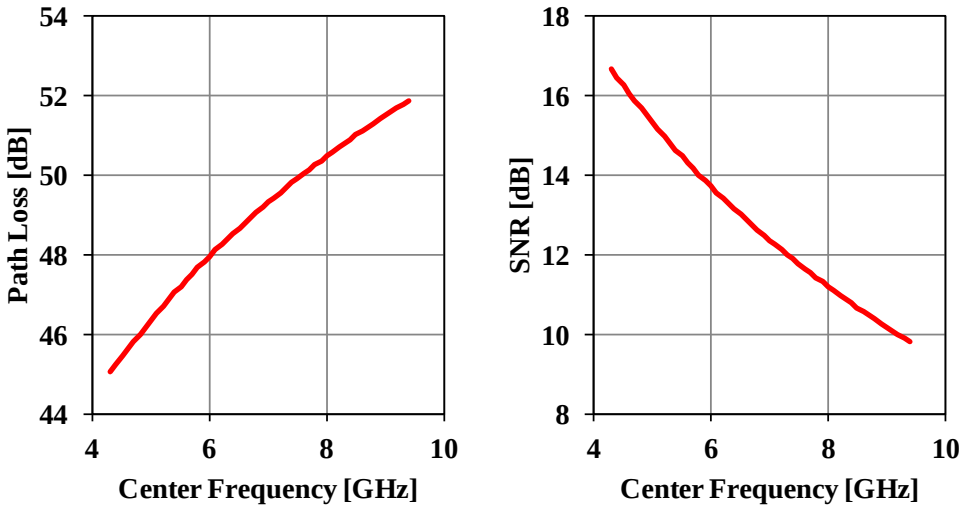


Figure 2.4: (a) Free path loss and (b) the SNR at the receiver with center frequency

2.4 Multi-Channel UWB-based Cognitive Radio

Multi-channel UWB-based CR is investigated to get high energy efficiency by using discrete channel spectrum aggregation technique. This one can be regarded as previous channelized receiver [8], but previous channelized radio has fixed carrier frequency for each channel. All channels of the multi-channel UWB-based CR operate independently, but they are not allocated at the same carrier frequency and have channel spacing to each other.

Fig. 2.5 shows how the multi-channel UWB-based CR uses discrete channels efficiently in order to allocate each carrier frequency at low frequency bands. In this example, triple-channel CR

is used and the null-to-null BW of each channel is 933MHz. Three sub-channel spectrums are allocated at lower frequency to compensate the free space path loss. Compared to single channel radio in Fig. 2.2(b), the allocated channel carrier frequencies are around 4.5GHz, 6GHz, and 8.5GHz in this example, which are lower than that of single channel radio example in Fig. 2.2(b).

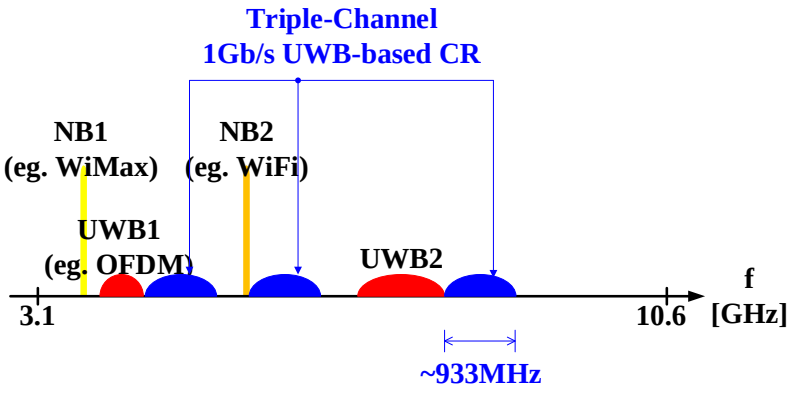


Figure 2.5: An example of the interferers with 30% channel occupation in MATLAB simulation (The carrier frequency is randomly decided with 10MHz resolution from 3.1GHz to 10.6GHz) and with a triple-channel 1Gb/s UWB-based CR with triangular BPSK pulses.

Fig. 2.5(a) shows the same example with Fig. 2.2(a). Fig. 2.5(b) shows how the multi-channel UWB-based CR uses discrete channels efficiently in order to allocate each carrier frequency at low frequency bands. In this example, triple-channel CR is used and the null-to-null BW of each channel is 933MHz. Three sub-channel spectrums are allocated at lower frequency to compensate the free space path loss. Compared to single channel radio in Fig. 2.2(b), the allocated channel

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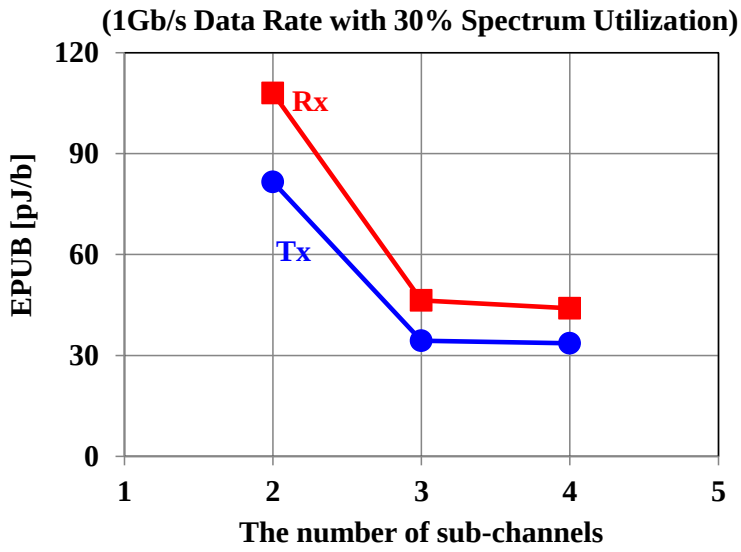


Figure 2.6: EPUB with the number of sub-channels in multi-channel UWB-based CR for 1Gb/s data rate with 30% spectrum utilization environment.

The statistical analysis is done to find out the optimum number of sub-channels of the multi-channel UWB-based CR for 1Gb/s data rate with 30% spectrum utilization environment. The number of channels is varied from two to four since five channels cannot be implemented since FCC allows UWB radios to have 500MHz of -10dB BW. Fig. 2.6 shows that three or four sub-channels have lower EPUB than that of two channel radio because less than 933MHz of null-to-null BW can be easily allocated at the lower frequency band under 30% channel occupancy environment. Three-channel radio is optimal as considering chip area for the multi-channel radio.

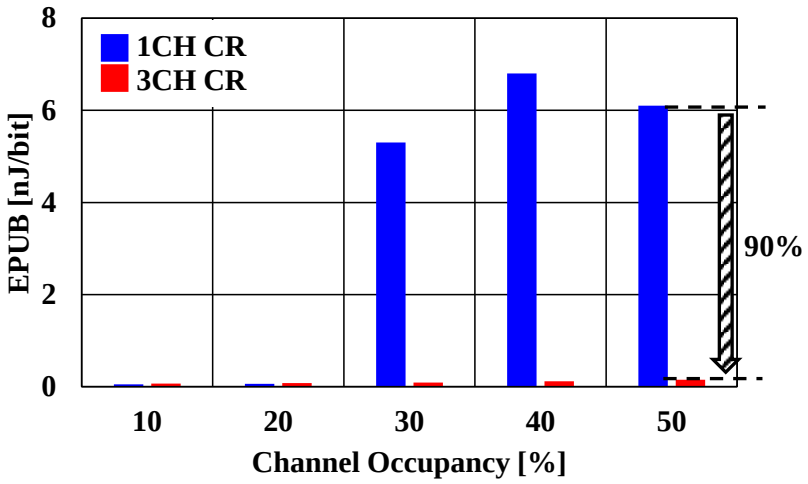


Figure 2.7: Performance comparison between a single-channel and a triple-channel UWB-based CRs in terms of EPUB except communication fail cases of the single-channel CR along with channel occupancy rate.

Fig. 2.7 compares performance in terms of EPUB between a single-channel and a single-channel and a triple-channel CRs. In case of the single-channel radio, communication failure cases are not counted. The triple-channel radio does not have any the failure to find out three sub-channels of about 933MHz. When the channel occupancy is below 20%, single channel radio is more energy efficient than the triple-channel radio since the carrier frequency of the single-channel radio can be located at lower frequency with high probability, and the single-channel radio has lesser circuitry than that of the triple-channel radio. However, when the channel occupancy goes over 20%, triple channel radio is much more energy efficient than the single-channel radio due to low probability of finding 2.4GHz contiguous vacant channel for the single channel radio. On the other hand, the probability to find out three discrete 933MHz contiguous channels is 100% even up to 50% channel occupancy case.

2.5 Adaptive BW Multi-Channel UWB-based Cognitive Radio

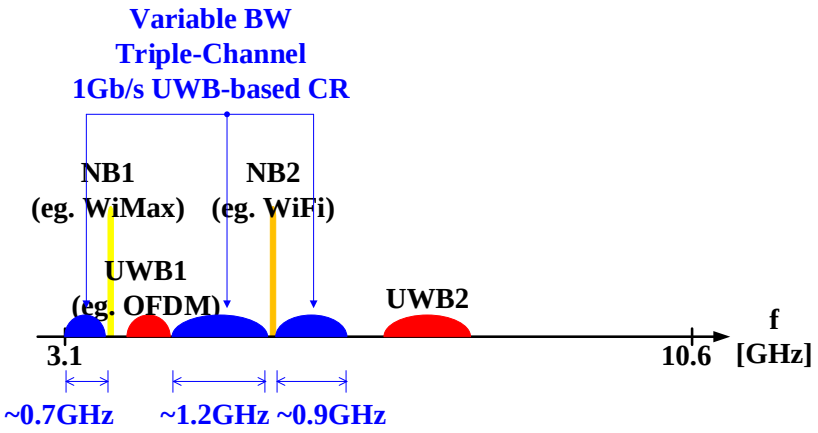


Figure 2.8: An example of the interferers with 30% channel occupation in MATLAB simulation (The carrier frequency is randomly decided with 10MHz resolution from 3.1GHz to 10.6GHz) with a triple-channel 1Gb/s UWB-based CR with triangular BPSK pulses and adaptive BW for respective sub-channels.

Fig. 2.8 illustrates adaptive BW triple-channel UWB based cognitive radio with 30% channel occupation. Each channel BW is adjustable in order to be allocated more efficiently lower frequency band than the constant BW triple-channel cognitive radio. In this example, the null-to-null BWs are about 700MHz, 1.2GHz, and 900MHz respectively. The allocated channel carrier frequencies are 3.45GHz, 4.4GHz, and 5.45GHz. Compared to the constant BW triple-channel cognitive radio in Fig. 2.5, the carrier frequencies of the adaptive BW triple-channel radio are lower than those of the constant BW triple-channel cognitive radio.

Three sub-channel spectrums are allocated at lower frequency to compensate the free space path loss. Compared to single channel radio in Fig. 2.2(b), the allocated channel carrier frequencies are around 4.5GHz, 6GHz, and 8.5GHz in this example, which are lower than that of single channel radio example in Fig. 2.2(b).

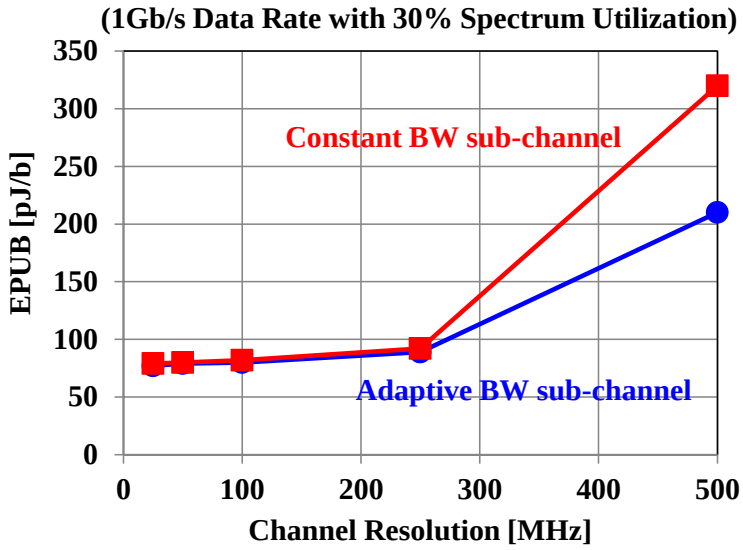


Figure 2.9: Comparison between constant BW and adaptive BW of the triple-channel CR in terms of EPUB with channel resolution.

Fig. 2.9 compares performance in terms of EPUB between a constant BW and an adaptive BW of the triple-channel CRs with channel resolution variation. The channel resolution defines the carrier frequency tuning step. When the resolution is 500MHz, an adaptive-BW radio has better performance since adaptive BW channel allows one or two of three channels to have less than 933MHz BW. The small spectrum channel can be more easily allocated at lower frequency band. However, when the resolution is less than 250MHz, there is no big difference between two radios because of FCC regulation. FCC limits the minimum -10dB BW of 500MHz for UWB radios.

Thus, if the channel resolution is less than 500MHz, adaptive BW technique lose its own flexibility to shrink channel bandwidth to use small vacant channel in lower frequency UWB band. Moreover, Adaptive BW technique requires different baseband clock frequencies for each channel, which increases design complexity and increases power consumption of the system.

2.6 Link Budget for Triple Channel UWB-based Cognitive Radio

It is possible to do a rough link budget calculation for the UWB-based CR. It is worth noting that a typical link budget found in a textbook [28] is often intended only for narrowband systems and has a frequency-based derivation implicitly including narrowband assumptions (e.g. that the signal bandwidth is small enough that it experiences similar fading to the center frequency).

Care must be taken if this narrowband link budget model is used, as certain terms like "center frequency" or "sensitivity" may appear misleading. An UWB signal may be defined to have a center frequency, but what happens at that frequency may not accurately represent what happens over the entire bandwidth. Additionally, impulse-UWB systems have receiver sensitivity, but it is in part a function of the pulse shape and is better represented as a received power over some period of time than as a simple, single number. An ultra-wideband link budget may be created by expanding the narrowband Friis power transmission formula [29] to be a function of frequency and integrating over the desired bandwidth [30].

Carrier to noise ratio (CNR) can be calculated as equation (2.2).

$$CNR = (P_{TX} + G_{TX} - L_{FS} + G_{RX}) / (N_{CH} + NF_{RX}) \quad (2.2)$$

The P_{TX} is transmitter output power in dBm as equation (2.3).

$$P_{TX} = -41.3dBm + 10*\log_{10}(BW*\eta) \quad (2.3)$$

where η is spectrum filling ratio. For example, η of the rectangular spectrum is 1. Real spectrum shape cannot be rectangular, so η is always less than 1. One of the purpose of pulse shaping for UWB radios is to maximize the value of the parameter, η.

G_{TX} and G_{RX} are transmitter antenna gain and receiver antenna gain in dBi respectively.

L_{FS} is free space loss in dB as equation (2.4).

$$L_{FS} = 20*\log_{10}(4\pi*d/c) \quad (2.4)$$

NCH is additive white Gaussian noise (AWGN) as equation (2.5)

$$NCH = -114dBm + 10*\log_{10}(BW) \quad (2.5)$$

NFRS is the noise figure of the receiver chain.

Signal to noise ratio (SNR) can be calculated with CNR, BW, and data rate (R) as equation (2.6).

$$SNR = CNR*3dB\_BW/R \quad (2.6)$$

Bit error rate with BPSK can be calculated with Q-function as equation (2.7).

$$BER = Q(sqrt(2*SNR)) \quad (2.7)$$

Table 2.1 summarizes target link budget with the single-channel UWB-based CR for 1Gb/s data rate. This estimation can also be applied to the triple-channel UWB-based CR since the target performance is the same with the single-channel radio. In this analysis, packet based communication is used, and the packet length is 1kb. The worst pack loss is 10%. The target BER is less than 1×10^{-4} with 8.3dB SNR of the required SNR with BPSK modulation.

Table 2.1: Link budget of the single-channel UWB-based CR for 1Gb/s data rate

Data Rate	1 Gb/s
EIRP	-41.3 dBm/MHz
Communication Distance	1m
Required Min. null-to-null BW	~ 2.8 GHz
3dB BW	~ 1 GHz
Spectrum Filling Ratio (η)	0.6
Packet Length	1 kb
Worst Packet Loss	0.1
BER	$< 1 \times 10^{-4}$
Required SNR with BPSK @ Receiver	8.3 dB

Target communication distance is from 0.1m to 1m, and the UWB-based CR uses whole UWB band from 3.1 to 10.6GHz. The result is plotted in Fig. 2.10 for different carrier frequencies from 4 to 9GHz with 0.1m and 1m communication distance. A single-channel UWB-based CR requires 2.8GHz null-to-null BW, so it can covers whole UWB band from 3.1 to 10.6GHz. This simple link budget predicts that the receiver sensitivity should be less than -63dBm and variable gain in receiver chain should provide 20dB gain variation. The required noise figure (NF) of the receiver chain is less than 7dB.

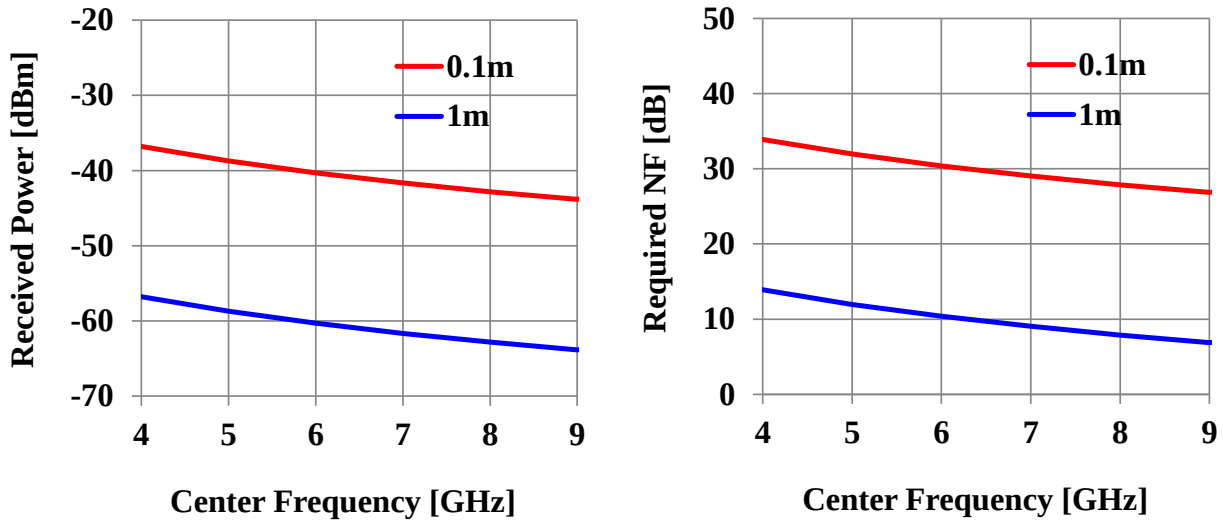


Figure 2.10: (a) Receiver sensitivity and (b) required noise figure of the receiver chain of the single-channel UWB-based CR with different carrier frequency and communication distance.

2.7 Group Delay of Multi-Channel UWB-based Cognitive Radio

One of the main challenges for a pulse-based system is the reliable generation of the time-domain pulses that meet the FCC's spectral mask. In addition to gain from the path loss reduction of the multi-channel UWB-based CR, it also mitigates the group-delay profile of a transmission path describing how the different spectral components of a signal arrive at the receiver, even in the absence of multipath fading and in a line-of-sight communication.

While designing a UWB antenna with a flat gain response and a good return loss is a challenge in itself, simultaneously maintaining a constant group delay over the signal BW only increases the difficulties [31]. Due to the group-delay distortion, the receiver performance can degrade significantly. Moreover, due to the changes in the location of the antenna and its surroundings, the channel transfer characteristics between the transmitter and the receiver change, and it is difficult to predict the group-delay profile of the complete communication path.

Chapter 3. Dual-Resolution Analog Wavelet-based Wideband Spectrum Sensing

3.1 Spectrum Sensing in UWB band

Depending on the regimes of spectrum utilization, the front-end architecture of CRs can be quite different [32]. In early stage of CR network deployment, the spectrum utilization is expected to be low (around 5%) and there is little spectrum scarcity. In this case, the radio front-end starts with a tunable narrowband band pass filter (BPF) to search for one narrow band signal. Existing spectrum sensing techniques are largely categorized into energy detection [33] and cyclostationary feature detection [34]. When the spectrum utilization is medium (below 20%) resulting in medium spectrum scarcity, the radio front-end should adopt a wideband architecture to search over multiple frequency bands at a time. Multiple narrow band BPFs can be employed to form a filter bank for wideband, sensing [32], but this architecture requires an increased, number of components and the filter range of each BPF is preset. In future networks where spectrum utilization is high (above 20%), the significant spectrum scarcity would call for different spectrum sharing mechanisms for the UWB based cognitive radios, which in turn entail different sensing tasks for spectrum overlay.

3.2 Wideband Spectrum Sensing

A simple approach to wideband spectrum sensing is to directly acquire the wideband signal using a high sampling rate ADC and then use digital signal processing techniques to detect spectral opportunities as shown in Fig. 3.1(a). Fast Fourier transform (FFT) is used to convert the wideband signals to the frequency domain. Finally, spectral opportunities were detected using binary hypotheses tests, where H_0 denotes the absence of interferers and H_1 denotes the presence of interferers. The optimal detection threshold was jointly chosen by using optimization techniques. Such an algorithm can achieve better performance than the single-band sensing case [35].

A wavelet-based spectrum sensing algorithm models the power spectral density (PSD) of the wideband spectrum as a train of consecutive frequency sub-bands, where the PSD is smooth within each sub-band but exhibits discontinuities and irregularities on the border of two neighboring sub-bands. The wavelet transform was then used to locate the singularities of the wideband PSD, and the wideband spectrum sensing was formulated as a spectral edge detection problem, as shown in Fig. 3.2(b) [36].

However, special attention should be paid to the signal sampling procedure. In these algorithms, sampling signals should follow Shannon's celebrated theorem: the sampling rate must be at least twice the maximum frequency present in the signal (known as Nyquist rate) in order to avoid spectral aliasing. Suppose that the wideband signal has frequency range 3~11 GHz; it should be uniformly sampled by a standard ADC at or above the Nyquist rate, 22 GHz, which will be unaffordable for next generation mobile networks.

Therefore, sensing wideband spectrum presents significant challenges in building sampling hardware that operates at a sufficiently high rate and designing high-speed signal processing

algorithms. With current hardware technologies, high-rate ADCs with high resolution and reasonable power consumption (e.g., 22GHz sampling rate with 16 bits resolution) are difficult to implement. Even if it becomes true, the real-time digital signal processing of sampled data could be very expensive.

One naive approach that could relax the high sampling rate requirement is to use super-heterodyne (frequency mixing) techniques that "sweep" across the frequency range of interest, as shown in Fig. 3.1(c). A local oscillator (LO) produces a sine wave that mixes with the wideband signal and down-converts it to a lower frequency. The down-converted signal is then filtered by a band pass filter (BPF), after which existing narrowband spectrum sensing techniques can be applied. This sweep-tune approach can be realized by using either a tunable BPF or a tunable LO. However, this approach is often slow and inflexible due to the sweep-tune operation.

Another solution is the filter bank algorithm as shown in Fig. 3.1(d) [37]. A bank of prototype filters (with different shifted central frequencies) was used to process the wideband signal. The baseband can be directly estimated by using a prototype filter, and other bands can be obtained through modulating the prototype filter. In each band, the corresponding portion of the spectrum for the wideband signal was down-converted to baseband and then low-pass filtered. This algorithm can therefore capture the dynamic nature of wideband spectrum by using low sampling rates. Unfortunately, due to the parallel structure of the filter bank, the implementation of this algorithm requires a large number of RF components.

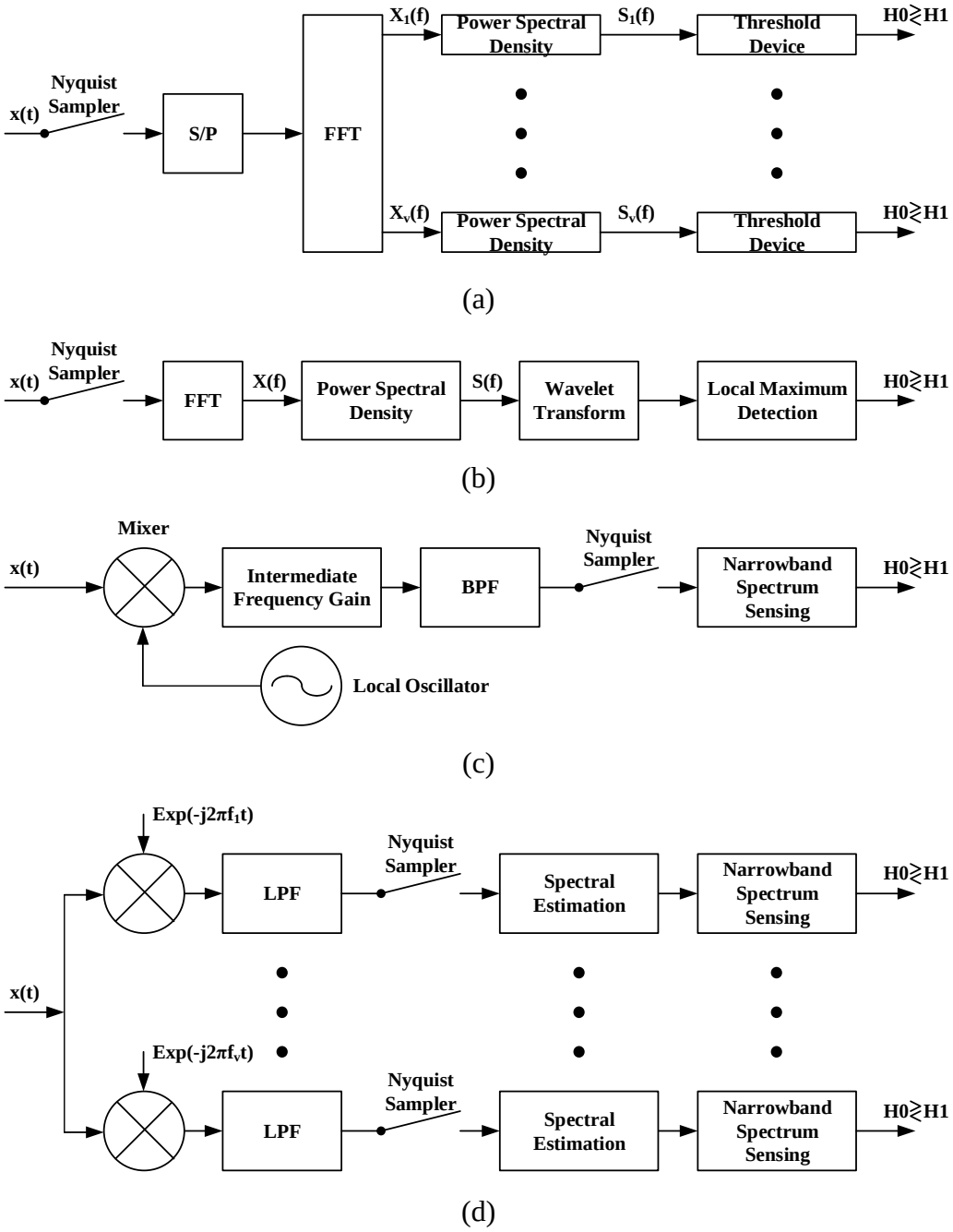


Figure 3.1: Block diagrams for Nyquist wideband sensing algorithms of (a) multiband joint detection, (b) wavelet detection, (c) sweep-tune detection, and (d) filter-band detection.

Due to the drawbacks of high sampling rate or high implementation complexity in Nyquist systems, sub-Nyquist approaches are drawing more and more attention in both academia and

industry. Sub-Nyquist wideband sensing refers to the procedure of acquiring wideband signals using sampling rates lower than the Nyquist rate and detecting spectral opportunities using these partial measurements. Two important types of sub-Nyquist wideband sensing are compressive sensing-based wideband sensing and multichannel sub-Nyquist wideband sensing.

Compressive sensing is a technique that can efficiently acquire a signal using relatively few measurements, by which unique representation of the signal can be found based on the signal's sparseness or compressibility in some domain. As the wideband spectrum is inherently sparse due to its low spectrum utilization, compressive sensing becomes a promising candidate to realize wideband spectrum sensing by using sub-Nyquist sampling rates [38]. This technique used fewer samples closer to the information rate, rather than the inverse of the bandwidth, to perform wideband spectrum sensing. After reconstruction of the wideband spectrum, wavelet-based edge detection was used to detect spectral opportunities across wideband spectrum. However, compressive sensing has concentrated on finite-length and discrete-time signals. The analog compressive sensing [39] is proposed with an analog-to-information converter (AIC), which could be a good basis for the above-mentioned algorithms. As shown in Fig. 3.2(a), the AIC-based model consists of a pseudo-random number generator, a mixer, an accumulator, and a low-rate sampler. The pseudo-random number generator produces a discrete-time sequence that demodulates the signal x(t) by a mixer. The accumulator is used to sum the demodulated signal for 1/w s, while its output signal is sampled using a low sampling rate. After that, the sparse signal can be directly reconstructed from partial measurements using compressive sensing algorithms. Unfortunately, it has been identified that the performance of the AIC model can easily be affected by design imperfections or model mismatches.

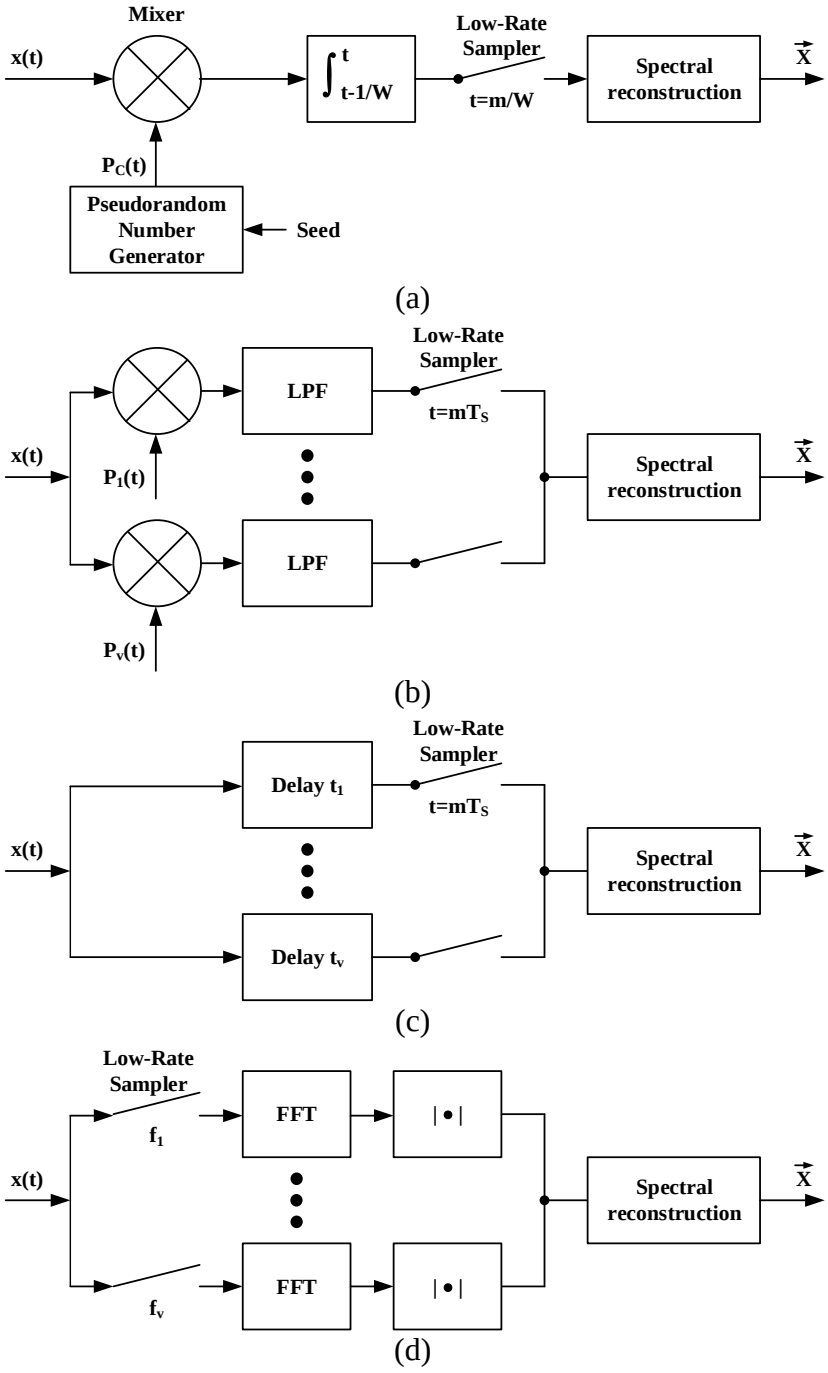


Figure 3.2: Block diagrams for sub-Nyquist wideband sensing algorithms of (a) analog-to-information converter based wideband sensing, (b) modulated wideband converter-based wideband sensing, (c) multi-coset sampling-based wideband sensing, and (d) multi-rate sub-Nyquist sampling-based wideband sensing.

To circumvent model mismatches, a modulated wideband converter (MWC) model was proposed in [40] by modifying the AIC model. The main difference between MWC and AIC is that MWC has multiple sampling channels, with the accumulator in each channel replaced by a general low-pass filter. One significant benefit of introducing a parallel channel structure in Fig. 3.2(b) is that it provides robustness against the noise and model mismatches. In addition, the dimension of the measurement matrix is reduced, making the spectral reconstruction more computationally efficient.

An alternative multichannel sub-Nyquist sampling approach is multi-coset sampling, as shown in Fig. 3.2(c). Multi-coset sampling is equivalent to choosing some samples from a uniform grid, which can be obtained using a sampling rate fs higher than the Nyquist rate. The uniform grid is then divided into blocks of m consecutive samples, and in each block v ($v < m$) samples are retained, while the rest of samples are skipped. Thus, multi-coset sampling is often implemented by using v sampling channels with sampling rate of fs/m, with different sampling channels having different time offsets. To obtain a unique solution for the wideband spectrum from these partial measurements, the sampling pattern should be carefully designed. In [41], some sampling patterns were proved to be valid for unique signal reconstruction. The advantage of the multi-coset approach is that the sampling rate in each channel is m times lower than the Nyquist rate. Moreover, the number of measurements is only (v–m)th of that in the Nyquist sampling case. One drawback of the multi-coset approach is that the channel synchronization should be met such that accurate time offsets between sampling channels are required to satisfy a specific sampling pattern for robust spectral reconstruction.

To relax the multichannel synchronization requirement, an asynchronous multi-rate wideband sensing approach was studied in [42]. In this approach, sub-Nyquist sampling was induced in each sampling channel to wrap the sparse spectrum occupancy map onto itself; the sampling rate can therefore be significantly reduced. By using different sampling rates in different sampling channels as shown in Fig. 3.2(d), the performance of wideband spectrum sensing can be improved. Specifically, in the same observation time, the numbers of samples in multiple sampling channels are chosen as different consecutive prime numbers.

Furthermore, as only the magnitudes of sub-Nyquist spectra are of interest, such a multi-rate wideband sensing approach does not require perfect synchronization between multiple sampling channels, leading to easier implementation.

3.3 An Analog Wavelet-based Wideband Spectrum Sensing

In [38], wavelets are used for detecting edges in the PSD of a wideband channel. Once the edges, which correspond to transitions from an occupied band to an empty band or vice versa, are detected, the powers within bands between two edges are estimated. Using this information and edge positions, the frequency spectrum can be characterized as occupied or empty in a binary fashion. The assumptions made in [38], however, needs to be relaxed for building a practical sensing algorithm. The method proposed in [38] is extended in [43] by using sub-Nyquist sampling. Assuming that the signal spectrum is sparse, sub-Nyquist sampling is used to obtain a coarse spectrum knowledge in an efficient way.

Analog implementation of wavelet-transform based sensing is proposed in [44] for wideband sensing. Multi-resolution spectrum sensing is achieved by changing the basis functions without severe modification to sensing circuitry as shown in Fig. 3.3. The basis function is changed by adjusting the wavelet's pulse width and carrier frequency. Hence, fast sensing is possible by focusing on the frequencies with active transmissions after an initial rough scanning. Fig. 3.3 shows the functional block diagram of the suggested analog multi resolution spectrum sensing (MRSS) technique. Building blocks consists of a wavelet waveform generator, multipliers, and integrators for computing correlation values, and low speed ADCs to digitize the calculated analog

correlation values. Since the MRSS processing is performed in the analog domain, low power and real time operations can be realized. Moreover, a wavelet pulse provides a band pass filtering effect for noisy RF input signals. Thus, image and noise rejection filters are not needed. The square root of S_I and S_Q that are the discrete values represents the spectral density at a specific frequency.

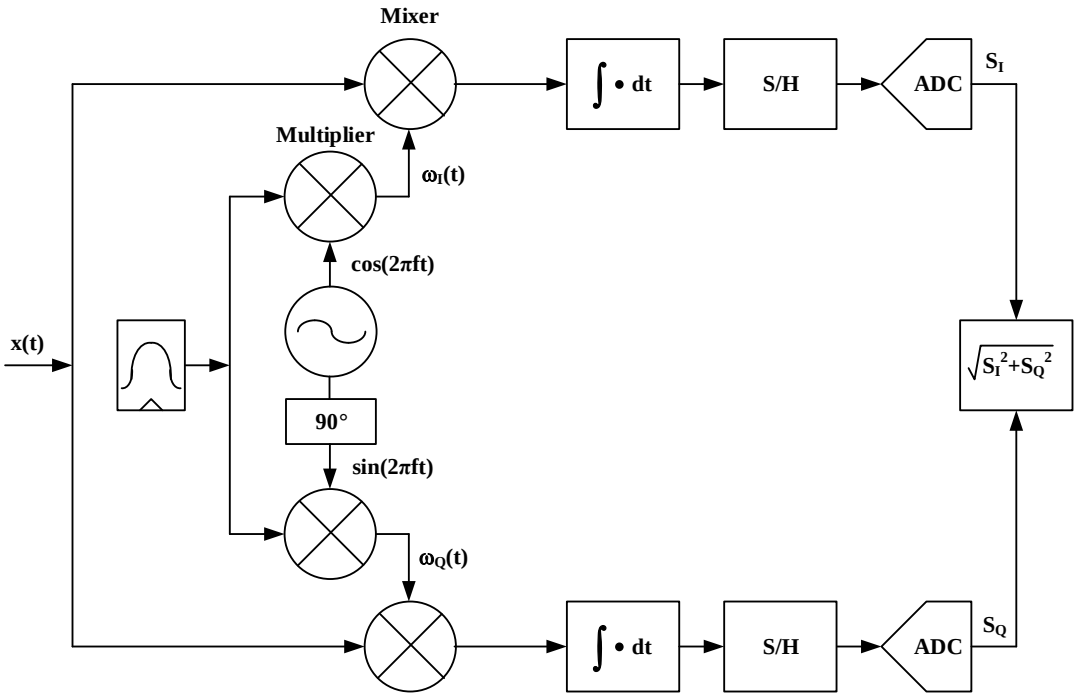


Figure 3.3: Functional block diagram of the analog wavelet-based spectrum sensing

The concept was implemented at VLSI [45, 46]. The basis function was generated by a digital window generator (DWG), which is one of the highest power consuming blocks in the system. The digital window generator (DWG) generates a window waveform with flexible durations. It is composed of a static RAMs (SRAMs), a DAC, and an LP. Changing the RAM address generates the window raw data for the DAC. The LPF reconstructs the digital window signal to an analog form by removing the harmonics of the clock frequencies from the DAC. The DWG consumes 18mW [45].

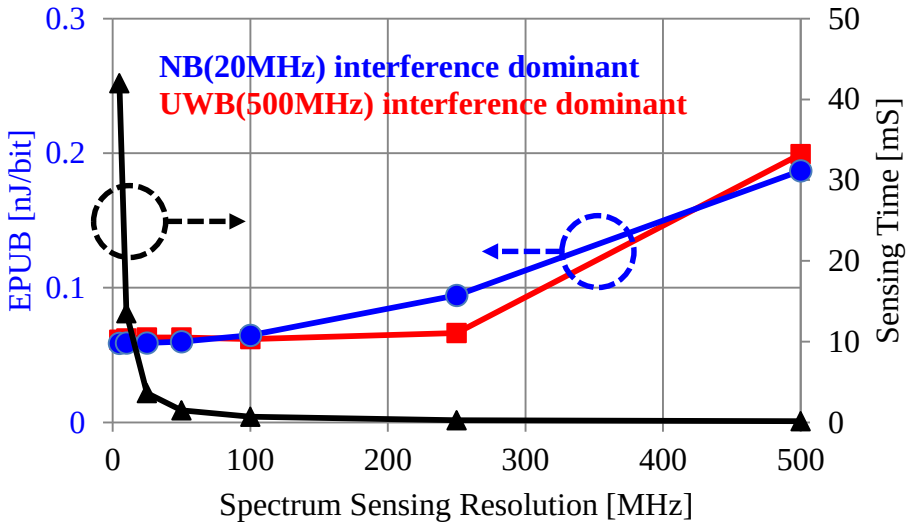
3.4 Spectrum Sensing Resolution for a UWB-based Cognitive Radios

The resolution of the spectrum sensing can be decided by the trade-off between the spectrum utilization efficiency and the total sensing time. The channel utilization efficiency can be defined by EPUB of the cognitive radio. The narrower the resolution, the more efficient the usage of vacant spectrum can be. Narrow resolution, however, increases spectrum sensing time exponentially as shown in Fig. 3.4(a). The sensing time can be calculated as equation (3.1).

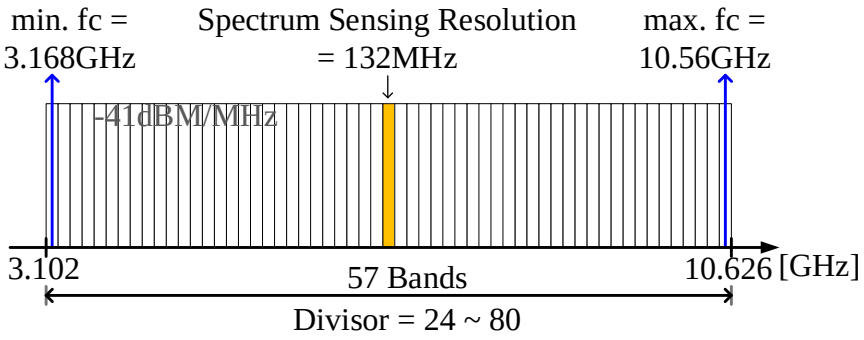
$$t_{sensing} = \left(\frac{f_{end}-f_{start}}{f_{resolution}} + 1\right) \times \left(N_{AVG} \times (t_{window} + t_{sw}) + t_{settling}\right) \quad (3.1)$$

where ($f_{end} - f_{start}$) is the frequency sweep range of the phase locked loop (PLL), fstep is the amount of frequency change in PLL, N_{AVG} is the number of averages at one PLL frequency, t_{window} is the window duration as derived from wavelet window effect, tsw is a timing margin between consecutive windows, and $t_{settling}$ is maximum settling time of the PLL.

Statistical analysis including a narrow 40 MHz BW and a wide 500 MHz BW interferers shows that a 100 MHz resolution is approximately optimal in terms of signal detection and sensing time with 30% spectrum occupancy. The 132MHz resolution is chosen by considering the spectrum usage and the divider depth of the PLL in the UWB band. The minimum frequency of the PLL is 3.168 GHz, and the maximum is 10.56GHz with 132MHz spectrum sensing resolution, which leads to 57 bands in UWB band as shown in Fig. 3.4(b).



(a)



(b)

Figure 3.4: (a) Statistical Analysis in terms of the spectrum utilization efficiency and the sensing time, and (b) the quantized spectrum sensing resolution and maximum and minimum carrier frequency of the PLL.

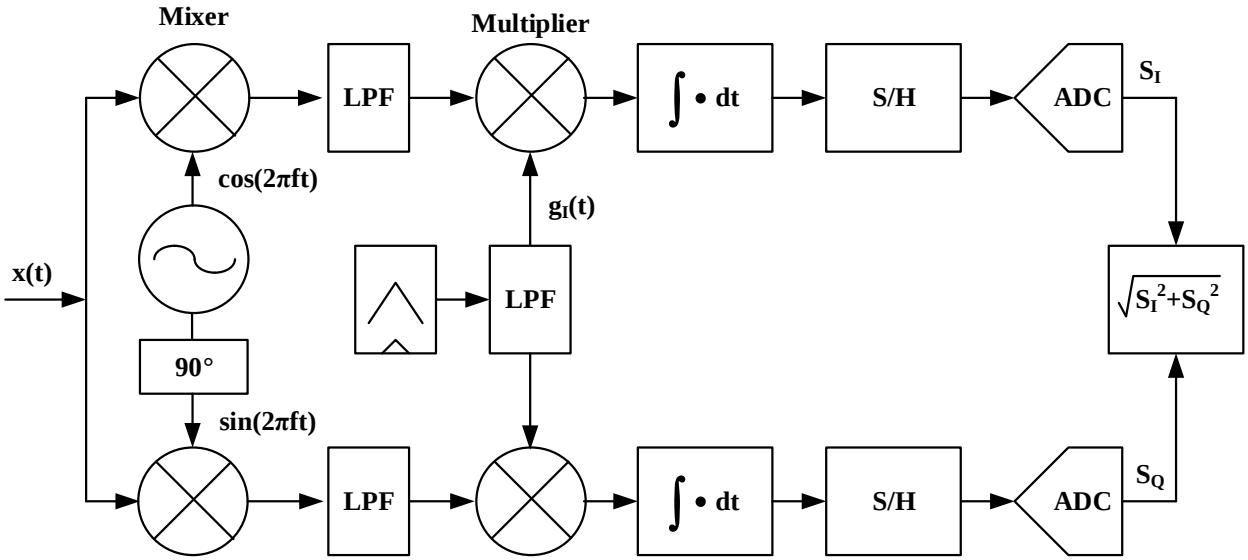


Figure 3.5: Functional block diagram of the modified analog wavelet-based spectrum sensing

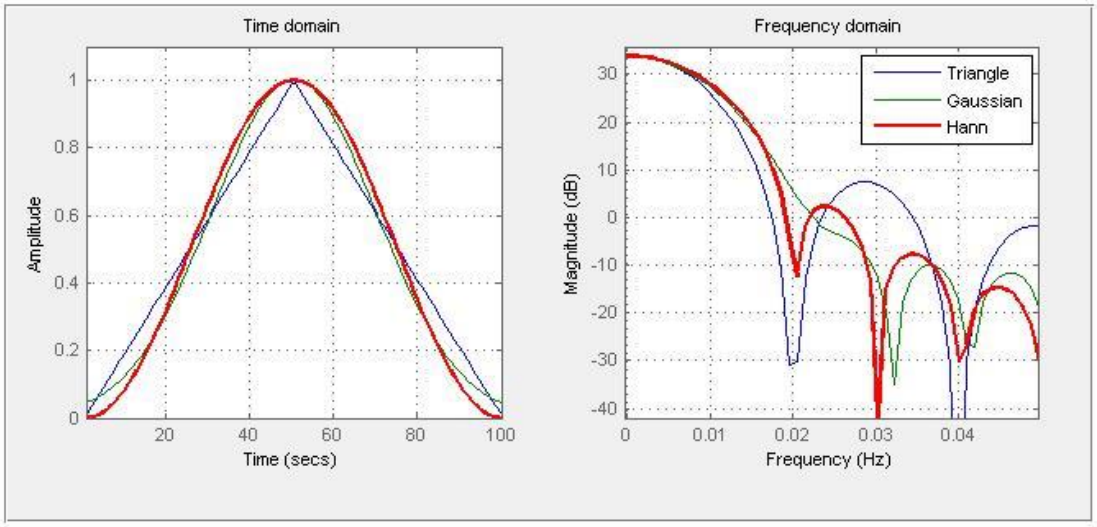
The Analog wavelet-based spectrum sensing is modified to separate local oscillator (LO) path and pulse template wave path as shown in Fig. 3.5. After a down-conversion mixer, a LPF is added to eliminate high frequency output of the mixer. The mathematical function is the exactly same with the previous architecture of [44].

3.5 Triangular waveform generation with Source Follower LPF for Side-lobe Reduction

3.5.1 Characteristics of Triangular Waveform

Power spectral density of the triangular waveform is compared with those of Gaussian and Hann waveforms. Fig. 3.6(a) shows the time-domain waveforms of the triangular, Gaussian, and Hann that have the same cycle. Fig. 3.6(b) shows the power spectral densities of three different

waveforms. Triangular waveform has similar 3dB BW, but the side-lobe leakage of the triangular waveforms is larger than those of Gaussian and Hann. The peak of the triangular waveforms has higher side-lobe peak by 6dB than Hann and by 18dB than Gaussian.



(a) (b)

Figure 3.6: (a) Time domain plot and (b) power spectral densities of triangular, Gaussian, and Hann waveforms.

3.5.2 A Low power Triangular Waveform Generator

A digital circuit technique can be used to generate UWB pulses thorough exciting a delay line [47, 48], or modulating the output of an oscillator [49, 50]. An oscillator-based solution can be advantageous since it requires fewer delay stages than an entire delay line, is highly amenable to bursting multiple pulses back-to-back, and can be used in conjunction with an integrated down-converting receiver. For spectral compliance purposes, pulse shaping may be implemented in the

delay-line approach by using variable current sources at the output of each delay cell [51]; ring oscillator-based designs can instead dynamically activate high-speed drivers in parallel [50].

Unfortunately, static CMOS-based pulse generation has significant DC content that is difficult to remove via pulse shaping alone, making spectral compliance challenging. Previous work has relied on Baluns [48] or off-chip filters [47, 52] to remove this low-frequency content and achieve spectral compliance. This typically requires significant chip or board area, thus increasing the size and cost of the wireless node.

Digital window generator [45, 46] can also provide arbitrary waveforms. However, it requires high power consumption due to a high speed DAC and SRAMs for high data rate application.

Triangular waveform generator using charge pump was introduced in [53] by using charging and discharging linear capacitor. It can achieve tunable bandwidth by controlling charging and discharging time, low power consumption, and precise timing generation. However, the triangle shape is asymmetric due to the reset path delay, and it is not acceptable to generate high frequency waveforms.

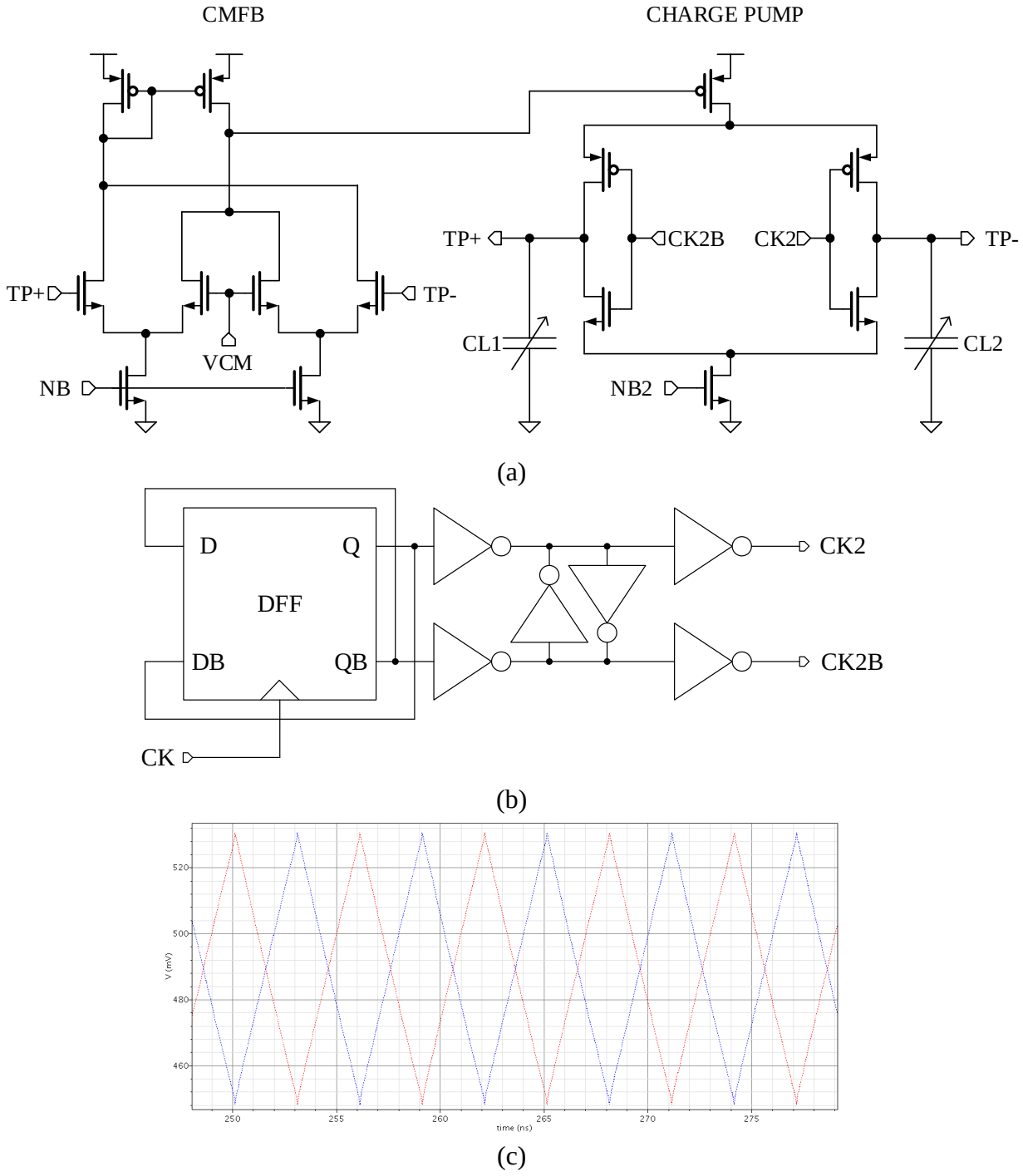


Figure 3.7: (a) Proposed fully differential Charge pump based triangular waveform generator, (b) a 50% duty cycle correction circuit with an edge-triggered differential DFF (Divided by two), and (c) simulated output waveforms of the triangular waveform generator.

Fig. 3.7(a) shows the proposed fully differential triangle waveform generator using charge pump circuits. The charge pump is push pull type, and there are up and down current source. The down current source is connected to the constant bias circuit, and the up current source is controlled by common mode feedback (CMFB) circuit. The triangular wave cycle can be adjusted by input clock (CK2 and CK2B) frequency. The current source current is adjusted with the clock cycle frequency in order to maintain the same peak-to-peak amplitude.

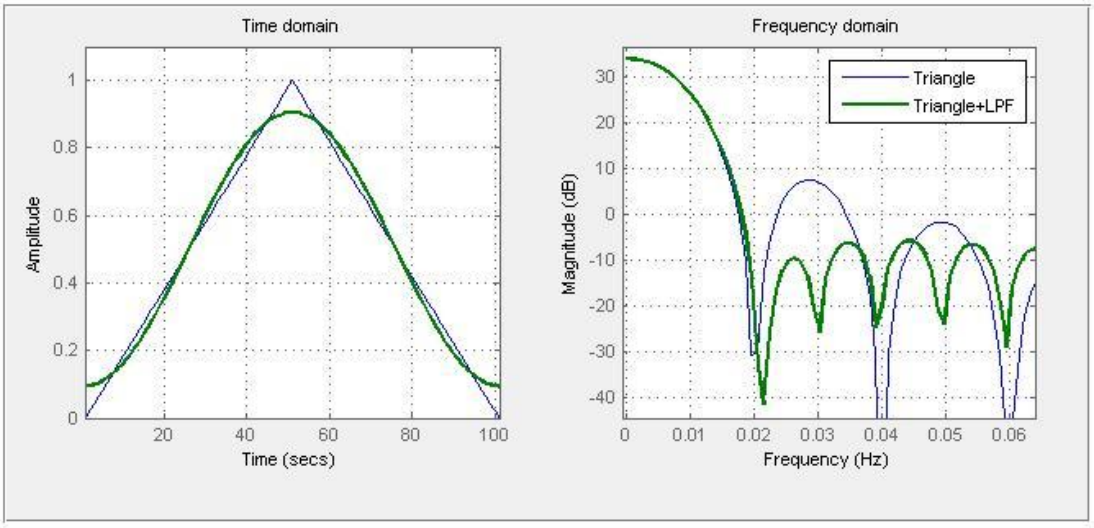
Duty cycle correction circuit of Fig. 3.7(b) is adopted to get 50% clock duty cycle since the duty cycle distortion affects the symmetry of the triangular waveform, which leads to asymmetry in power spectrum density in frequency domain. It also has tunable output capacitor for compensating mismatch on linear capacitor. The capacitor tuning range is +/- 15%, and the accuracy is less than 1% with 5bit control. Fig. 3.7(c) shows the simulated output waveform.

Output common mode level is also tunable within linear output dynamic range of the triangle waveform generator by changing the reference voltage level (VCM) in CMFB circuit.

3.5.3 Side-lobe Reduction of Triangular Waveform

LPF is added to reduce side-lobe peak of the triangular waveform. Butterworth LPF is used due to its flat gain in pass-band in order not to decrease power in useful bandwidth. More than 4^{th} order LPF is enough to reduce the peak of the side-lobe by 40dB. Thus, 4^{th} order Butterworth LPF is adopted by considering circuit complexity and power consumption. The optimal cut-off frequency of the Butterworth LPF is from 2 to 2.5 times of the triangular waveform frequency, which means it allows about +/- 10% variation of the LPF.

Triangular wave form with 4th order Butterworth LPF having cut-off frequency of 2 times of triangular waveform frequency shows Gaussian-shape time-domain waveform as shown in Fig. 3.8(a) and about 40dB side-lobe peak reduction in power spectral density as shown in Fig.3.8(b).



(a) (b)

Figure 3.8: (a) Time domain plot and (b) power spectral densities of the triangular waveform without LPF and with 4th order Butterworth LPF

3.5.4 Modified Source-Follower-based Butterworth LPF

In previous section, LPF can reduce side-lobe peak of the triangular waveform by 40dB. The requirement of the LPF is 4th order Butterworth. Moreover, it allows +/- 10% variation in terms of cut-off frequency.

Source-follower based LPF proposed in [54] is the best option to reduce power consumption compared to other active filters like gm-C filter. It is well known that the source-follower structure uses an internal feedback loop that increases linear range while reducing input MOS overdrive

voltage. This feature is exactly the opposite of any other filtering technique that requires large overdrive for large linearity. This, as a consequence, would increase the current (and power) level for a given transconductance to be performed. On the contrary, the proposed structure improves linearity while reducing overdrive and the current level, and, as a consequence, the power consumption. Moreover, a time constant only depends on the transistors transconductance and on the capacitive load (=C_L/gm). This means that the circuit does not need to drive any resistive load, avoiding having to consume current under signal regime.

Fig. 3.9 shows the modified source-follower-based 4th order Butterworth LPF. Compared to [54], input is connected to the gate of the NMOS of source follower in order to isolate previous stage and the LPF. If input common mode level is properly adjusted, the first stage operation is the exactly same with the unit stage on NMOS source follower LPF in [54].

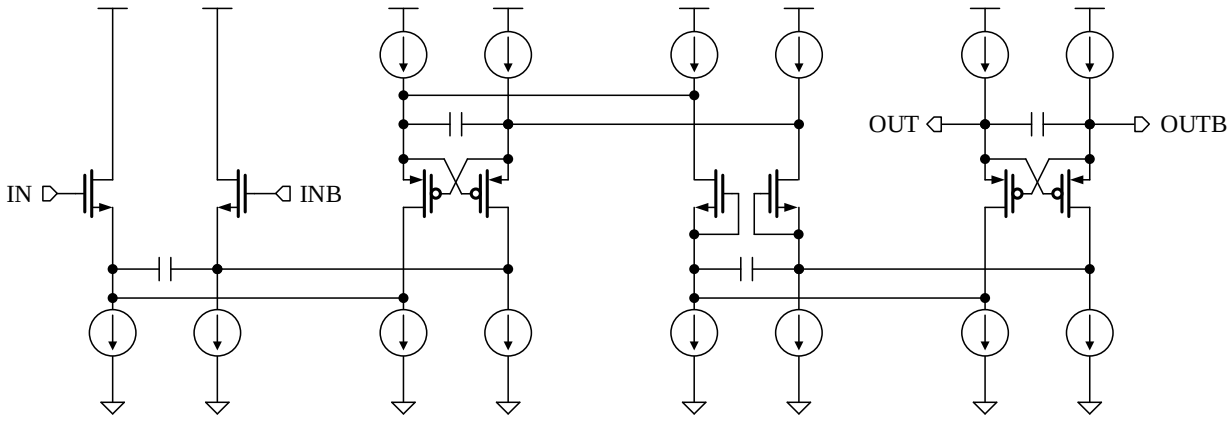
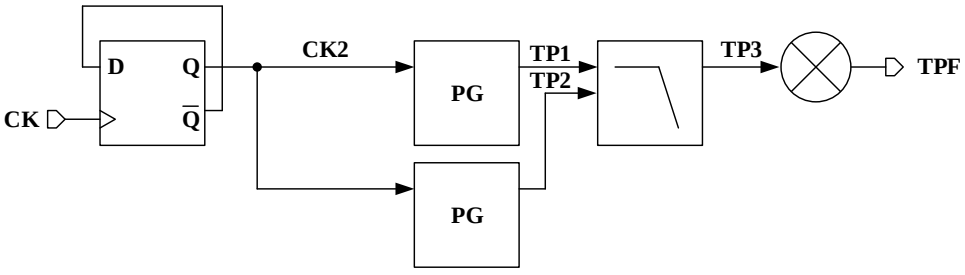


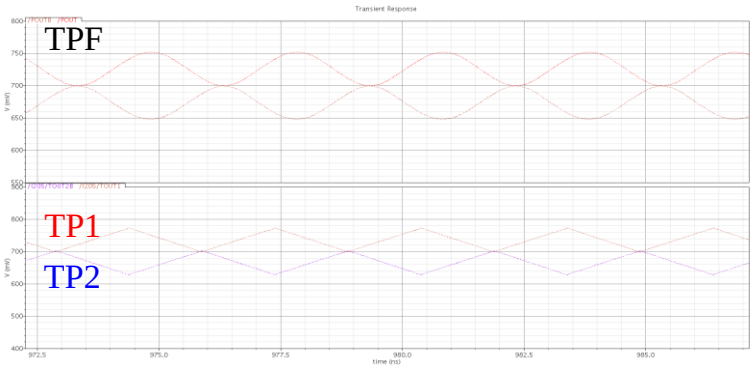
Figure 3.9: Modified source-follower-based 4th order Butterworth LPF.

3.5.5 Proposed Composite Triangular Waveform Generator with LPF

Fig. 3.10(a) shows the composite proposed triangular waveform generator that consists of a DCC, two triangular pulse generators (PG), and a source-follower-based LPF. Two PGs are used to generate differential waveforms. In spectrum sensing mode, the output wave forms are multiplied with the down-converted input signals that needs to be sensed. The multiplier is fully differential type to reduce leakage between two input ports, so the wavelet should be differential one. Even if each PG generates fully differential signal but the crossing point is the middle level of the wavelet peak-to-peak. If two PGs are used, the common mode level can be controlled independently. Thus, final waveforms after LPF can be represented as shown in Fig. 3.10(b).



(a)



(b)

Figure 3.10: (a) Proposed composite triangular waveform generator with LPF and (b) its output waveforms.

Dummy cell is attached at the other differential output that is not connected to LPF in order to compensate difference on load capacitance of the PG.

3.6 Dual-Resolution Spectrum Sensing

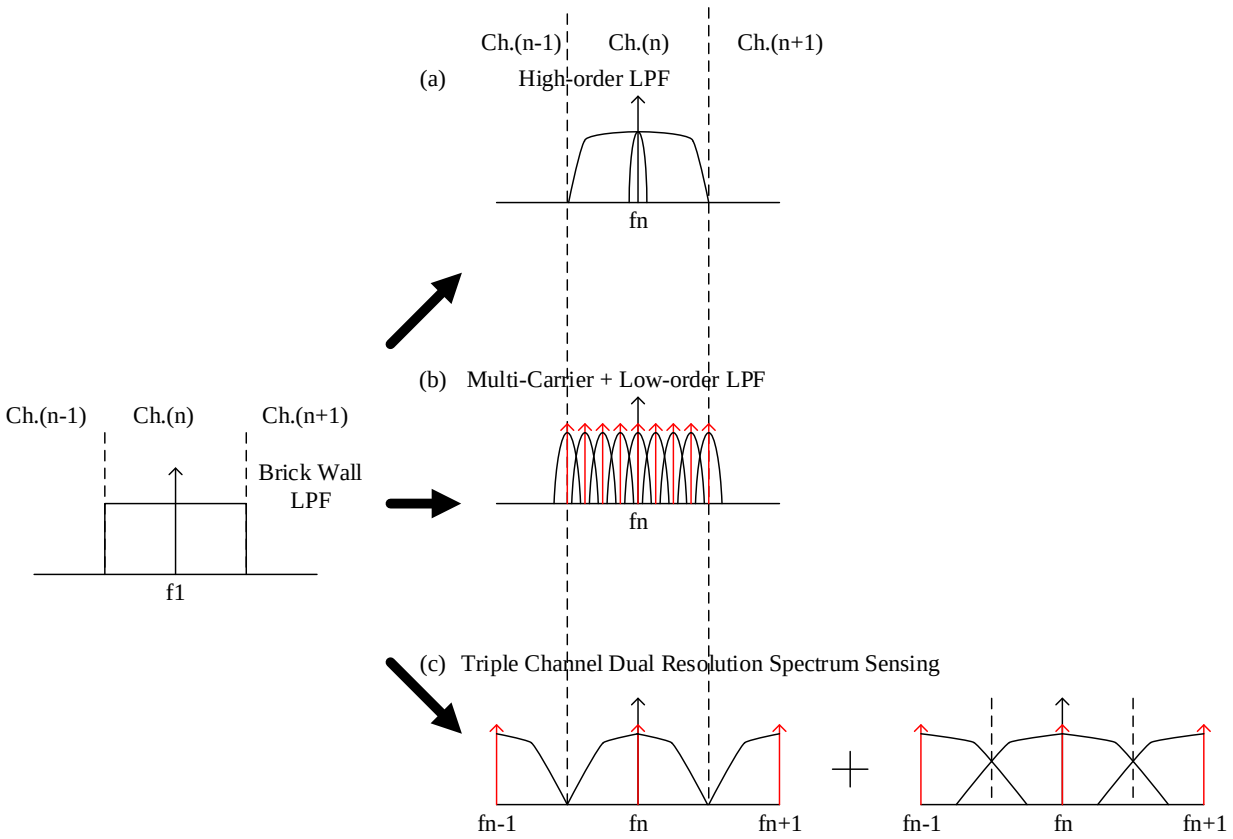


Figure 3.11: Methods to make brick wall BPF with (a) one carrier with a high-order LPF, (b) multi-carriers with a low-order narrow-BW LPF, and (c) Triple carrier with a tunable dual resolution LPF.

In analog wavelet spectrum sensing, the PLL output frequency is mixed with input RF signals, and the RF signal is down-converted to DC in direct conversion. The down-converted signals go through LPFs with defined channel BW. Thus, the whole process is tunable BPF operation by changing the PLL frequency and LPF BW. However, LPF roll-off is not an ideal brick-wall shape, so it is difficult to sense signals that are located at the boundary of each quantized channel.

An Extremely higher order LPF as shown in Fig. 3.11(a) can provide the similar performance of the ideal brick-wall filter, but it requires large area and high power consumption. Multi-carrier in a channel with low-order narrow-BW LPF can also perform the brick-wall filter as shown in Fig. 3.11(b), but PLL power consumption is increased to generate multiple fractional frequencies in a channel, and it takes a long time to sense spectrum in a channel due to PLL settling time for multiple carriers.

Triple-channel dual-resolution spectrum sensing is proposed in order to sense interferers even with low power consumption and channel spacing as shown in Fig. 3.11(c). Tunable LPFs can be done with analog correlation having a multiplier and an integrator in an analog wavelet-based spectrum sensing. The basis function of the wavelet is defined by pulse shape, pulse width, and carrier frequency, which offers active band pass filter operation with variable BW.

Fig. 3.12 shows the proposed dual-resolution analog wavelet-based spectrum sensing blocks. During the spectrum sensing mode, three carriers are generated on each different channel. There is 1/1.5 divider cell at the receiver chain of RX clock. First, the divider ratio is set by 1.5, and spectrum sensing is performed. The null-to-null BW is the same with channel BW. If there are narrow interferes at the boundary of the adjacent channels, it is hard to check the interferer signals. In dual-resolution operation, the sensing is performed again on the same channel with different divider ratio as 1 divisor. Then, the BW of the analog correlation LPF is increased by 50%. The

wider bandwidth can check the signals at the boundaries. Two composite information gives wideband and narrow band interferers' information efficiently without requiring large power consumption as other methods. Three PLLs increase power consumption, but it can reduce sensing time roughly by 1/3. Moreover, one PLL can do this operation by changing the carrier frequency linearly with 3 times longer sensing time.

LPF cut-off frequency of the waveform generator is changed according to input frequency by changing capacitor and current source value.

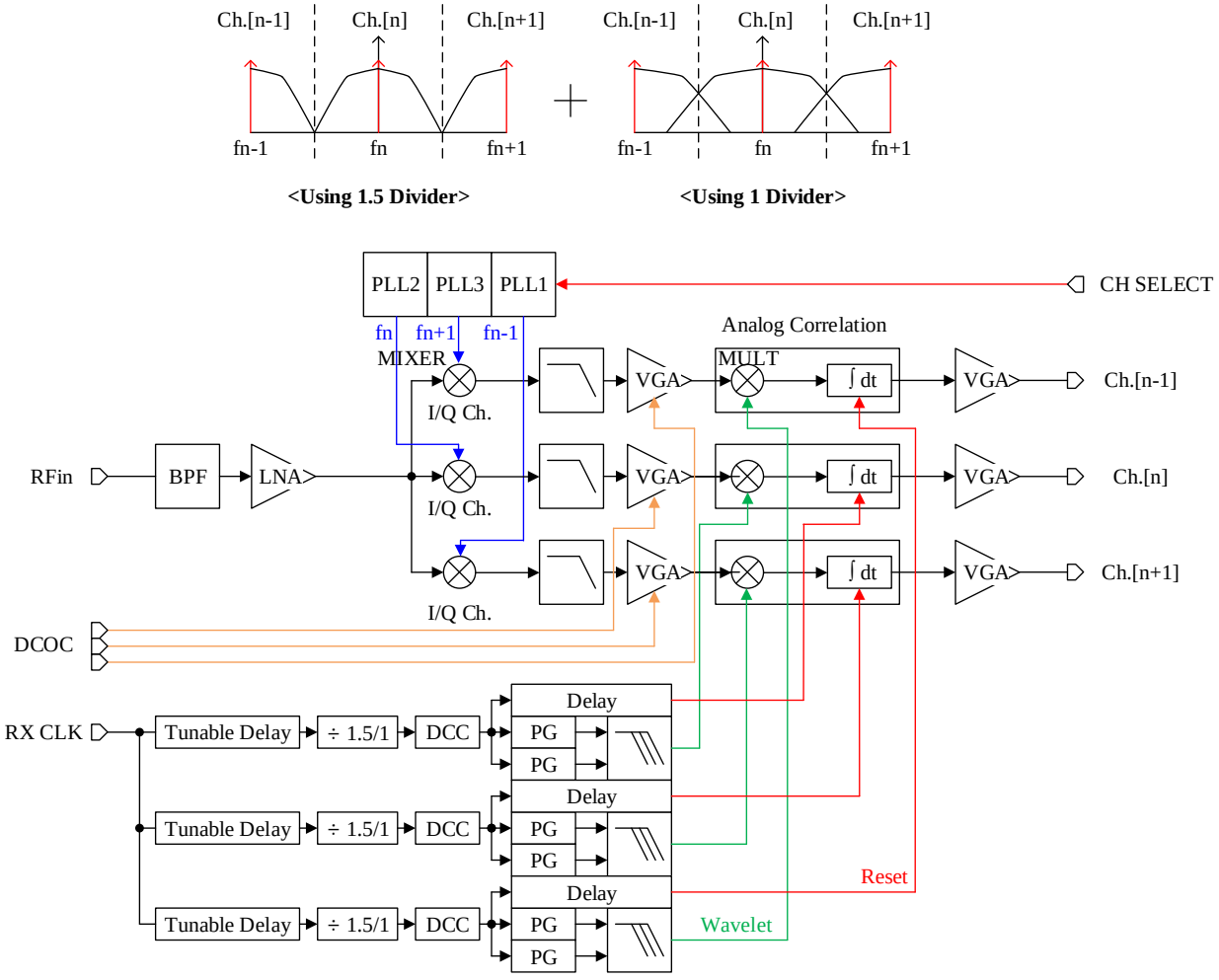


Figure 3.12: Proposed dual-resolution analog wavelet-based spectrum sensing

3.7 Measurement Results

The test chip was fabricated with 1V 65nm CMOS technology. The active area of the triangular wavelet generator with LPF is $0.11\times0.07mm^2$.

Fig. 3.13 shows the time-domain wavelet and spectrogram of the proposed triangular waveform generator with LPF. The RX clock frequency is 99MHz for spectrum sensing. It goes through DCC to get 50% duty cycle. In mode 0, the divider ratio is set by 1.5, and input clock frequency of the waveform generator is 33MHz. It can be referred to 132MHz null-to-null BW. Spectrogram shows that the third harmonic is lower than the fundamental tone by 45dB. For reference, ideal triangular waveform has 19dB difference between fundamental and third harmonic frequencies. It proves the side-lobe peak of the proposed waveform is reduced by 26dB. In mode 1, division ratio is set by 1, and the input frequency of the waveform generator is 49.5MHz. The null-to-null frequency is 198MHz. The third harmonic is lower than the fundamental tone by 43dB.

Fig. 3.14(a) shows the case that a narrow band interfere is located at the center of channel. The output of the analog correlation is shown in Fig. 3.14(b). For Mode 1 and Mode 0, there are finite value at the end of each cycle, which gives information that there is signals in the channel. Fig. 3.14(c) shows the case that a narrow interferer is located at the boundary of the channel. The output value of the analog correlation is below noise threshold for Mode 0, but the output value is over threshold for Mode 1 as shown in Fig. 3.14(d). For wideband interferers, analog correlation gives finite value over noise threshold for Mode 1 and Mode 0 since interferer BW is larger than spectrum sensing resolution as shown in Fig. 3.15. The DC power consumption of the triangular wave form generator is 75μW. Load capacitor value is programmable to get the same amplitude for Mode 0 and Mode 1. The DC power consumption of the LPF is 800μW, and the BW is

programmed by changing the capacitive load for Mode 0 and Mode 1. The capacitor is MOM type passive device.

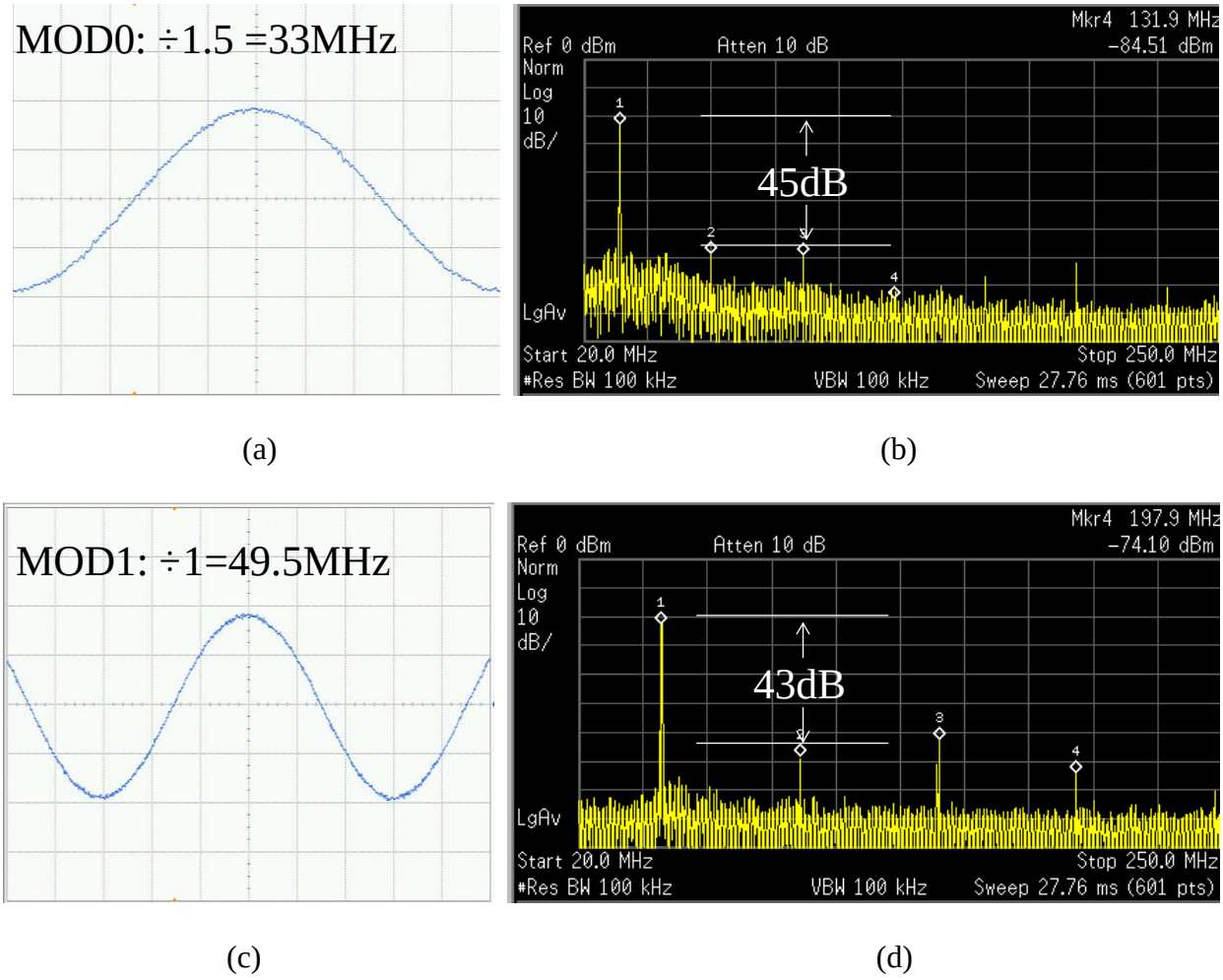
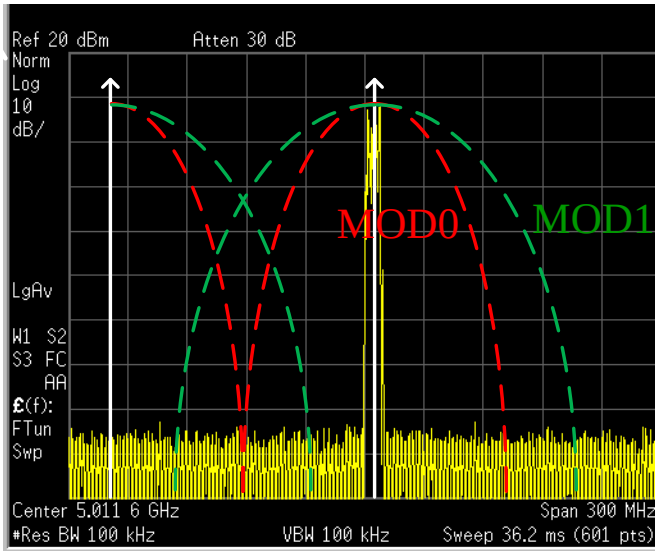
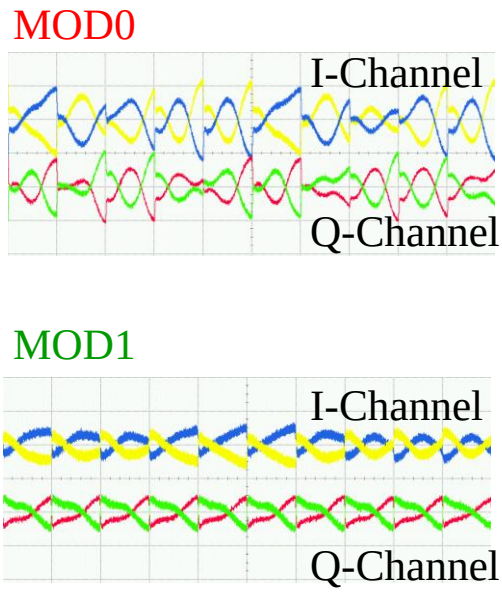


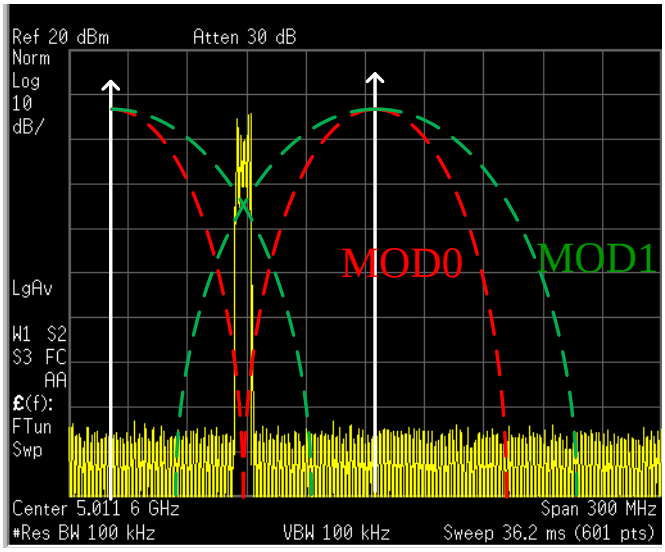
Figure 3.13: (a) time-domain wavelet and (b) spectrogram for MOD0 and (c) time-domain wavelet and (d) spectrogram for MOD1 of the proposed triangular waveform generator with LPF



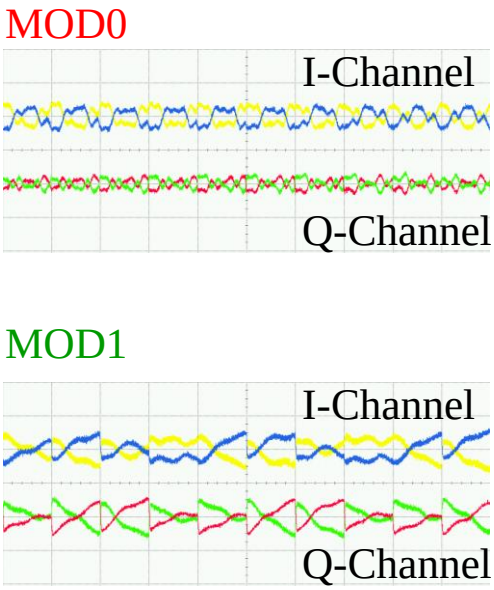
(a)



(b)

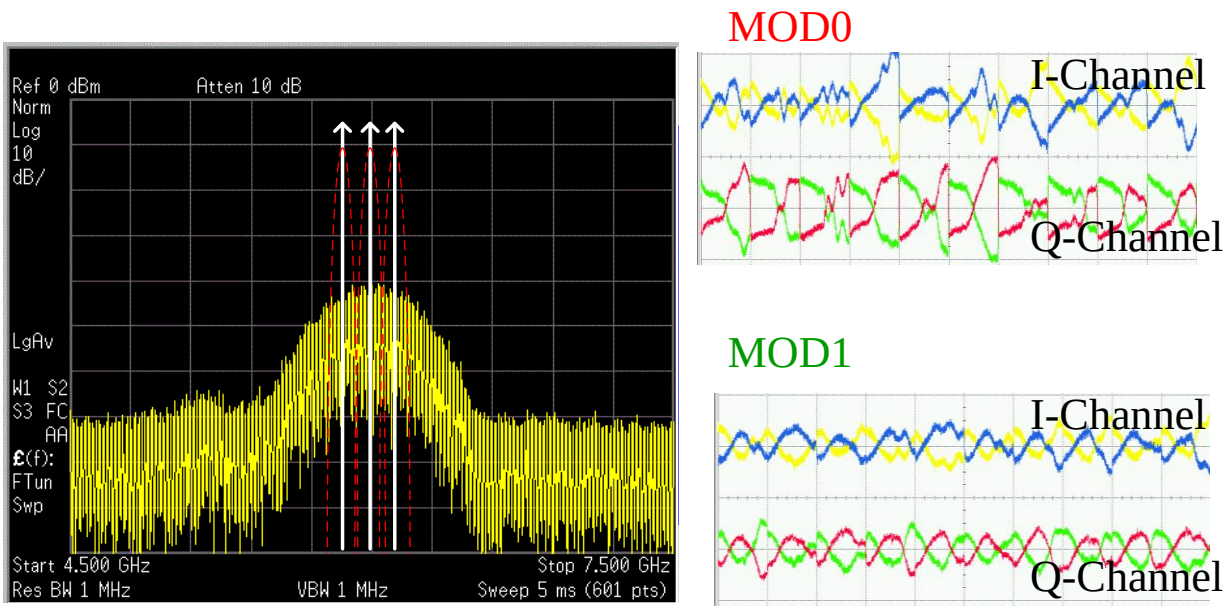


(c)



(d)

Figure 3.14: Dual-resolution analog wavelet-based spectrum sensing for narrow band interferer (a, b) at the center of the channel and (c, d) at the boundary of the channel



(a) (b)

Figure 3.15: Dual-resolution analog wavelet-based spectrum sensing for wideband interferer

3.8 Conclusion

Triangular wavelet generator with LPF was fabricated with 1V 65nm CMOS technology. Source-follower-based LPF reduces third harmonic tone by 40dB compared to fundamental tone in order to get small stop-band ripple for spectrum sensing. Dual-resolution spectrum sensing can detect narrow band interferers even at the channel boundaries. The DC power consumption of the generator is 950μW. The active area is 0.08mm^2. Modified LPF is tunable with the variation of current source and load capacitor value. The noise of the LPF is 42nV/√Hz at 1MHz for mode 0.

Chapter 4. A 3-11GHz Low-Power Integer-N QPLL

4.1 Wideband QPLL for UWB-based Cognitive Radio

The frequency synthesizer of the cognitive UWB should provide 3.1-10.6GHz lock range to accommodate higher capacity and data rates. Meanwhile, the phase noise requirement of the PLL for the impulse radio (IR) UWB is less stringent compared to that of the conventional narrowband radios. Moreover, an integer-N PLL can be used due to wide channel spacing of UWB. Thus, the integer-N PLL using a ring VCO can be adopted due to wide tuning range property, multiphase output, low power consumption, and small area.

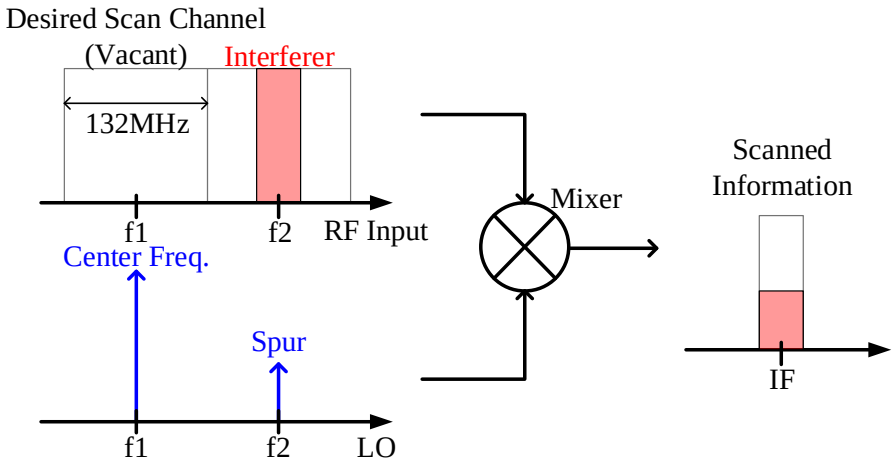
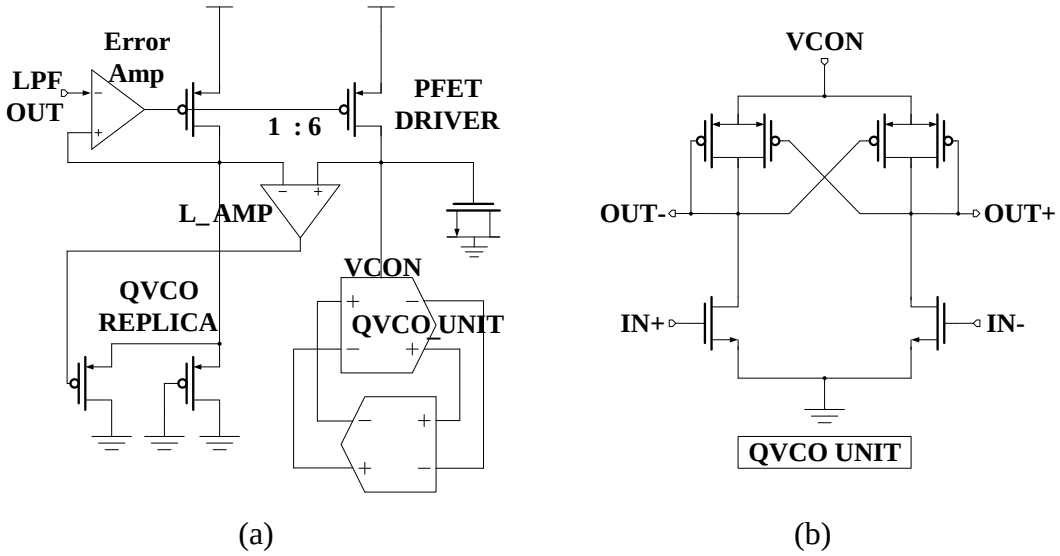


Figure 4.1: Reference spur issue in wavelet-based spectrum sensing.

The spurs of the PLL affects the spectrum sensing since the spurs convert neighbor channel information to the current scanning channel information after a mixer block as shown in Fig. 4.1. It is challenging to achieve low reference spur in wide lock range PLL due to high VCO gain, which is even worse when the wide PLL loop BW is required to get fast settling time and to suppress phase noise of the VCO.

4.2 Two-stage Linear Tuning Differential QVCO

Fig. 4.2 shows the proposed two stage ring oscillator. The QVCO unit includes an NMOS transconductance (gm,n) pair, a PMOS cross-coupled load pair, and a PMOS diode pair for the best power-consumption. The diode-connected and cross-coupled PMOS pair provides linear resistance, which enables linear tuning range with supply voltage (VCON) variation. The maximum output frequency can be set by $g_{m,n}/2\pi CL$, where CL is the load capacitance. The output frequency is tuned by regulated supply of the QVCO (VCON). The resulting QVCO gain is 23GHz/V, which is highly linear with the VCON tuning from 0.4V to 0.9V. The replica bias technique is applied to avoid power supply sensitivity peak issue. Small signal impedance of the replica circuit is set to 1/6 of the QVCO impedance. The replica is designed to track similar I-V characteristics as the ring oscillator with the regulator output voltage variation. The QVCO current can be mimicked by appropriately sized diode-connected PMOS transistor. The impedance mismatch between QVCO and the replica trimmed by source follower PMOS with gate voltage feedback control through the L_AMP having 40dB low frequency gain and 100kHz of 3dB BW. The output 3dB BW of the regulator varies from 22MHz to 40MHz according to output frequency since non-linear small signal impedance variation of the QVCO.



(a) (b)

Figure 4.2: (a) The proposed supply regulated two stage differential QVCO, and (b) the QVCO unit cell.

The LDO consists of the error amplifier and pass transistor. The error amplifier shown in Fig. 4.3(a) is a commonly used architecture since it has high gain and wide output dynamic range. However, when the input common mode level approaches 0.9V (for a 1V supply voltage), the VDS of the input NMOS pair falls into the triode region because of the finite output impedance of the current source. Fig. 4.3(b) shows the proposed error amplifier. The D_AMP maintains the drain voltage of the input NMOS pairs at VREF, 0.8V. Even if the common source node of the error amplifier does not follow input common mode due to finite output impedance of the current source, D_AMP helps input transistor to be in saturation region and enables to get high gain for wide input dynamic range as shown in Fig. 4.3(c). The transconductance of the input NMOS is enhanced due to increased VDS, and output impedance of output PMOS is decreased due to the same reason. The increase of the transconductance compensates the decrease of the output impedance. Thus, in Fig. 4.3(d), the proposed error amplifier has similar low frequency gain and enhancement on 3dB

BW by 4MHz compared to the conventional error amplifier of Fig. 4.3(a) with the same load. The D_AMP has 330MHz 3dB BW, 10dB low frequency gain, and 120µW power consumption.

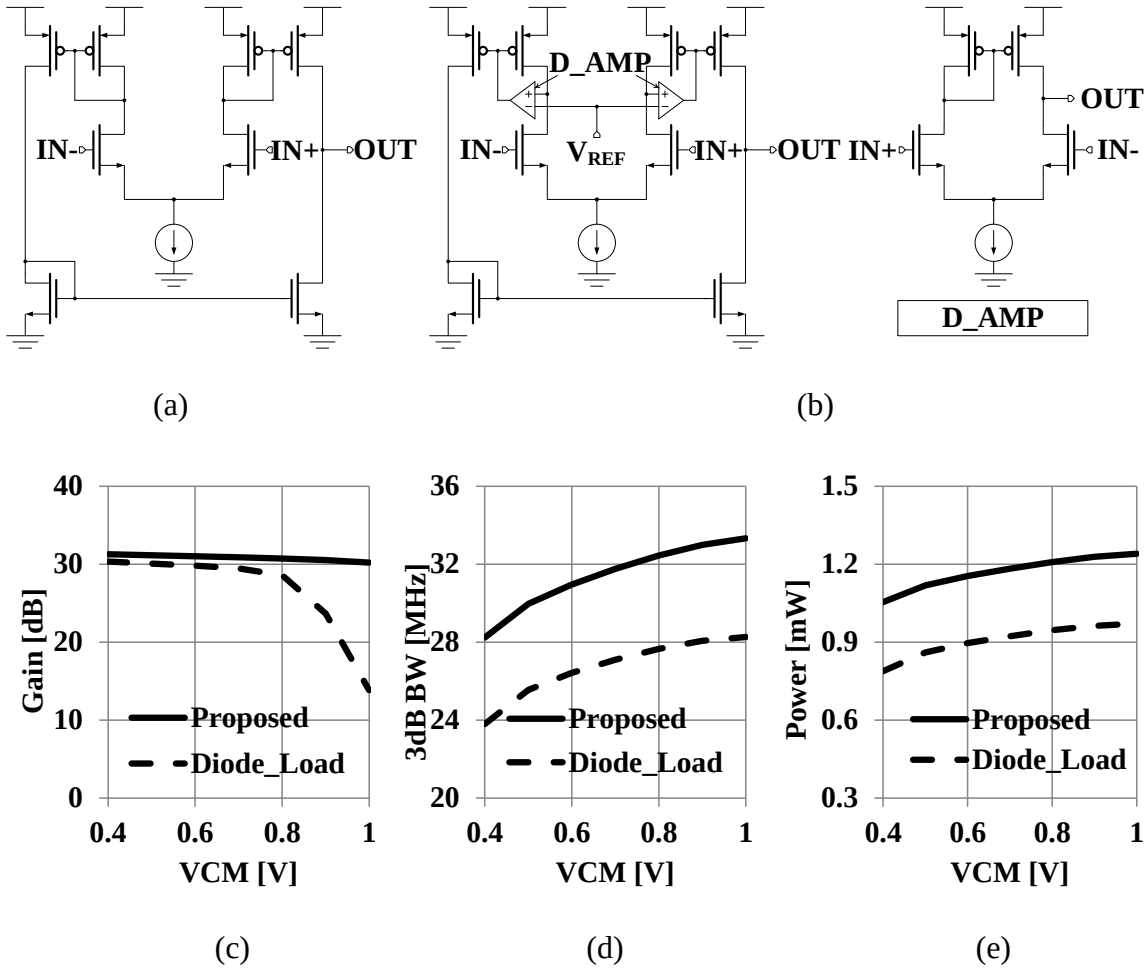


Figure 4.3: (a) The conventional dioded connected PMOS load error amplifier, (b) the proposed error amplifier with enhanced gm technique, and comparion in terms of (c) gain, (d) 3dB BW, and (e) power consumption with input common mode level (VCM).

4.3 Digital Calibration for Charge Pump Mismatch

The proposed type II charge-pump-based QPLL with total fourth order for cognitive UWB is shown in Fig. 4.4. Input reference clock (CKREF) is 66MHz, loop BW is 3.3MHz, and the third order LPF is used to attenuate the reference spur. The divider path provides 57 sub-bands carrier frequency. It includes a 2-divider at first stage and a truly modular programmable divider with 2/3-divider-cells. They are implemented with TSPC logic for low power consumption. The lock detector (LD) enables the digital calibration for the charge pump mismatch. The counter-based dual LD circuit with long-term and short-term can detect PLL lock status quickly and correctly.

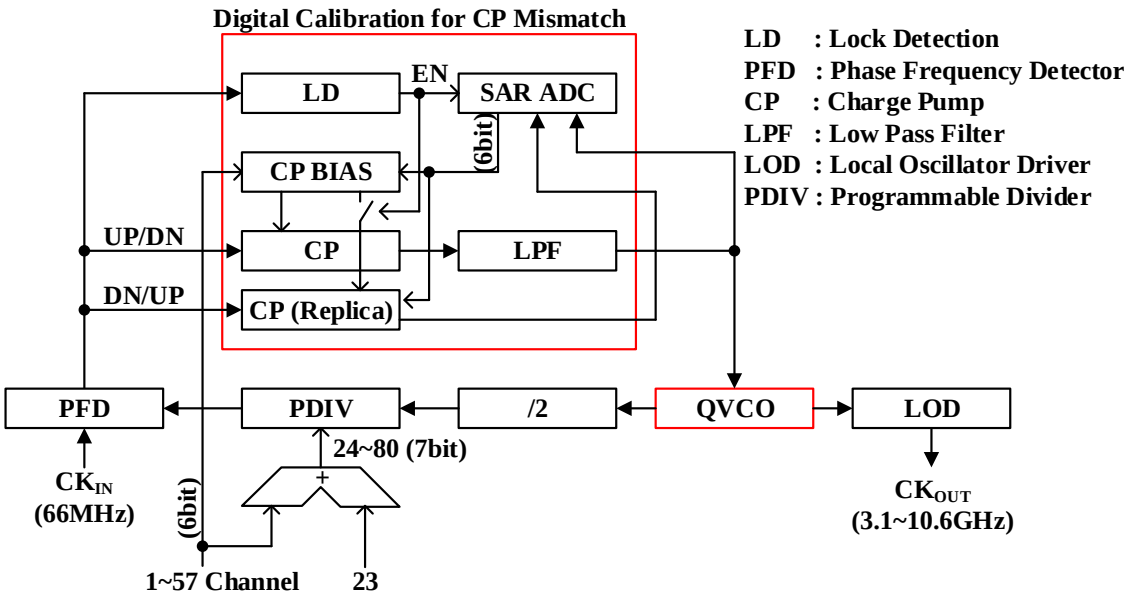


Figure 4.4: The proposed QPLL Architecture with digital calibration for CP.

Less than 1% CP up (Iup) / down (Idn) current mismatch is required with the 23GHz/V VCO gain and 3.3MHz PLL loop bandwidth for the below -60dBc spur level. Moreover, the wide dynamic output range of the CP aggravates the mismatch issue to provide 3-11GHz lock range with deep submicron technology. The proposed QPLL uses digital calibration for the CP. Unlike previous work [55], the proposed method uses background calibration not to change normal operation of main path circuitry. Fig. 4.5 shows the proposed CP with a replica CP. The replica is the same with main CP, but the replica CP receives opposite inputs that UP signal connected to down switch and DN signal connected to up switch. The local feedback with the U_AMP allows the CP to get wide output dynamic range with small Iup / Idn mismatch.

The calibration process is done by a SAR-type ADC after PLL frequency lock, and one step thermometer code is updated after 256 reference clock cycles to mitigate mismatch between the main CP and the replica CP and to avoid offset voltage issue of the comparator in the ADC as shown in Fig. 4.6. Fig. 4.7 describes conceptual operation of the digital calibration for Iup > Idn case. After frequency lock, the stabilized output voltage of the main CP is copied to the replica CP output through a unit gain buffer during pre-charge mode (EVALB). The unit gain buffer is disconnected from the main CP during evaluation period (EVAL). Then, two charge pump outputs have different values after receiving UP/DN signals from PFD because they receive opposite signals. The main CP has stabilized output even with current mismatch since PLL loop generates different pulse width of UP/DN signals, but the replica CP increases the output voltage due to the different PFD pulse width and current mismatch. The different charge amount is accumulated for 128 reference clock cycles and indicates Iup is greater than Idn. The counter turns off one Iup current source switch whose amount is 0.5% of the CP current. The operation is iterated to get < 1% mismatch. The Iup charge pump current can be calibrated by +/- 16% of the nominal current

with 6bit binary control (63bit thermometer code). Mismatch between the main CP and the replica CP is not critical since the mismatch only affects replica CP output voltage level, and the output voltage only indicates calibration direction to SAR ADC that decides which one is bigger than the other. However, current mismatch ratio of Iup to Idn at the replica CP should be the same with that at the main CP. Long channel device is used to reduce different channel length modulation effect between the replica CP and the main CP. Moreover, the same layouts are used for them, and they are located closely to get the same mismatch percentage for Iup and Idn of the replica CP from the main CP.

In addition to the CP mismatch reduction to minimize reference spur, the timing mismatch from PFD is reduced by careful layout and clock buffers. The MOM capacitor is used for the LPF to reduce leakage current. The dual path CP technique is applied to reduce the on-chip LPF area [56].

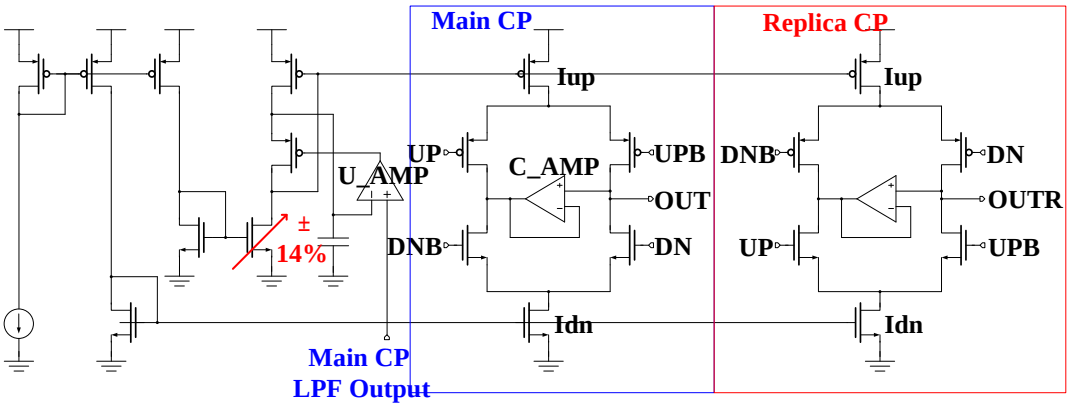


Figure 4.5: The proposed charge pump with the replica.

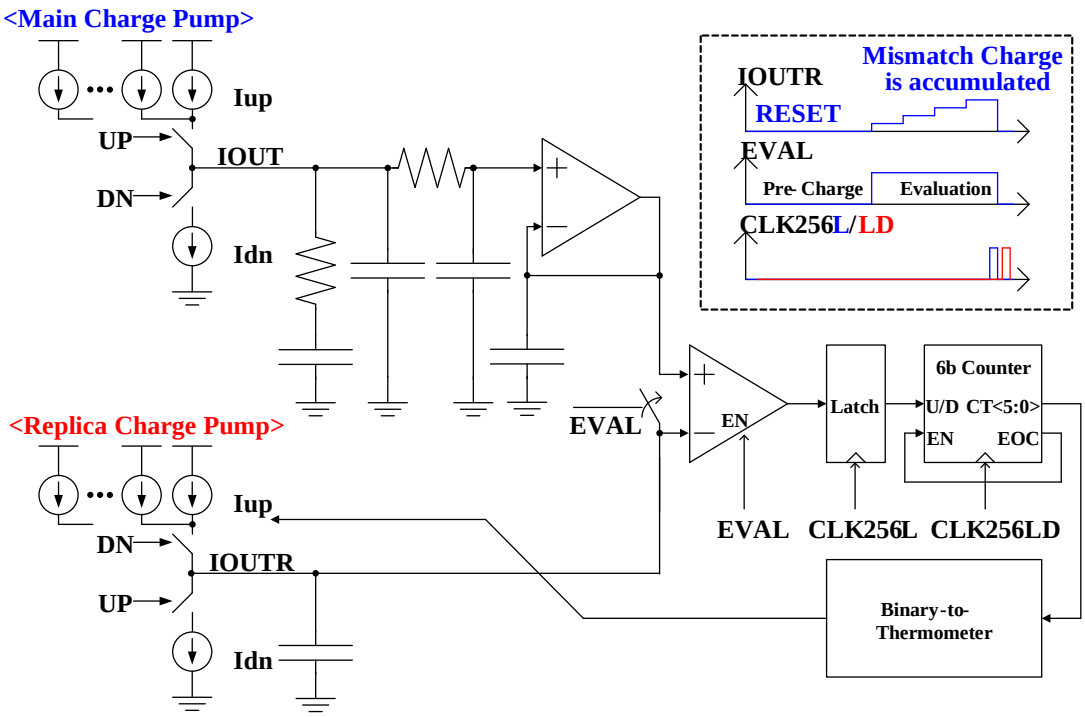


Figure 4.6: The proposed digital calibration for the CP current mismatch.

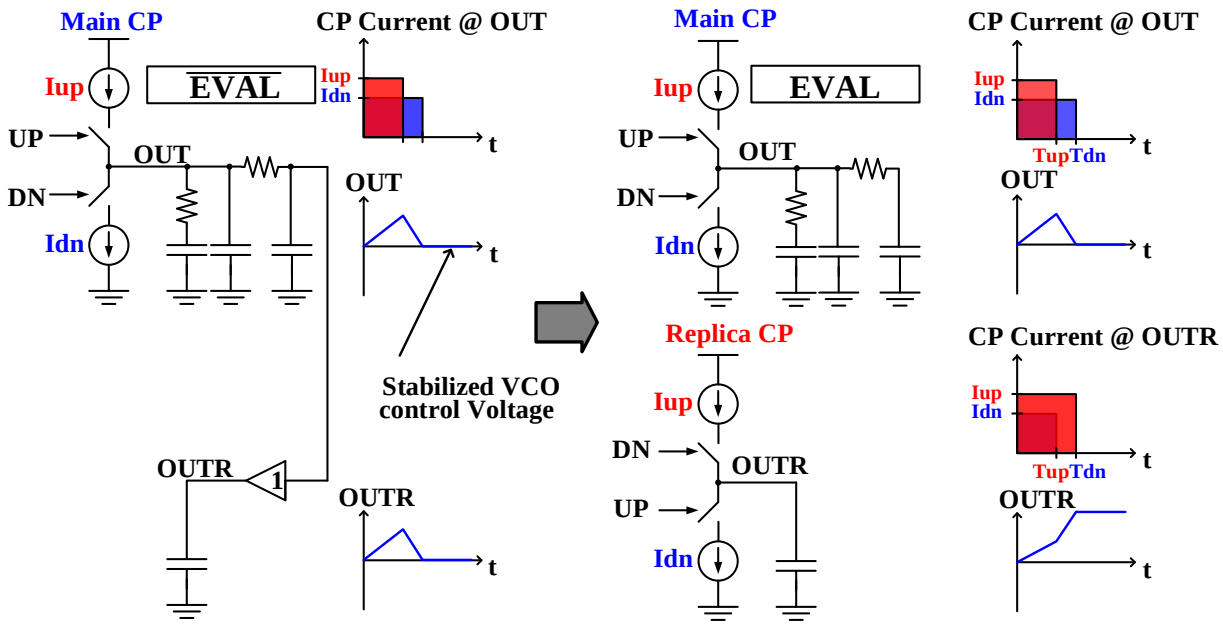


Figure 4.7: Principal operation of the digital cariblation for Iup > Idn case.

4.4 A Wideband Low-Power TSPC Frequency Divider

The high speed frequency divider is one of the key blocks for low power consumption since the output signal of the voltage controlled oscillator (VCO) asserts the input of the divider, so the divider operates at highest chip frequencies. In the PLL path, a 2-divider is placed at the first stage of the divider, and a programmable divider (PDIV) provides from 24 to 80 divisor as shown in Fig. 3.4(b). The frequency range of the PDIV should be wide from 6GHz to several hundred MHz due to wide tuning range VCO of the synthesizer.

The current mode logic (CML) is commonly used for Giga-hertz range applications, but the CML flip-flops suffer from high power consumption [57]. According to the international technology roadmap for semiconductors (ITRS) in Fig.4.8 [58], the intrinsic delay reduction of the MOSFETs enables the CMOS PDIV to achieve Gigahertz range operation and low power consumption with the technology scaling. The true-single-phase-clock (TSPC) PDIVs are used for the CMOS PDIVs due to their simple circuit architecture, compact implementation, and low power consumption [59-62]. Moreover, the single phase- clock operation simplifies clock distribution and layout complexity. However, previous works have focused on high frequency operation only. For wide lock range frequency synthesizer application, leakage current in deep sub-micron CMOS technologies should be addressed since the dynamic nodes of the TSPC flip-flops are susceptible to noise and leakage. As technology scales, the leakage current is increased exponentially as shown in Fig. 4.8.

The conditional leakage compensation technique [63] uses static keeper controlled by the external control signal with static and dynamic modes. However, the keeper degraded high frequency performance of the flip-flop since the keeper reduces the driving capability of the main

flip-flop path. The gated inverting keeper [64] relieves the drawback of the strength contention between the main path driver and the keeper. However, the required size of the stacked NMOS and PMOS keepers increases parasitic capacitance of the main path and clock load capacitance. Moreover, there is still current contention between the main path and the gated inverting keeper during transition time. In addition to the high frequency limitation, the strength ratio of the keeper to the driver limits low frequency operation due to leakage current at the dynamic nodes.

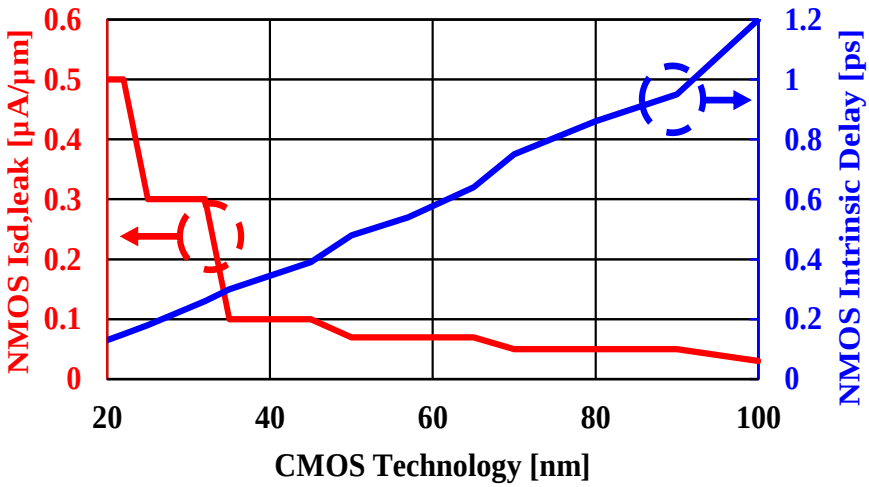


Figure 4.8: Intrinsic delay and sub-threshold source drain leakage current of the NMOS with technology scaling (ITRS2003).

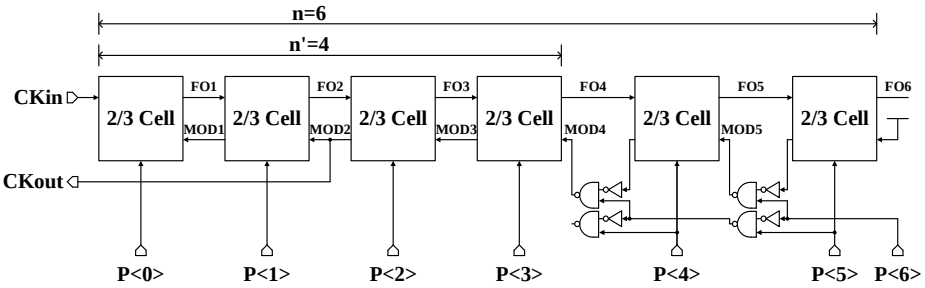
4.4.1 Truly Modular Programmable Divider

Vaucher et al. proposed a modified truly modular PDIV as shown in Fig. 4.9(a). It has cascaded 2/3-divider cells and control logic blocks to extend the division range to any desirable power-of-2 factor [57]. Moreover, this architecture improves maximum operation frequency due to short feedback path. The division ratio is defined by 7bit external control code (P<6:0>) from 16 to 125.

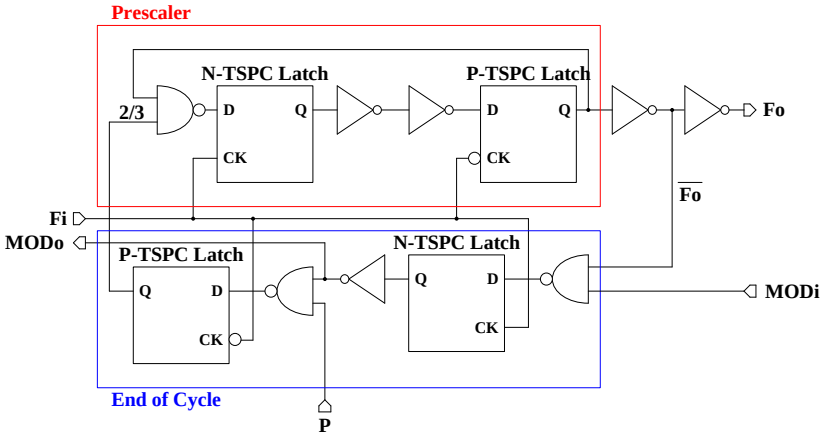
A 2/3-divider cell comprises prescaler logic and end-of cycle logic as shown in Fig. 4.9(b). The prescaler logic divides the input frequency by two or three according to the output of end-of-cycle logic. The 2/3-divider is modified to use TSPC logic without differential output and to minimize logic delay between two consecutive latches. The longest logic delay is an inverter and a NAND gate.

4.4.2 N/P-TSPC Latches with Gated Inverting Keeper

Fig. 4.10 shows the proposed N/P-TSPC latches. The gated inverter technique is employed to compensate for the leakage current at the dynamic nodes [64]. For an N-TSPC latch, PC2 and NC2 are used to control the activation of the inverting keeper (PC1 and NC1). PC2 is connected to CK, but NC2 should be connected to IN since ND1 blocks ND2 with CK, but there is no blocker for PD1 during hold mode (low CK). If IN is low during the hold state of the latch, n1 node is not floating, so the gated inverting keeper is disabled. When the input is high during the hold mode, the leakage current at the node n1 is compensated by the gated inverting keeper. P-TSPC latch operation is the same with N-TSPC latch except clock and input polarity.

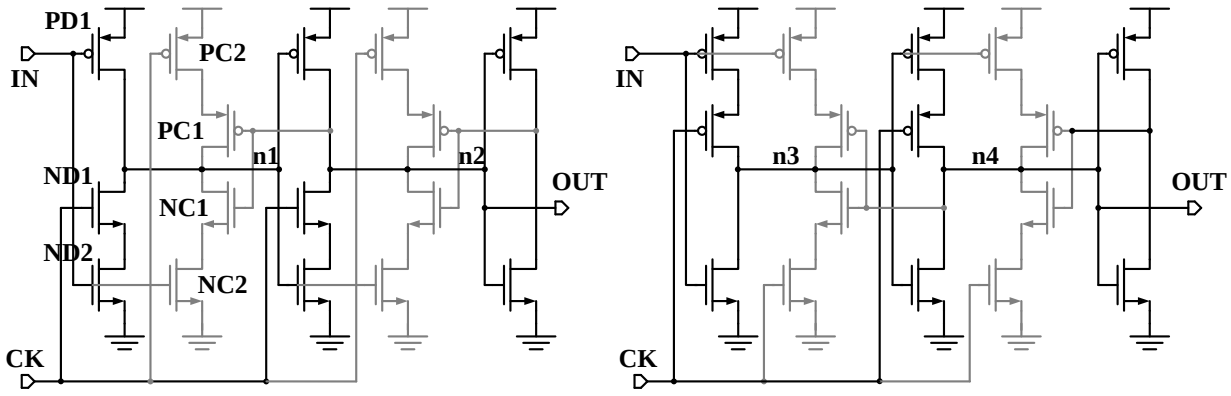


(a)



(b)

Figure 4.9: (a) Fully modular PDIV with extended division range architecture and (b) modified 2/3-divider cell for TSPC latches.

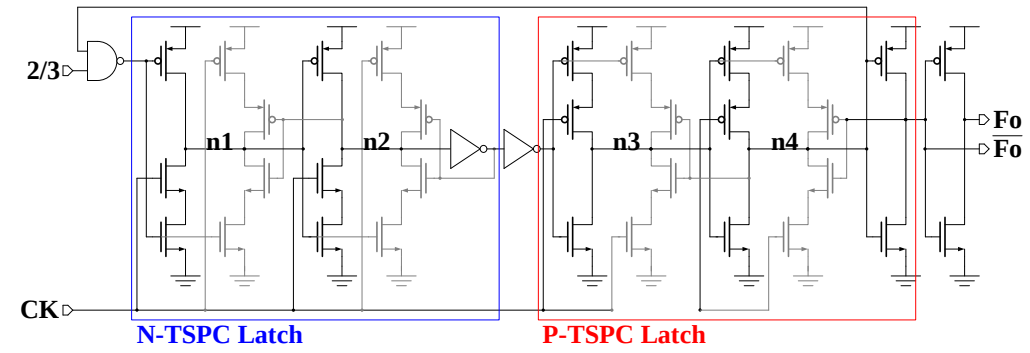


(a) (b)

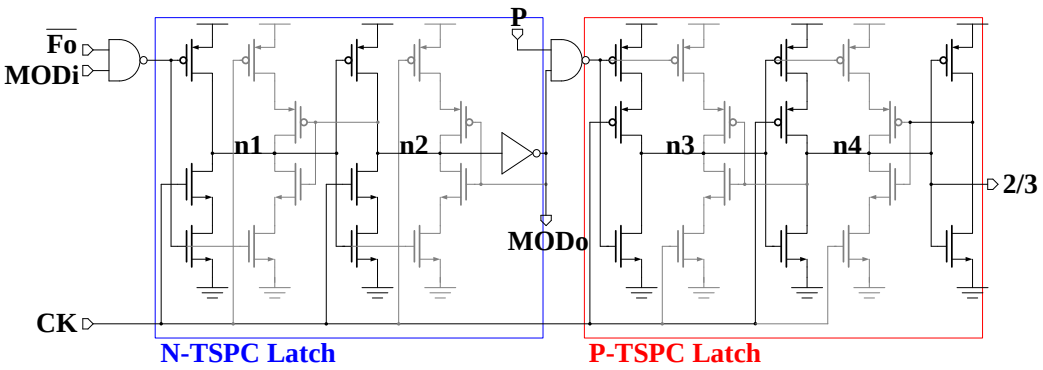
Figure 4.10: (a) N-TSPC and (b) P-TSPC latches with the gated inverter for leakage compensation at dynamic nodes.

Fig. 4.11 shows the prescaler logic and end-of-cycle logic with the proposed N/P-TSPC latches in a 2/3-divider cell. The minimum frequency is defined by the stored charge retention time at the dynamic node. The dynamic nodes are charged or discharged by the leakage current. Fig. 4.12 shows the leakage current effect on the dynamic nodes (n3 and n4) of the prescaler P-TSPC latch without leakage compensation technique. The leakage current starts charging or discharging the dynamic nodes during hold mode. After the voltage level of the node n3 passes the critical level, the voltage level of the node n4 rapidly drops due to VGS increase of the off-state NMOS driver. It affects the output waveform even during hold state. The delay to the critical voltage level of the dynamic nodes can define minimum frequency of the PDIV. Fig. 4.13(a) shows the minimum frequency with the strength ratio of the keeper to the driver. As the strength ratio is increased, the minimum frequency can be decreased since the keeper holds the dynamic nodes strongly.

The maximum frequency can be defined by the total delay including the clock to output delay (tCQ) and the setup time (tSU) of the N/P-TSPC latches, the total logic delay (tLG), and the clock skew (tSK). Fig. 4.13(b) shows the maximum frequency with the strength ratio of the keeper to the driver. During the transition time, there is current contention between the driver and keeper due to finite rising and falling time of the input and the clock even if the keeper is controlled by clock and data. The strength ratio affects tCQ, tSU, and tSK. As the ratio is increased, the maximum operating frequency is reduced. The proposed PDIV uses 0.2 of the strength ratio by considering maximum frequency, minimum frequency, and noise margin for the PDIV to get the operating frequency from 18MHz to 6.8GHz.



(a)



(b)

Figure 4.11: (a) Prescaler logic and (b) end-of-cycle logic with N/P-TSPC latches of the modified 2/3-divider.

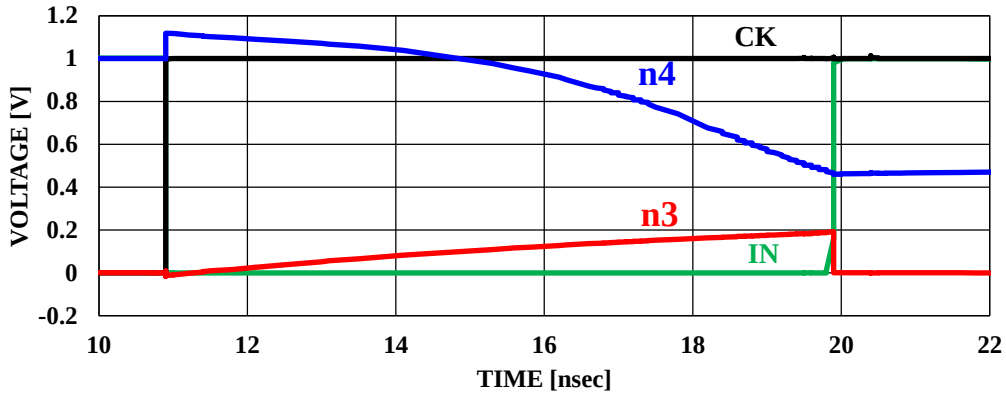
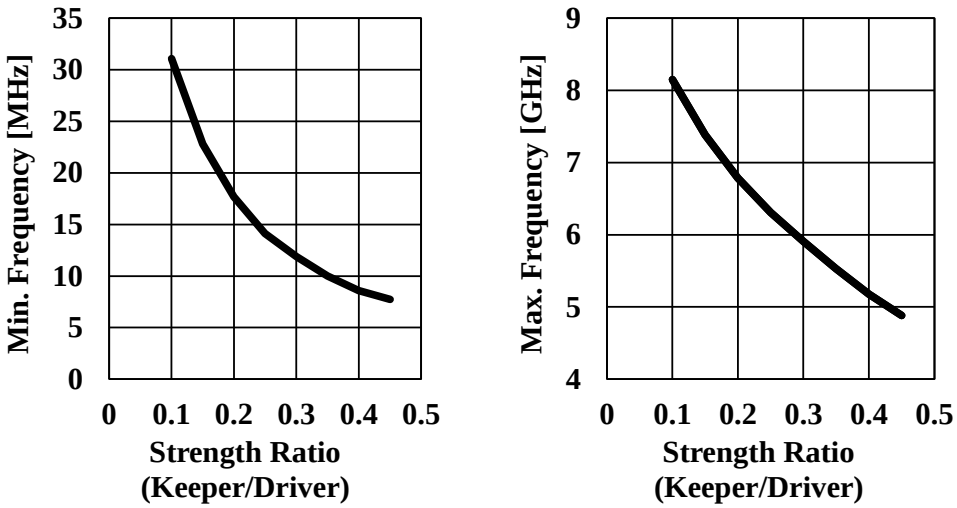


Figure 4.12: Simulated leakage effect on the dynamic nodes of the prescaler P-TSPC latch without compensation technique.



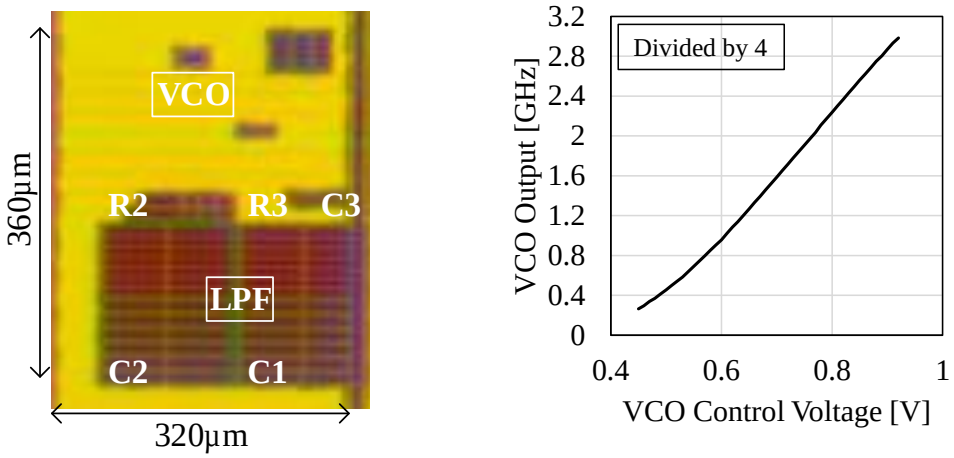
(a) (b)

Figure 4.13: Simulated (a) minimum and (b) maximum operating frequencies with the strength ratio of the keeper to the driver.

4.5 Measurement Results

4.5.1 A 3-11GHz Low-Power Integer-N QPLL with Spur Reduction Technique

The QPLL fabricated in a standard 1V 65nm CMOS process occupies an active area of $0.32\times0.36mm^2$ as shown in Fig. 4.14(a) and consumes 10.4mW at 10.6GHz output. The proposed QVCO and the QPLL are measured with a 4-divider at the output. Fig. 4.14(b) shows measured tuning range of the proposed two stage ring VCO. It demonstrates the ability to cover the full UWB band and a linear VCO gain of 22.5GHz/V.



(a) (b)

Figure 4.14: (a) Chip photo of the proposed QPLL and (b) Measured VCO output tuning range with an 4-divider.

The proposed QPLL output spectrums and phase noise (PN) without and with the digital calibration technique are shown in Fig. 4.15. The reference spur is -44dBc at 66MHz offset frequency without the digital calibration. When the calibration is enabled, the spur level is

attenuated to -59dBc. The PN measurement also shows the reference spur suppression with the calibration. However, the calibration circuitry increases the PN from -108.82dBc/Hz to -105.38dBc/Hz at 1MHz offset frequency due to the added replica charge pump circuitry.

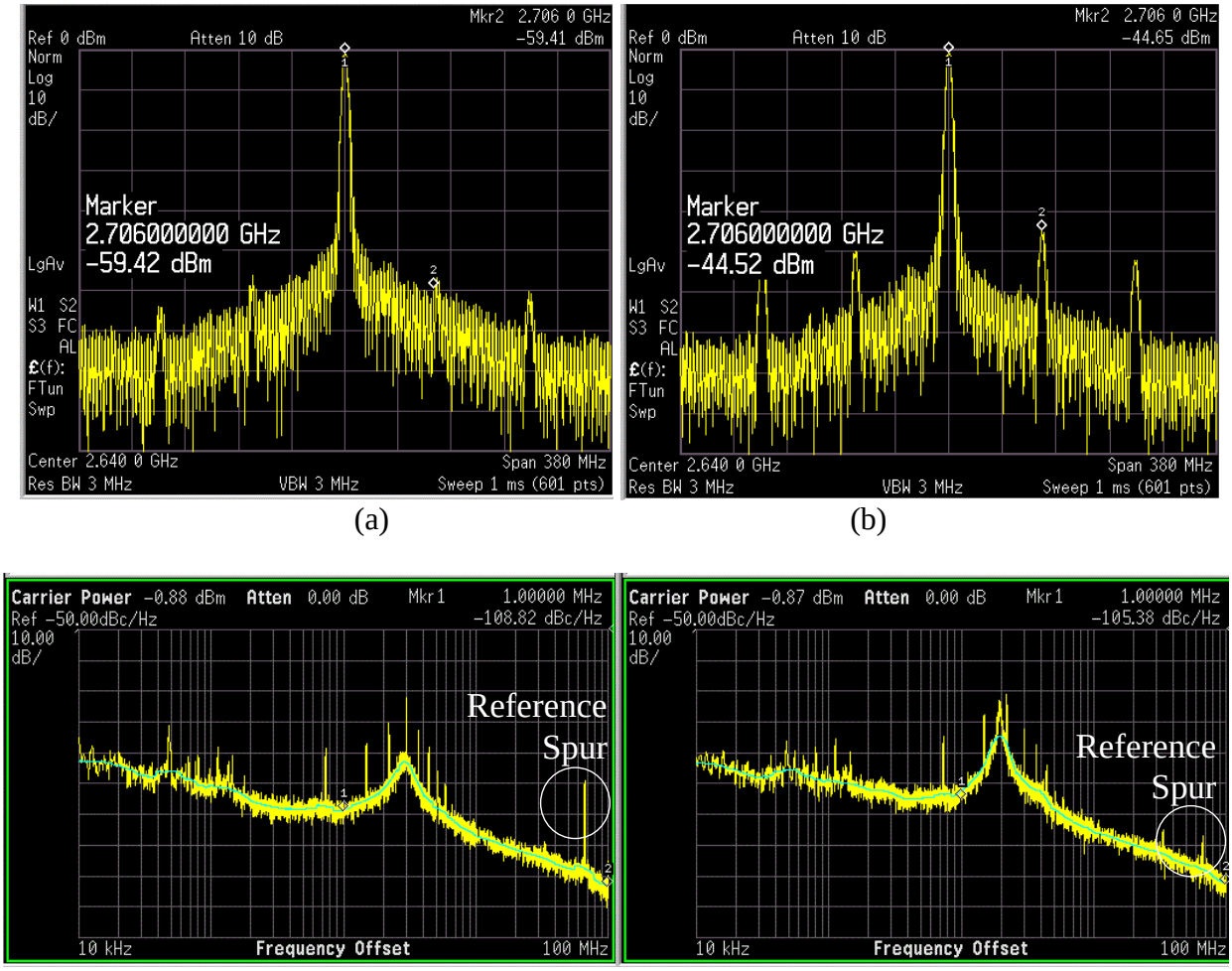


Figure 4.15: Comparison of the measured QPLL output spectrum and phase noise (a,c) without and (b,d) with the digital calibration technique.

Table 4.1 gives the performance summary and comparison with previous works for UWB radio application. The proposed QPLL can only provide full UWB band carrier frequency without SSB

mixers. Moreover, it shows the lowest power consumption, the smallest area, and the smallest reference spur level. The ring VCO deteriorates PN performance compared to LC VCOs. However, the PN is still compatible in IR-UWB application due to large BW of more than 500MHz even if considering the 4-divider effect at the QPLL output (about 12dB PN increase with ideal 4-divider).

Table 4.1: Performance summary and comparison of the proposed QPLL

	JSSC05 [65]	**JSSC06 [66]**	**JSSC07 [67]**	**JSSC08 [68]**	**JSSC09 [69]**	**TVLSI12 [70]**	**This Work**
Technology [nm]	180 (CMOS)	180 (CMOS)	180 (CMOS)	90 (CMOS)	180 (CMOS)	180 (CMOS)	65 (CMOS)
VCO Type	LC	LC	LC	Injection Lock LC	LC	LC	Ring VCO
Carrier Frequency Generation Method	VCO	SSB Mixer	SSB Mixer	SSB Mixer	SSB Mixer	SSB Mixer	VCO
Tuning Range [GHz]	6.336 – 8.976	3.432 – 7.92	6.336 – 10.56	7.656 – 8.712	6.336 – 10.56	3.42 – 10.296	3.168 – 10.56
No. of Bands	6	7	7	3	9	14	57
Reference Freq. [MHz]	528	264	66	528	66	264	66
Loop BW [MHz]	52.8	-	0.754	-	-	-	3.3
Settling Time [nsec]	300	1	-	-	-	1.59	2000
Spur [dBc]	-52	-37	-22	-38	-28	-33	-59
Phase Noise [dBc] (@ 1MHz offset)	-109.6	-116	-103.76	-112	-126.7 (@ 10MHz)	-98	-105.38 (Divided by 4)
Power [mW]	57.6	48	88.5	36	102.6	117	3.7 – 10.4

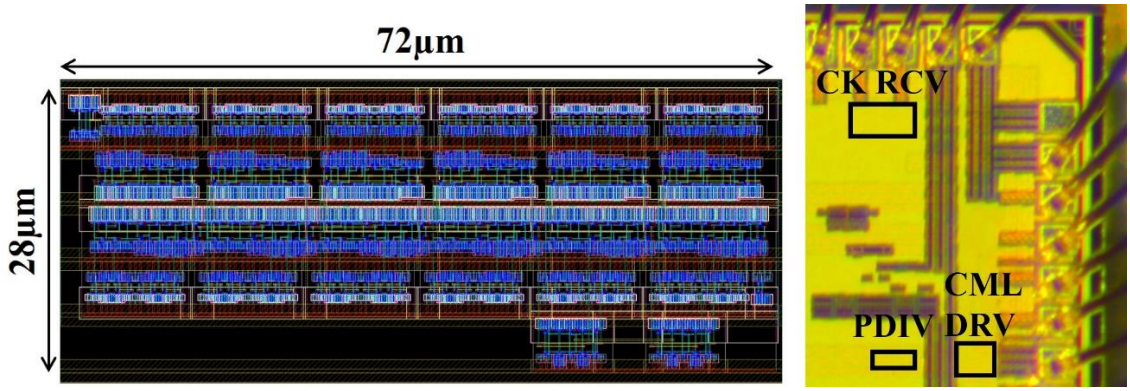
4.5.2 A 0.02-6.5GHz Low-Power TSPC Programmable Frequency Divider

The proposed TSPC PDIV with the gated inverting keeper, fabricated in a standard 1V 65nm CMOS process, occupies an active area of 0.072×0.028 mm^2 as shown in Fig. 4.16(a). Test chip involves a clock receiver, PDIVs, and a CML output driver as shown in Fig. 4.16(b). The test chip has two TSPC PDIVs with and without the gated inverting keepers.

Fig. 4.17 shows TSPC PDIV output waveforms without leakage compensation scheme. The stored data at the dynamic nodes are corrupted by the leakage current, so the output is oscillating regardless of the input frequency and division ratio. Fig. 4.18 (a) and (b) show that the proposed PDIV with the gated inverting keeper can divide input frequency up to 6.5GHz with 24 and 80 division ratio. Moreover, it can divide 20MHz input frequency as shown in Fig. 4.18 (c) and (d). The output waveform from 20MHz input frequency verifies mitigation of the leakage effect on the dynamic nodes by showing the extended stored charge retention time at the dynamic nodes.

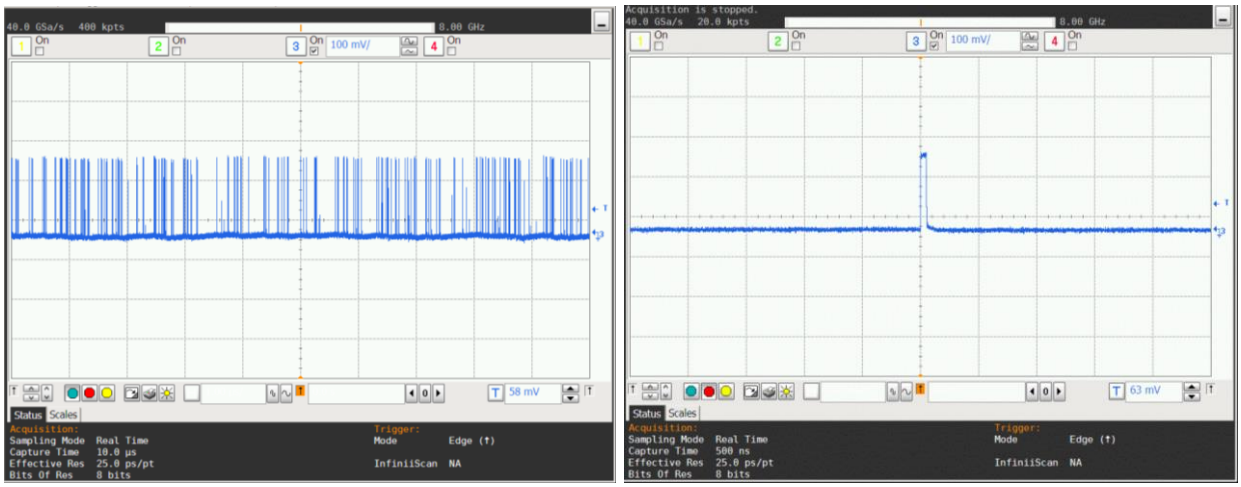
Fig. 4.19(a) shows power consumption of the PDIV with various input frequencies for 1V supply. The maximum power consumption is 1.03mW at 6.5GHz input frequency, which gives 6.31GHz/mW power efficiency. The phase noise of the PDIV is -141.21dBc/Hz at 1MHz offset as shown in Fig. 4.19(b).

Table 4.2 gives the performance summary and comparison with previous works of the TSPC PDIVs. The proposed PDIV achieves the highest power efficiency and the widest dynamic range.



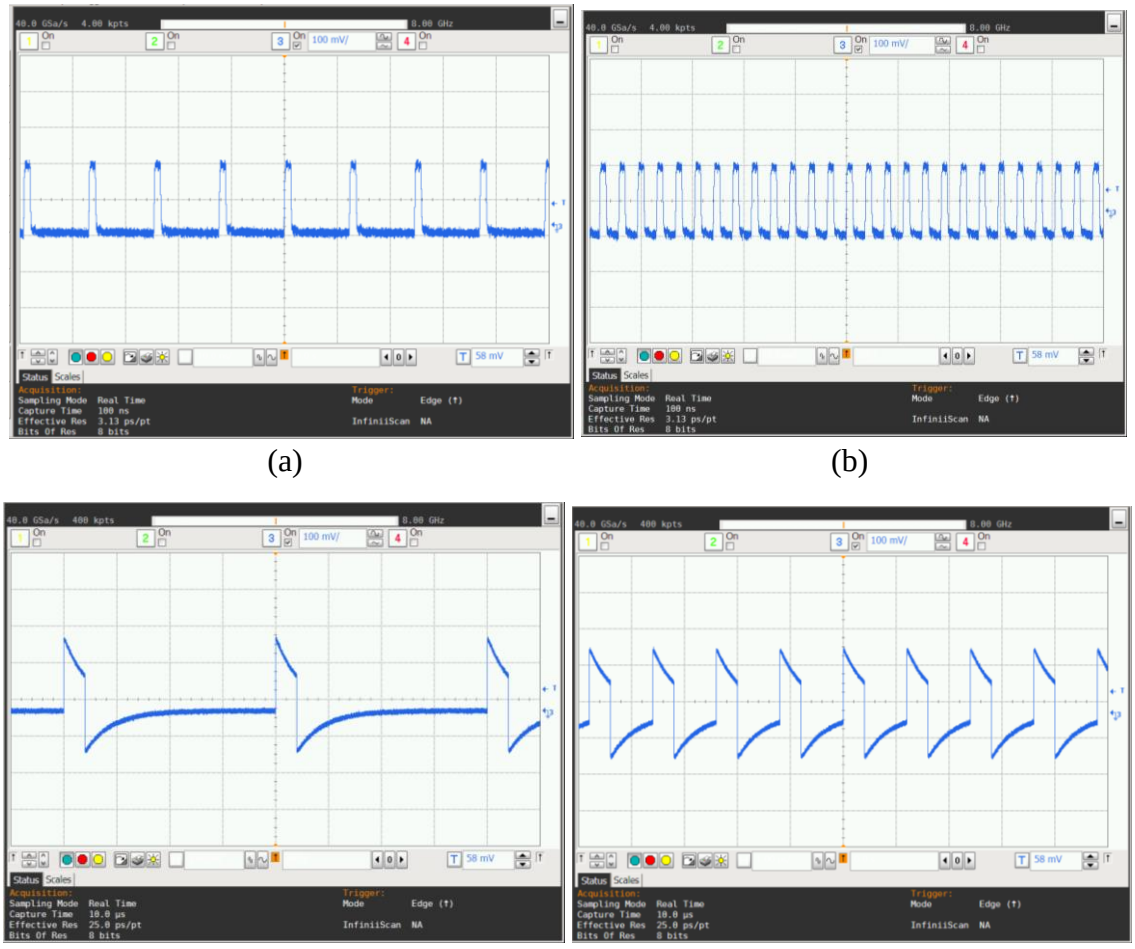
(a) (b)

Figure 4.16: (a) Layout of the proposed TSPC PDIV with the gated inverting keeper and (b) chip photo of the test chip.



(a) (b)

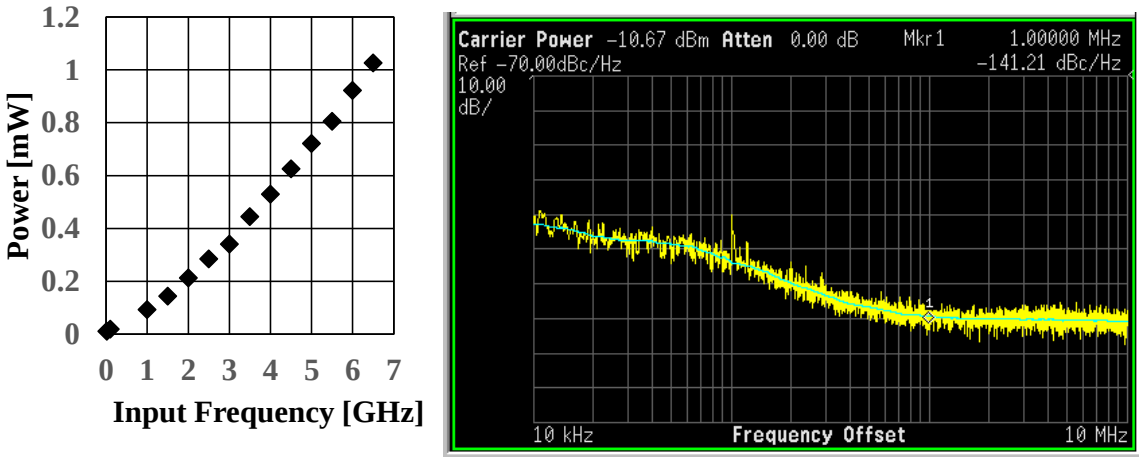
Figure 4.17: TSPC PDIV output of the non-gate inverting keeper with (a) 20MHz and (b) 1GHz input clocks (80-division).



(a) (b)

(c) (d)

Figure 4.18: TSPC PDIV output of the gate inverting keeper with (a) 80-division (6.5GHz), (b) 24-division (6.5GHz), (c) 80-division (20MHz), and (d) 24-division ratio (20MHz).



(a) (b)

Figure 4.19: (a) Power consumption of the PDIV and (b) phase noise with 6.5GHz input frequency.

Table 4.2: Performance summary and comparison of the proposed Programmable Divider

		[59]	[60]	[61]	[62]	**This work**
CMOS Tech [nm]		250	180	180	180	**65**
Freq. [GHz]	Max.	5.7	1.8	5	4.7	**6.5**
	Min.	5.14	0.5	0.6	0.01	**0.02**
Power Efficiency [GHz/mW]		0.91	0.31	0.25	1.79	**6.31**
PN [dBc/Hz] @ 1MHz offset		-	-148	3ps (Jitter)	-137	**-141**
Area [mm^2]		0.019	0.011	0.034	0.002	**0.002**

4.6 Conclusion

The 1V integer-N QPLL has been realized with the 65nm CMOS technology for the cognitive IR-UWB application. The proposed two stage linear tuning QVCO without SSB mixer technique enables the QPLL to accommodate higher capacity and data rate in full UWB band, 3.1 – 10.6GHz, with 23GHz/V linear VCO gain. The -59dBc reference spur is achieved with the proposed digitally background calibration for less than 1% of the CP mismatch. It mitigates the reference spur issue in spectrum sensing with 132MHz channel resolution. The settling time is less than 2μsec with 1% error.

The 0.02–6.5GHz wide operating frequency range TSPC PDIV achieves 6.31GHz/mW power efficiency. The gated inverting keeper technique enables the PDIV to operate at 20MHz input frequency by compensating leakage current issue in deep sub-micron technology. Analysis on the minimum and the maximum frequencies of the proposed TSPC PDIVs is suitable for designing wide lock range low power frequency synthesizers.

Chapter 5. Triple Channel UWB-based Cognitive IR-UWB

5.1 A Carrier-based UWB Radio

There are two types of signals used to transmit data in UWB systems: carrier-less and carrier-based signals. The Gaussian monocycle and its derivatives are often assumed in the literature as typical carrier-less UWB transmitted impulse waveforms [71]. The spectrum of the n-th-order derivative of a Gaussian waveform is given by

$$|P(f)| = A(2\pi f)^n \cdot exp - \frac{(2\pi f\sigma)^2}{2} \quad (5.1)$$

where A is a constant amplitude and σ is the original Gaussian standard deviation. The spectrum can be modified through the σ and n values. In [72], the authors show that one needs to take at least the seventh derivative to fit the PSD inside the FCC mask for indoor applications. The choice and especially the calibration of these parameters is not an easy task since the high- and low-frequency components of the PSD do not scale symmetrically. A little variation of the pulse shape caused by temperature, process variations and bias mismatch can enormously change the frequency spectrum of the pulse and the change may violate the FCC mask. In addition, this technique provide little flexibility in control of the power spectrum management. Moreover, the realization of these Gaussian shape pulses and their derivatives is also very difficult using standard CMOS circuits. Traditional carrier-less impulse generators provide wide-band monocycles that approximate Gaussian shapes using very specific components such as step recovery diodes [72] or

choke inductors [73]. These techniques suffer from a very limited tunability and require complex packaging techniques, thereby increasing substantially the system cost.

Compared to the carrier-less technique, a simple way to realize the short high-frequency UWB signals is by gating an oscillator as proposed in [74]. These signals are easier to manage within the FCC spectrum and produce less distortion by the antennas [75]. The oscillator center frequency defines the center frequency and the gate duration the bandwidth. The problem with this technique is that the output pulse features a square shape in time. The high side-lobe power in the spectrum must be filtered, resulting in poor system efficiency while increasing the system complexity. Moreover, in multiple-band systems, a good side-lobe rejection is mandatory for a good adjacent channel power rejection. The approach presented here is an oscillator whose output amplitude is modulated by a triangular signal. The smooth pulse shape of the triangular waveform provides a side-lobe rejection of more than 20 dB, and most of the power is confined in the useful bandwidth. The center frequency of the pulse can be calibrated independently from the bandwidth, which is very useful in multiple-channel systems. This specific signaling scheme will be defined as a "carrier-based" UWB.

5.2 A Triple-Channel UWB-based Cognitive Radio

In chapter 2, the optimal number of channel is three for a 1Gb/s UWB-based cognitive radio in terms of energy efficiency with 30% channel occupancy. Fig. 5.1 shows architecture of the proposed triple channel UWB-based cognitive IR-UWB radio. BPSK modulation is used since BPSK has a lower implementation complexity and gives the better BER performance than other modulation method.

In a transmitter, each channel consists of a 2^{23}-1 PRBS generating binary digital data signals, a multiplier modulating digital data with wavelet, and an up-conversion mixer. One wavelet generator provides triangular waveform to three different channels. A power amplifier (PA) covers whole UWB bands and transfers three different channel signals to one antenna. The output band-pass filter provides 3.1 to 10.6GHz UWB output filtering.

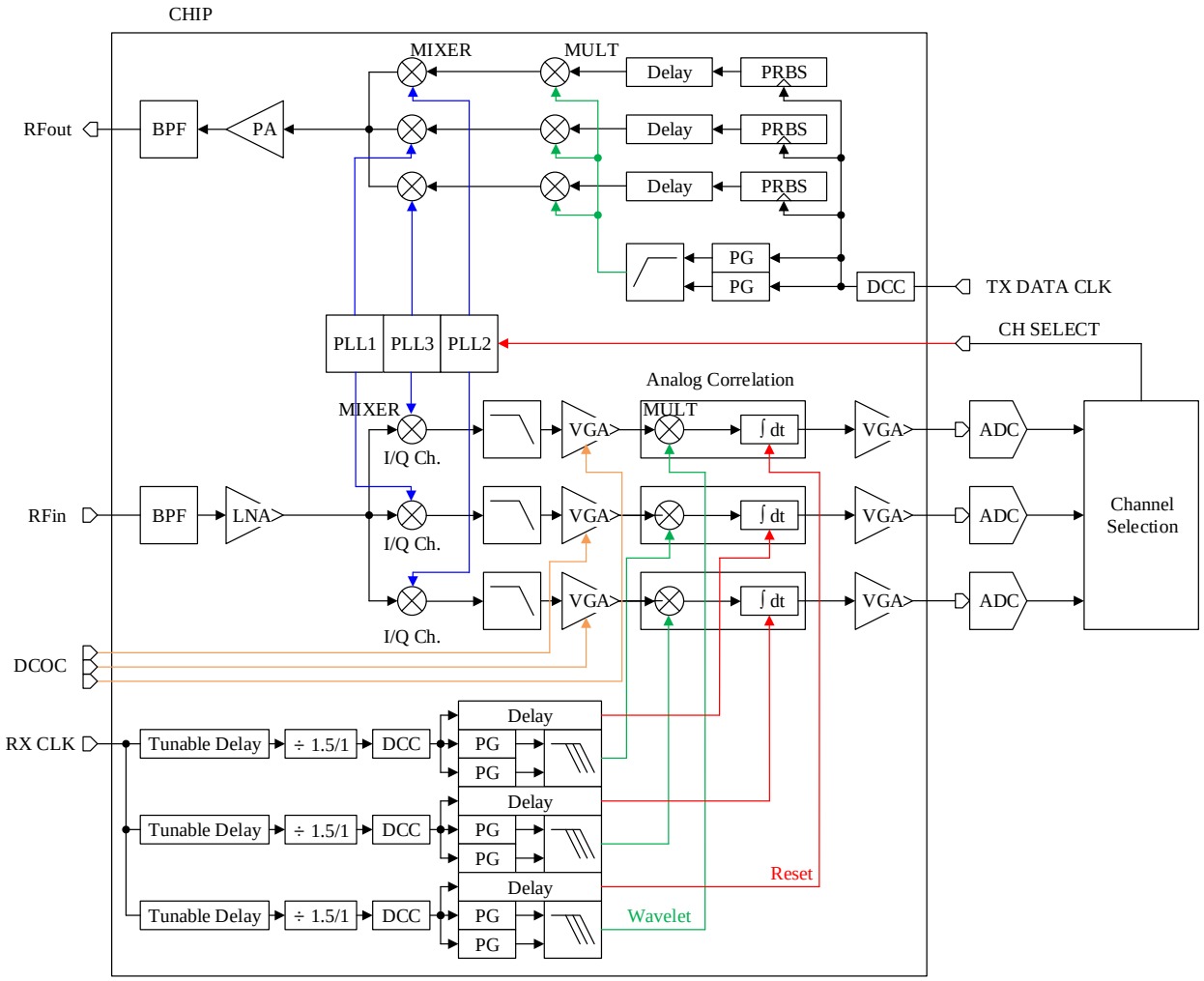


Figure 5.1: Architecture of Triple Channel UWB-based Cognitive IR-UWB

Quadrature analog correlation (a multiplier and an integrator) [76] is used since it reduces the sampling rate of the ADC down to pulse rate by implementing the matched filter correlation of the incoming pulses with the pulse template in the analog domain. In the receiver chain, a low noise amplifier (LNA) shares three channel and covers whole UWB band. Followed by LNA, there are three channels. Each channel consists of a down-conversion mixer, a low pass filter, an analog correlation circuit, and variable gain amplifier (VGA). The receiver chain also performs an analog wavelet-based spectrum sensing with only adding root square block after ADC to measure the power spectral density at certain frequency.

5.3 Transmitter of the triple-channel UWB-based Cognitive Radio

5.3.1 Triangular-shaped BPSK modulation

Fig. 5.2(a) shows block diagram of the proposed triangular-shaped BPSK modulation. The DCC circuit generates 50% duty cycle with 2X clock (CK) of the internal clock frequency (CK2). Two triangle pulse generator (PG) provides two different common mode level triangle waveforms (TP1 and TP2). The LPF reduces side-lobe peak of the TP1 and TP2, which leads to Gaussian-like waveform as TP3. TP3 is multiplied with input data at a multiplier, and triangle shaped BPSK modulated data are produced as shown in Fig. 5.2(b). The modified triangular shaped data with BPSK modulation provide spectrum-shaping at an up-conversion mixer.

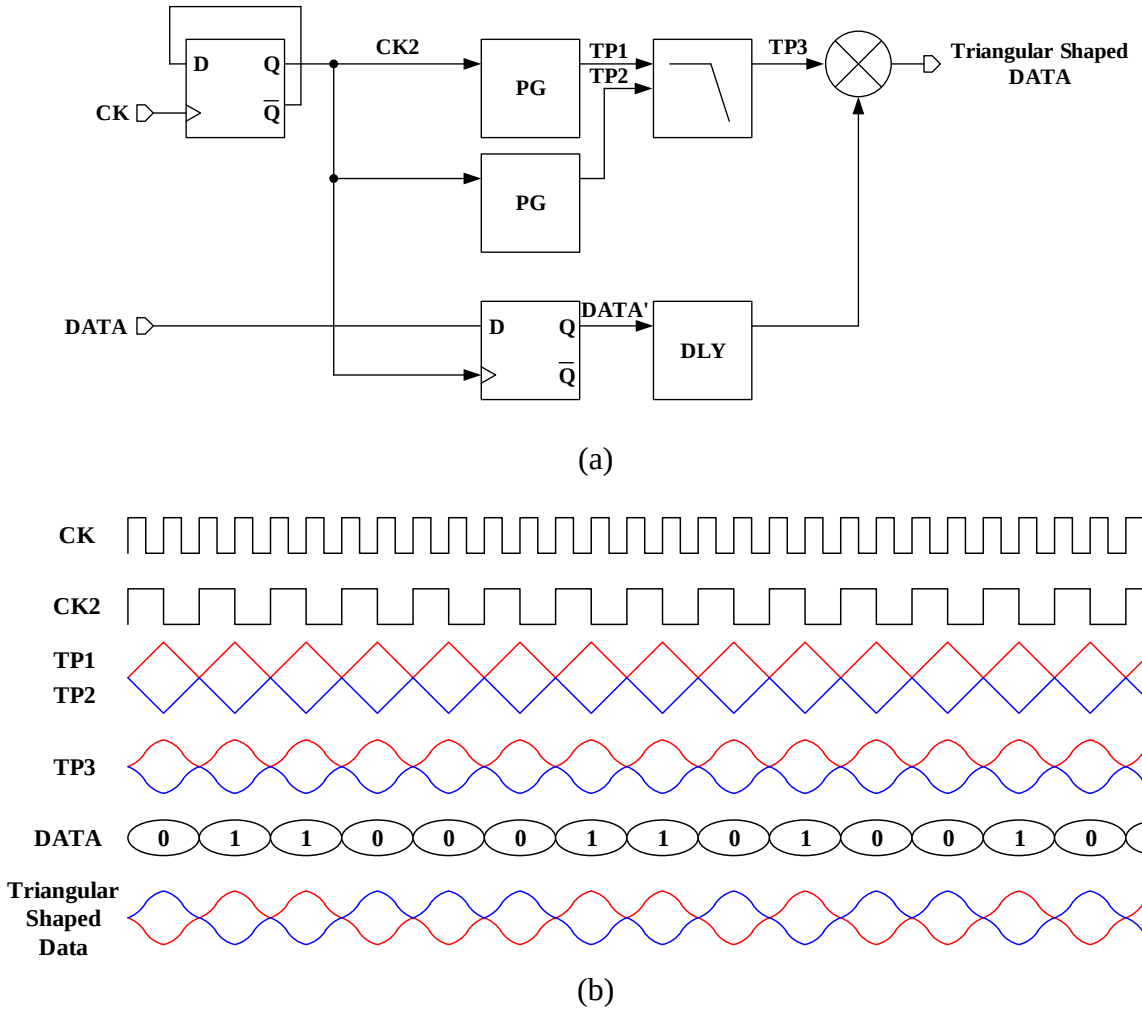


Figure 5.2: (a) Block diagram and (b) waveforms of the triangular-shaped BPSK modulation

5.3.2 Up-Conversion Mixer and Modulation Multiplier

Fig. 5.3 shows up-conversion and modulation multiplier for transmitter. In mixer stage, double balanced gilbert-type mixer is used to reduce LO leakage. Increasing the bias current of the RF transconductance stage makes higher gain and better linearity possible, but larger LO switching current causes voltage headroom issue. Therefore, the static current bleeding technique is implemented by using two PMOSFETs to reduce the bias current of the LO switches [77]. The load is a shunt-peaking resistor [78] to extend bandwidth.

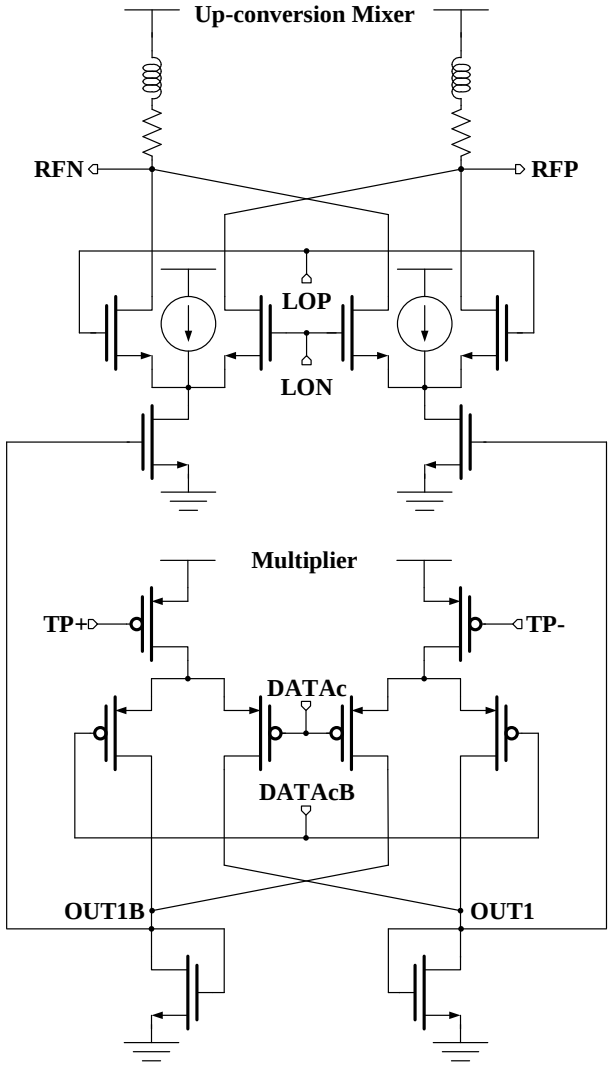


Figure 5.3: Up-conversion mixer and modulation multiplier for the triangular-shaped BPSK modulated signals

Triangular-shaped modulated BPSK data are achieved by multiplier stage with BPSK digital data and cyclic triangular waveforms. The multiplier is also gilbert cell type. The modulated data output is current that is mirrored to up-conversion mixer with current mirror. The current convey technique enables low voltage operation, high linearity, and wide dynamic range operation of the mixer and multiplier. The power consumption of the mixer and multiplier is 4mW.

5.3.3 Differential to Single-ended convertor and Antenna Driver

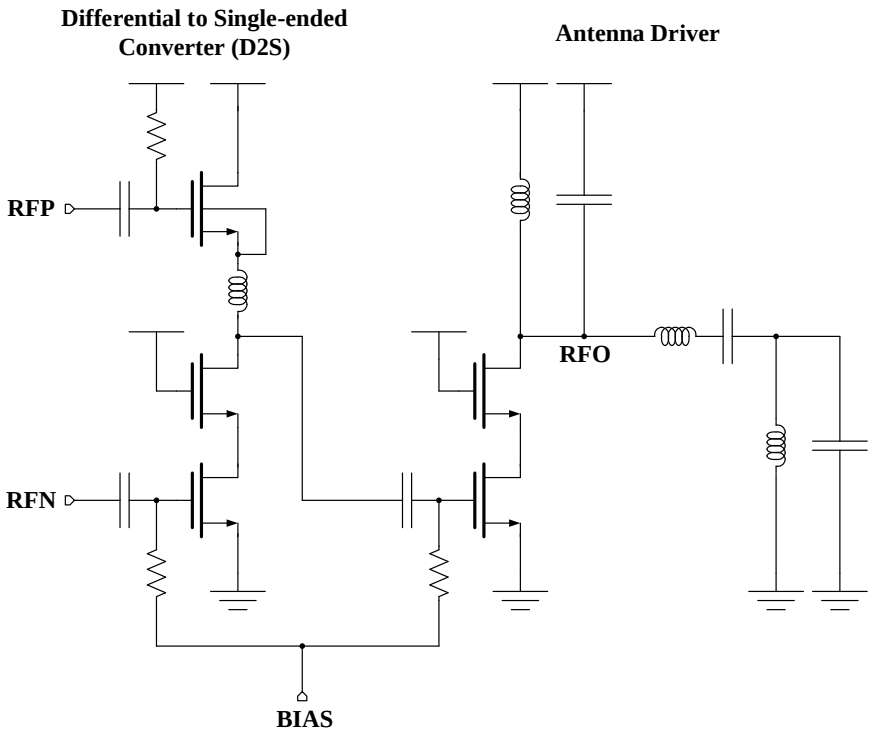


Figure 5.4: Differential to single-ended converter and antenna driver with BPF.

Fig. 5.4 shows a differential to single-ended converter to drive a single-ended antenna driver and antenna. One of the up-conversion mixer outputs is connected to source follower and the other output is connected to common source amplifier. Cascoded common source amplifier is used to increase the output impedance. Each input is biased differently to ensure saturation operation. The source follower stage and common source amplifier stage have the same gain due to the low impedance of the source follower. An inductor is added at the source follower output to extend bandwidth. The DC power consumption is 1.44mW.

Antenna driver is added to drive 50Ω antenna. Power efficiency is 0.016 since UWB output power is limited by -41dBm/MHz, so it is difficult to get high efficiency. 3rd order band pass filter is added at the output to get bandwidth from 3.1GHz to 10.6GHz. The DC power consumption is 5.78mW.

5.4 Receiver of the triple-channel UWB-based Cognitive Radio

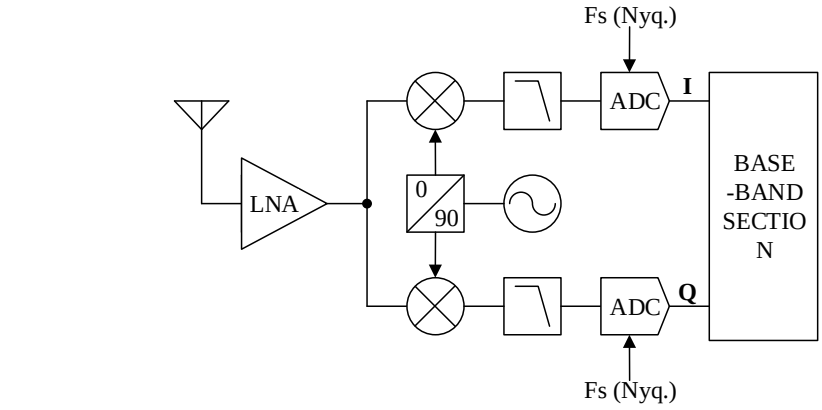
5.4.1 Quadrature Analog Correlation Receiver

Three different state-of-the-art UWB receiver topologies were analyzed: the direct conversion (DC), the quadrature analog correlation (QAC), and the transmitted reference (TR) as shown in Fig. 5.5 [79].

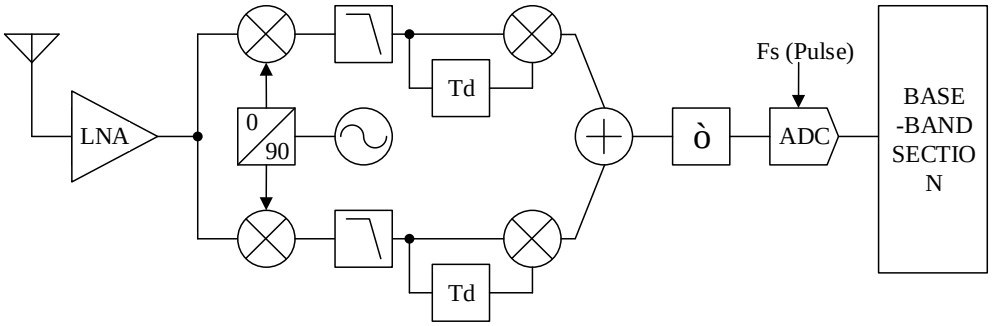
The DC UWB receiver was introduced in [80] for the 3–10.6 GHz band. In this topology, the incoming pulses are directly sampled by two parallel ADCs and processed in the digital domain. This results in a very flexible receiver, capable of doing wide parallel processing, hence, minimizing the acquisition time. The price to pay is the need for high-speed ADCs, which contribute significantly to the power budget. Another architecture worth considering is the transmitted reference (TR) receiver [81]. Instead of generating a pulse correlation template in the receiver, the reference pulse is delayed in the receiver to be correlated with the data pulse. TR receivers do not need any channel estimation and inherently capture all multipath components of the received signal. On the other hand, they suffer large performance degradation due to the very noisy correlation template. Moreover, the implementation of the analog delay line, necessary to

delay the reference pulse, is not straightforward. The high-speed ADCs can be avoided by moving the matched filtering of the incoming pulses with the pulse template from the digital to the analog domain [82]. This operation reduces the required sample frequency from Nyquist rate to pulse rate. The quadrature analog correlating (QAC) receiver architecture is based on this topology. It correlates the incoming pulses with windowed sinusoidal signal in the analog domain. Simplified channel compensation is done by repetitively opening and closing the window with a finite resolution time.

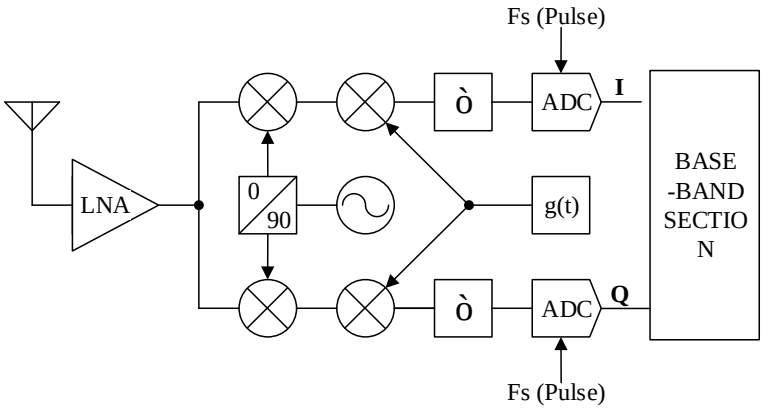
From [79] analysis, BER performance of the QAC receiver has less performance degradation due to ADC clipping from interferes since it benefits from its slower ADC. The TR receiver performs significantly worse than the other alternatives because of the noise cross-correlation term. The power consumption of the different alternatives is made based on state-of-the-art components and UWB front-ends reported in literature. The DC topology has high power consumption on baseband part since it requires high speed ADC and most of signal processing is done by baseband circuits. The TR topology requires high power consumption on the extra analog delay line. The QAC topology consumes similar power on analog front-end, but it consumes much lesser power on the ADC since the sampling rate can be reduced to the pulse rate. Moreover matched filter function is done at analog domain, so the power consumption on the baseband is much lesser than other topologies. The QAC receiver provides less synchronization effort thanks to I- and Q-channel information compared to single channel analog correlation receiver. In addition to performance benefits, the QAC receiver can easily employ an analog wavelet-based spectrum sensing without significant change in architecture.



(a)



(b)



(c)

Figure 5.5: (a) Direct conversion (DC), (b) transmitted reference (TR), and (c) quadrature analog correlation (QAC) receivers.

5.4.2 Wideband Low Noise Amplifier

A broadband amplifier is shown in Fig. 5.6, which employs a three-section Chebyshev active filter at input. The series RLC network formed by the transconductance stage forms a third section of the filter, which R is $\omega_T L_S$ series resistance in the source of transistor. The bandwidth of the matching stage of the inductively degenerated amplifier in Fig. 5.6 is very depended on the Q factor of the input Chebyshev filter. The input impedance of the MOS transistor with inductive degeneration is achieved as [83]

$$Z_{in}(s) = \frac{1}{s(C_{gs}+C_p)} + s(L_s + L_g) + \omega_T L_s \qquad (5.2)$$

where ω_T = gm/(Cgs + Cp) = gm/Ct. This network is embedded in the Chebyshev structure to form the input matching network. The parallel resonance occurs between Ls andCgs. The second series resonance, on the other hand, occurs between Lg and the equivalent capacitance resulting from the parallel combination of Ls and Cgd at frequencies higher than the parallel resonance.

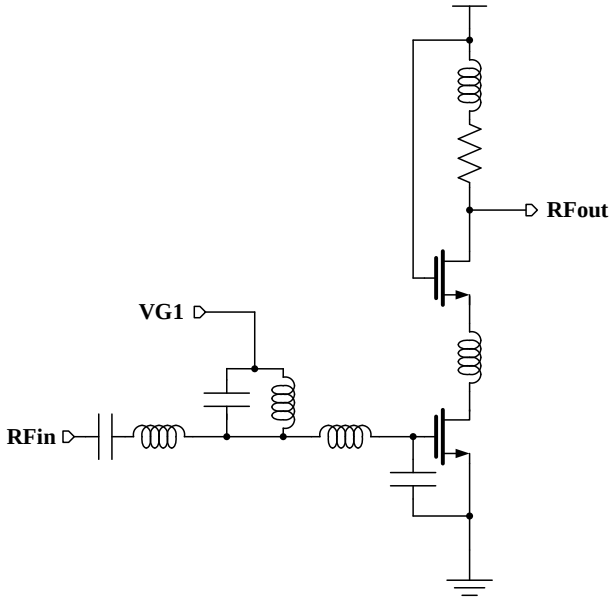


Figure 5.6: An ultra-wideband amplifier using Chebyshev active filter

From noise analysis perspective, the noise contribution of the input network is due to the limited quality factor Q of the integrated inductors. The noise optimization relies on achieving the highest Q for a given inductance value. The noise contribution of the transistor M1 relies on the choice of its width for a given current bias. The minimum noise figure can be achieved once Ls and Ct resonate, and consequently a low noise figure over the entire amplifier bandwidth is obtained.

The voltage gain of the amplifier can be found by Rs/W(s), where Ws is the Chebyshev filter transfer function. The transfer function of the Chebyshev filter is unity in-band and tends to zero out-of-band. So the impedance looking into the amplifier is Rs in-band, and it is very high out-of-band. The overall gain is

$$\frac{V_{out}}{V_{in}} = -\frac{g_m W(s)}{sC_t R_s} \cdot \frac{R_L\left(1+\frac{sL_L}{R_L}\right)}{1+sR_L C_{out}+s^2 L_L C_{out}} \qquad (5.3)$$

where R_L is the total resistance, L_L is the load inductance, and Cout is the total output parasitic capacitance at the drain of input transistor. The shunt-peaking load is compensating the gain roll off, which in equation (5.3) is set by L_L. The presence of parasitic capacitor Cout introduces spurious tones, which should be kept out-of-band. The results observed from this design benefits from the use of a ladder-filter input matching network. This LNA achieves wide bandwidth and input matching from 3−10 GHz. However, this wideband LNA needs too many components, specifically high Q inductors, to form the Chebyshev filter at the input. This drawback adds to the area and the cost of the design.

The designed LNA provides 3.1-10.6GHz bandwidth with 10.83-12.72dB gain, <-10dB return loss, and 1.24-4.18dB noise figure. The input referred intercept point (IIP3) is -8.65dBm, and the DC power consumption is 4.58mW.

5.4.3 Down-Conversion Mixer

Passive mixers dissipate no DC power, except their clock generation circuits, and offer better noise performance with lower supply voltage than active mixer [84]. Moreover, it follows the CMOS process scaling, which leads to smaller die area for the receivers. Furthermore, in terms of LO feed-through, a passive mixer outperforms an active mixer. However, there is crosstalk between I/Q channels and between different channels for multi-channel radio. As a result of this lack of reverse isolation, a passive mixer translates baseband impedances seen from its baseband side to the RF and vice versa through frequency shifting.

On the other hand, active mixers offer high conversion gains, and exhibit high reverse isolation between the IF and RF ports. This isolation essentially eliminates IQ crosstalk [85]. However, it requires higher power supplies due to stacking of transistors.

The designed Gilbert-type double balanced active mixer as shown in Fig. 5.7 blocks LO feed-through and provides 1GHz 3dB BW with 4.6dB conversion gain and < 14dB noise figure. The input referred intercept point (IIP3) is -0.01dBm, and the DC power consumption is 3.8mW. Source degeneration technology is applied to get high linearity. A resistor is used for the degeneration since the mixer should provide broadband operation. The resistor, however, increases noise figure of the mixer.

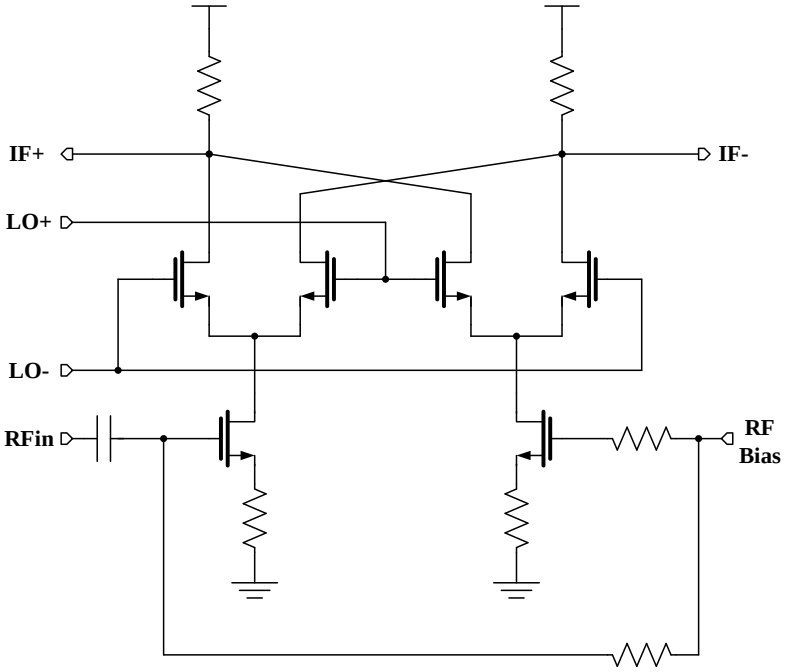


Figure 5.7: Gilbert-type double balanced active mixer with resistive source degeneration

5.4.4 Analog Correlation Circuit

For the coherent receiver, the incoming signal will be compared with the template one in phase. An analog correlation is used to realize the comparison in analog domain. It can be implemented with a multiplier and an integrator. The product of the multiplication will be proportional to the degree of correlation between the two signals, input signal and template one. The Gilbert-cell based multiplier [86] is employed to provide the wide bandwidth of the UWB band. Fig. 5.8 shows the proposed analog correlation circuit. The multiplication block includes the transconductance stage and switching stage with diode-connected PMOS loads. Both of the stages can provide gain to the output product. Bias is important for the multiplier to operate in saturation region since the correlation gain depends on the gain of the multiplier besides the amplitude of the template pulse

and the input signal, the synchronization error between two signals. The synchronization to boost correlation gain is done by variable delay change for the template pulses.

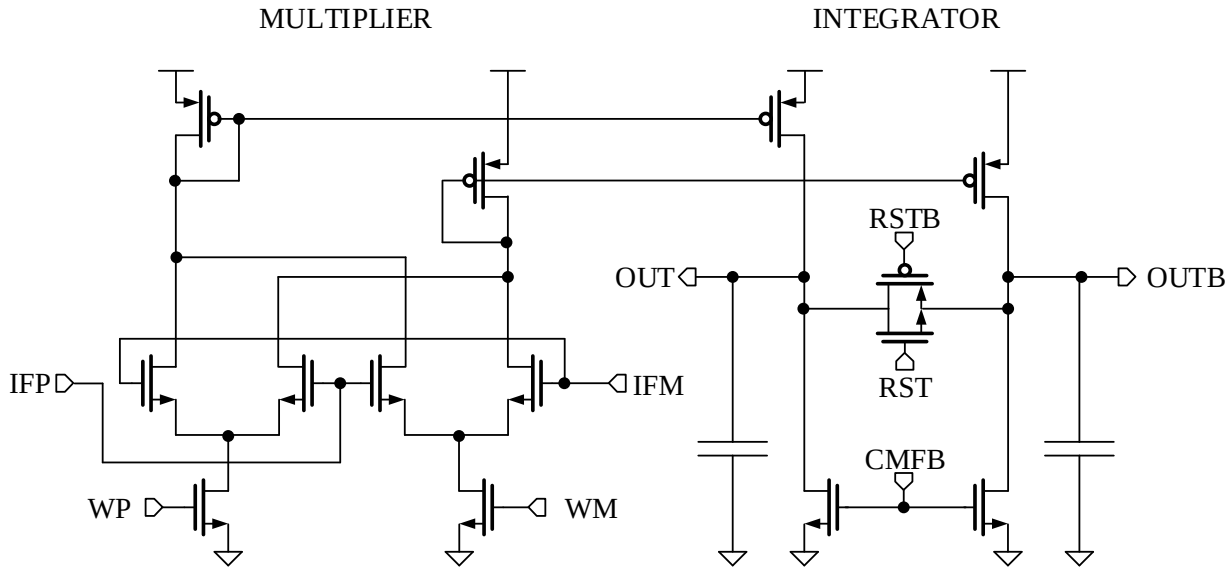


Figure 5.8: Gilbert-type analog correlation circuit with a multiplier and integrator.

The output current of the multiplication is transferred to the integrator through PMOS current mirror pairs, and it is integrated at the output load capacitors of the integrator. The AC response of the ideal integrator has a pole at DC and has a constant phase of 90 . However, the dominant pole of the practical integrator has finite output impedance, which results in a pole above DC. The dominant pole should be less than 1/5 times of the window frequency, f , to prevent the leakage of signal detection [87]. Across of the differential output, a switch is inserted. It consists of a PMOS and a NMOS with the gate is controlled by Reset clock signal. The switch is triggered every cycle for about 500ps. When the switch is ON, the two differential outputs are shorted, and CMFB makes the output go to the reference level. When the switch is OFF, the two outputs are evaluated during remain cycle time. The designed analog correlation circuit provides two mode options. One

is for QAC receiver and has 66MHz of 3dB bandwidth, and the other is for spectrum sensing mode and has 5MHz and 8MHz of the 3dB bandwidth at Mode 0 and at Mode 1 respectively.

5.4.5 Variable Gain Amplifier with DCOC

VGAs help tame signals that exhibit wide dynamic range. VGAs are used in two circumstances. The first encompasses all those situations where the circuit designer must match an input signal level to the full-scale input of the analog-to-digital converter (ADC) or an FM discriminator. To achieve the linear relationship between the VGA voltage gain and the control voltage, the Gilbert type four-quadrant multiplier is used since its output is equal to the product of the two inputs.

However, there are two drawbacks which make it difficult to implement this VGA using the Gilbert cell. First, the cascoded structure requires large voltage headroom and has difficulty functioning well with a 1.0V supply. Observe that the feedback loop of the AGC system works at very low speed; thus the control voltage varies at a very slow rate. Fig. 5.9(a) depicts the folded Gilbert cell [88], where the bottom differential pair of the original Gilbert cell can be folded without degrading its performance to reduce the number of cascoded transistors. Second, the voltage gain of the VGA changes its polarity as the control voltage changes. This limits the tuning range of the control voltage. To extend the linear control range, a constant current source which sinks a current slightly greater than the current source of the conventional cascade Gilbert cell multiplier, is added to the tail of one of the differential pairs to force one differential pair to possess a gain higher than the other's over the entire control range.

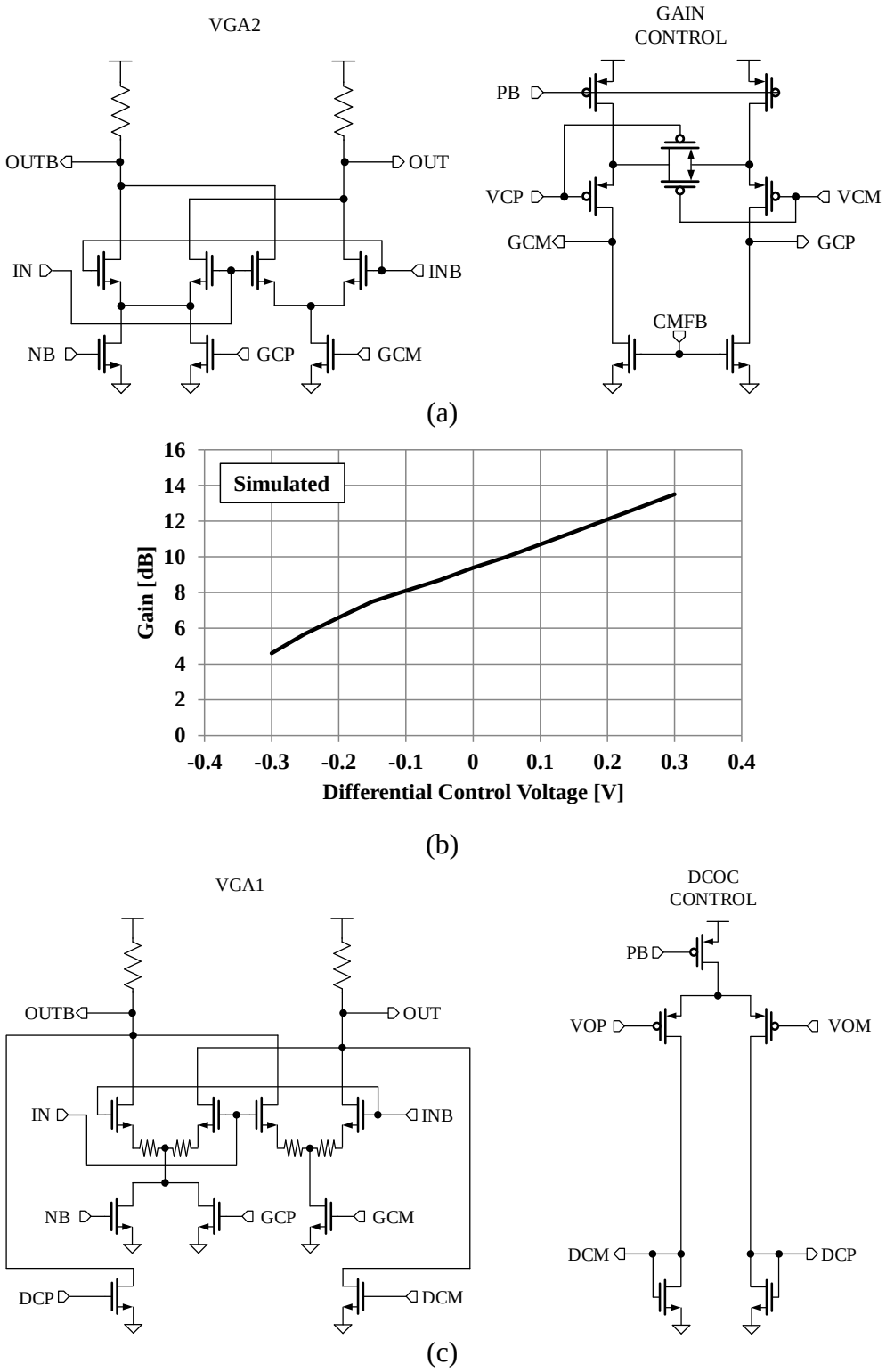


Figure 5.9: (a) Variable gain amplifier (VGA), (b) simulated gain curve with differential control voltage, and (c) VGA with DC offset cancellation and the control

The VGA is adopted for the output of the analog correlation circuit. The measured voltage gain as a function of control voltage VC (=VCP-VCM) has depicted in Fig. 5.9(b), revealing linear-in-magnitude gain transfer characteristic in VC from -0.3V to +0.3V for 4dB to 14dB gain variation.

There is another VGA in the receiver chain at the output of the down conversion mixer. The VGA adds DC offset cancellation (DCOC) function by adding differential current sources at VGA output. The cancellation level is controlled by diode-connected load amplifier as shown in Fig. 5.9(c). It provides 500MHz 3dB BW with 11dBm of the input referred intercept point (IIP3) and 1mW of the DC power consumption. Source degeneration technology is applied to get high linearity. The noise figure is less than 20dB.

5.5 UWB Chip Antenna 3.1 -10.3 GHz

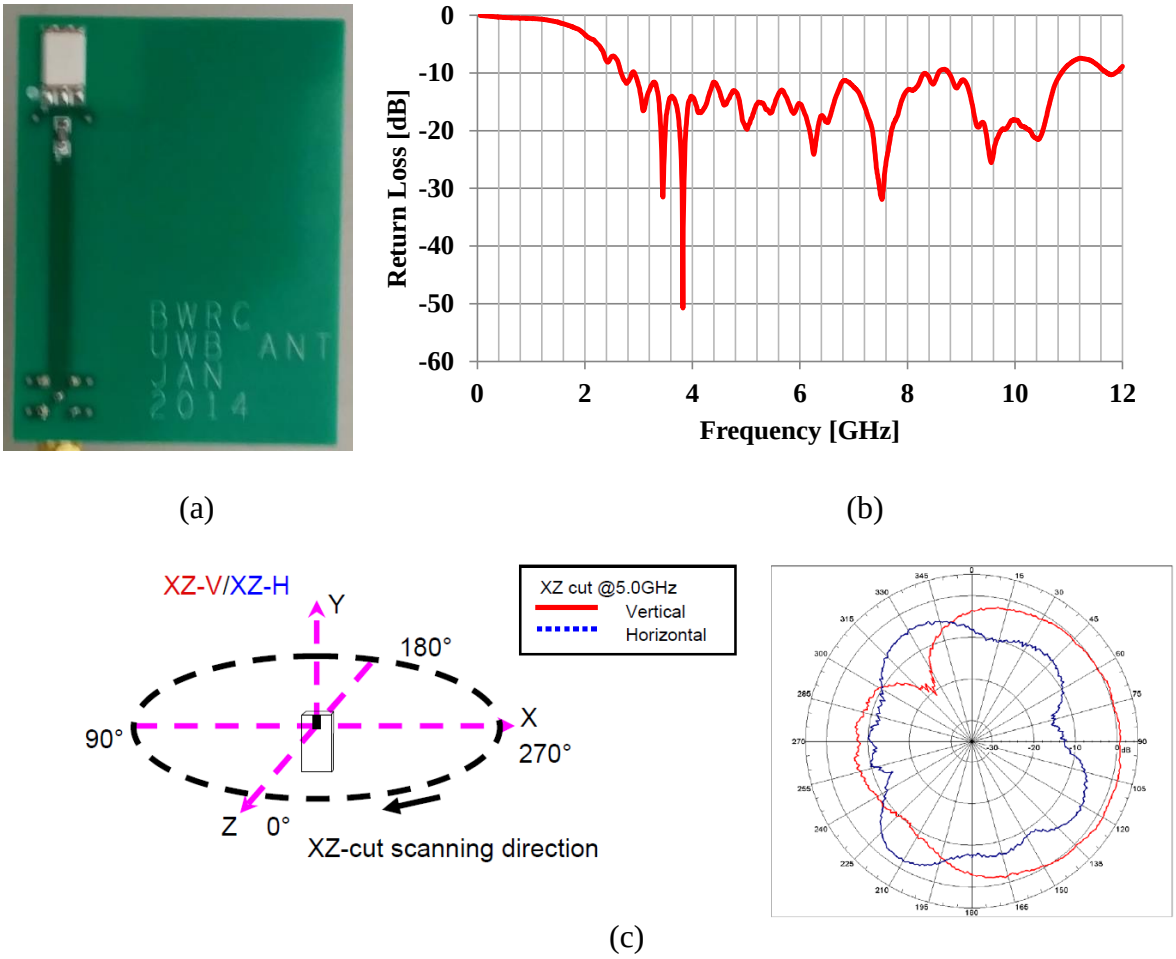


Figure 5.10: (a) Antenna board with UWB chip antenna, (b) antenna return loss and isolation, and (c) antenna radiation pattern

Antenna board is designed with UWB chip antenna from Johanson Technology® to cover from 3.1GHz to 10.3GHz frequency range as shown in Fig 5.10(a). Fig. 5.10(b) shows the return loss curves. The measured 10dB return loss bandwidth is from 3 to 11GHz. which confirms the UWB characteristic of the chip antenna performance. The minimum return loss is 9.5dB. Fig. 5.10(c)

shows antenna radiation pattern. The peak gain is 1.5dBi and the average gain is -3.5dBi in XZ-V plane.

5.6 Measurement Results

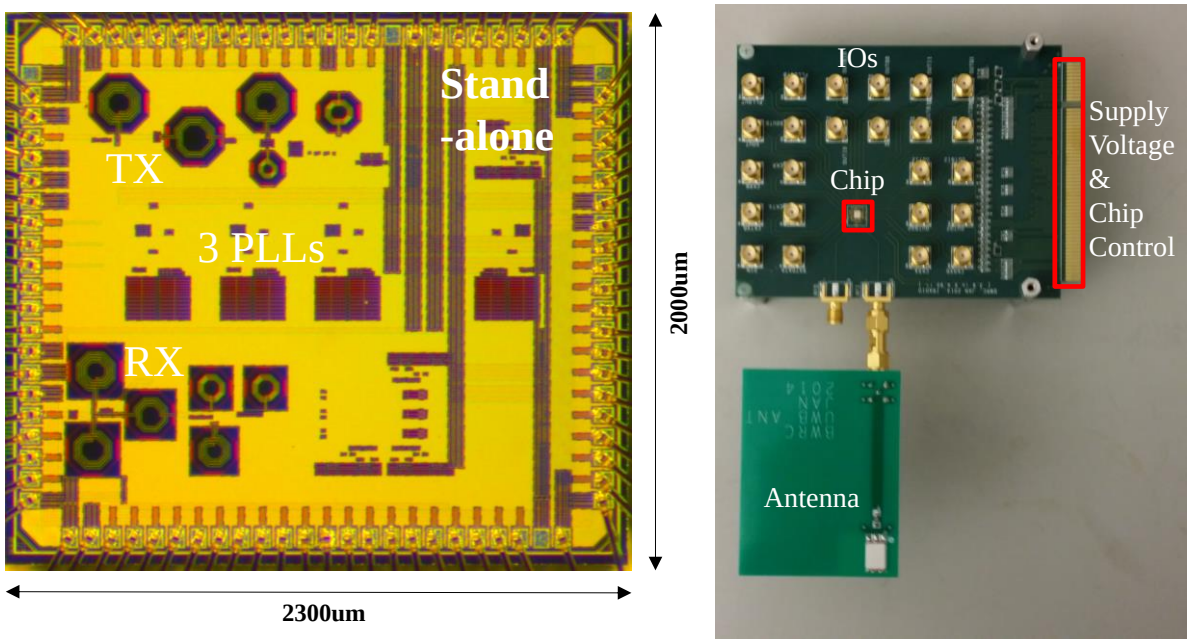


Figure 5.11: (a) Die microphotograph of the test chip and (b) PCB with chip-on-board packing for test chip and a UWB antenna board.

The prototype triple-channel UWB-based cognitive radio chip was fabricated in a 1.0V 65nm digital CMOS process provided by TSMC. The die measured 2.3mm×2mm^2. Active area is roughly 2.1mm^2. Fig. 5.11(a) shows a microphotograph of the chip. A PCB was designed for test measurements, and chip-on-board packaging was used to bond the chip directly to the PCB board. Fig. 5.11(b) shows the PCB and UWB antenna board. Supply voltages and DC control signals can

be provided through 32 bit PCI connector. Two test boards were used for a transmitter and a receiver. Communication distance is less than 1m.

Fig. 5.12(a) shows Measured BPSK triangular-shaped pulse with a center frequency of 3.564GHz with only one channel activation. Its power spectral density is less than -41dBm/MHz and null-to-null bandwidth is about 900MHz. Side-lobe is reduced to below noise floor level by using LPF at the triangular wave guide as shown in Fig. 5.12(b). Fig. 5.12(c) shows Measured BPSK triangular-shaped pulses with three different center frequencies of 3.564GHz 4.488GHz, and 5.412GHz with three channel activation together. Their power spectral densities are also less than -41dBm/MHz.

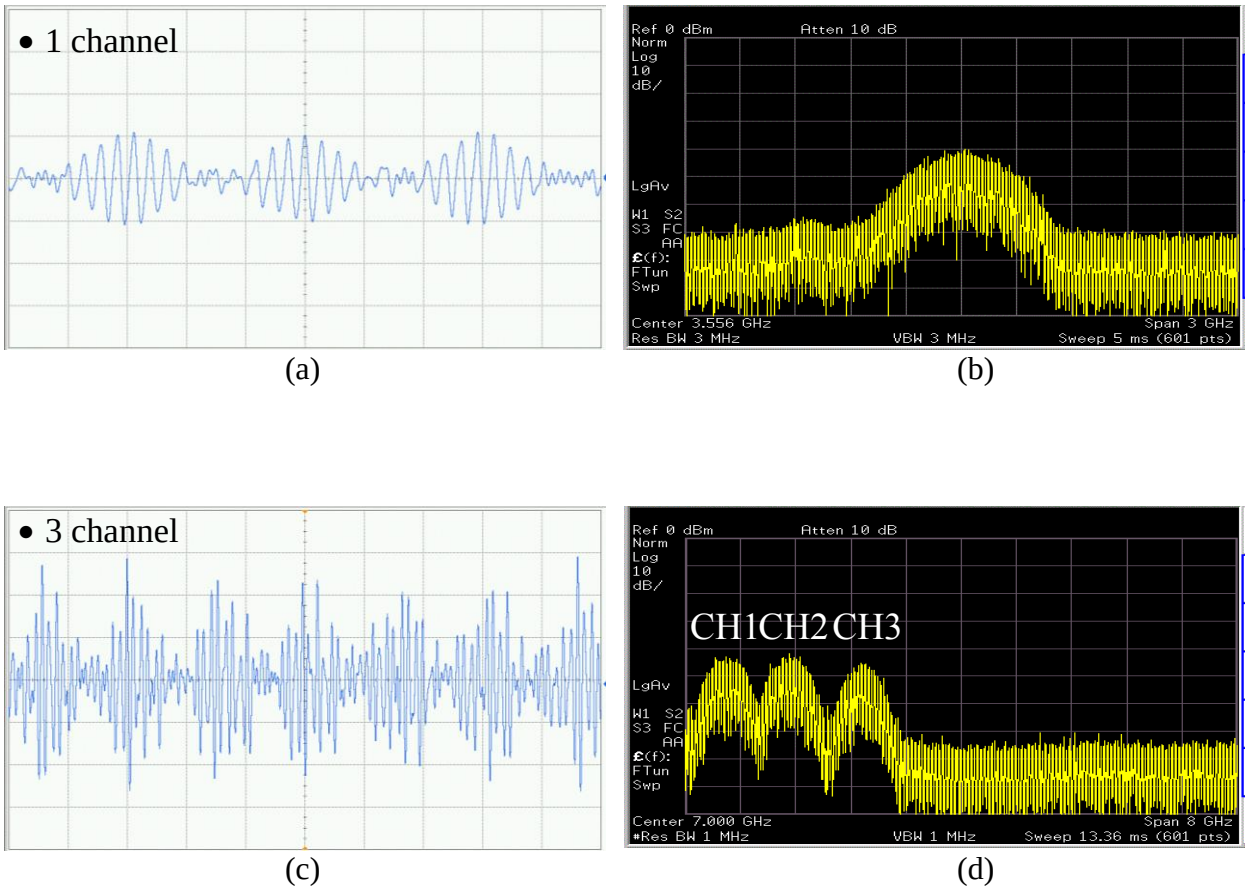


Figure 5.12: (a) Measured BPSK triangular-shaped pulse with a center frequency of 3.564GHz and (b) its power spectral density, and (c) measured BPSK triangular-shaped pules with three center frequencies of 3.564GHz, 4.488GHz, and 5.412GHz and (d) their power spectral densities.

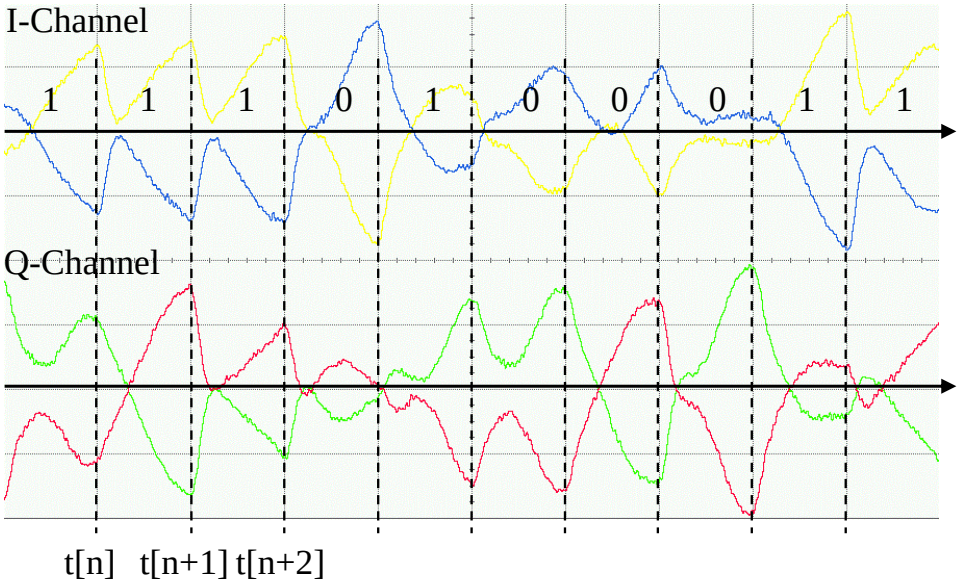


Figure 5.13: I- and Q- channel analog correlation output waveforms for QAC receiver mode

Fig. 5.13 shows the output waveforms of I- and Q- channel analog correlation during QAC receiver mode. Each output is reset at every pulse rate (333MHz). After about 500psec reset pulse period, the output is evaluated again. The sample and hold circuit catches the value right before the reset. The value is converted digital value with 4bit ADC.

A 30MHz of 3dB BW narrowband interferer and a 900MHz of null-to-null BW broadband interferer are intentionally generated as shown in Fig 5.14. The narrowband interferer is located at 5GHz to mimic Wi-Fi signal, and the broadband interferer is located at 5.94GHz with IR-UWB signal. These interferers affect CH3 signal of Fig. 5.12(d). Without these interferers, the measured BER of Fig. 5.12(d) case is 9.2×10^{-7}, which leads EPUB to 61pJ/bit. With these interferers, the BER of the CH3 is degraded to 1.5×10^{-1}, which increases total EPUB of the radio.

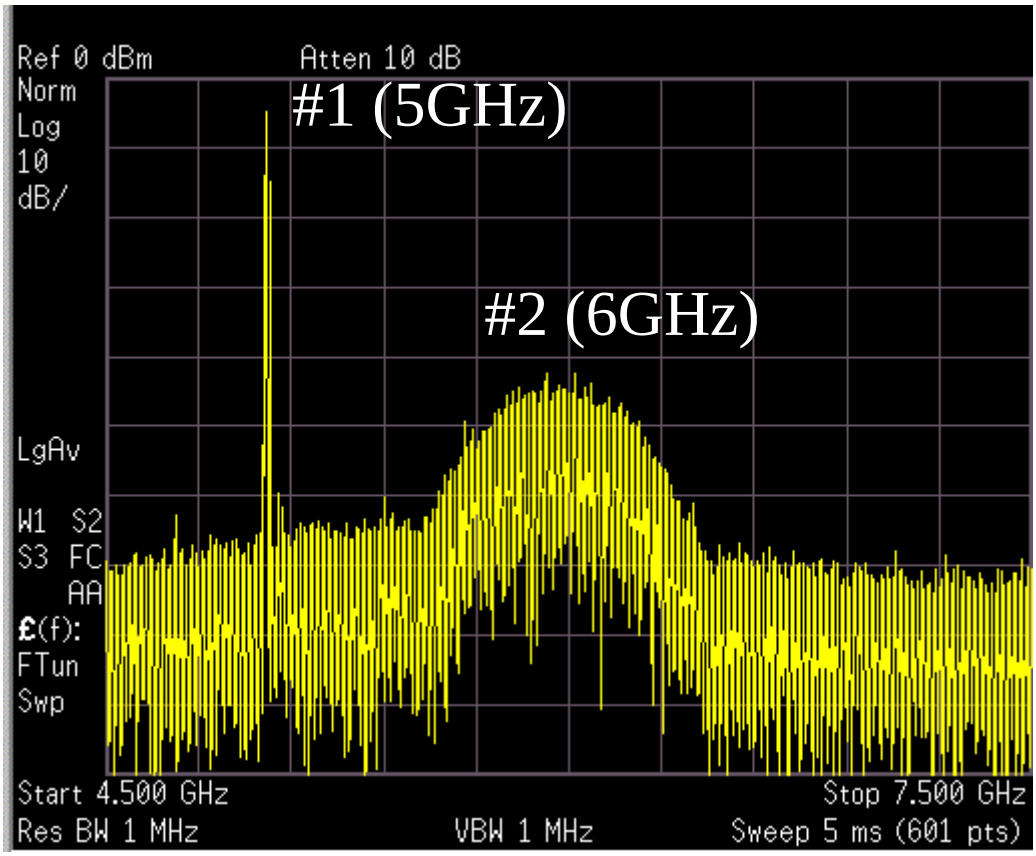


Figure 5.14: Measured narrowband interferer with a center frequency at 5GHz (about 30MHz of 3dB BW) and wideband interferer with a center frequency at 5.94GHz (about 900MHz of 3dB BW)

The center frequency of the CH3 moves to 6.864GHz to avoid the interferers of Fig. 5.14. Fig. 5.15 shows the carrier frequency change of the CH3. The measured BER of the CH3 is 4.8×10^{-6}, which leads EPUB to 63pJ/bit. This is higher than that of Fig. 5.12(d) without the interferers since the frequency difference on CH3 increases free path loss and power consumption increase of the PLL and LO path. However, this is much lesser than that of Fig. 5.12(d) with the interferers since CH3 signal can avoid the interferers.

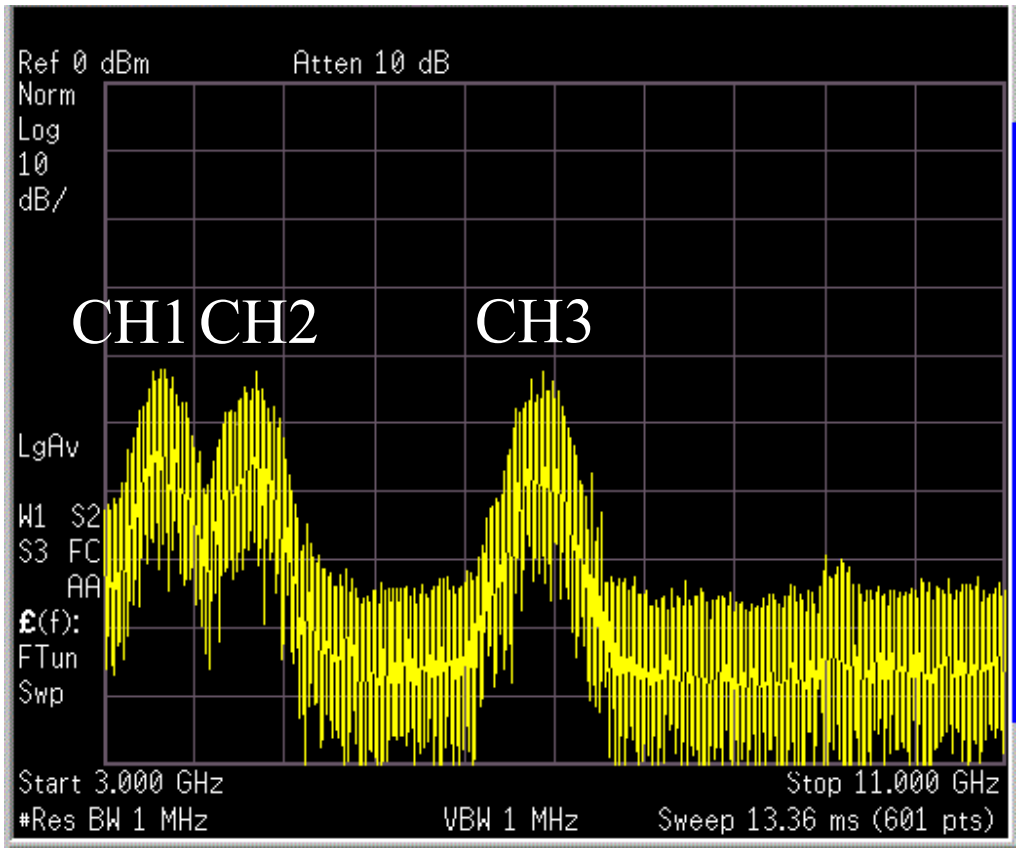


Figure 5.15: Measured power spectral density of the BPSK triangular-shaped pules with three center frequencies of 3.564GHz, 4.488GHz, and 6.864GHz.

Fig. 5.16 shows the worst case channel allocation. The carrier frequencies are 8,184GHz, 9.108GHz, and 10.032GHz. The measured BER is 1.1×10^{-4}, and the EPUB is increased to 102pJ/bit.

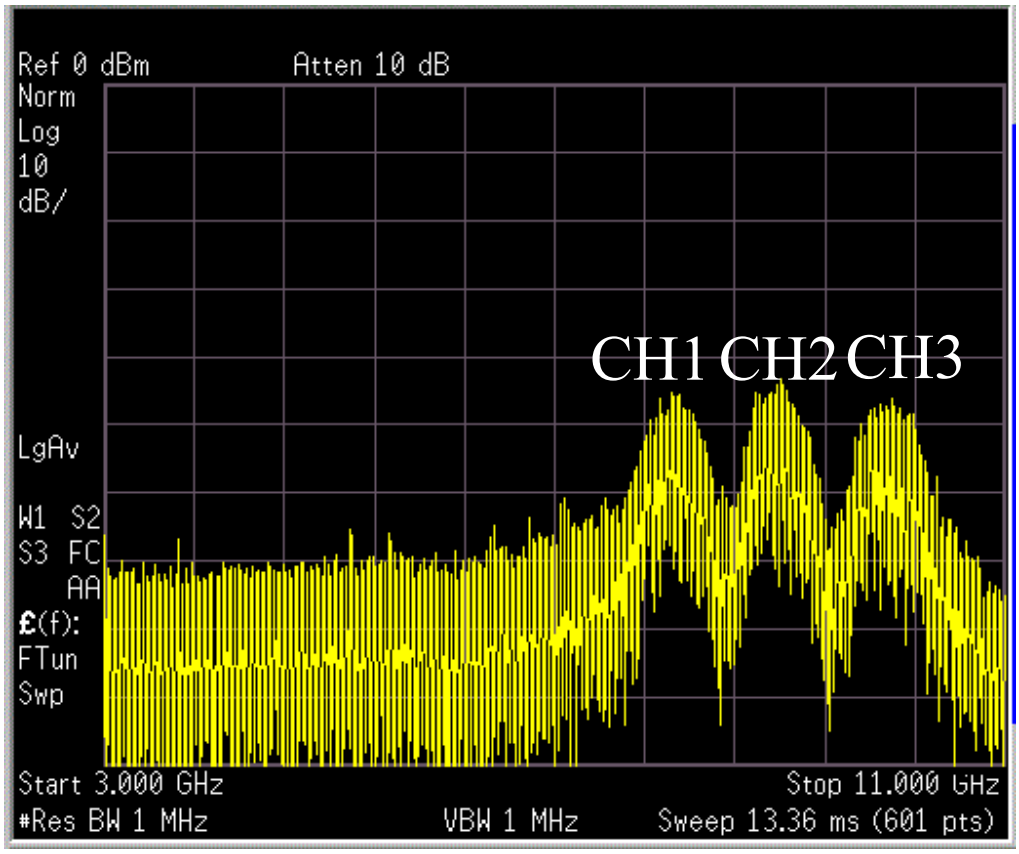


Figure 5.16: Measured power spectral density of the BPSK triangular-shaped pules with three center frequencies of 8.184GHz, 9.108GHz, and 10.032GHz.

Fig. 5.17 compares recently published UWB and 60GHz transceivers [6-15] with this work in terms of Energy/bit as a figure-of-merit (FoM). This work provides lowest energy/bit performance at 1Gb/s data rate. The best case is three lowest frequency allocation for three channel as 3.564GHz, 4.488GHz, and 6.864GHz. The worst case is three highest frequency allocation for three channel as 8.184GHz, 9.108GHz, and 10.032GHz.

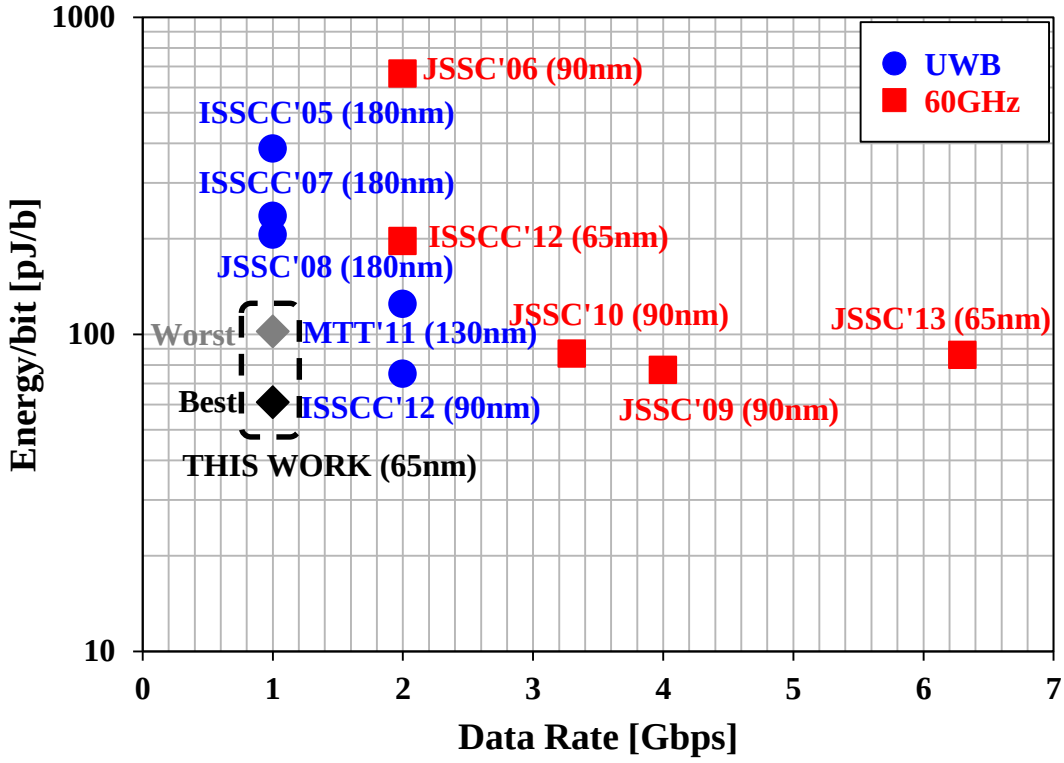


Figure 5.17: FoM (Energy/bit) comparison with data rate and process

Fig. 5.18 compares recently published UWB and 60GHz transceivers [6-15] with this work in terms of BER. The best BER is 9.2×10^{-7}, and the worst BER is 1.1×10^{-4}. Fig. 5.19 compares recently published UWB and 60GHz transceivers [6-15] with this work in terms of Communication distance. The maximum distance of this work is 1m, which is limited by noise figure of the whole receiver chain and PLL phase noise. There is the trade-off between communication distance and power consumption of the radio. Table 5.1 summarizes test chip performance.

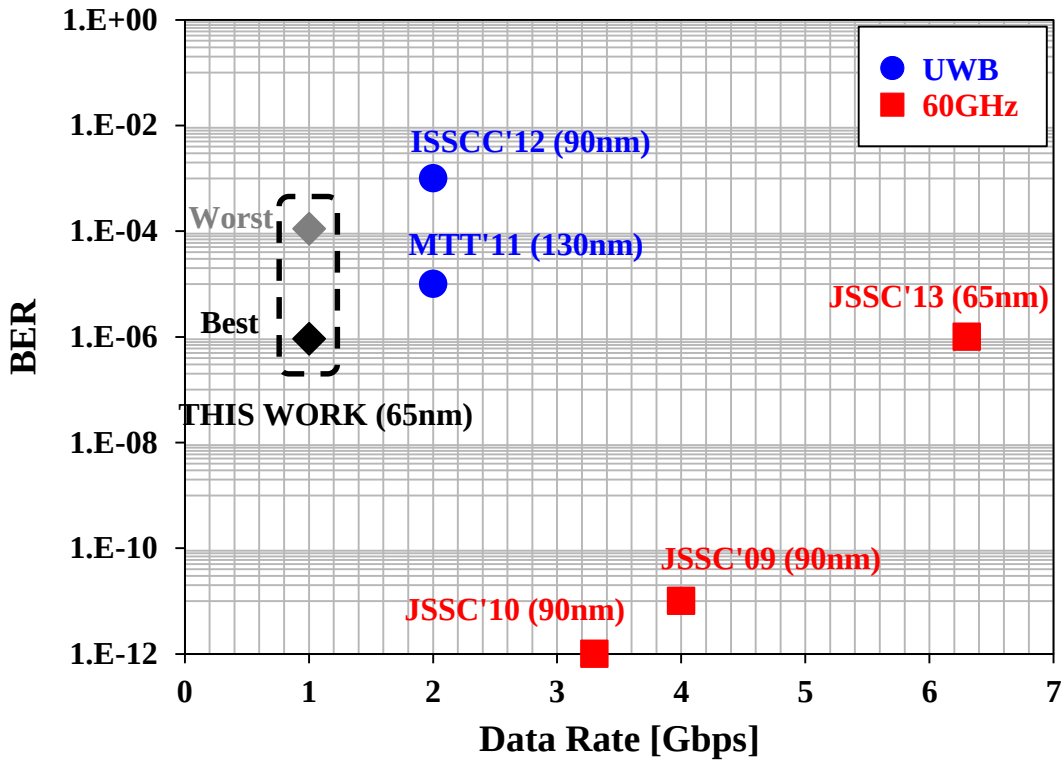


Figure 5.18: BER comparison with data rate and process

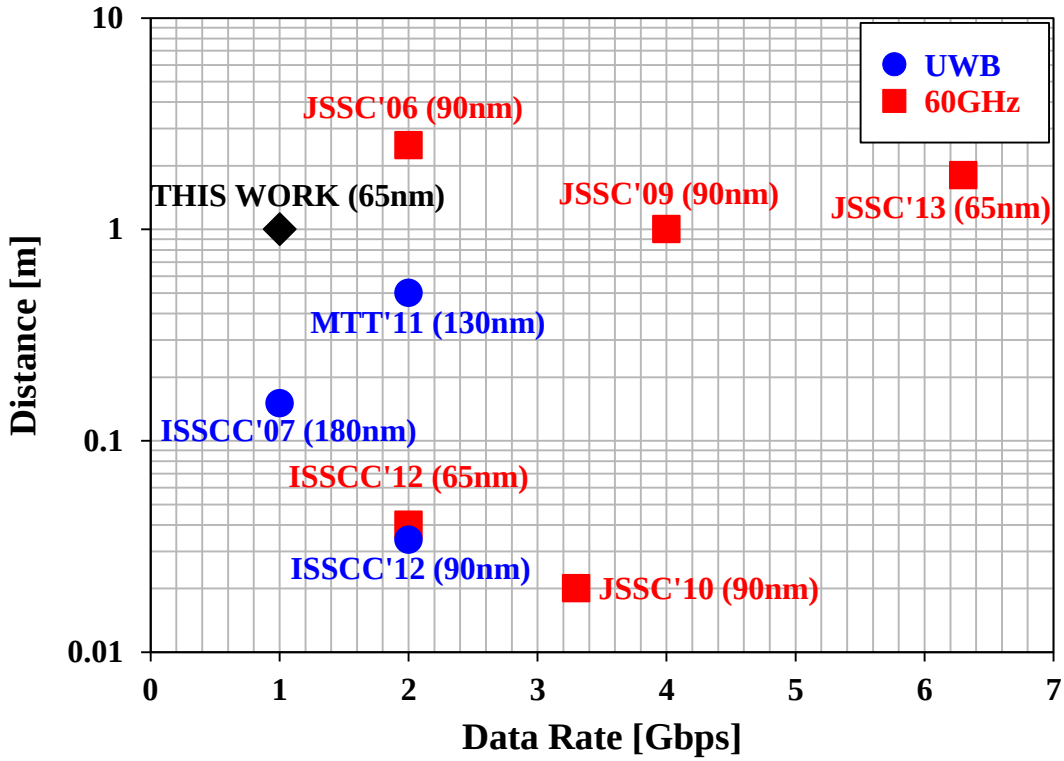


Figure 5.19: Communication distance comparison with data rate and process

Table 5.1: Chip performance summary

Technology [nm]		65 (TSMC GP CMOS)	
Supply Voltage [V]		1	
Area [mm^2]		2.3 × 2.0	
Frequency Range [GHz]		3.1 – 10.6	
The number of channels		3	
Data Rate [Gb/s]		1	
Modulation		BPSK	
Pulse Shaping		Triangular + LPF	
Maximum Communication Distance [m]		1	
		Best Case	Worst Case
Average Power [mW] (3 channels)	TX	24	39
	RX	22	36
	QPLL	15	27
BER		9.2×10^{-7}	1.1×10^{-4}

5.7 Conclusion

This chapter addressed the major interferer issues of the IR-UWB transceiver design. The proposed triple channel UWB-based cognitive radio achieves 1Gb/s data rate communication even with over 30% channel occupancy by aggregate three discrete channels. Each channel data rate is 333Mb/s. Communication distance is 1m.

The test chip is fabricated with 1V 65nm GP CMOS. Chip size is 2.3×2 mm^2. The test chip verified frequency-agile three independent channel cognitive radio. The lowest energy/bit is 61pJ/bit, and the highest energy/bit is 102pJ/bit. It achieves best BER of 9.2×10^{-7} and worst BER of 1.1×10^{-4}. The test chip demonstrated cognitive radio operation with intentional interferer assertion. The test chip provides lower energy/bit performance by avoiding interferers.

Chapter 6. Conclusion

6.1 Summary

Benefiting from extremely large bandwidth and low emission level allowed by the FCC, the UWB technology is capable of achieving high data rates of 1~2Gbps for short range wireless communications with high energy efficiency. However, UWB systems must coexist in the 3.1-10.6GHz band with a variety of high power narrow band licensed interferers and other UWB unlicensed interferers, which makes the UWB radios susceptible to the interferers. The proposed Triple-channel UWB-based cognitive radio addresses the interference challenge by allocating each channel at discrete available frequency range. The architecture is verified with statistical analysis with randomized interferer location and channel occupancy. The triple channel UWB-based cognitive radio consumes energy that is less than 10% of that of the single radio when the channel utilization is over 20%.

Dual-resolution spectrum sensing can detect narrow band interferers even at the channel boundaries. Source-follower-based LPF reduces third harmonic tone by 40dB compared to fundamental tone in order to get small stop-band ripple for spectrum sensing. Dual-resolution spectrum sensing can detect narrow band interferers even at the channel boundaries. The DC power consumption of the generator is 950μW. The active area is 0.08mm2. Modified LPF is tunable with the variation of current source and load capacitor value. The noise of the LPF is 42nV/√Hz at 1MHz for mode 0.

The proposed two stage linear tuning QVCO without SSB mixer technique enables the QPLL to accommodate higher capacity and data rate in full UWB band, 3.1 – 10.6GHz, with 23GHz/V linear VCO gain. The -59dBc reference spur is achieved with the proposed digitally background calibration for less than 1% of the CP mismatch. It mitigates the reference spur issue in spectrum sensing with 132MHz channel resolution. The 0.02–6.5GHz wide operating frequency range TSPC PDIV achieves 6.31GHz/mW power efficiency. The gated inverting keeper technique enables the PDIV to operate at 20MHz input frequency by compensating leakage current issue in deep sub-micron technology. Analysis on the minimum and the maximum frequencies of the proposed TSPC PDIVs is suitable for designing wide lock range low power frequency synthesizers.

The proposed triple-channel UWB-based cognitive radio addressed the major interferer issues of the IR-UWB transceiver design. The proposed triple channel UWB-based cognitive radio achieves 1Gb/s data rate communication even with over 30% channel occupancy by aggregate three discrete channels. Each channel data rate is 333Mb/s. Communication distance is 1m. The test chip is fabricated with 1V 65nm GP CMOS. Chip size is 2.3×2 mm^2. The test chip verified independent frequency-agile three channel cognitive radio. The lowest energy/bit is 61pJ/bit, and the highest energy/bit is 102pJ/bit. It achieves best BER of 9.2×10^{-7} and worst BER of 1.1×10^{-4}. The test chip demonstrated cognitive radio operation with intentional interferer assertion. The test chip provides lower energy/bit performance by avoiding interferers.

6.2 Contribution

This work has investigated the ways to implement a multi-channel cognitive radio in UWB band for high data rate and high energy efficiency while avoiding narrowband and wideband interferers. During the course, the following contributions have been made:

- Statistical analysis for finding optimal high data rate transceiver architecture and for defining pulse shaping, modulation method, and spectrum sensing resolution in terms of energy efficiency. Triple-channel is optimal with UWB-based cognitive radio even for over 20% channel occupancy. BPSK can minimize losses in the link budget and can obtain the maximum distance with more than hundreds Mb/s. Triangular pulse can provides optimal performance if all design parameters including BW, A, side-lobe leakage, and complexity, are considered.

- A low power spectrum sensing architecture has been investigated and implemented. For less than 1m cognitive radios, an analog wavelet-based spectrum sensing is used. Dual-Resolution wavelet-based spectrum sensing is proposed to find out narrowband and wideband interferers efficiently by changing cycle time of the triangular waveforms.

- A low power wideband QPLL has been developed with reference spur reduction technique. Low power consumption and wide band locking are achieved with the proposed two stag linear tuning ring VCO. Digitally background calibration on the charge pump mismatch enables the QPLL to get low reference spur with high VCO gain.

- A low power wideband programmable divider has been developed with true-single-phase-clock (TSPC) latches. Low power consumption is achieved with simple circuitry and layout routing. Wideband operation is achieved with the gated inverter feedback circuit. Timing analysis on the maximum and minimum cycle is investigated to tune the operation range.

- An energy efficient triple-channel UWB-based cognitive radio has been implemented in 65 nm CMOS process to demonstrate the framework. The implementation includes three different channel transmitters (including triangle-shaped data modulation circuit and an up-conversion mixer at each channel and shared antenna driver), receivers (including triangle wavelet generator, a down-conversion mixer, an analog correlation circuit, a LPF, and VGAs at each channel and shared LNA), and wideband QPLLs. It has been shown that the chip is not only lowest energy/bit without interferers but also can provide frequency-agile operation to avoid interferers in whole UWB band.

6.3 Future Work

The proposed triple-channel UWB-based cognitive radio has been verified with analog front end parts. However, mixed signal and digital processing parts need to be implemented to verify the whole system operation and to get exact power consumption of the system.

Three are three critical functions are needed for this system. The first one is low power synchronization algorithm for the QAC receiver chain in order to detect high data rate input signals properly. Another one is low power and fast spectrum sensing algorithm. In this work, linear searching is used, but new searching algorithm in the baseband can expedite spectrum sensing operation. Finally, channel equalization can enhance BER performance of the high data rate radio.

FCC regulates emission power density of the UWB radio by -41dBm/MHz in order not to interfere with other radios that use the same channel frequency band, which is underlay signal network. The cognitive radio technology on the UWB-based radio can avoid the underlay signal network, so the output power can be greater than the regulation (-41dBm/MHz). The enhanced output power can increase data rate or communication distance with high energy efficiency. It requires theoretical and statistical studies to identify the effect of the high output power UWB-base cognitive radios on other narrowband and wideband radios.

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