RF Transmitter Design for Large Array Applications

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Research Project

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Abstract

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Recent advance in wireless technologies has enabled rapid growth of data traffic. Consequently, emerging applications for mobile devices impose a big challenge on our network. To solve this problem, researchers at BWRC have proposed the “xG” vision. In our “xG” vision, we would build a network that can grow organically. Basically we would spread access points (hubs) everywhere and allow them to talk to each other to form a mesh network. Also, we would put large antenna arrays on the large surfaces around us – tables, walls, floors, ceilings, etc, so that these large antenna arrays (“eWallpaper”) could help out small terminals to do beam forming and signal processing. This report therefore focuses on the design of RF transmitters on the “eWallpaper”.

As part of the “xG” vision, the “eWallpaper” should have good spatial selectivity, low out-of-band noise and low power consumption, making the design of the RF transmitters challenging. Taking into account the limited power budget, this report investigates the design choices of the number of antennas in the whole system and on one chip. In order to reduce the out-of-band noise while minimizing the power consumption, a new topology called “current-integrating” DAC is proposed. It utilized the fact that integrating in time domain creates notches in frequency domain to cancel out the images of the signal. To improve the efficiency and scalability of the transmitter, switched-cap DC-DC converter is embedded in the “current-integrating” DAC.

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Chapter 1

Introduction and Motivation

Since its birth, the Internet has completely transformed the way we work, think, interact, entertain and do commerce, and this trend continues to transform new industries. Global mobile data traffic grew 69% in 2014, and last year's mobile data traffic was nearly 30 times the size of the entire global Internet in 2000. Cisco forecasts 24.3 Exabytes per month of mobile data traffic by 2019 (1). This imposes a big challenge on our network.

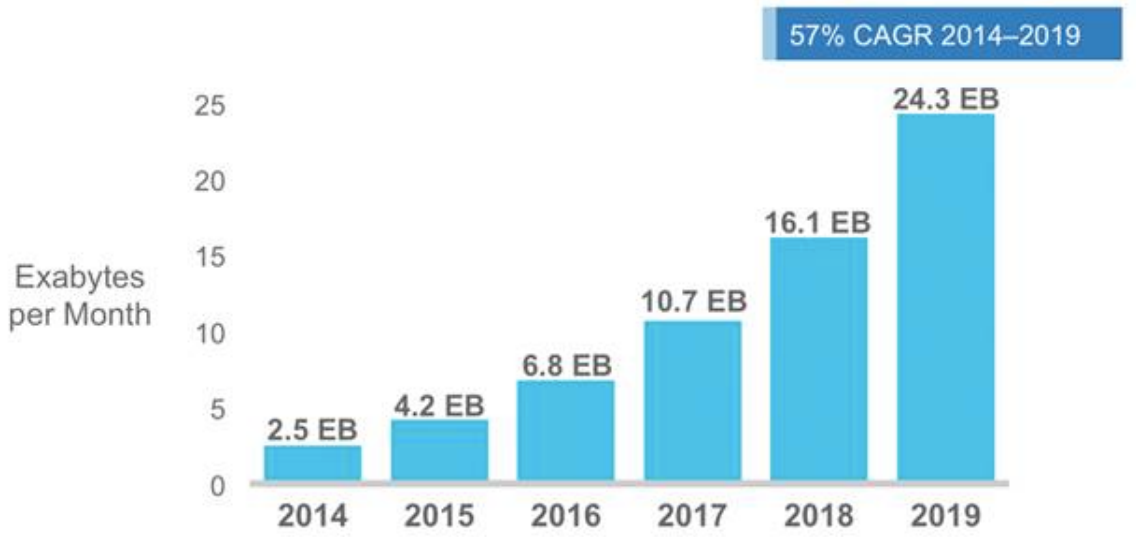


Figure 1.1 Cisco Forecasts 24.3 Exabytes per Month of Mobile Data Traffic by 2019

To solve this problem, researchers at BWRC have proposed the "xG" vision. In our "xG" vision (2), we would build a network that can grow organically with little to no user intervention or configuration. Basically we would spread access points (hubs) everywhere and allow them to talk to each other to form a mesh network. In order to reduce interference, antenna arrays should be used to create point-to-point links. One problem is that handsets have a limited surface area, while we need large arrays to achieve good spatial selectivity. However, there is plenty of area around us – tables, walls, floors, ceilings, etc. We could put large antenna arrays on these large surfaces to help out small terminals to do beam forming and signal processing. Small handsets do not need to

spread energy out into a sphere of 1km radius, but simply a few meters, to the nearest hub (potentially an "eWallpaper").

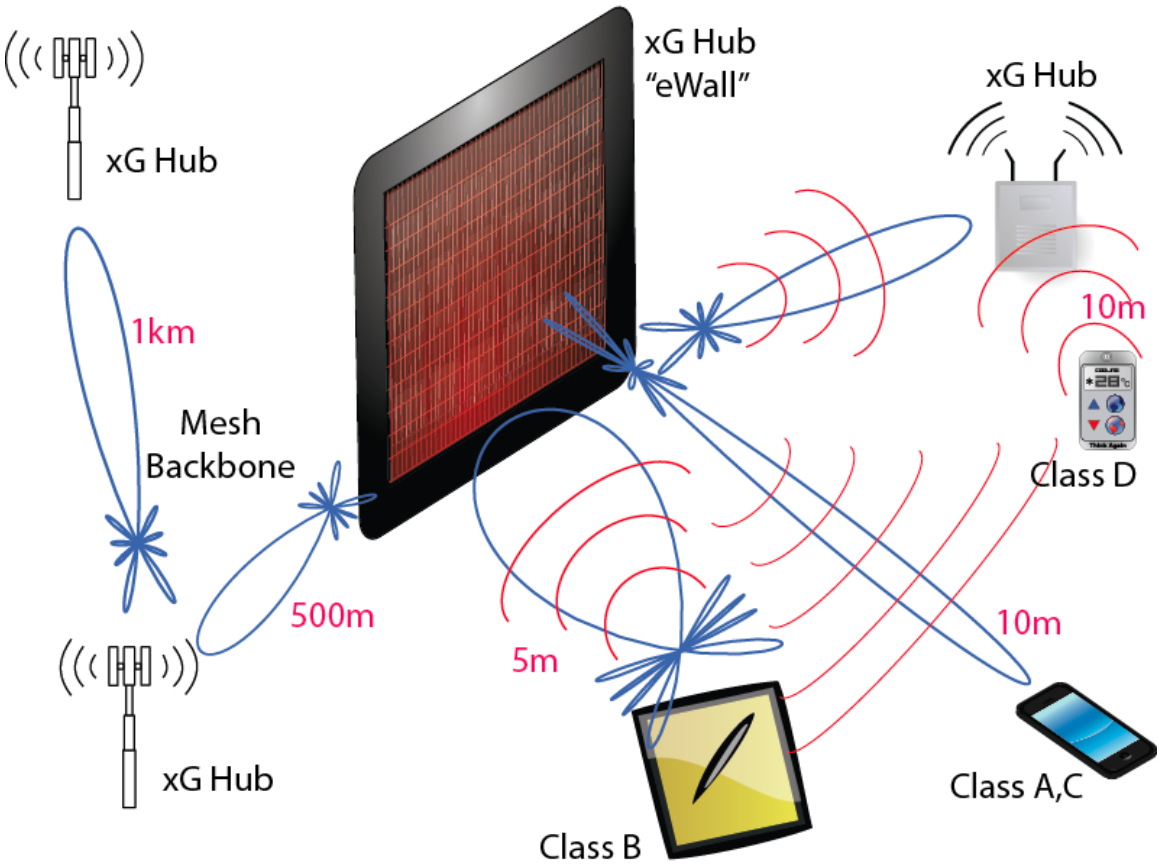


Figure 1.2 "xG" vision

According to the "xG" vision, the "eWallpaper" is a multi-antenna system that is broadband, and should be able to support multiple beams to multiple users simultaneously. To reduce interference between different users, it should have good spatial selectivity and low out-of-band noise, and low power consumption. As shown in Fig. 1.3, "eWallpaper" implements RF arrays out of a large number of digitally interconnected and controlled beam forming common module ASICs – with each of these ASICs including programmable RF front-ends, data-conversion, local digital signal processing, high-speed links and clock generation – assembled onto a flexible substrate containing printed antennas and other passive elements.

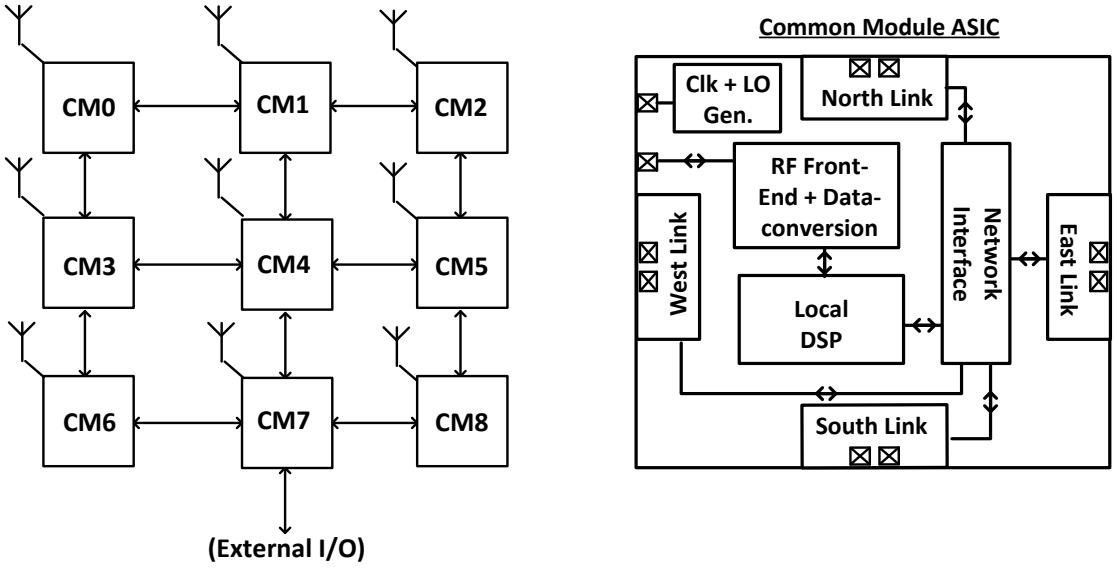


Figure 1.3 Block Diagram of the "eWallpaper"

This research focuses on the design of RF transmitter for the "eWallpaper". In Chapter 2, I develop a mathematical model to optimize power consumption at the system level. Chapter 3 discusses the circuit implementation of the RF transmitter block. Chapter 4 analyzes the power consumption of the circuit. In Chapter 5, System Verilog is used to simulate the circuit's performance.

Chapter 2

System-level Optimization

In this chapter, we will first look at the system-level trade-offs in the design of a power efficient multi-antenna array. Then we build a mathematical model and solve for numerical solutions to find power-optimized designs.

2.1 Introduction to Phased-Array

By definition, the power of an isotropic source spreads uniformly in all directions. So, at a fixed distance from the source, the power per unit (surface) area is $S_r = \frac{P_t}{4\pi R^2}$.

To get more power, we have to use a bigger area. An array (1D or 2D, flat or conformal) has an effectively larger aperture. What's more, a phased array can be steered to focus energy in the desired direction selectively.

In a phased-array system, there are multiple transceiver elements, each of them has its own antenna and phase shifter. The spacing between antennas is typically $\lambda/2$ to perform Nyquist sampling in space. (3)

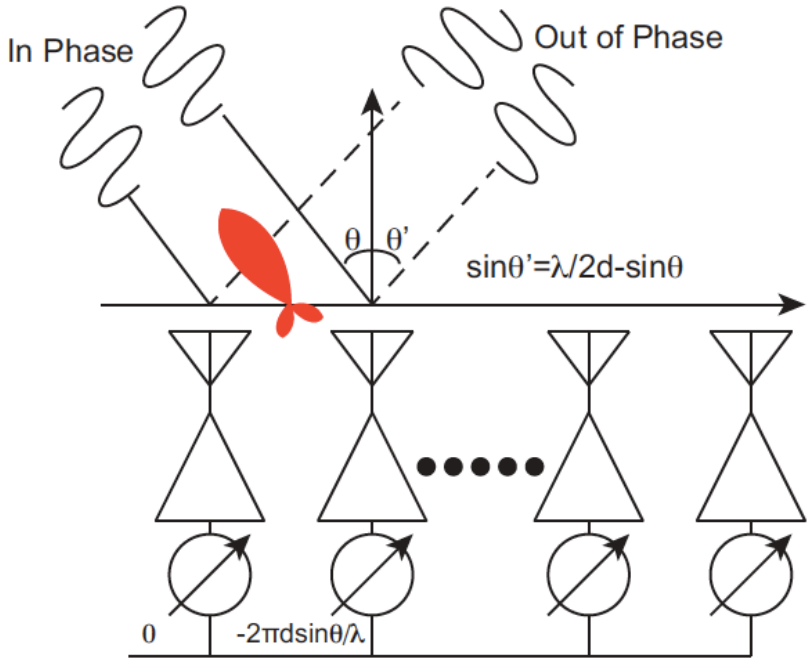


Figure 2.1 Operating principle of a phased array transmitter

Fig. 2.1 (4) illustrates the operating principle of a linear phased-array transmitter that points to incident angle θ. Each transmitter transmits its own signal through an omnidirectional antenna. Far away from the antennas in direction θ, due to the physical distance between any two nearest antennas, a phase difference $\phi = \frac{2\pi d}{\lambda}\cos\theta$ between signals from these two antennas occurs. If we intentionally shifted the phases of the signals in the transmitters by 0 and $-\phi$, the E-field generated by these two antennas will add in phase in direction θ.

In an arbitrary direction θ', note that the signal transmitted by the i[th] antenna is given by $S_i(t) = A\cos(\omega t - (i-1)\frac{2\pi d \sin\theta}{\lambda})$. Due to the time delay in space, the signal from the i[th] antenna received far away in the direction θ' is given by $S_i(t) = A\cos(\omega t - (i-1)\frac{2\pi d \sin\theta}{\lambda} - (N-i)\frac{2\pi d \sin\theta'}{\lambda})$. The Array Factor (AF) can be computed by summing all the channels:

$$AF = \left(\frac{\sin\frac{N\pi d}{\lambda}(\sin\theta' - \sin\theta)}{\sin\frac{\pi d}{\lambda}(\sin\theta' - \sin\theta)} \right)^2 .$$

Specifically, in the direction θ' that satisfies $\sin\theta' - \sin\theta = \frac{k}{N}\frac{\lambda}{d}$ (k=1,2,…,N-1), AF=0, meaning that the energy delivered in these directions is zero.

Similar behavior occurs on the receiver side. In the case of two elements, the received signal in the desired direction is enhanced by a factor of 4 compared with the single element case. Assuming the noise from two different antennas is uncorrelated, they are thus added in power (rather than in voltage). The noise power therefore doubles versus a single element case. The net effect is that the SNR is improved by a factor of 2. In a generalized case where N_{RX} elements are employed in the receiver, SNR will be enhanced by N_{RX}.

2.2 Trade-offs to Support Multiple antennas per ASIC

In Fig. 1.3, for simplicity, it was shown that each ASIC supports one antenna. In reality, each ASIC could support multiple antennas to reduce overall power and improve area efficiency.

Consider a 1000 antenna array, if each ASIC supports one antenna, there will be 1000 ASICs in the system. As mentioned in chapter 1, each ASIC should include data-conversion, clock generation and local digital signal processing circuits, thus part of the total power (power that is consumed in these blocks (P_{ovhd})) will grow linearly with the number of ASICs. Besides, the ASICs talk to each other through digital high-speed links. The number of high-speed links will also grow with the number of ASICs as well. In this case, the power consumption of all these blocks is $1000P_{ovhd} + 1000P_{link}$ if we put all the ASICs in a line (for the sake of simplicity for now). On the other extreme, if we use one ASIC to support all 1000 antennas, it could be imagined that routing from the ASIC to the 1000 antennas is messy and the distance between antennas and the ASIC is very far, so the loss of the signal to reach each antenna is large, and the RF front-end circuits need to output a very large power in order to get desired EIRP in space.

Based on the above discussion, it is obvious that for a large antenna array, there will be a trade-off between antenna efficiency and power consumption of clock generation, local DSP and high-speed links. We will build a mathematical model for this trade-off in the next section.

2.3 Mathematical Model for Power Consumption

In this section, we will first build a mathematical model for the total power consumed in a multi-antenna array. We can then solve for the conditions that minimize the total power.

Consider a 2D array where the ASICs are arranged in an R*C rectangular grid. Each ASIC supports A antennas, and uses up to 4 high-speed links to transmit/receive data to/from its neighbors. From the discussion in the last section, it is clear that the power consumption of all circuits in the system can be grouped into 3 categories: 1) local DSP, data conversion and clock generation, 2) high-speed links, 3) RF front-end. We will next establish mathematical equations for the 3 categories respectively.

a) Local DSP and clock generation

If each ASIC consumes $P_{ovhd,ASIC}$ in its local DSP and clock generation circuits, the whole array consumes $RCP_{ovhd,ASIC}$ due to these components.

b) High-speed links

There are generally two ways to construct the high-speed links in the system: "complete" and "incomplete". The "complete" structure looks like Fig. 1.3, in which each ASIC uses 4 transceivers to talk to all its nearest neighbors, so there are $2RC-R-C$ links in a "complete" array.

However, "complete" array is redundant, thus not efficient. Sometimes designers may prefer an "incomplete" array, in which each ASIC doesn't talk to all its nearest neighbors. From any ASIC, it is possible to reach any other ASIC in the array. An example of an incomplete array is shown in Fig. 2.2, it is one of the simplest structures one could construct for a 9-ASIC array. There are *RC* links in the simplest "incomplete" array.

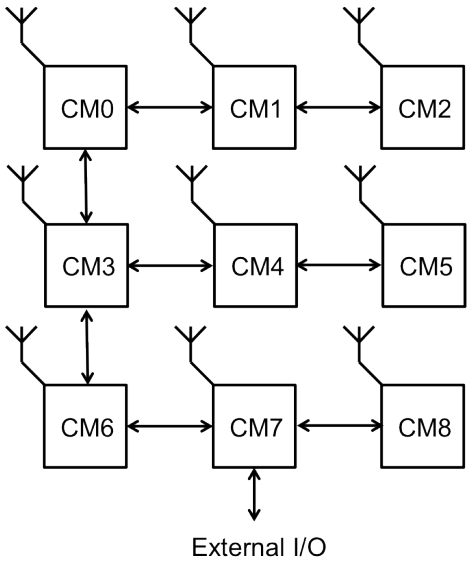


Figure 2.2 An "incomplete" RF array

c) RF front-end

Clearly, the total power consumption of RF front-ends is $RCAP_{DC,TX}$, where $P_{DC,TX}$ is the DC power consumed by one RF transmitter. To translate $P_{DC,TX}$ into design specifications, we need an inspection of the design of the RF front-ends.

i) TX Efficiency

Most TX architectures can be simplified as shown in Figure 2.3. The power consumed in one TX consists of power dissipated in the power amplifier as well as overhead power dissipated by modulation, data conversion, phase shifting, etc. $P_{DC,TX} = P_{ovhd,ant} + P_{DC,PA}$. Power efficiency of a power amplifier is defined as: $\eta = \frac{P_{out,RF}}{P_{DC,PA}}$. In most cases, η is a function of $P_{out,RF}$.

We can then substitute $P_{DC,TX}$ in terms of RF output power and PA efficiency: $P_{DC,RF} = P_{ovhd,ant} + \frac{P_{out,RF}}{\eta}$.

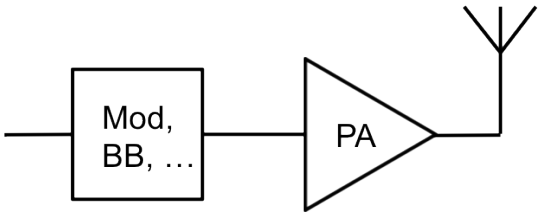


Figure 2.3 RF Transmitter Block Diagram

ii) Routing loss

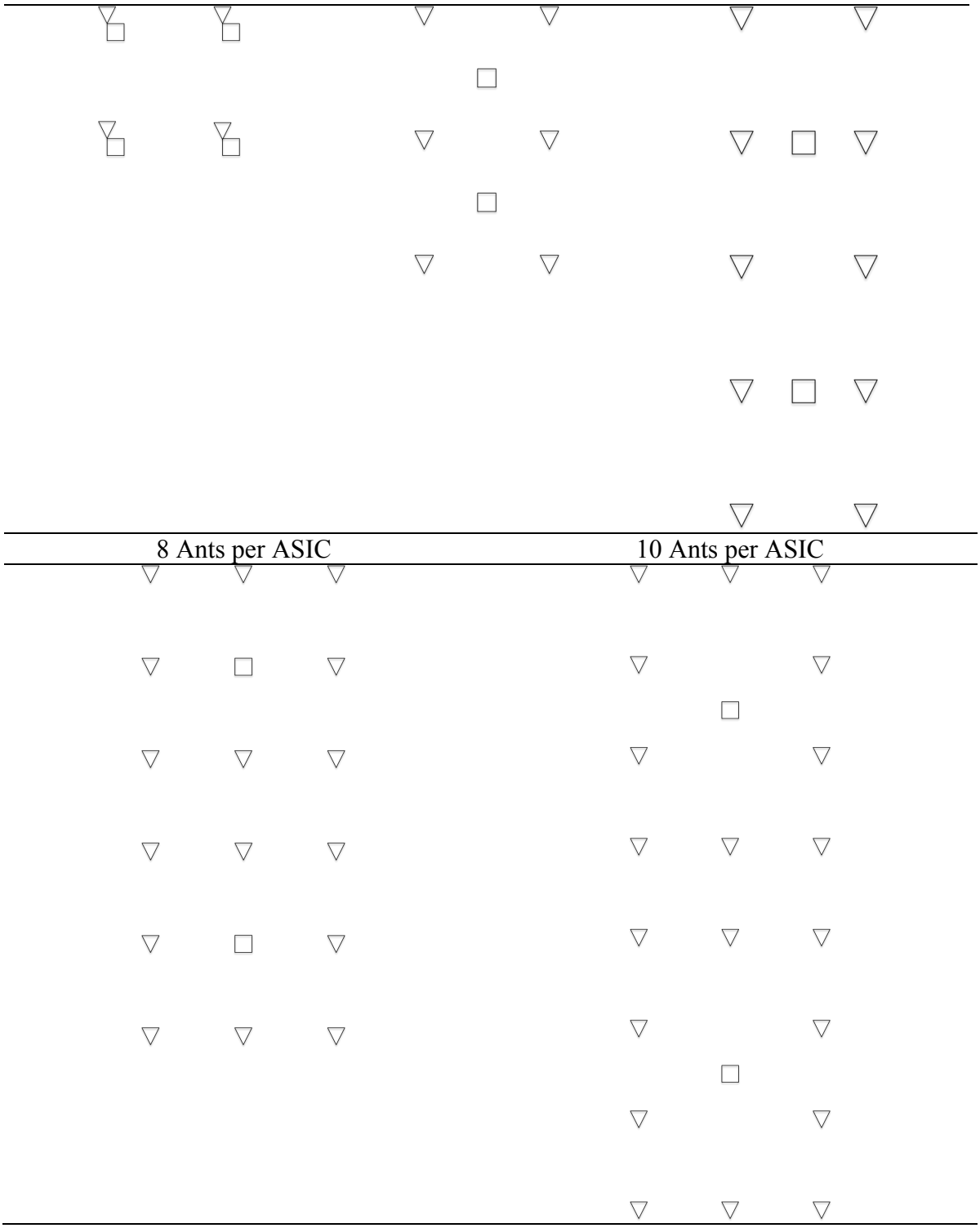
The output of the TX will be attenuated when it arrives at the antenna due to the losses of the routing. We could characterize the loss in terms of decibels per unit length. Here we define the antenna loss to be k dB per half-wavelength, which is equivalent to:

$P_{radiated} = P_{out,RF} 10^{-kl\frac{2}{\lambda}}$, where l is the antenna length. Then

$P_{DC,RF} = P_{ovhd,ant} + P_{radiated} \cdot 10^{kl\frac{2}{\lambda}} \frac{1}{\eta}$.

Clearly l increases with A (number of antennas each ASIC supports). To better illustrate this dependency, floorplans of ASICs with 1~10 antennas are shown in Table 2.1. Squares in the figure represent ASICs, and triangles represent antennas.

1 Ant per ASIC	4 Ants per ASIC	6 Ants per ASIC



8 Ants per ASIC	10 Ants per ASIC

Table 2.1 Floorplan of ASICs with 1~10 antennas

We summarize part of the results in Table 2.2.

A	Largest l (λ /2)
2~4	$1/\sqrt{2}$
5~6	$\sqrt{5}/2$
7~8	$\sqrt{2}$
9~10	$\sqrt{13}/2$

Table 2.2 Largest distance between antenna and ASIC

When A is not too large, l(A) can be approximated by $l(A) \approx \frac{\sqrt{A}-1}{\sqrt{2}}\frac{\lambda}{2}$.

iii) Array Gain

In this section, let's assume linear array at broadside, then, as discussed in section 2.1, the array factor (AF) is $(R*C*A)^2$, where (R*C*A) is the number of antennas in the array. The radiated power of one antenna equals to $P_{radiated} = \frac{EIRP}{(RCA)^2}$.

In summary, the total power consumption of RF front-ends is $RCAP_{DC,TX}$, and $P_{DC,RF} = P_{ovhd,ant} + \frac{EIRP}{(RCA)^2}\cdot 10^{kl\frac{2}{\lambda}}\frac{1}{\eta} = P_{ovhd,ant} + \frac{EIRP}{(RCA)^2}\cdot 10^{k\frac{\sqrt{A}-1}{\sqrt{2}}}\frac{1}{\eta}$. The total power consumed is therefore: $P_{total} = RCP_{ovhd,ASIC} + RCP_{link} + (RCA)P_{ovhd,ant} + \frac{EIRP}{RCA}\cdot 10^{k\frac{\sqrt{A}-1}{\sqrt{2}}}\frac{1}{\eta}$.

2.4 Optimization Results

Let the total number of antennas in the array be N, then we can rewrite P_{total} as:

$$P_{total} = \frac{N}{A}P_{ovhd,ASIC} + (\frac{N}{A}-1)P_{link} + NP_{ovhd,ant} + \frac{EIRP}{N}10^{kl(A)\frac{2}{\lambda}}\frac{1}{\eta}.$$

In reality, $P_{ovhd,ASIC}$, $P_{ovhd,ant}$, P_{link} and η all depend on N and A. However, we could assume them to be constant to get an insight into how we choose N and A in the first step.

For a given N, the optimal A is given by the following equation:

$$\frac{\ln(10)k}{2\sqrt{2}} A^{3/2} 10^{k\frac{\sqrt{A}-1}{\sqrt{2}}} = \frac{\eta N^2}{EIRP}(P_{ovhd,ASIC} + P_{link}) .$$

Recall that $\frac{EIRP}{N^2}$ is power radiated per antenna, $\frac{EIRP}{\eta N^2}$ is the DC PA power assuming zero antenna loss. The equation matches with our intuition – if the overhead power consumed in each ASIC or high-speed link is large compared with the PA power, we would prefer to have more antennas per ASIC because it costs a lot of power to distribute antennas onto different ASICs. On the other hand, if antenna loss is high (k is big), we would prefer to have fewer antennas per ASIC in order to shorten the routing from the ASIC to the antennas.

2.5 Numerical Optimization Results for 1st design prototype

For our first design prototype, we aim to meet WiFi standard. Based on some reasonable guesses of circuit performance (5), numerical solutions of this optimization problem are shown in Figure 2.4.

EIRP	30 dBm
Carrier Frequency	2.4 GHz
Bandwidth	20 MHz
Number of bits	10-bit I, 10-bit Q
Link efficiency	1 pJ/bit
P_{ovhd} (per antenna)	2 mW
P_{ovhd} (per ASIC)	2 mW
PA efficiency	10%
Antenna loss per half-wavelength	0.5 dB

Table 2.3 Design specifications of 1st design prototype

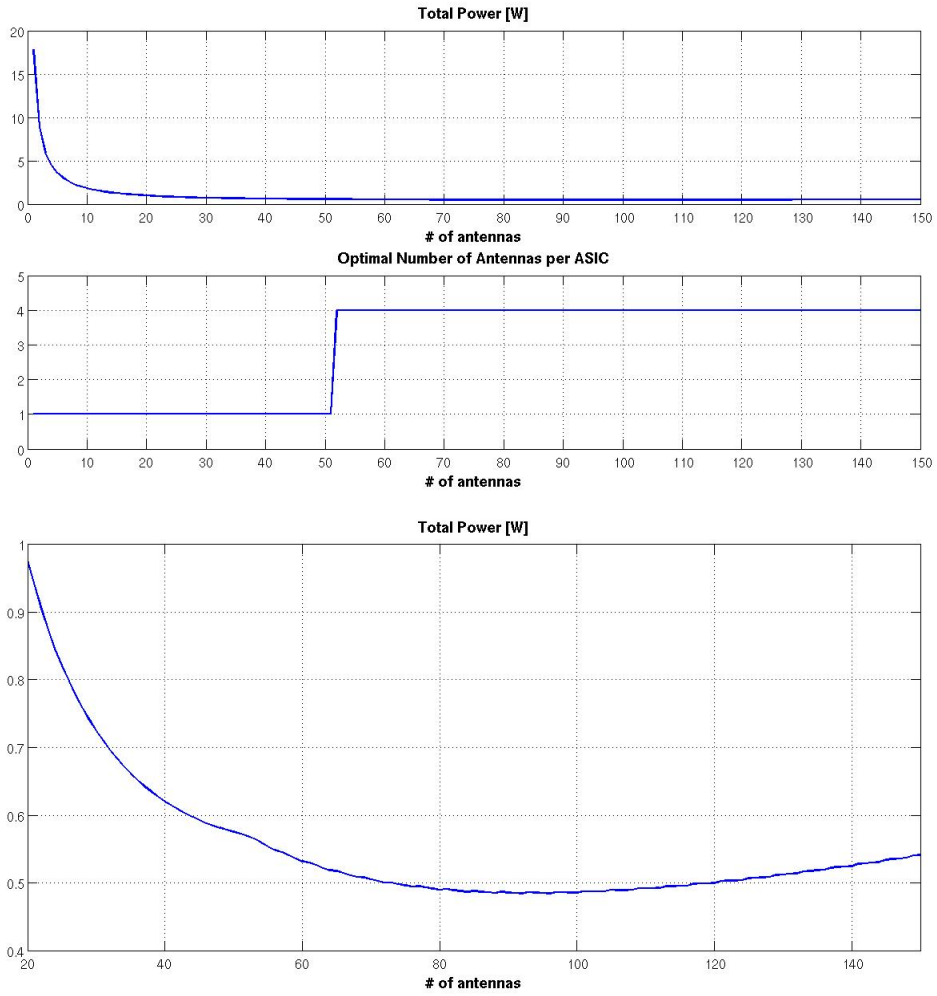


Figure 2.4 Total power consumption v.s. Number of antennas in the array. (b) Optimal number of antennas per ASIC v.s. Number of antennas in the array. (c) Zoomed-in of (a).

Figure 2.4 shows that total power consumption versus total number of antennas on the "eWallpaper" curve is relatively flat when N>40. The minimum total power is 0.484W when N=92. In our 1st design prototype, we choose N=64 for the sake of simplicity, with a resulting P_{total} = 0.519W (7% bigger than the minimum). In this design, P_{link} = 1pJ/bit * 20bit (10-bit I, 10-bit Q) * 20MHz = 0.4mW, and $P_{ovhd,ASIC}$ is dominated by clock generation circuits, estimated to be around 2mW. When N < 52, ($P_{ovhd,ASIC}$ + P_{link}) is small compared to $\frac{EIRP}{\eta N^2}$, therefore it costs a small portion of power to have more ASICs in the array, and the best choice is to have only 1 antenna per ASIC. When N > 52, because the output power of each antenna is smaller, relatively speaking, it costs more to support more ASICs in the array. The best choice for this 64-antenna array is to have 4 antennas per ASIC.

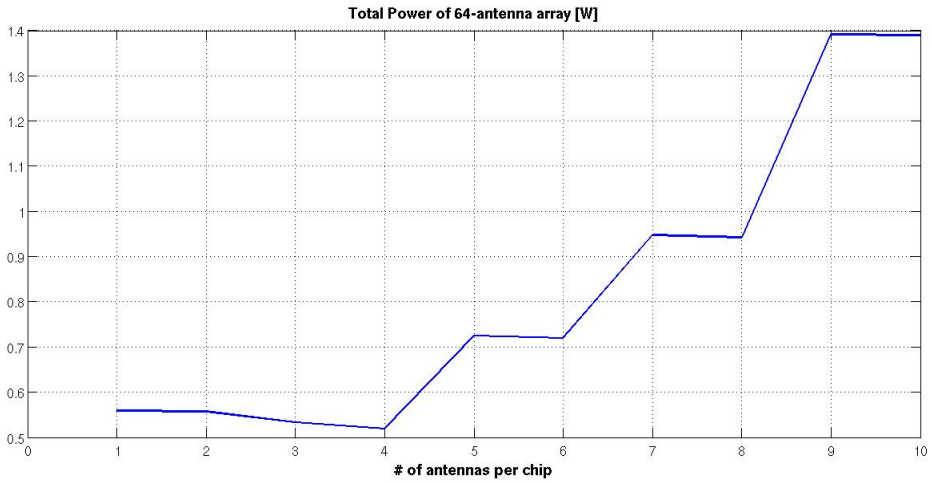


Figure 2.5 Power Consumption of a 64-antenna array v.s. Number of antennas per ASIC

Figure 2.6 shows the diagram of the 64-antenna array. The blue squares represent the ASICs. The yellow lines show the power distribution underneath the ASICs. There are 16 ASICs in this diagram and each ASIC supports 4 antennas.

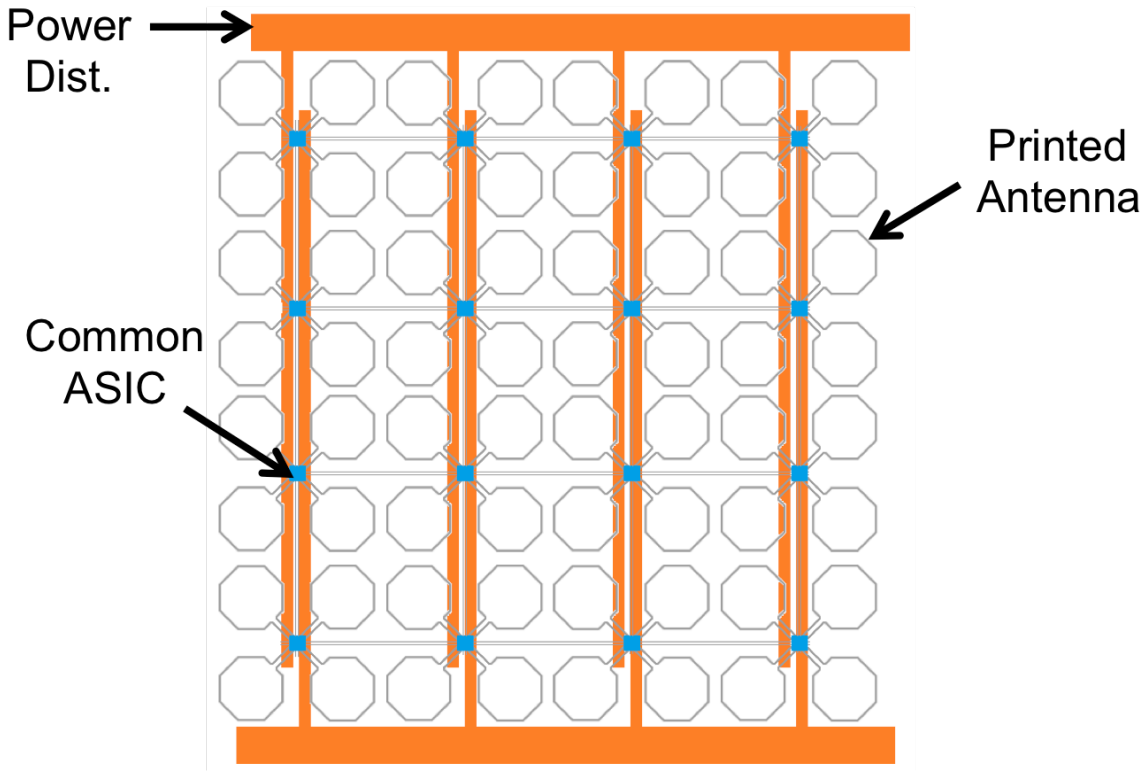


Figure 2.6 System Diagram of "eWallpaper"

Chapter 3

Circuit Implementation of RF Transmitter

In this chapter, we will discuss the circuit design of the RF transmitter for our first design prototype of the "eWallpaper". As mentioned in Chapter 1, the "eWallpaper" should have good spatial selectivity, low out-of-band noise and low power consumption. Good spatial selectivity is achieved by using a lot of antennas (64 in this version). Our primary goal is then to achieve low out-of-band noise and minimize the power consumption.

Figure 3.1 shows the block diagram of the RF TX. It consists of an oversampling "current-integrating DAC" with switched-cap DC-DC converter embedded, an analog reconstruction filter and a 25% duty-cycle passive mixer. Details in each block will be discussed in the next sections.

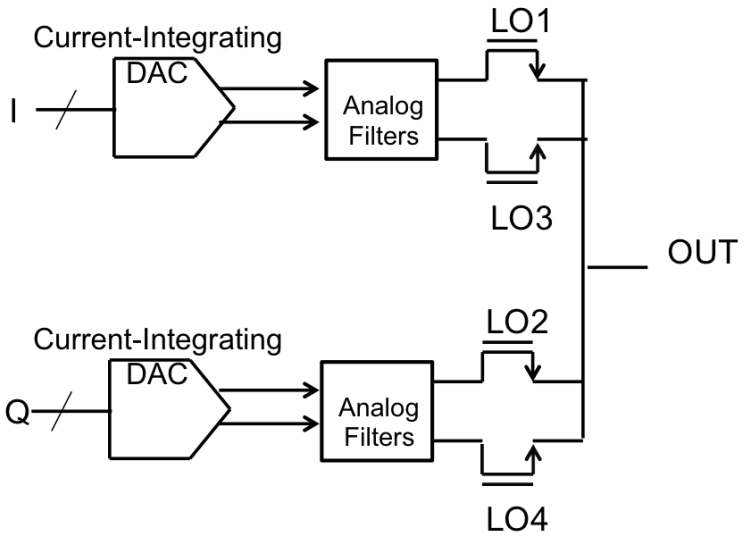


Figure 3.1 TX Block Diagram

3.1 Mixer

For a 64-antenna array, each antenna only needs to output -6dBm power to achieve 30dBm EIRP. For most state-of-art power amplifiers, efficiency (η) at this output power level is very low. It may in this case simply be more power efficient to use the output of the mixer in order to avoid extra stages, each with some minimum level of power dissipation that degrades the overall efficiency.

In transmitter applications, two techniques have proven to be effective in the implementation of mixers with high dynamic range:

1) Use a device that has a known and controlled nonlinearity.
2) Switch the baseband signal path on and off at the LO frequency.

The nonlinear mixer can be applicable at any frequency where the device presents a known nonlinearity. It is the only approach available at the upper mm-wave frequencies. When frequencies are low enough that good switches can be built, it is more straightforward to build a switching mixer. For our 1st design prototype, we chose the switching mixer.

Active or passive implementations can be used for the mixer. Each has its advantages and disadvantages. Compared with active mixers, passive mixers dissipate no DC power, except their clock generation circuits. Also, passive mixers can operate with much lower voltage supplies than their active counterparts. Therefore, for this specific design, passive mixer is the most suitable choice.

Our proposed block diagram of the transmitter and the timing diagram of the LO switches are shown in Figure 3.2. In this topology, we chose an IQ direct-conversion TX using 25% duty-cycle passive mixers. (Mirzaei, Murphy, & Darabi, 2011) (He & Sinderen, 2009) (He, Sinderen, & Rutten, 2010)

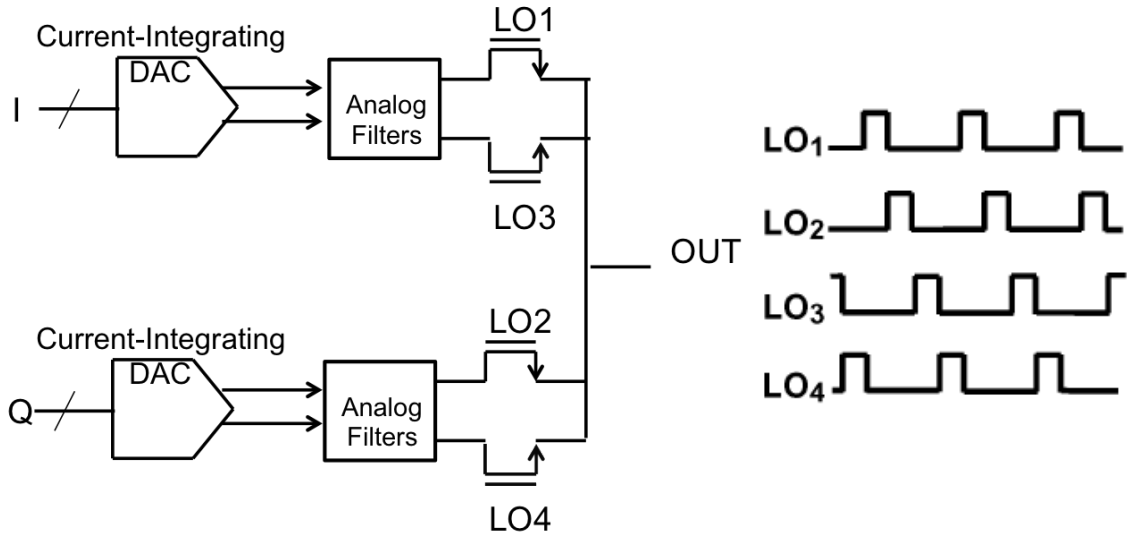


Figure 3.2 RF TX Block Diagram

Conventionally, an IQ direct-conversion passive mixer is usually driven by 50% duty-cycle clocks. However, due to inevitable unwanted interaction between the I and the Q baseband sections, the RF sides of the mixers cannot be shorted together. This is because at any given moment one mixer switch from the I channel and another mixer switch from the Q channel are on. Instead, the two RF sides of the mixers need to be buffered by two separate transconductors. The outputs of these transconductors are then hardwired

together, which add the up-converted I and Q RF currents together. This arrangement has a number of shortcomings. Typically the transconductor stages need to embed a portion of gain controllability of the transmitter which is usually done by dividing them into smaller cells. The transconductor units in the I and Q paths may not match well, which can result in a poor image-rejection ratio (IRR). Indeed, in this transmitter scheme, the IRR would be a function of gain control. To eliminate the need for two separate RF drivers, we use 25% duty-cycle clocks to drive the passive mixer. With the 25% passive mixers, at any given moment, only the I or the Q channel is connected to the RF side. Therefore, interaction between the I and Q baseband sections is minimized too.

3.2 Oversampling DAC and Digital Interpolation Filter

At the beginning of this chapter, it is mentioned that we built an oversampling "current-integrating" DAC. In this section, we will first explain why and how we built an oversampling DAC, and in the next two sections we will explain why and how we built a "current-integrating" DAC and why and how we embedded switched-cap DC-DC converter in the DAC.

Oversampling and digital filtering are commonly used in ADC to ease the requirements on the antialiasing filter that precedes the ADC. The concept of oversampling and interpolation can be used in a similar manner in high speed DACs used in communications applications.

The output of a reconstruction DAC can be represented as a series of rectangular pulses whose width is equal to the reciprocal of the clock rate (Kester, 2009).

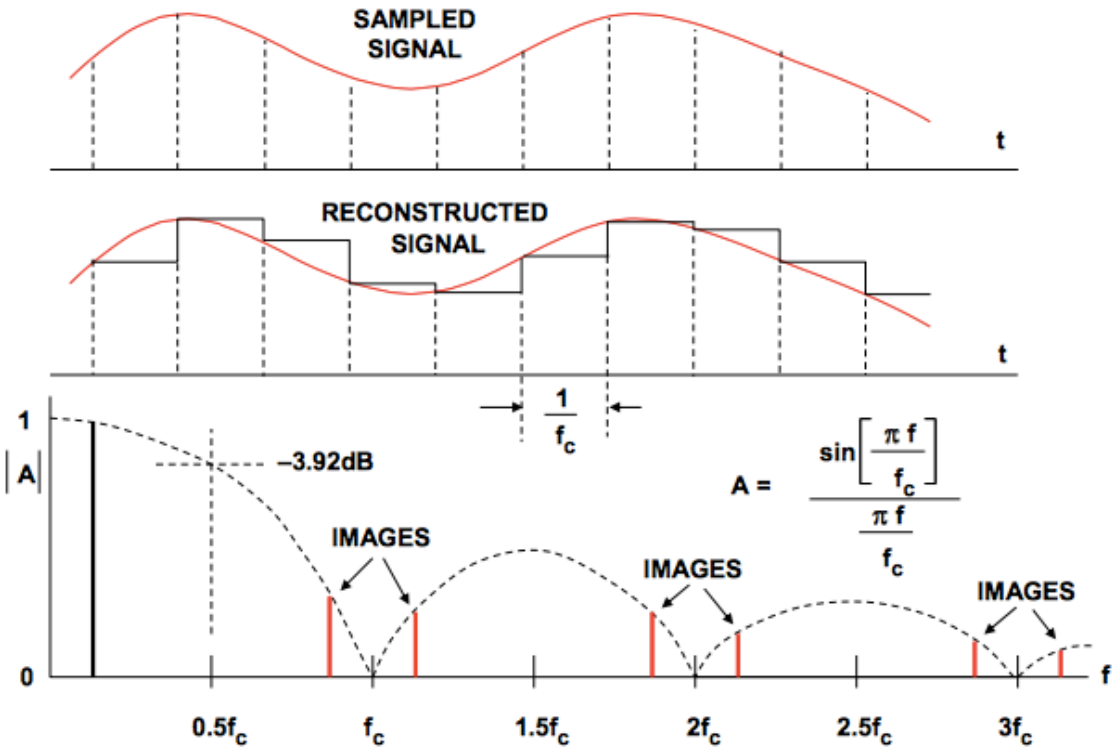


Figure 3.3 Unfiltered DAC with sin(x)/x roll-off

The basic concept of an oversampling/interpolating DAC is shown in Figure 3.4. (Kester, 2009). The N-bit words of input data are received at a rate of f_c. The digital interpolation filter is clocked at an oversampling frequency of Kf_c, and inserts the extra data points. In the Nyquist case shown in Figure 3.3, the requirements on the analog anti-imaging filter can be quite severe. By oversampling and interpolating, the requirements on the filter are greatly relaxed as shown in Figure 6.3.

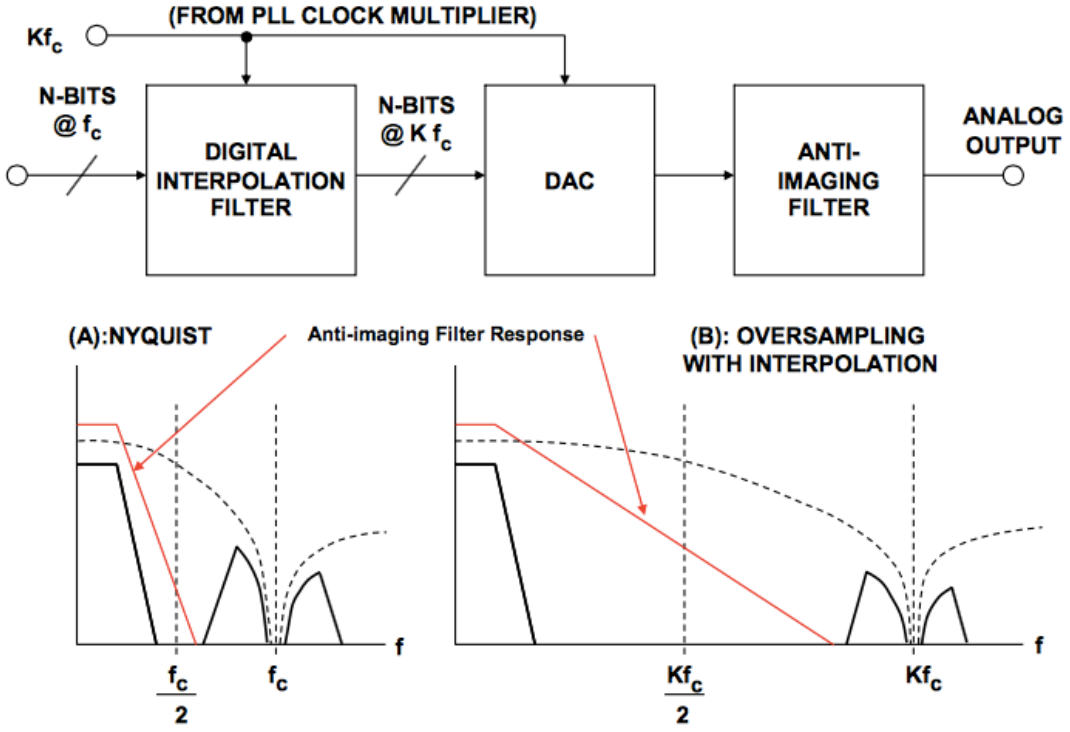


Figure 3.4 Basic concept of oversampling DAC

In this application, the filter is called an interpolation filter. Its design is discussed below. (Strang & Nguyen, 1997) (Stoica & Moses, 1997)

Let X(f) be the Fourier transform of any input waveform x(t), whose samples at some interval T, equal the x[n] sequence. Then the discrete-time Fourier transform (DTFT) of the x[n] sequence is the Fourier series representation of a periodic summation of X(f):

$$\sum_{n=-\infty}^{\infty} x(nT)e^{-i2\pi fnT} = \frac{1}{T}\sum_{k=-\infty}^{\infty} X(f-\frac{k}{T}).$$

When T has units of seconds, f has units of hertz. Sampling L times faster (at interval T/L) increases the periodicity by a factor of L: $\frac{L}{T}\sum_{k=-\infty}^{\infty} X(f-k\frac{L}{T})$, which is also the desired result of interpolation. An example of both these spectrum is depicted in the top two graphs. (Tan, 2008)

When the additional inserted samples are all zeros, they increase the data rate, but they have no effect on the frequency spectrum until the zeros are replaced by the interpolation filter. Many filter design programs use frequency units of cycles/sample, which is achieved by normalizing the frequency axis, based on the new data rate (L/T). The result is shown in the third graph of Figure 3.5. Also shown is the passband of the interpolation filter needed to make the third graph resemble the second one. Its cutoff frequency is

0.5/L. In terms of actual frequency, the cutoff is 0.5/T Hz, which is the Nyquist frequency of the original x[n] sequence.

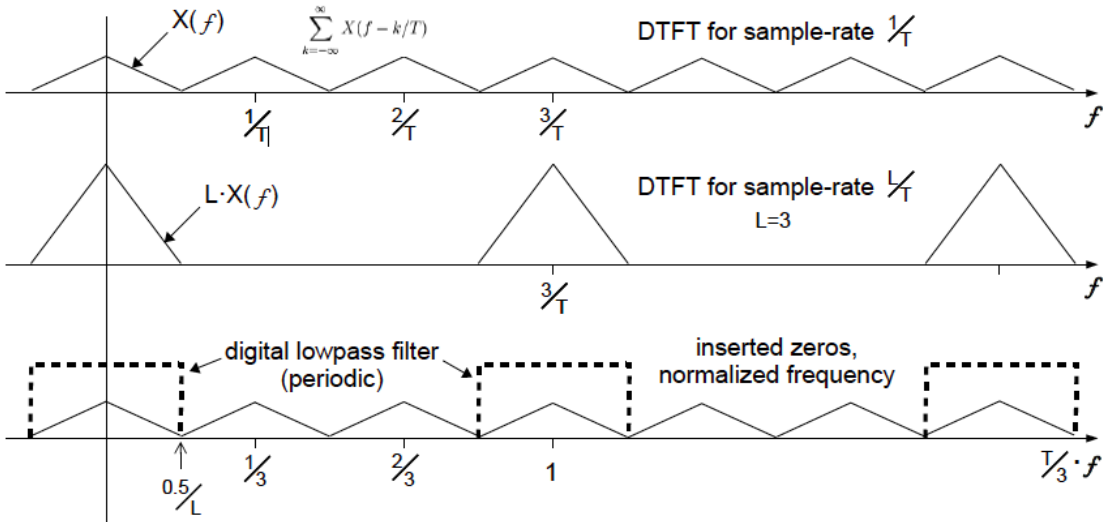


Figure 3.5 Spectral depictions of zero-fill and interpolation by lowpass filtering

When the interpolation filter is an FIR type, its efficiency can be improved, because the zeros contribute nothing to its dot product calculations. It is an easy matter to omit them from both the data stream and the calculations. The calculation performed by an efficient interpolation FIR filter for each output sample is a dot product:

$$y[j+nL] = \sum_{k=0}^{K} x[n-k] \cdot h[j+kL], j = 0,1,...L-1,$$

where the $h[\cdot]$ sequence is the impulse response, and K is the largest value of k for which h[j+kL] is non-zero.

3.3 Current-Integrating DAC

In section 3.2, we introduce that by oversampling/interpolating, the nearest image is moved from f_c to Kf_c, thus relaxing the requirements on the antialiasing filter. In this section, we will propose a "current-integrating" DAC topology that will move the nearest image from Kf_c to $2Kf_c$, thus further relax the requirements on the antialiasing filter. In other words, if we use the same antialiasing filter, this topology will have lower out-of-band noise compared with a tradition current DAC.

This idea first comes from the knowledge that integration in time domain (integration window is T_{int}) equals to a notch at $f=1/T_{int}$ in frequency domain. A straightforward circuit implementation of the integration function is shown in Figure 3.6.

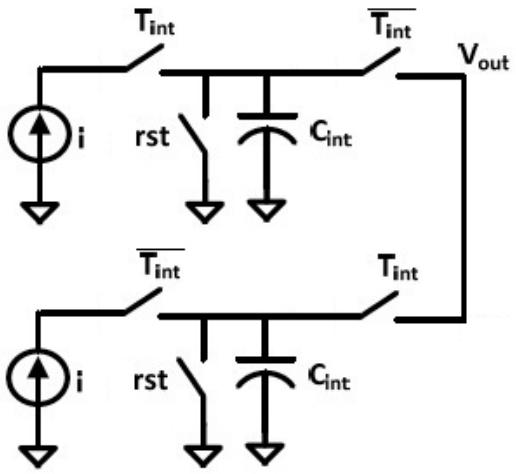


Figure 3.6 Circuit performing integration

During Phase 1 (Integration), the output current of the DAC integrates onto a capacitor C_{int}. Then in Phase 2 (Sampling), the voltage on C_{int} is sampled by the following stage. Finally in Phase 3 (Reset), the two plates of C_{int} are shorted together so that the C_{int} is discharged.

However, this circuit doesn't perform a perfect integration. It is equivalent to taking the samples of function $V_{\text{int},ideal}(t) = \int_{t}^{t+T_{\text{int}}} \frac{i(t)}{C_{\text{int}}} dt$ with sampling frequency $f_{samp} = \frac{1}{T_{\text{int}}}$. Taking the Fourier transform of $V_{int,ideal}(t)$, its spectrum will be:

$$V_{\text{int},ideal}(f) = \frac{i(f)}{C_{\text{int}}} T_{\text{int}} \frac{\sin(\pi f T_{\text{int}})}{\pi f T_{\text{int}}},$$

where I(f) is the spectrum of the DAC output current.

The output spectrum of sampled signal $V_{int,ideal}(t)$ (spectrum $V_{int,ideal}(f)$) with frequency f_{samp} is:

$$V_{dac,out}(f) = \frac{\sin(\pi f / f_{samp})}{\pi f / f_{samp}} \cdot e^{-j\pi f / f_{samp}} \sum_{n=-\infty}^{\infty} V_{\text{int},ideal}(f - n f_{samp}).$$

Assuming I(f) is white in frequency domain, the top plot in Figure 3.7 shows $V_{\text{int},ideal}(f - nf_{samp})$ when n=-3~3. If it was a perfect integration, the transfer function would have simply been the yellow curve in this plot. In this example, integration time is 3.125 ns, the notch frequency is therefore 320MHz. However, because of the sampling behavior, this transfer function should add with all its images at f_{sample}, $2f_{sample}$, etc. The second plot in Figure 3.7 shows the sum result. It is almost a white spectrum and the notches disappear. The bottom plot shows the output spectrum of this DAC. It only exhibits a zero-order-hold characteristic.

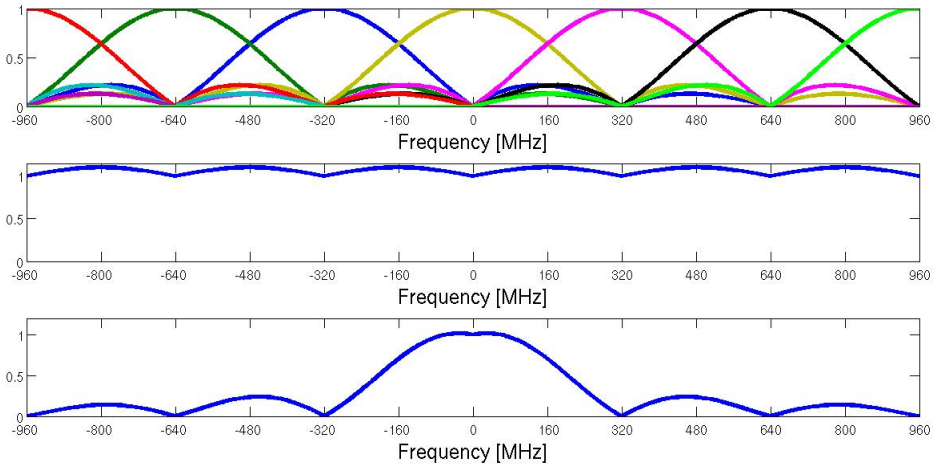


Figure 3.7 Transfer function of the integration circuit

We compare the spectrum with a zero-order-hold current DAC output spectrum. At 310MHz, zero-order-hold current DAC and this DAC have 29.84dB and 29.75dB attenuation respectively. At 330MHz, zero-order-hold current DAC and this DAC have 30.37dB and 30.29dB attenuation respectively. They basically have the same output spectrum.

In order to solve this problem, we could sample the integration result with higher frequency. $V_{\text{int},ideal}(f - nf_{samp})$ when n = -1~1, $\sum_{n=-\infty}^{\infty} V_{\text{int},ideal}(f - nf_{samp})$, and DAC' $V_{dac,out}(f)$ when T_{int}=1/320MHz and f_{samp}=640MHz are shown below in Figure 3.8.

It is clear from the plots that because the sampling frequency is twice of the notch frequency caused by the integration function, summing all the images doesn't change the notches.

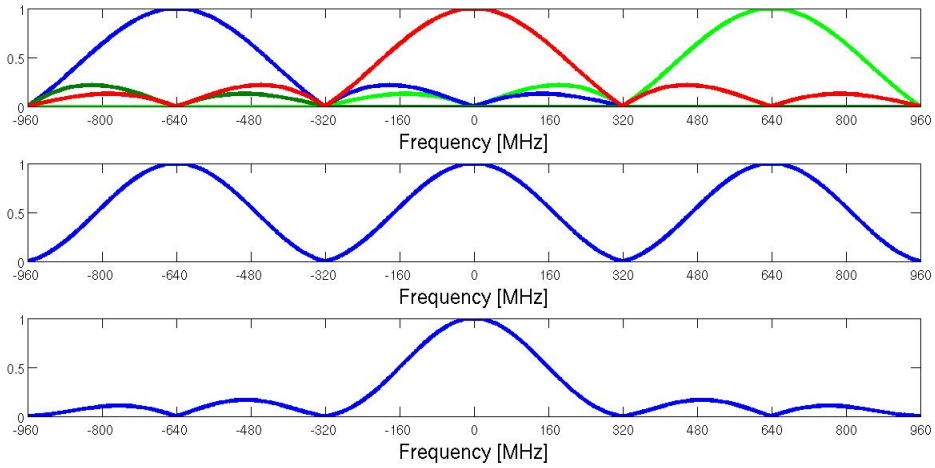


Figure 3.8 Transfer function of the revised integration circuit

It is clear from the plots that because the sampling frequency is twice of the notch frequency caused by the integration function, summing all the images doesn't change the notches. The DAC output spectrum will have more attenuation around 320MHz. At 310MHz, the output of the DAC has 41.79dB attenuation. At 330MHz, it has 42.29dB attenuation. This result is 12dB better than the result when f_{samp}=320MHz. The circuit implementation and timing diagram of the switches are shown below.

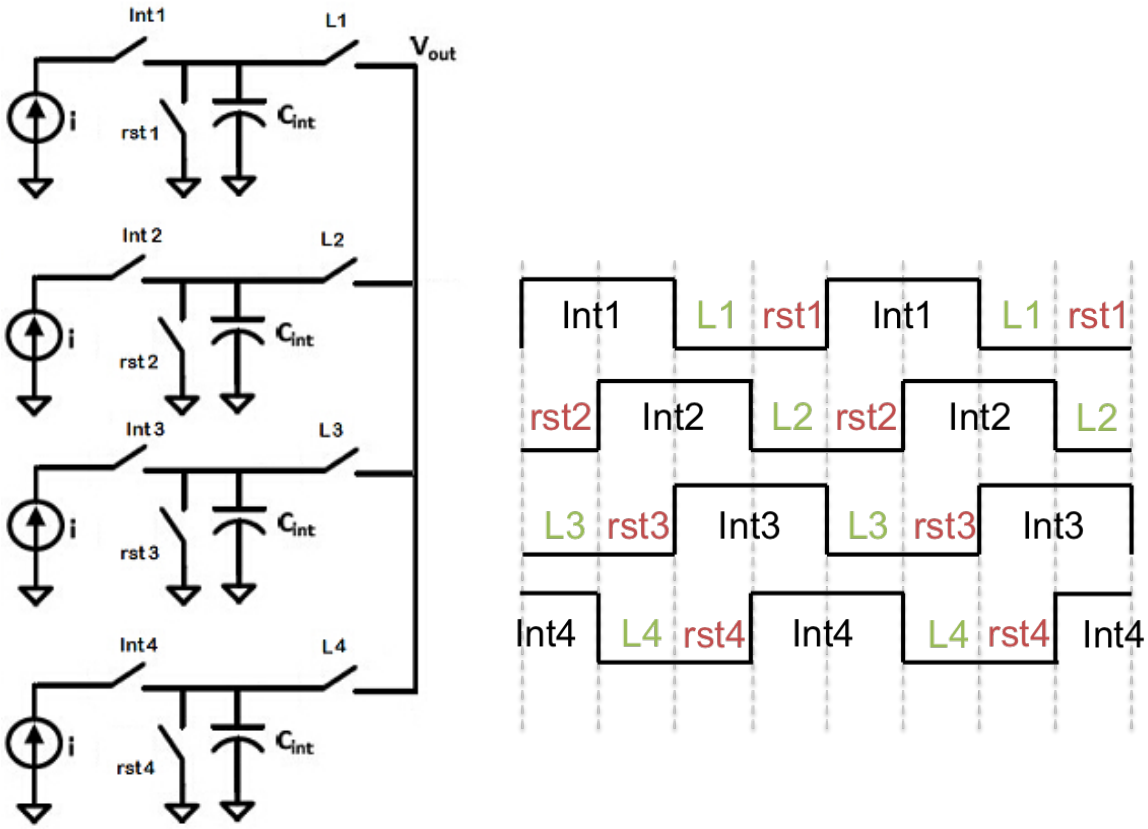


Figure 3.9 Circuit implementation and timing diagram of the integration circuit

Notice that we need two physically separate current sources in this topology. Because the "integration" phases of the first and third branches are completely complimentary, they could share 1 current source, and the second and the fourth could share the other current source.

3.4 Embedded Switched-Cap DC-DC Converter

There are two problems with the "current-integrating" DAC.

1) Its maximum output RF voltage is $V_{RF,fund,\max} = \frac{8}{\pi} \frac{R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{T_{\text{int}}} \frac{(\frac{V_{dd}}{2} - n_s V_{dsat})}{i_I}} (\frac{V_{dd}}{2} - n_s V_{dsat})$. It is impossible to output any voltage higher than $\frac{8}{\pi}(\frac{V_{dd}}{2} - n_s V_{dsat})$.
2) When its target output power is low, the efficiency is bad because it only uses a small portion of V_{dd}.

To solve these two problems, we embedded a switched capacitor DC-DC converter to the TX. shows the modified circuit. An SC converter with only two capacitors are drawn for simplicity.

The detailed block diagram of the RF TX baseband is shown in Figure 3.10.

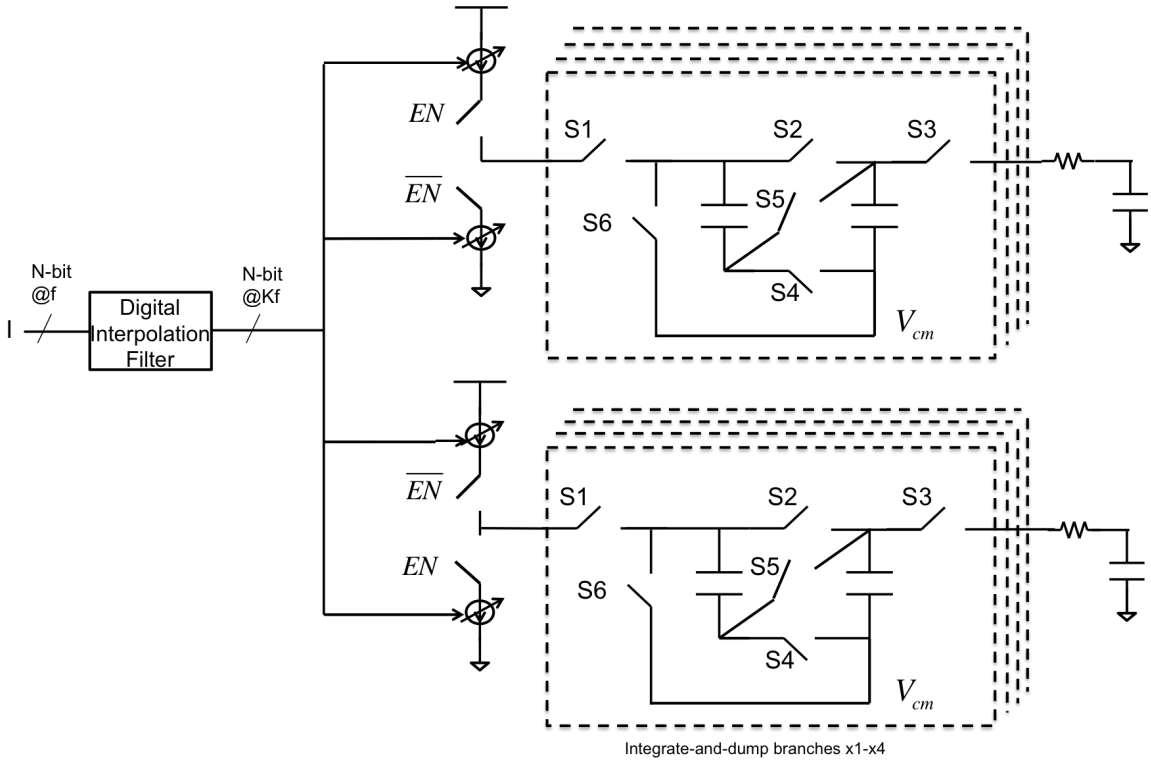


Figure 3.10 Detailed block diagram of the RF TX baseband

The input N-bit word (f samples per second) first passes through a digital interpolation filter, in which it is up-sampled and interpolated to Kf samples per second. Then the current-integrating DAC converts it to an analog signal, while at the same time creates a notch at Kf in the frequency domain. Then a RC filter is used to attenuate the high frequency images starting at 2Kf.

During the integration phase, as shown in the top right left picture of Figure 3.11, switches S1 and S5 are on and the other switches are off. The output currents of the DAC integrate onto 2 capacitors in series. During the sampling phase, the S4, S2 and S3 switches are on as shown in the right top picture, the following stages sample the voltage on the 2 capacitors in parallel. The bottom picture shows that during reset phase, S6, S2 and S4 are on, the charges on the two capacitors are discharged.

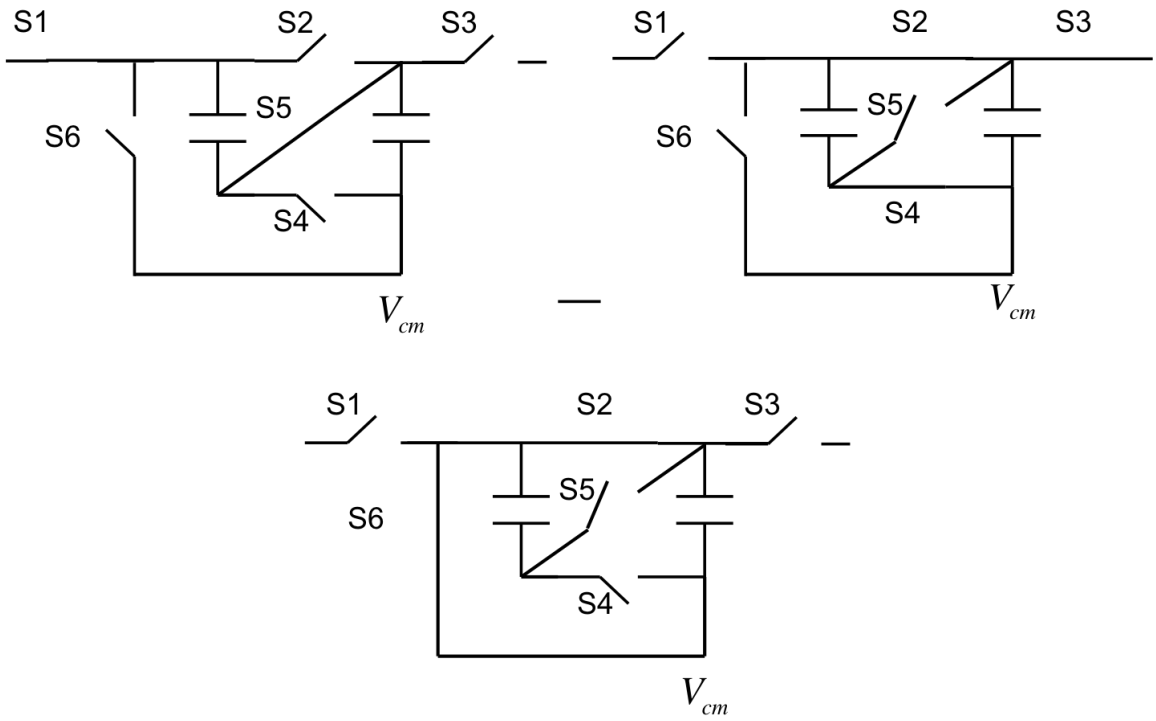


Figure 3.11 Illustration of Integration, Sampling and Reset Phases

Because the DC-DC converter enables us to use the full available voltage swing within the DAC itself, the efficiency of this circuit is better. Detail analysis will be carried out in chapter 4.

Chapter 4

Analysis of RF Transmitter Circuit

In this chapter, we will first analyze the transfer function of the current-integrating DAC and the 25% duty-cycle passive mixer. Then we will find out the power consumption of this RF transmitter.

4.1 TX Transfer Function

In appendix I, we analyzed the TX transfer function of the RF transmitter. The amplitude of the RF output voltage at the fundamental frequency f_{LO} is:

$$V_{RF,fund} = \frac{4\sqrt{2}}{\pi} \frac{R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}} \frac{T_{\text{int}}}{C_{\text{int}}} \sqrt{i_I^2 + i_Q^2} \ .$$

We can then draw an equivalent circuit of the TX baseband as shown below.

In Figure 4.1, the thevenin equivalent voltage and resistance are: $V_{eq} = \frac{i_I T_{\text{int}}}{C_{\text{int}}}$.

$R_{eq} = \frac{T_{samp}}{2NC_{\text{int}}}$.

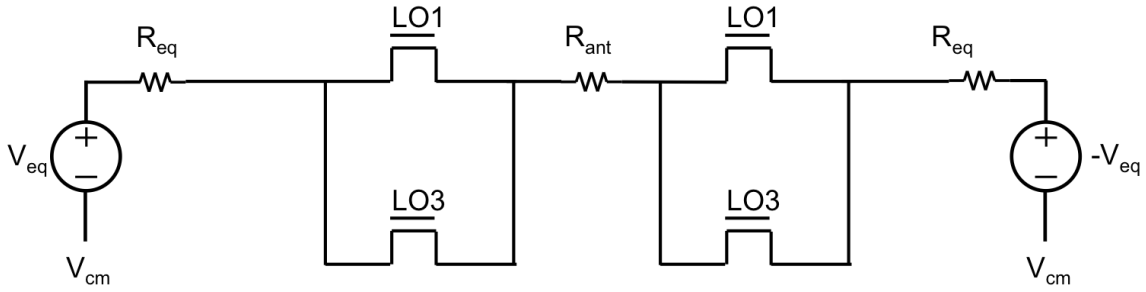


Figure 4.1 Equivalent Circuit of TX baseband

4.2 Analysis of TX power consumption

The total power consumption of the DAC consists of two parts:

1) DC power consumed in the current DAC.
2) Power used to reset the integration capacitor C_{int} in the "reset" phase.

$P_{DAC} = (2i_I + 2i_Q)V_{dd} + 8V_{cm}\frac{Q_{\text{int},I}}{T} + 8V_{cm}\frac{Q_{\text{int},Q}}{T}$. The first term in the equation is the DC power consumed in the current DAC. Both output currents of the DAC for the I and Q branches are multiplied by 2 because we need 2 separate current DACs for the 4 branches in the current-integrating DAC. The second term corresponds to the power dissipated to reset the 16 capacitors (8 for I and 8 for Q) in the circuit.
In Appendix I, we show that P_{DAC} and its associated efficiency η is:

$$P_{DAC} = \pi \frac{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}\frac{C_{\text{int}}}{T_{\text{int}}}}{R_{ant}}(\frac{1}{2}V_{dd} + V_{cm})V_{RF,fund} \quad .$$

$$\eta = \frac{P_{RF}}{P_{DAC}} = \frac{\frac{V_{RF}^2}{2R_{ant}}}{\pi \frac{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}\frac{C_{\text{int}}}{T_{\text{int}}}}{R_{ant}} V_{dd}V_{RF,fund}} \quad .$$

$$= \frac{V_{RF,fund}}{\pi V_{dd}} \frac{1}{(2R_{sw,LO} + R_{ant})\frac{2C_{\text{int}}}{T_{\text{int}}} + \frac{2T_{samp}}{NT_{\text{int}}}}$$

The voltage V_{int} on top of the integration capacitor C_{int} shouldn't be too high or too low in order to ensure that the current sources are in saturation region:

$n_s V_{dsat} < NV_{\text{int}} < V_{dd} - n_s V_{dsat}$, where n_s is the number of stack devices in the current sources.

When $\frac{i_I T_{\text{int}}}{C_{\text{int}}} = \frac{i_Q T_{\text{int}}}{C_{\text{int}}} = V_{dd} - n_s V_{dsat} - V_{cm}$, this topology achieves its maximum output power.

$$V_{RF,fund} = \frac{8}{\pi} \frac{R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{N^2 T_{\text{int}}}\frac{1}{i_I}(\frac{V_{dd}}{2} - n_s V_{dsat})} \frac{1}{N}(\frac{V_{dd}}{2} - n_s V_{dsat})$$

The analog part of the RF TX consumes: $P_{TX,ana\log} = P_{DAC} + P_{LO}$, where P_{LO} is the power used to drive the LO switches. It is inversely proportional to $R_{\text{sw,LO}}$: $P_{LO} = P_{ref}\frac{R_{ref}}{R_{sw,LO}}$ because the switch needs to be large to get low resistance, and it costs more power to drive the switch. If the current of the DAC decreases, meaning that the DC power consumed in the DAC decreases, the thevenin equivalent voltage decreases, so the switch resistance of the mixer switch $R_{\text{sw,LO}}$ has to decrease in order to achieve a certain RF output power. As a result, the power used to drive the mixer switches increases.

This trade-off problem is shown in Figure 4.2. When DC power of the DAC is small, the total power of the analog part of the RF TX P_{total} is dominated by the power used to drive the LO switches P_{LO}. As DC power of the DAC increases, P_{LO} decreases and P_{DAC} increases, the total power of the analog part of the RF TX P_{total} becomes dominated by P_{DAC} in the end. The optimal point is between the two extremes. $P_{DAC} : P_{LO} \approx 3.6$ at the optimal point.

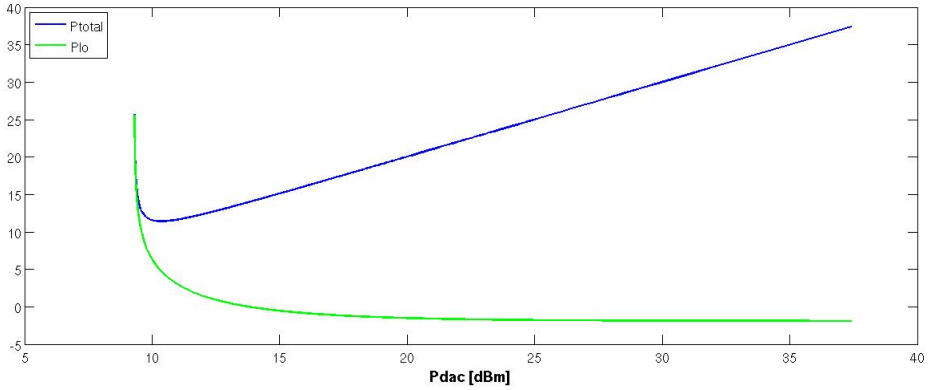


Figure 4.2 Power consumption of LO, DAC, and total

Figure 4.3 Detailed block diagram of revised RF TX baseband

For high output power applications, we could add switches in the circuit and re-arrange the clocking sequences such that in the integration phase, the current DAC integrates onto 2 capacitors in parallel and in sampling phase, the following stages sample the voltage on top of 2 capacitors in series.

The above equations still hold, just that N is smaller than 1 in this case. This structure will be able to output higher output power than $\frac{8}{\pi}(\frac{V_{dd}}{2} - n_s V_{dsat})$.

Table 4.1 shows the optimal designs for different RF output power.

P_{out} (dBm)	Best N	Best $R_{sw,LO}$ (Ω)	P_{DAC} (W)	P_{LO} (W)	P_{total} (W)
24	1/20	0.4	7.5207	0.0911	7.6118
18	1/10	0.7	1.9025	0.0520	1.9546
12	1/5	1.4	0.4892	0.0260	0.5152
6	1/3	3	0.1305	0.0121	0.1426
0	1/2	6.8	0.0386	0.0054	0.0440
-6	1	12.2	0.0108	0.0030	0.0138
-12	2	20.1	0.0033	0.0018	0.0051
-18	2	49	0.0013	0.0007	0.0021
-24	3	87	0.0005	0.0004	0.0009
-30	3	185.3	0.0002	0.0002	0.0004

Table 4.1 Optimal designs for different RF output power

4.4 Comparison with a conventional current DAC

From Table 4.1, the efficiency of the TX $\eta = \frac{P_{out}}{P_{DAC}}$ is 2.3% at -6dBm output power level. We will compare this with a conventional current DAC circuit in this section.

Figure 4.4 shows a TX baseband with a conventional current DAC.

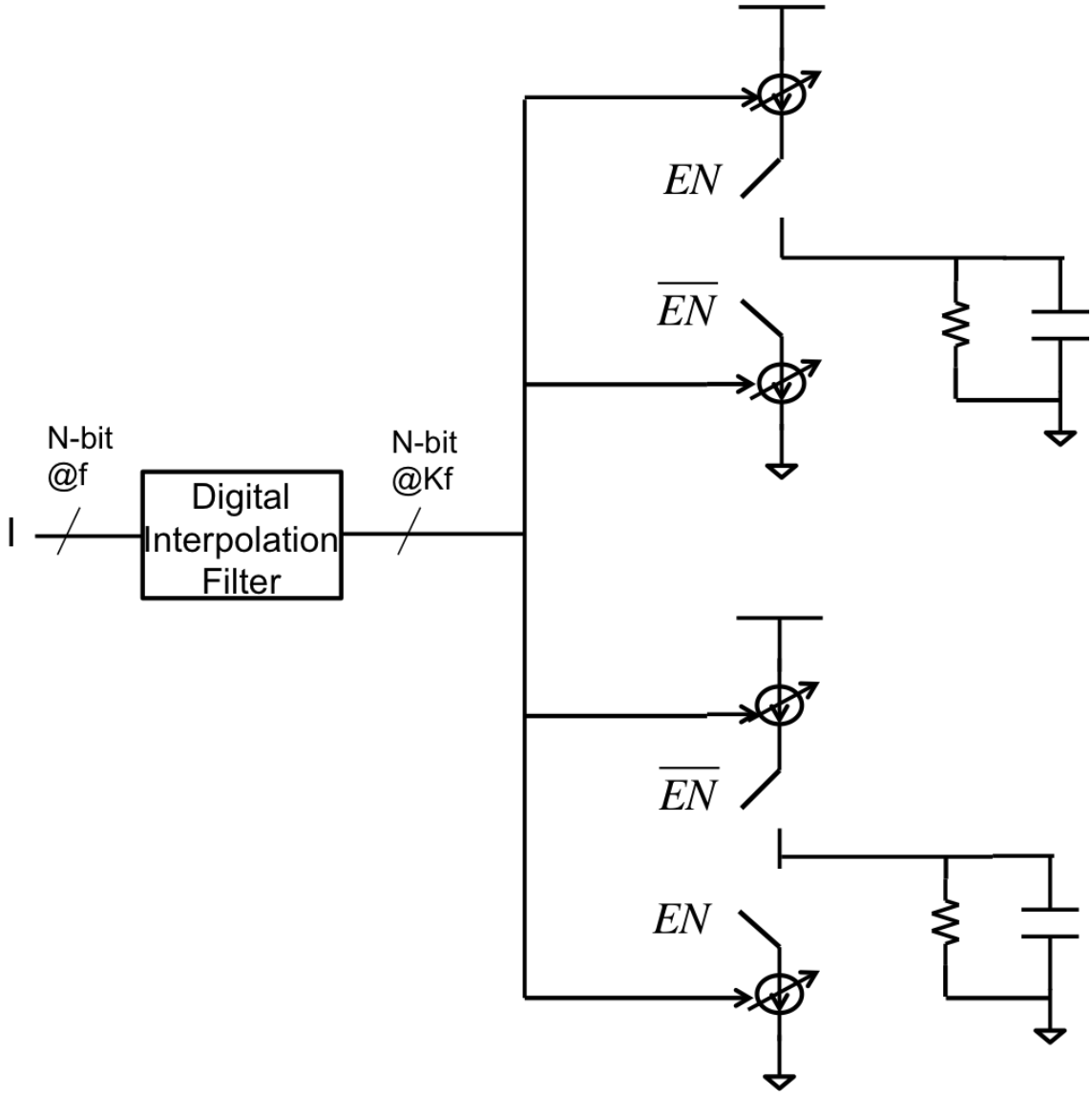


Figure 4.4 TX baseband diagram with a current DAC

Analysis of this topology is shown in Appendix II. The power consumption of the DAC and the efficiency of the TX front-end are:

$$P_{DAC} = \frac{\pi}{2}\frac{V_{RF,fund}}{R_{ant}}V_{dd}$$

$$\eta = \frac{P_{RF}}{P_{DAC}} = \frac{\frac{V_{RF,fund}^2}{2R_{ant}}}{\frac{\pi}{2}\frac{V_{RF,fund}}{R_{ant}}V_{dd}} = \frac{V_{RF,fund}}{\pi V_{dd}}$$

For -6dBm output power, P_{DAC} = 5.95mW, η = 4.2%. To ensure all the current source transistors are in saturation region, the maximum output RF voltage is: $V_{RF,fund} \le \frac{4}{\pi}\frac{R_{ant}}{2R_{sw,LO}+R_{ant}}(V_{dd} - 2n_s V_{dsat})$. Therefore, $R_{sw,LO}$ should be smaller than 55 Ω in this design. The power used to drive the LO switches is P_{LO} = 0.655mW, and the total power consumption of the analog part of the TX is P_{analog} = 6.6mW. This is about half of that for a TX with a current integrating DAC. This is mainly due to the fact the "current-integrating" DAC has to have two identical branches to keep the output continuous.

Chapter 5

Simulation Results and Conclusion

In this chapter, we will implement the whole RF transmitter with System Verilog, and discuss the simulation results.

In the semiconductor and electronic design industry, System Verilog is a combined hardware description language and hardware verification language based on extensions to Verilog. It can be used in digital circuit implementation and verification. Also, with the help of the data type "real", analog circuits could also be described and verified in System Verilog. Thus it is a convenient way to verify a mixed-signal circuit like RF transmitter.

5.1 Simulation Results

With a pulse test input running at 20MHz, Figure 5.1 shows the output spectrum of the digital interpolation filter and the current-integrating DAC. The digital interpolation filter creates notches at multiples of 20MHz because of the delay elements' zero-order-hold nature. With 15 taps, this filter achieves >57dB stop-band (>40MHz) attenuation. The current-integrating DAC creates a notch at 320MHz.

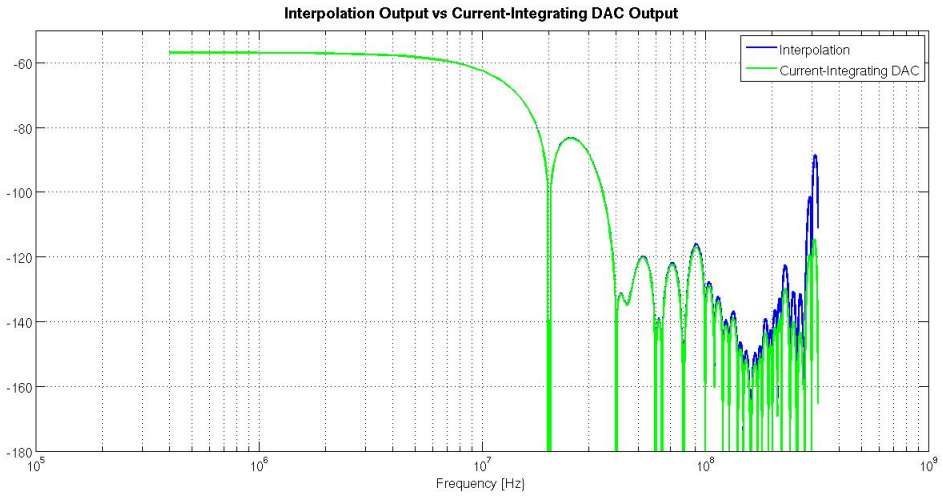


Figure 5.1 Output spectrum of digital interpolation filter and current-integrating DAC

The blue curve in Figure 5.2 shows the 1st-order RC filter output spectrum. The pole of the filter is 10MHz. It can be seen clearly from the figure that the RC filter introduces 20dB attenuation at 100MHz.

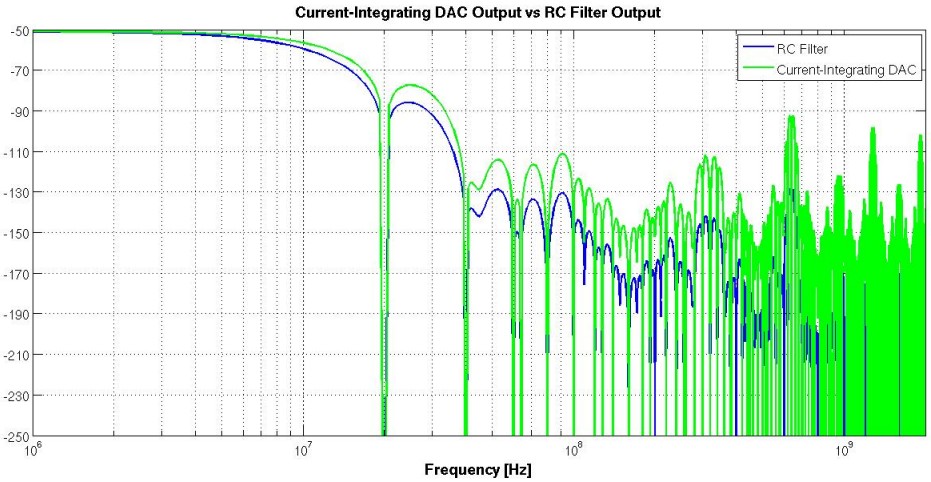


Figure 5.2 Output spectrum of 1st-order RC filter

The spectrum of the RF output is shown in Figure 5.3. The peak out-of-band noise is -77dB at 2GHz $\pm$ 640MHz.

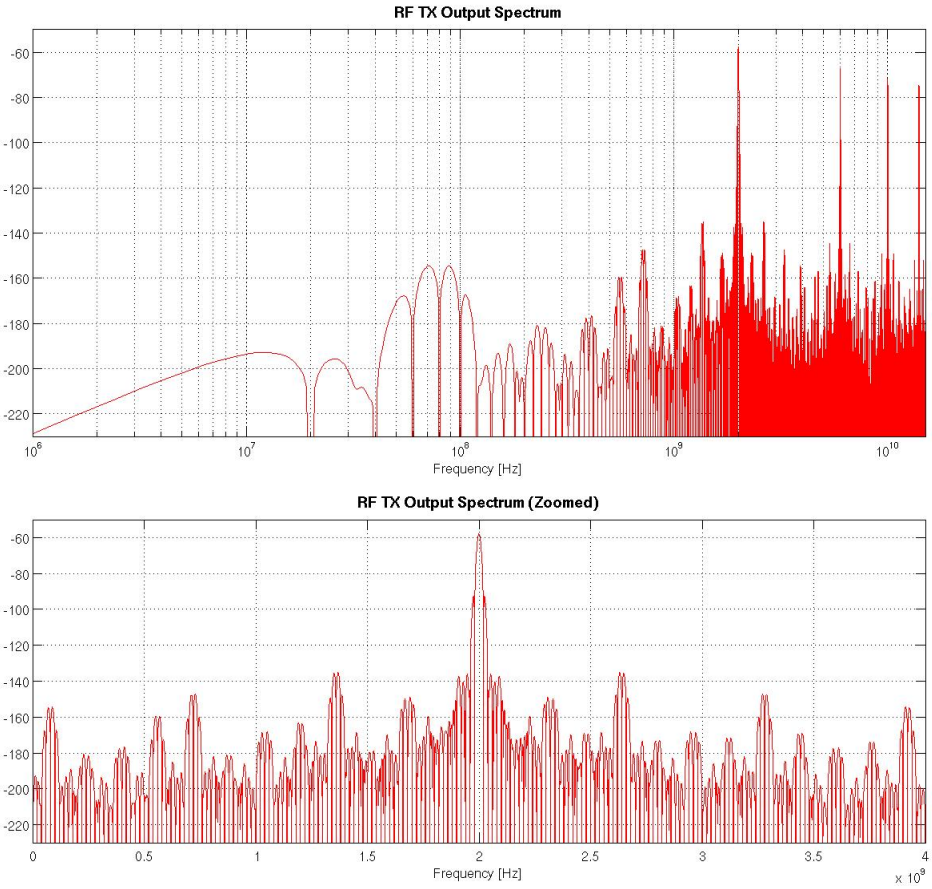


Figure 5.3 RF output spectrum

5.2 Conclusion

In this work, we discussed several design issues of RF transmitter for the "eWallpaper". The "eWallpaper" is a multi-antenna system that is broadband and capable of supporting multiple beams to multiple users simultaneously. In the "xG" vision, it helps out small terminals to do beam forming and signal processing. Therefore, it should have good spatial selectivity, low out-of-band noise and low power consumption.

In chapter 1, we optimized the power consumption of the "eWallpaper" in the RF transmitting cycle. This is basically a trade-off problem – having more ASICs in the array costs more per ASIC overhead power and high-speed links power, while supporting more antennas on each ASIC makes routing hard and attenuates power. We built a mathematical model for this trade-off problem, and solved numerically for our 1^{st} prototype. Then in chapter 2 and 3, we proposed a circuit implementation for RF transmitter. First, digital upsampling and digital interpolation filter upsample the signal data rate to Kf_c symbol/second, and kill the signal images between the signal and its image at Kf_c. Then the current-integrating DAC attenuates the signal image at Kf_c based on the fact that integration for t=T in time domain creates a notch at f=1/T in frequency domain, thus the dominant out-of-band noise is the signal image at $2Kf_c$. In the end, a 1^{st}-order RC filter is used to further attenuate high frequency images. System Verilog is used to verify the functionality and performance of this mixed-signal circuit.

5.3 Future work

In section 4.4, we compared the efficiency and total power consumption of a current DAC and a current integrating DAC. The latter one on consumes about twice power than the former one. In order to improve power efficiency, one possible solution is to push the filtering of the current-integrating DAC into mixed-signal or digital domain and to use a current DAC in this stage. Also we should try to implement similar impedance transformation block in the current DAC as we did in the current integrating DAC. This might further improve the power efficiency.

Appendix I

Analysis of RF transmitter with current-integrating DAC

In this appendix, we will analyze the transfer function and power consumption of the RF TX baseband with current-integrating DAC.

i. Transfer function of TX baseband

The RF TX baseband block diagram is shown in Figure 6.1. For the sake of convenience, it is shown below.

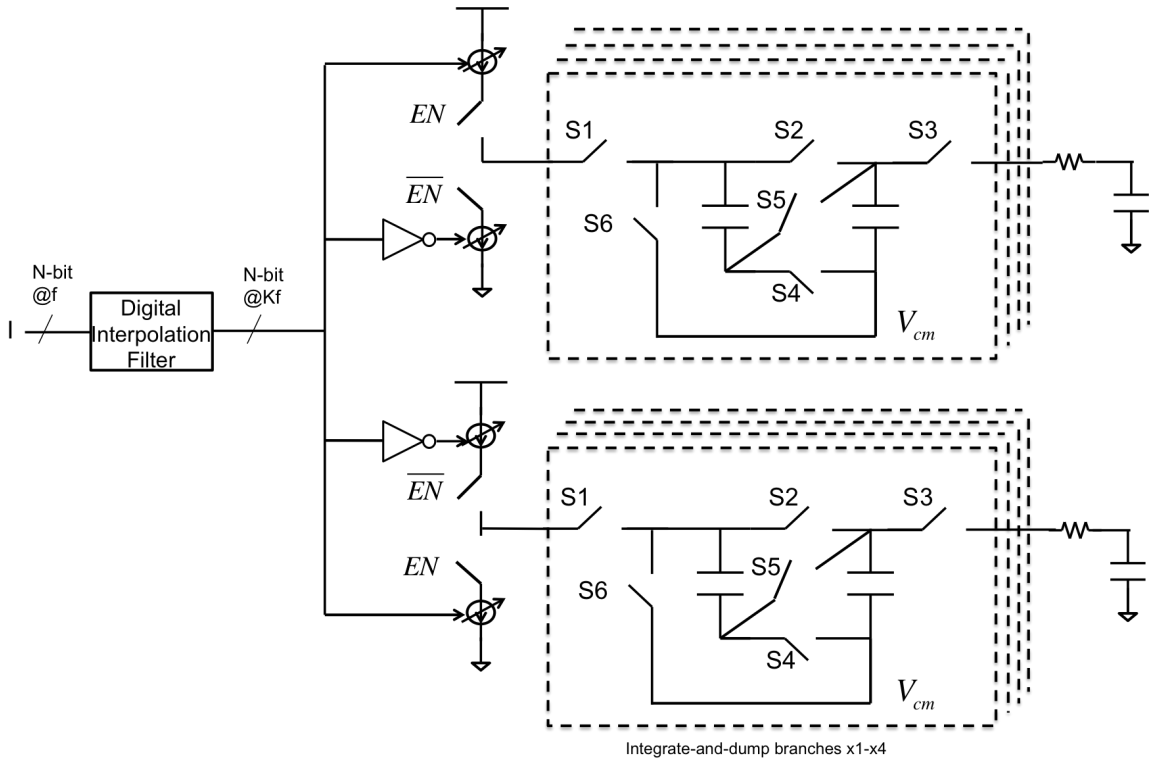


Figure 6.1 Detailed block diagram of TX

During the "integration" phase, S1 and S5 switches are on, output currents of the DAC integrate on N=2 capacitors in series. During the "sampling" phase, S2, S3 and S4 switches are on, the following stages sample the voltage on N=2 capacitors in parallel.

During the "sampling" phase of the current-integrating DAC, the RF front-end circuit can be simplified as shown below. The left side is from the I branch and the right side is from the Ibar branch.

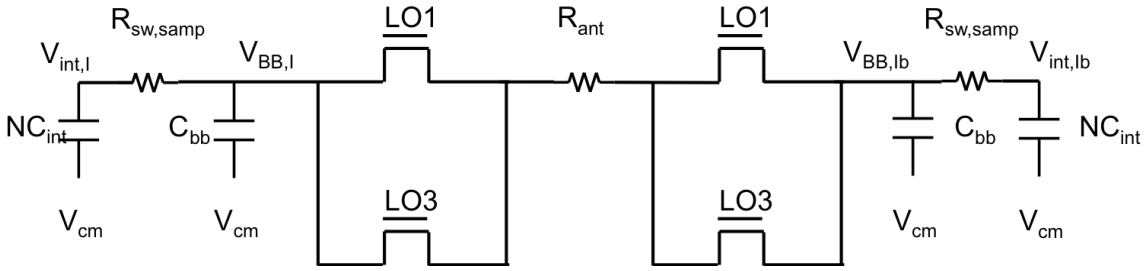


Figure 6.2 Circuit during sampling phase

At t=0 (when the "sample" switch just turns on), the voltages on the integration capacitors C_{int} equal to the voltages at the end of the "integrating" phase,

$V_{\text{int},I}(0) = \frac{i_I T_{\text{int}}}{C_{\text{int}}} + V_{cm}$, $V_{\text{int},Ib}(0) = -\frac{i_I T_{\text{int}}}{C_{\text{int}}} + V_{cm}$, where i_I is the output current of the current DAC.

Assume that $R_{sw,samp}$ is small enough that the time constant of the circuit is smaller than the "sampling" time, therefore at the end of the "sampling" phase, $V_{int,I} = V_{BB,I}$ and $V_{int,Ib} = V_{BB,Ib}$. Then during the "sampling" phase, the charge delivered from/on the two integration capacitors is: $Q = NC_{\text{int}}(V_{\text{int},I}(0) - V_{BB,I}) = NC_{\text{int}}(V_{BB,Ib} - V_{\text{int}.Ib}(0))$. This charge equals to the charge that flows through R_{ant} when LO1 or LO3 is on:

$$Q = \int_{LO1,LO3on} \frac{V_{BB,I} - V_{BB,Ib}}{2R_{sw,LO} + R_{ant}} dt = \frac{V_{BB,I} - V_{BB,Ib}}{2R_{sw,LO} + R_{ant}} \frac{T_{samp}}{2}.$$

By equating the above equations, we get:

$$V_{BB,I} = \frac{(2R_{sw,LO} + R_{ant})i_I}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}} \frac{T_{\text{int}}}{C_{\text{int}}} + V_{cm},$$

$$V_{BB,Ib} = -\frac{(2R_{sw,LO} + R_{ant})i_I}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}} \frac{T_{\text{int}}}{C_{\text{int}}} + V_{cm}.$$

When LO1 is on, the voltage across the antenna resistance $V_{RF} = \frac{R_{ant}}{2R_{sw,LO} + R_{ant}}(V_{BB,I} - V_{BB,Ib}) = \frac{2i_I R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}} \frac{T_{\text{int}}}{C_{\text{int}}}$. When LO3 is on:

$V_{RF} = \frac{R_{ant}}{2R_{sw,LO} + R_{ant}}(V_{BB,Ib} - V_{BB,I}) = -\frac{2i_I R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}} \frac{T_{\text{int}}}{C_{\text{int}}}$. When LO2 is on:

$V_{RF} = \frac{R_{ant}}{2R_{sw,LO} + R_{ant}}(V_{BB,Q} - V_{BB,Qb}) = \frac{2i_Q R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}} \frac{T_{\text{int}}}{C_{\text{int}}}$. When LO4 is on:

$V_{RF} = \frac{R_{ant}}{2R_{sw,LO} + R_{ant}}(V_{BB,Qb} - V_{BB,Q}) = -\frac{2i_Q R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}} \frac{T_{\text{int}}}{C_{\text{int}}}$. By Fourier transformation, the amplitude of the RF output voltage at fundamental frequency f_{LO} is:

$V_{RF,fund} = \frac{4\sqrt{2}}{\pi} \frac{R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}} \frac{T_{\text{int}}}{C_{\text{int}}} \sqrt{i_I^2 + i_Q^2}$.

We could then draw an equivalent circuit of the TX baseband as shown below.

In Fig, $V_{eq} = \frac{i_I T_{\text{int}}}{C_{\text{int}}}$. $R_{eq} = \frac{T_{samp}}{2NC_{\text{int}}}$.

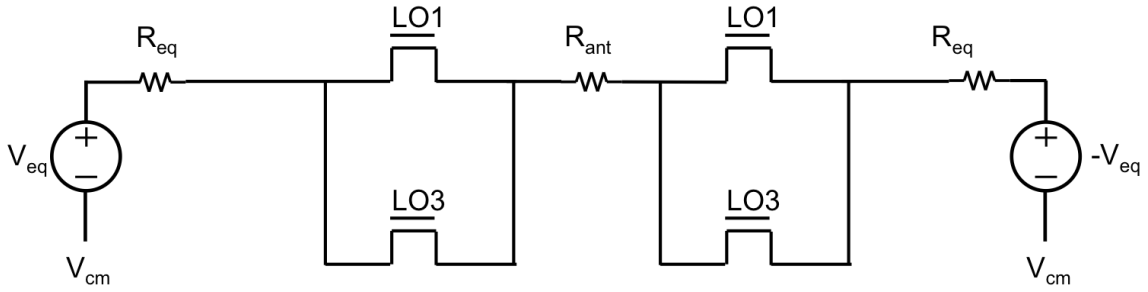


Figure 6.3 Equivalent Circuit of TX baseband

When N=1, it is a transmitter without impedance transformation. When N<1, the output current of the DAC integrate onto 1/N capacitors in parallel, and during the "sampling" phase, the following stage sample the voltage on top of 1/N capacitors in series.

ii. Power consumption of TX baseband

As we discussed in section 4.2, $P_{DAC} = (2i_I + 2i_Q)V_{dd} + 8V_{cm}\frac{Q_{\text{int},I}}{T} + 8V_{cm}\frac{Q_{\text{int},Q}}{T}$. The first term in the equation is the DC power consumed in the current DAC. Both output currents of DAC for I and Q are multiplied by 2 because we need 2 separate current DACs for the 4 branches in the current-integrating DAC. The second term corresponds to the power dissipated to reset the 16 capacitors (8 for I and 8 for Q) in the circuit.

The average current used to reset the capacitors is the charge on the capacitor divided by the period. Then we can rewrite P_{DAC} as:

$P_{DAC} = (2i_I + 2i_Q)V_{dd} + 8V_{cm}\frac{i_I T_{\text{int}}}{2T_{\text{int}}} + 8V_{cm}\frac{i_Q T_{\text{int}}}{2T_{\text{int}}}$.

To simply our discussion, we assume that $i_I = i_Q$ in the following discussion. Therefore, $V_{RF,fund} = \frac{8}{\pi} \frac{R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}} \frac{T_{\text{int}}}{C_{\text{int}}} i_I$. We could then write i_I in terms of $V_{RF,fund}$:

$$i_I = V_{RF,fund} \frac{\pi}{8} \frac{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}}{R_{ant}} \frac{C_{\text{int}}}{T_{\text{int}}}.$$

$$P_{DAC} = \pi \frac{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}}{R_{ant}} \frac{C_{\text{int}}}{T_{\text{int}}} (\frac{1}{2} V_{dd} + V_{cm}) V_{RF,fund}.$$

If we assume $V_{cm} = \frac{V_{dd}}{2}$,

$$P_{DAC} = \pi \frac{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}}{R_{ant}} \frac{C_{\text{int}}}{T_{\text{int}}} V_{dd} V_{RF,fund}. .$$

$$\eta = \frac{P_{RF}}{P_{DAC}} = \frac{\frac{V_{RF}^2}{2R_{ant}}}{\pi \frac{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{NC_{\text{int}}}}{R_{ant}} \frac{C_{\text{int}}}{T_{\text{int}}} V_{dd} V_{RF,fund}}$$

$$= \frac{V_{RF,fund}}{\pi V_{dd}} \frac{1}{(2R_{sw,LO} + R_{ant}) \frac{2C_{\text{int}}}{T_{\text{int}}} + \frac{2T_{samp}}{NT_{\text{int}}}}$$

The voltage V_{int} on top of the integration capacitor C_{int} shouldn't be too high or too low in order to ensure that the current sources are in saturation region: $n_s V_{dsat} < N V_{\text{int}} < V_{dd} - n_s V_{dsat}$, where n_s is the number of stack devices in the current sources. When $\frac{N i_I T_{\text{int}}}{C_{\text{int}}} = \frac{N i_Q T_{\text{int}}}{C_{\text{int}}} = V_{dd} - n_s V_{dsat} - V_{cm}$, this topology achieves its maximum output power:

$$V_{RF,fund} = \frac{8}{\pi} \frac{R_{ant}}{(2R_{sw,LO} + R_{ant}) + \frac{T_{samp}}{N^2 T_{\text{int}}} \frac{1}{i_I} (\frac{V_{dd}}{2} - n_s V_{dsat})} \frac{1}{N} (\frac{V_{dd}}{2} - n_s V_{dsat}).$$

Appendix II

Analysis of RF transmitter with current DAC

In this appendix, we analyze the transfer function and power consumption of an RF transmitter with current DAC.

i. Transfer function of RF TX with current DAC

The RF front-end circuit is shown below.

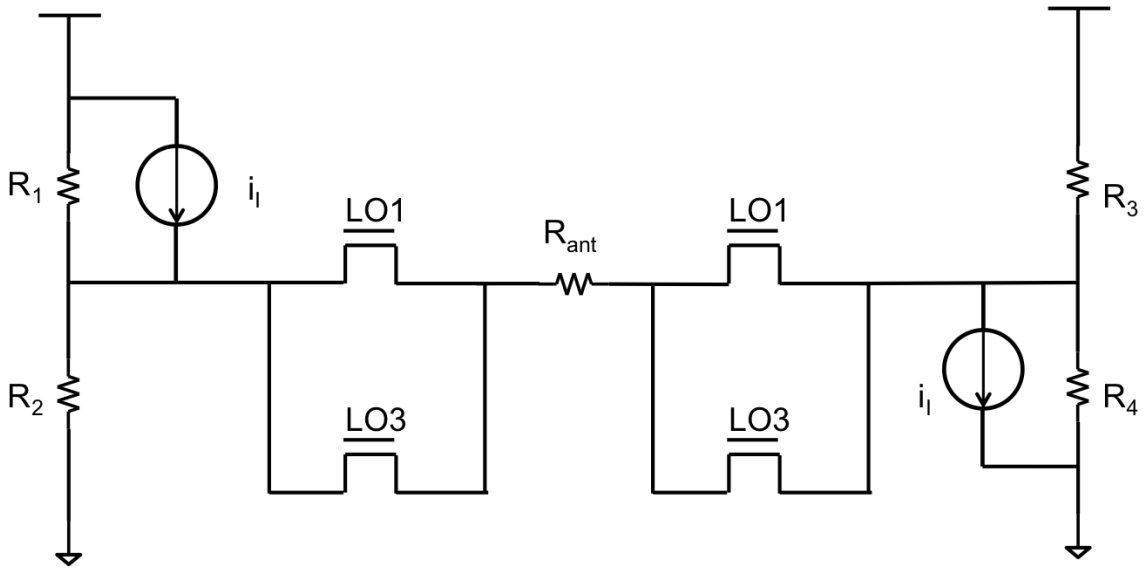


Figure 7.1 RF front-end circuit with current DAC

When LO1 or LO3 is on, the voltage across the antenna resistance is:

$$V_{RF} = \frac{V_{dd}\left[\frac{R_2}{R_1+R_2} - \frac{R_4}{R_3+R_4}\right] + i_I\left(\frac{R_1R_2}{R_1+R_2} + \frac{R_3R_4}{R_3+R_4}\right)}{\left(\frac{R_1R_2}{R_1+R_2} + \frac{R_3R_4}{R_3+R_4} + 2R_{sw,LO} + R_{ant}\right)} R_{ant}.$$

Let I_{unit} be the current of one current unit, N be the number of bits in the current DAC and n be the number of current units that is on when the output current is i_I. $R_{on,p}$ and $R_{off,p}$ are the on-resistance and off-resistance of one PMOS current unit respectively. $R_{on,n}$ and $R_{off,n}$ are the on-resistance and off-resistance of one NMOS current unit respectively.

$R_1 = \frac{R_{on,p}}{n} // \frac{R_{off,p}}{2^N - 1 - n}$, $R_2 = \frac{R_{off,n}}{2^N - 1}$, $R_3 = \frac{R_{off,p}}{2^N - 1}$, $R_4 = \frac{R_{on,n}}{n} // \frac{R_{off,n}}{2^N - 1 - n}$. For simplicity, we assume $R_{on} = R_{on,p} = R_{on,n}$ and $R_{off} = R_{off,p} = R_{off,n}$ in the future discussion.

$V_{RF} = \frac{R_{ant}}{2R_{out} + 2R_{sw,LO} + R_{ant}} [V_{dd} \frac{(R_{off} - R_{on})}{i_I (R_{off} - R_{on}) + 2R_{on}(2^N - 1) I_{unit}} + 2R_{out}] i_I$, where R_{out} is the output resistance of the current source:

$R_{out} = R_1 // R_2 = R_3 // R_4 = \frac{R_{on} \cdot R_{off}}{n(R_{off} - R_{on}) + 2(2^N - 1)R_{on}} = \frac{R_{on} \cdot R_{off} \cdot I_{unit}}{i_I (R_{off} - R_{on}) + 2R_{on}(2^N - 1) I_{unit}}$.

Because $R_{off} >> R_{on}$: $V_{RF} \approx \frac{R_{ant}}{2R_{out} + 2R_{sw,LO} + R_{ant}} [V_{dd} \frac{1}{i_I} + 2R_{out}] i_I$

Let V_{bb} be the voltage across the mixers and the antenna resistance:

$\frac{V_{bb}}{V_{RF}} = \frac{R_{ant} + 2R_{sw,LO}}{R_{ant}}$. Then we could rewrite $\frac{V_{dd}}{i_I}$ in terms of V_{dd} and V_{bb}:

$\frac{V_{dd}}{i_I} = V_{dd} \frac{1}{V_{bb}} \frac{V_{bb}}{i_I} \approx V_{dd} \frac{1}{V_{bb}} (R_{ant} + 2R_{sw,LO}) = \alpha (R_{ant} + 2R_{sw,LO})$, where α is V_{dd}/V_{bb}, so it is slightly larger than 1.

In most cases, $R_{out} >> R_{ant} + 2R_{sw,LO}$, therefore, $V_{RF} \approx i_I R_{ant}$.

Then by Fourier transform, the amplitude of the RF output voltage at its fundamental frequency is:

$V_{RF,fund} = \frac{2\sqrt{2}}{\pi} \sqrt{i_I^2 + i_Q^2} R_{ant}$.

The maximum voltage in this topology is also limited by the V* of the current sources:

$i_I (2R_{sw,LO} + R_{ant}) < V_{dd} - 2n_s V_{dsat}$, where n_s is the number of stacked transistors in the current source.

$V_{RF,fund} \le \frac{4}{\pi} \frac{R_{ant}}{2R_{sw,LO} + R_{ant}} (V_{dd} - 2n_s V_{dsat})$

ii. Power consumption of RF TX with current DAC

Power consumed by the current DAC can be easily calculated by multiplying the supply voltage and the current. $P_{DAC} = V_{dd}(i_I + i_Q)$. Again, for the sake of simplicity, we assume $i_I = i_Q$ in the following discussion.

$i_I = \frac{\pi}{4} \frac{V_{RF,fund}}{R_{ant}}$

$P_{DAC} = \frac{\pi}{2} \frac{V_{RF,fund}}{R_{ant}} V_{dd}$

$$\eta = \frac{P_{RF}}{P_{DAC}} = \frac{\frac{V_{RF,fund}^2}{2R_{ant}}}{\frac{\pi}{2}\frac{V_{RF,fund}}{R_{ant}}V_{dd}} = \frac{V_{RF,fund}}{\pi V_{dd}}$$

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