High Contrast Metastructures on Silicon for Optoelectronic Devices

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High Contrast Metastructures on Silicon for Optoelectronic Devices

by

James Enrico Ferrara Jr.

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requirements for the degree of

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Abstract

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Over the past few years, tremendous effort has gone into the development of various optical building blocks for the silicon photonics platform. Part of the allure is that photonics circuits on silicon can be very small and leverage over 5 decades of scaling and existing microelectronics infrastructure. As such, photonic integrated circuits (PICs) on silicon are poised to address the ever-growing high-bandwidth needs of the servers and data centers of tomorrow, where the high-volume processing of a silicon platform and the low cost of traditional optical communications could redefine the constraints of high-performance interconnects.

High contrast metastructures (HCMs) are an emerging solution for flat integrated photonic devices. These ultra-thin semiconductor ribbons can exhibit extraordinary properties that are atypical to traditional optical gratings, such as very broadband reflection at normal and shallow angles, high-Q resonances, and a readily engineered phase response. These properties have allowed for the design of a variety of novel optoelectronic devices such as vertical-cavity surface-emitting lasers (VCSELs), phase-arrays, lenses, and sensors.

In this work, we explore three different types of novel HCMs *on silicon*. The first is a hollow-core waveguide that can channel light at wavelengths where traditional solid waveguides encounter difficulties; next is a silicon-based HCG VCSEL with the potential of being an efficient light source for silicon PICs; and lastly, an integrated wavelength meter, which can circumvent bulky off-the shelf instruments to provide wavelength characterization of guided light on a chip.

To Nicole.

I kept my wedding vows.

Table of Contents

Table of Contents ..... **ii**
List of Figures ..... **v**
Acknowledgments ..... **xiii**
Chapter 1 Introduction **1**
1.1 High Contrast Gratings 5
1.2 Dissertation Overview 12
Chapter 2 Low Loss Hollow-Core Waveguides **13**
2.1 Introduction 13
2.2 HCG HCW Design and Fabrication 14
2.2.1 Simulations 16
2.2.2 HCG HCW fabrication 17
2.3 Experimental Results 18
2.3.1 Optical mode imaging and loss measurement 18
2.3.2 Data processing for waveguide loss 20
2.3.3 Dependence of lateral confinement on core height *d* 21
2.3.4 Light guiding in curved HCG HCWs 22
2.4 Summary 24
Chapter 3 Pairwise Integration of InP VCSEL to Silicon Photonics **25**
3.1 Introduction 25
3.1.1 Bonding approach: the AuSn material system 26
3.2 Silicon Photonics Chip Design 31
3.2.1 Input coupler simulation 31
3.2.2 Electrical contacts to VCSEL 34
3.3 Experimental Results 36
3.3.1 Flip chip bonding 36
3.3.2 VCSEL Performance before and after bonding 37
3.3.3 Optical profile 38
3.4 Summary 40
Chapter 4 Heterogeneously-integrated VCSEL using High-Contrast Grating on Silicon **41**

4.1 Introduction 41
4.2 HCG Design and Fabrication 41
4.2.1 Modeling of HCG VCSEL cavity 41
4.2.2 Thermal modeling of VCSEL structure 44
4.2.3 Proton-implant current aperture 46
4.2.4 HCG VCSEL fabrication 46
4.3 Experimental Results 49
4.3.1 Light-Current-Voltage (LIV) characteristics 49
4.3.2 Optical mode profile 49
4.3.3 Laser Spectrum and Thermal Performance 50
4.3.4 High-speed Modulation 51
4.3.5 VCSEL on a Flexible Substrate 52
4.4 Tunable VCSEL using MEMS Actuator 53
4.4.1 Electrostatic actuator modeling 55
4.4.2 Electrostatic actuator characterization 58
4.4.3 VCSEL tuning results 60
4.5 All HCG VCSEL 61
4.5.1 Design and simulation 62
4.5.2 Proton-implant simulations 63
4.5.3 Fabrication 65
4.5.4 Experimental results 66
4.6 Summary 67
Chapter 5 Integrated Wavemeter 68
5.1 Introduction 68
5.2 Design 69
5.2.1 Dielectric grating coupler principle 69
5.2.2 Four port coupler 71
5.2.3 Fabrication constraints 71
5.3 Simulation 72
5.3.1 Waveguide width parameter sweep 74
5.3.2 HCM thickness parameter sweep 75

5.3.3 HCM period parameter sweep 76
5.3.4 HCM bar width parameter sweep 77
5.3.5 HCM designs 78
5.4 Silicon Photonics Chip Design 79
5.5 Experimental Results 82
5.6 Summary 83
Chapter 6 Conclusion 84
References 85

List of Figures

Figure 1.1 Infographic representing the amount of data generated every minute, in 2014 [6]. 2

Figure 1.2 Cisco's Visual Networking Index (VNI) projects that by 2018, total traffic will be 3 times larger than 2013 [7]. 3

Figure 1.3 Dense metal interconnects (13 levels) in the Broadwell processor. [11] 3

Figure 1.4 Silicon nanophotonic waveguide supporting a single TE mode. The area of this waveguide has a 714X size reduction when compared to a single mode fiber. 4

Figure 1.5 Schematic of HCG, where Λ, HCG period; s, bar width; a, air gap width; t_g, HCG thickness. 5

Figure 1.6 (a) Reflectivity contour plot of HCG versus normalized wavelength (λ/Λ) and normalized thickness (tg/Λ). The white dotted line indicates a suitable design for broadband reflection. (b) Reflectivity spectrum for HCG designed for broadband reflection (blue) and broadband transmission (green). 6

Figure 1.7 Schematic of traditional long-wavelength distributed Bragg reflector with 40 pairs of thin films (~ 10λ), side-by-side with HCG reflector (15% λ). 6

Figure 1.8 HCG reflector and coupler simulation with FDTD. (a) Schematic indicating incident beam as vertical input. The HCG layer consists of a 358-nm thick silicon layer on an SOI substrate. The HCG is designed to have 863 nm period and 0.6 duty cycle. (b) >99.4% reflectivity for VCSEL. (c) 47% of the output power is coupled to bi-directional waveguides. 7

Figure 1.9 Reflectivity contour map for HCG parameter space in period and air gap width (inverse duty cycle), for designs with reflectivity greater than 99.99% for TE polarized light (electric field along the grating direction). An HCG with a thickness of 380 nm can have very high reflectivity for a variation of period of 80 nm, as well as 60 nm in air gap width. 8

Figure 1.10 HCG parameter space search for designs tolerant to deviations in period and air gap by ± 10 nm, while maintaining a propagation loss < 0.1 dB/m. TE polarization and 10 µm waveguides. 9

Figure 1.11 HCG parameter space search for designs tolerant to deviations in period and air gap by ± 10 nm, while maintaining a propagation loss < 0.1 dB/m. TE polarization and 15 µm waveguides. 9

Figure 1.12 HCG parameter space search for designs tolerant to deviations in period and air gap by ± 10 nm, while maintaining a propagation loss < 0.1 dB/m. TM polarization and 10 µm waveguides. 10

Figure 1.13 HCG parameter space search for designs tolerant to deviations in period and air gap by ± 10 nm, while maintaining a propagation loss < 0.1 dB/m. TM polarization and 10 µm waveguides. 10

Figure 1.14 3-D parameter space of RCWA simulation for TE HCG reflector tailored for a reflection angle corresponding to a 15 μm thick waveguide. 11

Figure 1.15 Corresponding 2-D slice sweeping air gap versus thickness. (a) 1550 nm, and (b) 1610 nm..... 12

Figure 1.16 Corresponding 2-D slice sweeping period versus thickness. (a) 1550 nm. (b) 1610 nm..... 12

Figure 2.1 The HCG HCW. Schematic of an HCG HCW. The silicon HCG sits on top of a SiO2 layer and silicon substrate. Two HCG chips are placed in parallel with a separation gap d, forming an HCW. In the lateral direction, the core and cladding are defined by different HCG parameters to provide lateral confinement..... 14

Figure 2.2 Ray optics illustration for a 1-D slab HCG HCW. The k vector is decomposed into the propagation constant k_z and transverse component k_x. θ is the angle between k and k_z; d is the waveguide height; E indicates the oscillation direction of the electrical field; Λ is the HCG period; s is the silicon grating bar width and t_g is the HCG thickness..... 15

Figure 2.3. Loss and effective index contour plots of HCG hollow-core slab waveguides at *d* of 9-μm. The contour plots provide the design template for the waveguide. Different HCG periods *Λ* and silicon grating bar widths *s* are chosen for the core (point A) and cladding (point B), as well as the transition region (dots linked with dashed lines). The HCG thickness t_g is fixed at 340 nm, and the buried oxide thickness is set to 2 μm. The wavelength of the light is 1550 nm. 16

Figure 2.4 Optical mode of an HCG HCW. (a) Propagation mode profile simulated by FEM. The core width is 10.9 μm, the transition region is 11.9 μm, and the cladding width is 42.7 μm. (b) Experimentally measured optical mode profile. 17

Figure 2.5. Fabricated HCG HCW chips. (a) Optical microscope image of the HCG chip. The core, transition and cladding regions are clearly distinguished by their diffracted colors. (b) and (c) The SEM image of the HCG grating bars in the core region and cladding regions. 18

Figure 2.6 Optical characterization system for the hollow-core waveguide prototype. 19

Figure 2.7 The measured mode profile from the fabricated device. The simulation (red curve) agrees well with experiment (blue line). The full width at half maximum (FWHM) is 4 μm in the transverse direction, and 25 μm in the lateral direction. The wavelength in both simulation and measurement is 1550 nm. 19

Figure 2.8 Loss spectrum of the HCG HCW for a 9-μm-high waveguide and lateral confinement. The total loss spectrum for an HCG HCW with four different lengths. The dashed dot line is the measured data. The oscillation is due to the laser and a residual Fabry-Pérot cavity in the optical path of the measurement system. To remove this noise, a smoothing spline method is applied and the solid curves show the clean spectra. 20

Figure 2.9 The experimental extracted propagation loss as a function of wavelength (blue) and the simulated loss spectrum obtained by FEM (red). Inset: the linear curve fitting used to extract the propagation loss and coupling loss at 1535 nm. 21

Figure 2.10 Mode profile at different waveguide heights d. As d decreases, $\Delta n/n_{core}$ increases, and the mode is more confined with reduced lateral leakage. The guidelines indicate the FWHM of the mode in the lateral direction. Experimental lateral FWHM of the fundamental mode versus different waveguide height *d* (blue dots as experiment sampling points, curve-fitted with blue curve). The $\Delta n/n_{core}$ value of the fundamental mode as simulated by FEM is shown in red. The wavelength for the measurement is 1550 nm. 21

Figure 2.11 (a) Mode profiles for three side-by-side HCWs, with lateral guiding (top), step-index guiding (middle) and anti-guided design where the core and cladding designs are swapped (bottom). For the mode profiles, the output power of the mode is kept constant and d is constant ~9 μm. The image window is 140 μm by 16 μm. The wavelength is set to 1550 nm. (b) Propagation loss versus waveguide height *d* at a wavelength of 1535 nm. At the optimized waveguide height of 9 μm, an optimal tradeoff between lateral leakage and transverse leakage is achieved. The FEM simulated loss for the fundamental mode is also plotted, in reasonable agreement with experiment. 22

Figure 2.12 (a) Layout of the "S-shape" and "double-S-shape" curved waveguides. For the "S-shape" layout, curved waveguides A-A' and B-B' are parallel, and the input port of A-A' is aligned with the output port of B-B'. Light is launched into port A. Light guiding by the bend is demonstrated with the output observed in A' rather than B'. (b) Experimental loss spectrum for waveguides with different radii of curvature R, extracted from various waveguide length combinations of the "double-S-shape" curved waveguide layout. The loss includes both the propagation loss and the mode coupling loss at the four bending junctures for an 18-mm long waveguide. (c) The slope of the linear fit of loss versus R^{-1}, α, as a function of wavelength; this is consistent with the FEM simulated $\Delta n/n_{core}$ spectrum. 23

Figure 3.1 Schematic for pairwise integration of VCSEL onto a silicon photonics chip. 26

Figure 3.2 Bonding approaches for hybrid integration of silicon and III-V materials systems.... 26

Figure 3.3 The Au-Sn material system phase diagram [41]. The 400 °C line corresponds to the maximum temperature of the Finetech Lambda flip-chip bonder. 28

Figure 3.4 Cartoon illustration of eutectic film stack including adhesion and diffusion blocking layers. 30

Figure 3.5 Schematic of IMEC passives. 31

Figure 3.6 (a) Vertical coupler schematic. The silicon device layer is 220 nm thick and lies on a 2 μm BOX. (b) FDTD simulation for a plane wave incident on a 2^{nd} order grating coupler. The grating period is 575 nm, duty cycle 62%, and has a shallow 70 nm etch. (c) The total coupling efficiency of double side output is 46.2%. The 3 dB bandwidth is 78 nm. Simulation performed by Li Zhu. 32

Figure 3.7 (a) Angled coupler schematic for coupling into single waveguide. (b) FDTD simulation. The grating period is 615 nm, duty cycle 53%, and has a shallow 70 nm etch. (c) The coupling efficiency is 40.1%. The 3 dB bandwidth is 65 nm. Simulation performed by Li Zhu. 32

Figure 3.8 Photograph of 8" SOI wafer with 6.3 mm x 6.1 mm chip design within 25.87 mm x 28.96 mm stepper window. 33

Figure 3.9 Silicon photonics chip layout for MPW shuttle run with IMEC-ePIXfab 3394 ('imec 11')..... 34

Figure 3.10 (a) Confocal image of AuSn bonding pads and electrical interconnects deposited by e-beam evaporation on the silicon photonics chip. The thickness of the AuSn metallic stack is 1.2 μm, the wire interconnects are 10 μm wide. (b) Confocal image of VCSEL contact and landing pads for bonding. 35

Figure 3.11 (a) Top view SEM image of the input grating coupler. (b) Tilted view SEM of same device. The 1.2 μm thickness of the AuSn bonding and contact layer can be appreciated. 35

Figure 3.12 Sequence of photographs showing VCSEL die being placed and bonded to the silicon photonics chip..... 36

Figure 3.13 (a) Confocal microscope image of HCG VCSEL die from HCG-side of device. (b) VCSEL flip-chip bonded to silicon photonics chip. The VCSEL frontside is now facing down towards the silicon photonics chip. Output couplers are on the left- and right-most sections of image, as indicated by red beams..... 37

Figure 3.14 CW LIV of HCG VCSEL before and after bonding to SiPh chip. Top insets show confocal image of the device under test. (Blue trace) CW LIV of "stand-alone" VCSEL die. Light collection is done from the front side (HCG end) of the VCSEL chip using a wide area Ge photodetector. (Red trace) CW LIV of bonded VCSEL on SiPh. Light collection is done from the backside (DBR end) of the VCSEL..... 38

Figure 3.15 Near field optical imaging of the bonded VCSEL using a 100X objective and InGaAs CCD. (Left) Light is collected from backside of VCSEL (DBR end). (Right) light is collected from 2nd order grating coupler. Using the normalized intensity of the IR CCD image, the ratio of power $I_{coupler}/I_{VCSEL}$ ~ 12%. 38

Figure 3.16: Infrared transverse mode profile measurements reveal fundamental-mode VCSEL operation. 39

Figure 3.17 Profile of light collected at output couplers after traveling through 500 nm-wide single-mode TM Si waveguides..... 39

Figure 4.1 Schematic of VCSEL with silicon HCG as bottom mirror. (a) Tilted-view of VCSEL cross-section with circulating red arrows indicating optical cavity, drawn to scale. (b) The two material systems are heterogeneously integrated via AuSn thin film, with a hermetically sealed cavity gap of length L within the cavity. The VCSEL employs a proton implant-defined aperture for current confinement, indicated by red curved lines between contacts. 42

Figure 4.2 Parameter space of HCG designs using analytical method in [64]. (a) Contour map for reflectivity >99%, highest possible reflectivity is 100%. (b) Corresponding phase response of HCG for same dimensions. An HCG design with 660 nm period and 275 nm air gap has a reflectivity >99.5% and a phase response of ~1.2π. 42

Figure 4.3 FDTD simulation of "cold-cavity" resonances for different metal thin films L_m. The length L_m is a segment of the total cavity gap L. Simulation was performed by varying the metal thin film thickness Lm from 500 nm (purple trace) to 700 nm (red trace) in 50 nm steps. Extending the length of the metal thin film makes the cavity length L longer and red-shifts the corresponding longitudinal mode of the cavity. 43

Figure 4.4 (a) TMM simulation of the VCSEL cavity. (b) Expanded view of region near semiconductor-air interface. The emerging wave A from the semiconductor must be in phase with the reflected wave B returning from silicon HCG to maintain resonance. 44

Figure 4.5 Radially-symmetric COMSOL FEM simulation modeling temperature distribution in VCSEL using 45 mW heat source in active region. (a) Bonded Si-HCG VCSEL on SOI substrate; active region z=0 μm, DBR extends from0.8<z<11.3 μm, air z>11.3 μm (since InP substrate is removed), thermal oxide -3>z>-4 μm, silicon substrate z<-4 μm, and 350 μm thick. (b) Standalone III-V VCSEL with InP substrate; structure has air above active region from z>0.8 μm, DBR extends from -0.8>z>-11.3 μm, InP substrate z<-11.3 μm, and 350 μm thick. 45

Figure 4.6 Maximum temperature vs DBR quaternary alloy thermal conductivity. The standalone III-V structure reaches higher temperature for DBR thermal conductivities below 7.2 W/mK. 45

Figure 4.7 TRIM simulation of H^+ implanted at 310 KeV with a dose of $2e^{14}$ ions/cm^2. 46

Figure 4.8 Silicon HCG VCSEL fabrication process flow. The heterogeneous process involves 9 lithography steps. 47

Figure 4.9. (a) Tilted-view colorized SEM of Si HCG reflector (blue hue) surrounded by AuSn film (orange hue). (b) SEM of fabricated Si-HCG VCSEL highlighting the active region in red, the III-V material in blue, and the corresponding p- and n-contacts in orange, and yellow, respectively. 48

Figure 4.10 (a) SEM cross-section of Si-HCG reflector showing shallow sidewall sloping after dry etching process. (b) FDTD simulation of sidewall slopes from 0 to 12° indicating high reflectivities across the spectrum. The actual HCG parameters a_{top} and a_{bottom} are used to model the HCG structure indicated by the dashed black line. 48

Figure 4.11 Temperature dependent CW LIV of Si HCG VCSEL from 15 to 60 °C. Top insets show near field intensity below and above threshold; bottom inset is confocal microscope image of fabricated VCSEL indicating emission direction. Light is collected with a large-area Ge photodiode for the LI measurement, and a 100X objective onto an InGaAs CCD for near field imaging. 49

Figure 4.12 The normalized near-field profile of the Si-HCG VCSEL. Light is collected through a 100X objective and imaged by an InGaAs CCD camera set to 10 μS integration time. The measured FWHM collapses from 11.4 μm (below threshold) to 4.7 μm at 11 mA bias (lasing). The proton-implant aperture is 7 μm in radius. 50

Figure 4.13 Spectrum at different (a) heat sink temperatures and (b) bias currents. Wavelength peaks are recorded to measure shift for varying injection biases, and heat sink temperatures, shown in the insets. The wavelength shift versus temperature is 0.098

nm/K, and the shift versus dissipated power is measured to be 0.143 nm/mW. The experimental thermal resistance of our device is 1.46 K/mW. 51

Figure 4.14 (a) Small signal direct modulation (S21) for Si HCG VCSEL at 20 °C for different current biases. A resonance frequency f_R= 2.5 GHz, parasitic pole frequency f_p=1.4 GHz, and damping factor γ=9.6x109 s^{-1}, are extracted from the family of curves. (b) D-factor fitting of VCSEL exhibiting thermal damping at 5.4 GHz. (c) BER measurements up to 5 Gb/s using On-Off-Keying (OOK) and eye diagrams before (back-to-back) and through a link of 2.5 km SMF. 52

Figure 4.15 (a) The schematic for the VCSEL on a flexible substrate. The VCSEL is embedded inside PDMS with the top surface exposed. (b) Photograph of the measurement setup. 53

Figure 4.16 (a) The LIV curve of the VCSEL embedded in PDMS. The threshold current is 8 mA and the maximum output power is 0.65mW with 13.2 mA bias current. (b) The optical spectrum of the VCSEL embedded in PDMS. The device is lasing at 1563.3 nm with 11mA bias current. 53

Figure 4.17 Biasing schematic of tunable Si HCG VCSEL. 54

Figure 4.18 Tilted-view SEM of HCG reflector from a 75° viewing angle. AuSn is colorized in orange, silicon HCG in blue. The silicon device layer has been released in HF vapor. (Left) stand-alone HCG reflector. (Right) Reflector/coupler with waveguide. The sharp taper inhibits unwanted reflection and terminates the channel. 54

Figure 4.19. SEM of suspended HCG. 55

Figure 4.20 Restoring force versus electrostatic force. Stability conditions are highlighted in blue (stable) and red (unstable). 56

Figure 4.21 Beam length vs spring constant, k, and pull-in voltage maintaining a fixed beam width of 1 μm. Beam width versus spring constant, k, and pull-in voltage, maintaining a fixed beam length of 15 μm. 57

Figure 4.22 Family of curves of spring constant k for (a) variety of beam widths, and (b) variety of beam lengths. 58

Figure 4.23 Close-up SEM image of released HCG reflector before actuation. 59

Figure 4.24 Confocal images of HCG MEMS actuator during a voltage sweep from 0 to 45 V. Pull-in failure occurs at 45 V, indicated by the purple region where the HCG bars experience stiction failure to the silicon substrate. 59

Figure 4.25 Confocal microscope 3D image of silicon HCG reflector biased at 0 V and 35 V. The HCG is displaced 380 nm below the original Si device layer. Up to 464 nm of displacement is achieved before pull-in failure at 45 V. 60

Figure 4.26 CW LIV of Si HCG VCSEL with suspended HCG from 0 to 20 mA. Threshold current is 2.3 mA, and peak CW power is 0.36 mW at 11.8 mA forward injection current. Light is collected with a large-area Ge photodiode for the LI measurement. 60

Figure 4.27 Spectrum of Si HCG VCSEL at different V_{MEMS} bias voltages, ranging from 0 to 45 V. Wavelength peaks are recorded to measure shift for varying V_{MEMS} bias. 61

Figure 4.28 (a) Cross section schematic of All HCG VCSEL on SOI. Because the cavity can be as short as 3 μm, this can also provide gains in MEMS tuning efficiency and faster high-speed direct modulation. (b) 3-D view drawn to scale. The BOX layer (grey) is 1 μm. 62

Figure 4.29 Overlap factor is 3.33%. Resonant cavity at 1523 nm. The photo luminescent (PL) peak of the epitaxial structure is located at at 1510 nm. 62

Figure 4.30 (a) TRIM Monte Carlo simulation showing the skewed normal distribution versus depth of H^+ ions implanted at 225 KeV into the all-HCG epitaxial stack. (b) The range versus implant energy, including lateral straggle. (c) The distance from the active region quantum well (QW) including radial straggle. 63

Figure 4.31 Infrared image of LEDs captured with an InGaAs CCD camera. For two implant energies. The 225 KeV implant energy provides much better current isolation. The implant dose used is $1x10^{13}$ cm^{-2}. The current injection bias is 25 mA. 64

Figure 4.32 I-V graphs for LEDs for various proton implant doses (in species/cm^2). The differential resistance of the devices is ~ 40 Ω. 65

Figure 4.33 All-HCG fabrication process flow. The heterogeneous process involves 11 lithography steps. 65

Figure 4.34 A confocal optical image of the fabricated device. 66

Figure 4.35 (a) Room temperature LIV measurement of all-HCG devices at different bias currents. Incremental current sweeps (0-3 mA, 0-4 mA, etc.) were performed on the device. (b) Infrared image of device under 2 mA bias and 100X magnification showing a well-defined proton-implanted aperture. 66

Figure 5.1 Schematic of wavemeter for a silicon photonics platform. The device is a four port coupler with a high-contrast metastructure in between single mode silicon waveguides. Light is collected by germanium photodetectors at exit ports. The footprint is roughly 20 x 2 $μm^2$. 68

Figure 5.2 Schematic of dielectric grating coupler into thin film waveguide. Light is incident at an angle θ onto dielectric gratings (light blue). A low index spacer (yellow) separates the diffractive structure from the thin film waveguide (dark blue). Schematic courtesy of Li Zhu. 69

Figure 5.3 Effective indices versus wavelength of a slab waveguide that is 230 nm thick, and a strip waveguide that is 230 nm thick by 300 nm wide. 70

Figure 5.4 Coupling angle versus wavelength for a dielectric grating coupler above a Si strip waveguide surrounded by silicon dioxide, with waveguide dimensions of 230 nm x 300 nm, and grating coupler period Λ = 775 nm. 70

Figure 5.5 Proposed scheme for a compact four-port coupler. Top view of silicon device layer. Incoming light arrives at Port 1. The power rations between Port 3 and Port 2 (P_3/P_2) and P_2/P_4 can be used to determine the wavelength of light. 71

Figure 5.6 Cartoon illustration of the cross-section of Sandia's SPP1 process with a subset of possible implant configurations. 71

Figure 5.7 Wavemeter parameters. *w*, the waveguide thickness; *g*, the spacing gap between waveguides and the HCM; t_g, the thickness of the HCM in the y-axis; *s*, semiconductor width of the HCM bars (duty cycle); and Λ, the period of an HCM. 72

Figure 5.8 Cross section of the waveguide with the neighboring HCM. The electric field intensity is plotted along the y-z cross section of the waveguide. The propagation direction is along the x axis..... 73

Figure 5.9 Electric field component along vertical E_z direction. 73

Figure 5.10 Parameter sweep of waveguide width versus lambda. The dashed white line corresponds to a waveguide width *w* of 300 nm. 74

Figure 5.11 Parameter sweep of HCM thickness t_g versus lambda. The dashed white line corresponds to an HCM thickness t_g of 985 nm..... 75

Figure 5.12 Parameter sweep of HCM period Λ versus lambda. The dashed white line corresponds to an HCM period Λ of 820 nm. 76

Figure 5.13 Parameter sweep of HCM bar width, *s*, versus lambda. The dashed white line corresponds to an HCM bar width *s* of 500 nm. 77

Figure 5.14 Summary of HCM wavemeter designs. Designs A and B have the same period and duty cycle, but different number of bars. Designs C and D have a larger period. Designs E and F have a chirped period while maintaining a constant duty cycle, and can be considered a combination of designs B-D, and A-C, respectively. Designs G and H employ a smaller duty cycle (48.1%)..... 78

Figure 5.15 FDTD simulation of HCM wavemeter. (a) Top view of structure using an electric field intensity monitor at a single wavelength. (b) Power collected at P_2 and P_3 for a wavelength sweep from 1.5 to 1.6 μm. (c) Monotonic intensity-independent power ratio between ports 2 and 3..... 79

Figure 5.16 (a) Confocal image of silicon photonics chip. (b) Mask layout. 80

Figure 5.17 BOSCH trench. (a) Top view with confocal microscope. Measured depth is 236 μm. (b) Side view with SEM. Measured depth 223 μm..... 80

Figure 5.18 Wavemeter Design D with resistive heater in vicinity. The rightmost illustration is a confocal microscope image of the wavemeter at 100X magnification..... 81

Figure 5.19 Measured power ratios between Port 3 and Port 2 for a wavelength window of 5 nm..... 82

Acknowledgments

My first memory of UC Berkeley was a lunch during the spring Visit Day in 2008. I sat next to a wise professor who asked me what I wanted to do with life. Daunted by the loaded question, I gave a vague answer, indicating that I did not yet know which specialized field I wanted to pursue. The wise professor, without blinking, cocked her head and said, "My advice to you is: don't be a dangling bond." I immediately knew I wanted to work with the wise professor. And so here we are now.

I would like to thank my advisor, Professor Connie Chang-Hasnain, for being, as they say in Ireland, "like a father and mother to me" for this very special time of my life. In particular, I want to thank her for believing in me when even I wouldn't believe in myself, and for figuring out how to motivate me, be it with a series of spontaneous deadlines, or impossible wagers and bets that somehow would ignite a competitive urge within that resulted in extreme productivity. I have enormous gratitude for her leadership and ever-victorious attitude, particularly since she always leads by example. Professor Chang-Hasnain is inspiring, and makes one feel like there is literally nothing that can't be done.

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To my family, my mom, dad, and siblings: thank you for all the words of encouragement, for providing such a tight-knit fabric of support, showing me what it means to work hard, and being the paradigm that I can only dream of emulating, someday, with a family of my own. To H and H.J., if it weren't for you, I would be editing this dissertation for two more years. To Luna, for always greeting me, no matter how late at night – or early in the morning for that matter – with excitement to wash away any setbacks encountered in the lab. To my better half, Nicole, without your undying support, the morning coffees, your bubbling attitude and infectious energy, and your endless optimism, none of this would be possible: "hakira me-ne-oh!"

Thank you all.

Chapter 1

Introduction

"Let's hunt the tiger.
Not the ducks, not the deer.
The birds are good too.
Focus on the largest animal."

In recent years, there has been a deluge of data generated from all over the world, by research centers, businesses, and consumers alike [1]. For example, the European Organization for Nuclear Research (CERN) has generated over 100 petabytes of physics data in the last 20 years. However, from 2010-2013, the Large Hadron Collider (LHC) *alone* generated 75 petabytes of data – a measure equivalent to 700 *years* of full HD-quality movies [2]. While the petabytes of data generated in scientific endeavors, such as these, are at the forefront of "big data", healthcare data is not far behind, with the generation of high-definition medical images such as MRI and CT scans, as well as with the use of artificial intelligence analytics, which must tap into vast databases of information, such as IBM's "Watson" [3].

However, it has been with the advent of cloud computing solutions, countless social networks, and on-demand video streaming services that an explosion in the generation and transmission of data has truly occurred. The Internet population has seen a compounded growth in users reaching numbers in the billions, especially due to the ubiquitous presence of smart devices, such as cellular phones and tablets, which have multiple ways of communicating with each other, be it through cellular phone networks or Wi-Fi. The capability of smart devices to capture high definition video and continuously upload them to seemingly endless-storage cloud-based systems, which in hand can stream hours and hours of video back to users *instantaneously,* has posed a great challenge to communication networks.

Figure 1.1 shows an infographic representing the amount of data generated every minute by social networks. At the time of writing of this dissertation, 300 hours of video were being uploaded to YouTube every minute [4]. Figure 1.2 shows Cisco's Visual Networking Index (VNI) for 2015. It is expected that by 2018, total internet traffic will be 3 times larger than in 2013 [5]. Furthermore, it is projected that consumer video alone will account for more than 89 exabytes of monthly traffic. This staggering amount of data will pose a daunting challenge for high-speed communication channels.

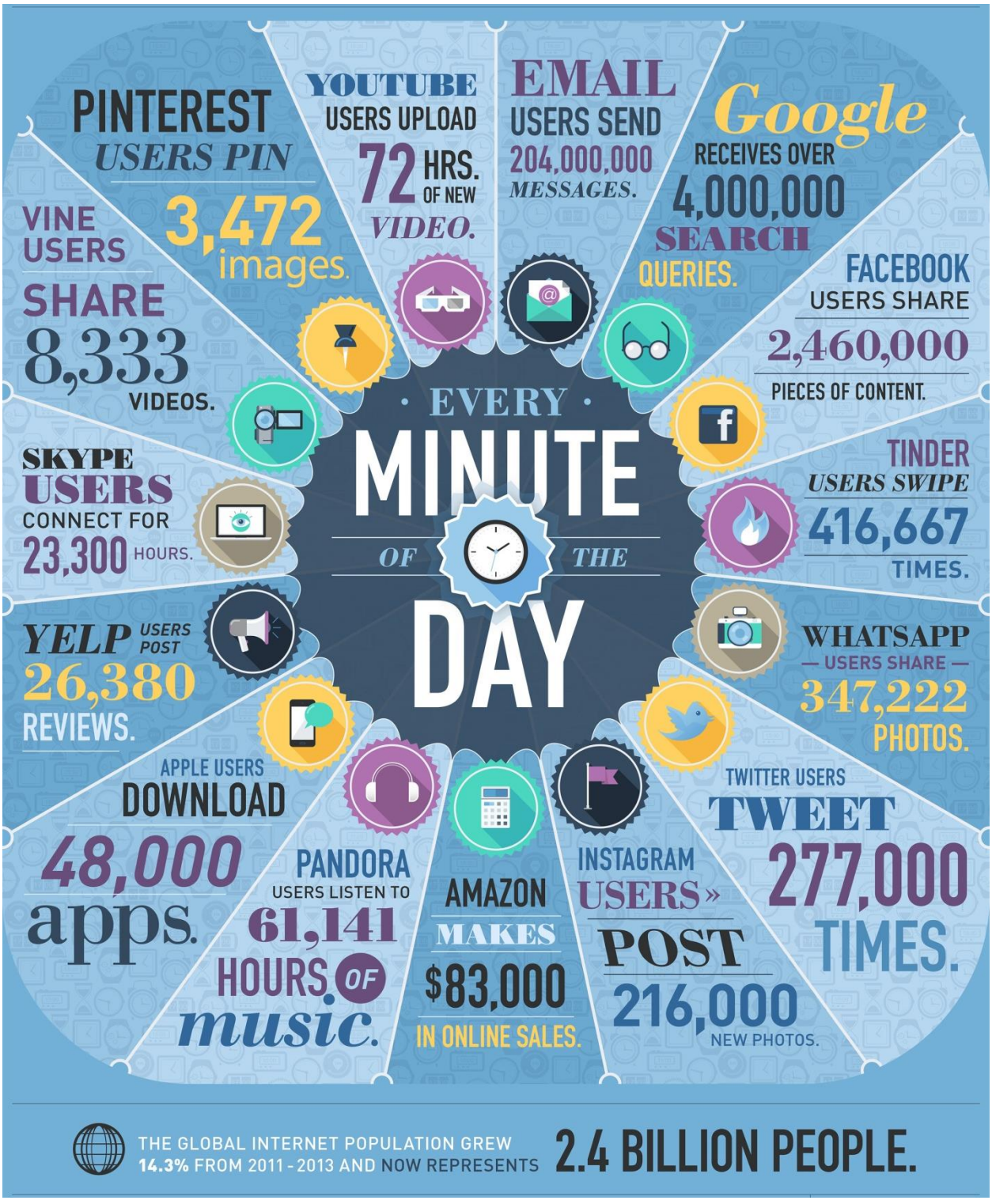


Figure 1.1 Infographic representing the amount of data generated every minute, in 2014 [6].

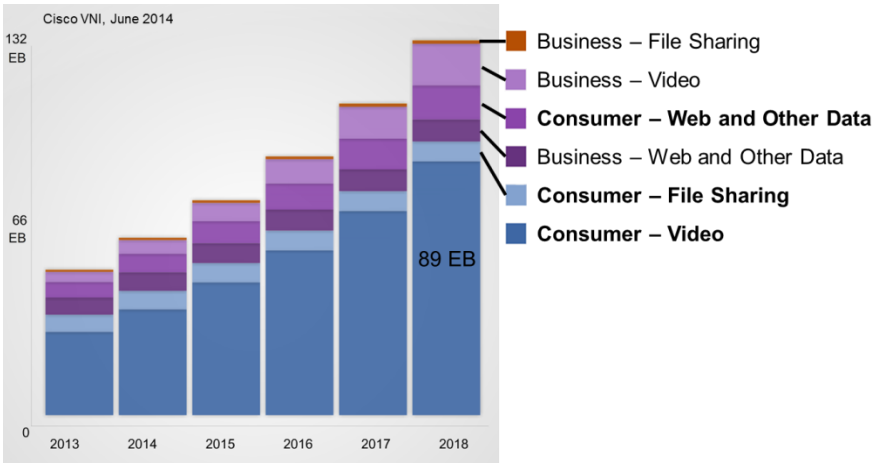


Figure 1.2 Cisco's Visual Networking Index (VNI) projects that by 2018, total traffic will be 3 times larger than 2013 [7].

Notwithstanding, the speed of which copious amounts of data are being transmitted is not the only challenge being faced by communication networks. There are also significant costs associated with the transport of bits at high data rates, and the costs are not only fixed by the hardware used, but also by the power consumed. Large data centers are now being built in climates and environments that offer natural cooling solutions to offset the staggering costs of operation [8]. The trend is for markets to not only consider the bits per second, but also the amount of joules per bit [9].

The trends that once replaced the bandwidth limitation of electrical cables over long distances with optical fiber-based communications, are also pointing towards alternatives to replace short-reach metal interconnects with optical ones [10]. Currently, there is aggressive competition between metal interconnects and optical interconnects at the board level. Heroic efforts in the scientific and industrial community are going into developing optical systems that may one day supplant copper at very short distances, perhaps even within a chip. At the chip-level, metal interconnects now reach 13 levels of metallic stacks (Figure 1.3).

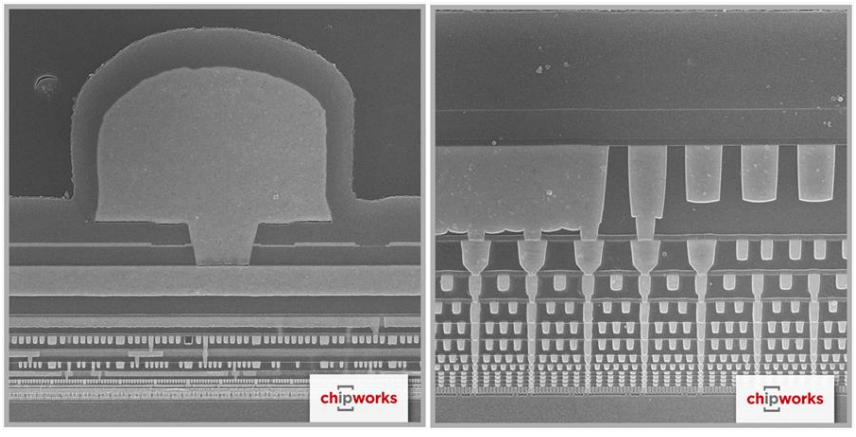


Figure 1.3 Dense metal interconnects (13 levels) in the Broadwell processor. [11]

Densely integrating devices on a single chip enables both complex functionality and economies of scale. This principle has been a driving force for the electronics industry, and it is certain to translate to photonic integrated circuits (PICs) as well. By combining components that generate, detect, and otherwise control light, PICs facilitate design of photonic architectures that prove far more powerful than any single photonic element alone. Already, they have sparked great interest for communications and computing technology. Other rapidly emerging applications meanwhile include light detection and ranging (LADAR), optofluidics, and wearable optoelectronics.

One of the principal research fields addressing the needs of high-speed data links is silicon photonics. Over the past few years, tremendous effort has gone into the development of various optical building blocks for the silicon photonics platform. Part of the allure is that photonics circuits on silicon can be very small due to the high refractive index of silicon, and can leverage over 5 decades of scaling and existing silicon microelectronics infrastructure.

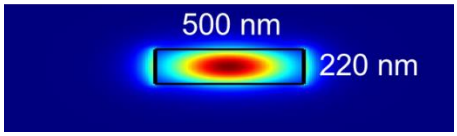


Figure 1.4 Silicon nanophotonic waveguide supporting a single TE mode. The area of this waveguide has a 714X size reduction when compared to a single mode fiber.

The benefits of monolithic integration of passive silicon photonics, active photonic components, and electronic logic on the same chip include scattering and heat loss minimization, assembly cost and physical footprint reduction. Silicon photonics fabricated in silicon-on-insulator (SOI) is believed to provide the necessary technology bridge between electronics and photonics. As such, photonic integrated circuits (PICs) on silicon have the likely target of addressing the ever-growing high-bandwidth needs of servers and data centers, where the high-volume processing of a silicon platform and the low cost of traditional optical communications could redefine the constraints for high-performance computing interconnects.

High contrast metastructures (HCMs) are an emerging solution for flat integrated photonic devices. Also known as high contrast gratings (HCGs), these ultra-thin semiconductor ribbons can exhibit extraordinary properties that are atypical to traditional optical gratings, such as very broadband reflection at normal and shallow angles, high-Q resonances, and a readily engineered phase response [12]. These properties have allowed for the design of a variety of novel optoelectronic devices such as vertical cavity surface emitting lasers (VCSELs), flat lenses, all-pass filters and phase-arrays, and sensors.

In this dissertation, silicon HCMs are employed to integrate active III-V semiconductor photonics with the silicon photonics platform. In the next section, we provide an introduction to HCMs, their properties, and a few applications which can provide a major step towards complex optoelectronics integration.

1.1 High Contrast Gratings

A high contrast grating (HCG) structure consists of a single near-wavelength grating made from an ultra-thin high-refractive index material embedded in a low-index medium, as shown in Figure 1.5.

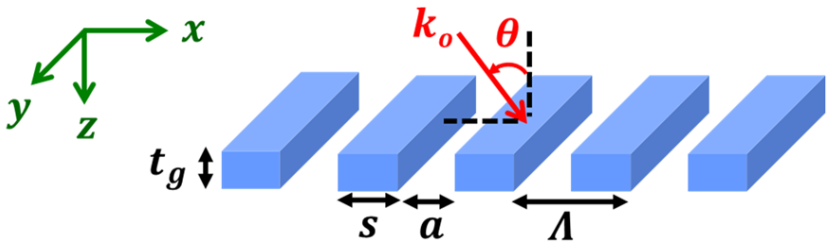


Figure 1.5 Schematic of HCG, where Λ, HCG period; s, bar width; a, air gap width; t_g, HCG thickness.

The grating bars can be considered as a periodic array of waveguides along the z-direction. Upon plane wave incidence, only a few waveguide array modes are excited. Due to a large index contrast and near-wavelength dimensions, there exists a wide wavelength range where only two modes have real propagation constants in the z-direction and, hence, carry energy. This is the regime of interest, and is referred as the dual-mode regime. The two modes then depart from the grating input plane (z = 0) and propagate downward (+z-direction) to the grating output plane (z = t_g), and then reflect back up. The higher order modes are typically below cutoff and have the form of evanescent surface-bound waves. After propagating through the HCG thickness, each propagating mode accumulates a different phase. At the exiting plane, due to a strong mismatch to the exiting plane wave, the waveguide modes not only reflect back to themselves but also couple into each other. As the modes propagate and return to the input plane, similar mode coupling occurs. Following the modes through one round trip, the reflectivity solution can be attained.

For an HCG infinite in the x-y plane, due to its subwavelength period in air, only the 0th diffraction order, i.e. plane wave, carries energy in reflection and transmission. The HCG thickness determines the phase accumulated by the modes and controls their interference, making it one of the most important design parameters. To obtain high reflection, the HCG thickness is chosen such that destructive interference is obtained at the exit plane, which cancels transmission. For full transmission, on the other hand, the thickness should be chosen such that the interference is well matched with the input plane wave at the input plane. Figure 1.6 (a) shows surface normal reflectivity spectra contour as a function of HCG thickness. It can be seen that reflectivity assumes a well-behaved checker-board pattern as a function of thickness and wavelength, both normalized to grating period (Λ). This somewhat periodic dependence on thickness attests to the mode interference effect.

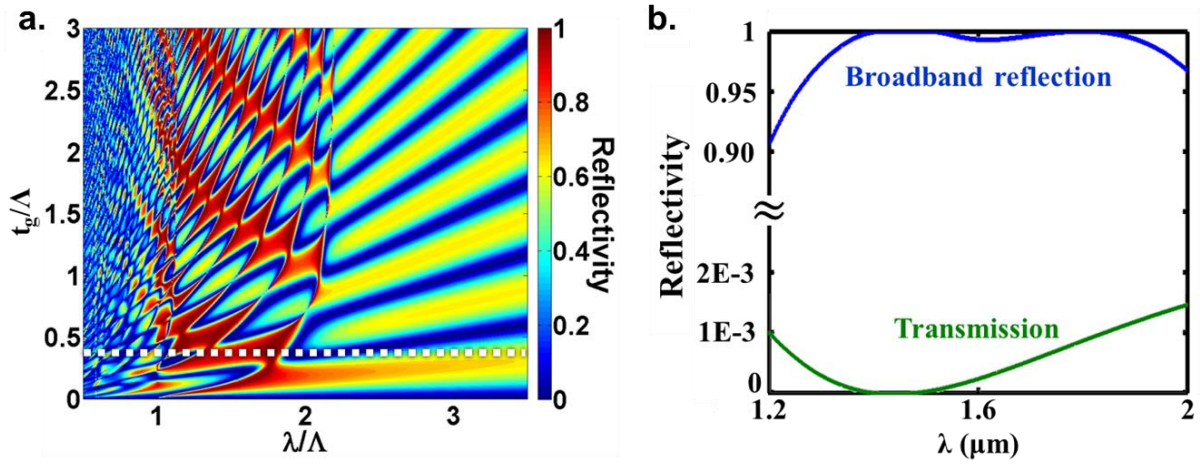


Figure 1.6 (a) Reflectivity contour plot of HCG versus normalized wavelength (λ/Λ) and normalized thickness (tg/Λ). The white dotted line indicates a suitable design for broadband reflection. (b) Reflectivity spectrum for HCG designed for broadband reflection (blue) and broadband transmission (green).

While the above analysis and simulation is for an infinite HCG, the boundary conditions of a finite size HCG can lead to reduced reflectivity and Q value. Nevertheless, reasonably high values have been reported for surface-normal reflection in VCSELs with as few as 4 periods totaling an HCG area of 3×3 μm^2 [13], [14].

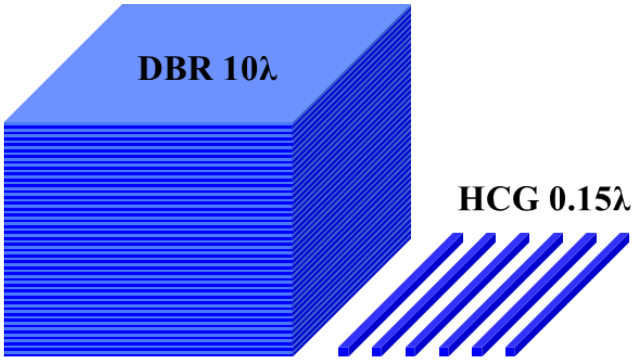


Figure 1.7 Schematic of traditional long-wavelength distributed Bragg reflector with 40 pairs of thin films (~ 10λ), side-by-side with HCG reflector (15% λ).

The boundary conditions due to the finite size can, on the other hand, be leveraged into coupling to the in-plane propagation direction by matching the k-value in the x or y direction with the propagation constant of an in-plane waveguide [15]. In Figure 1.8(a), we show a design that can provide lateral coupling on the same silicon (high index) layer. The finite-difference time-domain (FDTD) simulation in Figure 1.8 (b) shows that this HCG design provides both high out-of-plane reflectivity for a VCSEL, as well as efficient coupling into a silicon in-plane waveguide. We define total output as the power that is not reflected from the grating. At 1550 nm, the HCG reflects >99.4% of the light, and couples 47% of the output power into two opposite traveling in-

plane waveguides. The remaining 53% output power is transmitted through the HCG as vertical output, as shown in Figure 1.8 (c), which can be suitable for off-chip applications such as integrated 3D imaging systems[16].

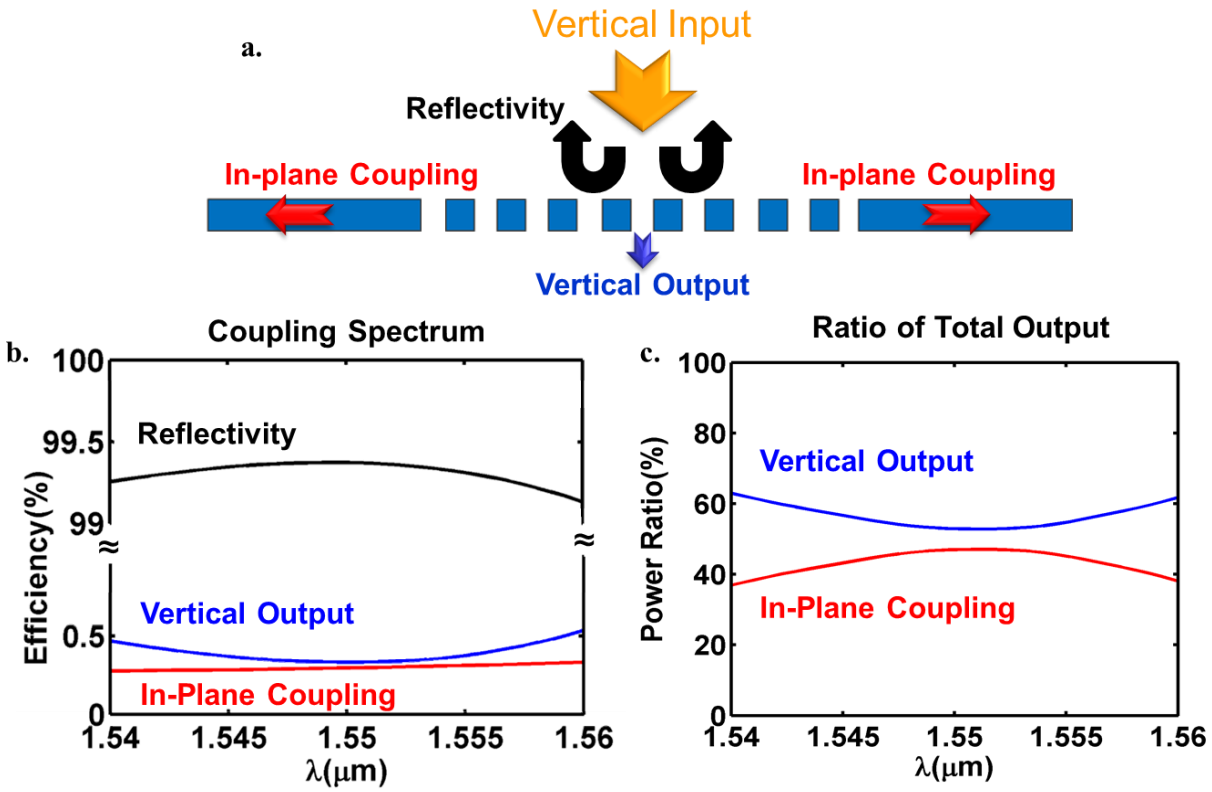


Figure 1.8 HCG reflector and coupler simulation with FDTD. (a) Schematic indicating incident beam as vertical input. The HCG layer consists of a 358-nm thick silicon layer on an SOI substrate. The HCG is designed to have 863 nm period and 0.6 duty cycle. (b) >99.4% reflectivity for VCSEL. (c) 47% of the output power is coupled to bi-directional waveguides.

The broadband high reflectivity also holds for glancing angle reflections. One application for this property is in hollow-core waveguides, which will be described thoroughly in Chapter 2. Here we focus on the design tolerance for glancing angle high broadband highly reflective HCGs. We use rigorous coupled wave analysis (RCWA) [17] to simulate a silicon HCG structure (index n=3.46) suspended in air (n=1). Figure 1.9 is a collection of reflectivity contour plots for light incident at 81.08° from normal (glancing angle), which corresponds to waveguide core width of 5 μm using a ray optics mode solution for a perfect reflector at a wavelength λ of 1.55 μm from Equation (1.2).

$$\frac{2\pi}{\lambda}\sin(\theta)d = m\pi \tag{1.1}$$

$$\theta = \arcsin\left(\frac{m\lambda}{2d}\right) \tag{1.2}$$

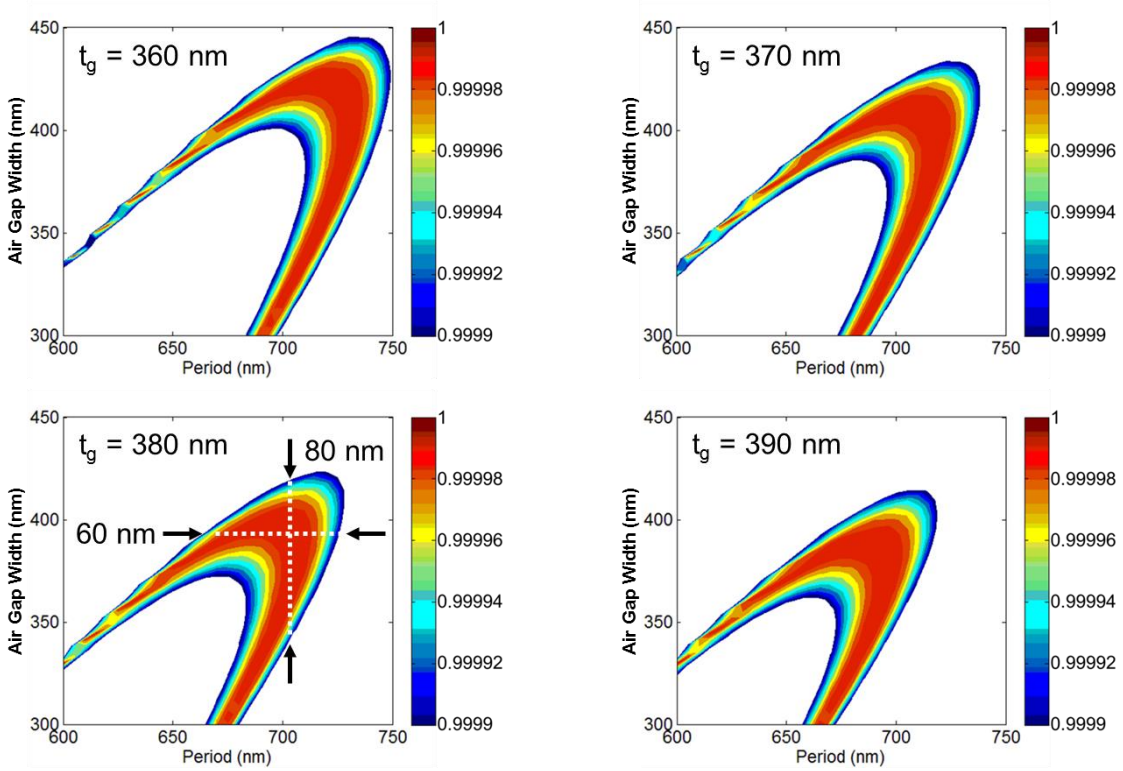


Figure 1.9 Reflectivity contour map for HCG parameter space in period and air gap width (inverse duty cycle), for designs with reflectivity greater than 99.99% for TE polarized light (electric field along the grating direction). An HCG with a thickness of 380 nm can have very high reflectivity for a variation of period of 80 nm, as well as 60 nm in air gap width.

The plots in Figure 1.9 show a grating thickness sweep from 360 nm to 390 nm in 10 nm steps. The period is sweep from 600 nm to 750 nm and the air gap width, which can be considered as the reverse duty cycle of the periodic structure, is swept from 300 nm to 450 nm. It should be noted that the Berkeley Microelectronics Laboratory had an ASML deep ultraviolet (DUV) step-lithography tool capable of resolving a 350 nm linewidth, whereas the current Marvell Nanofabrication Laboratory ASML DUV step-lithography tool can resolve down to 250 nm linewidths. The contour plots reveal large very-high reflectivity windows well within the fabrication tolerances of these ASML stepper tools. The HCG is quite tolerant to design variation. For instance, an HCG design with a 710 nm period and a 390 nm air gap (45.01% duty cycle) can stray by 80 nm in period, and 60 nm in air gap linewidth before dropping below 99.99% reflectivity!

Furthermore, the next set of figures (Figure 1.10 - Figure 1.13) explore the HCG parameter space for designs tolerant to deviations in period and air gap by ± 10 nm, while maintaining a propagation loss < 0.1 dB/m, which corresponds to a reflectivity greater than 99.9997% in a 10 μm waveguide (85.56°), and 99.9993% in a 15 μm waveguide (87.04°). The formulation to calculate propagation loss is also described in Chapter 2.

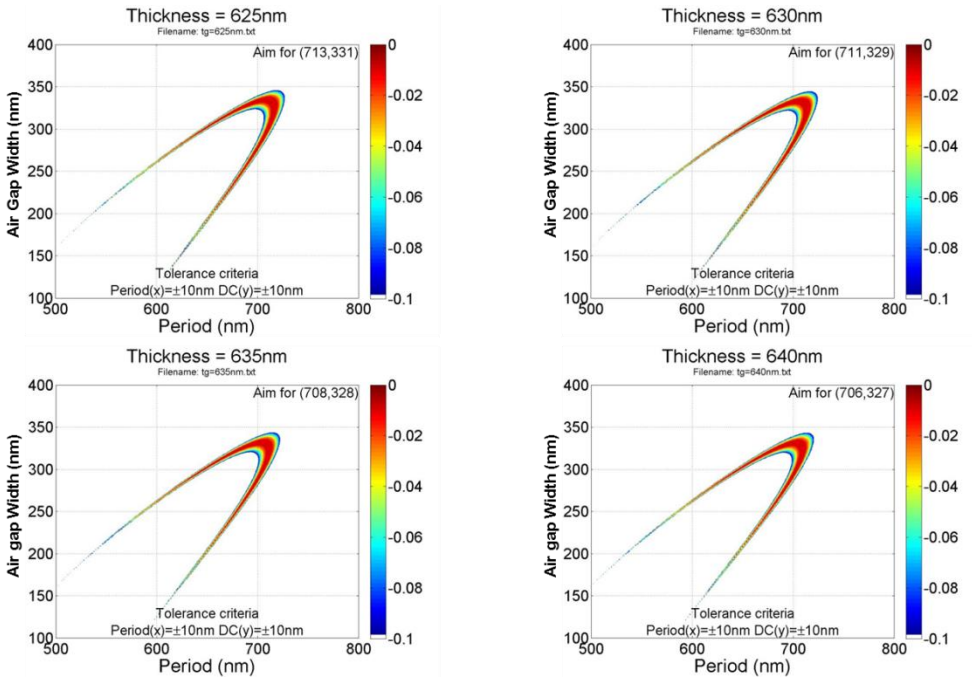


Figure 1.10 HCG parameter space search for designs tolerant to deviations in period and air gap by ± 10 nm, while maintaining a propagation loss < 0.1 dB/m. TE polarization and 10 µm waveguides.

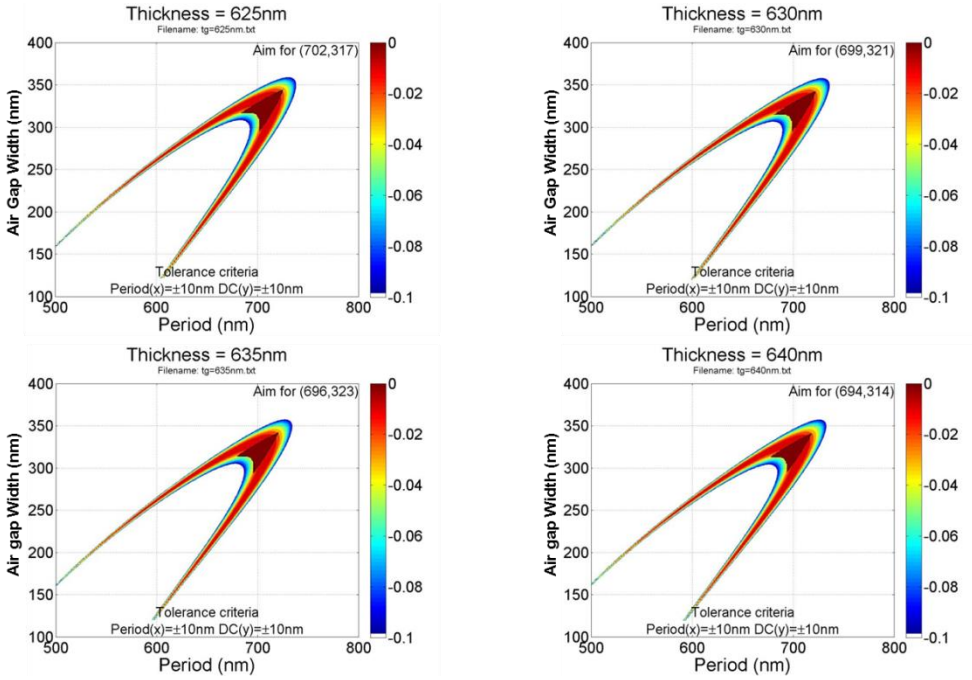


Figure 1.11 HCG parameter space search for designs tolerant to deviations in period and air gap by ± 10 nm, while maintaining a propagation loss < 0.1 dB/m. TE polarization and 15 µm waveguides.

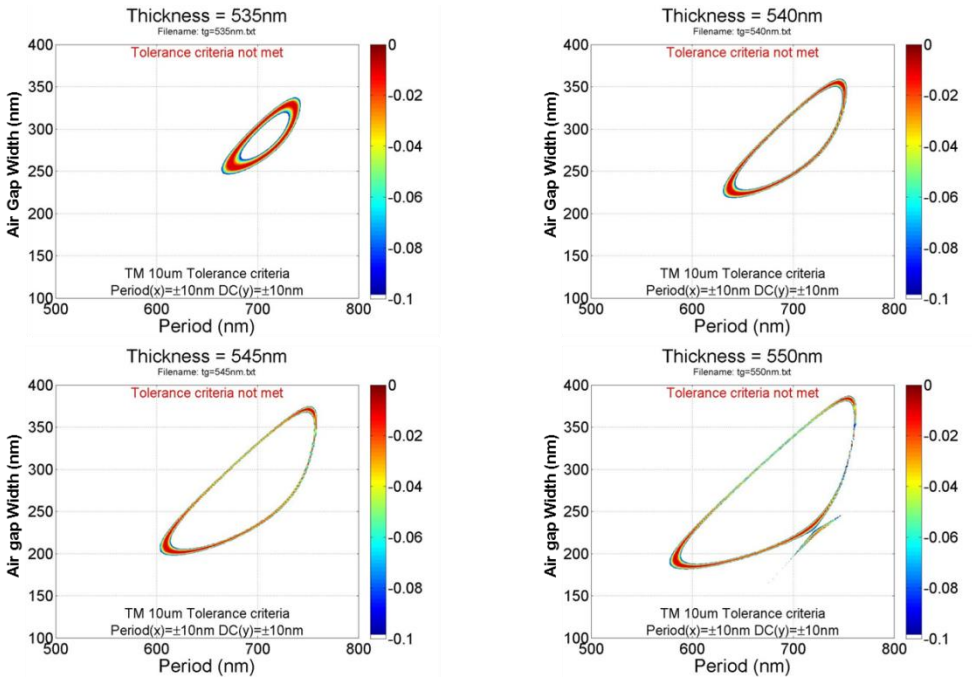


Figure 1.12 HCG parameter space search for designs tolerant to deviations in period and air gap by ± 10 nm, while maintaining a propagation loss < 0.1 dB/m. TM polarization and 10 µm waveguides.

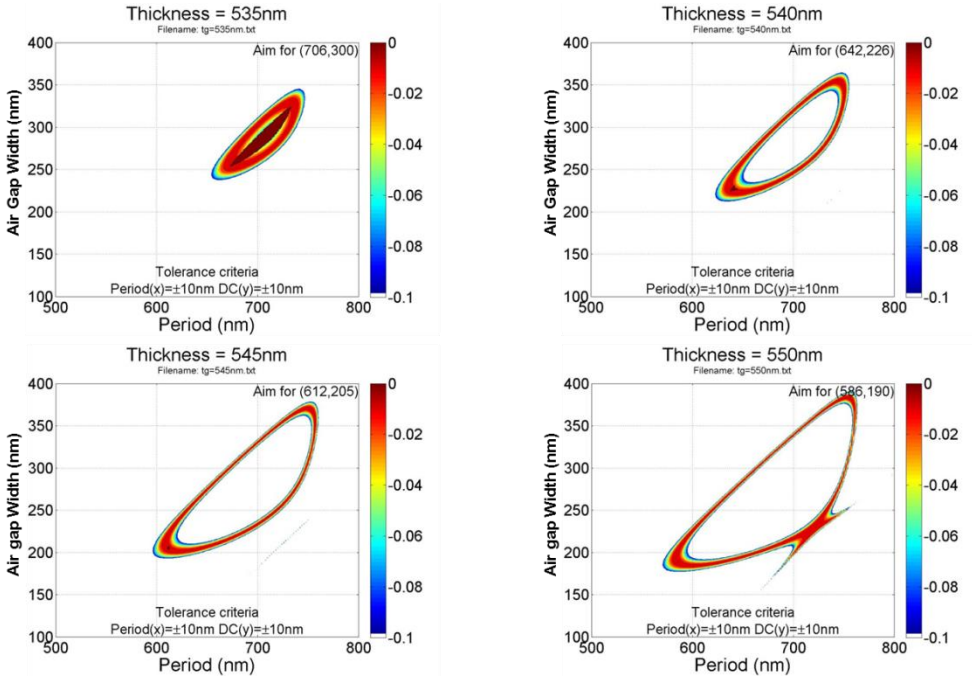


Figure 1.13 HCG parameter space search for designs tolerant to deviations in period and air gap by ± 10 nm, while maintaining a propagation loss < 0.1 dB/m. TM polarization and 10 µm waveguides.

We can make two conclusions from the sets of plots presented in the previous four figures. First, a 15 μm core waveguide has a much lower propagation loss than a 10 μm core, and much larger design tolerance. This is because in principle, a larger core has a smaller glancing angle, and requires fewer bounces per length between successive HCG reflections. Second, the gratings are indeed quite sensitive to the field polarization from the incident wave. Figure 1.10 and Figure 1.10Figure 1.11 are simulations of TE-polarized light incident on the gratings, and show fabrication-tolerant designs at a grating thickness t_g of ~ 625 to 640 nm, with a large window of periods and duty cycles. TM-polarized light, however, only has a tolerant design at a thickness t_g of 535 nm, and the design window closes rapidly in both period and duty cycle space. Both of these topics will be presented in Chapter 2 Low Loss Hollow-Core Waveguide.

Another realization is that grating dimensions can be readily fabricated using DUV lithography, and are not limited to e-beam resolution systems. Figure 1.14 shows a 3-D rendering of the HCG parameter space for dimensions that offer propagation losses lower than 0.1 dB/m. There are 3 design windows available for fabrication. Figure 1.15 (a) and Figure 1.16 (a) show the 2-D slices of the parameter space, sweeping air gap versus thickness, and period versus thickness, respectively. If the dimensions lie below the critical dimension (CD) of a lithography tool, the grating dimensions can be scaled with wavelength. In Figure 1.15 (b) and Figure 1.16 (b), the RCWA simulation is repeated for a longer wavelength at 1610 nm. The shift is less than 4%, but more designs become compatible with the 350 nm linewidth limit. The beauty of the HCG and one of its unique properties is that, in principle, it can be scaled to the wavelength of choice to overcome fabrication constraints.

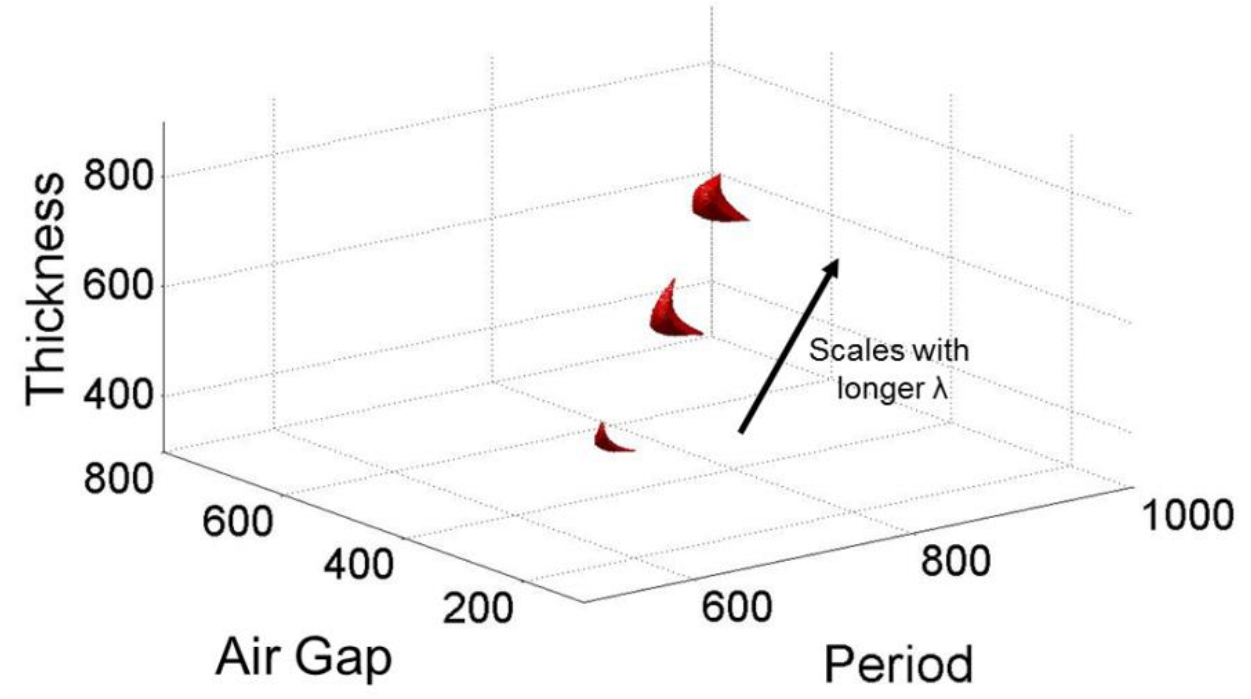


Figure 1.14 3-D parameter space of RCWA simulation for TE HCG reflector tailored for a reflection angle corresponding to a 15 μm thick waveguide.

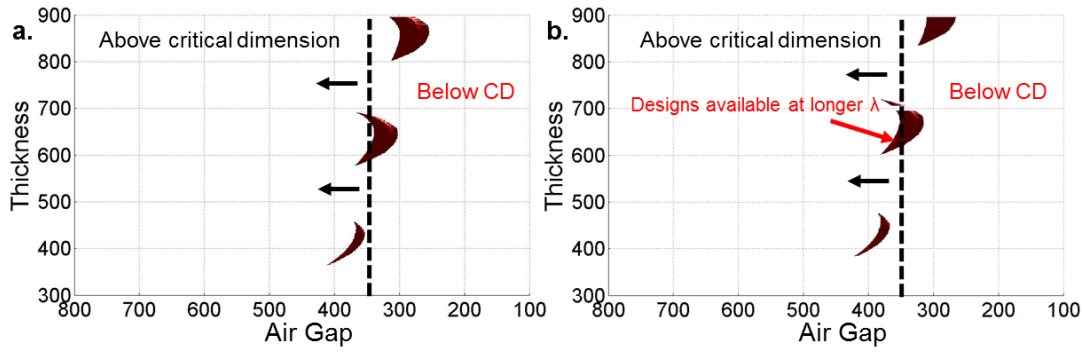


Figure 1.15 Corresponding 2-D slice sweeping air gap versus thickness. (a) 1550 nm, and (b) 1610 nm.

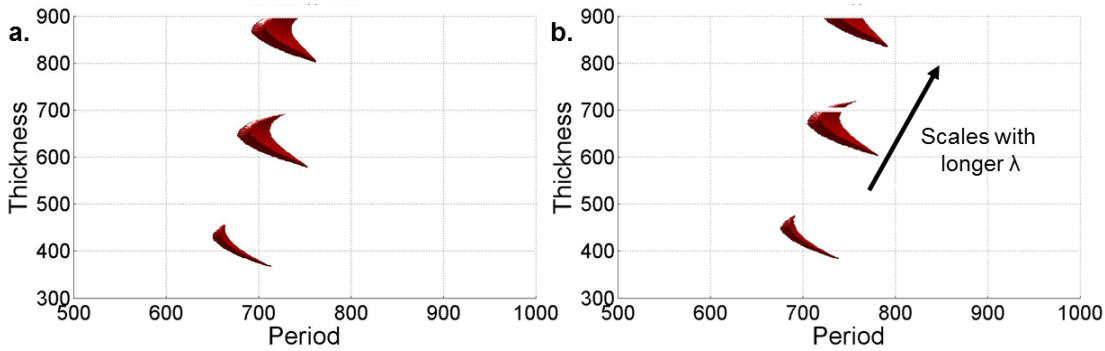


Figure 1.16 Corresponding 2-D slice sweeping period versus thickness. (a) 1550 nm. (b) 1610 nm.

1.2 Dissertation Overview

In this work, we explore three different types of novel HCMs *on silicon*. It should be noted that the terms HCM and HCG are used interchangeably, but fall under the same physical concept. The first is a hollow-core waveguide that can channel light at wavelengths where traditional solid waveguides encounter difficulties. The design, simulation, and fabrication of an HCG hollow-core waveguide prototype is covered in Chapter 2. Next is a silicon-based HCG VCSEL with the potential of being an efficient light source for silicon PICs. In Chapter 3 the pairwise integration of an HCG VCSEL on a silicon photonics chip is discussed, and in Chapter 4, the design, simulation, fabrication, and characterization of a hybrid VCSEL cavity based on a silicon HCG is described in detail. Lastly, preliminary results of an integrated wavelength meter, which can circumvent bulky off-the shelf instruments to provide wavelength characterization of guided light on a chip, is presented in Chapter 5. These devices are all possible due to the high reflectivity and broadband properties of the high contrast grating (HCG). The interference effects from modes excited in the HCG can results in complete cancellation of transmitted light and result in 100% reflection, for both normal and shallow incidence angles. The HCG is robust with respect to its design parameters, which makes it readily manufacturable in a variety of micro- and nano-fabrication laboratories, and compatible with scalable mass production.

Chapter 2

Low Loss Hollow-Core Waveguides

"Chicken to chicken, not chicken to eagle."

2.1 Introduction

Over the past few years, hollow-core waveguides (HCWs) have received much attention for their properties at wavelengths where traditional solid waveguides encounter difficulties, such as excessive optical absorption and undesirable non-linear effects. As gas sensors [18], they can provide an alternative to integrated-circuit technology, where electromagnetic interference and high temperature environments can be detrimental. Other applications include infrared high-power optical delivery and non-linear optics, where high beam intensities and long interaction lengths are desirable for increased light-matter interactions [19]. Many designs have been shown to efficiently confine light in a hollow-core waveguide such as photonic crystal fibers [20], [21], DBR reflectors [22], and ARROW waveguides [23], [24]. However, the reflection principles for these hollow-core waveguides require interactions with multiple layers of very precisely laid-out films, which can be cumbersome to fabricate and make them nearly impossible to form integrated optical components.

In this work, we present a novel form of hollow-core waveguiding that enables the possibility of chip-scale integration of light sources, detectors and electronics on a silicon platform. In an HCW, an optical beam is guided along a low-index medium by zig-zag reflections of the guiding walls[22], [25]. To attain low propagation losses, the sidewall reflectivity must be exceptionally high at the propagating wavelengths due to large numbers of bounces per unit length. High contrast subwavelength gratings (HCGs) have been found to offer very high reflection for surface-normal incident light [26]–[29], and recently, we reported numerical simulation results of a one-dimensional (1D) waveguide guided by two parallel layers of HCGs whose periodicity is parallel to the direction of propagation [25]. Top and bottom subwavelength HCGs separated by air and with periodicity perpendicular to the propagation of light are capable of reflecting light at shallow angles with extremely low loss. Our work demonstrates the light-guiding properties of HCG hollow-core waveguides with a novel form of lateral beam confinement that employs the effective index guiding method [30]. HCG HCWs are capable of bending light around curves without the aid of sidewalls. The lack of sidewalls is especially attractive for applications where gases or fluids have difficulty flowing into a device due to small core openings. The increase in speed for these waveguides can be increased by a factor of L^2/d^2, where the length L can be several orders of magnitude greater than d.

2.2 HCG HCW Design and Fabrication

Two parallel planar wafers are used to define straight and curved HCG HCWs, each containing a single layer of HCGs. The guided wave propagates along the HCG grating bars, as shown schematically in Fig. 1a, with lateral guidance provided by subtle HCG dimension variations that create an effective refractive index variation to confine light within a single mode. The design method is simple and intuitive, and does not require lengthy numerical simulation. The propagation loss in a straight waveguide with a 9-μm waveguide height is measured to be 0.37 dB/cm, the lowest loss for a small core HCW.

An HCG structure consists of a single layer of grating made from a high-refractive-index material (such as silicon), fully surrounded by a low-refractive-index material (such as air or oxide). They have been shown to be high reflection mirrors at normal incident angle for vertical-cavity surface-emitting lasers (VCSELs) [27]–[29]. Simulations show that HCGs retain their high reflection and wide bandwidth properties for glancing angles as well [25]. In this work, we demonstrate a rather counter-intuitive configuration with the propagation direction of the guided light being parallel to the HCG grating bars.

Fabricated on a silicon-on-insulator (SOI) platform, the gratings are formed on the silicon device layer above silicon dioxide (SiO_2). By placing two HCG-patterned wafers in parallel, separated by an air-gap d, shown schematically in Figure 2.1 (a), we have an HCW with the added freedom of controlling the waveguide core height d. The device arrangement provides a dynamic understanding of the HCG waveguiding concept, allowing for d to be varied in-measurement. Monolithic integration of HCG HCWs can be made possible through various bonding schemes or by using sophisticated multi-layer SOI wafer topologies.

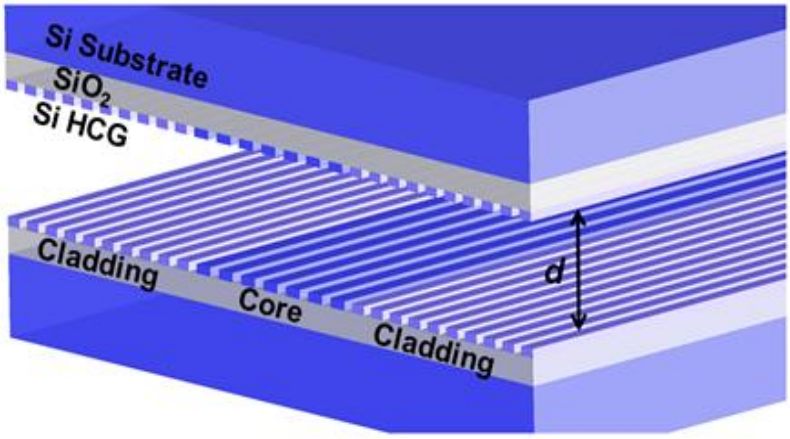


Figure 2.1 The HCG HCW. Schematic of an HCG HCW. The silicon HCG sits on top of a SiO2 layer and silicon substrate. Two HCG chips are placed in parallel with a separation gap d, forming an HCW. In the lateral direction, the core and cladding are defined by different HCG parameters to provide lateral confinement.

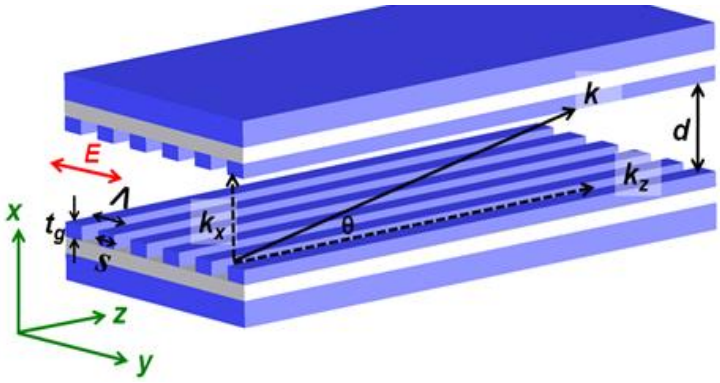


Figure 2.2 Ray optics illustration for a 1-D slab HCG HCW. The k vector is decomposed into the propagation constant k_z and transverse component k_x. θ is the angle between k and k_z; d is the waveguide height; E indicates the oscillation direction of the electrical field; Λ is the HCG period; s is the silicon grating bar width and t_g is the HCG thickness.

The waveguide design begins with a 1-D model using simple ray optics [25]. The propagation loss and the effective refractive index n_{eff} of the fundamental waveguide mode are given by:

$$Loss\left[dB/m\right] = -10\frac{\tan\theta}{d_{eff}}\log_{10}\left|r\right|^2 \tag{2.1}$$

$$n_{eff} = \cos\theta = \frac{k_z}{k} \tag{2.2}$$

As illustrated in Figure 2.1 b, θ is the angle between the ray and the waveguide, k_z is the propagation constant, k is the wave vector of the light in free space, and d_{eff} is the effective waveguide height. d_{eff} takes into account both the physical waveguide height d and the reflection phase φ_r, which is approximately π in general. The parameter d_{eff} can be calculated by the round-trip phase condition of the fundamental mode:

$$2k_x d + 2\phi_r = 4\pi \tag{2.3}$$

$$2k_x d + 2\phi_r = 2k_x d_{eff} + 2\pi \tag{2.4}$$

To first order, the ray angle θ can be determined from:

$$\frac{2\pi}{\lambda}\sin(\theta)d = m\pi \qquad \theta = \arcsin\left(\frac{m\lambda}{2d}\right) \tag{2.5}$$

As an example, the corresponding ray angle θ of a waveguide height d of 5 μm, at a wavelength λ of 1.55 μm is 81.08° from normal.

For solid-core waveguides, a typical lateral guiding design employed is the effective index method [17], that uses different k_z values in the core and cladding region. Here, we also propose the same -- obtaining lateral confinement by using different HCG designs for the core and cladding region so that the effective refractive index of the core is higher than that of the cladding[9]. This can be achieved by fine-tuning the HCG reflection phase, φ_r, which determines the effective index n_{eff} of the 1D-slab waveguide in Eqquation (2.2)-(2.4). The 2D waveguide is a piece-wise composition of 1D HCG slab waveguides (forming an HCG double heterostructure, i.e. cladding/core/cladding), with the condition that both HCGs designs have high reflectivity. To maintain a flat structure, we consider only a single HCG thickness t_g, for both core and cladding designs. Even with this limitation, HCG designs with different periods Λ and grating widths s can provide remarkably large differences in φ_r while maintaining a high reflectivity; this results in a *variation in effective refractive index between HCG designs on a flat surface*.

2.2.1 Simulations

Rigorous coupled wave analysis (RCWA) [17] is used to calculate the complex reflection coefficient r of the HCG. r is calculated for different HCG periods Λ and silicon grating bar widths (or air gaps) for discrete HCG thicknesses. At a t_g of 340 nm, on a 2-μm-thick layer of buried oxide the incidence angle of the light on the HCG is 85.06°, corresponding to the angle between the light ray and the normal of the HCG reflector in a 9-μm waveguide, and an HCG reflection phase φ_r of π. The wavelength of the light is 1550 nm, and the light polarization is TE from the perspective of the waveguide. Based on the ray optics for an HCW, r is converted into the propagation loss, as well as the effective refractive index n_{eff} of the 1D slab waveguide's fundamental mode using Eq. (2.1)-(2.4). Equivalently, finite element method (FEM) can be used to simulate the propagation mode of the HCG hollow-core slab waveguide, and propagation loss and effective refractive index can be extracted. Figure 2.3 shows the contour plot of loss and effective refractive index calculated by FEM. This provides the design template for glancing angle HCG.

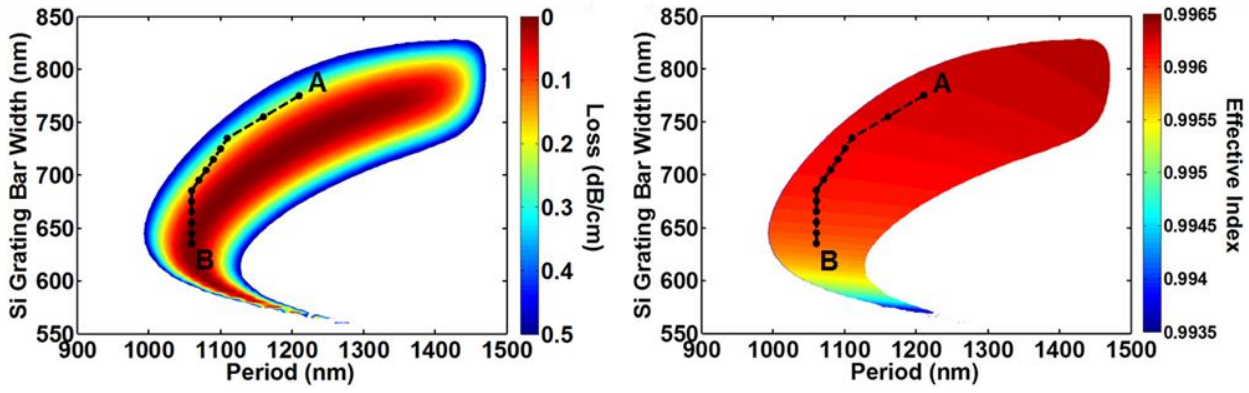


Figure 2.3. Loss and effective index contour plots of HCG hollow-core slab waveguides at d of 9-μm. The contour plots provide the design template for the waveguide. Different HCG periods Λ and silicon grating bar widths s are chosen for the core (point A) and cladding (point B), as well as the transition region (dots linked with dashed lines). The HCG thickness t_g is fixed at 340 nm, and the buried oxide thickness is set to 2 μm. The wavelength of the light is 1550 nm.

We design the HCG period and silicon bar width to be 1210 nm and 775 nm for the core region, and 1060 nm and 635 nm for the cladding region. Also known for solid core waveguides, graded-index waveguides typically exhibit lower loss than step-index waveguides[16]. A graded effective-index profile is introduced by chirping HCG dimensions on the order of tens nanometers (gradually changing parameters from A to B, in Fig.2). The core width W_c and the transition region width W_t are 10.9 μm and 11.9 μm respectively. The cladding width of the waveguide is 42.7 μm on each side. The relative effective refractive index difference between the core and cladding is 0.04%.

Figure 2.4 (a) shows the simulated mode profile of the fundamental mode of a 2D HCG HCW, simulated by FEM. The mode effective refractive index is simulated to be 0.9961 and propagation loss 0.35 dB/cm at 1550 nm. The minimum loss is 0.31 dB/cm at 1535 nm. It is truly remarkable to note that, although the guided mode has very little energy in the HCGs, the effective index model can be used and obtained with simple and small parameter changes of the HCG.

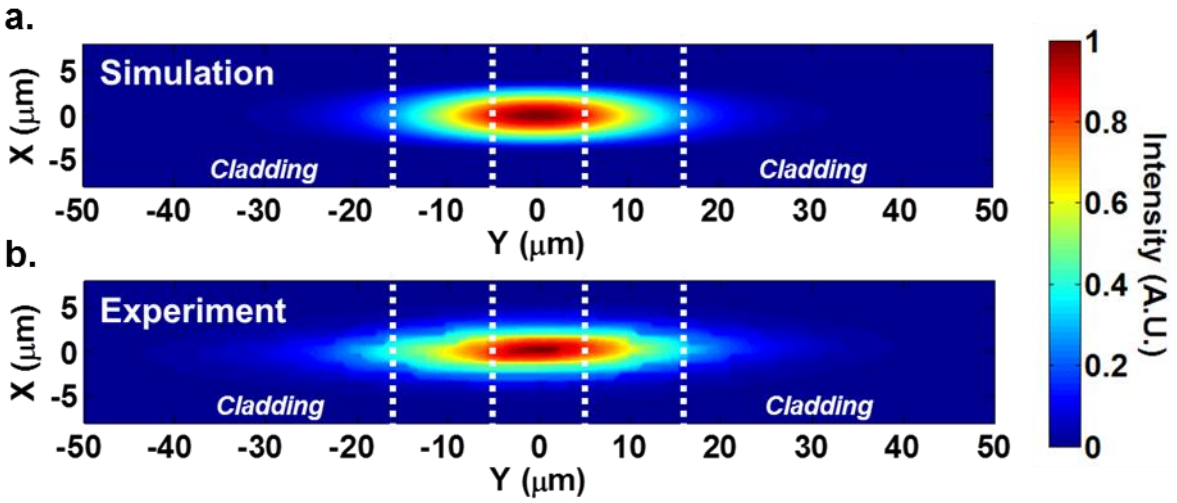


Figure 2.4 Optical mode of an HCG HCW. (a) Propagation mode profile simulated by FEM. The core width is 10.9 μm, the transition region is 11.9 μm, and the cladding width is 42.7 μm. (b) Experimentally measured optical mode profile.

2.2.2 HCG HCW fabrication

The HCG HCW was fabricated using deep ultra-violet lithography on 6-inch SOI wafers, followed by a standard silicon inductively coupled plasma reactive-ion etching (ICP-RIE) process. The great advantage of this lateral confinement scheme is that only a single etching step is required. Figure 2.5 shows the top-view optical microscope image of the fabricated chips (a) as well as the scanning electron microscope image of the HCG in the core (b) and cladding (c) region. The core, transition, and cladding regions of the waveguide can be clearly distinguished under the optical microscope. The HCG grating bars have a smooth surface and a sidewall roughness of about 10 nm. The period and silicon grating bar width of the HCG are in agreement

with the design values, and the silicon grating bar width varies by <±1.5% across the 6-inch wafer. For loss measurements, the waveguides are cut into different lengths and two pieces of patterned HCG chips are then mounted onto two translation stages. The stages are aligned and brought close together to form the HCG HCW.

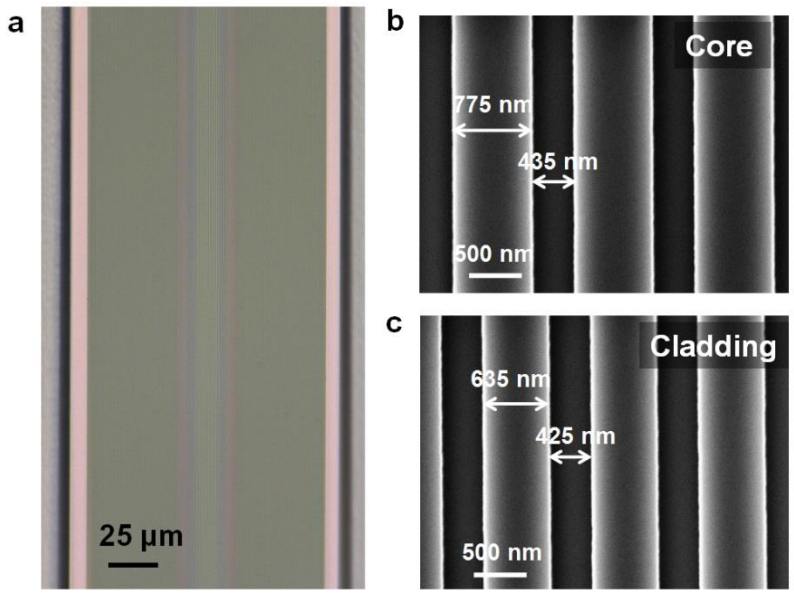


Figure 2.5. Fabricated HCG HCW chips. (a) Optical microscope image of the HCG chip. The core, transition and cladding regions are clearly distinguished by their diffracted colors. (b) and (c) The SEM image of the HCG grating bars in the core region and cladding regions.

2.3 Experimental Results

2.3.1 Optical mode imaging and loss measurement

To characterize the light guiding in the HCG HCW, a laser beam from a tunable laser source is first polarization adjusted and then collimated by a fiber collimator, and launched into the HCG HCW sample by a series of objectives. A 50X objective is used to collect the light for output facet imaging. Figure 2.6 shows the schematic for the characterization system. With precise alignment of the two chips, an optical mode can be seen at the output facet. Figure 2.7 (b) shows the output image with the waveguide height d set to 9 μm. The measured profiles in the transverse and lateral direction are shown in Figure 2.7 with 4 μm and 25 μm full width at half maximum (FWHM), respectively, at a wavelength of 1550 nm. Excellent agreement is obtained between simulation and experiment.

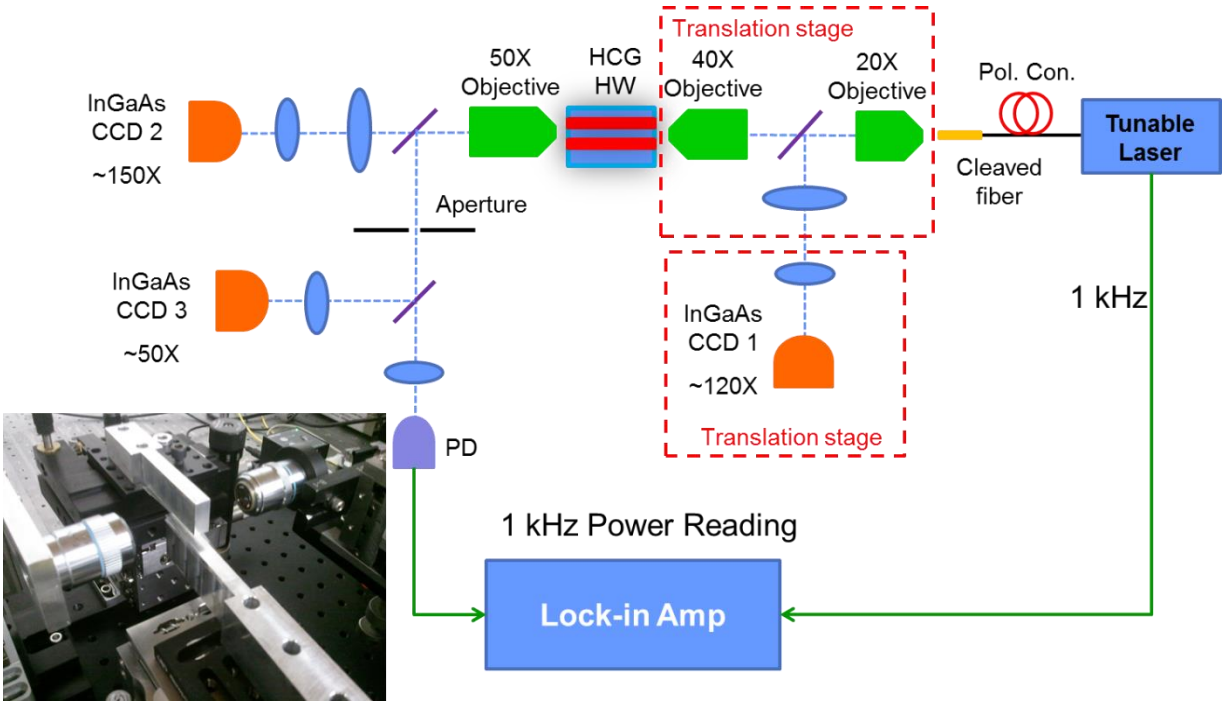


Figure 2.6 Optical characterization system for the hollow-core waveguide prototype.

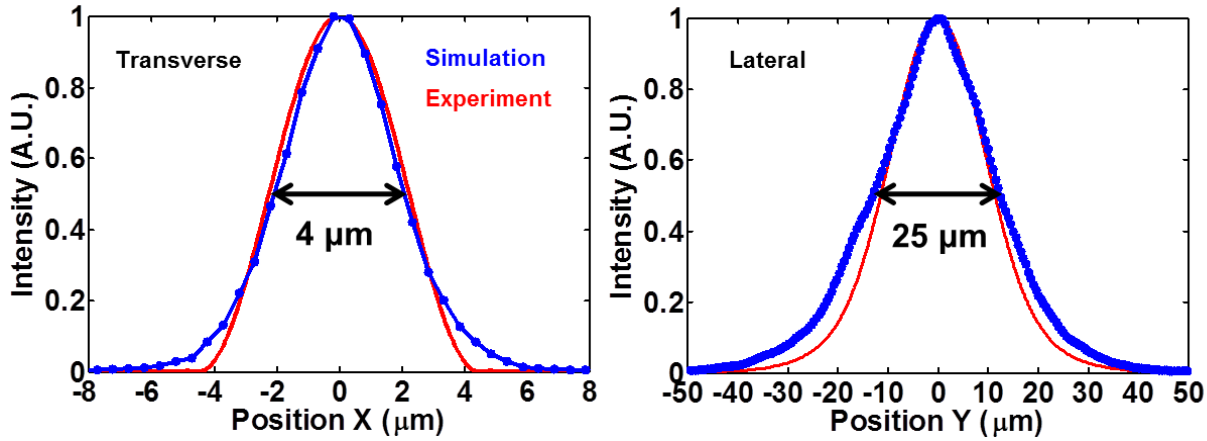


Figure 2.7 The measured mode profile from the fabricated device. The simulation (red curve) agrees well with experiment (blue line). The full width at half maximum (FWHM) is 4 μm in the transverse direction, and 25 μm in the lateral direction. The wavelength in both simulation and measurement is 1550 nm.

For loss measurement, the laser is internally modulated at 1 kHz. The 50X objective is replaced with a photodetector that butt-couples the light from the waveguide in order to allow the optical power to be measured with a lock-in amplifier.

2.3.2 Data processing for waveguide loss

A cut-back method is applied to extract the net propagation loss and the coupling loss of the HCG HCW, shown in Figure 2.8. The loss spectrum of the whole optical path is first measured without the HCG HCW. The total loss spectrum is then measured for different lengths of waveguides. As mentioned above, due to the fabrication variation across the 6-inch SOI wafer, the HCG dimensions are not identical on all different pieces of waveguides. The silicon grating bar width varies by <±1.5% across the 6-inch wafer. This leads to a shift of the loss spectra (<20 nm with respect to the wavelength) between different pieces of waveguides. To improve the accuracy of the cut-back method, the loss spectra for the four different waveguide lengths are aligned in a range according to their minimum loss values. The net propagation loss is extracted for each wavelength based on a linear fit for the total loss of the four different lengths, and the propagation loss spectrum is obtained.

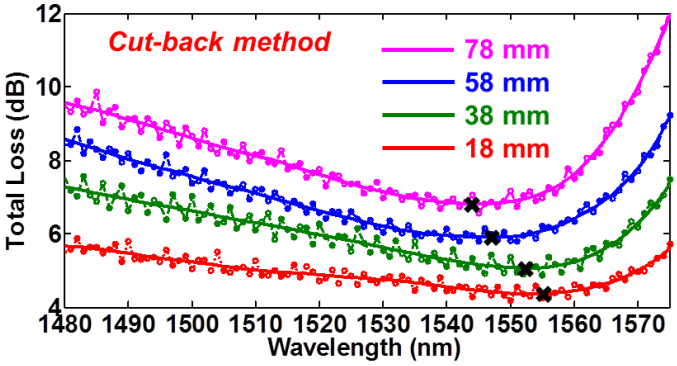


Figure 2.8 Loss spectrum of the HCG HCW for a 9-μm-high waveguide and lateral confinement. The total loss spectrum for an HCG HCW with four different lengths. The dashed dot line is the measured data. The oscillation is due to the laser and a residual Fabry-Pérot cavity in the optical path of the measurement system. To remove this noise, a smoothing spline method is applied and the solid curves show the clean spectra.

Figure 2.9 shows the measured total loss spectrum for straight waveguides with lengths of 18 mm, 38 mm, 58 mm and 78 mm. The extracted propagation loss spectrum agrees well with the results of the simulation. The minimum loss value from experiment is 0.37 dB/cm at 1535 nm, slightly higher than the simulated value, shown in Figure 2.9. This difference is attributed to a slight warping of the two HCG chips across their length, which leads to some variation of core height on the order of ±1 μm. In addition, the HCG surface scattering loss may contribute to additional loss. The coupling loss is estimated to be 4 dB, which can be further reduced by improving the coupling region. By optimizing the HCG dimensions and waveguide layout, an even lower loss can be expected.

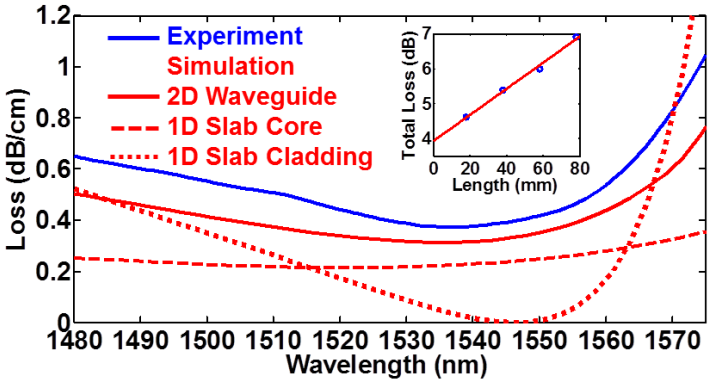


Figure 2.9 The experimental extracted propagation loss as a function of wavelength (blue) and the simulated loss spectrum obtained by FEM (red). Inset: the linear curve fitting used to extract the propagation loss and coupling loss at 1535 nm.

2.3.3 Dependence of lateral confinement on core height *d*

The effective index method is the main concept for the proposed lateral confinement scheme. It is further tested and illustrated by varying the waveguide height *d*. As seen in Figure 2.1 (b) and Equation (2.4), for a round trip in the transverse direction, the beam acquires phase through two components: interaction with the HCG (associated with a phase of $2\varphi_r$) and travel through the air trajectory (associated with a phase of $2k_x d$). Since the latter component is nearly constant for both the core and cladding regions, the HCG phase component creates the effective index difference ($\Delta n/n_{core}$). As *d* reduces, the contribution from the HCG increases relative to the air contribution, and thus $\Delta n/n_{core}$ becomes more pronounced. This results in a stronger lateral confinement and a narrowing of mode with reduced *d*, as illustrated in Figure 2.10 with experimental measured mode profiles versus *d*.

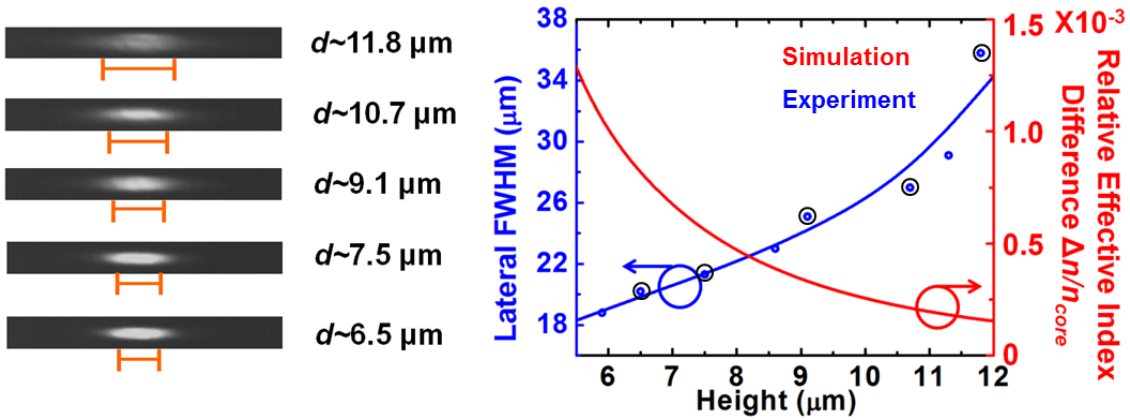


Figure 2.10 Mode profile at different waveguide heights d. As d decreases, $\Delta n/n_{core}$ increases, and the mode is more confined with reduced lateral leakage. The guidelines indicate the FWHM of the mode in the lateral direction. Experimental lateral FWHM of the fundamental mode versus different waveguide

height d (blue dots as experiment sampling points, curve-fitted with blue curve). The $\Delta n/n_{core}$ value of the fundamental mode as simulated by FEM is shown in red. The wavelength for the measurement is 1550 nm.

To further illustrate lateral index guiding, we fabricated various waveguides on the same chip with step-index guiding (uniform HCG design) and anti-guiding (with swapped core and cladding designs from the original). The output mode profiles are presented in Figure 2.11, and they show distinct differences with light dispersed in the waveguide without the appropriate HCG design. These lateral confinement measurements demonstrate the effectiveness of the effective index method for an HCW for the first time. It is truly remarkable that with little optical energy in the HCG, lateral guiding can be obtained with a planar structure. This enables light to be guided in an HCW without the aid of physical side reflectors, and opens up a new regime of optical waveguiding.

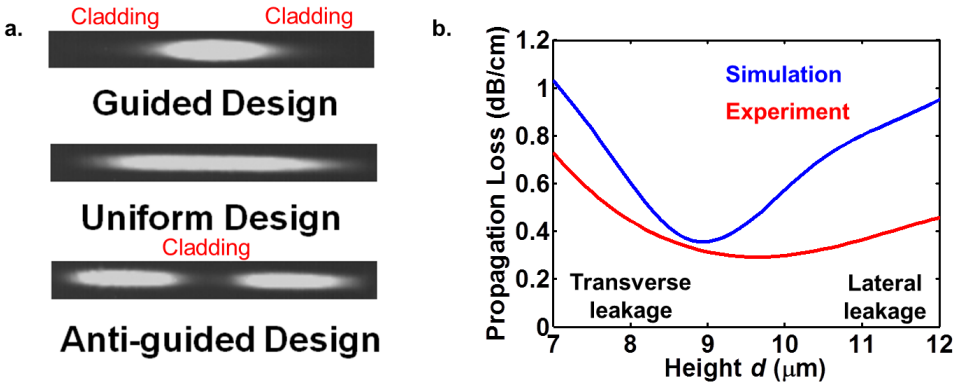


Figure 2.11 (a) Mode profiles for three side-by-side HCWs, with lateral guiding (top), step-index guiding (middle) and anti-guided design where the core and cladding designs are swapped (bottom). For the mode profiles, the output power of the mode is kept constant and d is constant ~9 μm. The image window is 140 μm by 16 μm. The wavelength is set to 1550 nm. (b) Propagation loss versus waveguide height d at a wavelength of 1535 nm. At the optimized waveguide height of 9 μm, an optimal tradeoff between lateral leakage and transverse leakage is achieved. The FEM simulated loss for the fundamental mode is also plotted, in reasonable agreement with experiment.

2.3.4 Light guiding in curved HCG HCWs

Light can also bend and stay guided by this sidewall-less waveguides. Figure 2.12 (a) shows a top view of the curved waveguide layout. For very large d, light launched into port A of the waveguide is observed at both A' and B' output ports, a result of weak lateral confinement. As d is decreased, the lateral confinement mechanism is strengthened, as described in 2.3.3, and light output at port B is quenched. The mode profile in Figure 2.12 (a) shows light output only observed at port A'. We fabricated and confirmed well-confined modes for curved waveguides with 80 mm, 50 mm, and 30 mm radii-of-curvature (ROC). The "double-S-shape" waveguide is used to extract the bending loss, with various waveguide length combinations. Figure 2.12 (b)

shows the loss spectra for various bending radii R extracted from 18 mm to 38 mm long waveguides, with a waveguide height d of 6 μm. It is seen that as the bending radius of curvature decreases, the loss spectrum slightly red-shifts. This is because lateral confinement tends to be stronger at longer wavelengths, as indicated by the FEM simulated spectrum of Δn/n core, shown in Figure 2.12 (c). This also explains why the loss difference between the straight and the curved waveguides becomes smaller as the wavelength increases. To quantify this, a linear fit is applied to the loss as a function of R^{-1} for each wavelength, and the slope α is extracted. The slope of this graph indicates how well the light is confined to the waveguide. The slope decreases with increasing wavelength, consistent with the simulated spectrum of $\Delta n/n_{core}$.

$$Loss\left[cm^{-1}\right] = A\exp\left(\alpha/R\right) \tag{2.6}$$

$$Loss\left[dB/cm\right] = 10\log_{10} A + \frac{10}{R}\alpha\log_{10} e \tag{2.7}$$

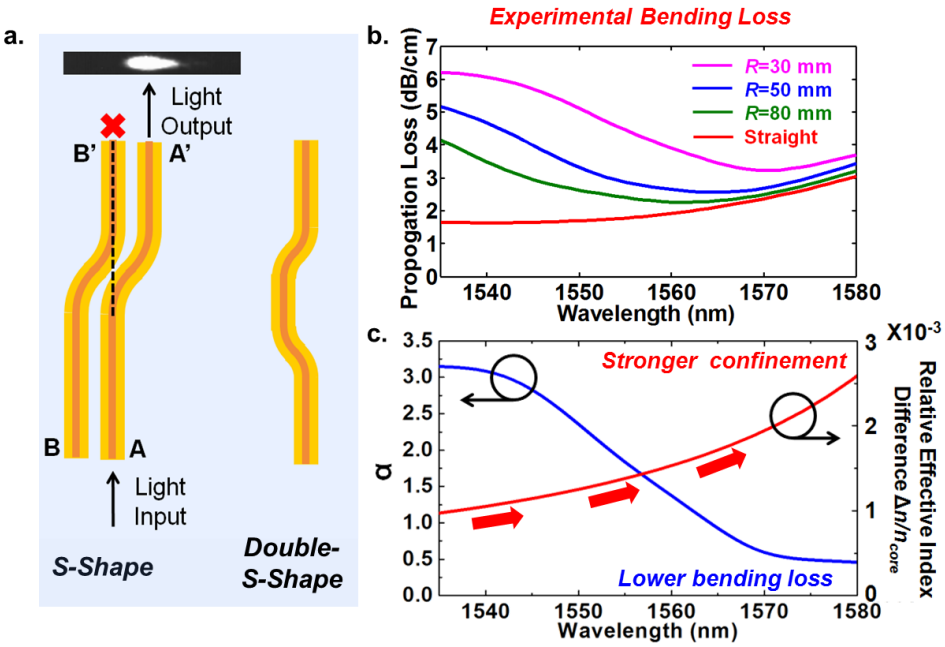


Figure 2.12 (a) Layout of the "S-shape" and "double-S-shape" curved waveguides. For the "S-shape" layout, curved waveguides A-A' and B-B' are parallel, and the input port of A-A' is aligned with the output port of B-B'. Light is launched into port A. Light guiding by the bend is demonstrated with the output observed in A' rather than B'. (b) Experimental loss spectrum for waveguides with different radii of curvature R, extracted from various waveguide length combinations of the "double-S-shape" curved waveguide layout. The loss includes both the propagation loss and the mode coupling loss at the four bending junctures for an 18-mm long waveguide. (c) The slope of the linear fit of loss versus R^{-1}, α, as a function of wavelength; this is consistent with the FEM simulated $\Delta n/n_{core}$ spectrum.

2.4 Summary

The ability to engineer the phase response of a planar HCG double heterostructure has led to the development of low-loss HCG HCWs on silicon. These waveguides feature a lateral confinement scheme that is unique to them in that they do not require sidewalls to maintain a well-defined lateral mode, a property that makes them particularly attractive for use in compact, low-power, fast on-chip gas/fluid sensing applications. Typical HCWs used in gas/fluid sensing experiments are limited by the long diffusion times of molecules into the waveguided region, where only the input and output ends serve as inlets. Other setups require separate bulky pumping devices that increase the complexity of the system. With no sidewalls, gaseous or fluidic molecules can penetrate into the HCG HCW nearly instantaneously when compared to conventional HCW counterparts. Other potential applications for waveguides that allow dispersion engineering include radio-frequency (RF) filters and low noise oscillators, optical routers and couplers based on multi-mode interference, among others.

In this chapter, we present the first experimental device showing lateral confinement in a low-loss planar HCW structure. The planar structure of the HCG makes fabrication simple, only a single etching step is required. Although the waveguides presented here offer a proof-of-concept, monolithic integration of the HCG double heterostructures is possible by flip-chip bonding, or by processing on a multi-stack SOI wafer. The HCG designs are chosen through straightforward slab waveguide numerical simulations in conjunction with the effective index method, both of which are experimentally confirmed in an HCW. The measured propagation loss is the lowest among all HCWs that are mode-matched to a single-mode optical fiber, and with further optimization of the HCG dimensions based on the loss contour and effective index contour map losses can be lower than 0.1 dB/cm in FEM simulations. In closing, this unique HCG HCW lateral confinement mechanism without sidewalls opens up a new scheme of waveguide engineering.

Chapter 3

Pairwise Integration of InP VCSEL to Silicon Photonics

"You have some peaches, eat them."

3.1 Introduction

Over the past few years, tremendous effort has gone into the development of various optical building blocks for the silicon photonics platform. Silicon photonics has the likely target of addressing the high-bandwidth needs of servers and data centers, where the high-volume processing of a silicon platform and the low cost of optical communications could redefine the constraints for high-performance computing interconnects. Demonstrations of an integrated photonic link consisting of lasers, modulators, multiplexers, demultiplexers, and photodetectors has been demonstrated on silicon with transmission rates greater than 50 Gbit/s [31].

Typically, hybrid laser integration schemes on silicon employ evanescent coupling from an active III-V gain medium onto passive silicon waveguides, which can have distributed feedback, distributed Bragg reflector (DBR), and sampled grating (SG DBR) structures built into them lithographically. Although these in-plane schemes can produce lasers with single wavelength operation and relatively high power delivery, they also suffer from high threshold currents, small free spectral range (FSR), longitudinal mode hopping, and high operating currents, typically greater than 50 mA [32].

A rather unexplored topic is the integration of VCSELs onto silicon photonics. VCSELs offer many advantages over their edge-emitting counterparts in that they have low power consumption, can be directly modulated at high speeds with low driving currents, can be tested in large-scale 2-D arrays, have single longitudinal mode operation, and can offer continuous wavelength tuning with electromechanical systems [33]. One challenging issue for VCSELs is coupling light from a surface normal direction into an in-plane nanophotonic waveguide. In this chapter, we describe an approach using flip-chip bonding to join III-V VCSELs onto a silicon photonics chip using grating couplers. Figure 3.1 is a schematic of the proposed approach of pairwise integration of an InP VCSEL to a silicon photonics chip.

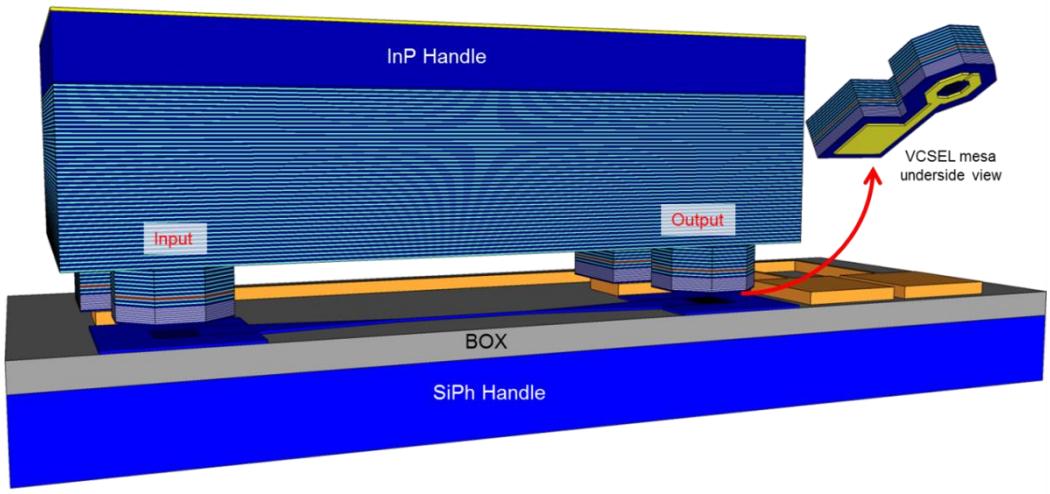


Figure 3.1 Schematic for pairwise integration of VCSEL onto a silicon photonics chip.

3.1.1 Bonding approach: the AuSn material system

The diagram in Figure 3.2 summarizes different kinds of bonding approaches used for the hybrid integration of silicon and III-V material systems [34].

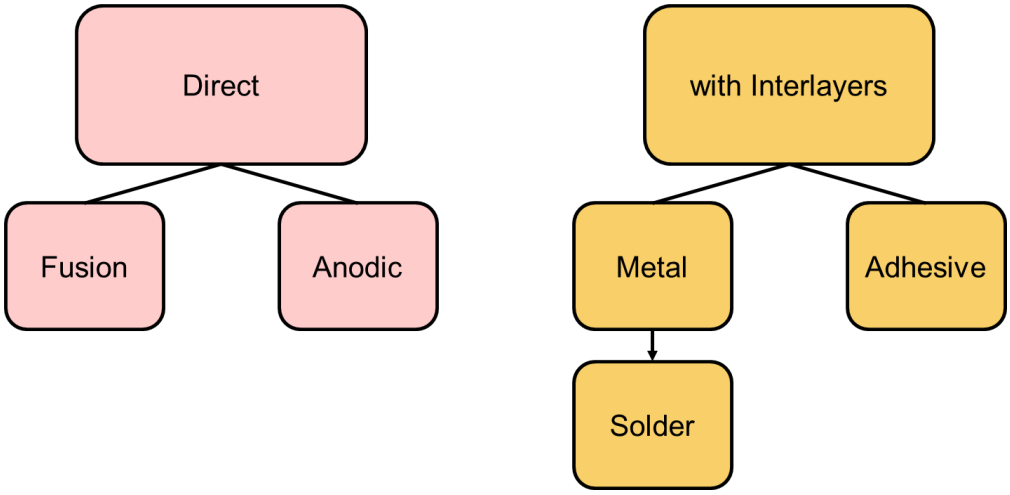


Figure 3.2 Bonding approaches for hybrid integration of silicon and III-V materials systems.

Two general categories can be considered: direct bonding, and bonding with interlayers. The first category involves the bonding of two surfaces under direct contact due to molecular bonds. Initially, bonds may be weakly formed by Van der Waals forces, but with surface treatment and annealing, very strong covalent bonds may be attained. This approach is also known as *fusion* or *molecular* bonding [35]. Anodic bonding is another type of direct bonding in which covalent bond formation is assisted by the presence of a strong electric field, which drives alkali ions from

one interface into another and form oxidation layers joining them [36]. Typically, direct bonding delivers very strong bonds, but requires very flat and clean surfaces for high yields.

Interlayer bonding, as the name suggests, involves the use of intermediate films between the material systems for the bonding process. Adhesive bonding is a technique that uses organic polymers, often benzocyclobutene (BCB), which can be cured at low temperatures [37], or with ultraviolet light.

Another interlayer bonding alternative is with the use of metal films using thermocompression under high temperatures and forces [38], or via eutectic bonding layers which work with much lower temperatures [39]. These latter approaches have the great benefit of providing electrical contacts. Table 3.1 summarizes the main properties of direct, adhesive, and metal bonding techniques.

Table 3.1 Summary of bonding approach properties

Properties	**Direct**	**Adhesive**	**Metal**
Particulate tolerance	Low	High	Good
Surface roughness	Low	High	Good
Mechanical strength	High	Low	High
Electrical contacts	No	No	Yes
Hermetic cavity	No	No	Yes

Due to its lower processing temperatures, the favorable bonding approach for these VCSELs is eutectic bonding. A eutectic is a specific alloy composition that changes directly from solid to liquid at a unique triple point in the phase diagram. The transition to a liquid phase provides a viscous interface that can planarize and overcome particles along a bonding surface. As mentioned above, metal bonds not only allow for physical, but also electrical and thermal contact. They can also provide hermetic sealing for MEMS cantilevers. There are many types of eutectic alloys that are compatible with standard silicon processing techniques; some are listed below.

Table 3.2 Eutectic alloys commonly used in wafer level packaging

Eutectic Alloy	**Composition**	**Temperature**
Au-In	0.6 wt.% Au	156 °C
Cu-Sn	5 wt.% Cu	231 °C
Au-Sn	80 wt.% Au	280 °C
Au-Ge	28 wt.% Au	361 °C
Au-Si	97.1 wt.% Au	363 °C
Al-Ge	49% wt.% Al	419 °C

Of the listed material systems, Au-Sn can be readily processed in the Marvell Nanofabrication Laboratory *and* has a eutectic transition temperature that is suitable for annealing proton

implanted VCSELs without damaging the aperture. If the transition temperature is too high, hydrogen implant species lose their isolation properties in InP [40]. Au-In and Cu-Sn are two other material systems that have transition temperatures compatible with implanted VCSELs, but there are oxidation concerns with indium-based alloys, and copper-tin is not commonly used in the Marvell physical deposition tools. The Au-Sn eutectic diagram is shown in Figure 3.3 below.

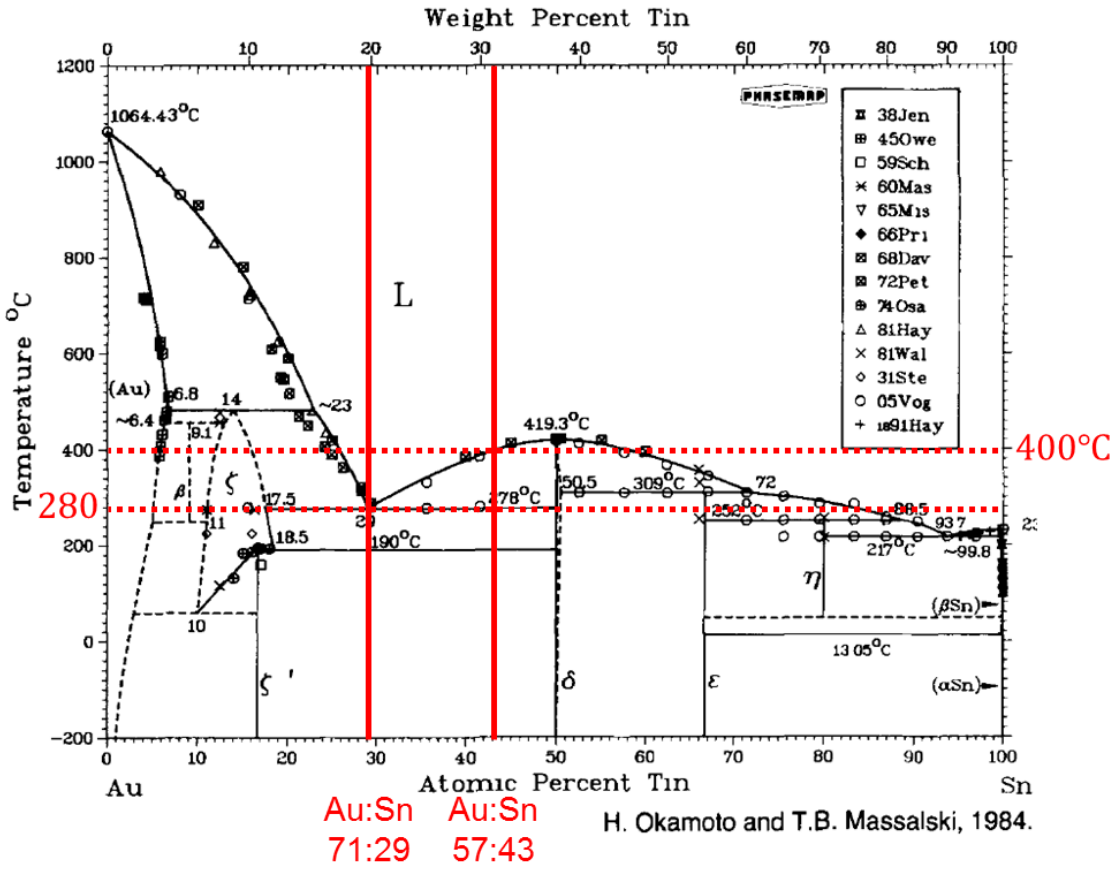


Figure 3.3 The Au-Sn material system phase diagram [41]. The 400 °C line corresponds to the maximum temperature of the Finetech Lambda flip-chip bonder.

The eutectic composition is 71 atomic percent (at. %) gold atoms, and 29 at. % tin atoms. One approach for bonding with eutectic alloys is to deposit the individual materials that constitute the alloy on separate substrates, and then use thermocompression below the eutectic temperature to allow for interface mixing via diffusion, and then increase the temperature above the eutectic to reflow the alloy [42]. Once the material is mixed and melted, the samples are cooled.

The composition of the alloys can be tailored via the thickness control of thin film evaporation. The thickness of films can be written in terms of their mass (m), density (ρ), and area (A):

$$m = \rho V \qquad m = \rho A t \qquad t = \frac{m}{\rho A} \tag{3.1}$$

By taking the ratio of the thicknesses of films in a stack, we can eliminate the area A of the films, since they are the same. Then we have:

$$\frac{t_{Sn}}{t_{Au}} = \frac{m_{Sn}/\rho_{Sn}}{m_{Au}/\rho_{Au}} = \frac{m_{Sn}}{m_{Au}} \times \frac{\rho_{Au}}{\rho_{Sn}} = \frac{at.\%_{Sn}}{at.\%_{Au}} \times \frac{AMU_{Sn}}{AMU_{Au}} \times \frac{\rho_{Au}}{\rho_{Sn}} \tag{3.2}$$

Where $AMU_{Sn,Au}$ are the atomic weights of tin and gold in atomic mass units, reproduced below in Table 3.3.

Table 3.3 Material properties of gold and tin.

Material	Density (R.T.)	Atomic Weight
Au	19.30 g/cm^3	196.97
Sn (white)	7.365 g/cm^3	118.71

Hence, the thickness ratio of the film stack is determined by the alloy composition. For example, to achieve a 71:29 Au:Sn alloy composition, we have:

$$\frac{t_{Sn}}{t_{Au}} = \frac{29}{71} \times \frac{118.71[AMU]}{196.97[AMU]} \times \frac{19.3[g/cm^3]}{7.365[g/cm^3]} = 0.645 \tag{3.3}$$

which means that for every 100 nm of gold, 64.5 nm of tin must be added to the stack to achieve the eutectic composition. One method is to prepare separate substrates by evaporating a thin adhesion layer (e.g. 25 nm titanium), followed by a diffusion blocking layer (e.g. 50 nm palladium or platinum) on both substrates. Then, a Au-Sn-Au film stack is evaporated on the SOI substrate, and a single Au layer is added to the III-V substrate. The total ratio of gold to tin on *both* substrates should adhere to the 0.645 ratio computed from Equation (2.6). For example, if the goal is to evaporate a total film stack of 1.3 μm, then by subtracting the adhesion and diffusion blocking layers from both substrates we have a remainder of 1.15 μm to be evaporated. Using the 0.645 ratio, 470.6 nm should be Sn, and 729.4 nm Au. If we cap both film stacks with 100 nm of Au for oxidation protection then the film stacks become

III-V:	Ti / Pt / Au	25 / 50 / 100 nm
SOI:	Ti / Pt / Au / Sn / Au	25 / 50 / 529.4 / 470.6 / 100 nm

This film stack is illustrated in Figure 3.4.

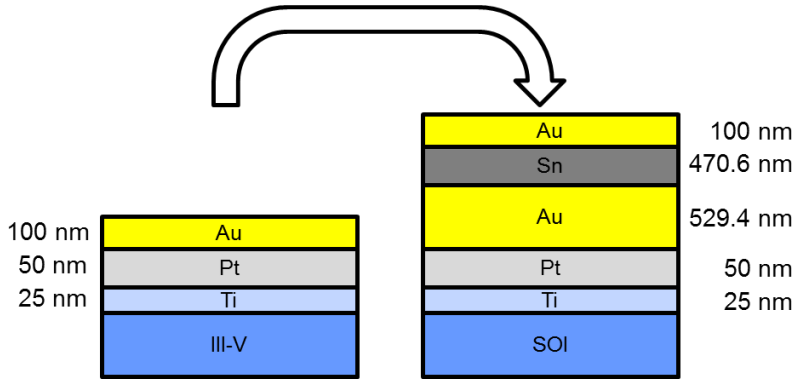


Figure 3.4 Cartoon illustration of eutectic film stack including adhesion and diffusion blocking layers.

Tin has a rather high vapor pressure [43]. As a result, evaporating Sn is not straightforward, as it tends to melt and desorb from surfaces. In practice, eutectic stacks must be tin "rich" to melt at lower temperatures. By over-compensating with the thickness of Sn films, the alloy may be in a hyper eutectic region of the phase diagram. For Au-Sn in particular, it is preferable to be at a Sn-rich composition than a Sn-poor, due to the stepper slope versus temperature at the liquidus line for Sn poor alloys. The formation of a hyper-eutectic microstructure is as follows (descending from the liquidus line): AuSn grains nucleate in an increasingly Au rich melt, where the volume ratio of the two is determined by the tie-line length rule. As the eutectic temperature is reached, eutectic solid forms out of the solutions, consisting of alternating grains of AuSn and Sn solid solution. Under the right conditions and as the temperature is reduced further, the solid solution holds less Sn, and the Au_5Sn phase is formed.

To verify the Au-Sn composition of the thin film stack two experiments were performed. First, a thin film stack with a 30.7 % Sn target is evaporated and analyzed with the Electron Probe Micro-Anaylzer (EPMA), a Cameca SX-51 electron microscope capable of wavelength dispersive spectroscopy (WDS). The measurements yielded a 26.7 % Sn composition. Then, four evaporation runs for 30.7%, 32.4%, 33.9%, and 35 % Sn were evaporated. The substrates were simultaneously heated to 400 °C with a ramp rate of 20 °C/s under a zoom lens camera system. The temperatures at which phase changes occurred are tabulated in Table 3.4.

Table 3.4 Observable phase transitions of AuSn alloy stacks.

Sn Composition	T_1	T_2	T_3
30.7		343	370
32.4	314	343	370
33.9	306	343	370
35	306	343	370

Empirically, the 33.9% and 35% Sn alloy compositions exhibited the lowest uniform phase transitions, and are used for the devices in this chapter and Chapter 4.

3.2 Silicon Photonics Chip Design

The silicon photonics chip was fabricated through the ePIXfab service on a multi-project wafer (MPW) shuttle run at IMEC, formerly known as the Interuniversity Microelectronics Centre, with headquarters in Leuven, Belgium. At the time, IMEC was providing a passives run consisting of crystalline silicon waveguides (strip and ridge) in a 220 nm SOI platform with 2 μm BOX. A cross section of the process is show in Figure 5.6, and a summary of the processing guidelines is in Table 5.1.

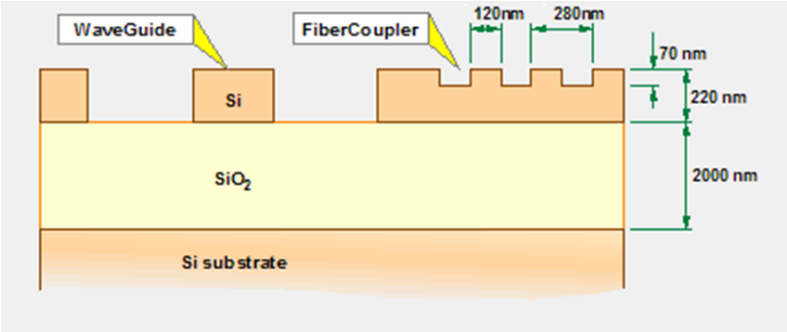


Figure 3.5 Schematic of IMEC passives.

Table 3.5 IMEC passives silicon photonics processing guidelines

Minimum linewidth	120 nm
Minimum spacing	280 nm
Waveguide loss (500 nm)	3 dB/cm
Fiber coupler efficiency	30 % 30 nm 1 dB

3.2.1 Input coupler simulation

The coupler efficiency quoted in Table 3.1 is for angled coupling similar to the one by Taillaert et al [44]. However, to couple a VCSEL, a surface-normal to in-plane coupler is necessary. Figure 3.6 (a) shows a schematic of a 2nd order grating coupler that channels light into bi-directional waveguides. Using FDTD, Li Zhu verified that a 2nd order grating coupler with a grating period of 575 nm, a duty cycle of 62% (corresponding to a 276 nm stripes of material removed from the waveguide) and a 70 nm shallow etch can have 46.2% total coupling efficiency, and a 3 dB bandwidth of 78 nm. In a similar fashion, the IMEC coupler design for angled incidence was also verified via FDTD, shown in Figure 3.7. In this case, light is incident at 10° from normal. The grating period elongates to 615 nm, the duty cycle shrinks to 53% (corresponding to 289 nm stripes) but maintaining the same shallow etch depth of 70 nm. Although the *total* coupling efficiency is lower, the light is collected at a single waveguide. Hence, a single channel may have more power. For this case, the 3 dB bandwidth is 65 nm.

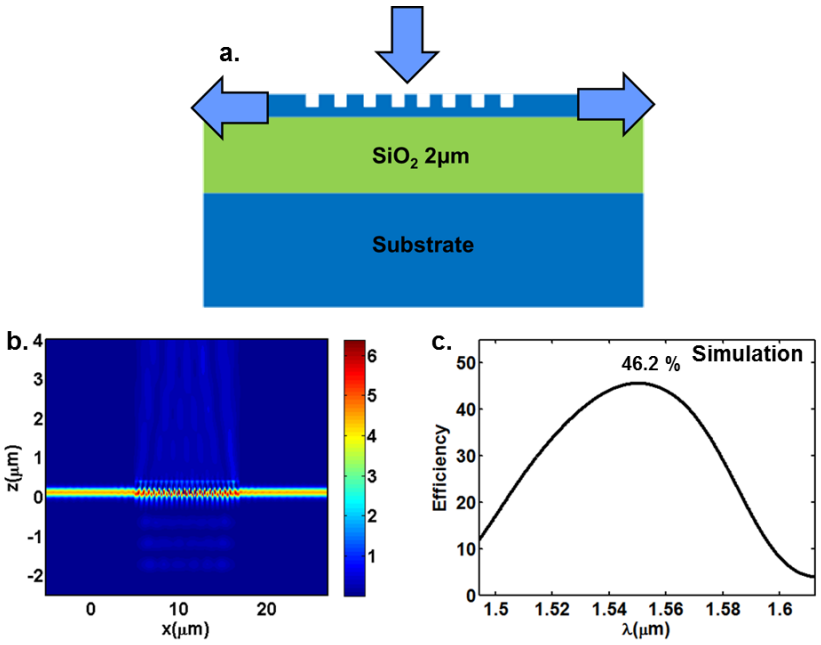


Figure 3.6 (a) Vertical coupler schematic. The silicon device layer is 220 nm thick and lies on a 2 µm BOX. (b) FDTD simulation for a plane wave incident on a 2nd order grating coupler. The grating period is 575 nm, duty cycle 62%, and has a shallow 70 nm etch. (c) The total coupling efficiency of double side output is 46.2%. The 3 dB bandwidth is 78 nm. Simulation performed by Li Zhu.

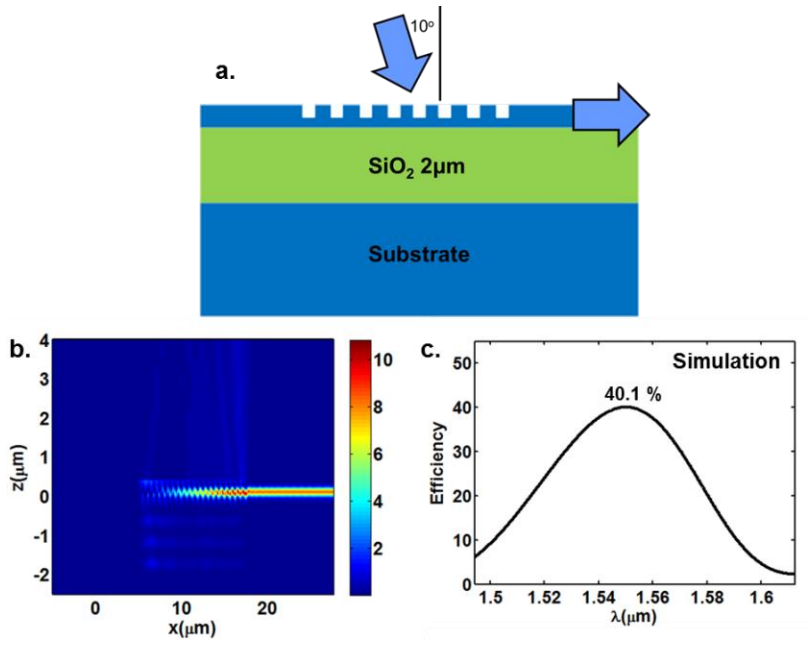


Figure 3.7 (a) Angled coupler schematic for coupling into single waveguide. (b) FDTD simulation. The grating period is 615 nm, duty cycle 53%, and has a shallow 70 nm etch. (c) The coupling efficiency is 40.1%. The 3 dB bandwidth is 65 nm. Simulation performed by Li Zhu.

The design area of the chip is 6.3 mm x 6.1 mm, where the actual die size is defined by a stepper window of 25.87 mm x 28.96 mm. Regions outside of the 6.3 mm x 6.1 mm design area are etched away, as they contain proprietary designs from other users on the MPW shuttle run. Figure 3.8 shows a photograph of the full 8" wafer.

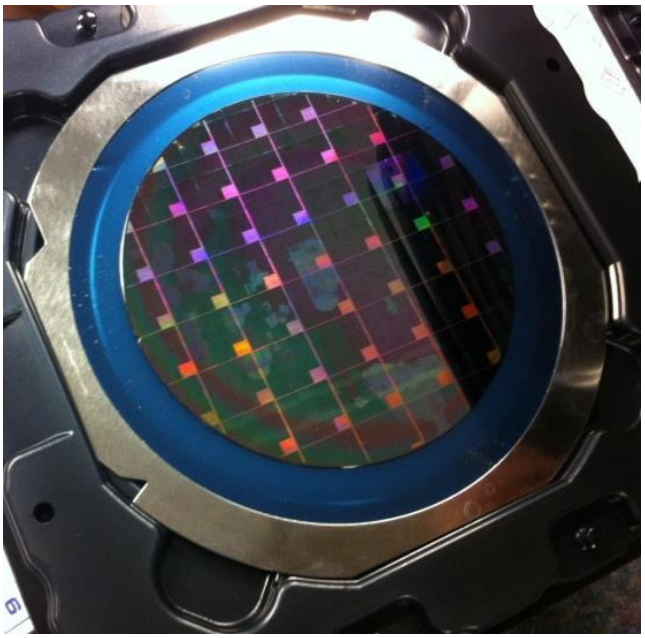


Figure 3.8 Photograph of 8" SOI wafer with 6.3 mm x 6.1 mm chip design within 25.87 mm x 28.96 mm stepper window.

The complete layout of the chip is shown in Figure 3.9. The chip is grouped into two regions: the top half features devices that employ an I/O strategy combining 90° couplers (surface normal to in-plane) and angled fiber output couplers connected by varying waveguide tapers and lengths; the bottom features I/O strictly from 90° couplers. The first 5 rows of each horizontal cell utilize couplers areas of 20 x 20 μm^2; the bottom 5 rows employ 30 x 30 μm^2 couplers. The chip can also be grouped into 3 columns, each about a 1/3 of the chip width. The 1st column uses 100 μm taper lengths to adiabatically shrink the multi-mode waveguide connected to the coupler from 20, or 30 μm (depending on the row), down to a single mode TE waveguide measuring 500 nm in width. Thus, the interconnect distance between I/O ports consists of two tapers and a short stretch of single mode waveguide that is 100 μm long. The 2nd and 3rd columns use longer tapers of 200 μm and 300 μm, respectively. The resulting pitch between I/O couplers increases from 300 μm for the 1st column, to 500 μm for the 2nd column, and 700 μm for the 3rd column.

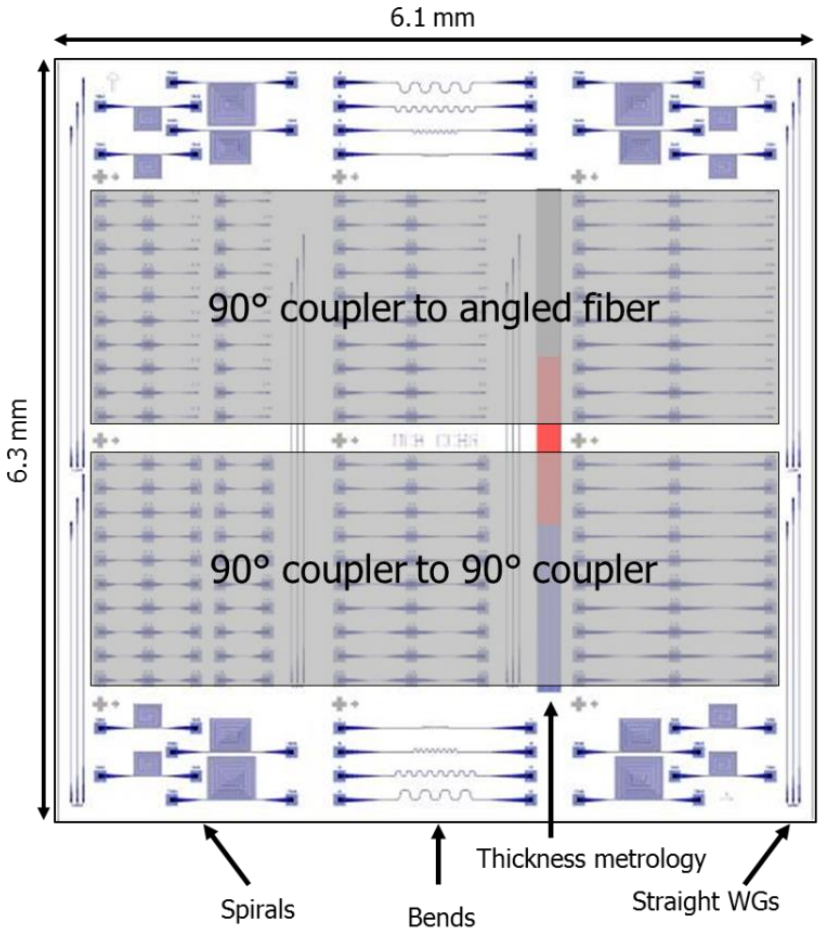


Figure 3.9 Silicon photonics chip layout for MPW shuttle run with IMEC-ePIXfab 3394 (‘imec 11’).

In addition, test structures were deployed to characterize the silicon waveguide propagation. Straight waveguides with 2, 2.5, and 3 mm lengths employing 100, 200, and 300 μm taper lengths are on the left and right edges of the chip. Waveguides with bends with 5, 10, 20, and 40 μm radii are at the bottom and top center regions of the chip. Regions to qualify the thickness of the different silicon heights (silicon strip 220 nm, silicon ridge 150 nm, and full etch) are included for metrology purposes. Finally, spirals with 5 mm, 10 mm, and 15 mm lengths, 200 μm tapers, and 5 μm bends are on the 4 corners of the chip. The latter are designed to mimic the long arms of a Mach–Zehnder interferometer (MZI) for use on future silicon photonics chips.

3.2.2 Electrical contacts to VCSEL

The fixed wavelength VCSEL used for the experiment has a single contact on the front side (emission through HCG mirror), and a single contact on the backside (emission through DBR mirror). To flip-chip bond the VCSEL die, thin AuSn eutectic solder bonding pads on each corner of the die are required. The “landing” pads are shown in Figure 3.10, as well as the electric interconnect that allows biasing, crossing the image horizontally.

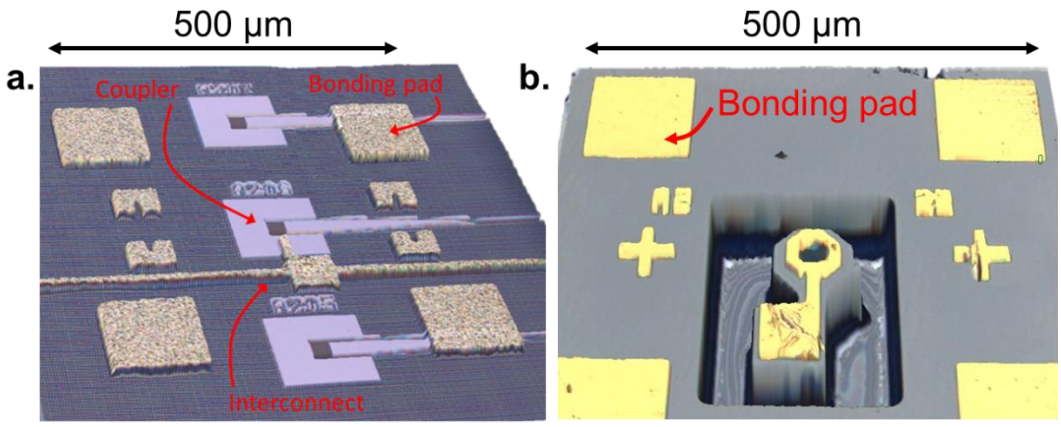


Figure 3.10 (a) Confocal image of AuSn bonding pads and electrical interconnects deposited by e-beam evaporation on the silicon photonics chip. The thickness of the AuSn metallic stack is 1.2 µm, the wire interconnects are 10 µm wide. (b) Confocal image of VCSEL contact and landing pads for bonding.

A top view SEM of the input grating coupler is shown in Figure 3.11. The grating coupler is 20 µm x 20 µm, much larger than the optical mode exiting the VCSEL. The discrepancy in size is to account for any flip-chip bonding misalignment, and leads to very conservative alignment constraints. The thin film used for bonding 1.2 µm thick to overcome particles that may inhibit bonding. The aspect ratio for flatness considerations is 500 µm by 1.2 µm, or 1 part in 416. In Chapter 4, an aspect ratio of 8000 µm by 0.650 µm is achieved, or 1 part in 12308, which makes this bonding effort rather trivial.

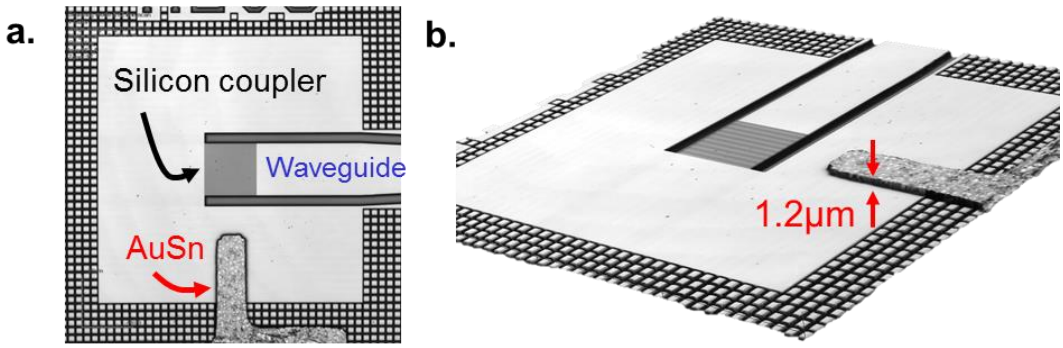


Figure 3.11 (a) Top view SEM image of the input grating coupler. (b) Tilted view SEM of same device. The 1.2 µm thickness of the AuSn bonding and contact layer can be appreciated.

3.3 Experimental Results

3.3.1 Flip chip bonding

In Figure 3.12, a sequence of photographs illustrates the pick-and-place capabilities of the Finetech Lambda Bonder. The bonding arm picks up the VCSEL chip and places it with micron-accuracy on the target substrate, in this case, the silicon photonic chip. Once the samples are aligned at a temperature of 150 ºC, the flip-chip thermo-compression bonding process is performed in inert nitrogen ambient at 340 ºC with 10 N of force.

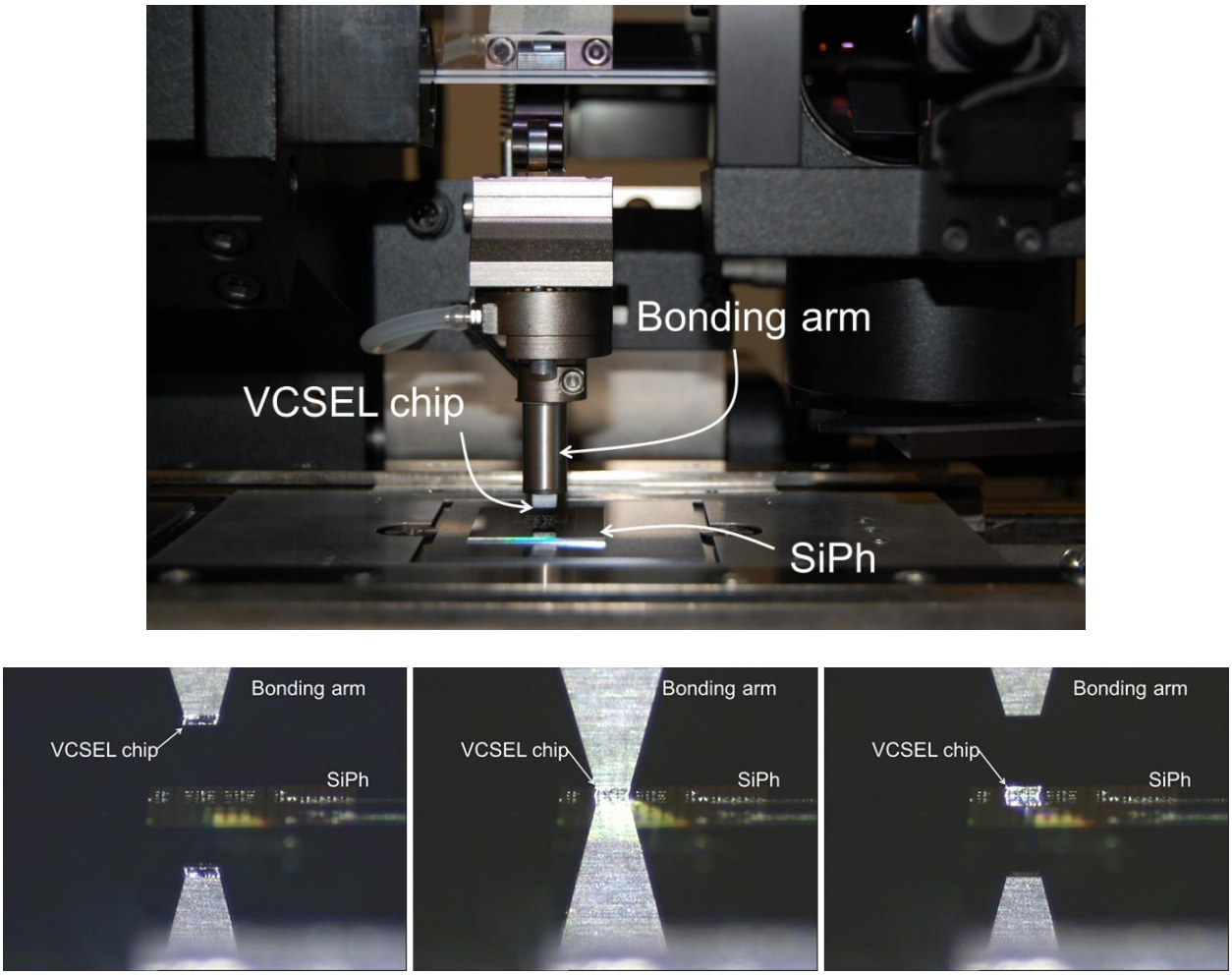


Figure 3.12 Sequence of photographs showing VCSEL die being placed and bonded to the silicon photonics chip.

Figure 3.13 shows a confocal image of the 500 x 500 μm^2 HCG VCSEL die on the silicon photonics passives chip. The n-contact of the VCSEL is probed on the backside of the device, whereas the p-contact is biased via the AuSn interconnect illustrated in Figure 3.11 (b).

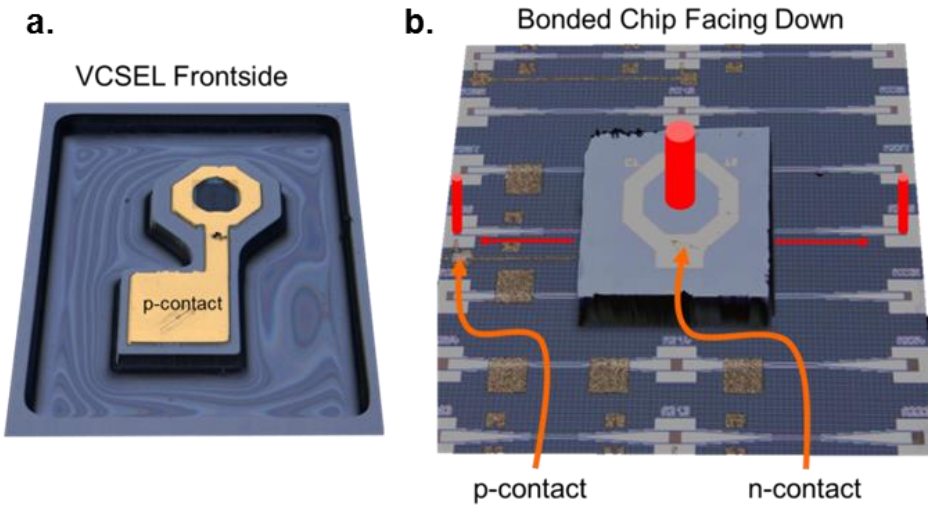


Figure 3.13 (a) Confocal microscope image of HCG VCSEL die from HCG-side of device. (b) VCSEL flip-chip bonded to silicon photonics chip. The VCSEL frontside is now facing down towards the silicon photonics chip. Output couplers are on the left- and right-most sections of image, as indicated by red beams.

3.3.2 VCSEL Performance before and after bonding

Figure 3.14 shows the room-temperature LIV of the device before and after bonding. The integrated VCSEL current threshold is measured to be as small as 1.8 mA, with a CW-operation output power of 330 μW. The change in threshold before and after bonding is negligible. The difference in collected powers is attributed to a mismatch in mirror reflectivities between the HCG and DBR mirrors. The trace in blue is for the stand-alone VCSEL, where light is collected via the HCG mirror of the device. The ripples on the LI curve are due to residue reflection from the metal plate on which the VCSEL die was mounted during probing. The trace in red is for the *bonded* VCSEL, where light is collected via the DBR mirror of the device. In this case, the ripples are not as pronounced, where the interference may come from the 2nd order grating reflection, or from the silicon substrate interface. Nonetheless, the IV characteristics before and after bonding agree well, with the bonded trace having slightly higher voltage due to the narrow AuSn electrical interconnects used to bias the laser.

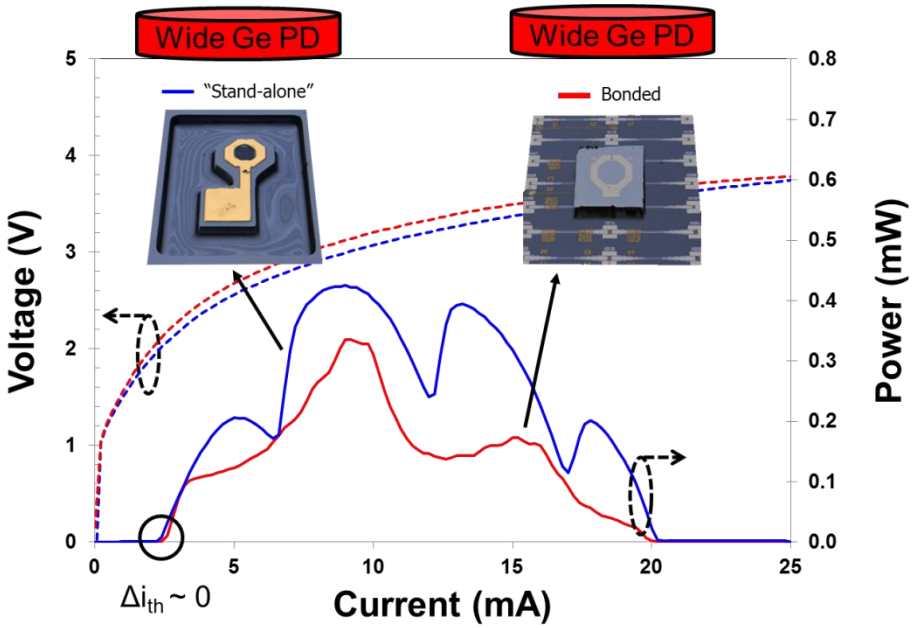


Figure 3.14 CW LIV of HCG VCSEL before and after bonding to SiPh chip. Top insets show confocal image of the device under test. (Blue trace) CW LIV of "stand-alone" VCSEL die. Light collection is done from the front side (HCG end) of the VCSEL chip using a wide area Ge photodetector. (Red trace) CW LIV of bonded VCSEL on SiPh. Light collection is done from the backside (DBR end) of the VCSEL.

3.3.3 Optical profile

Infrared imaging of the output ports of the integrated device confirms coupling between the VCSEL and silicon photonics chip (Figure 3.17). The integrated VCSEL maintains fundamental transverse-mode operation across a wide range of biasing currents with compact spots sizes ranging between 4.3 and 5.9 μm (Figure 3.16).

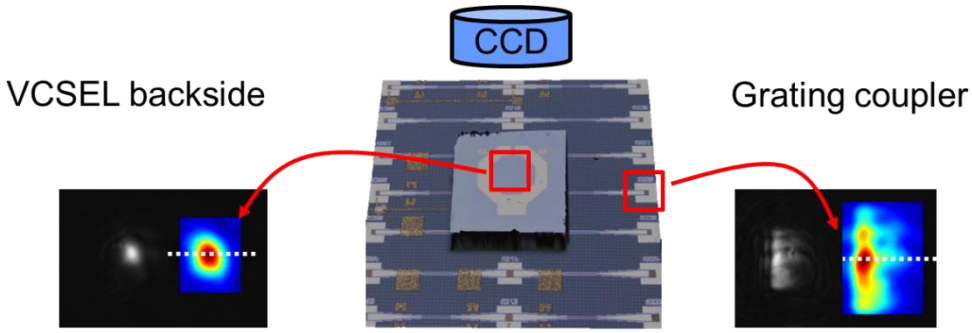


Figure 3.15 Near field optical imaging of the bonded VCSEL using a 100X objective and InGaAs CCD. (Left) Light is collected from backside of VCSEL (DBR end). (Right) light is collected from 2nd order grating coupler. Using the normalized intensity of the IR CCD image, the ratio of power $I_{coupler}/I_{VCSEL}$ ~ 12%.

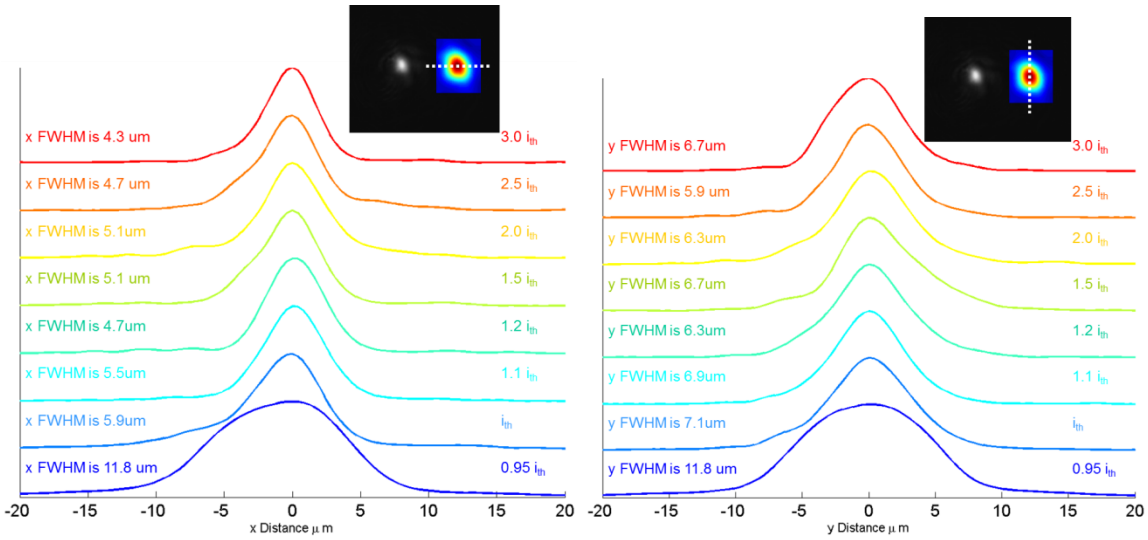


Figure 3.16: Infrared transverse mode profile measurements reveal fundamental-mode VCSEL operation.

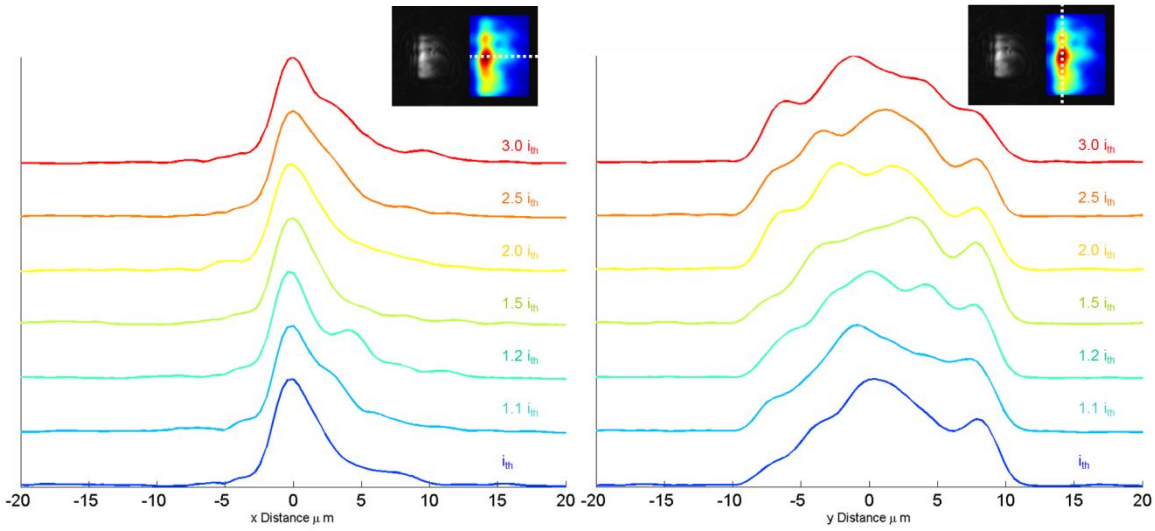


Figure 3.17 Profile of light collected at output couplers after traveling through 500 nm-wide single-mode TM Si waveguides.

By integrating the intensity of the images captured at the InGaAs CCD in Figure 3.16 and Figure 3.17, and normalizing with respect to the sensitivity of camera within a linear regime, we can convert the arbitrary intensity counts into power ratios. The computed intensity ratio between the backside of the VCSEL (output power through DBR) and the light collected from the grating coupler is $I_{coupler}/I_{VCSEL}$ ~ 12%. Thus, we can estimate the coupling loss of 2 couplers, 2 tapers to be roughly 10 dB.

3.4 Summary

In this chapter, we describe a set of experiments in which a long-wavelength InP-HCG VCSEL die is flip chip bonded to a silicon photonics chip using AuSn eutectic bonding pads. The silicon photonics chip has I/O ports made from grating couplers etched into the silicon device layer, which can couple light from a VCSEL into a bi-directional single mode waveguides in silicon. Capturing output light with an InGaAs CCD, the intensity at the output of the grating coupler is estimated to be ~ 40 μW using the backside of the VCSEL as a reference. The power ratios are calculated to be 12%, which leads to the I/O coupling efficiency to be estimated at ~ 10 dB.

In the next chapter, we aim to describe a VCSEL based on a silicon HCG which is part of a hybrid III-V and silicon optical cavity.

Chapter 4

Heterogeneously-integrated VCSEL using High-Contrast Grating on Silicon

"Having a resistor in a VCSEL is like sleeping with a bomb."

4.1 Introduction

A light source integrated with silicon will play a key role in applications such as optical interconnects for multi-core computing, lab-on-a-chip systems, and range detection [45]–[52]. Part of the allure is that photonics circuits on silicon can be very small and leverage over 50 years of existing microelectronics infrastructure. VCSELs have inherent advantages over their edge-emitting counterparts because they can be easily tested in vast 2D arrays and are energy efficient at high data rates [33], [53]–[60]. By employing MEMS actuators, they can also offer the flexibility necessary for circuit or network designers to reduce wavelength inventory and reduce integrated system costs [61]. Although several structures have been reported with vertical emission light sources on silicon-on-insulator (SOI) substrates [62], [63] electrically pumped, uncooled continuous-wave (CW) devices have not been achieved.

Our scalable approach targets the thermal resistance of VCSELs by: (i) employing a unique eutectic metal bonding process that acts as an efficient heat sink; and by (ii) substituting traditional III-V distributed Bragg reflector (DBR) mirrors used in VCSELs – which are thermally inefficient – with ultra-thin high contrast gratings (HCGs). We report an electrically pumped AlGaInAs-silicon VCSEL structure using an HCG mirror on silicon. The VCSEL operates in the L band with >1.5 mW CW output power, and single-mode operation up to 65 ºC. The thermal resistance of our device is measured to be 1.46 K/mW. We demonstrate >2.5 GHz 3-dB direct modulation bandwidth, and we show 5 Gb/s direct modulation through a fiber link of 2.5 km single mode fiber (SMF).

4.2 HCG Design and Fabrication

4.2.1 Modeling of HCG VCSEL cavity

Figure 4.1 (a) shows a schematic of a HCG VCSEL structure using an ultra-thin silicon HCG optimized as a reflector on a silicon-on-insulator (SOI) substrate. The active layer contains AlGaInAs compressively-strained quantum wells (QWs), and employs a proton implant-defined aperture for current confinement, as illustrated by Figure 4.1 (b). A tunnel junction close to the active region allows tunneling from the valence band to the conduction band, to limit the thickness of the p-type layer. The Fabry–Pérot cavity, indicated by circulating red arrows, is formed by a III-V DBR top mirror and the Si-HCG bottom mirror. The two material systems are

heterogeneously integrated via a AuSn eutectic thin film bonding process that provides electrical contact, as well as excellent thermal heat-sinking properties.

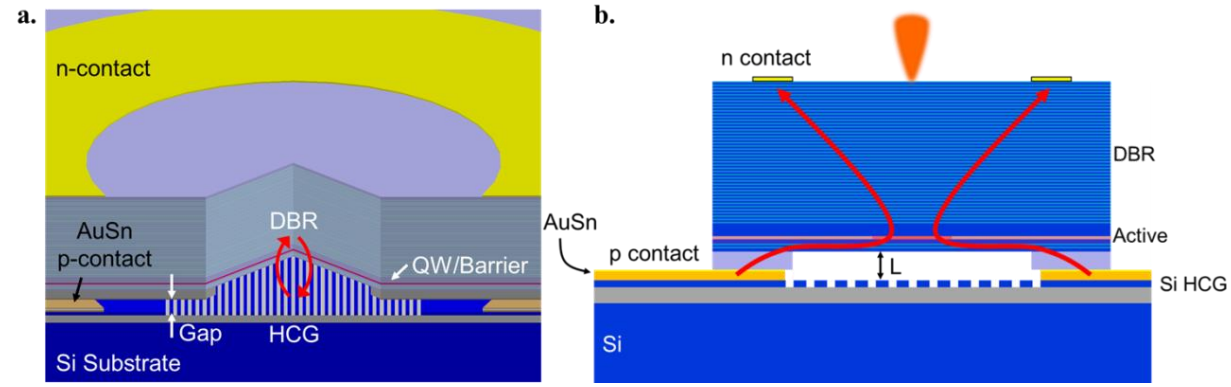


Figure 4.1 Schematic of VCSEL with silicon HCG as bottom mirror. (a) Tilted-view of VCSEL cross-section with circulating red arrows indicating optical cavity, drawn to scale. (b) The two material systems are heterogeneously integrated via AuSn thin film, with a hermetically sealed cavity gap of length L within the cavity. The VCSEL employs a proton implant-defined aperture for current confinement, indicated by red curved lines between contacts.

Using the analytical tool from [64], the HCG parameter space is scanned for a fixed silicon grating thickness t_g to generate a contour map of favorable designs, shown in Figure 4.2.

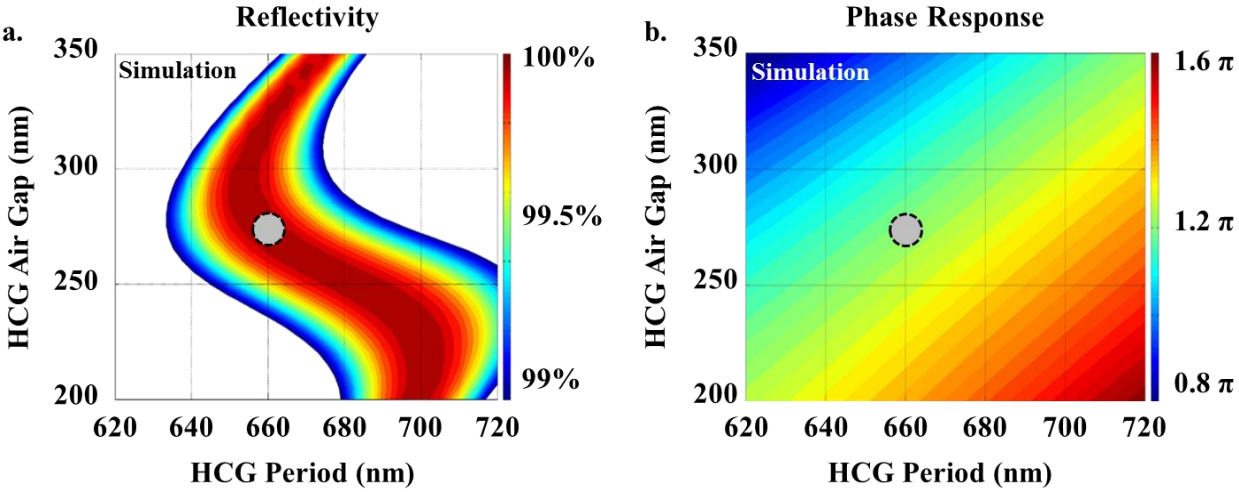


Figure 4.2 Parameter space of HCG designs using analytical method in [64]. (a) Contour map for reflectivity >99%, highest possible reflectivity is 100%. (b) Corresponding phase response of HCG for same dimensions. An HCG design with 660 nm period and 275 nm air gap has a reflectivity >99.5% and a phase response of ~1.2π.

The HCG design is chosen to have a reflectivity in excess of 99.5%. Since the VCSEL has a hermetically-sealed cavity gap of controllable length L within the cavity, the design must also have a phase response that maintains resonance. The round-trip phase condition is given by:

$$\frac{2\pi}{\lambda}2L+\varphi_{HCG}=2m\pi. \tag{4.1}$$

where φ_{HCG} is the phase response of the silicon HCG, and L is the cavity gap length. An HCG design with 660 nm period and 275 nm air gap has a phase response of 1.2π. At λ=1.55 μm, the cavity gap thickness must be set to L=1.8 μm to achieve resonance. The length L can be controlled during fabrication by tailoring the thickness of the eutectic metal thin film used for bonding, L_m, a segment of L. Figure 4.3 shows Lumerical FDTD simulations highlighting the resonant peaks of the "cold-cavity" for various L_m, ranging from 500 to 700 nm.

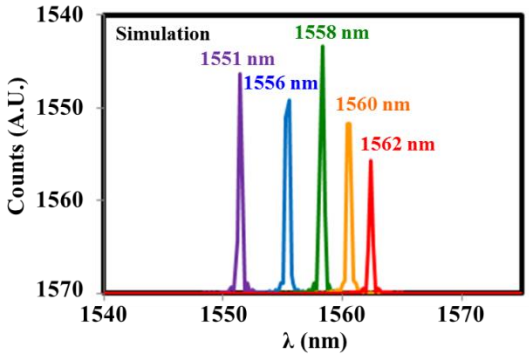


Figure 4.3 FDTD simulation of "cold-cavity" resonances for different metal thin films L_m. The length L_m is a segment of the total cavity gap L. Simulation was performed by varying the metal thin film thickness Lm from 500 nm (purple trace) to 700 nm (red trace) in 50 nm steps. Extending the length of the metal thin film makes the cavity length L longer and red-shifts the corresponding longitudinal mode of the cavity.

The Transfer Matrix Method (TMM) is used to verify the existence of an optical cavity within the VCSEL structure, as shown by the multi-color traces in Figure 4.4. Red indicates the refractive index of the epitaxial structure; green are energy bands; and blue is the optical field intensity within the cavity. Figure 4.4. (a) illustrates the numerous alternating pairs of DBR and the decaying optical field into the III-V mirror. The confinement factor between the cavity and the active region is 2.1%. In order to meet the round-trip phase requirements established by Eq. (4.1), the emerging wave A from the semiconductor must be in phase with the reflected wave B returning from the silicon HCG, as illustrated in Figure 4.4(b).

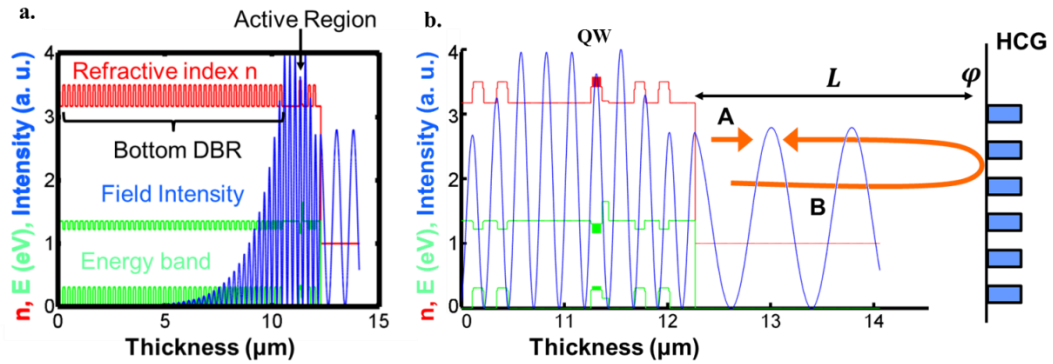


Figure 4.4 (a) TMM simulation of the VCSEL cavity. (b) Expanded view of region near semiconductor-air interface. The emerging wave A from the semiconductor must be in phase with the reflected wave B returning from silicon HCG to maintain resonance.

4.2.2 Thermal modeling of VCSEL structure

Using COMSOL, a Finite Element Method (FEM) simulation tool, the heat distribution of the HCG VCSEL structure was modeled by an 8-μm aperture with 25, 45, and 65 mW heat sources in the active region. The boundary conditions are set as thermal insulation at the semiconductor-air interface to provide a worse-case scenario for heat dissipation.

The heat transfer in the vertical and radial directions can be very different in a multilayer system such as a DBR [65], where the thermal resistance of each layer adds up in series and in parallel, respectively. Moreover, the heat flow is strongly affected by the alloy impurities and layer interfaces, due to the restriction of the phonon mean free path [66]. In conventional standalone VCSELs, the heat dissipation relies on the bottom DBR in between the heat source and heat sink. In flip-chip-bonded VCSELs, the heat can be carried away through the AuSn bonding layer.

In Figure 4.5, we show a comparison between a flip-chip bonded VCSEL on SOI using AuSn, and a standalone III-V VCSEL structure, with the DBR thermal conductivity modeled after the approach in [67]. For the case where the VCSEL is bonded on SOI, the maximum temperature generated is 125 ºC, shown in Figure 4.5(a). The active region is located at z=0 μm the DBR extends from 0.8<z<11.3 μm, the air interfaces from z>11.3 μm (since InP substrate is removed), thermal oxide -3>z>-4 μm, and silicon substrate extends from z<-4 μm for 350 μm in thickness. Using the same III-V epitaxial structure, boundary conditions, and temperature scale, the standalone III-V structure reached a maximum temperature of 183 ºC, as shown in Figure 4.5(b). For this latter case, the active region is also located at z=0 μm but the structure has the air interface above the active region from z>0.8 μm, the DBR extends from 0.8>z>-11.3 μm, and the InP substrate extends from z<1.3 μm for 350 μm in thickness.

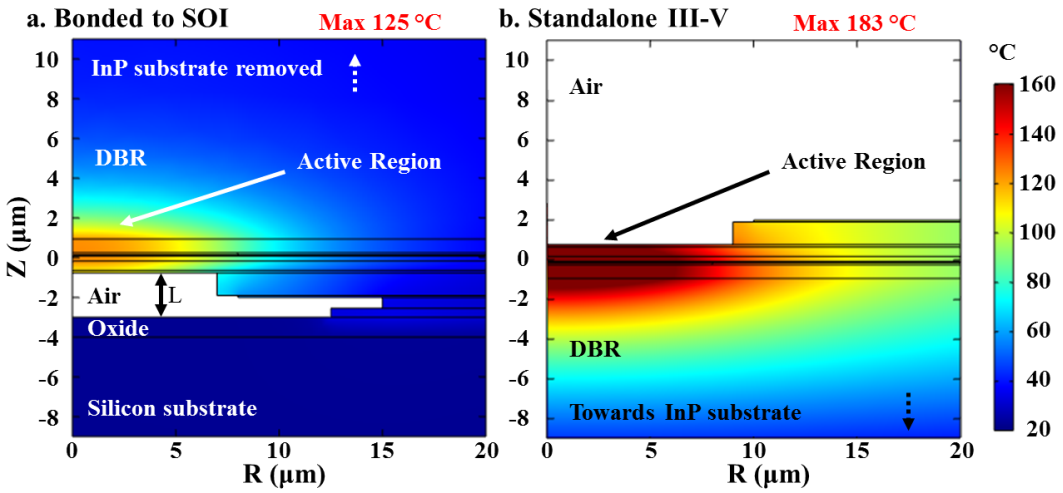


Figure 4.5 Radially-symmetric COMSOL FEM simulation modeling temperature distribution in VCSEL using 45 mW heat source in active region. (a) Bonded Si-HCG VCSEL on SOI substrate; active region z=0 μm, DBR extends from0.8<z<11.3 μm, air z>11.3 μm (since InP substrate is removed), thermal oxide -3>z>-4 μm, silicon substrate z<-4 μm, and 350 μm thick. (b) Standalone III-V VCSEL with InP substrate; structure has air above active region from z>0.8 μm, DBR extends from -0.8>z>-11.3 μm, InP substrate z<-11.3 μm, and 350 μm thick.

Although the flip-chip VCSEL is resting on insulator (SOI), the graph in Figure 4.6 shows that, at a given input thermal power, the average temperature in the active region has a stronger dependence on the vertical thermal conductivity of the DBR for standalone VCSELs (red) than flip-chip-bonded VCSELs (blue). This means the flip-chip-bonded VCSELs can overcome the restriction of heat flow caused by the DBR alloy impurities and interfaces. The thermal conductivity of AuSn is 57 W/Km, roughly an order of magnitude better than for a standard DBR quaternary alloy, i.e. 5 W/Km for AlGaInAs [68]. For alloy compositions with thermal conductivities below 7.2 W/mK, the bonded device exhibits superior thermal performance.

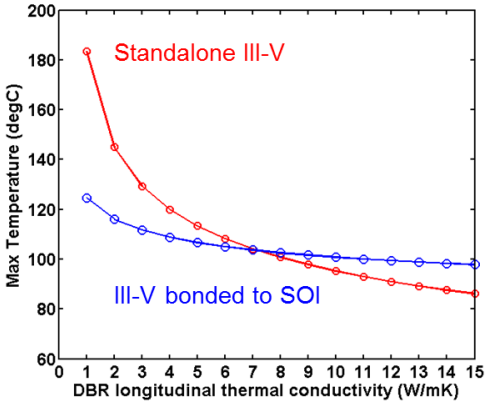


Figure 4.6 Maximum temperature vs DBR quaternary alloy thermal conductivity. The standalone III-V structure reaches higher temperature for DBR thermal conductivities below 7.2 W/mK.

4.2.3 Proton-implant current aperture

The design of the implant depth was done with a Monte Carlo software package TRIM (the Transport of Ions in Matter) [69]. The goal of the simulations is to find the energy at which the peak distribution of implanted ions is within 100-200 nm of the active region. Figure 4.7 shows the distribution versus depth of H^+ ions commonly used to achieve high resistivity layers in III-V semiconductors [70]. In InP, p-type layers are generally preferred for electrical isolation using proton implantation since they require a much lower threshold dosage than n-type layers.

For instance, a dose of 10^{13} ions/cm^2 can achieve a sheet resistance in excess of 10^7 Ω/sq in p-type InP, whereas a dose of 10^{14} ions/cm^2 can achieve a meager 10^5 Ω/sq in n-type material [40]. The epitaxial structure of this laser employs an n-n$^+$-p$^+$-p-i-n doping scheme where a tunnel junction (TJ) lies at the high doping boundaries. Electrons in the highly doped p$^+$ region tunnel out towards the n$^+$ cladding layers, thus injecting holes into the active region. This reduces the free carrier absorption and high resistivity associated with p-type InP structures. As a result, the thin p-type layers must be isolated. Damage incurred by the n-type layers can be repaired via rapid thermal annealing.

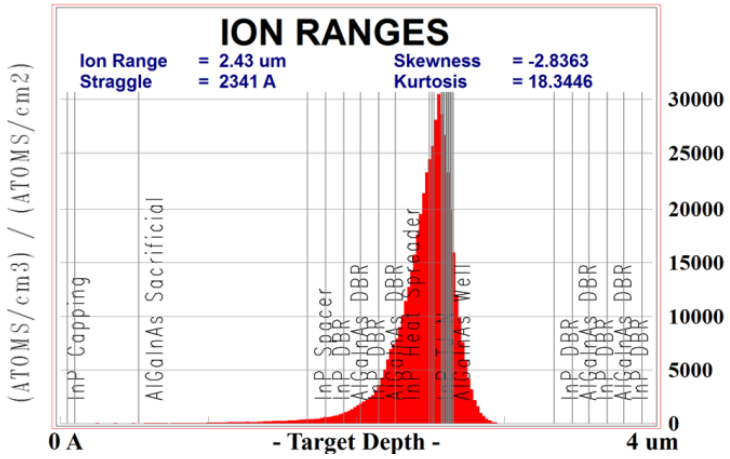


Figure 4.7 TRIM simulation of H^+ implanted at 310 KeV with a dose of 2e^{14} ions/cm^2.

4.2.4 HCG VCSEL fabrication

The step-by-step fabrication process is summarized in Figure 4.8, and involves 9 lithography steps.

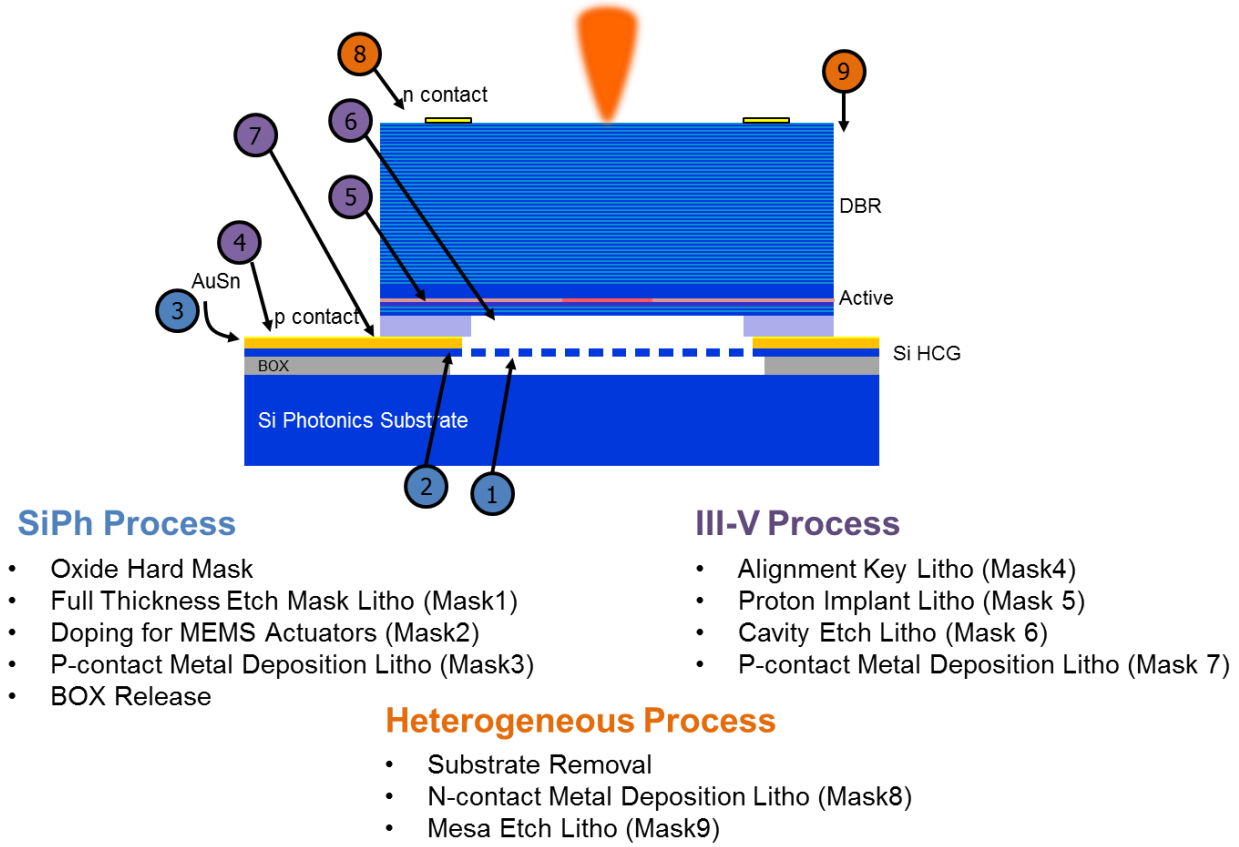


Figure 4.8 Silicon HCG VCSEL fabrication process flow. The heterogeneous process involves 9 lithography steps.

The silicon HCG is fabricated on a 6" SOI wafer using a 248nm DUV ASML lithography stepper and a Cl_2-HBr dry etching process. A 1.3 μm thin film metallic stack is deposited with electron-beam evaporation at a hyper-eutectic composition for the AuSn material system. In Figure 4.9 (a) we show a tilted-view colorized SEM of the Si-HCG reflector on an SOI substrate, surrounded by the AuSn thin film (yellow) ready for bonding. The flip-chip thermo-compression bonding process is performed in inert nitrogen ambient at 340 ºC with 10 N of force. InP substrate removal is done via wet chemical etching using an HCl:H_3PO_4 1:1 mixture. Figure 4.9(b) shows a colorized SEM of the fabricated Si-HCG VCSEL highlighting the active region in red, the III-V material in blue, and the corresponding p- and n-contacts in orange, and yellow, respectively.

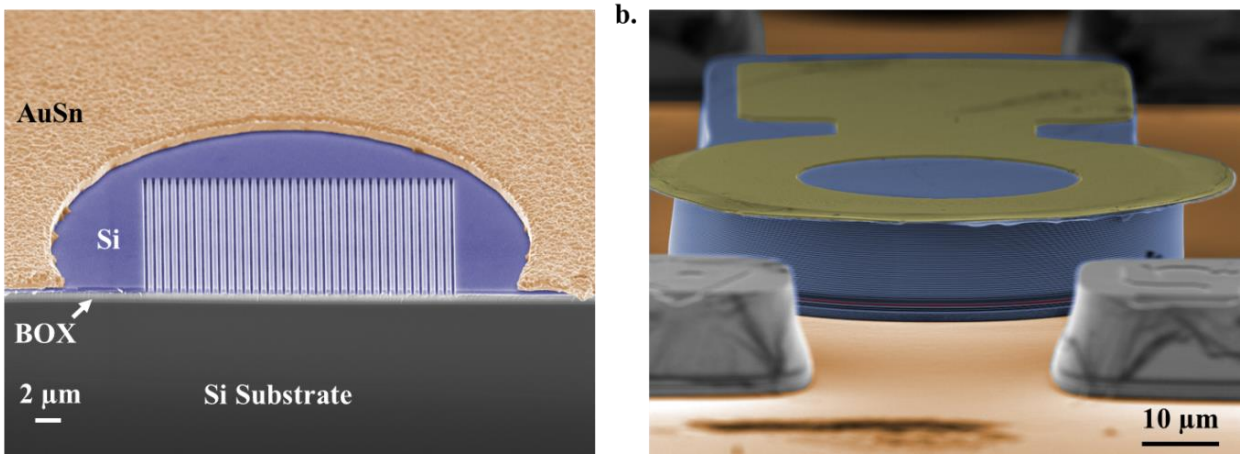


Figure 4.9. (a) Tilted-view colorized SEM of Si HCG reflector (blue hue) surrounded by AuSn film (orange hue). (b) SEM of fabricated Si-HCG VCSEL highlighting the active region in red, the III-V material in blue, and the corresponding p- and n-contacts in orange, and yellow, respectively.

After the dry etching process, the Si-HCG exhibits a shallow sidewall angle of roughly 9° (81° from oxide plane), as shown in Figure 4.10(a). Using FDTD, a variety of sidewall angles are modeled in Figure 4.10(b). The reflectivity remains above 99.5% for sidewalls steeper than 9° across a broadband region. The air gap dimensions outlined in Figure 4.10(a), a_{top} and a_{bottom} are used to model the actual structure, indicated by the dashed black line in Figure 4.10(b). The HCG design is robust and tolerant to standard fabrication methods.

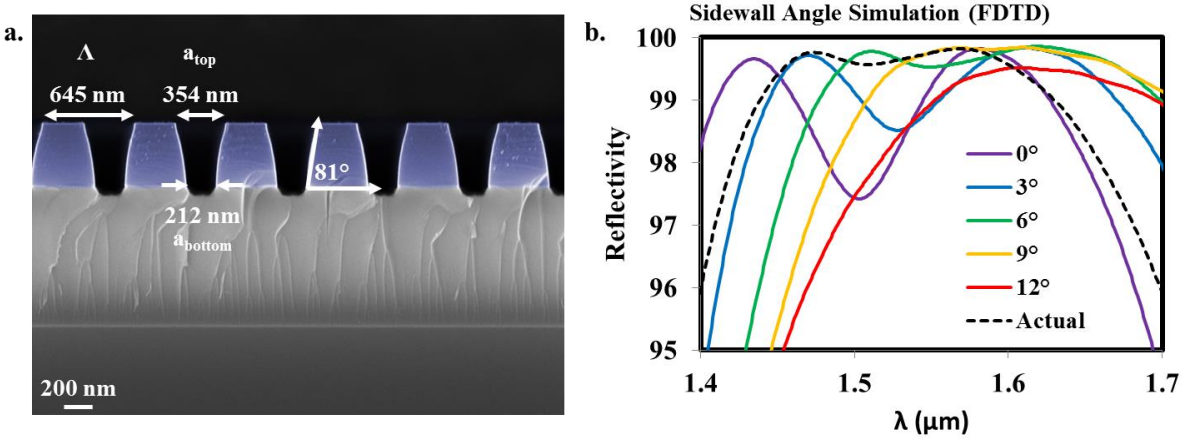


Figure 4.10 (a) SEM cross-section of Si-HCG reflector showing shallow sidewall sloping after dry etching process. (b) FDTD simulation of sidewall slopes from 0 to 12° indicating high reflectivities across the spectrum. The actual HCG parameters a_{top} and a_{bottom} are used to model the HCG structure indicated by the dashed black line.

4.3 Experimental Results

4.3.1 Light-Current-Voltage (LIV) characteristics

Figure 4.11 shows the temperature dependent light-current-voltage (LIV) characteristic of a VCSEL with CW operation achieved up to 60º C, and >1 mW CW power out-coupled from the semiconductor DBR at 15 ºC. Devices with CW output power > 1.5 mW at 15 ºC have also been achieved. The device temperature is controlled with a thermo-electric cooler on a copper chuck. A Keithley current source is used to bias the VCSEL via electrical probing. Light is collected by a large-area germanium photodetector placed above the VCSEL. The inset shows the near field intensity below and above threshold taken with a Xenics InGaAs CCD camera through a 100-X objective at high-gain sensitivity. The mode distortion is due to speckle interference visible at high-gain camera settings. Single transverse and longitudinal mode emission was observed over the entire current and temperature range. The VCSELs exhibit thermal rollover with increasing current bias due to gain spectrum red-shifting more rapidly than the resonant cavity spectrum, an effect typical in VCSELs [53]. The devices have slope efficiencies of ~0.3 mW/mA and threshold current i_{th} as low as of 7 mA. The ripples on the LI curve are due to residue reflection from the back of the silicon substrate/air interface, as verified by the output spectra measured at various currents corresponding to the peaks and valleys of the L-I curve and the substrate thickness. The L-I ripples can be eliminated with backside roughening of the substrate.

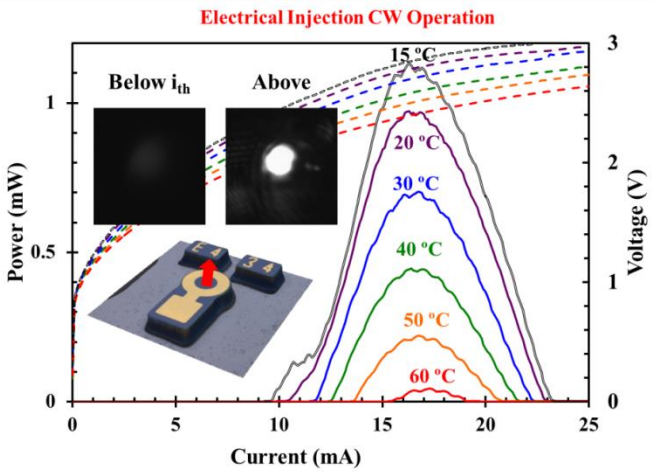


Figure 4.11 Temperature dependent CW LIV of Si HCG VCSEL from 15 to 60 °C. Top insets show near field intensity below and above threshold; bottom inset is confocal microscope image of fabricated VCSEL indicating emission direction. Light is collected with a large-area Ge photodiode for the LI measurement, and a 100X objective onto an InGaAs CCD for near field imaging.

4.3.2 Optical mode profile

Using the same method from Section 4.3.1, light is collected through a 100X objective and imaged onto an InGaAs CCD camera. To obtain an unsaturated image of the laser optical mode profile, the near field intensity measurement is taken at low-gain sensitivity (10 μS integration

time). Figure 4.12 shows the fundamental mode of the Si-HCG VCSEL biased at 11 mA. The measured FWHM collapses from 11.4 μm (biased below threshold) down to 4.7 μm at 11 mA bias (lasing). The proton implant aperture for the device is 7 μm in radius.

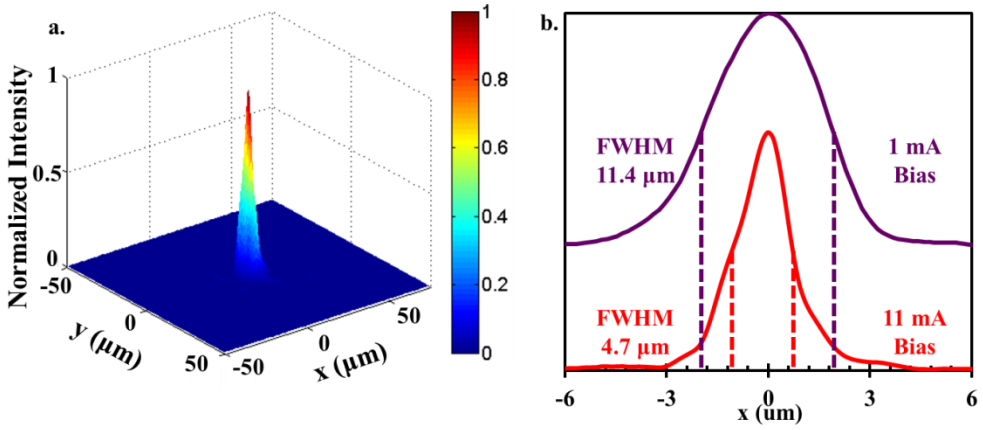


Figure 4.12 The normalized near-field profile of the Si-HCG VCSEL. Light is collected through a 100X objective and imaged by an InGaAs CCD camera set to 10 μS integration time. The measured FWHM collapses from 11.4 μm (below threshold) to 4.7 μm at 11 mA bias (lasing). The proton-implant aperture is 7 μm in radius.

4.3.3 Laser Spectrum and Thermal Performance

Using a Si HCG and AuSn bonding layer—instead of a traditional quaternary alloy DBR—results in excellent thermal performance. As mentioned above, the thermal conductivity of AuSn is roughly an order of magnitude better than for a quaternary alloy such as AlGaInAs. The thermal resistance of the laser is determined by the following ratio:

$$R_{th} = \frac{\Delta T}{\Delta P} = \frac{\Delta\lambda / \Delta P}{\Delta\lambda / \Delta T}. \tag{4.2}$$

The top and bottom terms in Eq. (4.2) can be extracted from the spectral properties of the laser. Figure 4.13 shows the wavelength shift of the device for varying injection bias (at a fixed heat sink temperature of 20 ºC), as well as the wavelength shift versus temperature (at a fixed injection current of 1.5 i_{th}). The wavelength shift versus temperature is 0.098 nm/K, and the shift versus dissipated power is measured to be 0.143 nm/mW, as shown in the insets of Figure 9(a) and (b), respectively, for an 8-μm radius proton-implant aperture VCSEL. Taking the ratio of these two numbers, the experimental thermal resistance of our device is 1.46 K/mW.

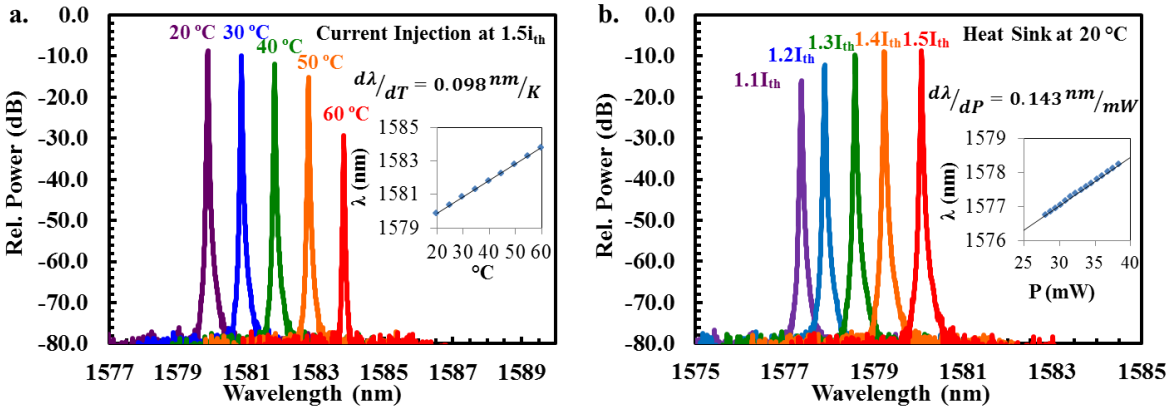


Figure 4.13 Spectrum at different (a) heat sink temperatures and (b) bias currents. Wavelength peaks are recorded to measure shift for varying injection biases, and heat sink temperatures, shown in the insets. The wavelength shift versus temperature is 0.098 nm/K, and the shift versus dissipated power is measured to be 0.143 nm/mW. The experimental thermal resistance of our device is 1.46 K/mW.

4.3.4 High-speed Modulation

Figure 4.14(a) shows the small signal direct modulation (S21) characteristics of the silicon HCG-VCSEL under room temperature CW operation, biased at various current levels. The photon-electron oscillation can be treated as a two-pole system. In a real system, the presence of device parasitics introduces a third pole:

$$H(\omega) = \frac{\omega_R^{\,2}}{\omega_R^{\,2} - \omega^2 + j\omega\gamma} \frac{\omega_P}{\omega_P + j\omega}. \tag{4}$$

where ω_R is the relaxation frequency of the VCSEL, γ is the damping parameter, and ω_P is the parasitic pole. From the family of curves, we extract a -3 dB frequency of 2.5 GHz, a damping coefficient of 9.6 x 10^9 s^{-1}, and a parasitic pole located at 1.4 GHz. As a result of the large mesa size, the device is limited by RC parasitics. Furthermore, we can extract the D-factor fitting from resonance frequency versus bias current to be approximately 5.8 GHz/$mA^{1/2}$, with a maximum resonance frequency of 5.4 GHz caused by thermal damping, as shown in Figure 4.14 (b).

For large signal modulation, the bit-error-rate (BER) waterfall curves and eye diagrams of a directly modulated HCG-VCSEL are shown in Figure 4.14(c). The device has error free (BER < 10^{-9}) operation up to 5 Gb/s at 20 ºC. Fiber transmission performance of the signal was assessed using before (back-to-back) and after transmission through a link of 2.5 km SMF.

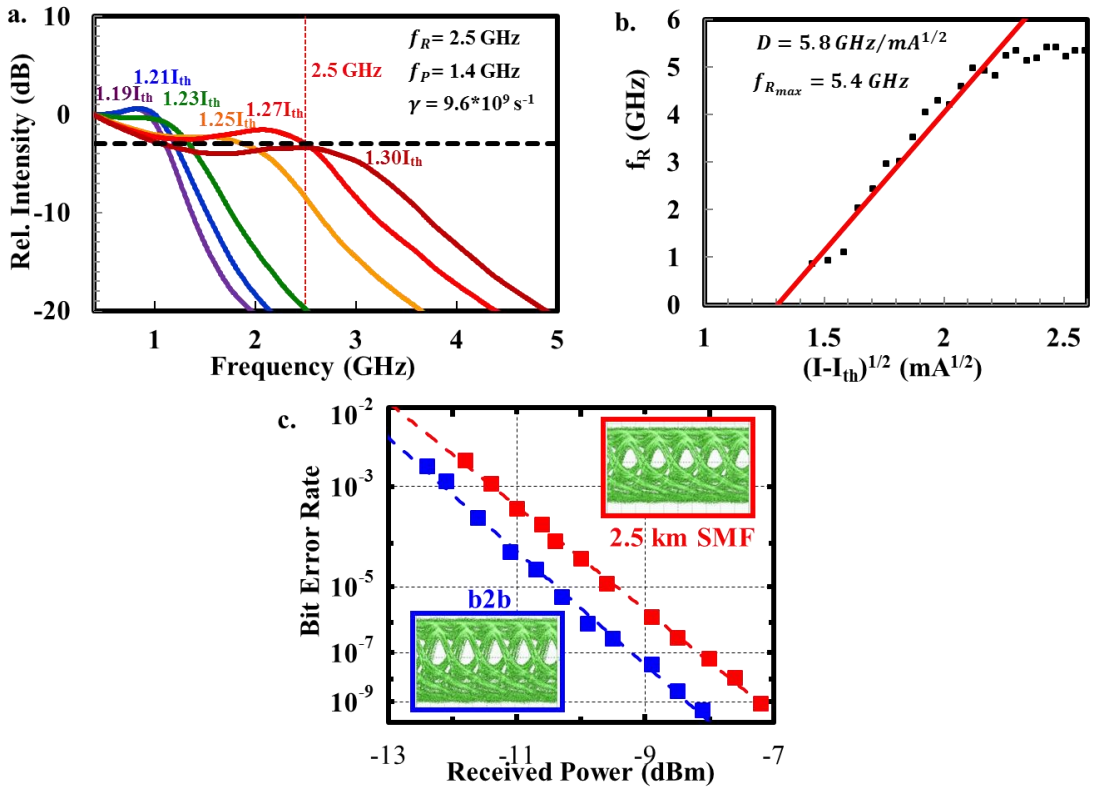


Figure 4.14 (a) Small signal direct modulation (S21) for Si HCG VCSEL at 20 °C for different current biases. A resonance frequency f_R= 2.5 GHz, parasitic pole frequency f_p=1.4 GHz, and damping factor γ=9.6x109 s^{-1}, are extracted from the family of curves. (b) D-factor fitting of VCSEL exhibiting thermal damping at 5.4 GHz. (c) BER measurements up to 5 Gb/s using On-Off-Keying (OOK) and eye diagrams before (back-to-back) and through a link of 2.5 km SMF.

4.3.5 VCSEL on a Flexible Substrate

Owing to its excellent thermal performance, individual dies of the hybrid VCSEL were transferred to a polydimethylsiloxane (PDMS) flexible substrate, as seen by the schematic in Figure 4. (a). The substrate is readily bendable without incurring damage to the VCSEL.

Figure 4.15 (a) The schematic for the VCSEL on a flexible substrate. The VCSEL is embedded inside PDMS with the top surface exposed. (b) Photograph of the measurement setup.

The device is biased using DC CuBe electrical probes and imaged with high magnification objectives. Even though the VCSEL is embedded in a low thermal conductance polymer, the device achieves lasing at 1562 nm under electrical pumping with continuous power greater than 0.6 mW. This is the first report for a C-band semiconductor laser working on a flexible carrier.

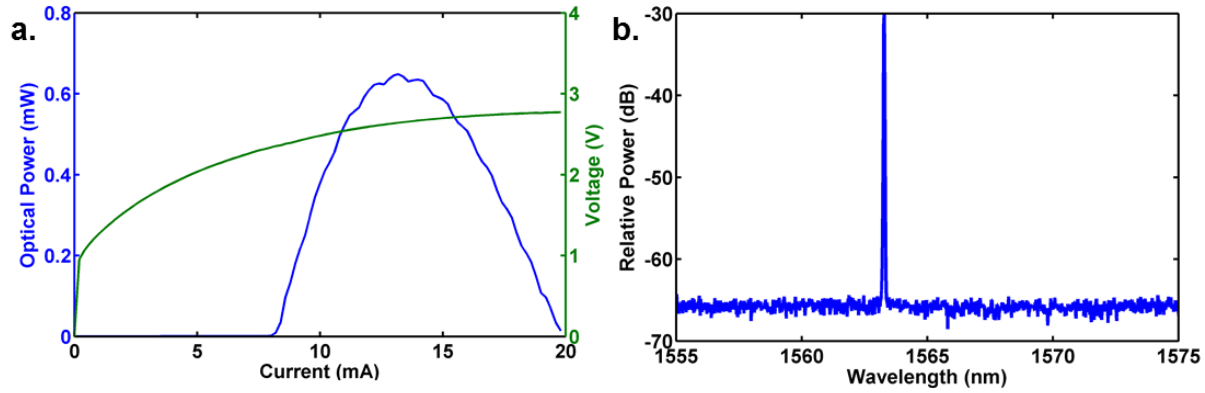


Figure 4.16 (a) The LIV curve of the VCSEL embedded in PDMS. The threshold current is 8 mA and the maximum output power is 0.65mW with 13.2 mA bias current. (b) The optical spectrum of the VCSEL embedded in PDMS. The device is lasing at 1563.3 nm with 11mA bias current.

4.4 Tunable VCSEL using MEMS Actuator

The tunable VCSEL is achieved by etching the buried-oxide layer in HF vapor and releasing the silicon HCG, as shown in the schematic in Figure 4.17. A major advantage of an HCG VCSEL on SOI is the sizeable buried oxide (BOX) thickness below the silicon device layer. The bottom silicon mirror of the HCG VCSEL can be actuated up to 1/3 of the gap thickness, which in standard SOI platforms is 3 microns. This translates to >40 nm of continuous MEMS tuning for a single-HCG structure with a 25:1 nm tuning efficiency.

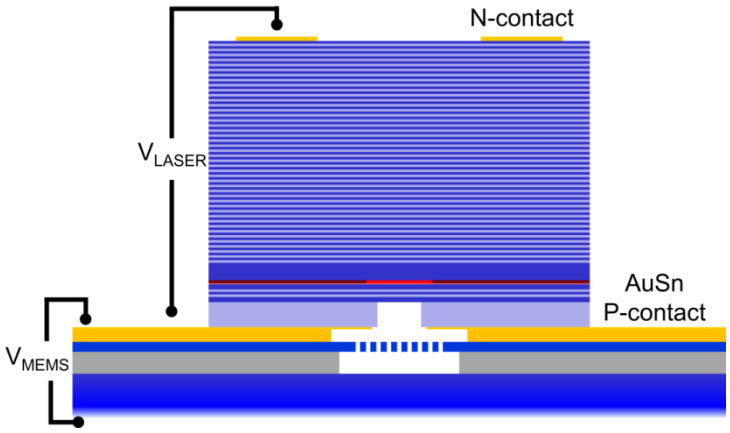


Figure 4.17 Biasing schematic of tunable Si HCG VCSEL.

The bottom mirror of the laser consists of a silicon HCG resting on oxide, as shown in the SEM in Figure 4.18 taken after the etching release step but before bonding with the III-V material system.

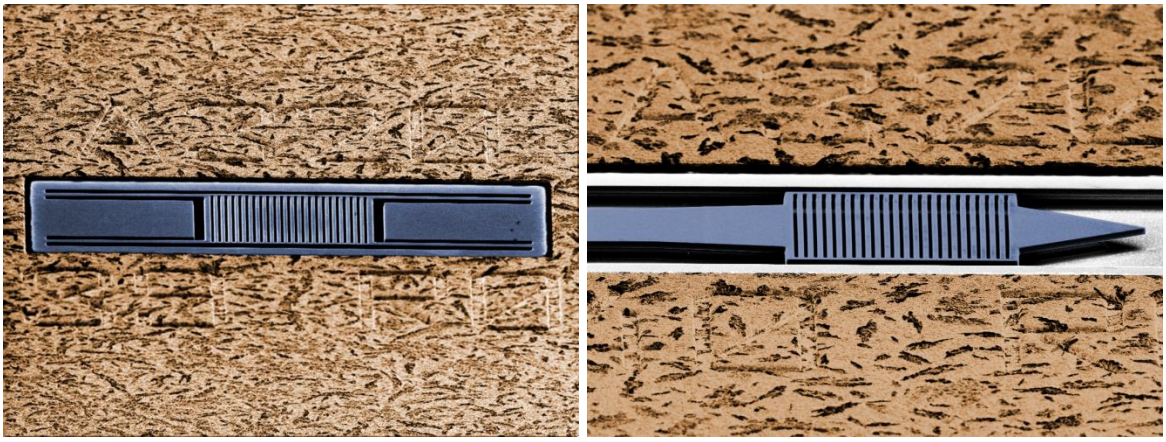


Figure 4.18 Tilted-view SEM of HCG reflector from a 75° viewing angle. AuSn is colorized in orange, silicon HCG in blue. The silicon device layer has been released in HF vapor. (Left) stand-alone HCG reflector. (Right) Reflector/coupler with waveguide. The sharp taper inhibits unwanted reflection and terminates the channel.

We also propose a reflector/coupler to channel the VCSEL light into a silicon waveguide (schematic is in Figure 1.8). The reflector/coupler device is also shown after the release step in Figure 4.18, with a waveguide to the left of the image.

4.4.1 Electrostatic actuator modeling

The MEMS structure consists of 15 μm-long and 1 μm-wide beams across a four-anchor suspended frame that is 450 nm thick (Si device layer). The buried oxide layer (BOX) is 1 μm thick. The HCG reflector pictured in Figure 4.23 is 16 μm x 16 μm, including the frame, and has an HCG with a period of 650 nm with a 50.77% duty cycle.

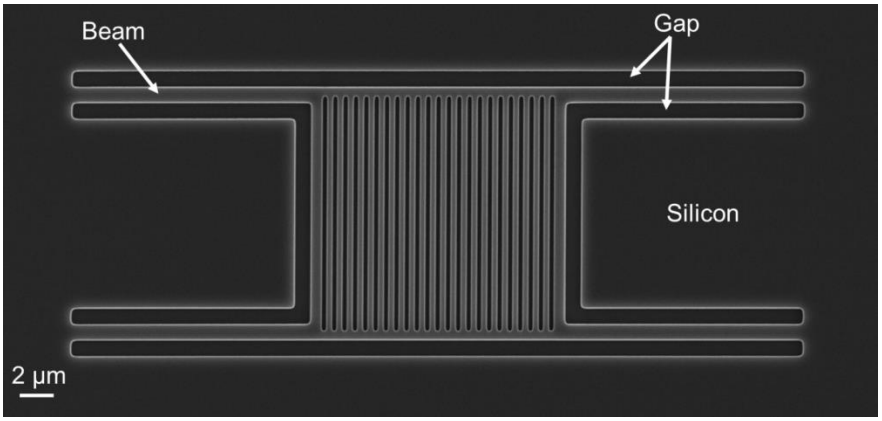


Figure 4.19. SEM of suspended HCG.

The actuator can be modeled as a parallel plate capacitor:

$$C = \frac{\varepsilon A}{(d_0 - z)} \tag{4.3}$$

where d_0 is the initial gap distance, and z is the displacement distance towards the substrate. The potential energy of the capacitor and spring system is given by:

$$U_{pot} = \frac{1}{2}CV^2 + \frac{1}{2}kz^2 = \frac{1}{2}\frac{\varepsilon A}{(d_0 - z)}V^2 + \frac{1}{2}kz^2 \tag{4.4}$$

where k is the spring constant of the structure. In equilibrium, the net forces acting on the structure is zero, or $F = \frac{\delta}{\delta z}U_{pot} = 0$, in which case we have:

$$F = kz - \frac{1}{2}\frac{\varepsilon A}{(d_0 - z)^2}V^2 = 0 \tag{4.5}$$

$$kz = \frac{1}{2}\frac{\varepsilon A}{(d_0 - z)^2}V^2 \tag{4.6}$$

Equation (4.5) is plotted in Figure 4.20.

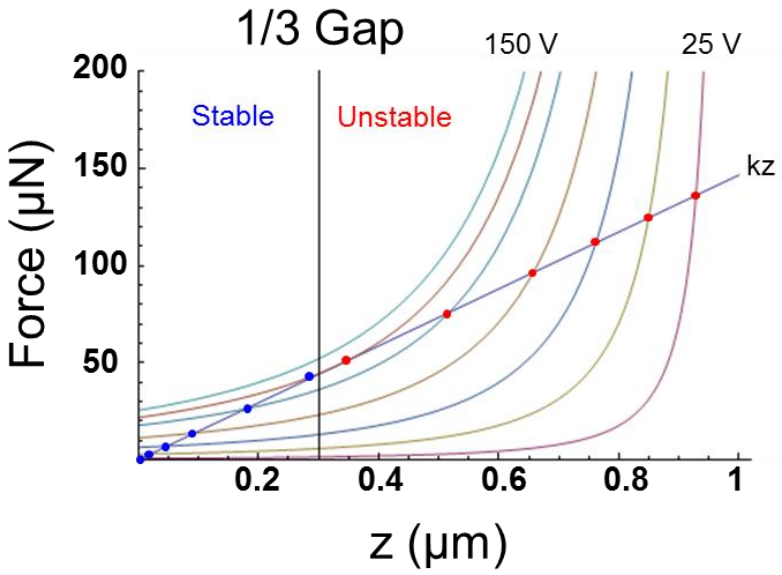


Figure 4.20 Restoring force versus electrostatic force. Stability conditions are highlighted in blue (stable) and red (unstable).

We can see from the plot that there are two solutions for every combination. However, stable solutions are only met when an increase in z results in a restoring force (straight line) that is larger than the electrostatic force (curved line). The stable condition can be described by the region where the slope of the total force is negative, or $\frac{\delta F}{\delta z} < 0$. With some algebra, it can be shown that the travel z of the actuator must not exceed 1/3 of the gap, also known as the "pull-in" condition:

$$\frac{\varepsilon A}{(d_0 - z)^3} V^2 - k < 0 \tag{4.7}$$

$$\frac{2}{(d_0 - z)} \frac{1}{2} \frac{\varepsilon A}{(d_0 - z)^2} V^2 - k < 0 \tag{4.8}$$

$$\frac{2}{(d_0 - z)} kz - k < 0 \tag{4.9}$$

$$z < \frac{1}{3} d_0 \tag{4.10}$$

The pull-in condition can be extracted from Eq. (4.7) and solving for the voltage, V:

$$V < \sqrt{\left(\frac{2}{3} d_0\right)^3 \frac{k}{\varepsilon A}} = \sqrt{\frac{8}{27} {d_0}^3 \frac{k}{\varepsilon A}} \simeq 0.544 \sqrt{{d_0}^3 \frac{k}{\varepsilon A}} \tag{4.11}$$

Using the model described in [71], the spring constant of a 4-beam actuator, or trampoline, can be described as:

$$k = 32Y\left(\frac{t}{L}\right)^3 w \tag{4.12}$$

where Y is the Young's modulus of the membrane material, t is the thickness of the membrane, L is the length of the spring arm, and w is the width of the beam. For the silicon HCG from Figure 4.19, we have:

$$k = 32 * 0.170\times10^{12}\left[N/m^2\right]\left(\frac{450\times10^{-9}\left[m\right]}{15\times10^{-6}\left[m\right]}\right)^3 * 1\times10^{-6}\left[m\right] = 146\left[N/m\right] \tag{4.13}$$

Applying the result from (4.13) into Eq. (4.11) provides a pull-in voltage of 196 volts. A series of calculated spring constants and pull-in voltages for various actuator designs is shown in Figure 4.21 and Figure 4.22.

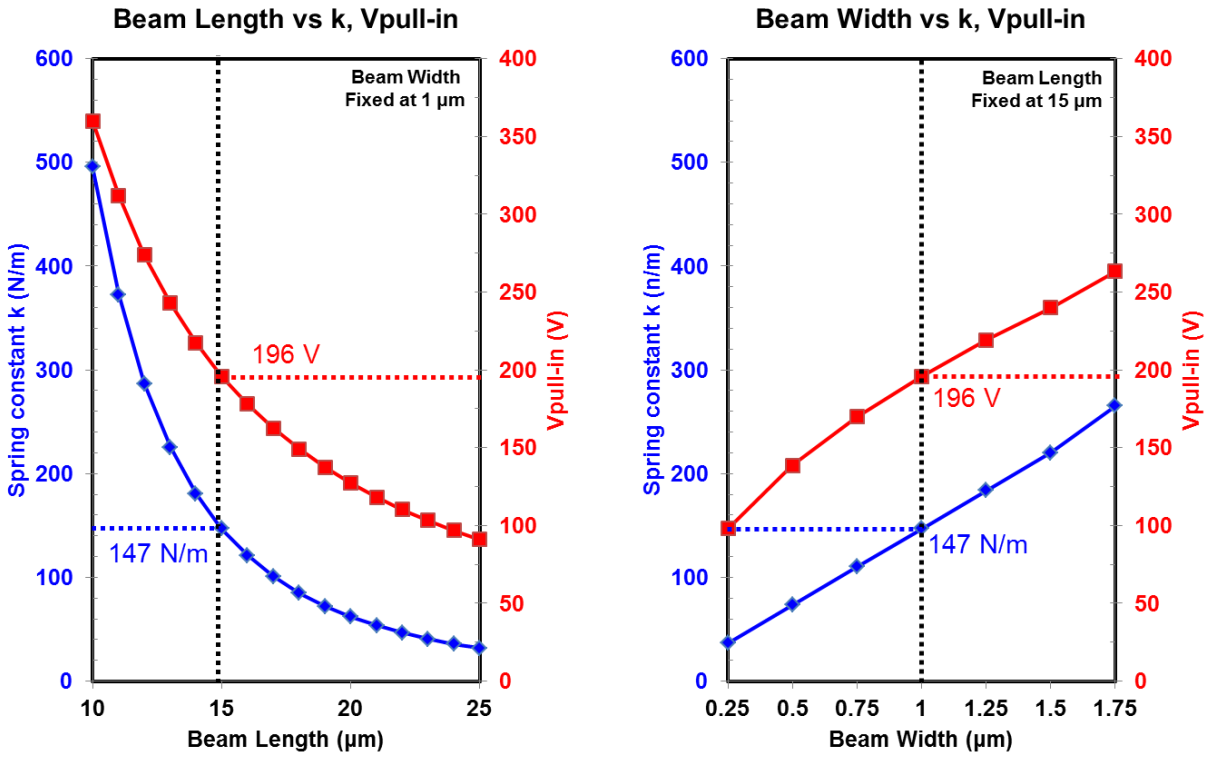


Figure 4.21 Beam length vs spring constant, k, and pull-in voltage maintaining a fixed beam width of 1 µm. Beam width versus spring constant, k, and pull-in voltage, maintaining a fixed beam length of 15 µm.

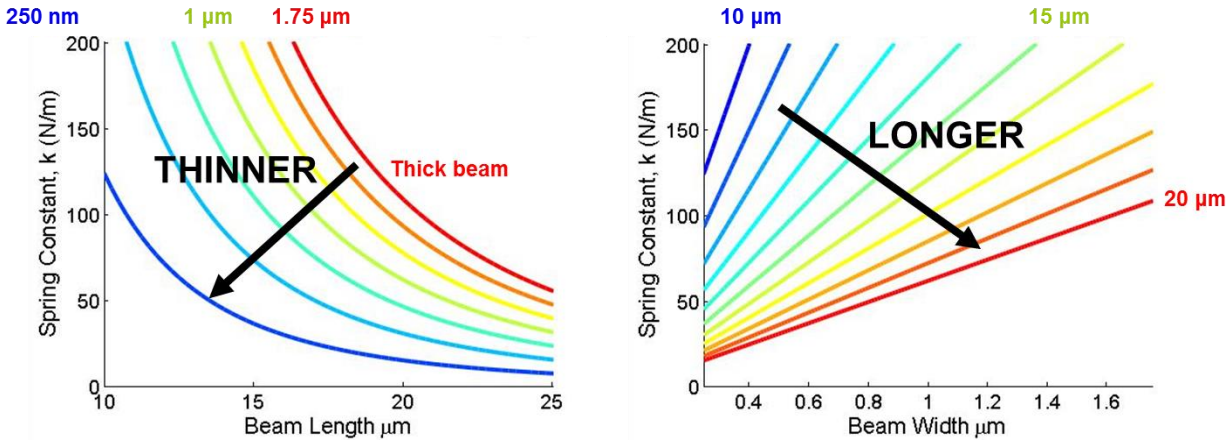


Figure 4.22 Family of curves of spring constant k for (a) variety of beam widths, and (b) variety of beam lengths.

With a known spring constant, k, and bias voltage V, we can use Equation (4.5) to compute the actuator displacement. For our structure, a 25:1 nm tuning efficiency is expected from the FDTD simulations in section 4.2.1.

Table 4.1 Calculated actuator displacement versus voltage.

Voltage	Displacement	Tuning
10	0.7 nm	28 nm
20	3.1 nm	124 nm
30	7.0 nm	280 nm
40	12.7 nm	508 nm
50	20.1 nm	804 nm
60	29.5 nm	1180 nm

4.4.2 Electrostatic actuator characterization

Before hermetic encapsulation with the III-V active structure, a AuSn contact and bonding layer is evaporated on the sample (Figure 4.23), the Si MEMS reflector is actuated by applying a bias between the AuSn metal contact resting on the silicon device layer and the backside of the SOI wafer. as illustrated in Figure 4.17

Figure 4.23 Close-up SEM image of released HCG reflector before actuation.

Using a confocal microscope, the displacement of the HCG reflector is measured in-situ mid-actuation. In Figure 4.25 we show a side-to-side comparison between a bias-free structure and an actuated HCG with a 35 V applied bias. For the latter, a 380 nm displacement below the original Si device layer is measured. Up to 464 nm of displacement is achieved before pull-in failure at 45 V. With a 25:1 tuning efficiency for our VCSEL structure, this actuation can potentially lead to > 18 nm of MEMS tuning. The displacement distance can be extended by using devices with BOX > 1 μm. For example, there are standard silicon photonics SOI wafers that have a 3 μm BOX. The voltage requirements are a function of the spring constant. Longer and thinner beams can reduce the spring constant considerably. Since the HCG actuator is inherently very thin, spring constants on the order of 10s of N/m can be designed. By reducing the beam width from 1 μm to 250 nm, and extending the beam length from 15 μm to 20 μm, the spring constant of the 460 nm thick HCG becomes 15.5 N/m.

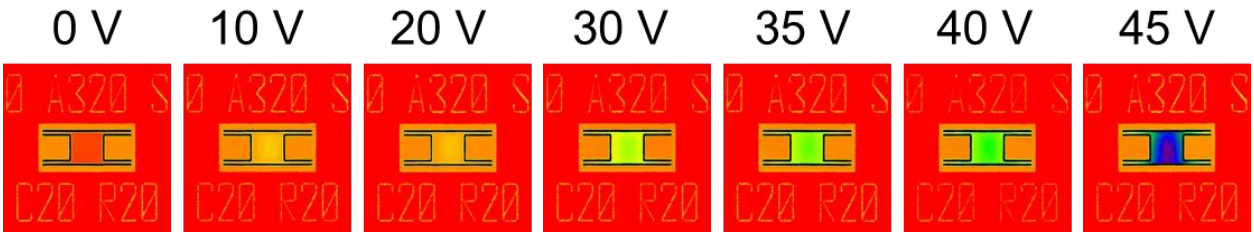


Figure 4.24 Confocal images of HCG MEMS actuator during a voltage sweep from 0 to 45 V. Pull-in failure occurs at 45 V, indicated by the purple region where the HCG bars experience stiction failure to the silicon substrate.

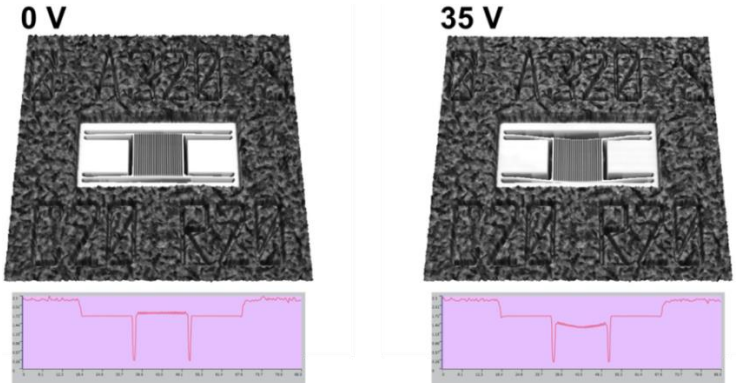


Figure 4.25 Confocal microscope 3D image of silicon HCG reflector biased at 0 V and 35 V. The HCG is displaced 380 nm below the original Si device layer. Up to 464 nm of displacement is achieved before pull-in failure at 45 V.

4.4.3 VCSEL tuning results

Figure 4.26 shows preliminary light-current-voltage (LIV) characteristic of a VCSEL with CW operation with >0.3 mW CW power out-coupled from the semiconductor DBR at 15 ºC. The device temperature is controlled with a thermo-electric cooler on a copper chuck. A Keithley current source is used to bias the VCSEL via electrical probing. Light is collected by a large-area germanium photodetector placed above the VCSEL. The VCSELs exhibit thermal rollover with increasing current bias due to gain spectrum red-shifting more rapidly than the resonant cavity spectrum, an effect typical in VCSELs. The device threshold current i_{th} is 2.3 mA, substantially lower than fixed wavelength HCG VCSELs. This is attributed to the higher index contrast of the released reflector. The ripples on the LI curve are due to residue reflection from the back of the silicon substrate/air interface, as verified by the output spectra measured at various currents corresponding to the peaks and valleys of the L-I curve and the substrate thickness. The L-I ripples can be eliminated with backside roughening of the substrate.

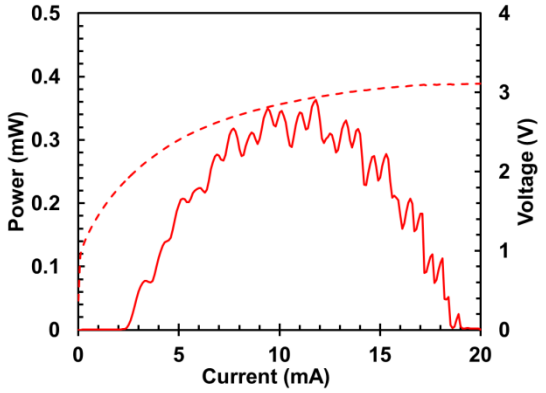


Figure 4.26 CW LIV of Si HCG VCSEL with suspended HCG from 0 to 20 mA. Threshold current is 2.3 mA, and peak CW power is 0.36 mW at 11.8 mA forward injection current. Light is collected with a large-area Ge photodiode for the LI measurement.

Furthermore, a secondary voltage source (V_{MEMS}) is used to actuate the suspended Si HCG to perform wavelength tuning of the VCSEL. A voltage sweep from 0 to 45 V provides 0.32 nm of wavelength tuning, shown in Figure 4.27.

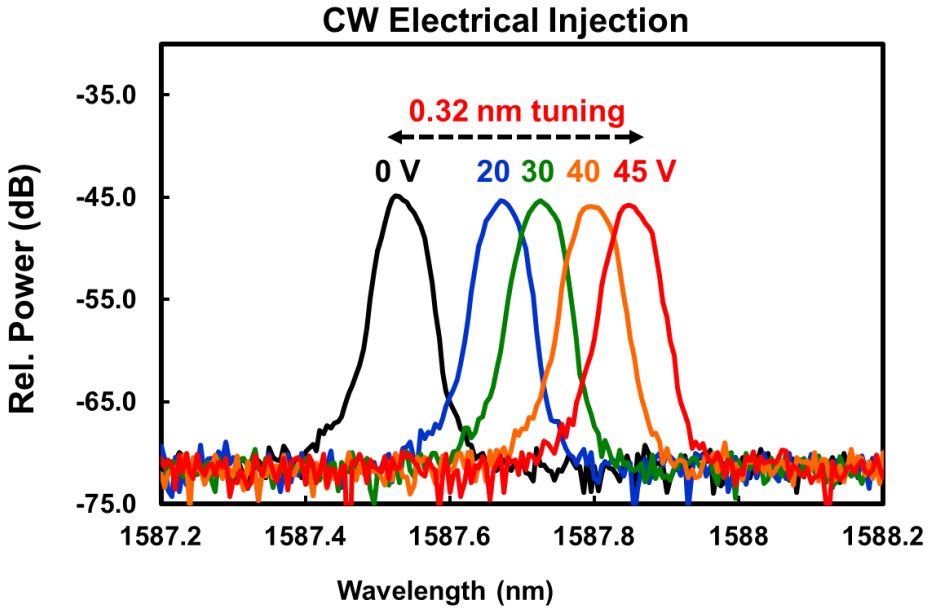


Figure 4.27 Spectrum of Si HCG VCSEL at different V_{MEMS} bias voltages, ranging from 0 to 45 V. Wavelength peaks are recorded to measure shift for varying V_{MEMS} bias.

Although the tuning distance falls short of the expected 18 nm, the results are quite promising. In our current arrangement, the MEMS actuators are addressed as an ensemble. That is, all 900 devices on the chip are actuated *simultaneously*. This is a consequence of a legacy version of our SOI contact scheme and can be readily engineered to perform single addressing. However, one of the repercussions of ensemble addressing is that many shunts paths may form along the contact plane of the SOI and the backside of the device. Much of the heterogeneous processing was performed after release, including bonding and mesa wet etching, during which several of the actuators are exposed to viscous liquids, which causes them to collapse onto the substrate. As a result, the applied voltage has to overcome an ensemble parasitic resistance to actuate a single VCSEL. Although we applied the same bias from the actuator experiment in 4.4.2, the voltages seen in Figure 4.27 are not directly across the tuning junction.

4.5 All HCG VCSEL

In this section we describe work towards an all-HCG VCSEL on silicon. As in previous the previous sections, the active layer of this device consists of AlGaInAs compressively-strained quantum wells (QWs) and employs proton implant for current confinement. For an all-HCG structure, we no longer employ a tunnel junction for carrier conversion. The Fabry–Pérot cavity,

indicated by circulating red arrows in Figure 4.28, is formed by an InP HCG top mirror and a silicon-on-insulator (SOI) HCG bottom mirror.

The total thickness of the double-HCG VCSEL can be only 3 μm, much thinner than the conventional VCSEL (~ 10μm). The effective cavity length is also smaller, making it possible to achieve ultra-wide frequency tuning range without mode hops. The light-weight HCG mirror also enables ultrafast (> 10 MHz) frequency sweeping of FMCW sources.

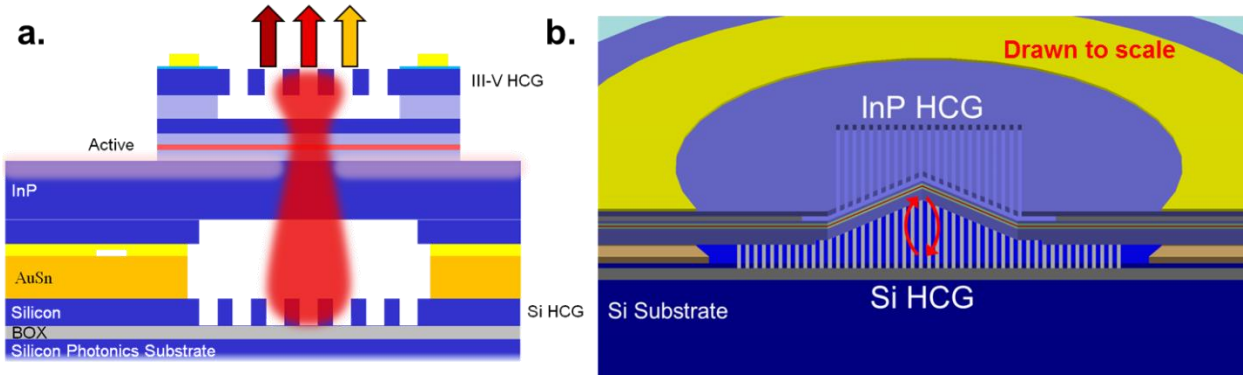


Figure 4.28 (a) Cross section schematic of All HCG VCSEL on SOI. Because the cavity can be as short as 3 μm, this can also provide gains in MEMS tuning efficiency and faster high-speed direct modulation. (b) 3-D view drawn to scale. The BOX layer (grey) is 1 μm.

4.5.1 Design and simulation

The top InP HCG has a period of 710 nm and a duty cycle of 64.79%. The bottom SOI HCG is the same as in section 4.2.1. Using the Transfer Matrix Method, we verify the existence of a suitable all-HCG optical cavity, as shown by the traces in Figure 4.29 (a) and (b).

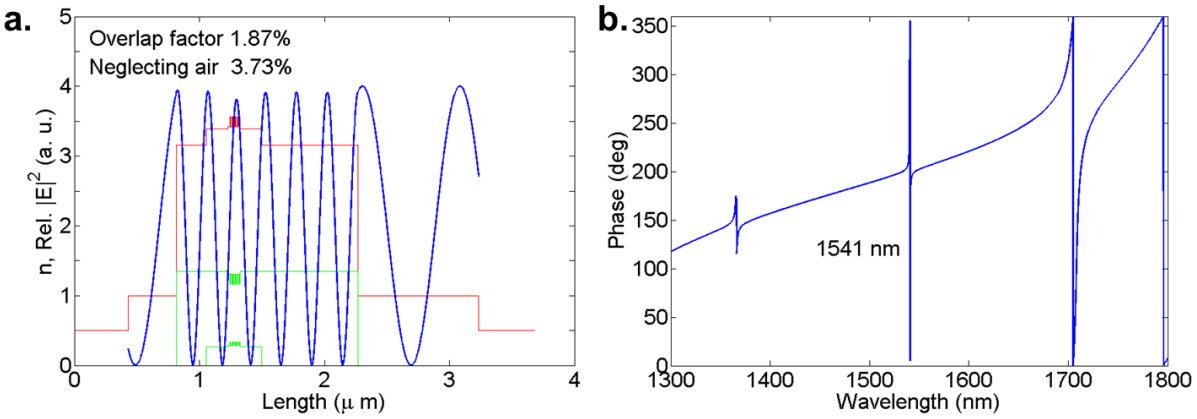


Figure 4.29 Overlap factor is 3.33%. Resonant cavity at 1523 nm. The photo luminescent (PL) peak of the epitaxial structure is located at at 1510 nm.

The red trace denotes the optical index of refraction along the epitaxial structure; green represents the conduction and valence bands; and the blue trace indicates the optical intensity buildup within the cavity. With our current InP and Si HCG designs, we can attain a **3.73%** overlap factor with the quantum well structures. Furthermore, the cavity exhibits a high Q resonance at 1541 nm, shown in Figure 4.29 (b), which is designed to target the C-band emission of the device.

4.5.2 Proton-implant simulations

Following the same procedure as in section 4.2.3, the design of the implant depth was simulated with TRIM. One important difference is that the epitaxial structure employed for the all HCG VCSEL does not have a tunnel junction. The doping profile is p-i-n. As mentioned in 4.2.3 structure, the goal of the simulations is to find the energy at which the peak distribution of implanted ions is within 100-200 nm of the active region. However, care must be exercised in choosing the dose of implant species, since implanted regions *will not* repair easily with rapid thermal annealing (RTA). Figure 4.30 (a) shows the distribution versus depth of H^+ ions for a 225 KeV implant energy, which reaches a median depth of 1.79 μm. Figure 4.30 (b) highlights the range of the peak ion concentration versus energy and the corresponding lateral straggle. Higher energy species tend to walk-off in random directions, and may close off an implant window. From the simulations, a 225 KeV implant energy will result in a 700 nm lateral straggle through the epitaxial structure. The implant blocking protection used to define the aperture of the VCSEL must take into account the lateral straggle.

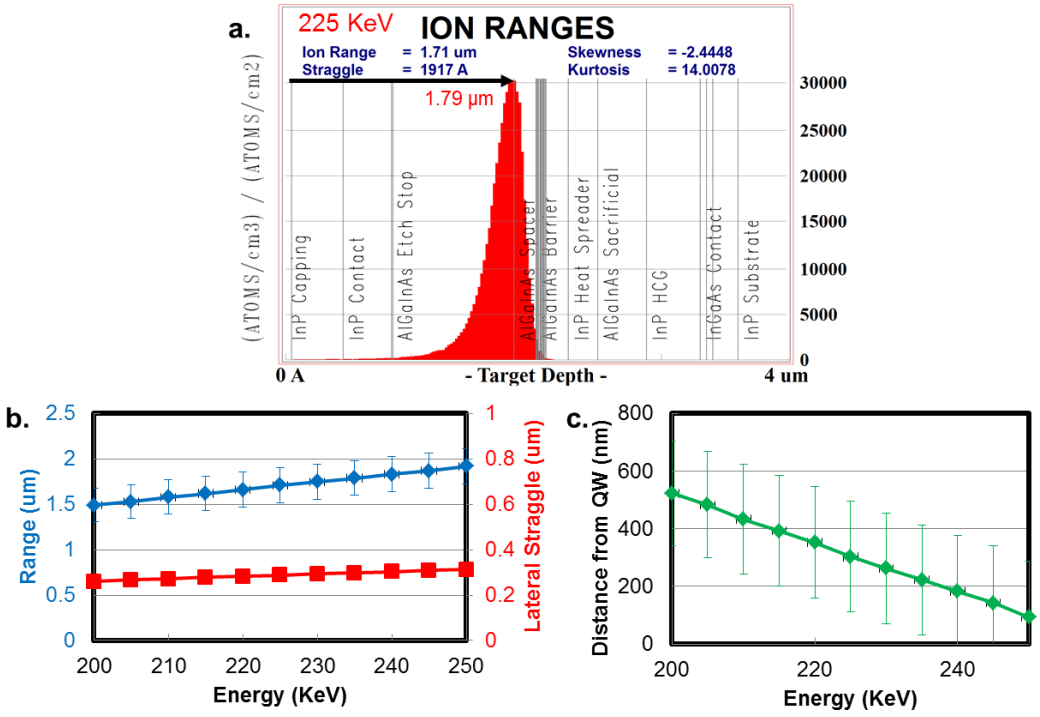


Figure 4.30 (a) TRIM Monte Carlo simulation showing the skewed normal distribution versus depth of H^+ ions implanted at 225 KeV into the all-HCG

epitaxial stack. (b) The range versus implant energy, including lateral straggle. (c) The distance from the active region quantum well (QW) including radial straggle.

A set of implant energies and doses were tested on the epitaxial wafers. Figure 4.31 highlights the main results of electroluminescence experiments on the samples. For the case of 200 KeV implant energy, the peak distributions of protons falls well short of the active region. This allows the injected holes to diffuse out from under the implant sheet and spread into the active region. As a result, the whole mesa structure of the LED formed with the epitaxial structure becomes illuminated. The bottom half of Figure 4.31 shows that the highest intensity is captured near the implant aperture surrounded by the metal annulus. For the case with 225 KeV implant energy, the current is well-confined to the region surrounded by the metal contact. The result is a well-defined region of radiative-recombination.

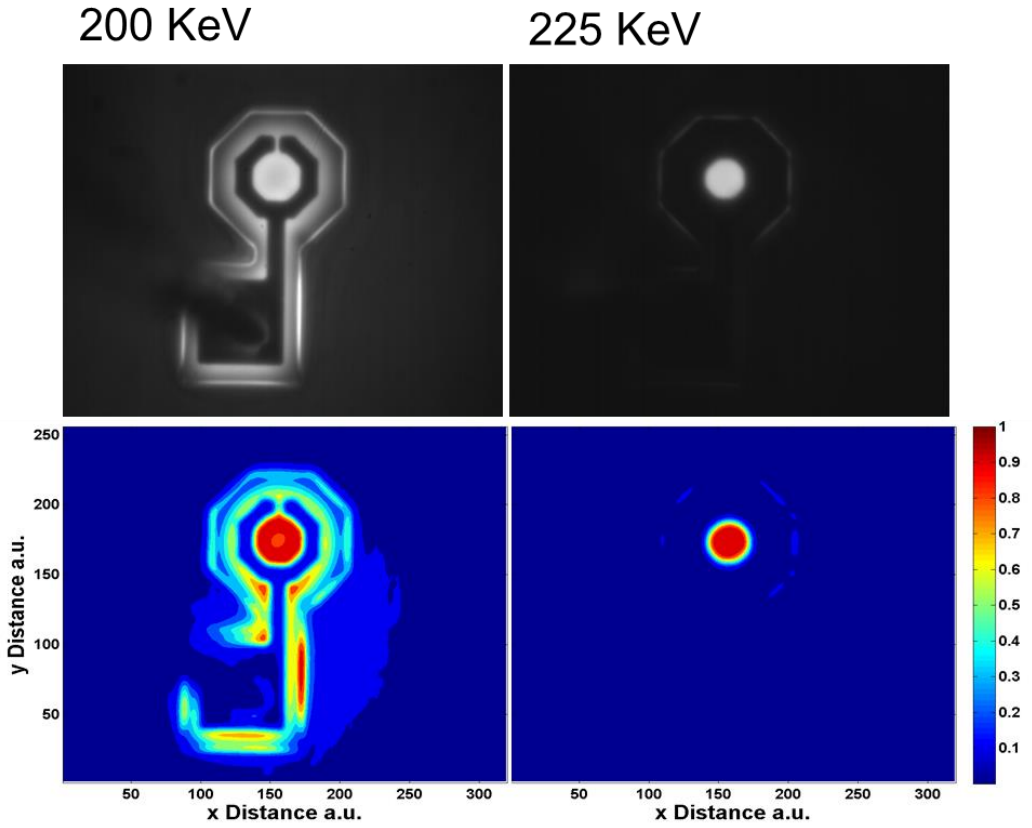


Figure 4.31 Infrared image of LEDs captured with an InGaAs CCD camera. For two implant energies. The 225 KeV implant energy provides much better current isolation. The implant dose used is $1x10^{13}$ cm^{-2}. The current injection bias is 25 mA.

Furthermore, the current blocking properties of different doses were characterized via I-V measurements. Figure 4.32 shows families of traces for devices with different implant aperture sizes grouped by dose quantity. The voltages measured correspond very nearly to leakage open circuit voltages, since the p-type implant region was not thermally annealed. The result is

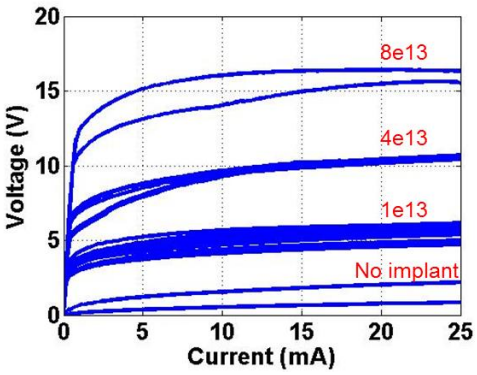
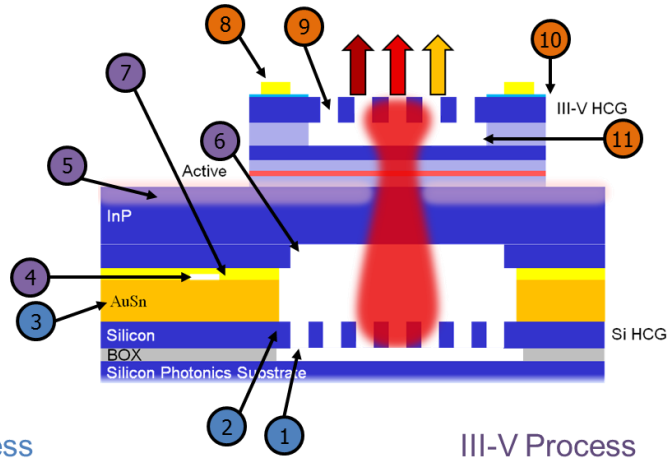


Figure 4.32 I-V graphs for LEDs for various proton implant doses (in species/cm^2). The differential resistance of the devices is ~ 40 Ω.

4.5.3 Fabrication

Figure 4.33 summarizes the process flow for the all-HCG VCSEL. The process consists of three ASML DUV stepper lithography steps (blue), eight contact lithography steps (purple and orange), and a single e-beam step which is substitutable by DUV lithography. Figure 4.34 is a confocal image of the fabricated device.



SiPh Process

- Oxide Hard Mask
- Full Thickness Etch Mask Litho (Mask1)
- Doping for MEMS Actuators (Mask2)
- P-contact Metal Deposition Litho (Mask3)
- BOX Release

III-V Process

- Alignment Key Litho (Mask4)
- Proton Implant Litho (Mask 5)
- Cavity Etch Litho (Mask 6)
- P-contact Metal Deposition Litho (Mask 7)

Heterogeneous Process

- Substrate Removal
- N-contact Metal Deposition Litho (Mask8)
- HCG Patterning via E-Beam (Mask9)
- Mesa Etch Litho (Mask10)
- Release Etch Litho (Mask11)

Figure 4.33 All-HCG fabrication process flow. The heterogeneous process involves 11 lithography steps.

Figure 4.34 A confocal optical image of the fabricated device.

4.5.4 Experimental results

Figure 4.35 (a) shows the room temperature LIV measurements for an all-HCG device, and (b) is an infrared image of a device under forward bias showing a well-defined proton-implanted aperture. In order to avoid damaging the device, small current injection sweeps were performed from 0 to 7 mA. Proton implant devices benefit from a self-healing process known as "burn-in", in which current is injected across an implanted junction to reduce series resistance. However, for current greater than 7 mA, the device shunts and loses rectifying behavior, extinguishing any radiative recombination.

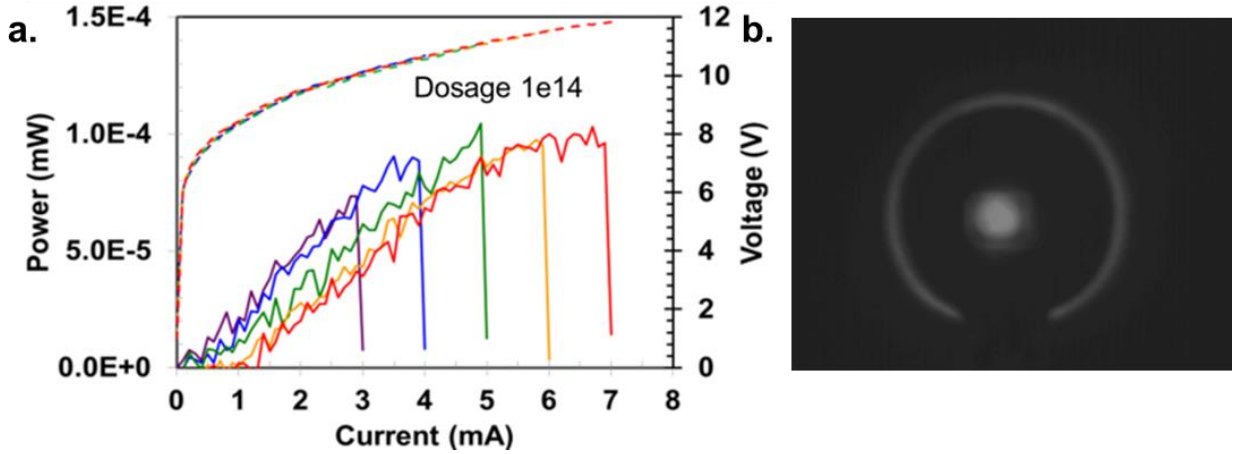


Figure 4.35 (a) Room temperature LIV measurement of all-HCG devices at different bias currents. Incremental current sweeps (0-3 mA, 0-4 mA, etc.) were performed on the device. (b) Infrared image of device under 2 mA bias and 100X magnification showing a well-defined proton-implanted aperture.

The cause is attributed to a very narrow pathway allowed for carriers to pass from the p-type layer into the active region. Step 6 in Figure 4.33 involves the etching of a large trench in the epitaxial structure to shorten the cavity length of the device and ensure round trip resonance. However, this has a detrimental effect for the electrical properties of the device. The lateral travel distance for carriers becomes quite large to reach the active region, on the order of 10s of microns, whereas the vertical direction is a few lambdas. This sheet of material that carriers have to transverse is also heavily implanted with protons, and since it is p-type, it is not readily annealed. This manifests itself in the very high voltage across the device, often greater than 5 V. Thus, the excessive heating and consequent shunt, prevent the device from reaching lasing threshold. The all-HCG epitaxial structure can be redesigned to circumvent the need for a cavity trench, and the electrical contacts can be brought closer to the center region without overlap with implant species. This will ensure proper electrical behavior conducive to lasing devices.

4.6 Summary

In this chapter, an electrically pumped AlGaInAs-silicon VCSEL structure using a high contrast grating is described. The device exhibits CW power >1 mW and operation up to 65º C. Direct modulation of the VCSEL with small-signal bandwidth >2.5 GHz, and 5 Gb/s large-signal direct modulation was also realized with error free transmission over a 2.5 km fiber link. Employing the Si HCG as a MEMS electrostatic actuator, CW tuning across 0.32 nm is also reported.

In an attempt to improve the thermal performance and power output of the device, an effort to develop an all-HCG VCSEL on SOI is also documented. Because the cavity of an all HCG can be as short as 3 μm, this can also provide gains in MEMS tuning efficiency and faster high-speed direct modulation. Electrical injection devices were designed, fabricated, and characterized, but did not achieve lasing threshold. This is attributed to epitaxial structure constraints, as well as implant layer design issues which can be readily overcome with new designs.

HCG-VCSELs on silicon offer a low cost, energy efficient, scalable solution for integrated laser sources for silicon photonics circuits. A Si-HCG can be designed to provide high reflection (>99.4 %) as well as function as a coupler for in-plane SOI waveguides. This device can be important for scalable, low-cost integrated photonic circuits including lasers, optical amplifiers and other III-V based active components.

Chapter 5

Integrated Wavemeter

"What is why?"

5.1 Introduction

An optical wavelength meter, or *wavemeter*, is an instrument that provides the wavelength of a monochromatic signal. This principle can be extended to an optical spectrum, in which case we arrive at the instrument known as a *spectrometer*. Traditional wavemeters consist of bulk optical components that may contain scanning parts such as Michelson interferometers[72]–[75], Fabry-Pérot etalons [76], static Fizeau interferometers [77]–[81] and Wollaston prisms [82]. Generally the instruments require very stable conditions and have a large footprint.

Although resolution may be considered a key metric for the performance of a wavemeter, there are cases where a coarse estimate of wavelength is sufficient. With the recent emergence of tunable lasers as key components for dense wavelength-division-multiplexed (DWDM) optical telecommunication systems [83]–[85], there is an increasing need for compact, efficient, and low-cost wavemeters.

In this chapter, we propose and describe a wavemeter design that employs high contrast metastructures (HCMs) and operates on a silicon photonic integrated circuit (PIC) platform. The 3D schematic in shown in Figure 5.1.

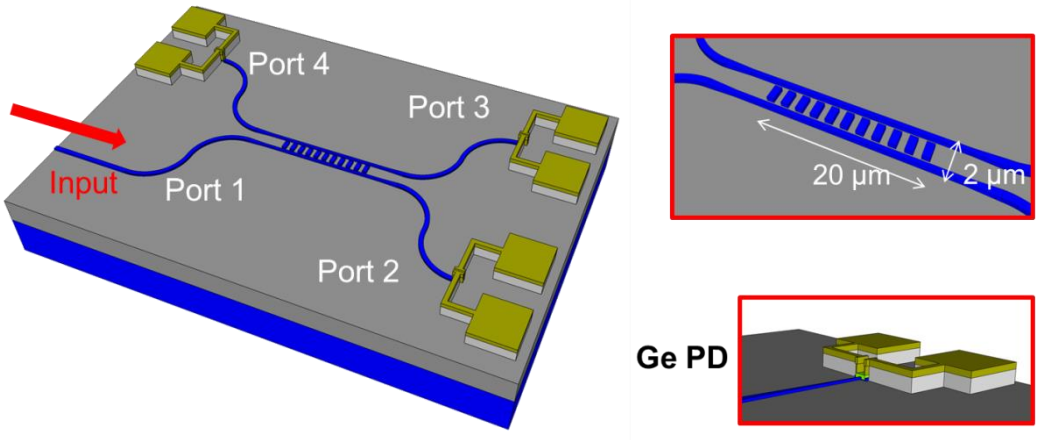


Figure 5.1 Schematic of wavemeter for a silicon photonics platform. The device is a four port coupler with a high-contrast metastructure in between single mode silicon waveguides. Light is collected by germanium photodetectors at exit ports. The footprint is roughly 20 x 2 μm^2.

5.2 Design

5.2.1 Dielectric grating coupler principle

The design of the wavemeter is modeled after a traditional dielectric grating coupler for injecting light into a thin-film optical waveguide [86]. A simplified example is shown in Figure 5.2. Free-space light is incident on the diffractive structure with a propagation constant $\boldsymbol{k_0 \sin\theta}$. The subwavelength grating creastes an additional propagation constant $\boldsymbol{m\frac{2\pi}{\Lambda}}$, which provides the necessary momentum to the light beam to match the waveguide mode $\boldsymbol{n_{eff}k_0}$. The phase matching condition can be readily described by the following equation:

$$k_0 \sin\theta + m\frac{2\pi}{\Lambda} = n_{eff}k_0 \tag{5.1}$$

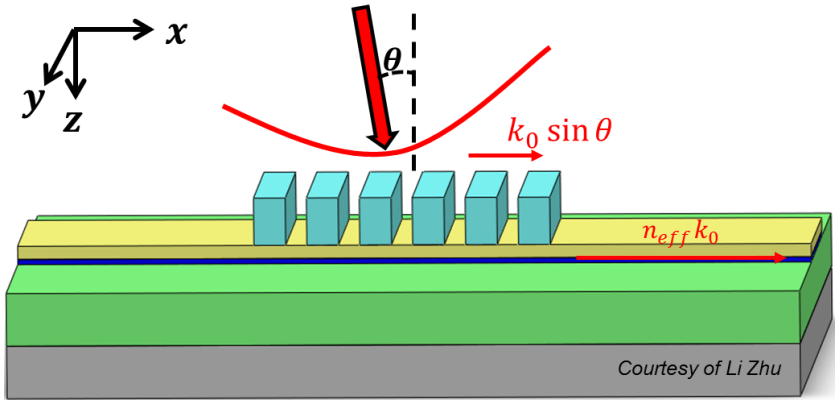


Figure 5.2 Schematic of dielectric grating coupler into thin film waveguide. Light is incident at an angle θ onto dielectric gratings (light blue). A low index spacer (yellow) separates the diffractive structure from the thin film waveguide (dark blue). Schematic courtesy of Li Zhu.

Expanding on this principle, we can define the coupling angle of incident light as a function of wavelength:

$$\theta = arc\sin\left(n_{eff(\lambda)} - m\frac{\lambda}{\Lambda}\right) \tag{5.2}$$

The effective index of a waveguide is a function of the index of refraction of the core of the waveguide, as well as its surroundings, the waveguide dimensions (width and thickness), and also the polarization of light. Using the effective index method [30], the solutions for both slab and strip waveguides are calculated with the following parameters at λ=1.55 μm: (for slab) top cladding n = 1.45, core n = 3.46, bottom cladding n = 1.45, thickness = 230 nm, polarization = TE; (for strip) side cladding: n=1.45, core index = n_{slab}, width = 300 nm, and polarization=TM.

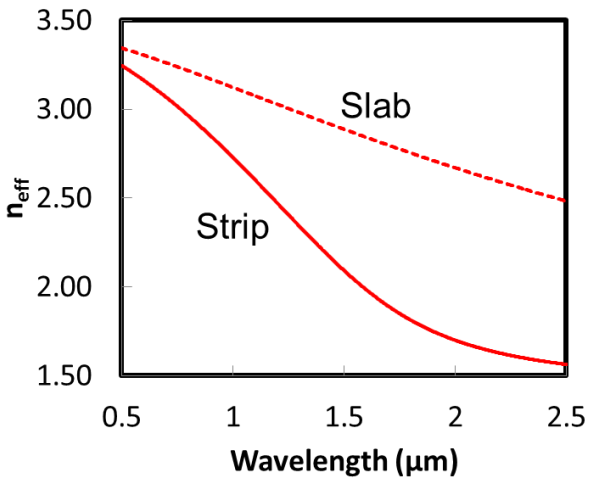


Figure 5.3 Effective indices versus wavelength of a slab waveguide that is 230 nm thick, and a strip waveguide that is 230 nm thick by 300 nm wide.

Intuitively, the guided mode will travel with an effective index that lies somewhere in between the index of refraction of the core and surrounding cladding, in this case silicon (n=3.46), and silicon dioxide (n=1.45), respectively. The strip waveguide will have a have a smaller effective index due to confinement effects.

Feeding these results into Eq. (5.2), the relationship between coupling angle and wavelength is plotted below for different orders *m*. It is desirable to find a wavelength window where the coupling angle behaves in a linear fashion, and also inject predictable forward or backward leakage waves into the thin film waveguide.

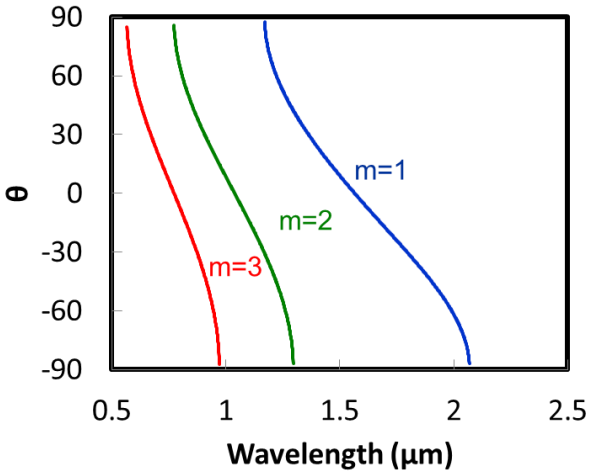


Figure 5.4 Coupling angle versus wavelength for a dielectric grating coupler above a Si strip waveguide surrounded by silicon dioxide, with waveguide dimensions of 230 nm x 300 nm, and grating coupler period Λ = 775 nm.

5.2.2 Four port coupler

This dielectric grating coupler principle can be extended to a four port coupler with neighboring waveguides, as shown below in the schematic in Figure 5.5. The goal is to design an HCM with known, well-behaved wavelength dependence, such that the ratios between the ports can be used to determine the absolute wavelength, power, and temperature of incoming light. For example, if we treat port 1 as the input, we can measure the power ratio between the through port 2 (S_{21}) and the coupled port 3 (S_{31}) using photodetectors. If the ratio S_{31}/S_{21} has a well-known pre-determined value with respect to wavelength, the absolute wavelength incoming from port 1 can be determined. The varying coupling angle dependence of the grating from Eq. (5.2) meets these requirements.

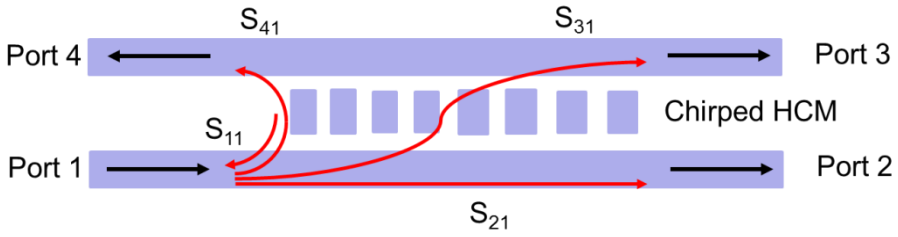


Figure 5.5 Proposed scheme for a compact four-port coupler. Top view of silicon device layer. Incoming light arrives at Port 1. The power rations between Port 3 and Port 2 (P_3/P_2) and P_2/P_4 can be used to determine the wavelength of light.

5.2.3 Fabrication constraints

In order to make the wavemeter, we participated in a multi-university collaboration with Sandia National Laboratories (SNL) and their Microsystems and Engineering Sciences Applications (MESA) facility. In recent years, the MESA facility has engineered a 1st generation silicon photonics process for electro-optical silicon photonic integrated circuits built on silicon-on-insulator (SOI) wafer technology. The process includes silicon and silicon nitride waveguide interconnects, p- and n-dopants, metal interconnects, and germanium epitaxial growth with dopant implants. A cross section of the process is show in Figure 5.6, and a summary of the processing guidelines is in Table 5.1.

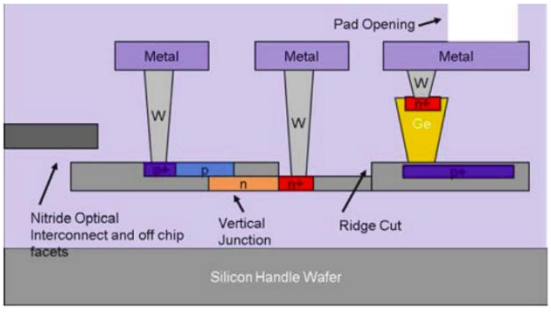


Figure 5.6 Cartoon illustration of the cross-section of Sandia's SPP1 process with a subset of possible implant configurations.

Table 5.1 SNL MESA silicon photonics processing guidelines

Resolution limit	180 nm
Minimum linewidth	100 nm
Minimum spacing	280 nm
Recommended waveguide width	400 nm
Recommended coupling waveguide width	320 nm

The constraints for the wavemeter dimensions are delimited by the processing guidelines in Table 5.1. The parameter sweep for the wavemeter design thus entails the following parts (summarized in Figure 5.7): *w*, the waveguide thickness (adjacent to HCM); *g*, the spacing gap between waveguides and the HCM; t_g, the thickness of the HCM; *s*, semiconductor width of the HCM bars (duty cycle); and Λ, the period of an HCM. The SOI device layer thickness is fixed at 230 nm. In the figure, $M_{1\text{-}5}$ indicate regions of interest for power and field calculations.

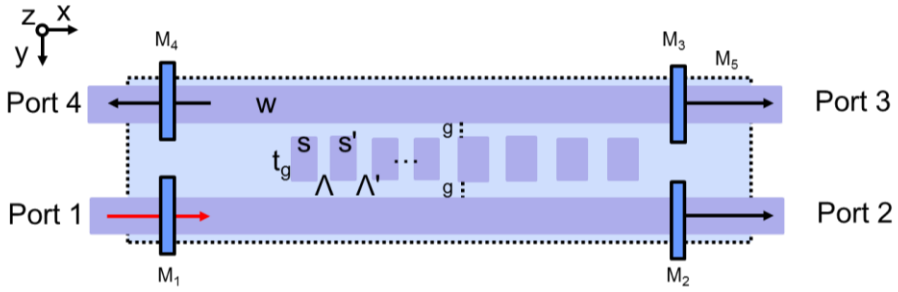


Figure 5.7 Wavemeter parameters. *w*, the waveguide thickness; *g*, the spacing gap between waveguides and the HCM; t_g, the thickness of the HCM in the y-axis; *s*, semiconductor width of the HCM bars (duty cycle); and Λ, the period of an HCM.

5.3 Simulation

The 3-D parameter space of the wavemeter is explored using FDTD. The starting conditions are:

Table 5.2 Wavemeter starting conditions.

Waveguide width, w	300 nm
Waveguide thickness	230 nm
Gap, g	280 nm
HCM number of bars, N	10
HCM period, Λ	820 nm
HCM width, s	500 nm
HCM thickness, t_g	985 nm
Waveguide polarization	TM

A waveguide mode is launched into a 300 nm wide by 230 nm silicon channel embedded in silicon dioxide. Figure 5.8 shows the electric field intensity of the waveguide mode extending in the vertical z direction. However, coupling occurs evanescently in the y direction.

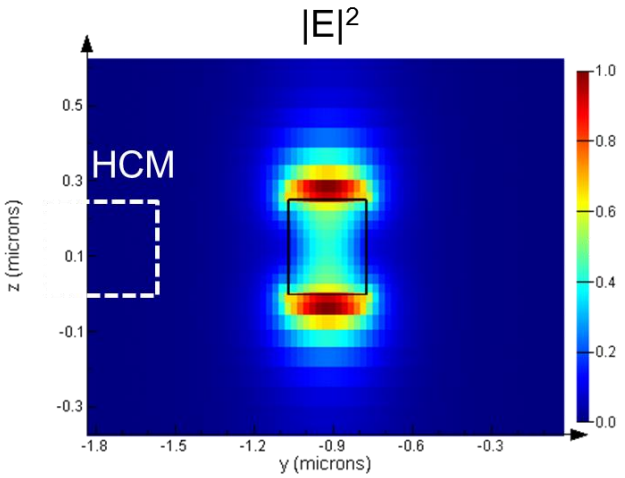


Figure 5.8 Cross section of the waveguide with the neighboring HCM. The electric field intensity is plotted along the y-z cross section of the waveguide. The propagation direction is along the x axis.

In Figure 5.9, the E_z component of the electric field is plotted. The majority of the intensity comes from this component, which makes it a TM polarized waveguide. The HCM is polarization sensitive to TM.

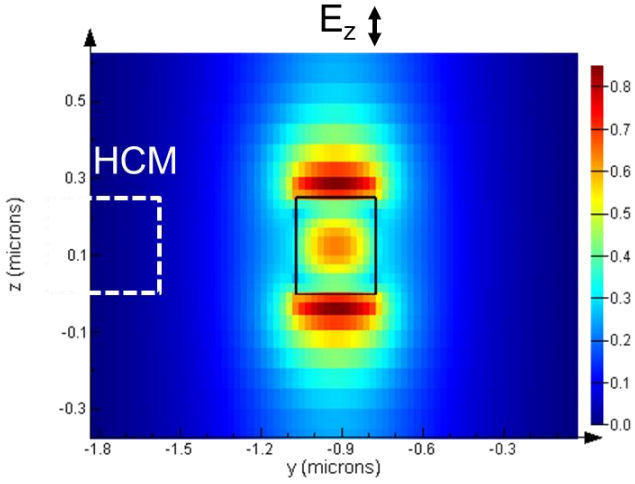


Figure 5.9 Electric field component along vertical E_z direction.

5.3.1 Waveguide width parameter sweep

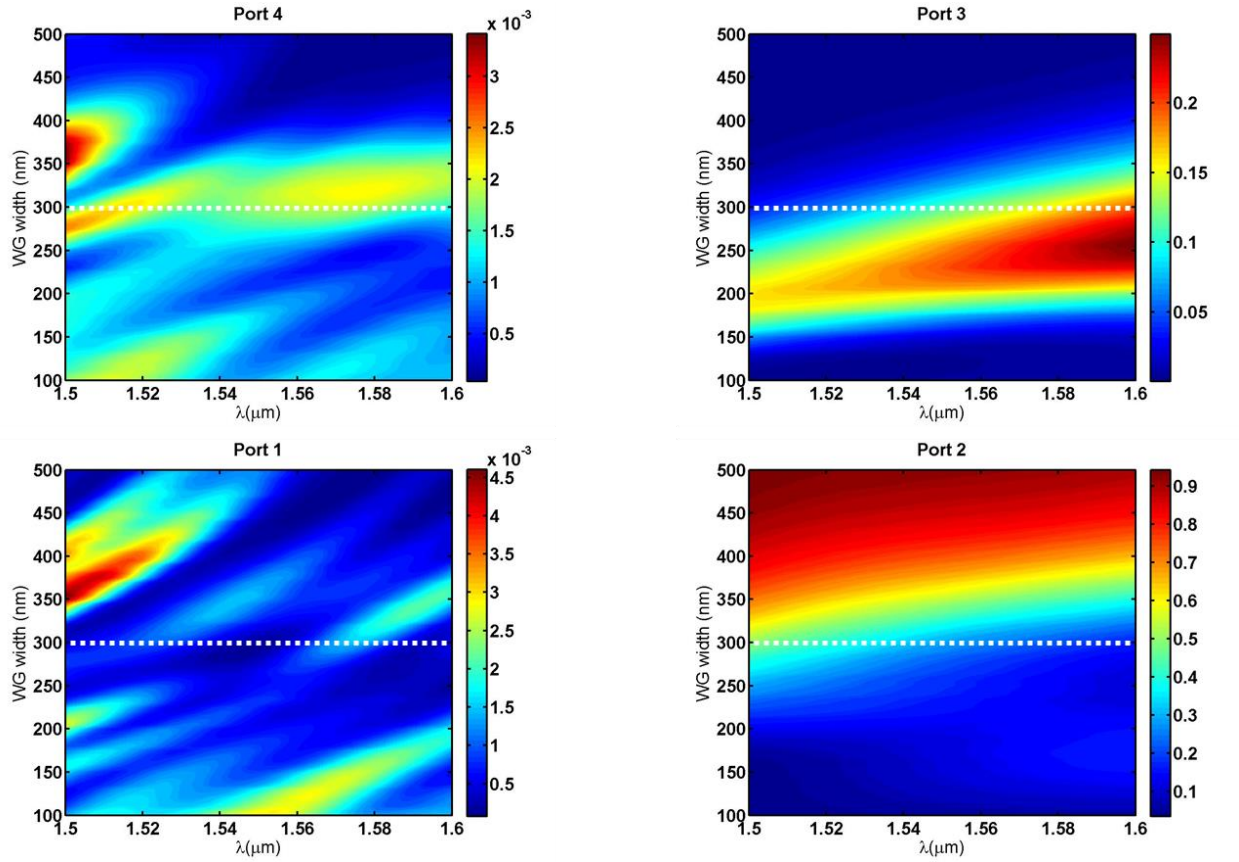


Figure 5.10 Parameter sweep of waveguide width versus lambda. The dashed white line corresponds to a waveguide width *w* of 300 nm.

The first parameter swept is the width of the Si waveguide. The recommended width for signal propagation is 400 nm (Table 5.1), which provides ~ 4- 5 dB/cm propagation loss. However, to couple light into the HCM structure, the waveguide mode needs to extend past the Si boundary. The HCM is designed to couple light from neighboring waveguides via evanescent coupling, hence a very narrow waveguide would provide a larger exponential decay arm into the structure. To achieve this, the width of the waveguide may be shrunk. The result is a trade-off between propagation loss and coupling efficiency.

In Figure 5.10, the dotted white line indicates a waveguide width of 300 nm, which is well above the resolution limit (180 nm) and the minimum fabrication line width (100 nm). It is also close the recommended coupling spacing (320 nm). We opt for 300 nm to allow more light to escape from the input waveguide, and to reduce the denominator value in the coupling efficiencies of P_3/P_2 and P_4/P_2.

5.3.2 HCM thickness parameter sweep

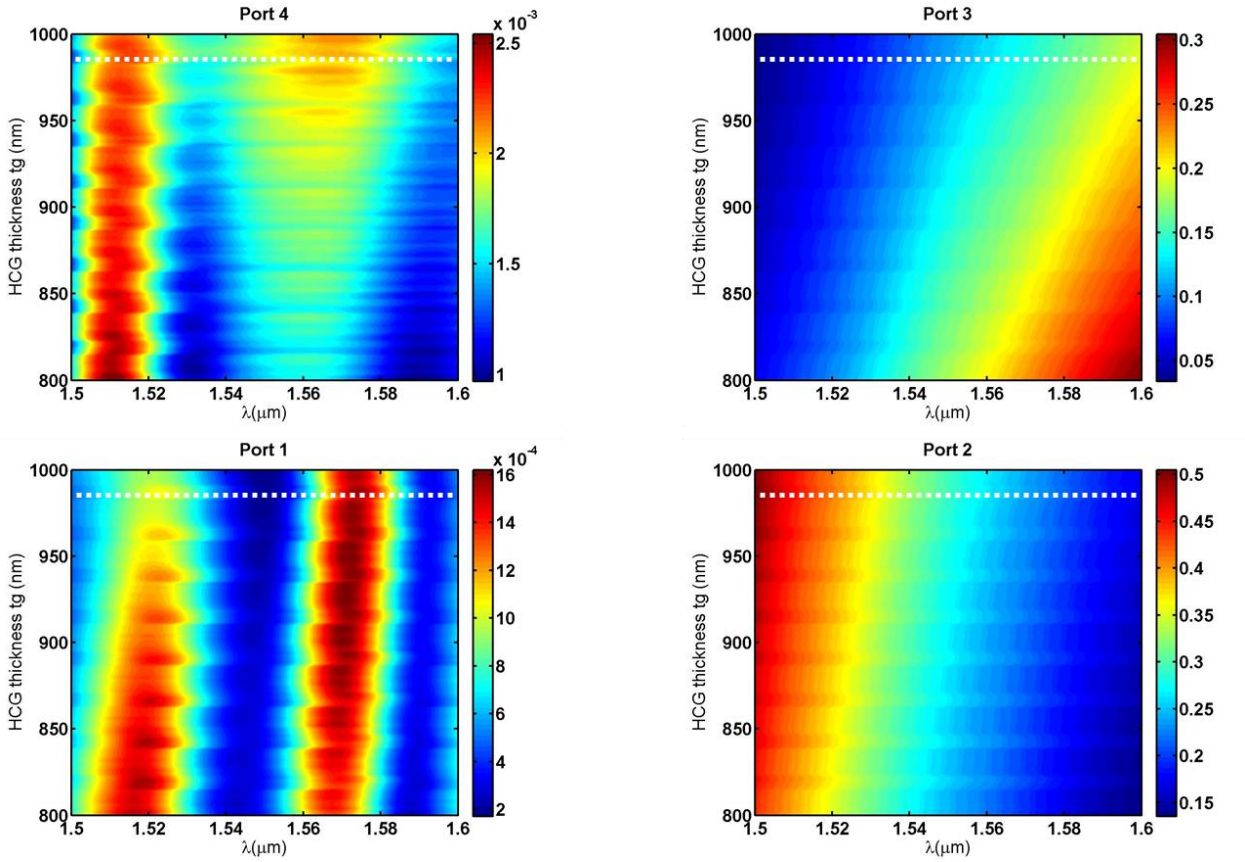


Figure 5.11 Parameter sweep of HCM thickness t_g versus lambda. The dashed white line corresponds to an HCM thickness t_g of 985 nm.

Next, we sweep the thickness t_g of the HCM. The thickness of the HCM is along the length in between the two waveguides. This parameter may account for any resonance build-up within the HCM, and thus the overall increase in coupling efficiency of the structure.

In this parameter sweep, shown above in Figure 5.11, however, a resonance effect is not found. From the plot for Port 2, the effect on coupling efficiency appears to be minimal, but there is a trend for more cross-coupling into Port 3 for smaller thicknesses at red wavelengths. The key is to pick a parameter with shows monotonic behavior versus wavelength. In this case, the initial guess using RCWA of 985 nm is suitable.

5.3.3 HCM period parameter sweep

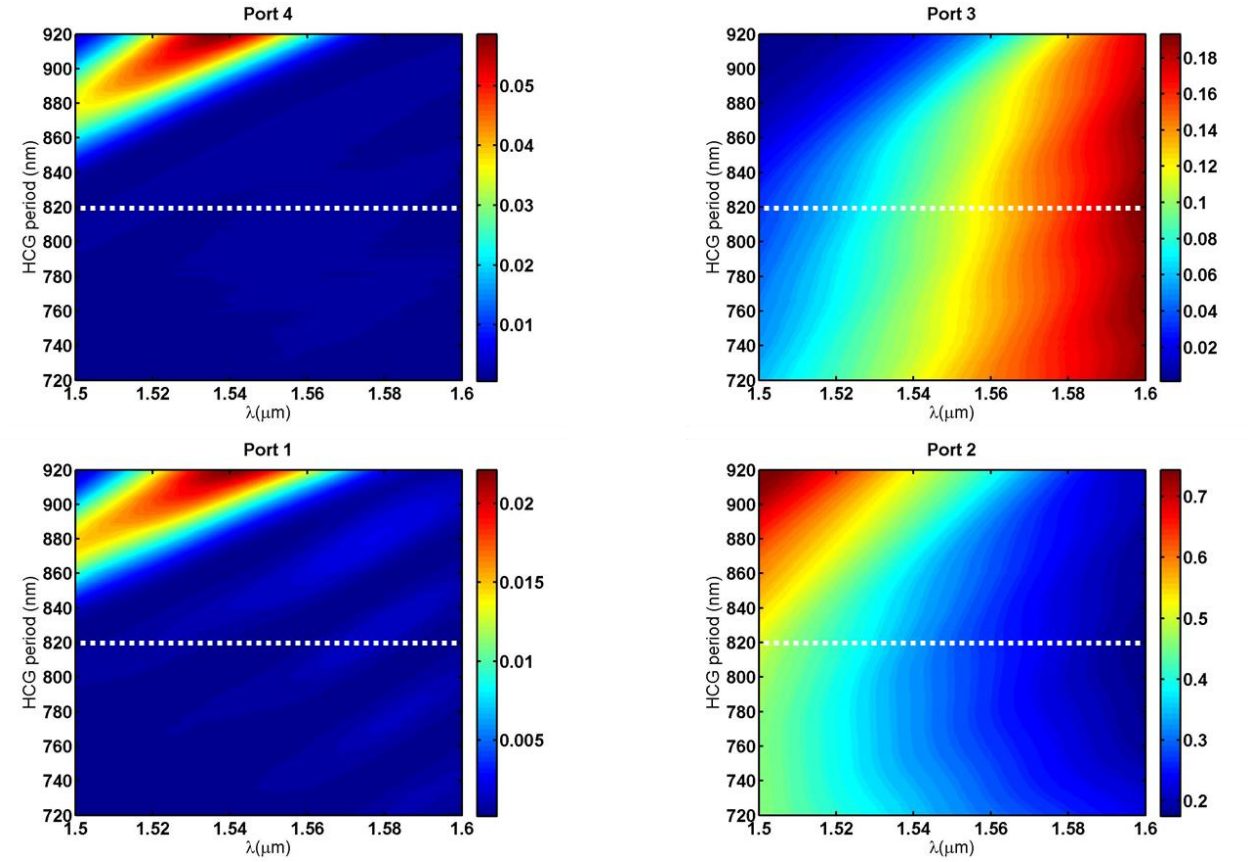


Figure 5.12 Parameter sweep of HCM period Λ versus lambda. The dashed white line corresponds to an HCM period Λ of 820 nm.

The period of the HCM bars will likely have the largest effect on the coupling efficiency of the structure. This can be ascertained by the scale of the color bar of Port 2 in Figure 5.12. The initial guess of 820 nm is near the gradient of the wavelength sweep, a desirable condition for the wavemeter design.

By increasing the period upwards of 900 nm, the coupling angle of the HCM is eventually changed *enough* to channel light up to Port 4, as predicted by Eq. (5.2) . The trade-off is that light is also reflected back into Port 1, the input channel. Albeit, it is a fraction of the light coupled into Port 4. We also hypothesize that by using a combination of chirped HCMs, we can couple light into both Port 3 *and* Port 4, to have a structure that can measure both power ratios simultaneously.

5.3.4 HCM bar width parameter sweep

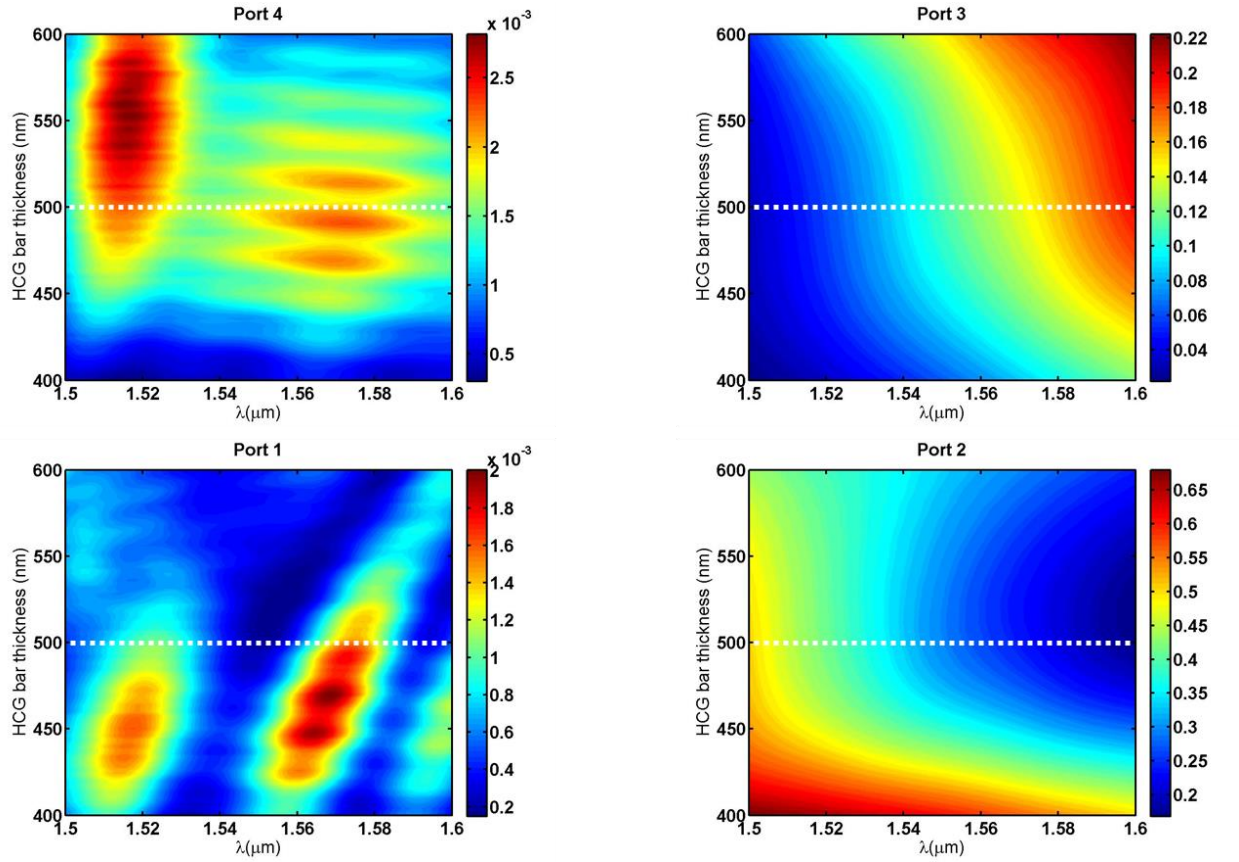


Figure 5.13 Parameter sweep of HCM bar width, *s*, versus lambda. The dashed white line corresponds to an HCM bar width *s* of 500 nm.

Lastly, we sweep the HCM bar width, or duty cycle of the periodic structure. This final parameter has a significant effect on the coupling efficiencies of the wavemeter. A bar width of 500 nm accounts for a 61.0% duty cycle (period of 820 nm), and lies near the gradient of both Port 2 and Port 3 coupling maps.

Interestingly, it also provides an additional knob to differentiate between back coupling to Port 4 and reflection to Port 1. By increasing the duty cycle of the HCM, the coupling into Port 4 can be increased, while simultaneously decrease reflection into the input port.

5.3.5 HCM designs

A selection of eight HCM designs were chosen for the photonics chip layout. The period, duty cycle, and number of bars were varied, as listed in Table 5.3.

Table 5.3. Selection of HCM Wavemeter Parameters

Design	Period (nm)	Bar Width (nm)	Duty Cycle (%)	Number of bars	Description
A	800	500	62.5	10	Preferential coupling to P_3
B	800	500	62.5	5	Same as A, fewer bars.
C	950	595	62.6	10	Preferential coupling to P_4
D	950	595	62.6	5	Same as D, fewer bars
E	800 950	500 595	62.5 62.6	5 5	Chirped period (B & D), each period has 5 bars.
F	800 950	500 595	62.5 62.6	10 10	Same as E, more bars.
G	800 950	500 475	62.5 48.1	5 5	Similar to E, different duty cycle.
H	800 950	500 475	62.5 48.1	10 10	Same as G, more bars.

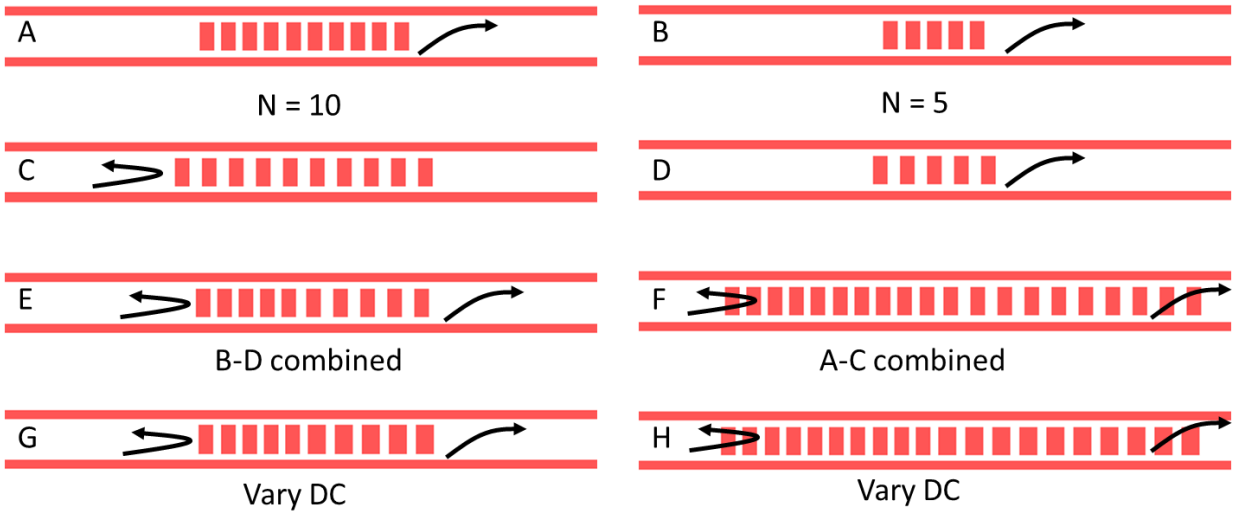


Figure 5.14 Summary of HCM wavemeter designs. Designs A and B have the same period and duty cycle, but different number of bars. Designs C and D have a larger period. Designs E and F have a chirped period while maintaining a constant duty cycle, and can be considered a combination of designs B-D, and A-C, respectively. Designs G and H employ a smaller duty cycle (48.1%).

Figure 5.15 (a) shows the top view of an FDTD simulation for Design A highlighting the electric field intensity within the structure. A TM polarized waveguide mode is sourced from Port 1 traveling down a 300 nm wide waveguide along the x-axis. Power monitors are placed at Port 2 (through-guide) and Port 3 (cross-coupling), whereas an electric field monitor is used to provide a cross-sectional slice of the structure. The electric field intensity image shows energy buildup in the grating structure, and coupled light traveling along Port 2.

The efficiency relative to the source mode is plotted in Figure 5.15 (b). The power measured at P_2 drops with longer wavelength, as the HCM increasingly extracts more light from the input channel, coupling it towards Port 3. The ratio of the powers at P_3 and P_2 is plotted Figure 5.15 (c). The monotonic behavior of the power ratio can be used to determine the wavelength of light incoming from P_1, independent from intensity.

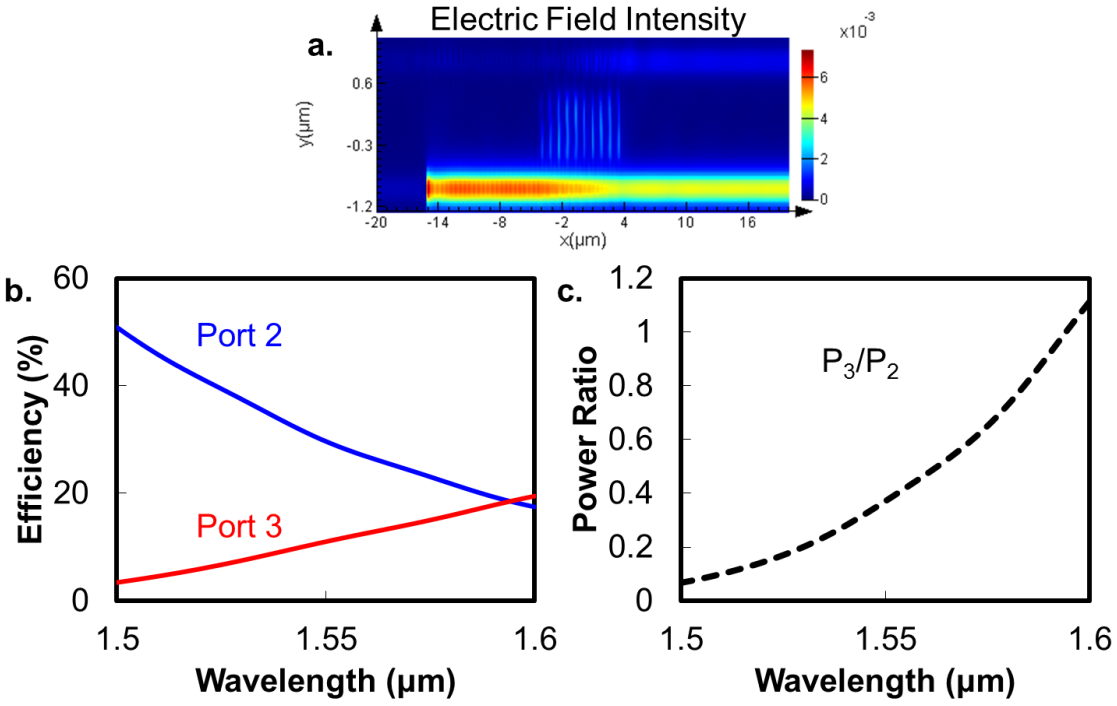


Figure 5.15 FDTD simulation of HCM wavemeter. (a) Top view of structure using an electric field intensity monitor at a single wavelength. (b) Power collected at P_2 and P_3 for a wavelength sweep from 1.5 to 1.6 μm. (c) Monotonic intensity-independent power ratio between ports 2 and 3.

5.4 Silicon Photonics Chip Design

The design area of the chip is 4.5 mm x 3.5 mm. The complete layout of the chip is shown in Figure 5.16. The chip is mirrored along the horizontal axis (top to bottom half), and has partial symmetry along the vertical axis (left to right). Edge coupling is performed at top and bottom of the chip, electrical pads are on the left and right edges of the chip.

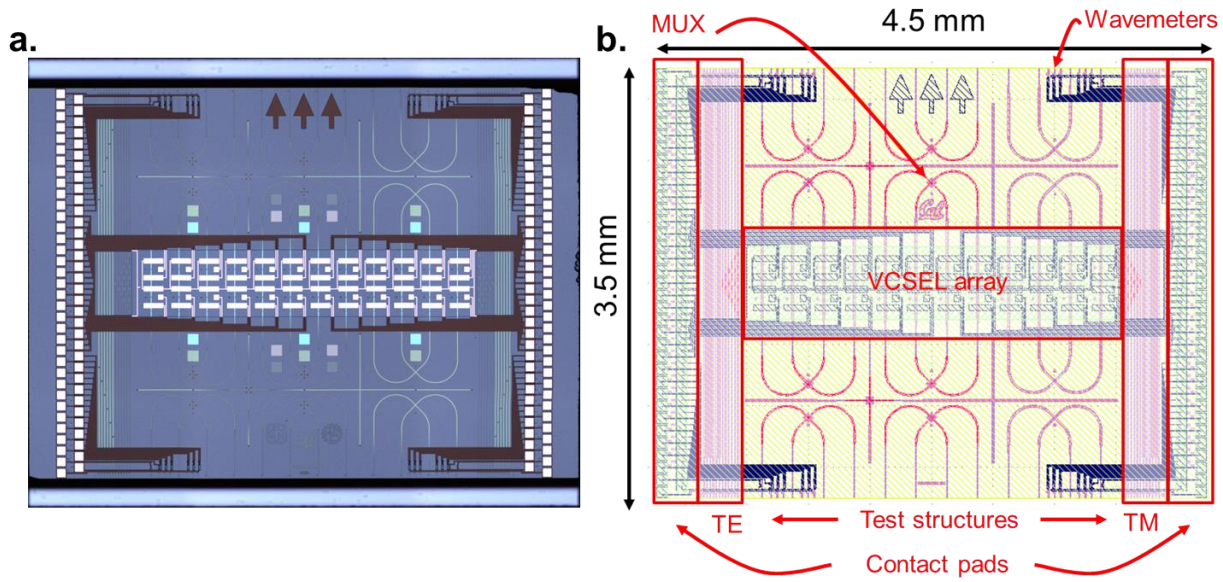


Figure 5.16 (a) Confocal image of silicon photonics chip. (b) Mask layout.

The chip features three kinds of optical I/O: the first are edge couplers using expanded mode waveguides, where a silicon strip waveguide width is reduced until the effective index of the traveling mode matches that of fiber. TE and TM versions of the edge coupler are included. In addition, a ~225 μm BOSCH etch trench is at the top and bottom edge of the chip to facilitate edge butt-coupling to fiber, shown in Figure 5.17. The second optical I/O is via surface-to-in-plane 2nd order grating couplers, and is used to launch light incident from a VCSEL, or from a fiber, into 10 μm silicon waveguides. The third is an output channel through a high contrast metastructure multiplexer (MUX), which employs 10 μm wide silicon nitride waveguides to evanescently interact with the output coupler. The latter is out of the scope of this dissertation and will be discussed in the dissertation of Li Zhu.

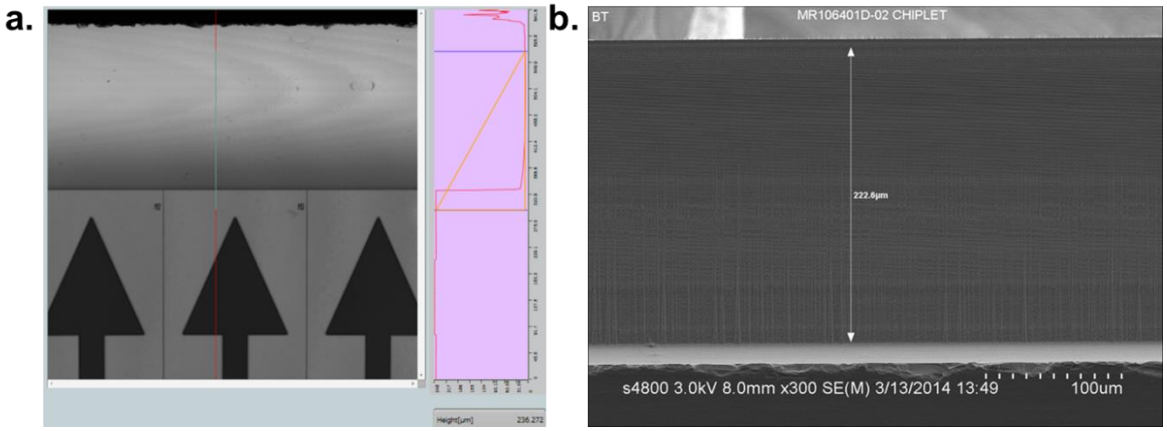


Figure 5.17 BOSCH trench. (a) Top view with confocal microscope. Measured depth is 236 μm. (b) Side view with SEM. Measured depth 223 μm.

Since this silicon photonic chip also has active components, electrical I/O is also possible. The chip features germanium photodiodes (Ge PDs) that are modified from the standard SNL library. Instead of having three contacts in a ground-signal-ground (GSG) template, one of the contacts is removed. This hinders the high speed operation of the detector, but saves valuable real estate on the chip close to the wavemeters. The Ge PDs are located near the four corners of the chip and have wires fanning out to the left and right contact pad arrays accordingly. Three Ge PDs are used per wavemeter. There are 8 wavemeter designs, each is repeated 3 times. Hence, there are 24 wavemeters, and 72 Ge PDs on chip. Some wavemeters have heaters in their vicinity, as shown in Figure 5.18. The heaters are made from doped silicon channels that affect nearby regions via resistive heating. Another active device is a Sandia design which uses vertical doping in silicon to control the absorption of a microdisk, acting as a high speed modulator. Only the outermost channels of the corner MUXes have these modulators.

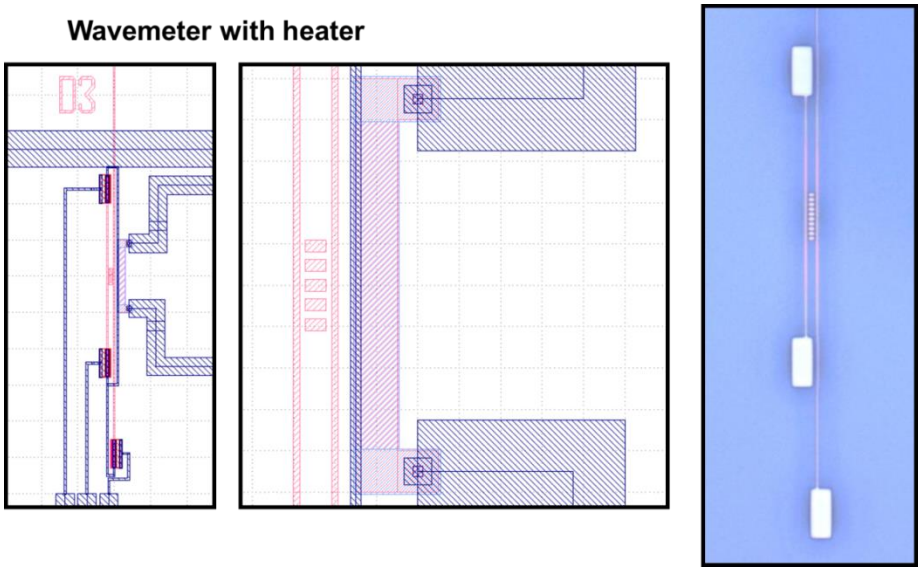


Figure 5.18 Wavemeter Design D with resistive heater in vicinity. The rightmost illustration is a confocal microscope image of the wavemeter at 100X magnification.

There are 3 different MUX designs, two of which employ silicon nitride waveguides and a full silicon etch (left and middle columns), and one which employs plain silicon waveguides and a shallow silicon etch. For the MUXes, there are two I/O formats: the first is edge coupling to MUX, all of which are near the top and bottom edges of the chip, and the second is vertical grating coupler to MUX, which occurs near the center of the chip. For the latter, there are two options. One, a set of straight waveguides feed light from fibers and grating couplers converging on a MUX, and two, a set of curved waveguides feed light from VCSELs and grating couplers towards a MUX.

Finally, a 24-VCSEL contact pad array is at the center of the chip. A window is etched into the field oxide of the chip to expose the contact pads. The contact pad scheme laser-ground-tune

(LGT) matches the tunable VCSEL design of Bandwidth10 high-speed devices, and is arranged in a 250 μm pitch. The ground pads for each VCSEL are combined into one contact pad to conserve real estate. The contact pad arrays have a 100 μm pitch in the vertical axis, and 160 μm in the horizontal axis. There is a 50 μm vertical displacement between the two columns. In total, there are 138 contact pads. Each pad is a metal square 88 μm x 88 μm, and has a 78 μm x 78 μm window for probing.

The single mode silicon waveguides are all strip waveguides with 400 nm widths, unless they are in the vicinity of a coupling region, in which case they are either 300 nm (for wavemeters), and 320 nm (for modulators). The tapers from the grating couplers are all 300 μm long.

5.5 Experimental Results

The chip is mounted on 3-axis NanoMax stage and imaged from an inclined angle with a visible-spectrum CCD and optical zoom lens system for alignment purposes. A lensed fiber is aligned and coupled to the expanded-mode edge coupler on the chip, residing on a 225 μm BOSCH deep trench shelf. A tunable laser is used to sweep the wavelength, and a manual fiber polarization controller is used to filter and couple TM polarized light into the silicon waveguides. Electrical probing of the germanium photodiodes is done with CuBe probes. Generated current is sent to a Keithley low voltage sourcemeter. The measured current can be converted to power using the responsivity specification provided by Sandia National Laboratories. For our purposes, we take the ratio of the raw currents generated for each wavelength. Figure 5.19 shows preliminary results for a wavemeter (design E).

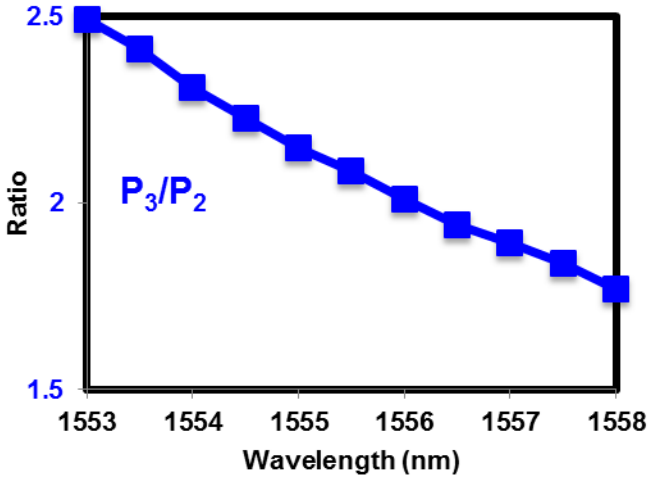


Figure 5.19 Measured power ratios between Port 3 and Port 2 for a wavelength window of 5 nm.

5.6 Summary

In this chapter, the basis for a compact chip-scale wavemeter compatible with silicon-on-insulator technology is described. The proposed structure employs standard silicon single mode waveguides, is sensitive to TM polarized light, and excluding photodetectors – has a footprint as small as 8 μm^2. The device is modeled using a traditional grating coupler for waveguides and the effective index method. Modeling of the dispersive behavior of the metastructure is performed using FDTD, where the parameter space of the periodic structure is thoroughly explored. The device prototype is manufactured through a Sandia National Laboratories silicon photonics active/passives process through a multi-university collaborative effort. The chip layout details are described. Lastly, the preliminary electrical properties of a wavemeter are presented for one of the 8 designs, and the results promised a 1:1 correspondence between wavelength and power ratios at detectors, which is necessary for identification of an unknown wavelength on chip.

Chapter 6

Conclusion

"Mountain is mountain, tree is tree.
Mountain is not mountain, tree is not tree.
Then you become Buddha:
mountain is mountain."

In this dissertation, three different types of novel HCMs on silicon are presented.

The first is a novel, low-loss, double heterostructure HCG hollow-core waveguide (HCW). The waveguide features a lateral confinement scheme that does not require sidewalls to maintain a well-defined lateral mode and can be monolithically integrated with flip-chip bonding, or by multi-stack processing of an SOI wafer. The design, simulation, and characterization of the HCG HCW were thoroughly reviewed. The propagation loss in a straight waveguide with a 9-μm waveguide height is measured to be 0.37 dB/cm, the lowest loss for a small core HCW.

Next, the pairwise integration of an HCG-based VCSEL with a silicon photonics chip was presented. The integration employs a thin AuSn eutectic solder for bonding pads and electrical interconnects, and uses a 500 x 500 μm^2 HCG VCSEL die placed with μm-accuracy with flip-chip technology on a silicon photonics passives chip. Grating couplers on the silicon photonics chip were used for vertical I/O into 500 nm-wide single-mode TE waveguides. Single mode operation of the VCSEL was observed before and after bonding. Capturing output light with an InGaAs CCD, the intensity at the output of the grating coupler is estimated to be ~ 40 μW using the backside of the VCSEL as a reference. The power ratios are calculated to be 12%, which leads to the I/O coupling efficiency to be estimated at ~ 10 dB.

Along a similar thread, an electrically pumped AlGaInAs-silicon hybrid VCSEL structure using a high contrast grating was described. The device exhibits CW power >1 mW and operation up to 65º C. Direct modulation of the VCSEL with small-signal bandwidth >2.5 GHz, and 5 Gb/s large-signal direct modulation was also realized with error free transmission over a 2.5 km fiber link. Employing the Si HCG as a MEMS electrostatic actuator, CW tuning across 0.32 nm is also reported. In an attempt to improve the thermal performance and power output of the device, an effort to develop an all-HCG VCSEL on SOI is also documented. Because the cavity of an all HCG can be as short as 3 μm, this can also provide gains in MEMS tuning efficiency and faster high-speed direct modulation. Future work will be aimed towards an HCG-VCSEL light source with coupling to silicon photonics waveguides.

Finally, an overview of the simulations and preliminary testing of a novel HCM structure that can function as an on-chip wavemeter were discussed. This compact device can provide the necessary feedback loop for wavelength control for high-data rate links without resorting to off – the-shelf instruments for wavelength characterization.

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