OMNI: A Distributed, Modular, Closed-Loop Neuromodulation Device for the Treatment of Neuropsychiatric Disorders

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by Ali Moin

Research Project

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Date

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Date

Abstract

OMNI: A Distributed, Modular, Closed-Loop Neuromodulation Device for the Treatment of Neuropsychiatric Disorders

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Neuromodulation methods have shown increasing promise to treat and cure neuropsychiatric disorders. This requires an active electronic device capable of modulating the brain system. However, existing "neurostimulators" have very limited capabilities and are not advancing as fast as the clinical research. They support small number and low density of neural data acquisition channels and stimulation sites. Moreover, a single region of the brain is often targeted. However, research shows that an effective therapy requires system-level modulation to force the brain to unlearn its dysfunction.

Octopus-Mimetic Neural Implant (OMNI) is a novel neuromodulation system which acts at the system level and provides real-time closed-loop therapy. It targets a wide range of neuropsychiatric disorders including Major Depressive Disorder (MDD) and Generalized Anxiety Disorder (GAD). OMNI's unique properties can be summarized by the following keywords: multi-scale, distributed, modular and self-contained. The system is a network of several neural implants performing simultaneous recording and stimulation from multiple sites, both cortical and subcortical, and in both hemispheres. It includes flexible and modular data aggregation, and contains sufficient computation power, storage and energy supply.

To achieve such a complex distributed system, definition of a complete custom network protocol stack is required as well as the hardware, software and firmware design for each module. In this thesis, we have designed and implemented the first prototype of OMNI device in collaboration with Cortera Neurotechnologies Inc. and Lawrence Livermore National Laboratory.

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Acknowledgments

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Finally, I would like to thank my parents for their infinite love and support throughout my undergraduate and graduate studies.

Chapter 1

Introduction

1.1 Neuromodulation

Psychiatric disorders are known as a prevalent class of diseases, with over a third of people in most countries reporting sufficient criteria to be diagnosed at some point in their life [1]. The World Health Organization (WHO) reported in 2001 that about 450 million people worldwide suffer from some form of mental disorder or brain condition, and that one in four people meet that criteria at some stage of their life [2].

Conventional treatments for neuropsychiatric disorders include counseling, physical therapy, pharmaceuticals and altering or augmenting tissue through surgery and injections. The growing field of neuromodulation is a new class of therapies that involves directly treating the nervous system itself, often through small implanted devices that target a specific area, to rebalance the activity of neural circuits and manage symptoms. Neuromodulation is defined as the alteration of nerve activity through the delivery of electrical stimulation or chemical agents to targeted sites of the body [3]. This method has much less negative side effects comparing to traditional pharmacological treatments.

A common example of neuromodulation treatment is the Deep Brain Stimulation (DBS) method which was approved by the FDA for essential tremor in 1997 and Parkinson's disease in 2002 (Figure 1.1) [4]. This method involves the implantation of a medical device called a neurostimulator (know as a 'brain pacemaker'), which sends electrical impulses, through implanted electrodes, to specific parts of the brain.

These neurostimulator devices have already been implanted in a considerable number of patients and evolved since their emergence. For instance, more than 100,000 patients worldwide have received Medtronic DBS therapy since 1997. Neuropace Responsive Neurostimulation (RNS) device is another example capable of epilepsy and seizure treatment by responsive direct brain stimulation (Figure 1.2) [5]. However, these devices still have very limited capabilities and there is a huge opportunity to improve them. They support very small number of electrodes (typically single-digit number of electrodes) which means poor amount of recorded neural signals and also limited access to different brain regions.

Figure 1.1: Medtronic DBS Therapy [4]

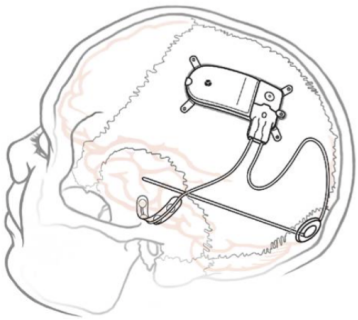

Figure 1.2: NeuroPace RNS Therapy [5]

1.2 Project Goal

As mentioned in previous section, neuromodulation methods have been used in treating a number of disorders including Parkinson's Disease (PD) and epilepsy. However, recent research has shown the efficacy of this methods in treating and even curing a wider range of neuropsychiatric disorders, including Post-traumatic stress disorder (PTSD) [6], Major Depressive Disorder (MDD) [7] and Generalized Anxiety Disorder (GAD) [8]. The underlying hypothesis is that because of the brain's plasticity, we might be able to force the brain to unlearn these dysfunctions by stimulating it in a closed-loop system. This might even lead to curing the neuropsychiatric disorder permanently and removal of the implanted device after the therapy period.

Although these results seem promising, the clinical research cannot lead to actual treatment in humans unless a novel advanced neural implant device exists. This device should have several unique features that are not found in current state-of-the-art neurostimulator devices:

- **Distributed**: The neurosurgeon should be able to reach every region of the brain

based on each disorder's characteristics. Therefore, it should support both cortical and sub-cortical electrode arrays with a large number of recording and stimulation channels.

- **Modular**: The architecture and physical placement of the device should be easily reconfigurable. This way the neurosurgeon can decide on the most effective configuration of implants for each individual patient based on their needs.

- **Intelligent**: The device should operate in a closed-loop fashion. This means it should record the neural signals, do some processing on them and perform stimulation based on that. Therefore, the stimulation is conducted in an adaptive way. This can be done by having on-board processing and storage capability on the implanted device.

- **Efficient**: Since the device is implanted, it should be extremely energy-efficient to have minimal need for battery recharging or wireless power transmission. However, this should not compromise the performance of the system in the above aspects.

We designed and implemented the OMNI device with having these key features in mind. It can be used by neuroscientists to do research in this area and ultimately - after going through the FDA approval - attempt to treat and cure the huge population affected with neuropsychiatric disorders.

Chapter 2

The OMNI Device

Octopus Mimetic Neural Implant (OMNI) consists of three main types of module (Figure 2.1). The Neuromodulator Modules (NMs) consist of high-density thin-film electrode arrays with tiny low-power chips placed right at the end of each array. They record the neural signals at each site and send them via cables to a central router in the skull called the Aggregator Module (AM). The AM serializes data from all NMs and sends it through a single cable to the main processor of the device called the Control Module (CM). The CM performs processing on the received data and decides on stimulation locations and parameters. It will then send the stimulation commands to the desired NMs through the AM path and NMs start stimulating those sites by generating electrical pulses.

We will now explain each module in more detail.

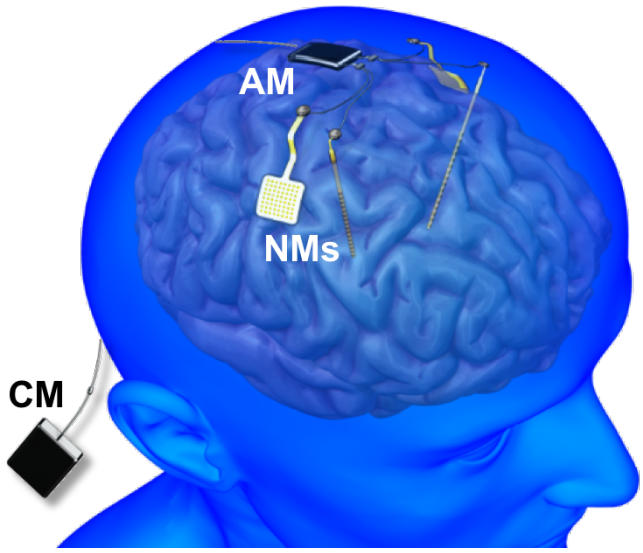

Figure 2.1: Octopus Mimetic Neural Implant (Image Courtesy of LLNL)

2.1 Neuromodulator Module (NM)

NM modules are the front-ends of the device. They are responsible for recording neural signals and also stimulating desired points of the brain. The device is designed to support up to 8 NMs while the current version supports up to 4. The NM consists of two main parts (Figure 2.2):

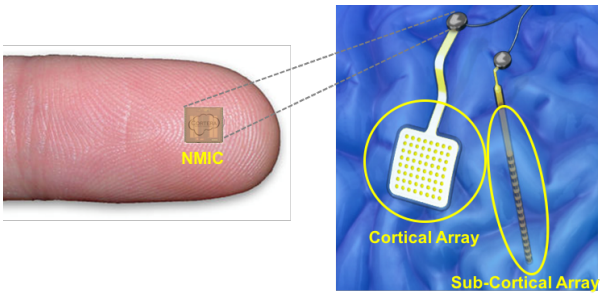

Figure 2.2: Neuromodulator Module Components

1. **Micro-Electrode Arrays**: Thin-film high-density micro-fabricated arrays of electrodes (Figure 2.2) are placed either on the surface of the brain cortex (cortical arrays) or penetrated into the brain tissue (sub-cortical arrays). Each array has 32 (phase 1 device) or 64 (phase 2 device) electrodes, and each electrode records the local field potential (LFP) of that site or pump current into that spot. As one of the collaborators in this project, Lawrence Livermore National Lab designs and fabricates the electrode arrays.

2. **Neuromodulator Module Integrated Circuit (NMIC)**: Each electrode array has a tiny ASIC packaged and attached to it (black packages in Figure 2.2). The fact that it is located right at the end of the electrode array helps in having no long analog signal routes which means lower artifacts and signal attenuation. The NMIC has the following roles:

   - Amplifying, filtering and converting 64 analog channels of neural signal into digital packets and sending it to the AM.
   - Performing electrical stimulation by pumping current into the brain tissue at a selected electrode with arbitrary pattern. Each NM has 4 stimulation units which can be connected to any of the 64 electrodes and rapidly reconfigured.
   - Enabling simultaneous low-noise recording with high-voltage stimulation (up to $\pm 12\,\mathrm{V}$) by canceling stimulation artifacts
   - Integrated impedance measurement unit

Table 2.1: Overview of NMIC Specifications and Features

# of Rec. and Stim Channels	64
# of Stimulation Units	4
Impedance Measurement	Up to 64 channels simultaneously
Rec. Subsystem Power	500 µW
Max Stim Current	5 mA

Table 2.1 shows an overview of Cortera's NMIC specifications and features. The NMIC interposer PCB and package are illustrated in Figure 2.3.

As one of the collaborators in this project, the NMIC is designed by Cortera Neurotechnologies Inc..

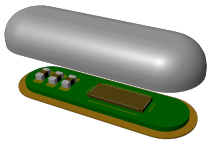

Figure 2.3: NMIC Interposer and Package (Image Courtesy of Cortera Inc.)

2.2 Aggregator Module (AM)

The OMNI device is the first network of neural implants. NMs resemble the end-points or clients of the network and the CM acts as the server. In this analogy, the AM is the central hub or router in a star topology to which all other modules are connected. The main roles of the AM are as follows:

- **Enabling a single cable from the skull to the chest**: As mentioned before, the main processing unit of the device is the CM and all of the NMs should be connected to that. Having a separate subcutaneous cable to connect each NM to the CM is not a viable option. The cables are routed subcutaneously and obviously having minimal length is preferred. Therefore, NMs are first routed with a relatively short cable (10cm) to the AM located in the center of the skull. The AM merges all the packets and sends them out to the CM via a single long cable from the skull to the chest (50cm).

- **Having safety power switches**: The CM includes the battery and sources the electric power to all other implants. The power is routed from there to the NMs through the AM. If for any reason something goes wrong and one of the NMs starts malfunctioning, we should be able to shut it down completely. This is crucial for the safety of

the device and from the regulatory perspective. For instance, imagine that the NMIC breaks and it starts pumping huge amount of current into the brain tissue constantly. In that case, the digital circuitry might also be broken and it cannot decode the chip reset or turn off command from the CM. The only solution would be disconnecting the chip voltage supply. Therefore, for each NM there is a power switch on the AM which is controlled by the digital logic on the AM. So in the case of failure, the CM asks the AM to shut off the power for the failed NM.

Aggregator Module Hardware Design

The AM electronics for the phase 1 device are designed and implemented from off-the-shelf discrete components. Phase 1 AM supports up to four NMs and the Phase 2 device is planned to have an ASIC supporting up to eight NMs.

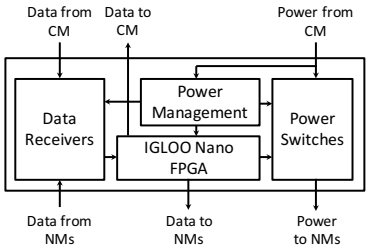

Figure 2.4: Aggregator Module Block Diagram

Figure 2.4 shows the Aggregator Module block diagram and Figure 2.5 shows its fabricated PCB. An Igloo low-power FPGA is responsible for the digital protocol logic and IO handling. Based on the medical implant regulations, the implanted cables should carry zero DC component in order to prevent body tissue damage. Therefore, the power is distributed as AC and all signal links are AC-coupled at both ends. As a result, there is a full-wave bridge rectifier and a DC-DC converter on the AM PCB to supply the board with required 1.2V. Also, since the received signals are single-ended and AC-coupled, there is a cross-coupled inverter pair as the receiver for each signal (Figure 2.6).

2.3 Control Module (CM)

CM is the main brain of the device which does all the computation and signal processing. Figure 2.7 shows front and back view of its PCB. It includes the following sub-modules:

- Processor:

  A microcontroller SoC (Microsemi SmartFusion2) which consists of an FPGA fabric, ARM Cortex M3 core and number of different digital blocks is used on CM. The fabric is the interface with the AM and the ARM core does the processing. It can

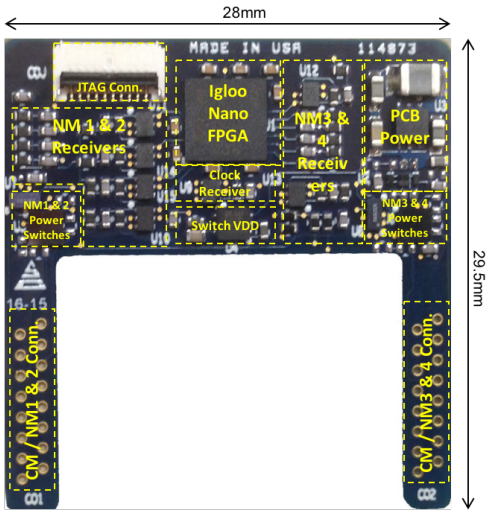

Figure 2.5: Aggregator Module PCB

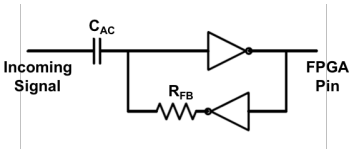

Figure 2.6: AM Data Receivers

support closed-loop control algorithms such as MPC and PCA. The SoC is completely programmable and reconfigurable. Therefore, as the project goes forward and the clinical team discovers new approaches, the device can be reprogrammed and updated based on that.

- Data Storage Unit:

  An 8Gb flash memory is placed on the CM board for saving neural data on board locally.

- Wireless Telemetry Unit:

  This unit streams out data to the graphical user interface (GUI) software on the PC and also receive commands from the PC. A commercial 2.4GHz Nordic radio (nRF51822) is used for this phase of the device which can handle up to 2Mbps bandwidth.

- Battery and Power Circuitry:

  The energy source of the whole device is located in the CM package and the power is distributed from there through cables. We are using a 600mAh Li-ion battery. One of the main reasons of having the CM implanted in chest is that the battery is a

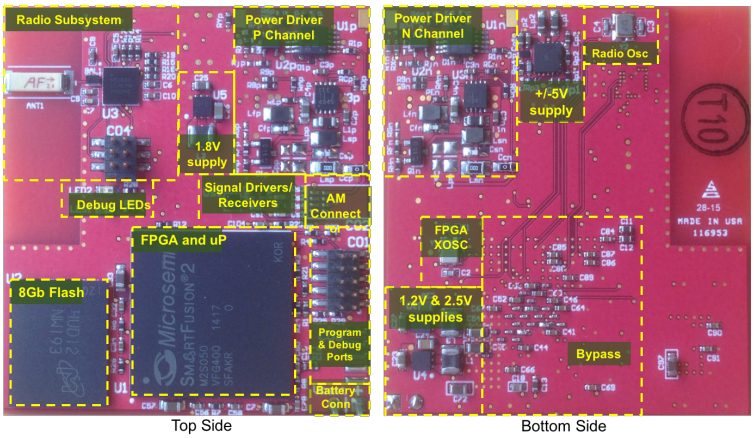

Figure 2.7: Control Module PCB

bulky element and having that in the chest similar to a cardiac pacemaker is much more convenient for a chronic treatment in which the patient should always carry the device.

The CM is DC powered from the battery; however, it is distributed as AC to all other modules. So there are two power drivers on the CM that generate 20MHz sinusoidal waves with 180°phase difference. These differential AC voltages will then be converted in the AM and each NM to DC voltage and fed to the modules.

The CM electronics for the phase 1 device are designed and implemented from off-the-shelf discrete components (Figure 2.8); the CM will be outside of the body for the first phase. However, the Phase 2 device will be hermetically sealed and packaged in metal case by Lawrence Livermore National Lab.

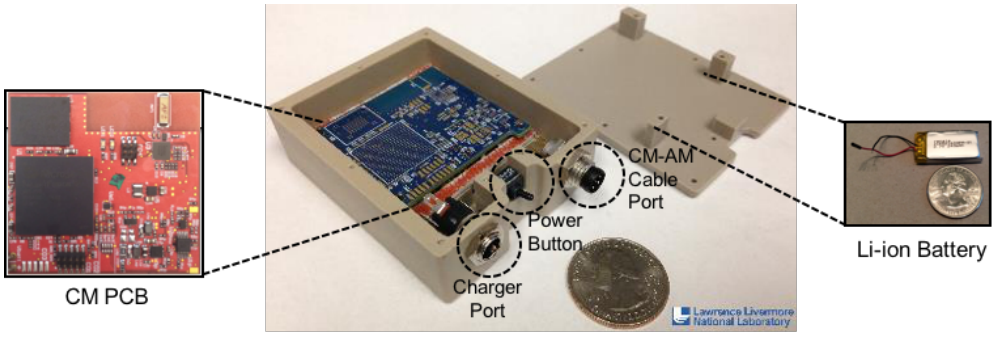

Figure 2.8: Control Module First Prototype (Image Courtesy of LLNL)

Chapter 3

Data and Power Distribution Networks

As mentioned before, OMNI is a network of several modules around the body which are connected together via cables. The physical design and structure of the cables will be discussed in this chapter as well as the higher levels of the communication interface and power transfer between modules.

The interface being used in CM-AM and AM-NM links consists of two differential power wires, three data signal wires and one common wire. Each category will be discussed below.

3.1 Power Distribution Network

Figure 3.1 shows the block diagram of the Control Module power network. It is supplied by a 3.7V Li-ion battery which is then regulated to 1.8V for the CPU, radio and memory and 3.3V for AC power drivers.

As mentioned before, there cannot be any DC power transfer in the implantable medical devices, since it can cause tissue damage. So the power wires in the cables carry sinusoidal currents. There are two Class-E power amplifier circuits in the CM, each of which generating 20MHz 3.3Vpp sinusoidal voltages with 180°phase shift. The drivers are designed in a feedback loop to be adaptively tuned based on the variable load of the whole system (AM and NMs).

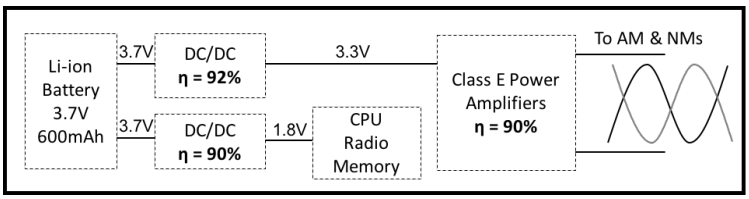

Figure 3.1: CM Power Network

The plan for the final device is to have it recharged wirelessly. However, since the current version of CM is external to the body, the battery can be charged with a wired charger. Table 3.1 shows the specifications of the battery.

Table 3.1: Battery Specifications

Model	Renata ICP622540 Rechargeable Li-ion polymer
Dimensions	42.5 x 25.7 x 6.5 mm
Weight	11g
Nominal voltage	3.7V
Nominal capacity	600mAh
Charging characteristics	300mA nominal charging current, 2-3 hours charge time (depends on precise charge current and depth of discharge)
Lifespan	>500 cycles charge/discharge

Figure 3.2 shows the Aggregator Module power network. The AC power is rectified through a full-wave bridge rectifier and stepped down to 1.2VDC to be used by the Igloo FPGA and the receivers. It also goes to the power switches in a separate parallel path. As mentioned before, these switches are controlled by the CM and shut the power of the malfunctioning NM down in the potential case of failure.

The AC power is a synchronous signal which is routed to all modules of the network. Therefore, we decided to use it as the synchronous clock as well. So each module recovers its internal clock from the power wire. Since the maximum data-rate is chosen to be 20MHz (based on the neural signal sampling rate of NMs and the total required data rate for streaming all channels), the AC power frequency is defined to be 20MHz as well.

3.2 Data Communication Network

The data transfer protocol is defined in two layers: Frames and Packets. Each frame includes a single bit from each NM and a meaningful combination of these bits forms a data packet.

Data Frame

The data transfer is based on time multiplexing the data from/to each NM to/from the CM. The data rate in CM-AM link is 20MHz, we have divided it into 10 time slots (each with 2MHz bandwidth) and allocate each time slot to one NM. The two extra time slots are used as pilot signal for synchronization and some low-level controls such as reset. Therefore, data rate from/to each NM is 2MHz (Figure 3.3). Each 10 time-slots is called one frame.

There are two signals between modules: valid and data

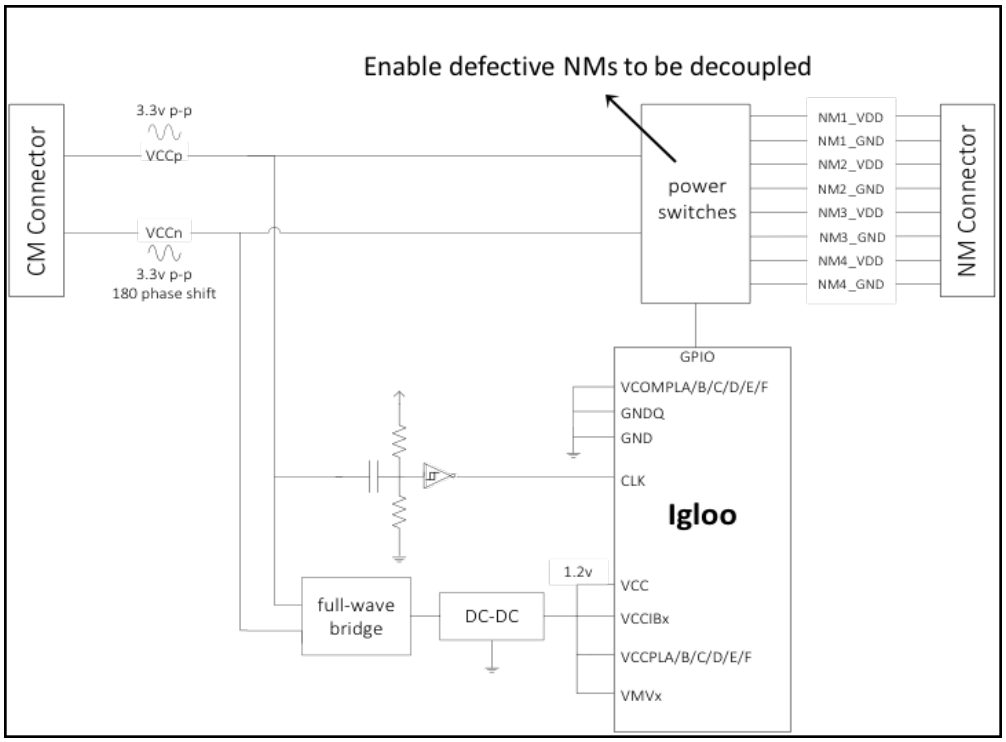

Figure 3.2: AM Power Network

When there is data available for a time-slot, the valid signal is set to high during that time-slot and the data signal shows the actual bit value for that. Therefore, the receiver picks up the data whenever the corresponding valid is high. Note that the signals are updated on the clock rising edge and sampled on the falling edge.

Each module has an internal counter for data communication. These counters should be synched for each module relative to others. This way, CM and AM would know when to put which bit on the link.

Table 3.2 shows different cases for the first two time-slots (pilot and reset-type). The pilot is being used to detect the start of the frame in receiver. Resetting AM and NMs is also implemented in this lowest layer of protocol because when a reset is needed, the packet decoder unit might not be functional and not be able to decode the reset command. Also the safety power switches that shut off the power to NMs in case of failure are being controlled in this layer of the protocol. The reset-type bit is responsible for these cases.

Data Packets:

Data packets are the main units of actual neural data or commands which are being sent from CM to a specific NM or in the opposite direction. Each packet is then transmitted bit by bit through the frames. In other words, a group of data frames will form a data packet.

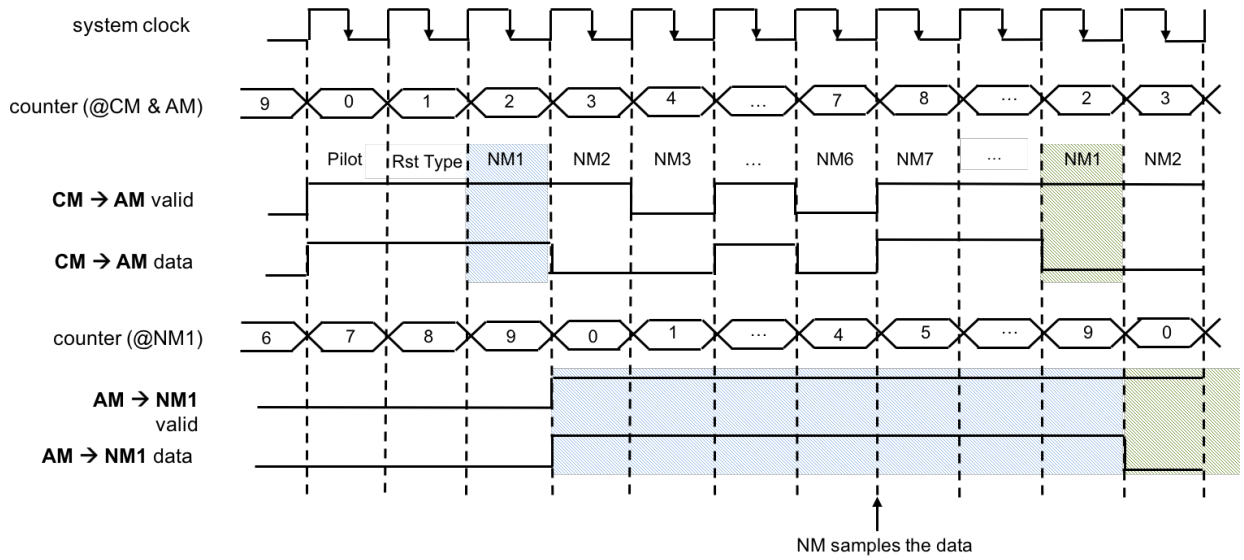

Figure 3.3: Digital Protocol

Table 3.2: Frame Format Special Commands

	Sending to NM1			**Resetting AM**			**Resetting NM1**			**NM1 ON/OFF**		
	Plt	Rst	NM1	Plt	Rst	NM1	Plt	Rst	NM1	Plt	Rst	NM1
valid	1	1	1	1	1	x	1	1	1	1	0	1
data	1	1	0/1	0	1	x	0	0	x	0	0	1/0

Different packet structures will be discussed below:

CM to NM Packets

There are two types of packets in this direction:

- **Command Packet**: CM is the controlling unit and therefore it should send control commands to NM. These commands include starting stimulation, starting impedance measurement and so on (Table 3.3).

Table 3.3: CM to NM Command Packet

Field:	**TYPE_IND**	**CMD**	**CRC5**
Size (Bits):	1	10	5
Description:	Type Indicator: 1 = command 0 = reg op	Command	CRC Poly: $x^5 + x^2 + 1$ Initial all 1s

- **Register Operation Packet**: There are bunch of registers on the NMIC including status registers which contain the current state of the chip and control registers that control the function of the chip. Reg-Op packets can read or write the register value in a specified address (Table 3.4) .

Table 3.4: CM to NM Register Operation Packet

Field:	**TYPE_IND**	**RW**	**ADDR**	**DATA**	**CRC5**
Size (Bits):	1	1	16	16	5
Description:	Type Indicator: 1 = command 0 = reg op	Read/Write: 1 = write 0 = read	Register Address	Register Data Don't care for read op	CRC Poly: $x^5 + x^2 + 1$ Initial all 1s

Both packet types have a 5-bit CRC poly that is used for error detection.

NM to CM Packets

There are two types of packets in this direction:

- **Register Read-Back Packet**: NM sends back the address and contents of the register that CM has asked for (Table 3.5).

Table 3.5: NM to CM Register Read-Back Packet

Field:	**START**	**TYPE_IND**	**ALARM**	**CRC_ERR**	**REG_ADDR**	**REG_DATA**	**CRC8**
Size (Bits):	5	1	1	1	16	16	8
Description:	Start Sequence: Always 10101	Type Indicator: 1 = data 0 = reg. read	Alarm Flag: 1 = alarm 0 = no alarm	CRC Error Flag 1 = CRC error occurred 0 = all OK since last indication	Register Address	Register Data	CRC Poly: $x^8 + x^6 + x^3 + x^2 + 1$ Initial 0xFF

- **Neural Data Packet**: This packet contains a single sample from all 64 channels of the NM. Therefore, the Data Block length would be 64 channels $\times$ 16 bit/channel = 1024 bits (Table 3.6).

Table 3.6: NM to CM Neural Data Packet

Field:	**START**	**TYPE_IND**	**ALARM**	**CRC_ERR**	**DATA**	**CRC8**
Size (Bits):	5	1	1	1	1024	8
Description:	Start Sequence: Always 10101	Type Indicator: 1 = data 0 = reg. read	Alarm Flag: 1 = alarm 0 = no alarm	CRC Error Flag 1 = CRC error occurred 0 = all OK since last indication	Data Block 64 channels $\times$ 16 bit/channel	CRC Poly: $x^8 + x^6 + x^3 + x^2 + 1$ Initial 0xFF

Both packet types have a 5-bit start sequence for the receiver to detect its start (10101 pattern) and an 8-bit CRC poly for error detection. CRC_ERR flag shows an error in the

CRC of the latest received packet, so CM can resend that packet. ALARM flag will also go high to indicate any error on the NM side. ALARM will stay high until the CM manually resets it to zero.

Common Wire

The initial plan was to have the valid and data wires in both directions. Therefore, the cable bundle was designed to be 6 wires (2 powers and 4 signals). LLNL designed and locked down the cable connector design accordingly. However, after the design became more mature and we further analyzed the whole power and data transfer network, it turned out a return path for the signals and power is needed. This wire is basically a common wire or ground point of the whole system. Since the 6-wire interface was locked down, we needed to replace one of the existing signals with the common wire (Figure 3.4).

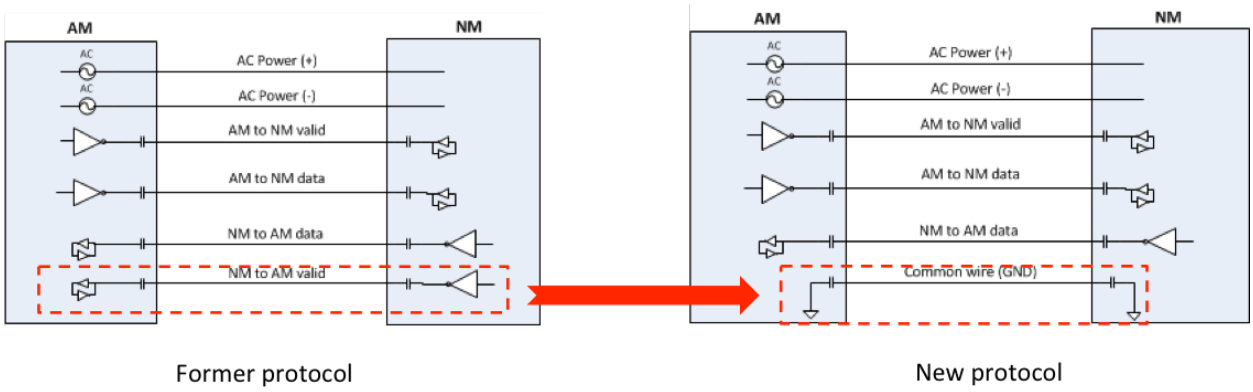

Figure 3.4: Changing n2c_valid Signal with Common (Ground) Wire

We realized the valid signal in NM→AM→CM (n2c) direction can be a good candidate. We are using the pilot and reset-type time-slots for either synchronizing or resetting modules which is in CM→AM→NM (c2n) direction in both cases. The only reason for initially having them in n2c direction was to determine the start of the frame. In order to solve that, we added a fixed 5-bit sequence to the start of the n2c packets for the CM receiver to detect the start of packet.

Receivers Initialization

Figure 3.5 shows the typical data transfer link used in OMNI. Since the links are AC-coupled, cross-coupled inverter pair should be used to detect and receive the signals at the receive side. However, the initial state of this inverter pair is not guaranteed to be in agreement with the transmitter.

Figure 3.6 is one example of this failure case. The Tx is initially low but the Rx is high. After a low-to-high transition on Tx, the Rx point goes higher than V_{DD}. If the next

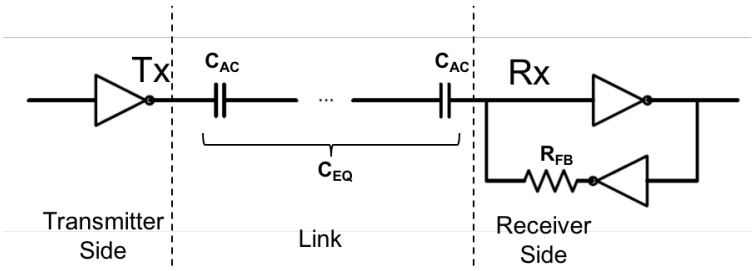

Figure 3.5: Data Transfer Link

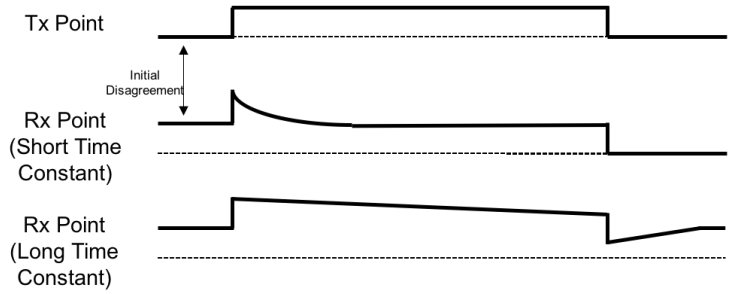

Figure 3.6: Cross-Coupled Inverter Pair Initialization

high-to-low transition happens immediately after that, the Rx point voltage would go back to V_{DD} and effectively nothing is sensed at the receive side module. However, if the Tx stays high long enough, the Rx would be settled down to V_{DD} value (second row in Figure 3.6) and Tx and Rx will be in agreement after that. Note that the feedback resistor value should be chosen appropriately, otherwise the Rx might never settle down due to very long time constant (third row in Figure 3.6).

This initialization is done by the AM and CM during the system start up. For instance, AM sends a long sequence of all-zeros followed by all-ones to CM and that initializes the receivers on the CM.

3.3 Cabling and Interconnect

Two types of cables connect the modules together:

1. a longer 50cm cable connecting CM (implanted in chest) to AM (implanted in skull)
2. shorter 10cm cables connecting AM to the NMs

The cable thickness is limited due to being subcutaneously implanted. Therefore, the individual wires are close to each other and that will cause cross-talk. Also when they are implanted, they will be surrounded by body environment which is similar to saline. It

means we should design the cable keeping in mind as it is soaked in a conducting solution. Mechanical stability and sustainability should also be observed in our design.

LLNL is in charge of the cable fabrication. Their original plan was to have custom micro-fabricated cables. However, this proved to be infeasible and they switched to regular cables. Since this had a huge impact on the system from the electrical design standpoint, we performed excessive simulation and study on the cable design. This process took a long time and we tried several cable architectures and geometries. They will be discussed in the rest of this chapter:

Design #1: Bundle of Multiple Parallel Wires

The initial proposed design by LLNL was a bundle of 7 individually insulated wires (Figure 3.7). The 6 planetary wires were supposed to be connected to the 6 required signals and powers. The central one is responsible for mechanical stability.

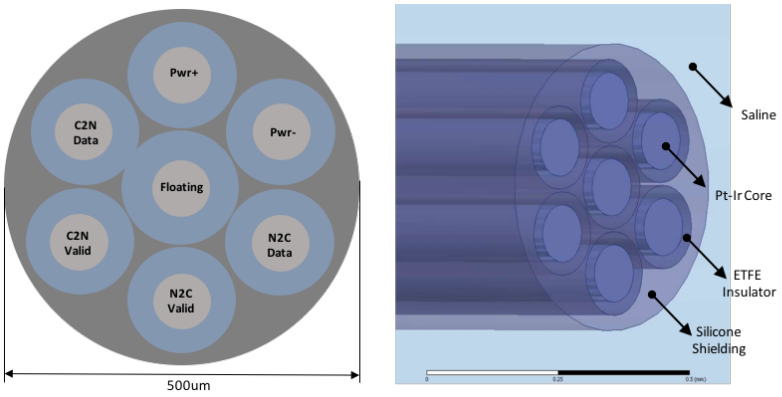

Figure 3.7: Cable Design #1 HFSS Model Cross Section and Signal Assignments

We performed electromagnetic FEM simulation to find the cable electrical characteristics and imported the results into circuit level simulator. It turned out that this design is not a feasible option because of the high cross-talk from the following main sources:

- Zero spacing between adjacent wires
- No ground shielding between wires
- Asymmetric structure causing parasitics mismatch

These issues will be discussed along with the governing equations in Section 3.3.

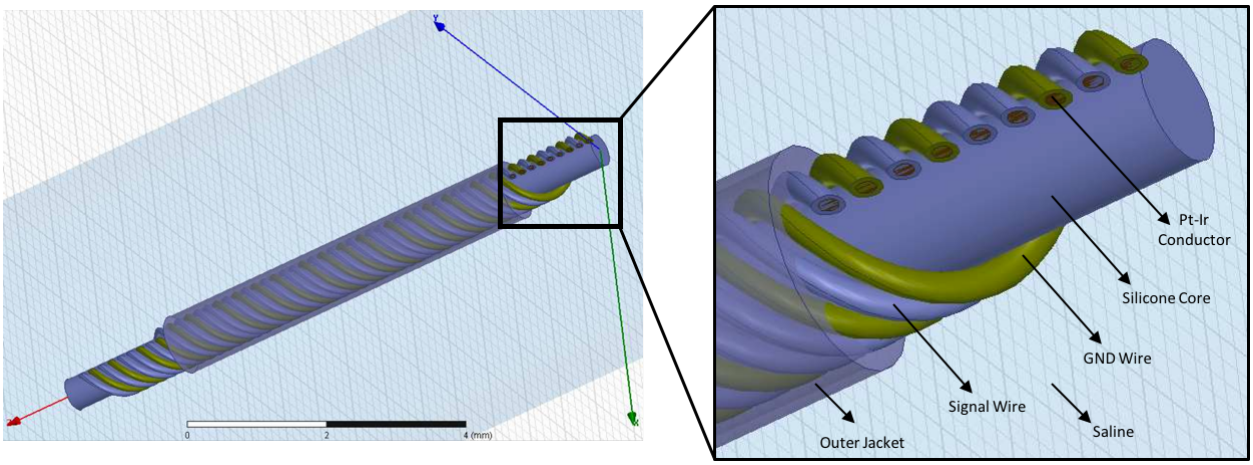

Figure 3.8: Cable Design #2 HFSS Model Cross Section

Design #2: Multi-Filar Coiled Cable

In order to solve the problems with the initial design and based on our feedback, LLNL offered another geometry for the cables. In this design, there is a central silicone core and the insulated wires are coiled around that (Figure 3.8).

We decided to increase the number of wires from 6 to 9. The additional wires are used as ground shielding between the data signals and also between data and power lines. We also increased the pitch of the wires from 9 wires to 27 wires. This means having spacing equal to 2 wires between adjacent wires. The extra space helps in reducing the coupling capacitance. Note that the two power wires are next to each other and there is no ground shielding between them. This way, the electric fields caused by them will cancel out and the net effect of power wires on a data wire would be minimized.

Figure 3.9 shows the HFSS simulation result for the cable parasitic capacitance as a function of cable length for the two cases of ETFE and Polyurethane outer jacket material. The complex geometry of this design caused long simulator run-times to form the mesh and solve the EM equations. Therefore, the simulation is done for a very small piece of the cable and then extrapolated for the full length.

Figure 3.10 shows the cable prototype and its test boards. The test PCBs are designed to solder the cable conductors to it since the conductor's diameter is just 25 µm and it is not possible to clamp it to the measurement equipment. The test setup is then connected to a VNA and the S-parameters are extracted. The approximate capacitance values are then extracted by looking at the imaginary part of the Z-matrix converted from the S-matrix.

The simulation results as well as the measured values looked promising and this design met our system electrical specifications.

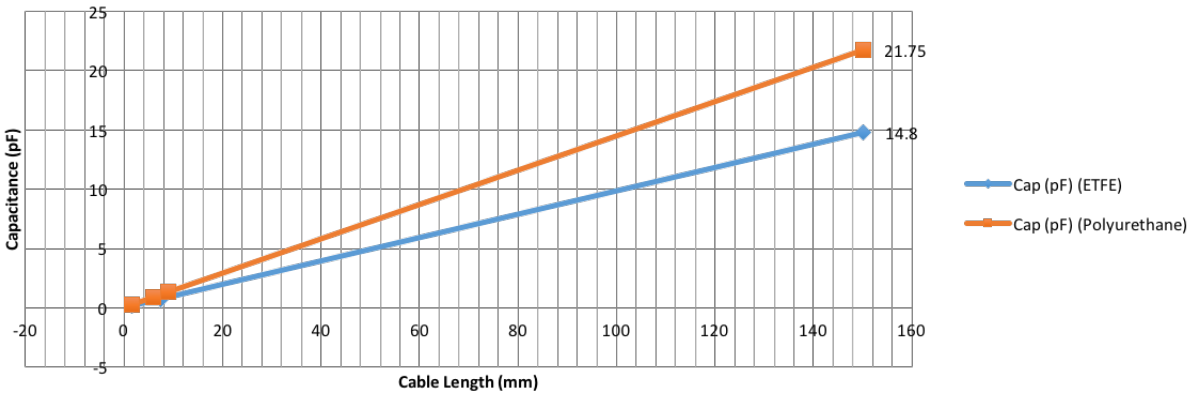

Figure 3.9: Cable Design #2 Parasitic Capacitance vs. Length from HFSS Simulation

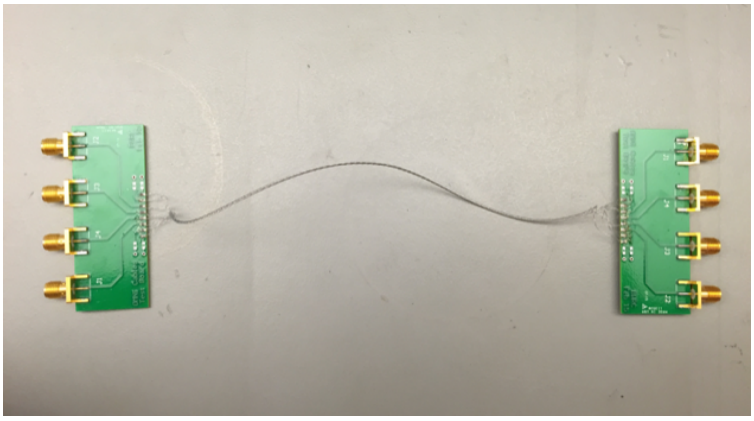

Figure 3.10: Cable Design #2 Sample

Design #3: Straight Multi-Lumen Cable

Although the previous design met the electrical requirements, it turned out its manufacturing is too expensive and also poses risks from the mechanical design perspective. The final alternative proposed cable geometry is a multi-lumen Polyurethane jacket which has a twisted pair in the central lumen and 6 planetary wires in the 6 straight lumens around the central lumen (Figure 3.11).

The positive and negative power twisted pair helps in canceling the cross-talk effect from high-voltage sinusoidal power signal to lower voltage more sensitive data signals. Also being in the center minimizes the cap mismatch between each power to any of data wires. The three data wires are slid into the planetary lumens with a ground shielding wire between each two.

Figure 3.12 shows the measurement setup for this design. We used an LRC meter this

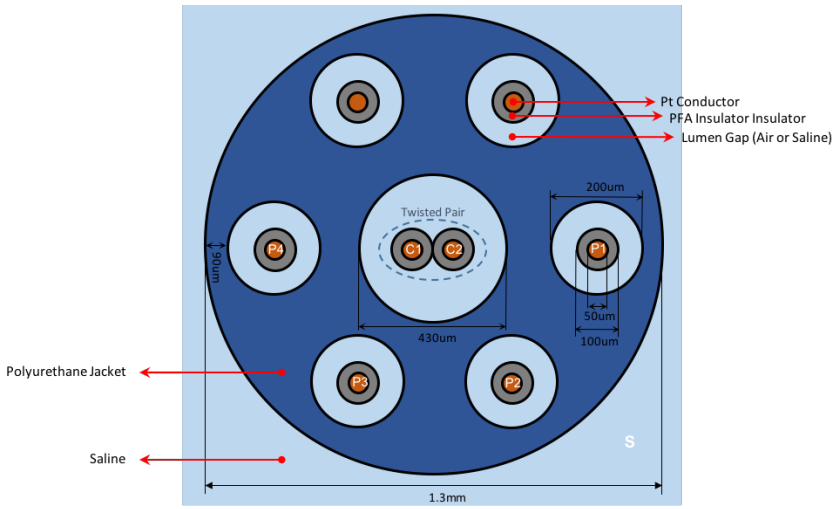

Figure 3.11: Cable Design #3 Cross Section

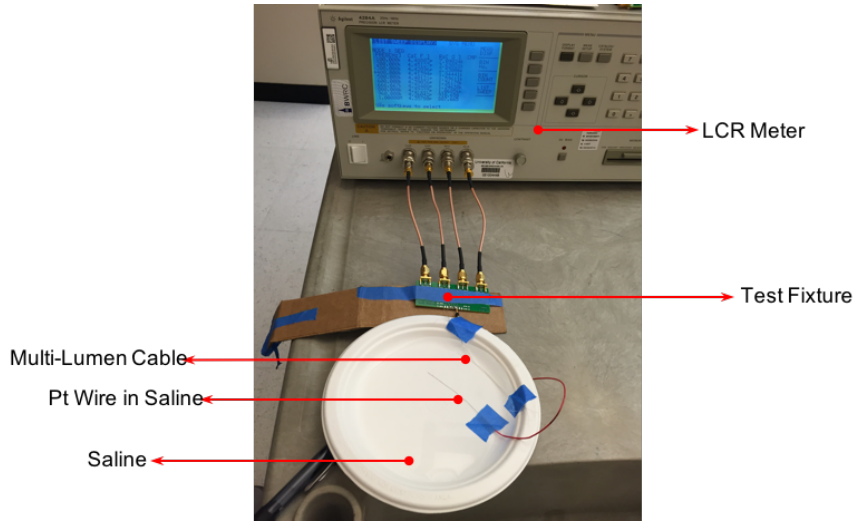

Figure 3.12: Cable Design #3 Measurement Results

time instead of the VNA because the VNA is supposed to be used in high frequencies (GHz Order) and our operation frequency is 20MHz. The sample cable is soldered to the test fixture PCB and soaked in saline to be similar to actual implanted situation. A platinum wire is also placed in saline for measuring capacitance from the wire to the body tissue (saline).

Table 3.7 shows the measured capacitances of Figure 3.11. The characteristics of this design met all the electrical requirements. Therefore, this became the final design for the cables.

Table 3.7: Cable Design #3 Measured Capacitance

Freq (KHz)	P1-P2 Cap (pF)	P1-P3 Cap (pF)	P1-P4 Cap (pF)	P1-C1 Cap (pF)	P1-C2 Cap (pF)	P1-S Cap (pF)	P2-S Cap (pF)	C1-S Cap (pF)	C1-C2 Cap (pF)
100	2.017	1.613	1.537	1.786	1.767	4.481	4.409	0.145	0.108
200	2.002	1.599	1.536	1.776	1.758	4.448	4.365	0.144	0.107
300	1.992	1.59	1.526	1.77	1.752	4.426	4.34	0.144	0.107
400	1.986	1.585	1.519	1.766	1.748	4.411	4.322	0.144	0.107
500	1.981	1.58	1.514	1.762	1.745	4.398	4.308	0.144	0.107
600	1.976	1.576	1.51	1.759	1.741	4.388	4.296	0.143	0.107
666.66	1.974	1.574	1.508	1.757	1.74	4.382	4.289	0.143	0.107
800	1.969	1.569	1.504	1.754	1.737	4.37	4.276	0.143	0.107
960	1.964	1.565	1.499	1.751	1.733	4.356	4.264	0.143	0.106
1000	1.963	1.564	1.499	1.75	1.733	4.355	4.261	0.143	0.106

Cable Design Requirements

In order for the custom cables to be compatible with OMNI modules, they should meet some electrical requirements. The main limiting factors are:

1. Cross-Talk between wires
   a) Power wires to data wire mismatch
   b) Capacitive divider between data wires
2. Cable RC Delay
3. Transmitter Drive Strength

The equation for each of these constraints will be derived below:

Cross-Talk between wires

Cross-coupled inverters are being used as receivers on AM and CM. Since the voltage margin for switching inverters is ∼200 mV, the total cross-talk should be well below this value.

- Power wires to data wire mismatch (ΔCp-d) (Figure 3.13)

$$V_{xtalk} = \frac{\Delta C_{p-d}}{C_{p-d} + C_{d-gnd}} * V_{ac} \tag{3.1}$$

  while $\Delta C_{p-d} = C_{p1-d} - C_{p2-d}$ is the two power wires to data wire capacitance mismatch.

  According to the measured values of Table 3.7, this mismatch is ≈20 fF for the final cable design which is definitely acceptable.

- Capacitive divider between data wires (Figure 3.14)

  The coupling capacitance between two data wires (C_{d1-d2}) forms a capacitive divider with the total capacitance from the wire to the ground (C_{d2-gnd}).

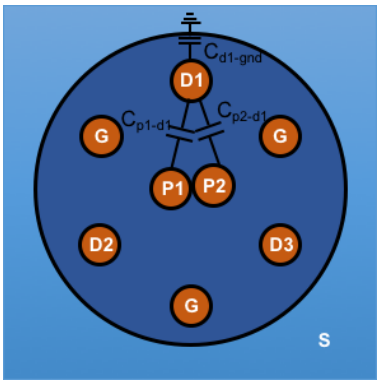

Figure 3.13: Power wires to data wire mismatch (ΔCp-d)

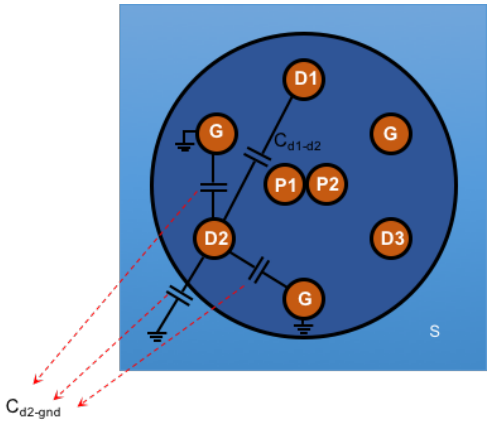

Figure 3.14: Capacitive divider between data wires

$$V_{xtalk} = \frac{C_{d1-d2}}{C_{d1-d2} + C_{d2-gnd} + C_{ac-coupl}} * V_{swing} \tag{3.2}$$

Figure 3.15 shows the divider equivalent circuit schematic.

RC time constant

The links are operating at 20MHz which is equal to 50ns period. Since the sampling is done on the negative edge of the clock and the signals are updated on the positive edge, the signal should be settled in half a period clock.

$$3\tau < T_{clk}/2 \tag{3.3}$$

which in our case means

$$R_{total} * C_{total} < 8.3ns \tag{3.4}$$

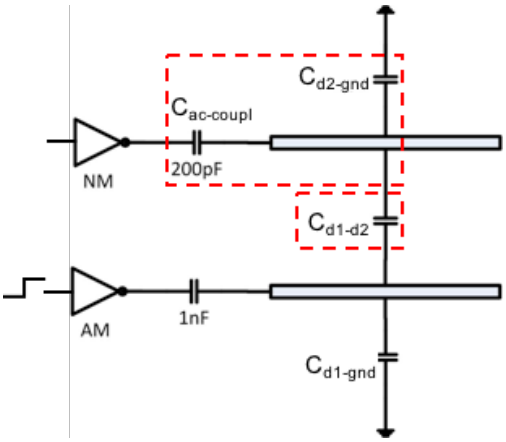

Figure 3.15: Capacitive divider Schematic

Transmitter Drive Strength

We used the FPGA IO pins as the signal drivers on AM and CM in order to save area on the PCB. The driving strength of the Igloo Nano FPGA on AM is relatively small (1mA) and can be a limiting factor.

$$C_{total} < I_{O_{FPGA}} * \frac{T_{clk}}{2V_{swing}} \tag{3.5}$$

Plugging in the numbers for the AM leads to 20.8pF for the lumped capacitance. This value is easily reachable for the short cable from AM to NMs. However, for the longer cable from AM to CM it can be hardly met by custom-designed cables. Therefore, a future improvement is to add separate driver for each signal rather than relying on FPGA pins.

$$C_{total} < 1mA * \frac{50ns}{2 * 1.2} \Rightarrow C_{total} < 20.8pF \tag{3.6}$$

Chapter 4

System Demonstration and Results

Figure 4.1 shows the full-system prototype demonstration. A fake neural signal (sinusoidal signal) is generated by a function generator and injected into the saline through a platinum wire. LLNL micro-electrode array acquires the signal and the NMIC converts it to digital packets. Then the neural data packets are sent to the AM through the custom-designed multi-lumen cable. AM routes the data to the CM and CM sends that to the PC. The neural waveforms are then plotted on the PC graphical user interface (GUI) shown in Figure 4.2. In the opposite direction, an arbitrary stimulation pattern is defined through the GUI on PC and then the stimulation commands are sent from CM to the NMIC. The electrode array applies the desired stimulation pattern into the saline as the brain tissue.

The following should be noted about the demo:

- There was a minor bug in NMIC that caused the NM to draw high current from the power drivers. Since the power drivers were not designed for that loading and could not afford it, we used a function generator to feed the differential 20MHz sinusoidal power signals to the AM and NM.
- The aforementioned bug caused issues in the data link as well. This large current is being returned through the ground wire which is also the reference for digital signal receivers. Therefore, we get bunch of 20MHz harmonics on the the ground reference which causes errors in receiving signals. We were able to overcome that temporarily by adding RC filters to the links. We expect these bugs to be fixed with the NMIC revised chip.
- The cable connecting CM to AM in this demo is not the actual one. We used the commercial Omnetics neuro connectors and cables for this testing stage. However, the actual custom-designed cable is used in the AM to NM path.
- CM is designed to communicate with PC wirelessly. However, in this demo CM is connected to the USB port on PC through FTDI UART to USB converter module. This allowed us to focus on the OMNI main modules functionality and made debugging easier.

This demonstration successfully verified the main components of OMNI which are discussed in this thesis including the communication network protocol and physical layer (cables) design.

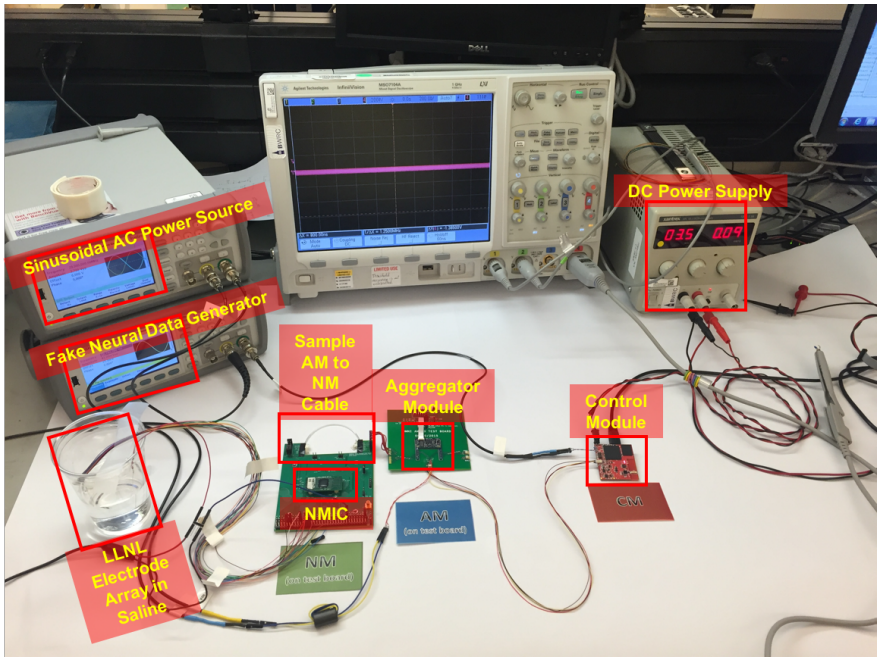

Figure 4.1: OMNI Prototype Demonstration Setup

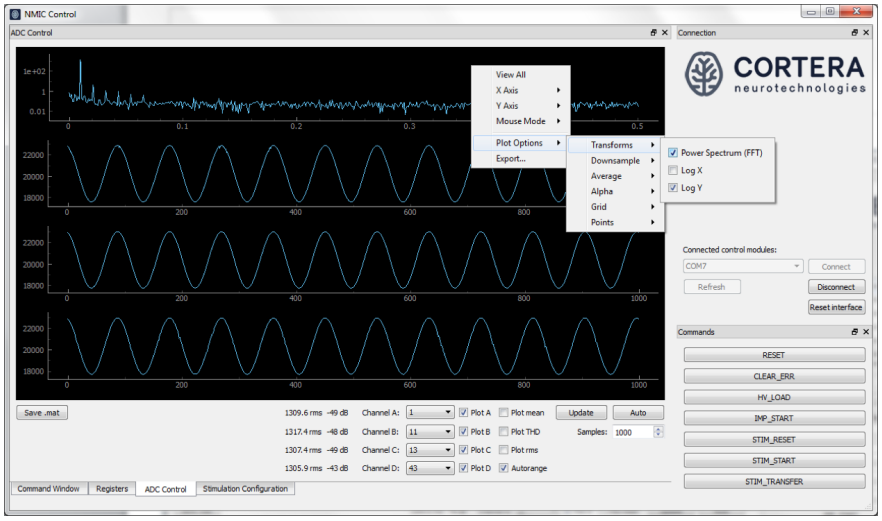

Figure 4.2: OMNI Graphical User Interface on PC

Chapter 5

Conclusion and Future Work

In this thesis, we have explored the development of a distributed, modular and closed-loop neuromodulation device for the treatment of a wide variety of neuropsychiatric disorders. The device, called OMNI, is the first network of active implantable devices in human body which introduced lots of challenges and also areas for potential research. Different layers of the network protocol stack are defined and implemented, from Physical Layer (cables) all the way up to Application Layer (GUI on PC). The required hardware for different modules is also designed and the first prototype is fabricated in collaboration with Cortera Neurotechnologies Inc. and Lawrence Livermore National Laboratory.

Although the complete system prototype is demonstrated and verified, there are a number of minor bugs that should be resolved in the future in order to become ready for the FDA approval:

- The wireless link between CM and PC is implemented and tested individually. However, it should be integrated with the whole system.
- The power drivers on CM were designed for a fixed load. However, the parasitics from the cables and other sources change the loading to the extend that the RLC tank no longer resonates at 20MHz. Therefore, the tank fixed capacitors should be replaced with digitally tunable capacitors to be able to be calibrated.
- The FPGA IO pins are used as the data transmitters for simplicity and saving PCB area. This can afford the required drive strength for AM to NM link. However, it is either infeasible or very marginal for the longer CM to AM link. Therefore, external drivers should be added to AM and CM for that link.

This project is planned for two phases. Some improvements should be made for transitioning to phase two:

- The current AM hardware supports up to four NMs. It should be modified to support up to eight NMs for the second phase. Fortunately, the network protocol is defined for

the ultimate phase two device, so the only change needed is replicating some hardware blocks.

- CM is currently external to the body. However, phase two device should be completely implanted which requires high confidence in hardware and software as well as hermetically metallic packaging similar to AM.
- Wireless charging ability should be added to CM. Moreover, the power consumption of all modules should be optimized to meet the battery life requirement. This might require migrating to ASIC for non-ASIC modules, i.e. AM and CM.

Table 5.1 shows the overall specifications of the ultimate OMNI device and a comparison to two existing neurostimulator devices:

Table 5.1: OMNI Device Specifications and Comparison

Specification	**Neuropace RNS**	**Medtronic Activa PC+S**	**DARPA OMNI**
Number of electrode arrays	1 cortical strip, 1 sub-cortical array	2 arrays, combination of sub-cortical and cortical arrays	4 cortical and 4 sub-cortical arrays (Total of 4 in Phase 1)
Number of channels	4 per array, 3.5mm and 10mm spacing	4 per array, 1.5mm spacing	512 (256 in Phase 1)
Recordable channels	Each channel selectable	Maximum of 2 at 800Hz	512 (256 in Phase 1)
Sampling Rate	200 - 600Hz	200 - 800Hz	1000 Hz
Stimulation Compliance	$\pm$12 V	$\pm$10 V	$\pm$12 V
Stimulation Parameters	Biphasic, 40 ms - 1000 ms Pulse Width	Biphasic, varies	Biphasic, Duration and Frequency Highly Programmable
Recording Noise Floor	N/A, blanked during stimulation	<150nV/$\sqrt{Hz}$ no stim, <300 nV/$\sqrt{Hz}$ with stim	<100nV/rtHz
Algorithm Supported	N/A	Support Vector Machine (Linear kernel, 4DOF)	Feature extraction, Artifact elimination, Machine learning
Real time Telemetry	N/A	11.7kbps	2Mb/s - 100Mb/s (2Mb/s in Phase 1)
Triggering	Internal	Internal/External	Internal/External
Battery Life	2-3.5 years (705mAh)	10 years (replacement)	>30days between recharge ($\approx$ a Day for Phase 1)

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