Assembly of a Wireless Ultrasonic Backscatter System

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by

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A report submitted in partial satisfaction
of the requirements for the degree of

Master of Science

Committee:
Professor Michel M. Maharbiz, Chair
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Electrical Engineering and Computer Science
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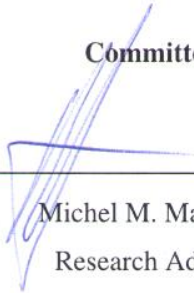
by Konlin Shen

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

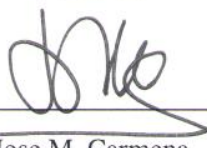Approval for the Report and Comprehensive Examination:

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Abstract

High fidelity brain recordings have enabled the development of sophisticated closed-loop brain-machine interfaces (BMIs) in which electrochemical signals generated by the brain can be used to control machines. This technology has great potential as a therapeutic tool for spinal cord injury, epilepsy, stroke, and other neurological disorders. A key challenge towards implementing BMI technology in medicine is the development of a fully implantable and chronic neural interfaces. This work details the assembly process for a 0.8mm x 3mm x 1mm implantable sensor mote for neural dust, a wireless ultrasonic backscatter system which may provide a path towards truly chronic BMI. Design constraints are delimited and failure modes from previous attempts are explained. Additionally, this work suggests possible improvements, extensions, and variants of the neural dust system for other neural and non-neural applications.

Contents

1. Introduction

1.1. Motivation

Both neuroscience and medicine have progressed through the use of neural interfaces. A neural interface is a tool which detects neuronal activity or proxies for neuronal activity, such as blood flow. Neural interfaces have found a niche in the medical community through use in BMI technology, in which communication is established between the brain and a machine. The communication link can be unidirectional, such as a cochlear implant [1], or bidirectional, such as the "brain-machine-brain" interface [2]. There is much interest in developing BMI technology as an approach to restore voluntary motor control([3], [4], [5]), as well as utilize BMI technology for closed-loop brain monitoring of various neurological conditions ([6], [7], [8]). Indeed, clinical BMI systems have already shown remarkable promise, enabling tetraplegic patients to volitionally control a robot arm to reach and grasp for items such as a thermos of coffee [9].

Despite all the promise of BMI technology, there are several technological challenges that must be solved before it can be fully adopted by the medical community. Many of these challenges are focused on improving the neural interface, in particular, managing signal stability, increasing device lifetime, and creating a completely implantable device [10]. Signal instability potentially arises due to movement of the interface or of the sampled neuronal ensemble, and can be mitigated during signal processing. Of primary concern to this work, is the creation of a completely implantable and chronic neural interface.

To begin the design of such an interface, let us recall that communication in the brain is
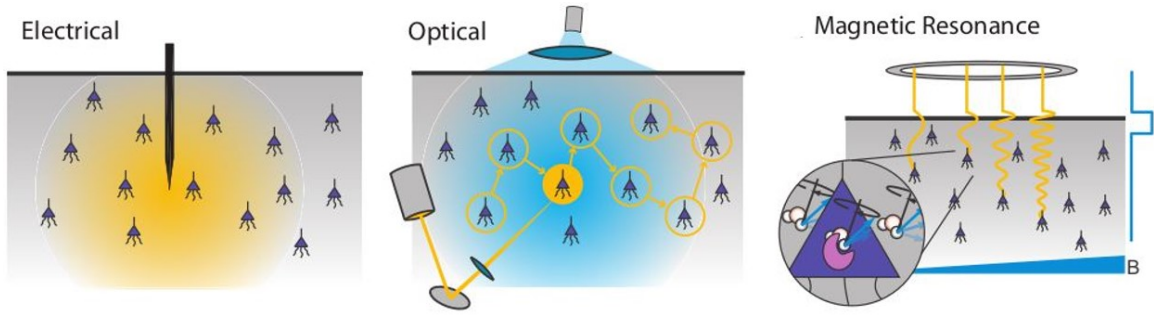
Figure 1.1.: Three common modalities for neural probing adapted from [12]. In electrophysiology, electric fields generated by neural activity are measured. For optical recording, a fluorophore whose brightness is modulated by neuronal activity is imaged. Magnetic resonance imaging utilizes the energy generated by state transitions of protons or hemoglobin molecules.

performed via electrochemical signaling between neurons [11]. While measuring electrical activity is then likely the most direct method of obtaining neural information, it can be communicated using several different energy domains such as electrical, optical, magnetic resonance, and molecular(Fig.1.1) [12]. Each domain comes with its own physical trade-offs, whether it be a limitation in spatiotemporal resolution, invasiveness, signal-to-noise ratio (SNR), or power consumption. Because we hope to achieve completely implantable devices with high spatiotemporal resolution, we focus on electrical recording methods.

1.2. Electrophysiology

As stated in the previous section, electrical signals are generated by the cell due to the flow of ions across the membrane. The cell membrane is generally impermeable to ion transfer; due to osmotic and electric pressures, the interior of the cell sits at a different potential than the extracellular solution. However, the membrane is dotted with transmembrane proteins which can allow the passage of ions through the membrane. These proteins are known as channels (passive) or pumps (active). Small molecules such as neurotransmitters can bind to these proteins to open them and allow ions to flow into or out of the cell, changing the membrane potential relative to the extracellular bath. If the membrane

potential exceeds a threshold level (predetermined by the physical properties of the membrane), the neuron fires an action potential, a stereotyped pattern of Na^+ and K^+ movement in and out of the cell (Fig.1.2). These action potentials occur on the order of milliseconds and are the primary means by which the neuronal signal is used in BMI systems.

Electrically recording neural activity has been done since the mid-1800s when Emil du Bois-Reymond connected a galvanometer to the sciatic nerve of a frog and noted that the meter's needle deflected whenever he connected a bettery to the nerve [13]. Since then, a plethora of electrically based recording techniques have been developed such as: electroencephalogram (EEG), electrocorticography (ECoG), and extracellular recording. The key difference between all of these methods is a tradeoff between spatiotemporal resolution and invasiveness. An EEG consists of electrodes which are simply placed over the skull. Generally a conductive paste is also added to improve adhesion and decrease contact resistance. While application of an EEG is quite convenient, the spatial resolution is poor due to the distortion of the neural

Figure 1.2.: Cartoon of an action potential. The action potential is marked by four major states 1) sub-threshold, 2) rising phase, 3) falling phase, 4) hyperpolarization. In general, action potentials are roughly 100 mV depolarizations that occur within milliseconds.

signal by the skull ([14], [15], [16]). Implantable extracellular recording devices such as microwires, Michigan arrays, and Utah arrays are capable of distinguishing single neuron activity, but are significantly more invasive as they require surgery for implantation and penetrate the cortex ([17], [18]). ECoGs and μECoGs serve as an intermediate, laying
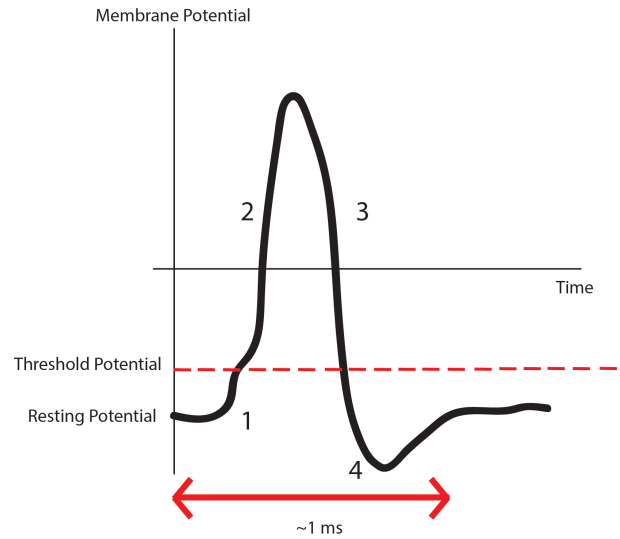
planar electrodes over the cortex, but not penetrating. However, they lack the excellent spatial resolution endowed by implantable extracellular recording devices ([19], [20]).

For implantable electrodes, the inflammatory response is the primary mechanism for device failure. Implanted devices generate glial scarring ([21], [22], [23]) due to the tissue damage from the implanataion of the device as well as repeated damage to tissue around the implantation site due to micromotions of the brain. The glial scar attempts to separate damaged tissue from healthy tissue. These scars fully form after the sixth week post implantation and envelope the implanted device and its recording sites, significantly degrading signal quality. While many efforts to alleviate the inflammatory response involve surface modification [24] or different electrode materials [25], miniaturization may also be an effective method of controlling the foreign body response. A study performed by Seymour et. al. involved implanting a parylene coated "thick" shank probe (50μm thick) integrated with a very thin lateral platform (5μm thick) in a rat for four weeks. Immunostaining sectioned tissue for NeuN (neuronal marker) and taking the difference against a Hoechst stain (DNA label), allowed for the imaging of non-neuronal cell types (i.e. cellular components of scar tissue). It was found that the local density of non-neuronal cells was significantly lower for the thin lateral platforms than the thicker shanks, implying that miniaturizing the geometry of a probe may be able to significantly reduce the inflammatory response [26].

1.3. Thesis Outline

The rest of this thesis will focus on the theory, design, and assembly of a fully implantable neural interface. In Chapter 2, two iterations of the device will be described, one using an FR-4 substrate and another using a polyimide substrate. Electrical properties and *in vivo* data will be presented, as well as potential pitfalls and their solutions. In Chapter 3, possible extensions and applications of the device will be examined. Chapter 4 summarizes and concludes the thesis, as well as mentioning near-future improvements that could be made in the existing set-up. This work also contains detailed instructions

on how to assemble the device in Appendix A, an analysis of serpentine trace design in Appendix B, code for continuous resistance measurement using a Keithley 2400 in Appendix C, and finally a possible process flow for a silicon carbide version of Neural Dust in Appendix D. The author hopes that this work can be used as a guide and foundation for building an implantable sensor mote for any application.

2. Neural Dust

Neural Dust is designed to be a completely implantable, wireless, and scalable ultrasonic backscatter system for chronic BMI [27]. The following chapter will describe the assembly of the first proof-of-concept Neural Dust sensor. The final device is roughly 0.8 mm x 3 mm x 1 mm and is capable of acute electroneurogram recordings as well as electromyograms from the sciatic nerve of an anesthetized rat.

2.1. Introduction

As elaborated upon in chapter 1, BMIs have great potential in the medical space, but in order for them to become clinically useful, they must become completely implantable with long device lifetimes as well as collect a useful signal for effective control of the machine. This boils down to the following device amenities:

- Wireless communication between the fully implanted sensor and an external hub

- Minimized foreign body response

- Temporally stable encapsulation material

- High spatiotemporal resolution over a large volume

A fully implanted device implies that the device is not only fully contained within the body, but the implantation site is also completely closed. This is essential for chronic implantations as a wired device leave not only an open wound in the patient's body, but the wires also provide a route for infectious agents to access the brain. Minimizing the foreign body response is important to prevent glial scarring and maintain signal quality.
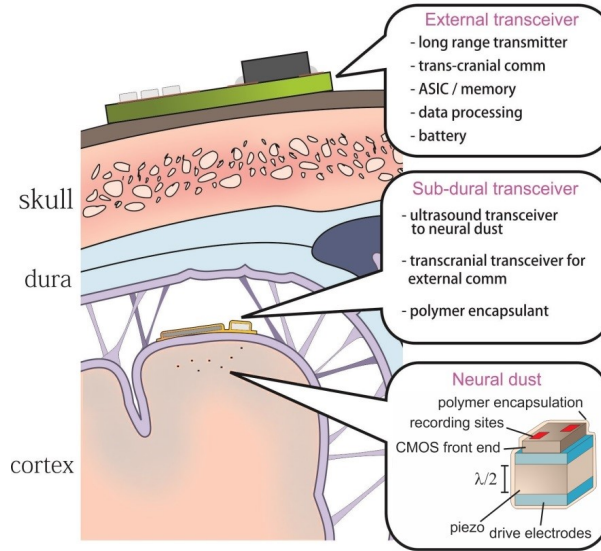
Figure 2.1.: An overview of the Neural Dust system (Figure used with permission from [28]). There are three major components, the sensor motes, the sub-dural ultrasonic interrogator, and the external electromagnetically coupled transceiver

The encapsulation material must remain stable over time in order to prevent extracellular fluid from leaking into the device and and causing shorts. Finally, high spatiotemporal resolution over a large volume allows for the collection of large amounts of high fidelity neural data, which greatly facilitates effective volitional control of prosthetics.

To satisfy these conditions, Seo et. al. [27] has proposed a system design utilizing ultra-miniature sensor motes which communicate wirelessly to a subcranial ultrasonic interrogator, which in turn communicates electromagnetically with an external transceiver(Fig.2.1). The goal of miniaturization effectively solves both the foreign body response challenge (refer to Chapter 1) as well as the high resolution and large recording volume challenge. Miniaturization enables high spatial resolution as minimizing the recording electrodes decreases the amount of spatial averaging, increasing SNR. Furthermore, by minimizing the tissue displacement of each sensor, we allow for the introduction of more sensors, and thus can sample a larger volume of the brain.

The use of ultrasound as a communication modality synergizes nicely with aggressive miniaturization. As our device decreases in size, the resonant frequency of its coupling component increases. To maximize coupling efficiency, it is generally best to transmit

at the resonant frequency of the coupling component. However, the attenuation of electromagnetics, the conventional energy modality for wireless communication, in tissue decreases exponentially as frequency increases [29]. This results in poorer link efficiency as the device is scaled down. On the other hand, the attenuation of ultrasound in tissue is significantly lower than electromagnetic attenuation since electromagnetics is severely attenuated via dielectric loss whereas acoustic loss is only due to medium viscosity [30].

The Neural Dust system consists of a piezoelectric element attached to the drain and source of a transistor. Exposed electrodes connecting the source and gate of the transistor report the local environment by modulating the drain-source current of the transistor (Fig.2.2). Power is delivered to the FET by hitting the piezoelectric element with ultrasonic energy. Modulation of the gate-source voltage by local activity similarly modulates the drain-source current. This current clamps the piezoelectric element thus reducing the amplitude of the backscattered wave, which is received by the ultrasonic transducer. The amplitude fluctuation of the transducer is then back-calculated to reveal the signal recorded by the sensor. A schematic of this system is shown in Figure 2.1. The system has been theoretically shown to be valid with an SNR of 3 down to mote sizes of 50 μm.

The work in this thesis builds upon the theoretical framework and model validation of Neural Dust found in [27] and [28] and details the assembly of the first Neural Dust system used *in-vivo* to record electroneurograms and electromyograms of rat peripheral nerve and skeletal muscle, respectively.

2.2. Neural Dust Assembly Process

The Neural Dust mote consists of a piezoelectric crystal, a custom application-specific integrated chip (ASIC), and a printed circuit board (PCB). In short form, the assembly steps are as follows:

1. Attach ASIC to PCB

2. Wirebond ASIC ports to PCB

3. Attach piezoelectric element to PCB

4. Wirebond piezoelectric element ports to PCB

5. Encapsulate full device except for recording electrodes

The ASIC measures 450μm by 500μm by 500μm and is fabricated by Taiwan Semiconductor Manufacturing Company's 65nm process. Each chip contains two transistors with 5 ports each: source, drain, gate, and center, and bulk. Each FET uses the same bulk, so either bulk pad can be bonded to, but the transistors differ in that the transistor padded out to the top row does not contain a resistor bias network whereas the transistor padded out in the bottom row does. The chip additionally con-

Figure 2.2.: The circuit architecture for backscatter modulation adapted from [27]. A FET operating in the subthreshold regime alters its impedance as a function of gate voltage, which in turns alters the reflectivity of the piezoelectric element.

tains smaller pads for electroplating. These pads were not used in this work. Three versions of the FET were taped out:

- Die 1: Long channel FET with threshold voltage: 500 mV

- Die 2: Short channel FET with threshold voltage at 500 mV

- Die 3: Native FET with threshold voltage at 0 mV

Confirmation of electrical characteristics of these FETs were measured using a specially designed CMOS characterization board which consisted of a set of pads as wirebonding targets and a second set of pads in which wires were soldered to (Fig.2.4). A sourcemeter (2400 Sourcemeter, Keithley Instruments, Cleveland, OH) was used to supply V_{DS} to
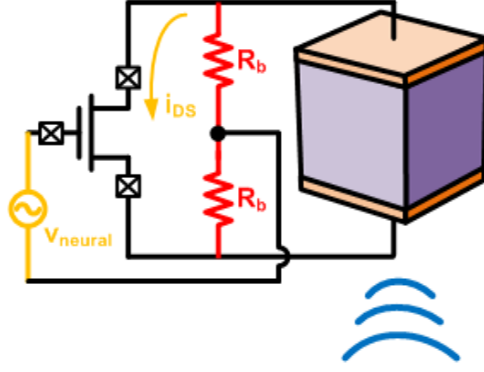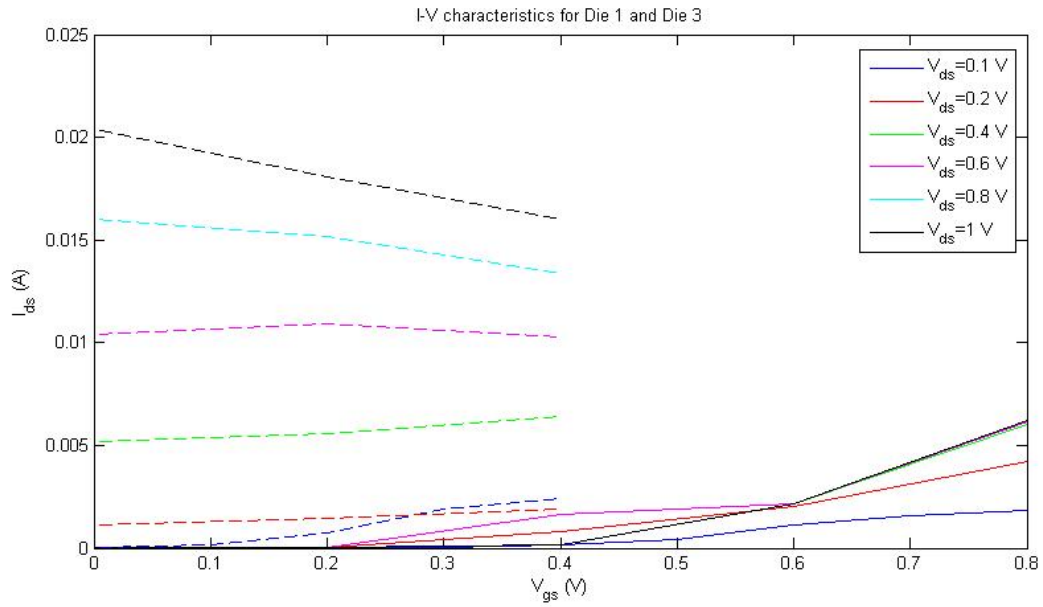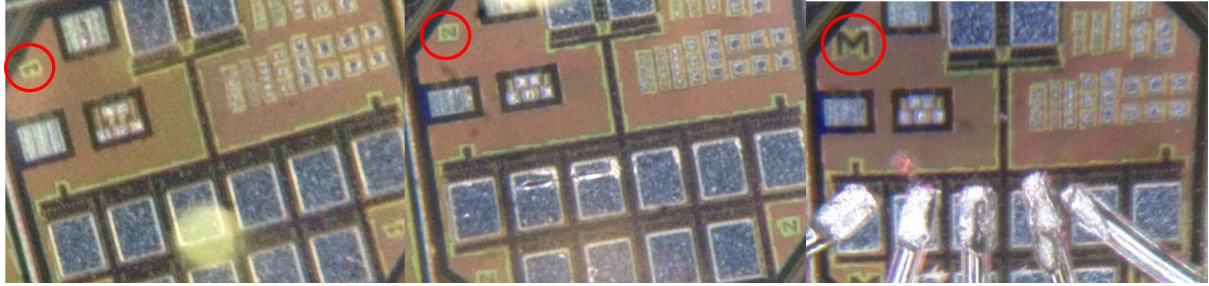
Figure 2.3.: Top: Physical markings on the die showing their type (1,2,3 from left to right). Bottom: I-V curves for Die 1 and Die 3. Note that because Die 3 has a threshold voltage of 0 V, we did not test the dies above 0.4 V as a safeguard against damaging the device.
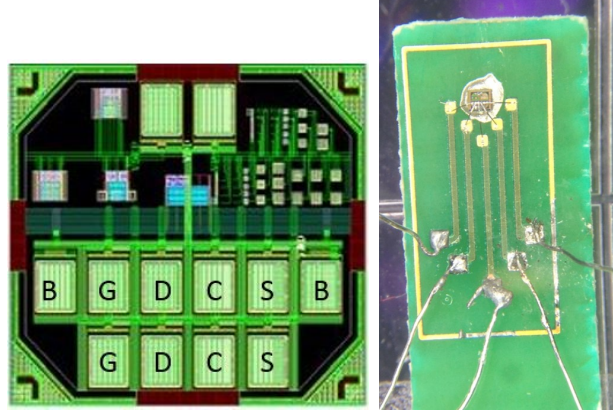
Figure 2.4.: Left: An annotated layout of the ASIC. The ASIC measures roughly $500\mu m$ by $450\mu m$. The pad labels are as follows: B - bulk, G - gate, D - drain, C - center, S - source Right: ASIC testing PCB. The die is attached to the PCB using silver epoxy and is wirebonded to the small pads surrounding it. The wirebonding target pads are routed out to larger pads which can have wires soldered to them for easy access.

the FET and measure I_{DS}. An adjustable powersupply (E3631A, Agilent, Santa Clara, CA) was used to modulate V_{GS} and the I-V characteristics of the FETs were obtained (Fig.2.3). We consistently measured uncharacteristic IV curves for type 2 dies, and upon impedance measurement, found that the short channel of the die 2s would short out the FET.

The piezoelectric element is lead-zirconium titanate (PZT). It is purchased as a disc from APC International and diced into 750 μm x 750 μm x 750 μm cubes using a wafer saw (DAD3240, Disco, Santa Clara, CA) with a ceramic blade (PN CX-010-270-080-H). This mote size was chosen as it maximized power transfer efficiency. For more details see [28].

Our sensor mote is implantated in the sciatic nerve of a Long-Evans rat (Fig 2.5). This nerve is large diameter nerve bundle which innervates the hindlimb. The nerve is between 1-1.5 mm in diameter and its size and accessibility make it an ideal candidate for Dust implementation [31]. While several iterations of Dust were made, the following section will detail the development of the two versions of the Neural Dust mote which were implanted in rat models.

2.2.1. Substrate Design

The Neural Dust substrate integrates the ASIC with the piezoelectric element and recording electrodes. The first version of Dust used custom-designed PCBs purchased from The Boardworks (Oakland, CA) as a substrate. The PCBs were made of FR-4 and were 30 mil in thickness. The dimensions of the board were 3 mm x 1 mm. This design was the first attempt at an integrated communication and sense platform, so pad size and spacing was cho-
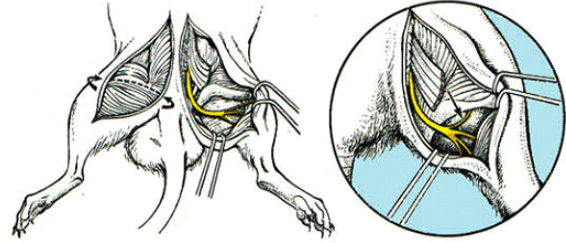

Figure 2.5.: A cartoon of the sciatic nerve of a rat, highlighted in yellow. Image adapted from [32]

sen to facilitate assembly at the cost of larger size. To conserve PCB real-estate, each face of the PCB included pads for either the piezoelectric element or the ASIC and its respective connections to the PCB. Additionally, two recording pads were placed on the ASIC-face of the board. All exposed electrodes were plated with ENIG by The Boardworks. The pad for the ASIC to sit on was 500μm by 500μm, chosen to fit the size of the die. The wirebond target pad size was chosen to be 200μm by 200μm and spaced roughly 200μm away from the edge of the die in order to give enough clearance for wirebonding (discussed below). Electrode size and spacing varied and were empirically optimized. It was found that electrode spacings greater than 1.5 mm were optimal for recording (Fig 2.6).

In the second iteration of Dust, we primarily addressed three concerns: 1) size, 2) ease of wirebonding, 3) implantation/communication. First, to decrease board thickness we replaced the FR-4 substrate with a 2 mil thick polyimide flexible PCB (AltaFlex, Santa Clara, CA), as well as thinning the ASIC (Grinding and Dicing Services Inc., San Jose, CA) to 100μm. To facilitate bonding, the ASIC and PZT coupon were moved to the same side, with only the recording electrodes on the backside of the substrate. While putting the ASIC and PZT coupon on the same side of the board does impose a limit on
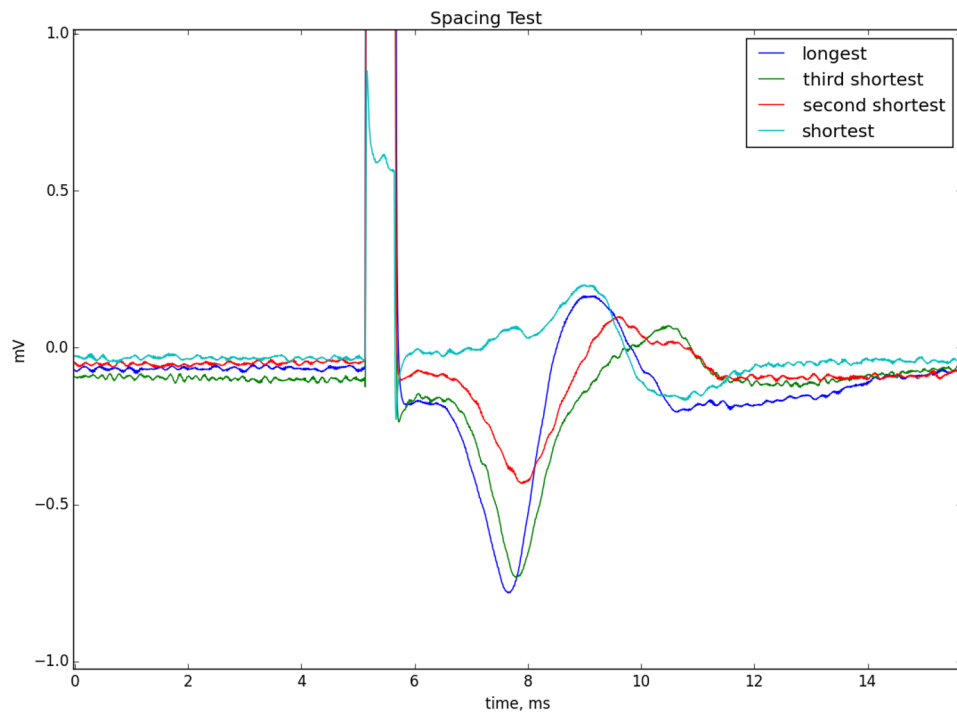
Figure 2.6.: Signal amplitude as a function of electrode spacing. Four pairs of electrodes spaced 2 mm, 1.5 mm, 1 mm, and 0.5 mm away from each other were used. Minimal signal attenuation was noted between 2 mm and 1.5 mm, but a signal strength decreased by about 33% between 1.5 mm and 1 mm.
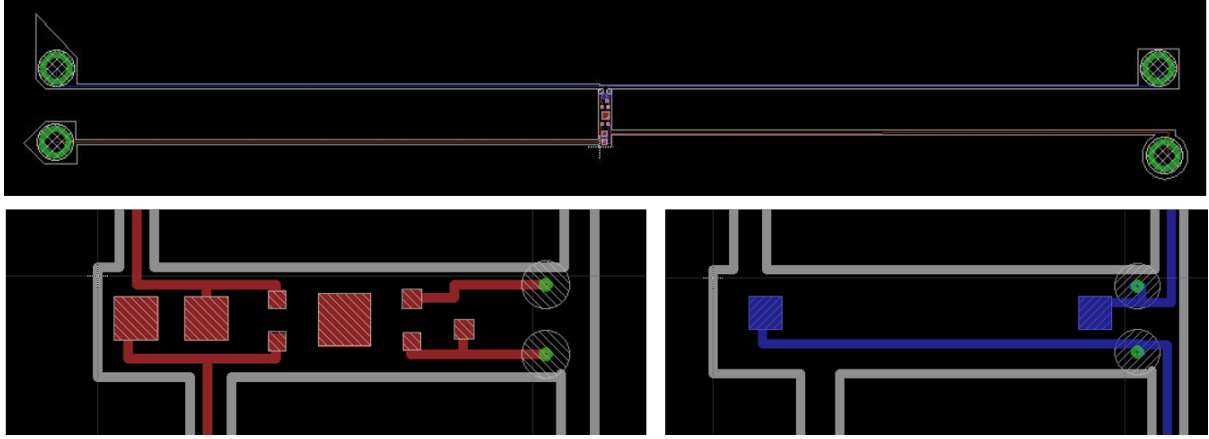
Figure 2.7.: Top: Full layout of version 2 Neural Dust boards. Bottom Left: Close up of version 2 board ASIC/PZT side. Bottom right: Close up of version 2 electrode side.

how much the substrate size can be reduced, we were already restricted to a board length of at least 2 mm in order to obtain proper spacing between the recording electrodes. To push minimization efforts ASIC bonding pads were reduced to 100μm by 100μm, but the 200μm spacing between bonding pads and the ASIC itself had to be maintained to provide space for wirebonding. The attachment pads for the PZT coupon was also shrunk and placed closer to the edge of the board, with the rationale that the PZT coupon did not have to wholly sit on the board, but could hang off it. Additionally, the location of the pads relative to the ASIC was also modified to facilitate bonding. In the original design, the bond pad layout surrounding the ASIC required two wirebonds to cross. This is not impossible, but very difficult to avoid shorting the pads (Fig. 2.12). Thus, the pad layout was shifted so that the bonds are relatively straight paths. Finally, during animal experiments, we found that alignment of the neural dust mote was quite difficult. To combat this, we added four 1 in. test leads that extended off the board, two of which connected directly to the source and drain of the device so that we could measure harvested power and use that as an alignment metric. The other two leads connect to the gate and center ports in order to obtain a ground truth signal. In order to prevent confusion over which lead belonged to which port, the vias were given unique geometries (Fig. 2.8).

There was some fear that the test leads may be easily broken or would easily displace the mote if force was applied on them. Thus, we designed a version with serpentine traces. Serpentine traces (Fig.2.9) have often been used to enable deformable interconnects([33], [34], [35]) as their structure allows them to "accordion" out. Conceptually, the serpentine trace design can be though of a series of cantilevers in series via

Figure 2.8.: The vias of the Neural Dust version 2 board test leads were uniquely shaped to facilitate port recognition. The "tooth" geometry corresponded to the gate, the pentagon corresponding to the drain, the circle corresponding to the center, and the square corresponding to the source .

connector beams. A detailed analysis of serpentine trace design can be found in Appendix B.

Along with the presented designs, a miniaturized version of the Dust mote using both sides of the substrate was also designed and assembled (Fig. 2.10). In this design, the board measures roughly 1.5 mm by 0.6 mm by 1mm. Due to the miniaturization of the board, the device cannot be used for recording without attaching a 5 mil silver wire "tail" to the board to act as an electrode and was not used *in vivo*.

2.2.2. Die and PZT attach

The ASIC and PZT coupon were attached to the PCB substrate using adhesives. There are three majors concerns

Figure 2.9.: Serpentine tail design.

to choosing an adhesive: 1) the adhesive needs to fix the ASIC and PZT tightly enough that the ultrasonic power from wirebonding does not shake the components, 2) due to the sub-millimeter scales and pitches of the components/substrate pads, application of the
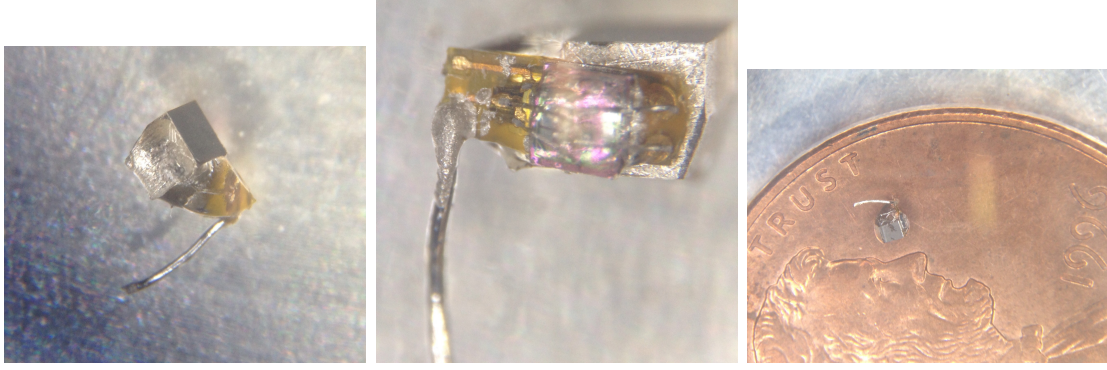
Figure 2.10.: A "condensed" version of the neural dust mote. Assembly is performed in the same manner as the standard board, except a 5 mil silver wire is silver pasted to one of the pads to act as a "tail" in order to preserve signal strength.

adhesive must be done in a relatively precise way, and 3) the adhesive must be electrically conductive.

The ASIC and diced PZT were originally attached to the PCB substrate using a low temperature-curing solder paste. Solder paste consists of powder metal solder suspended as spheres in flux. When heat is applied, the solder balls begin to melt and fuse together. However, it was found that the curing of the solder paste would often result in translating or rotating the PZT coupon or mote during reflow. This presented problems for PZT alignment and power harvesting, as well as problems for wirebonding due to the bondpads no longer being appropriately positioned from the chip. However, we found that a two-part silver epoxy, which simply consists of silver particles suspended in epoxy was capable of curing without repositioning the chip or PZT coupon. Thus, the ASIC and diced PZT were pasted onto the PCB using a two-part conductive silver epoxy (H20E, Epotek, Billerica, MA). The PCBs were then affixed to a glass slide using kapton tape (Polyimide Film Tape 5413, 3M, St. Paul, MN) and put into a convection oven at 150°C for 15 minutes to cure the epoxy. While higher temperatures could yield faster curing (Fig. 2.11), care was taken to avoid heating the PZT beyond 160°C, half the Curie temperature of the PZT. Heating the PZT any higher runs the risk of depolarizing the PZT [37]. We found that the 150°C cure had no effect on the CMOS performance.
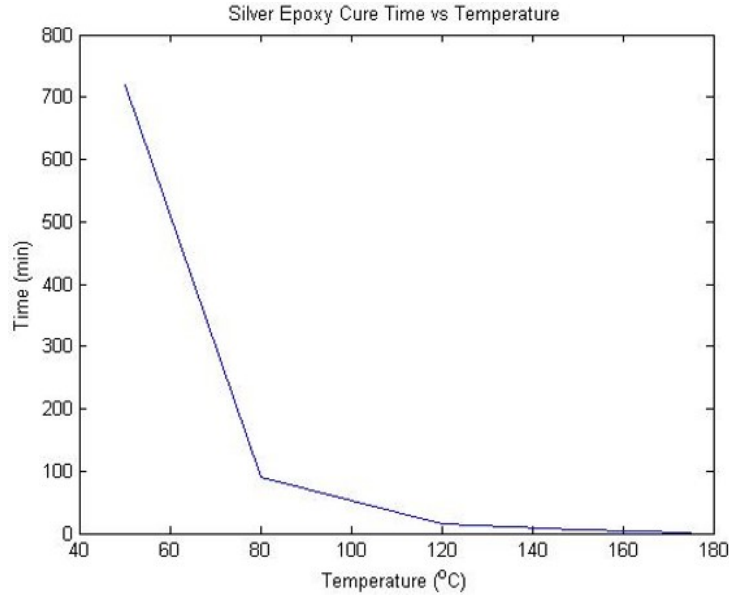
Figure 2.11.: Silver epoxy cure time versus bake temperature. Data points from [36] and empirically verified.

2.2.3. Wirebonding

The connections between the top of the PZT and the PCB as well as the ASIC and the PCB were made by wirebonding 1 mil Al wire using an ultrasonic wedge bonder(7400B, West Bond, Scotts Valley, CA); in this method of bonding, the Al wire is threaded through the wedge of the bondhead and ultrasonic energy "scrubs" the Al wire against the substrate, generating heat through friction. This heat results in welding the two materials together.

Wirebonding to the ASIC was challenging to avoid shorts due to the size of the CMOS pads and the size of the foot of the wirebond. This problem was accentuated due to the positioning of the wirebonding targets in the first version of the Neural Dust board, which forced the feet of two bonds to be placed across the smaller width of the ASIC pad rather than the length. While thinner gold wire was available to use for bonding, the difficulty of bonding gold thermosonically with a wedge bonder made it impractical to use gold wires for bonding. Furthermore, in order to effectively wirebond, it is important to have a flat and fixed substrate; hence, our original design of having the ASIC and PZT on different sides of the board often caused trouble during the wirebonding process in

our first version of Neural Dust boards. Thus, the substrate design choices made in the second iteration of dust (moving ASIC and PZT to the same side, repositioning the pads to provide straight paths to wirebond targets) greatly improved wirebonding yield.

Finally, because we used an ultrasonic bonder, we found that bonding to the PZT resulted in a charge build up would damage the chip once the PZT was fully bonded to the substrate. To avoid this, the source and drain test leads of the device were discharged to Earth ground directly prior to wirebonding the PZT.

2.2.4. Encapsulation

The final step of Dust assembly is encapsulation. This important step must achieve two goals: 1) insulation of the PZT, bondpads, and ASIC from aqueous environments and 2) protection of the
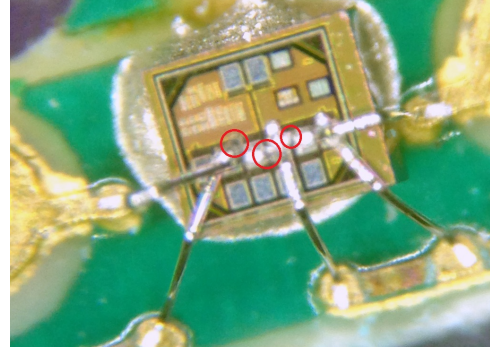
Figure 2.12.: Wirebonds connecting the ASIC to the version 1 Neural Dust PCB substrate. Problem spots caused by wire crossovers are circled in red.

wirebonds between the ASIC/PZT coupon and the PCB. At the same time, there must be some method to either remove or prevent the encapsulant from covering the recording electrodes. Additionally, the encapsulant must not impede device implantation. Finally, while it is not crucial, it is of interest to choose an encapsulant that is optically transparent so that the device can be inspected for physical defects if some damage occurred during the encapsulation.

The first encapsulant we used was Cystalbond (509 , SPI Supplies, West Chester, PA). Crystalbond is an adhesive that is solid at room temperature but begins to soften at 71°C and melts into a viscous liquid at 121°C. Upon removing heat from the Crystalbond, it resolidifies within minutes, allowing for good control. To encapsulate the mote, a small flake of Crystalbond was shaved off with a razor and placed directly over the device. We

then heated the board using a hotplate, first bringing the temperature to around 70°C when the flake would begin to deform and then slowly increasing the temperature until the Crystalbond became fully liquid. Once the edge of the liquid Crystalbond drop expanded past the furthest wirebond but not the recording pad, the hotplate was turned off and the board was quickly moved off the plate onto a cooling chuck where the Crystalbond would resolidify.

While Crystalbond was effective, we found that UV curable epoxies could give us better selectivity and biocompatibility, as well as rapid curing. We first tested a light-curable acrylic (3526, Loctite, Dusseldorf, Germany), which cures with exposure to ultraviolet light. A sewing needle was used as an applicator to obtain high precision and the epoxy was cured with a 405 nm laser point for 2 minutes. This epoxy worked well, but was not medical-grade and thus not appropriate for a biological implant. We thus tried a medical-grade UV curable epoxy (OG116-31, EPO-TEK, Billerica, MA). The epoxy was cured in a UV chamber (Flash, Asiga, Anaheim Hills, CA) with 92 mW/cm^2 at 365 nm for 5 minutes. While this epoxy was slightly less viscous than the Loctite epoxy, using a sewing needle again as an applicator allowed for selective encapsulation. As an insulator and protection mechanism for the wirebonds, the epoxy was very effective, but was found to leak during prolonged submersion in water ($\sim$ 1 hour). A second medical grade epoxy which touted stability for up to a year, was considered (301-2, EPO-TEK, Billerica, MA), but was found to be not viscous enough and required oven-baking for curing. Despite the instability of the UV epoxy, the duration of use was suitable for acute *in vivo* experiments.

To improve encapsulant stability, parylene-C was also considered as an encapsulation material. Parylene-C is an FDA approved biocompatible polymer which is chemically and biologically inert, a good barrier and electrical insulator, and extremely conformal when vapor deposited ([38], [39], [40]). Vapor deposition of Parylene-C is achieved by vaporizing powder Parylene-C dimer at temperatures above 150 °C. The vapor Parylene-C dimer is then heated at 690°C in order for pyrolysis to occur, cleaving the Parylene-C dimer into monomers. The monomer then fills the chamber which is kept at room temperature. The monomer almost instantaneously polymerizes once it comes into contact

Table 2.1.: Parylene-C Deposition Parameters

Furnace Temperature	690°C
Chamber Gauge Temperature	135°C
Vaporizer Temperature	175°C
Base Pressure	14 mTorr
Operating Pressure	35 mTorr
Parylene-C Mass	5g

with any surfaces [41]. For all devices, parylene-C was deposited using a parylene deposition system (SCS Labcoter 2 Parylene Deposition System, Specialty Coating Systems, Indianapolis, IN) with the parameters shown in Table2.1. Note that the table indicates the chamber gauge temperature as 135°C. This is distinct from the actual chamber temperature; rather the chamber gauge is simply the vacuum gauge of the process chamber. It is important to keep the temperature to at least 135°C to prevent parylene from depositing onto the gauge. For the first batch of FR-4 boards, we attempted to address parylene selectivity by using kapton tape to mask off the electrodes. However, we found that due to the small pitch between the recording electrodes and the ASIC wirebonding targets, there was not enough surface area for the tape to affix well to the board and it often slipped off, resulting in coated electrode pads. In the second iteration of dust, we attempted to parylene coat again and chose a strategy in which we would coat the entire board, then remove the parylene off the electrodes with a probe tip. In order to assure that parylene was coated onto the entire device, the dust motes were suspended in air by clamping them between two stacks of glass slides (Fig.2.13). However, we found that devices coated in parylene all displayed unusual I-V characteristics. The exact mechanism as to why parylene coated resulted in this problem is unknown, but we hypothesize that stray charge stored in the parylene may discharge into the ASIC, shorting it. A less likely alternative may be that small vibrations of the parylene chamber could be causing the PZT to discharge into the ASIC.
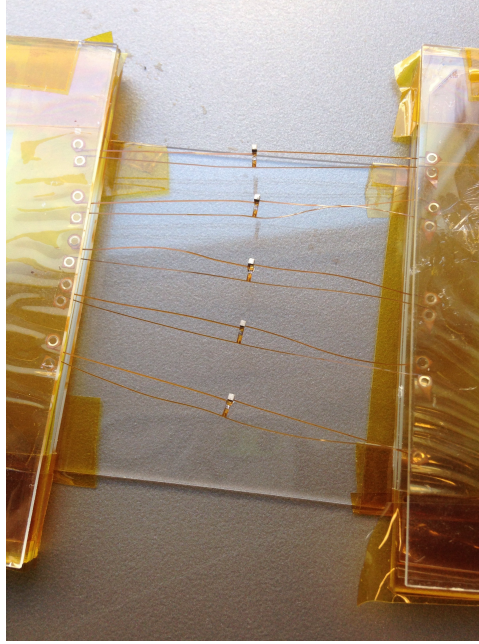
Figure 2.13.: Parylene Test Jig

2.3. Neural Dust Test Board

Testing of Neural Dust motes has always been tricky due to the thin-ness of the test leads that extend out from the board. Clipping onto and off of these vias for I-V measurements has often resulted in pulling the leads off the body of the device. Furthermore, due to the test leads, it is difficult to perform water-tank test measurements, as exposed electronics in water would result in shorts. In order to circumvent this issue, a PCB was designed to serve as a testbed for Neural Dust measurements (Fig. 2.14).The PCB (Bay Area Circuits, Fremont, CA) was made of FR-4 and 60 mil thick; it includes four vias, distributed on the board to match the layout of the version two Neural Dust boards.

Gold header pins (Pin Strip Header, 3M, Austin, TX) were soldered into the vias so that they extended from the board on both sides of the board. This enabled us to place our devices onto the test bed, and tap into the mote by accessing the header pins. Next, to insulate the vias, plastic caps made out of polyethylene terephthalate (PETG) were 3D printed (Flashforge Creator X, FlashForge, Jinhua, China). These caps were printed with a groove so that an O-ring could be placed inside the groove and create a waterproof seal around the header pins. The caps were connected to the board and
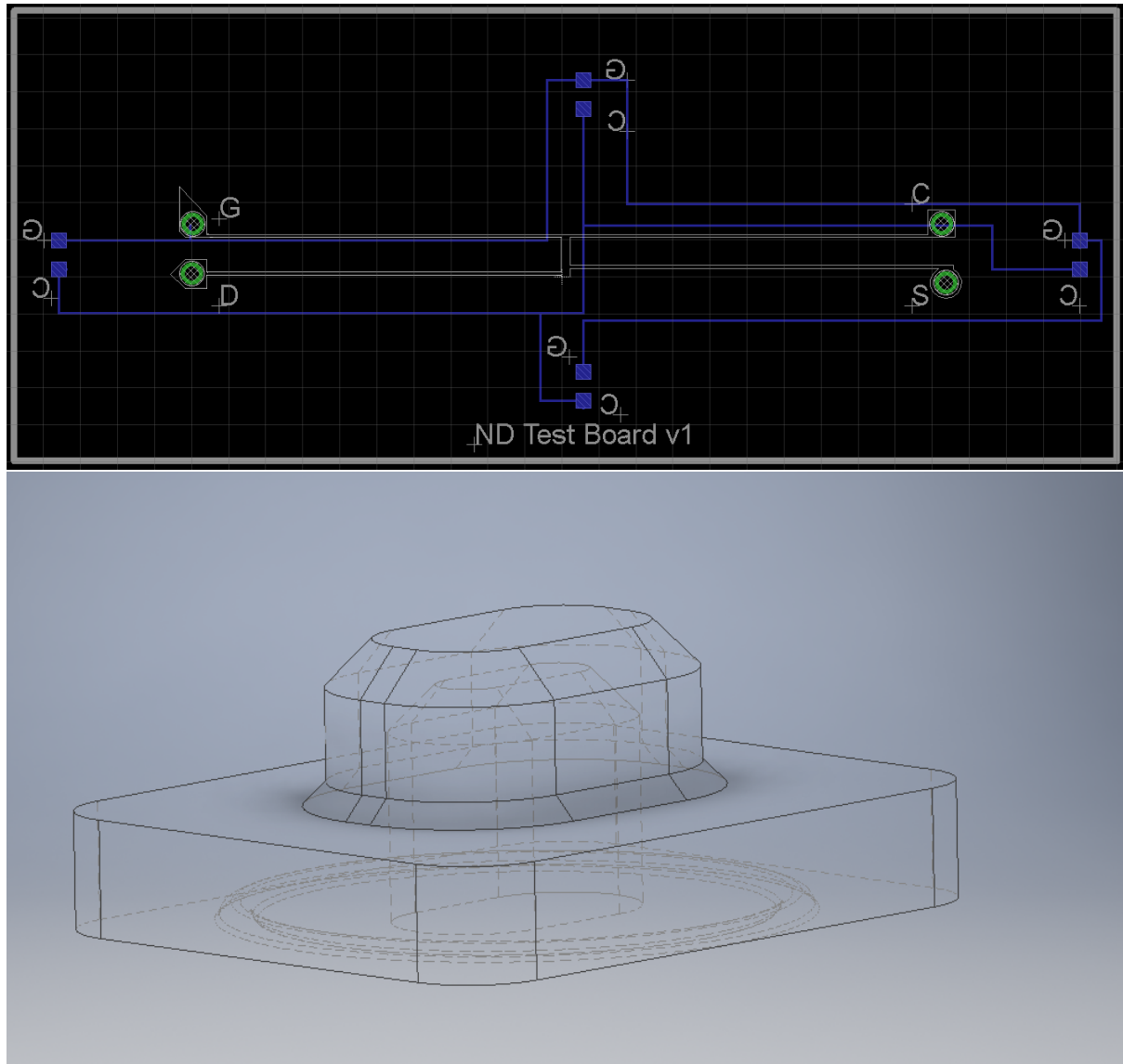
22

Figure 2.14.: Top: Layout of testbed. Vias are designed to fit 1 mm header pins so that test leads of the Dust version 2 boards could be placed over them. Pads were included on the backside to enable external electrode connections if necessary. Bottom: Model of 3D printed cap.
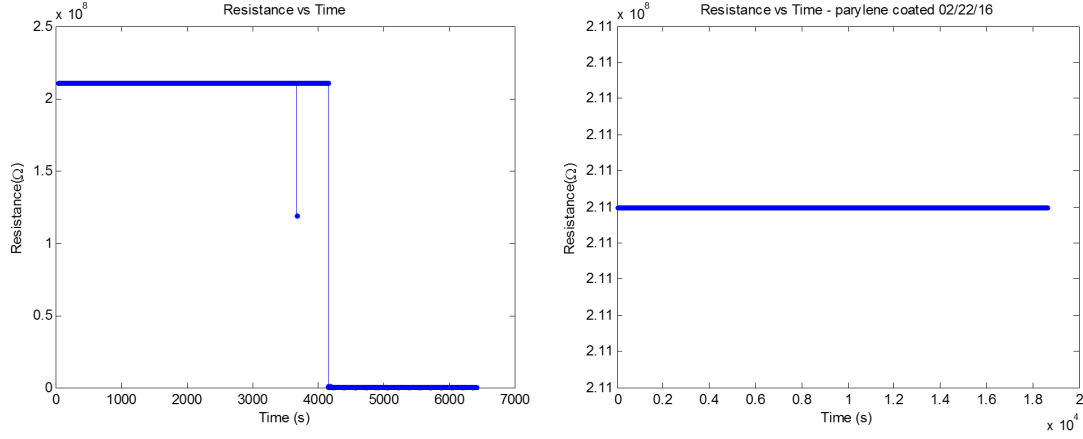
Figure 2.15.: Resistance between two neighboring pins of the testbed subermeged in a salt water solution as a function of time for only epoxy insulation (left) and epoxy plus parylene insulation (right). Without a parylene barrier, the epoxy begins to leak, allowing salt water to short out the pins of the testbed.

compression was created by drilling 2 mm holes through the PCB and cap using a micro-mill (47158, Harbor Freight, Camarillo, CA) and screwing the cap and board together. Wires extending from the testbed were soldered to the header pins and the pins were then encapsulated. To measure the effectiveness of the seal, the boards were submerged in an aqueous 6 M NaCl solution and the resistance between the pins was measured using a Keithley 2400. A MATLAB script (see appendix C) was written to automatically record and plot the resistance over time. A drop in the resistance would indicate that the seal was broken. As an additional test, a piece of litmus paper was also put under the plastic cap with the intention that if the cap leaked, the litmus paper would change color. We encapsulated the pins using the same medical grade epoxy used to encapsulate the neural dust boards and parylene was deposited over the epoxy on the backside of the testboards for a completely waterproof barrier.

2.4. Results and Discussion

The first version of Neural Dust were 1 mm x 3 mm x 1 mm PCBs made of FR-4 with a PZT piezoelectric, silicon ASIC, and encapsulated using crystal bond (Fig. 2.16). These were implanted into a the sciatic nerve of an Adult male Long-Evans rat anesthestized
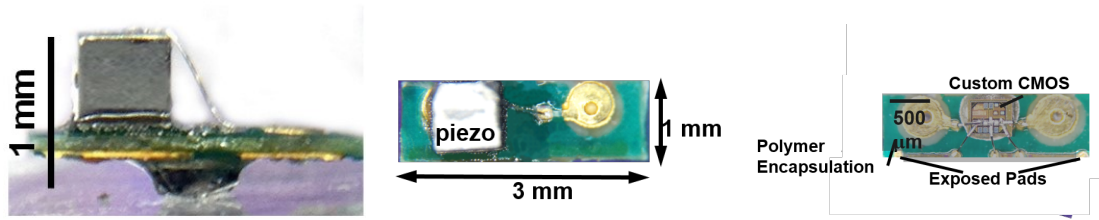
Figure 2.16.: A fully assembled version 1 Neural Dust sensor mote from side view, top view, and bottom view (left, center, and right respectively).

with a mixture of ketamine and xylazine IP (Fig. 2.17). A ground truth measurement was obtained using a tungsten microwire with a 28G stainless steel needle electrode placed in the foot of the animal as a reference. Nerve activity was evoked using electrical stimulation and backscatter data was acquired by sending and receiving pressure waves using a transducer (V323-SU-F, Olympus, Waltham, MA).

The original signal across the dust mote was later calculated from the backscatter data using MATLAB. A representative trace of the reconstructed signal versus the ground truth is shown in Figure 2.18.

The reconstructed mote data followed the general profile of the ground truth, capturing the compound action potential of the nerve, but several features present in the reconstructed data (such as the "dips" found from the first to third second) could not be explained.

The second version of the dust mote were roughly 0.8 mm x 3 mm x 1 mm and used a polyimide substrate and medical-grade UV curable epoxy as encapsulation. A crucial change was the addition of test leads 1 in. long, allowing us to see the voltage across the piezoelectric element as well as take ground truth measurements by tapping into the recording electrodes. The same device implantation protocol was used in version two as was used in version one, but reconstruction of the backscattered signal was done on the fly using a custom transceiver board. Results are not shown here, but more information regarding the set-up and results of the experiment using version 2 Neural Dust sensor motes can be found in [42].

Figure 2.17.: Version 1 Neural Dust mote implanted in the sciatic nerve of an adult Sprague-Dawley rat.
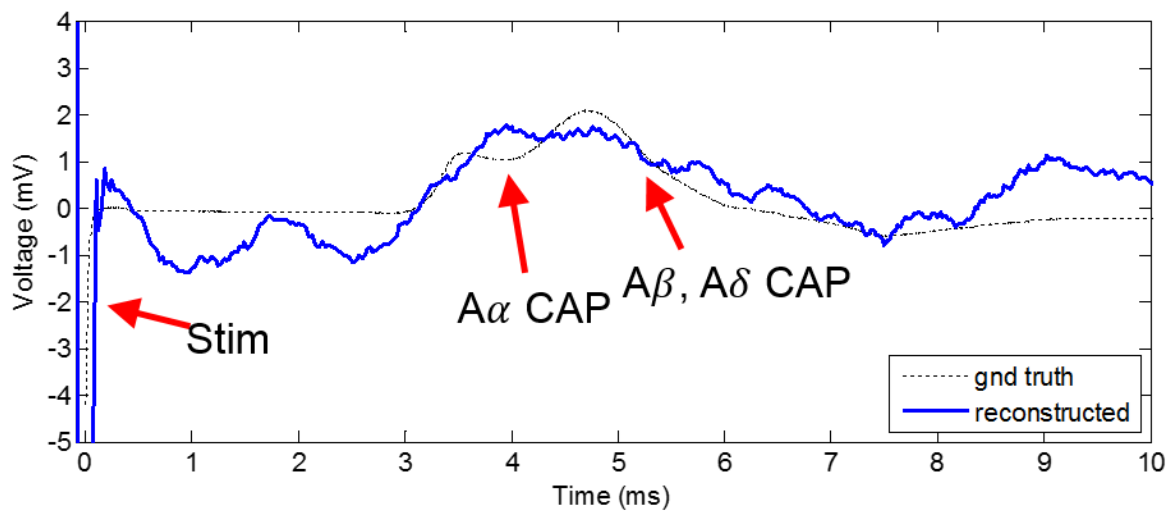

Figure 2.18.: Recorded ENG utilizing version 1 Neural Dust sensor motes. The dotted trace shows the signal recorded by the ground truth electrode. A general profile consisting of compound action potentials matching the profile of the ground truth was reconstructed (blue) from the acquired Neural Dust data.

3. Applications

While the presented work demonstrates the wireless detection of peripheral nerve activity, the use of ultrasound to transfer energy through the body can be universally applied to many different implantable systems. In this chapter, we will consider other applications the Dust platform could be used for, both neural as well as non-neural.

3.1. Future Neural Directions

3.1.1. SiC Dust

We have shown a version of Dust which is capable of acute PNS recordings, but the longevity of our polymer encapsulant fails over many hours of submersion in liquid, as seen in Fig.2.14. Rather than an epoxy encpasulant, silicon carbide (SiC) may be a more effective material for insulating and protecting the device. SiC is formed by the covalent bonding of Si and C, forming tetrahedrally oriented molecules with short bond length and thus, high bond strength, imparting high chemical and mechanical stability(Fig.3.1). Amorphous SiC (a-SiC) has been welcomed by the biomedical community as a coating material as it can be deposited at much lower temperatures than ordinarily required by crystalline SiC and is an electrical insulator [44]. Deposition of a-SiC is generally performed via plasma enhanced chemical vapor deposition (PECVD) or sputtering. Ongoing research using sputtered a-SiC has shown that it is difficult to achieve a pinhole free layer of SiC. Rather, PECVD using SiH_4 and CH_4 as precursors is capable of yielding impressive, pinhole free SiC films.

Furthermore, implanted a-SiC has shown impressive biocompatibility ([45], [46]). In-

deed, a histology study by Hess and colleagues showed that a 50μm iridium shaft coated with a-SiC implanted in the rabbit cortex for 120 days did not show the usual chronic inflammatory response of macrophage, lymphocyte, monocyte recruited to the insertion site [47].

It is interesting to consider an approach to Dust that would involve constructing the devices on silicon with a silicon carbide encapsulant for a truly chronic implant. A possible process is shown in Appendix C. One of the largest challenges here is ensuring that the PECVD of SiC does not depole the piezoelectric material. In order to have contamination-free films, it is important to deposit at minimum temperature 200°C. This is below the Curie temperature of PZT, but above half the Curie temperature, so it is unclear how the PZT will be affected.
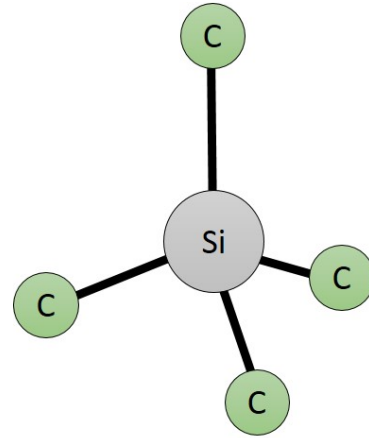
Figure 3.1.: Cartoon of a SiC molecule adapted from [43]. The molecule is tetrahedral with Si-C bond length roughly $1.89\mathring{A}$

3.1.2. CNS Dust

It is important to note that by enabling a chronic, closed-loop BMI system, we are enabling therapies for a slew of neurodegenerative diseases, not just paralysis. In theory, Dust could be used to monitor brain activity to track epileptic activity before it begins or optimize a cochlear implant([48], [49]). The current iterations of Dust are far too large to be placed in the brain, hence we targeted the PNS. However, accessing the central nervous system (CNS) can be handled in two ways:

1. Use of the existing polyimide substrate as a communication platform and connect CNS-compatible electrodes to the substrate

2. General miniaturization of the device

Communication Dust

As it curently exists, the Dust platform could be used as a communication platform. The recording electrodes of the Dust substrate could be bonded or soldered to microwires which can be inserted into the cortex. For this application, carbon fiber (CF) may make an excellent electrode material due to their single-micron scale diameter and similar density to brain tissue. Furthermore, while the insertion force of the dura and cortex is not well characterized, it has been empirically determined that fibers with aspect ratios of up to 1000 are capable of insertion without buckling due to the stiffness of CF. Of course, this stiffness acts as a double-edged sword; due to the small size of CF, handling is very difficult and thus its brittleness can often lead to fracture. Additionally, the impedance of CF is much higher than those of metals, so effective CF electrodes must be functionalized or plated with more conductive polymers [50].

Use of CF electrodes with the current iteration of dust would involve drilling holes in the recording electrode pads of the original substrate and threading the CF through. Silver paste may be used to ensure electrical connection as well as fix the electrodes in place.

While this application would be an excellent proof-of-concept for CNS recordings, it is arguable how much more advantageous Dust as a communication platform may be than a standard EM link. The main advantage of Dust is the ability to obtain deep brain recordings from free-floating sensors. In this case we have wired electrodes which are unable to penetrate deep into the cortex. If we wanted to maintain our use of ultrasound as an information transfer modality, we will have to contend with the the attenuation of ultrasound through the skull. Alongside with the absorption and scattering of the acoustic wave in the bone, there is also a large amount of reflection of the wave at the skull-dura interface due to the large acoustic impedance mismatch [51]. Furthermore, due to the irregularity of bone thickness across the skull, the skull may shift the focal point from its predicted position or even decollimate the transmitted acoustic wave at

frequencies higher than 1 MHz. One possible method to mitigate this is use of a phased array to correct for the distortion; in order to do this, one must first know what the phase correction for each element of the array needs to be, which is arguably just a function of bone thickness. One possible way of determining this could be time-of-flight measurements of the reflected ultrasonic wave between the scalp-skull and skull-dura interfaces - alternatively CT or MRI scans could provide the same information.

Miniaturization of the device

Ultimately, Dust was designed for aggressive miniaturization down to cellular dimensions (tens of microns), which is two orders of magnitude smaller than the existing versions of dust. The first step towards this goal is reduction of the mote by one order of magnitude to sub-millimeter scales. One possible method for this is flip-chip bonding the ASIC to the substrate to reduce the size of the mote to that of the ASIC. In order to do this, a PCB with a footprint matching that of the ASIC is created. Next, small balls of Au/Sn solder are placed on each pad of the ASIC, and the ASIC is "flipped" onto the PCB and heated, causing the solder to reflow and make electrical contact between the ASIC and the PCB. To prevent any possible shorting or damage, the spaces between solder contacts are filled with a dielectric.

The piezoelectric element can then be silver pasted and wirebonded appropriately. Of course, miniturization of the substrate will also result in reduced electrode spacing if we intend to place the electrodes on chip. As found in the previous chapter, electrode spacings of less than 2 mm have substantial signal degradation. As in the condensed board case, we will need to employ a "tail" of some sort which houses a recording pad, while the other recording pad sits on the body of the mote. A possible PCB layout is presented in Figure 3.2

3.1.3. Stimulation Dust

So far we have focused on recording neural activity, but there is a need to create a version of Neural Dust which stimulates neural activity rather than passively record-
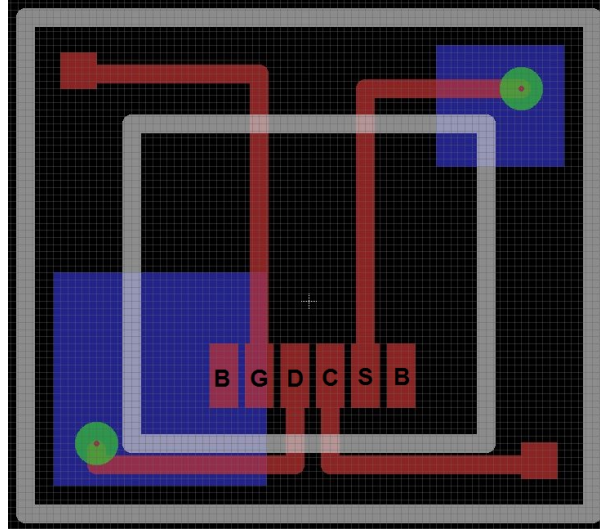
Figure 3.2.: A possible flip-chip compatible PCB design for a miniaturized mote. The overall size is 800μm by 800μm. Traces in red designate the ASIC side, whereas the blue pads designate the PZT coupon side. The recording pads are 50μm by 50μm, but one could be used for tail attachment to overcome electrode separation challenges. As in the current version of dust, the PZT coupon is designed to hang off the substrate in order to have space for wirebonding.

ing. Neuronal stimulation has found uses in breaking seizures [52], feedback in BMI systems [53], and blocking signal transmission in the nervous system [54]. In addition, stimulation is an important element for basic neuroscience applications in order to investigate functional connections between neurons.

Stimulation can be performed electrically, as well as thermally ([55], [56]). Electrically, one can imagine that the simplest method of stimulation would be to charge a capacitor ultrasonically and then upon a trigger (perhaps another piezoelectric element with a different resonance frequency), discharge the stored charge into the body. Thermal mechanisms are quite interesting, as they could potentially incur greater spatial resolution than electrical stimulation [57]. To explain thermal stimulation, one must recall that the cell membrane can act as a capacitor in that it is impermeable to ions and the cell relative to the extracellular environment is at a higher electrical potential. The capacitance of the membrane then becomes a function of the charge distribution (ion distribution) in the extracellular environment, which follows Boltzmann statistics and thus has an exponential depedence on temperature. Temperature changes are thus reflected in membrane

capacitance changes, which have corresponding membrane voltage fluctuations.

To deliver heat, we propose an IR LED could be placed on the mote rather than the ASIC and turned-on via ultrasonically harvested power. Since water is the primary chromophore for IR in the extracellular environment, the optimal wavelengths can be determined by examining the absoprtion spectrum of water for IR wavelengths. Previous work has demonstrated that for the sciatic nerve, the average threshold stimulation exposure for a 2.12μm holmium:YAG laser was 0.32 J/cm^2 while the average ablation threshold was 2 J/cm^2 demonstrating that IR stimulation does not pose a large safety risk in terms of excessive heating. What may be more of a concern, however, is that the bulk aqeuous media most neurons are bathed in may very quickly diffuse the heat transferred by the radiation. It will be crucial to determine how long an IR pulse must be on for a given wavelength and compare that with the thermal diffusivity of extracellular fluid.

3.2. Future non-neural Directions

3.2.1. OncoDust and DosimetryDust

The key feature of the Dust backscatter system is that changes in the environment surround a mote reflects changes in drain-source current. A manifestation of such modulation has been observed in radiation-sensing field effect transistors (RADFETs), in which the threshold voltage of a transistor can be shifted by impinging radiation on the FET [58]. The mechanism by which this occurs is the generation of charge within the gate-insulator layer of a MOSFET. The gate voltage of a MOSFET controls the resistance of the surface channel connecting the drain and source of the FET. By generating charge within the gate insulator, we effectively add an internal offset in the MOSCAP controlling the channel conductivity [59]. This opens up the possibility for Dust as a communication system for detection of radioactive tracers within the body (henceforth referred to as "OncoDust" for reasons that will be explained below) or the detection of radiation impinging onto the body (henceforth referred to as "DosimetryDust"). For

both of these applications, one of the largest challenges is determining how to release the stored charge and restore the I-V characteristics of FET back to its original state.

OncoDust

Cancer treatments have evolved considerably since radiation therapies were developed in 1899 [60]. However, due to the heterogeneity of cell types within a tumor, full removal may not always be possible allowing for distal tumor recurrence. While the mechanism behind this phenomena is still unknown, a possible theory is that tumors are "seeded" by cancer stem cells, which make up a small population of the tumor [61]. Removal techniques may remove the bulk of tumor cells, but leave the cancer stem cells intact, allowing them to become circulating tumor cells. These cells can then form micro-metastases in various locations of the body. Unfortunately, the detection of these micro-metastases is difficult since micro-metastases typically only contain between 10^4 to 10^5 cells, whereas traditional tomography methods require on the order of 10^8 to 10^9 cells to detect tumors. This resolution requirement is due to a large imaging distance and a lack of cell-type specificity resulting in large background noise. Dust motes could provide an interesting solution to this problem because they could be completely implanted millimeters within the tumor-site. To provide a measureable signal, radiolabels tagged onto cancer cells could modulate the threshold voltage of a RADFET, in turn modulating I_{DS} for a constant V_{DS} supplied by an ultrasonic pulse from the interrogator. The variation in I_{DS} as a function of impinging radiation will result in a modulation of the backscatter amplitude from the dust mote.

DosimetryDust

Radiation therapy (RTx) is a common form of treating cancer and tumors using ionizing radiation. Impinging radiation damages the DNA of cancerous tissues leading to cell death. Unfortunately, there is no established method for targeting specific cell-types, which means that healthy tissues are often damaged as a side-effect. To mitigate this, the procedure for radiation therapy is very complex, involving a team consisting of a

doctor, radiologist, and physicist. Together, the team takes an initial CT scan of the patient, obtaining a reference image. Using this reference image, the team designs and simulates an intricate therapy procedure over a number of days or weeks, specifying radiation dose and direction to minimize irradiation of healthy tissue [62]. On each day of treatment, the patient is given an x-ray and the x-ray is compared to the reference image and radiation directions are offset to account for day-to-day variation. Unfortunately, despite the best efforts of the team to properly align the beam, there is no feedback as to what the real radiation profile is inside the body. If the tumor persists after RTx, it is unknown whether the failure is due to improper alignment or cell-type resistance. Thus, the RADFET concept tied together with the dust system may become useful for providing real time dosimetry measurement and feedback. One could imagine a closed-loop system in which feedback from Dust manages the radiation profile of the source allowing more efficient and effective therapies.

3.2.2. GlucoDust

As a final thought on dust applications, we will consider the use of dust for glucose monitoring in diabetic patients. Diabetes is a group of metabolic diseases in which the blood sugar levels are elevated for long periods of time, resulting in dehydration, cardiovascular damage, nerve damage, and more ([63], [64]). Currently there is no cure for diabetes, and those who suffer from the disease must constantly monitor their blood glucose levels, as careful regulation of glucose conditions can control diabetic complications [65]. Conventional glucose monitoring is performed by patients using a lancet to draw blood and running the blood sample through a glucose monitor. This is un- pleasant for patients and purchasing lancets and test strips can become quite costly, since diabetic pa- tients must monitor their glucose levels six to seven times a day. Alternate methods of glucose monitoring attempt to address the issue of repeated needle insertion by creating continuous glucose monitors, but these are either more expensive and still require needle insertion or are non-invasive but less accurate [66]. Here, dust may be able to play a role in continuous glucose monitoring; a chronically implanted dust mote

in which the backscatter is modulated by glucose oxidation, could allow for continuous glucose monitoring just by patching an interrogator with conductive gel over the body.

Electrochemical glucose monitoring has been long implemented with amperometric measurements ([67], [68], [69]), using electrodes coated with enzymes such as glucose oxidase to ensure specificity. Unfortunately, such devices tend to have low device lifetimes - commercially purchased subcutaneous continuous glucose monitors often only have 3-7 day lifetimes [70] due to the instability of the enzyme layer at body temperatures. To counteract this, nonenzymatic probes have been developed. Unfortunately, one of the leading causes for failure of these devices is simply the introduction of foreign bodies into subcutaneous tissue ([71], [72]). The issue of foreign body reponse is similar to the challenge faced in chronic neural interface implantation, so dust - in particular SiC dust, may become a powerful solution.

4. Conclusion

Wireless and chronic neural interfaces are crucial for the effective use of closed-loop BMI in medicine. One method of implementing such a system is Neural Dust, which aims to completely implant tetherless, ultra-miniature, sensor motes with an ultrasonic telemetry system. Presented in this work is a discussion of the assembly process for the first proof-of-concept sensor motes. The design and material challenges are delimited and possible solutions were presented. Two iterations of the device were examined:

1. A 1 mm x 3 mm x 1 mm FR-4 PCB using silver epoxy for die/ASIC attach and Crystalbond for encapsulation.

2. A 0.8 mm x 3 mm x 1 mm polyimide flexible PCB using silver epoxy for die/ASIC attach and medical-grade UV curable epoxy for encapsulation.

Following that, an overview and discussion of possible extensions and variations of Dust in various domains were considered, such as neurostimulation, dosimetry, and glucose monitoring.

There is still much work to do even in just the improvement of the current assembly process. In particular, the encapsulation process is not well controlled as we are simply dabbing epoxy over the device, nor is the encapsulant chronic. We hope to resolve this issue using SiC as an encapsulant, and hopefully that will enable a wealth of Dust applications as described in Chapter 4. Additonal work will be required, of course, particularly for CNS recordings. A fabrication process for cellular-scale Dust must be developed in order to actualize the dream of 1000s-10,000s of free-floating Dust motes in the brain. Furthermore, this work does not include any discussion of mote interrogation

or implantation. Transducer arrays may enable effective beamsteering to interrogate multiple implanted motes and possible methods of implantation may involve dissolvable tethers such as a silk-based adhesives [73] which may allow the dust mote to be deeply inserted in the brain on a microneedle and freed by dissolving the adhesive with artificial cerebrospinal fluid.

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A. Building Neural Dust: A Step-by Step Guide

This chapter will, in full detail, demonstrate the assembly of the current Neural Dust mote described in this report. Before beginning, ensure that you have all the components necessary for assembly (i.e. PCBs, ASICs, diced PZT, etc.) and have put on a pair of gloves to prevent oils from the skin or other debris to dirty the PCBs or dies.

A.1. Prepare sample holder slides and mix silver paste

Before beginning to work with the PCBs, ASICs, or PZT coupons, prepare two sample holders for the dust boards. To do so, simply take two glass slides (3 mm x 1 mm x 1 mm slides work well) and put a strip of double-sided tape on the slide lengthwise. The tape will be used to fix the dust motes in place so that we can perform the rest of our steps. On one of the slides, also add a piece of Kapton tape (3M) sticky-side up on top of the double-sided tape. This slide will be the slide used for curing as the high temperature of the cure can cause problems with the adhesive on the double-sided tape.

Next, mix a small amount of silver paste by weighing out a 1:1 ratio of part A and part B in a weighboat. A large amount of silver-epoxy is not needed for the assembly process. Shown below is roughly 10g of epoxy (5g of each part) which is more than enough for three boards. Note that the mixed-silver epoxy has a shelf life of two weeks if placed at 4°C. So leftover epoxy can and should be refridgeratorated when not in use. Additionally, older epoxies (several days to a week) tend to be slightly more viscous than fresh epoxy which can make application easier.

Figure A.1.: Left: the two components of silver epoxy Right: The silver epoxy on a
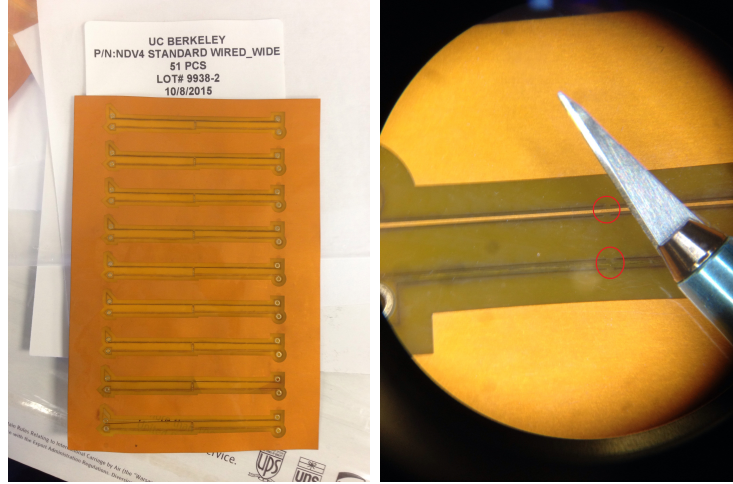weighboat. Pictured is roughly 10g.

Figure A.2.: Left: A panel of PCBs from AltaFlex Right: A zoom-in on the tabs (circled red) that need to be cut to singulate PCBs.

A.2. Remove PCBs from panel

The neural dust substrates come panelized (Fig.A.2) and will need to be removed. Each board is connected to the panel at several attachment points on the test leads and vias - these attachment points can be cut using a micro-scalpel (Feather Safety Razor Co., Osaka, Japan).

Once the PCB has been singulated, using carbon-fiber tipped tweezers or ESD plastic tweezers, place the singulated PCB onto the high-temperature sample holder.

A.3. Attach the die

The diced/thinned die are shipped on dicing tape, which can make it tricky to remove the die. In order to reduce the adhesion between the die and tape, it can be helpful to deform the tape. Using carbon-tipped or ESD plastic tweezers, gently press the tape and work the tweezers in a circular motion around the die (Fig.A.4).

To check if the die has been freed, gently nudge the chip with the tip of the tweezers. If the die does not come off easily, continue to press into tape surrounding the chip. Once the chip has come off, carefully place the chip onto the high-temperature sample holder next to its board. It is advisable to bring the sample holder to the chip rather than the other way around so that the chip is not in transit. Care must be taken in this step to avoid losing or damaging the die. Never force a die off the tape, as excessive force can cause a chip to fly off the tape.
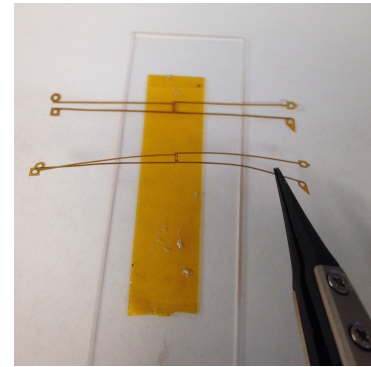

Figure A.3.: Placing the PCB using carbon-fiber tipped tweezers onto the high-temperature sample holder (kapton tape on double-sided tape).

Figure A.4.: Left: Dies as they appear after grinding. Right: Zoom in on die removal. Using tweezers to flex the dicing tape membrane can help gently lift dies off the tape.
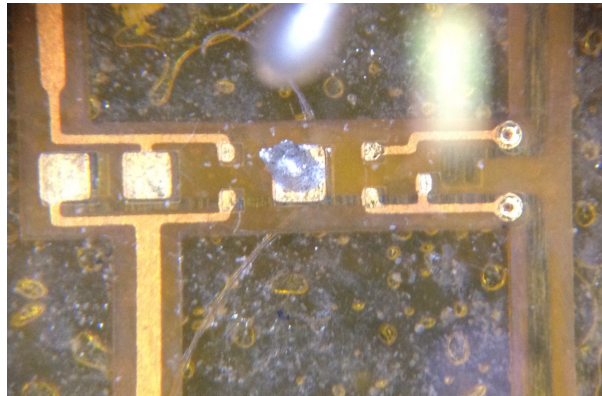

Figure A.5.: A small drop of silver epoxy applied by sewing needle to the ASIC pad

Next, attach the die using silver epoxy. Under a microscope, use a pin or something equally fine to apply a small amount silver epoxy to the CMOS pad on the PCB.

In this step, it is better to err on the side of too little epoxy than too much epoxy since more silver paste can always be applied, but removing silver paste is non-trivial. Small amounts of uncured epoxy can be scraped away with the same tool used for application, just ensure the epoxy has been wiped off the tool.

Once the epoxy has been placed on the pad, the ASIC can be placed onto the epoxy. Due to a CAD error, some of the chips have been reflected (Fig.A.6). It is important to take care that chips which are reflected have been oriented the correct way on the board to ensure no wires need to cross during wirebonding.

Once the ASICs have been situated on the boards correctly, the silver epoxy can be cured by placing it into an oven at 150°C for 15 minutes. Note that different temperatures can be used if needed - see Fig.2.11 for details. After the silver epoxy has been cured,
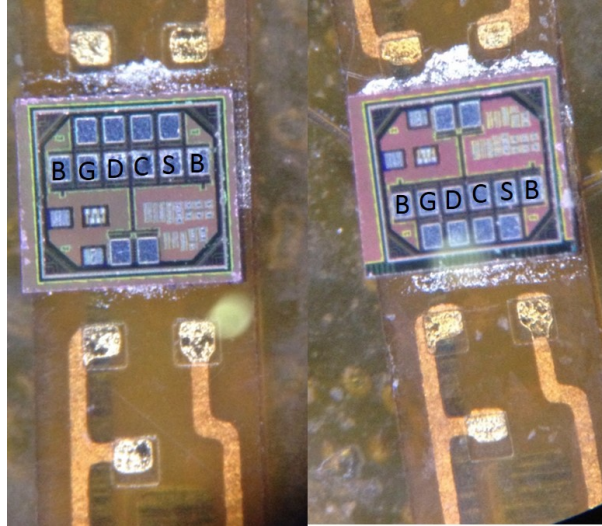
Figure A.6.: An image showing a regular die and a reflected die and their proper orientations on the PCB

double-check adhesion by gently pushing on each die. If the die moves, a second coat of silver epoxy will be needed.

A.4. CMOS wirebonding

To prepare for wirebonding, move the devices from the high-temperature sample holder to the regular sample holder. This change is necessary because the adhesion of double-sided tape is stronger than that of the Kapton tape so wirebonding will be made easier.

A piece of double-sided tape should be good enough to affix the sample holder to the wirebonder's workholder. It is best to ensure that the workholder has not been previously covered with double-sided tape so that the test leads do not get accidentally stuck to anything. If necessary, clean-room tape can be used to provide additional clamping of the sample holder (Fig.A.7).

Ensure the wirebonder is in good condition by making bonds on the provided test-substrate using default settings. This step is critical as a damaged wedge will not bond well and effectively just damage the ASIC pads. Forward bonds (first bond on the die, second bond on the substrate) should be made in the following order:

Figure A.7.: The slide taped down to the workholder. A piece of double-sided tape is underneath the slide, and the top and bottom of the slide are fixed with clean room tape.

Table A.1.: Westbond 7400B Al Parameters for ASIC

Bond #	Power	Time
1 (ASIC)	420	40 ms
2 (Substrate)	490	40 ms

1. Gate

2. Bulk

3. Center

4. Drain

5. Source

While it is not critical that the bonds be made in this order, this order minimizes the number of substrate reorientations and prevents accidental damage to the bonds due to the bondhead. Small angle adjustments of the workholder can be made to facilitate bonding; it is imperative that the bond be as straight as possible. In the case that the foot of the second bond lifts from the substrate, changing the number of bonds to one and bonding the foot again may help. If proper adhesion cannot be made, a potential solution is to connect the foot of the bond and the substrate using silver epoxy(Fig.A.8). Additionally, shorts caused by two bond-feet touching can be resolved by very carefully cutting away the bridging metal using a microscalpel.
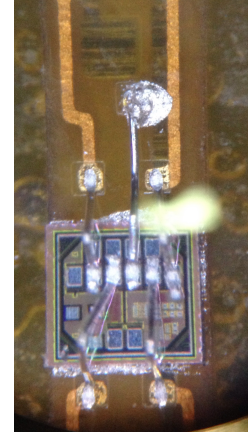
Figure A.8.: An example showing a silver-paste fix for a wirebond lifted off the gate pad.

Known working bonding parameters can be found in Table A.1. These parameters are simply guidelines and should be modified as necessary. Needing excess power (greater than 490) is typically indicative of a problem: substrate fixing (both PCB to glass slide and CMOS to PCB), wedge condition, and pad condition should all be checked. In the case of pad condition, damaged pads due to previous wirebonding attempts will usually require higher power - in some cases, the devices are salvageable, but failed attempts to bond with power higher than 600 usually results in too much damage to the pads for good bonding.

Post-wirebonding, the device should undergo electrical testing to ensure proper bonding(Fig.A.10). If using a type 1 die, the I-V characteristics should be roughly as follows:

If the I-V characteristics do not seem correct, a valuable troubleshooting method is checking the resistances between the drain and center, source and center, and drain and source. If the die is working properly, one should expect roughly 90 kΩ resistances
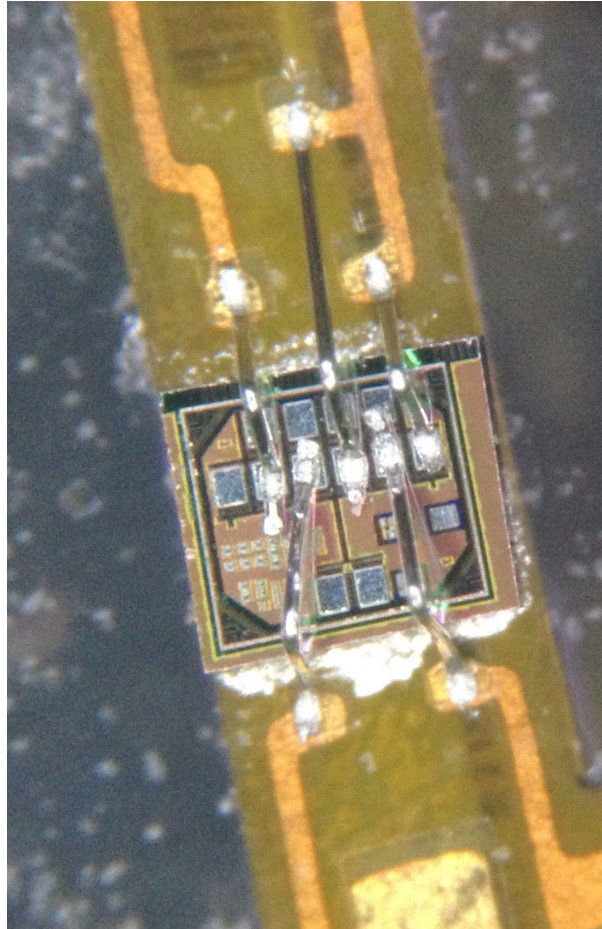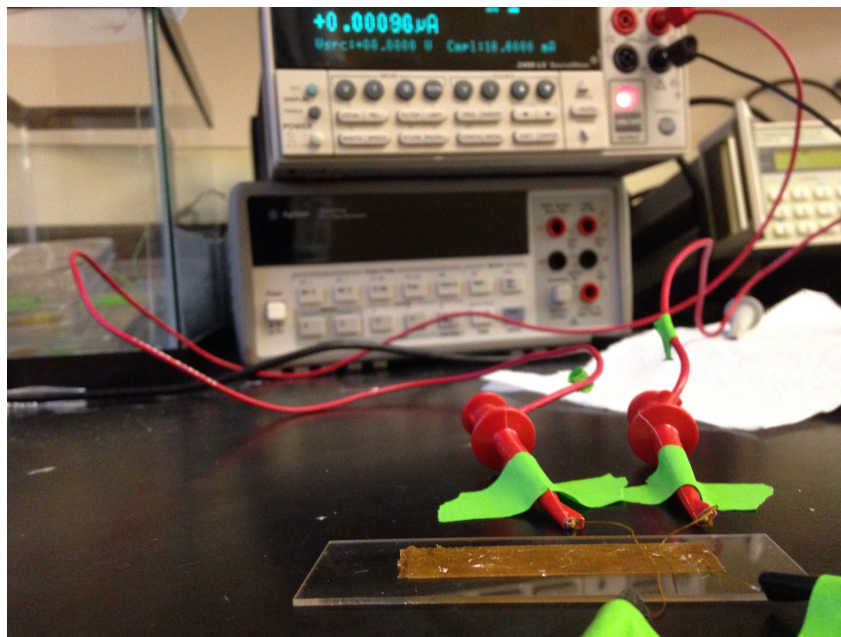
Figure A.9.: The wirebonded ASIC

Figure A.10.: Electrical test set up of the test die. Tape is used to prevent the cables from accidentally pulling the leads off or displacing the mote.

Table A.2.: Typical I-V characteristics for Type 1 Die under $V_{ds} = 0.1\ V$

V_{gs}	I_{ds}
0 V	0.5 μA
0.1 V	0.74 μA
0.2 V	10.6 μA
0.3 V	51.4 μA
0.4 V	0.192 mA
0.5 V	0.39 mA
0.6 V	1.14 mA
0.7 V	1.55 mA
0.8 V	1.85 mA

between the drain and center and source and center, and roughtly 180 kΩ between the drain and source.

A.5. PZT attach

After confirmation that the FET is connected properly, the PZT coupon should be attached. This is done in a similar fashion to attaching the ASIC: place a dab of silver epoxy using a sewing needle on the appropriate pad. It is best to put the epoxy dab on the back edge of the pad (towards the end of the board) since the PZT coupon will not be centered on the pad, but pushed back so that the coupon hangs off the board. Keep in mind that the polarity of the PZT coupon has a small effect on its efficiency. To determine whether or not the coupon is in the correct position, check if the bottom face is larger than the top face(Fig. A.11). Due to the path of the dicing saw, the bottom of the coupon is slightly larger than the top of the coupon. Thus, the edges of the bottom face can be seen from a topdown view, then the coupon has been placed in the same orientation as it was when the disk was diced.
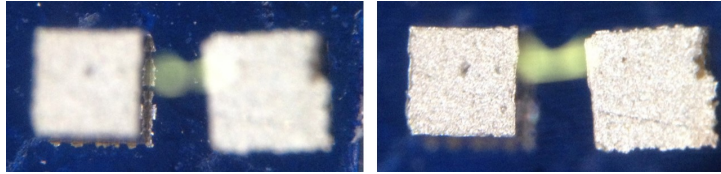

Figure A.11.: A side-by-side copmarison of PZT coupons. The left coupon is placed in the same orientation it was cut in. The right coupon is upside-down. Left: Image focused on the bottom of the PZT coupon to bring the "rough edges" due to dicing into focus. Right: Image focused on the top of the PZT coupon so that the clean edge can be seen.

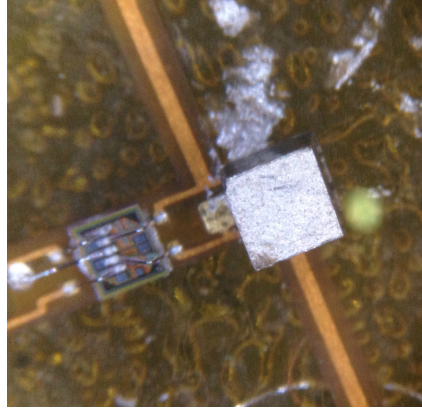Following this step, the board should appear as in Figure A.12.

Figure A.12.: The mote after PZT attach and prior to PZT bonding.

Table A.3.: Westbond 7400B Al Parameters for PZT

Bond #	Power	Time
1 (PZT)	390	40 ms
2 (Substrate)	490	40 ms

A.6. PZT wirebonding

Wirebonding the PZT is done in a similar manner to the ASIC (forward bonding the PZT to the PCB). However, one crucial change is that the drain and source vias should be grounded. There is an earth ground port (Fig A.13) next to Westbond which can be accessed via a banana connector. As a guideline, the parameters shown in table A.3 have been known to work.

A successful bond may require several attempts depending on how well the PZT coupon is attached to the substrate. The more attempts that are made, the worse the mechanical structure of the PZT becomes (the silver coating will become damaged) so it is best to try to very quickly optimize the process. Bonds that fail due to foot detachment generally imply not enough power. Bonds that fail due to the wire breaking at the foot generally imply too much power.
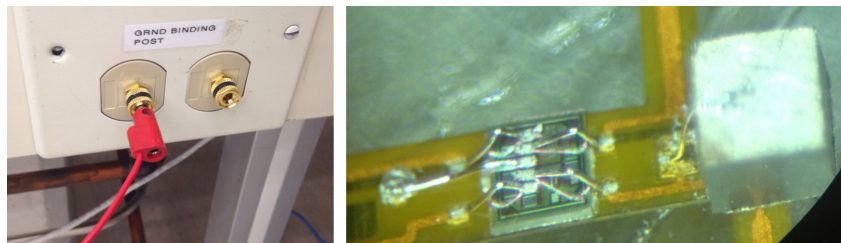

Figure A.13.: Left: The earth ground port next to Westbond. Right: The wirebonded PZT

After a successful bond is made, it is always good to do another electrical test to ensure that bonding the PZT has not damaged the ASIC.

Figure A.14.: Top left: the wire spool and cut test wires. Top right: A partially uninsulated wire. The melted coating forms a ball as it recedes. Bottom: The dust mote after leads have been soldered to the vias.

A.7. Wire attach + Encapsulation

As a final step, we solder test wires to the vias and encapsulate the device. The test wires are 3 mil silver wires. Note that these wires are insulated; the insulation can be removed by putting the wire close to a flame (not in the flame) and watching the plastic melt and recede.

After soldering wires, the device can now be encapsulated. The encapsulant is OG116-31 medical-grade UV curable epoxy and should be dispensed using a sewing needle. An effective method is to put a large drop of epoxy over the PZT coupon and a large drop over the ASIC. Using a clean needle, push the droplet over the board so that the entire topside of the board is coated. The epoxy should wet the board, but not spill over due to its surface tension. Once the main body of the board is coated, the vias should also be coated, as well as the side faces of the piezo. The board can then be cured in a UV chamber for roughly 5 minutes. It has been found that the test wires can occasionally contact something in the UV chamber and short the ASIC. Thus, prior to putting the board in the chamber, it is good to wrap the wires down or place it on some tape in order to isolate them from any chamber surfaces (Fig. A.16).

Following curing, the backside should be coated. In particular the exposed PZT coupon which hangs over the board as well as the backside of the test vias and the two vias on the backside of the board which connect the electrodes to the topside of the board (Fig. A.15. This part can be a little tricky due to the small space between the backside vias and the electrodes, so it is best to start with a very small amount of epoxy and place it near the edge of the board, then drag the epoxy up towards the vias. The backside of the board should be cured in the same manner as the topside. Once the board is fully encapsulated, a final electrical test should be done, and upon passing, the Neural Dust sensor mote is now complete!
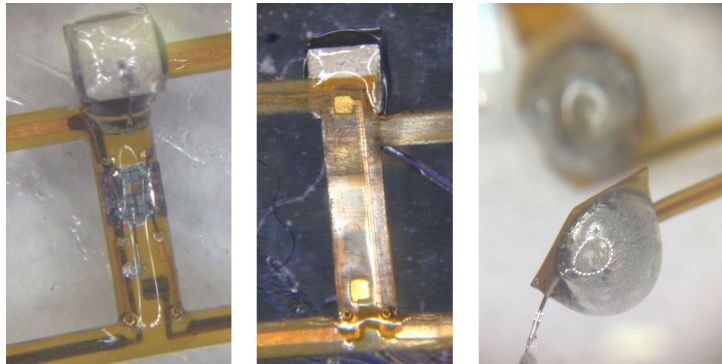
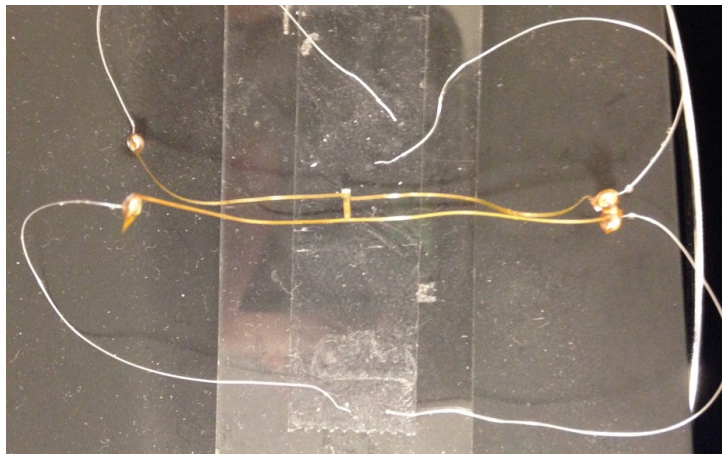Figure A.15.: Encapsulation of the top, bottom, and test vias.

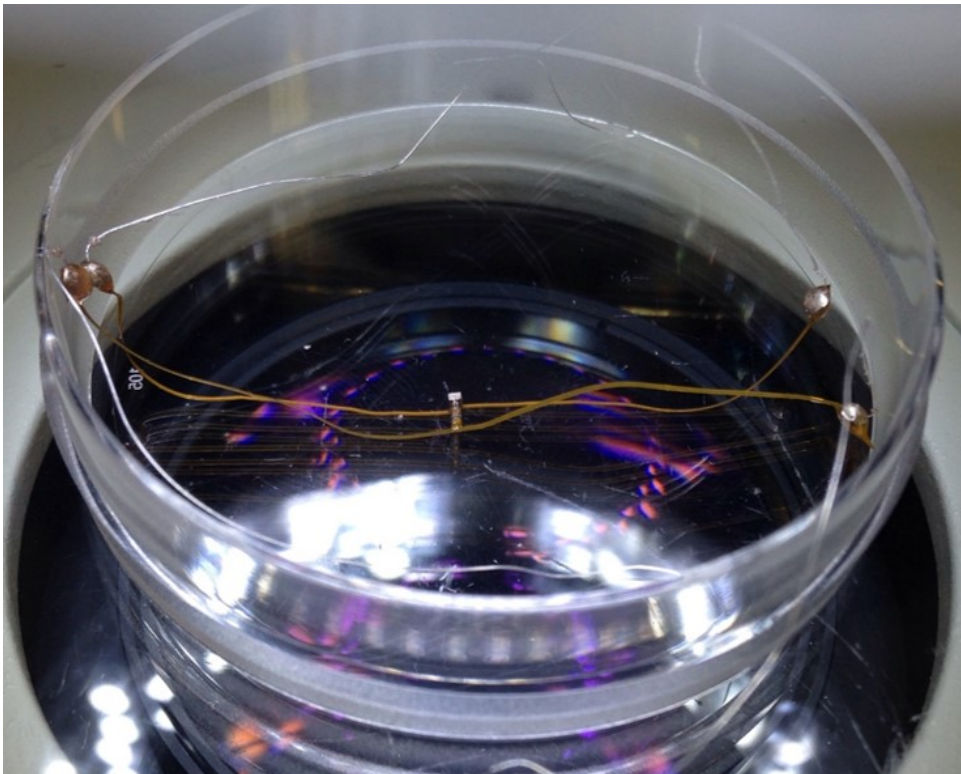Figure A.16.: One way of keeping the wires contained so that they do not contact the inside of the UV chamber.

Figure A.17.: The assembled Dust mote in a 6cm petri dish
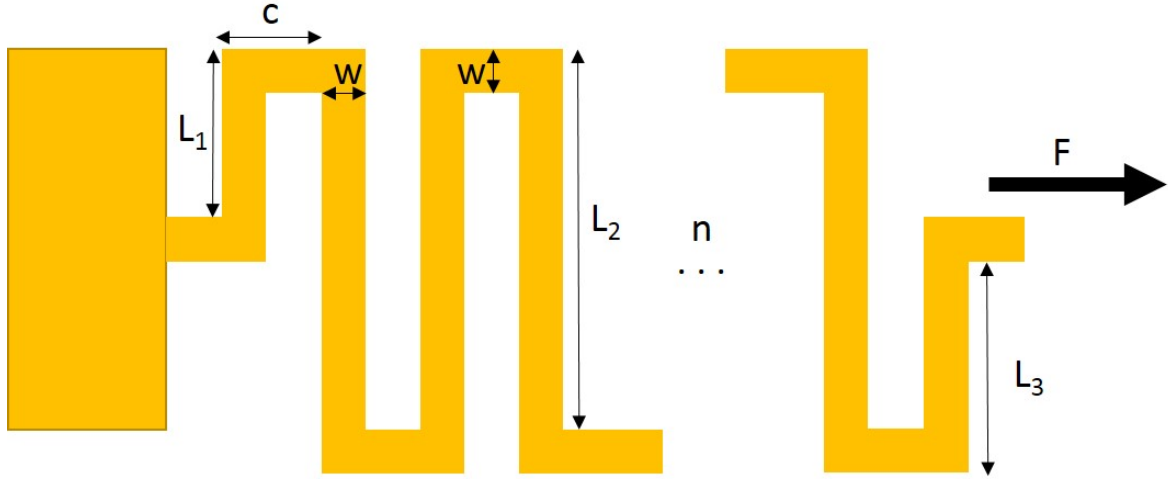
B. Serpentine Trace Design

Figure B.1.:

Consider the general example shown in Fig.B.1. Here, each connector beam is of length c and each cantilever is of length L_2 except for the first and last cantilevers which are of length L_1 and L_3 respectively. All beams are of width w and thickness t. The axial stiffness of the connector beams can be given by:

$$k_{connector} = \frac{wtE}{c}$$

This can be derived via the definitions of stress and strain, $\sigma = \frac{F}{A} = \epsilon E$ where $\epsilon = \frac{\Delta L}{L}$. The bending stiffness of the cantilevers can be generalized as:

$$k_{cantilever} = \frac{Etw^3}{4L^3}$$

Which can be derived using Euler-Bernoulli beam theory. Let us assume that the axial stiffness of the connector beams is much greater than that of the cantilever such that we can ignore the stretching of the connector beams. The compound stiffness of cantilevers in series can be calculated in the same way the total resistance of resistors in parallel can be computed. Given n meanders, we write:

$$k_{serpentine} = \left(\frac{1}{k_1} + \frac{n}{k_2} + \frac{1}{k_3} \right)^{-1}$$

$$\Rightarrow = \frac{4(L_1^3 + nL_2^3 + L_3^3)}{Etw^3}$$

To calculate how much our new flexure will be allowed to stretch, we must consider the ultimate tensile stress (UTS) of the polyimide, which determines how much the polyimide can elongate before tearing. A rigorous analysis is difficult due to the behavior of material under large deformation, but an analysis assuming small angle bending can give us a starting point for design. First, let us determine the maximum strain in the beam assuming pure bending (only transverse loads). The strain of the beam is non-uniform through the thickness of the beam, as it is a metric of how much a transaxial slice of the beam is elongated versus its neutral axis. As it turns out, this strain is linear with position:

$$\epsilon = \frac{z}{\rho}$$

Where z is the distance of the of the "slice" from the neutral axis and ρ is the radius of curvature. Thus the largest strain will be found at the surface of the beam - assuming the neutral axis can be found in the middle of the beam, the maximum strain is:

$$\epsilon_{max} = \frac{t}{2\rho}$$

From Euler-Bernoulli beam theory, the radius of curvature of a bent beam is simply the inverse of the second order derivative of the beam's displacement as a function of distance along the beam:

$$\frac{1}{\rho} = \frac{d^2r}{dx^2} = \frac{12F}{Etw^3}(L - x)$$

Where $r(x)$ is the displacement of the cantilever using the fixed-end of the beam as the origin. The maximum strain then is also found at the fixed-end of the beam such that:

$$\epsilon_{max} = \frac{6L}{Etw^2}F$$

Since stress and strain are related by the Young's modulus in the elastic (small bending) regime we can write:

$$\sigma_{max} = \frac{6L}{tw^2}F$$

We know that for a desired flexure displacement Γ, the force required is:

$$F_\Gamma = k_{serpentine}\Gamma$$

Thus to determine the necessary cantilever dimensions we must satisfy:

$$\sigma_{max} = UTS_{polyimide} = \frac{6Lk_{serpentine}\Gamma}{tw^2}$$

C. MATLAB Code for Neural Dust Testbed seal test

```
%----------------------------------------------------------------------%
%Script which communicates with Keithley 2400 for Neural Dust testing   %
%                                                                       %
%Written by Konlin Shen                                                 %
%Last updated:2/17/16                                                   %
%----------------------------------------------------------------------%

function [i,v,r,t]=testbedIV
%initialize output variables
i=[];v=[];r=[];t=[];

%get hardware info
keithley=instrhwinfo('gpib', 'ni');

%create GPIB object
fObj=eval(keithley.ObjectConstructorName{1});

%connect to keithley
fopen(fObj);

%reset keithley to defaults
fprintf(fObj, '*RST');

%ask Keithley to measure resistance and autorange
fprintf(fObj, ':SENS:FUNC "RES"');
fprintf(fObj, ':SENS:RES:MODE AUTO');
fprintf(fObj, ':SENS:RANG:AUTO');

%set timestamp to be relative time
fprintf(fObj, ':TRAC:TST:FORM DELT');

%start outputting
fprintf(fObj, ':OUTP ON');

%sentinel
stop=0;

%set figure properties
hFigure=figure('KeyPressFcn',@stopfunc);
```

```matlab
hLine=plot(nan);
set(hLine,'Marker','.','MarkerSize',10,'LineStyle','-');
hold on;
xlabel('Time (s)');
ylabel('Resistance(\Omega)');

%pull and display data
while ~stop
    dataString=query(fObj, ':READ?');
    stringCell=strsplit(dataString, ',');
    v=[v,str2double(stringCell{1})];
    i=[i,str2double(stringCell{2})];
    r=[r,str2double(stringCell{3})];
    if isempty(t)
        t0=str2double(stringCell{4});
        t=0;
    else
        t=[t,str2double(stringCell{4})-t0];
    end

    set(hLine,'XData',t,'YData',r);
    drawnow
    stop
    pause(0.001);
end

%reset buffer
fprintf(fObj,':TRAC:CLE');
fprintf(fObj,':OUTP OFF');
fclose(fObj);

    function stopfunc(hFigure,event)
        stop=1;
    end

end
```

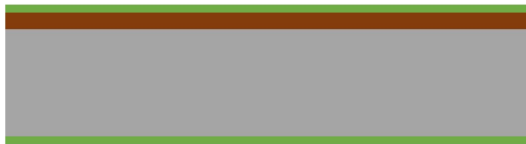# D. Possible process flow for SiC neural dust
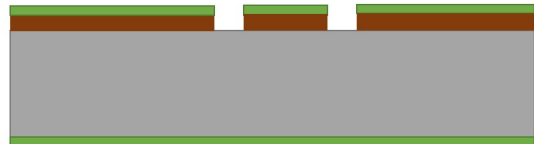
1. Start w/ SCS

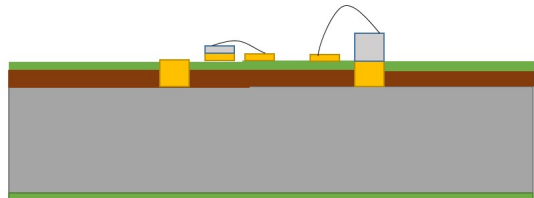2. Spin PI layer

3. PECVD a-SiC
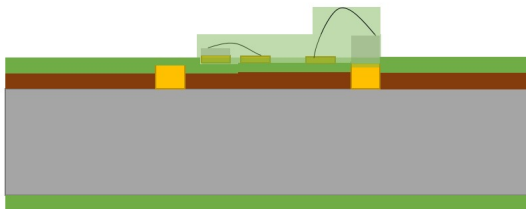
4. RIE openings for electrodes

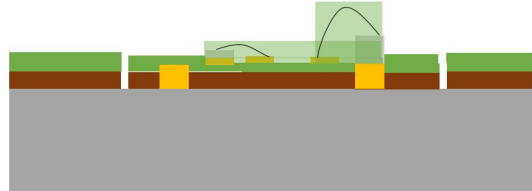5. Evaporate ruthenium and plate gold onto electrode sites

6. Die/Piezo attach and wirebond

7. PECVD a-SiC encapsulation

8. RIE emboss topside, remove film from backside

9. Dissolve wafer (TMAH)