Design and Characterization of Ferroelectric Negative Capacitance

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by

Korok Chatterjee

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Abstract

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Because of the thermal distribution of electrons in a semiconductor, modern transistors cannot be turned on more sharply than 60 mV of gate voltage for an order of magnitude increase in drain current, the so-called "Boltzmann tyranny." This results in an inability to reduce supply voltage, increasing power dissipation in advanced complementary metal-oxide-semiconductor (CMOS) technologies, which threatens the continuation of exponential transistor scaling, also known as Moore's Law. For this reason, there has been a push in the device research community to invent novel steep swing devices. Negative capacitance in ferroelectric materials was proposed in 2008 by Salahuddin and Datta to provide voltage amplification without needing to design a totally new device. A negative gate capacitance would step-up the applied gate voltage at the semiconductor channel, causing the surface potential to rise faster than the gate voltage, lowering the subthreshold slope below 60 mV/decade. In this work, we attempt to characterize the charge-voltage characteristics of ferroelectrics biased into the negative capacitance regime. Although negative capacitance was experimentally demonstrated in 2010, significant challenges have remained to the practical realization of negative capacitance field-effect transistors (FETs).

First, we investigate negative capacitance in an isolated ferroelectric capacitor, and show that the negative capacitance states can be directly observed during switching. Careful analysis of the switching dynamics and phase-field modeling show that the signature of negative capacitance arises from the accelerating growth of domain walls, when an increasing volume fraction of the ferroelectric is depolarized. Although this offers insight into the origins of negative capacitance and help to establish its existence scientifically, it does not address the problem of design. A primary concern is the speed of polarization response, which should be on the order of 1 picosecond or less in order to maintain circuit performance. By analyzing the electromagnetic absorption spectrum of hafnium oxide, the primary candidate for CMOS integration, we are able to estimate the intrinsic delay time as being on the order of 270 fs. Next, in order to maximize the amplification and provide adequate margins for hysteresis-free operation, it is necessary to understand how coupling of the ferroelectric material to the interfacial oxide and semiconductor affects its behavior, and to be able

to predict what values of negative capacitance will be realized for a certain material and geometry. This is the problem of capacitance matching, which we aim to solve by using the underlying transistor itself as a charge sensor. By calibrating the drain current to the surface potential in reference devices, we may ascertain the characteristics of the ferroelectric in the negative capacitance devices. This is first carried out with an epitaxial ferroelectric capacitor externally connected to the gate of pre-fabricated Fin-FETs. Following this, we describe the development of an in-house fabrication process using silicon-on-insulator substrates, which allows for simple and efficient process flows. Then, we describe the characterization of these devices, including quasistatic and low-frequency current-voltage (I-V) and capacitance voltage (C-V) measurements, a fast pulse-gated I-V measurement, and an excursion into the memory characteristics of our fabricated FETs. Finally, we discuss efforts to build a computational model of our devices from which we can extract the ferroelectric characteristics needed for predictive design.

"With four parameters I can fit an elephant, and with five I can make him wiggle his trunk." –John von Neumann

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Chapter 1

Introduction

1.1 Motivation: Power Dissipation in CMOS Electronics

The Rise of the Electronic Age

Few inventions in human history have been as transformative as the integrated circuit. In the span of half a century, electronics has come to dominate virtually every aspect of modern life. When Shockley, Bardeen, and Brattain invented the transistor in 1947, science fiction writers and futurists were already fervently anticipating what has since come to fruition - smartphones, space flight, artificial intelligence, and guided missiles [1]. However, the dream was stalled by the so-called "tyranny of numbers," the seemingly insurmountable cost and reliability issues arising from needing to wire together a large number of discrete components. In 1958, Jack Kilby working at Texas Instruments proposed and demonstrated the first prototype of a monolithically integrated circuit. Soon afterwards, Robert Noyce at Fairchild Semiconductor devised the prevailing solutions to the problems of device isolation and metallization, and the first integrated circuits went on the market in 1961. Spurred by investment from NASA and the military, critical production mass was reached, and by 1964 costs had dropped enough to make mass-scale commercialization possible [2].

Powered by Moore's law [3], the exponential growth in the doubling of the number of transistors per dollar roughly every two years, total computational capacity has exploded. The internet has enabled near-instant communication across the globe and aggregated a vast compilation of human knowledge, removing almost all barriers to information. The compactness of electronic systems has allowed for distribution on a huge scale, the so-called "internet of things" (IoT). We can now monitor the structural integrity of concrete structures, seismic and atmospheric activity in remote locations, toxin and nutrient concentrations in industrial agricultural systems, and the glucose levels in our own blood. 1.1 summarizes the history of microprocessor performance metrics. This surge has been accompanied by the proliferation of computers for personal entertainment and communication, large-scale data

processing, and scientific computing. High-energy particle physics, genomic sequencing, modern drug design, and autonomous vehicles would all be impossible without the firehose of high performance digital logic. The economic impact is commensurate. IoT alone is estimated to become a $6.2 trillion industry by 2025 [4]. Semiconductor manufacturing in just the last 20 years has nearly quadrupled its monthly revenue from $10 billion to $38.7 billion [5]. The pervasiveness of electronics in modern life is so extreme that its impact is comparable to that of agriculture or industrialization.

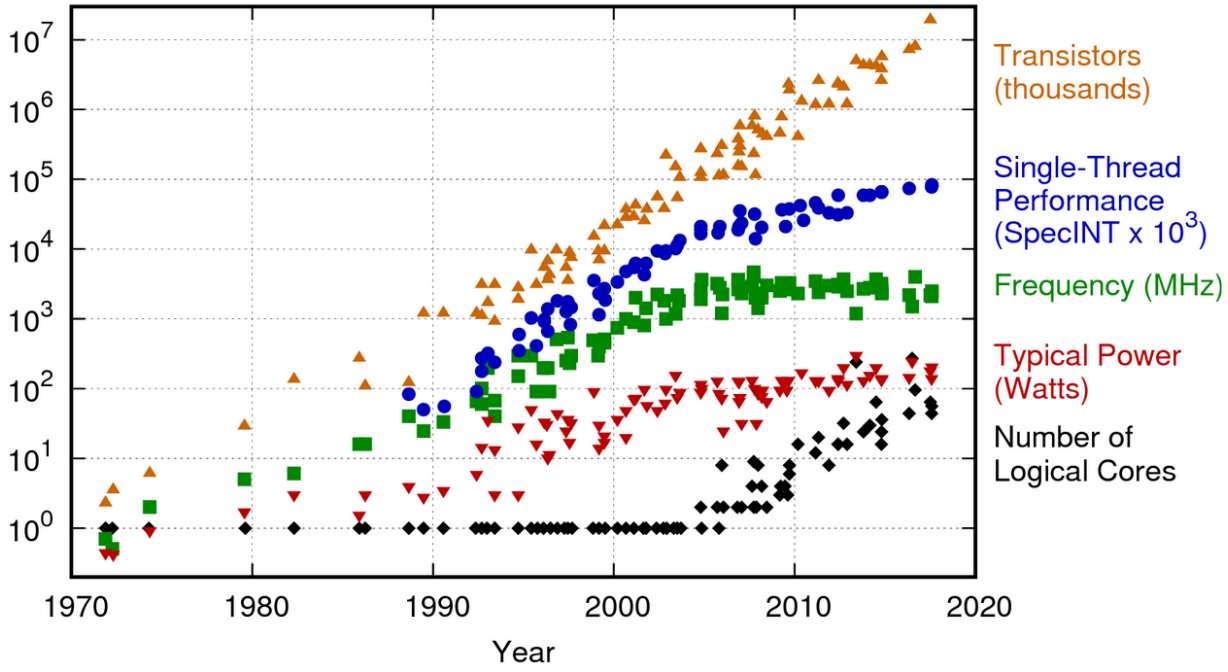

Figure 1.1: Industry trends for microprocessors over the last 42 years. Taken from [6].

The Boltzmann Tyranny

In 1974, Robert H. Dennard with others published a landmark analysis on the scaling of characteristics and fabrication requirements with continued reduction of the physical dimension of metal-oxide-semiconductor field-effect transistors (MOSFETs) [7]. Almost all modern processors are constructed using the complementary metal-oxide-semiconductor (CMOS) platform; MOSFETs are the workhorse of modern computing. The central result of this analysis for device characteristics is shown in 1.1. As long as Dennard scaling holds, the per stage delay scales with the physical dimension and the power density remains constant. This means the clock frequency can be increased with scaling, as is seen in the first part of 1.1, further amplifying the increase of computational throughput with technology generation. By the mid to late 2000s, increased off-state leakage had increased power dissipation

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance ϵA/t	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Table 1.1: Dennard scaling results for circuit performance. Taken from [7].

to the point that threshold voltage scaling and thus also frequency scaling were no longer possible [8]. To cope with this lack of scaling, circuit designers have made innovations at the architecture level, employing parallel processing and a larger number of cores per processing unit. The end of Dennard scaling has seen the rise of power dissipation as a critical problem which threatens the progress of digital logic performance [9].

The root of this problem is the statistical distribution of electrons in the semiconductor. In a MOSFET, the gate is capacitively coupled to the channel, where it populates carriers by changing the surface potential Ψ_S [10]. The Fermi-Dirac distribution can usually be approximated by a Boltzmann distribution, so the inversion charge density, and thus the subthreshold source-drain current, is proportional to $exp\{q\Psi_S/k_BT\}$, where q is the electron charge, k_B is Boltzmann's constant, and T is the absolute temperature. In the case where the gate has perfect electrostatic control over the channel, a factor of 10 increase of drain current requires 60 mV of gate voltage at room temperature. Thus, in order to maintain a certain ratio of on-current to off-current, the operating voltage must be held constant. This limit of 60 mV/decade on subthreshold slope is termed the "Boltzmann tyranny." Without changing the physical principles of operation behind the MOSFET, this limitation cannot be overcome. From this the impetus to "reinvent the transistor" was born [11].

A number of solutions to Boltzmann tyranny have been proposed. Nanoelectromechanical (NEM) relays, tunneling field-effect transistors (TFETs), nanomagnetic logic, resonant body transistors, and field-induced phase transition switches are all being investigated as alternatives to conventional FETs [9]. All of these approaches use some novel physical mechanism to control the conductance between two terminals. In addition to these exotic devices, it was proposed in 2008 by Salahuddin and Datta [12] that a negative differential gate capacitance in a MOSFET could amplify the surface potential relative to the gate voltage, bringing the subthreshold slope below 60 mV/decade thereby reducing the operating voltage, all without having to invent a new device.

The contention is that negative capacitance can be obtained by using a ferroelectric material as a gate dielectric. The depolarizing field from the semiconductor capacitance

drives the ferroelectric material into a locally unstable state where $\partial Q/\partial V$ is negative. This concept is elaborated subsequently.

1.2 The Case for Ferroelectric Negative Capacitance

Why Negative Capacitance?

To illustrate how negative capacitance can lower the subthreshold slope below 60 mV/decade, it is useful to consider a MOSFET as a simple capacitive divider, as shown in 1.2. V_G is the applied gate voltage, C_{ox} and C_S are the oxide and semiconductor capacitances, respectively. We acknowledge that this is a simplistic model. Fringing field, source-channel, drain-channel, and other parasitic capacitances are lumped into the quantity C_S. A MOSFET is a four-terminal device, and a comprehensive model needs to consider the full 4×4 capacitance matrix [13]. Nevertheless, this simple model is valid in many cases and yields insight into the basic principle of operation of an NCFET. Noting that the capacitors are in series, they must share the same charge Q. Straightforward calculation shows that Ψ_S is related to V_G by 1.1.

$$\Psi_S = \frac{C_{ox}}{C_{ox} + C_S} V_G \tag{1.1}$$

Because in general capacitors are nonlinear, it is more useful to use the differential relationships between quantities, which we assume throughout this text ("capacitance" refers to differential capacitance, "amplification" to differential amplification, etc., unless explicitly stated otherwise. The relationship between surface potential and gate voltage is commonly termed the "body factor" denoted by m [12], and is given by:

$$m^{-1} = \frac{\partial \Psi_S}{\partial V_G} = (1 + \frac{C_S}{C_{ox}})^{-1} \tag{1.2}$$

Subthreshold slope (SS) is defined as $\partial V_G / \partial log_{10}(I_D)$, which is expanded in 1.3.

$$SS^{-1} = \frac{\partial log_{10}(I_D)}{\partial V_G} = \frac{\partial log_{10}(I_D)}{\partial \Psi_S} \frac{\partial \Psi_S}{\partial V_G} = \frac{1}{log(10)} \frac{q}{k_B T} \frac{1}{1 + C_S/C_{ox}} \tag{1.3}$$

Now it is manifestly apparent from the functional form of m and SS that a negative oxide capacitance amplifies the surface potential relative to the gate voltage, lowering the body factor below m, and thus the subthreshold slope below 60 mV/decade. One can also calculate the total equivalent capacitance seen from the gate $C_{eq}^{-1} = C_{ox}^{-1} + C_S^{-1}$. In the case of negative C_{ox}, C_{eq} is larger than C_S, whereas for positive capacitors in series the equivalent capacitance is always lower than each of the individual capacitors. Negative capacitance can be understood to provide capacitance enhancement - less voltage is required to bring in a given amount of charge. This results in a negative differential voltage on the negative capacitor and a boosting of the internal node voltage, which, for a MOSFET can bring the

subthreshold slope below the Boltzmann limit. In principle there is no limit on how far the subthreshold slope may be lowered.

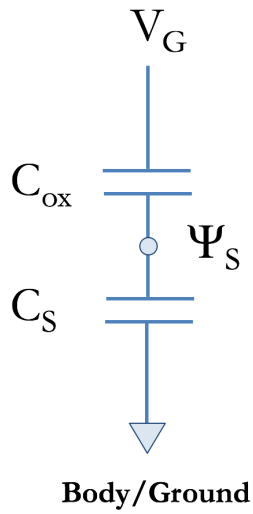

Figure 1.2: Simplified depiction of a MOSFET as a capacitive divider.

It is worth noting that an isolated negative capacitance is inherently unstable. Capacitance is normally defined as $\partial Q/\partial V$, but it may equivalently be defined with respect to the internal energy U. In electrostatics, $dU = V\ dQ$, so that capacitance can be defined as $C = (\frac{\partial^2 U}{\partial Q^2})^{-1}$ [14]. Therefore the capacitance is just the curvature of the internal energy with respect to its internal parameter(s), and work can be extracted out of a system in a state with negative capacitance - thus it is unstable. The key point is that in an NCFET, the system is *not isolated*. If the depolarization fields can overcome the internal dipole fields that give rise to ferroelectricity, a balance is reached, and the series condition asserted earlier, $Q_{ox} = Q_S$, is realized. In the simple lumped capacitor model, if $|C_{ox}| > C_S$, the total capacitance is positive, and the negative capacitance is stable. The internal energy of C_{ox} would be decreased by increasing Q, but this would require a greater energetic cost in the charging of C_S. Finally, we note that in strong inversion, the channel is effectively shorted to ground through the source terminal, and the capacitance seen at the gate is just C_{ox} [10]. Thus the gate capacitance must be engineered to only be negative in subthreshold.

Ferroelectricity: A Source of Negative Capacitance

Having established the potential benefits of negative capacitance, the question remains as to where such states may occur in nature. In thinking of capacitance as curvature of the internal energy landscape, one is led naturally to ferroelectric materials. A ferroelectric is defined as a material which exhibits a spontaneous polarization that can be reversed with an

applied electric field [15]. In other words, the internal energy of a ferroelectric is minimized by a nonzero polarization, with at least two minima. This is referred to as the "spontaneous polarization," typically in the range of 1-100 μC/cm^2. If the internal energy is a smooth function of the out-of-plane component of polarization, then its qualitative form would be given by something like 1.3.

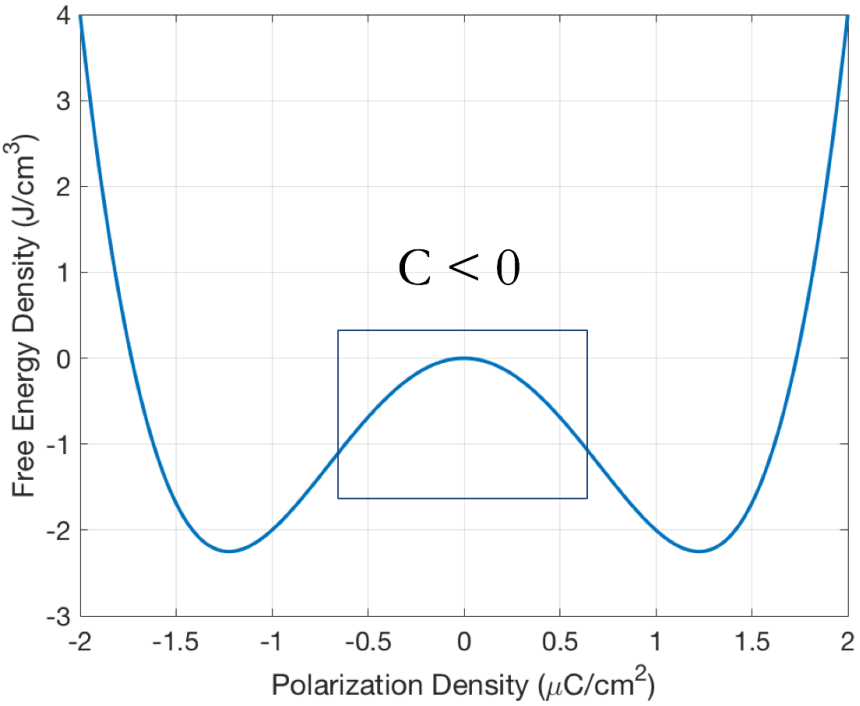

Figure 1.3: Energy landscape of a hypothetical ferroelectric material. The region of negative capacitance states between the spontaneous polarization states is indicated.

Now we must consider how this relates to charge on the plates of a capacitor. Recall that the charge density is given by the displacement electric field at the surface, $D = \epsilon_0 E + P$, where ϵ_0 is the permittivity of free space, E is the electric field, and P is the polarization density in the material between the capacitor electrodes [14]. So the charge Q is just the area A times the displacement field, $Q = A(\epsilon_0 E + P)$. In practice, $P \gg \epsilon_0 E$, and $Q \approx AP$, so that ferroelectric polarization and capacitor charge may be treated interchangeably in most contexts. Strictly speaking, the function shown in 1.3 is the free energy per unit volume, so its curvature is the dielectric susceptibility. These considerations suggest that, if the ferroelectric material can be brought near the $P = 0$ state, its capacitance will be negative.

1.3 Summary of Previous Work

The story of ferroelectricity goes back to the 17th century, in the town of La Rochelle in the south of France. In 1665, an apothecary named Elie Seignette concocted potassium sodium tartrate tetrahydrate ($NaKC_4H_4O_6{\cdot}4H_2O$), which came to be sold as "sel polychreste" as a mineral-derived medicine. Although its medicinal use eventually fell out of favor, it remained on the market for over two centuries and later came to be known as Rochelle salt [16]. In 1824, David Brewster, observed pyroelectricity in a number of materials, including Rochelle salt, and it entered the world of materials science. In 1880 Pierre and Paul-Jacques Curie systematically studied the temperature dependence of Rochelle salt, and identified its piezoelectricity, which lead to its use as a transducer material in military applications during WWI. In 1912, Peter Debye, who had been following the developments in piezoelectricity, hypothesized that the experimental results could be explained by the existence of a permanent electric dipole moment, analogous to the permanent magnetic dipole moments in ferromagnets. Furthering this analogy, Debye proposed that the dielectric susceptibility χ should diverge at the Curie temperature according to the Curie-Weiss law, 1.4.

$$\chi = \frac{C}{T - T_C} \tag{1.4}$$

Here C is the material-dependent Curie constant, T is temperature, and T_C is the Curie temperature. Above the Curie temperature, the material behaves as a normal insulator, but as the temperature is lowered, the susceptibility diverges, and a spontaneous dipole moment appears even in the absence of a field [15]. Erwin Schrödinger generalized this work to the case of solids rather than just molecules, and coined the term "ferroelectricity" (German: "ferroelektrisch").

In 1920, Joseph Valasek, a graduate student at the University of Minnesota in Minneapolis carried out systematic studies on Rochelle salt, drawing an analogy between the relationship between the B and H fields of ferromagnets and the E and D fields of ferroelectrics [17]. His work lead to the first experimental observation of ferroelectric hysteresis, shown in 1.4.

The advent of WWII produced a surge of interest in ferroelectric research, which lead to the discovery of ferroelectricity in barium titanate ($BaTiO_3$). This was the first discovery of ferroelectricity in a simple oxide, without hydrogen bonds. The class of materials to which $BaTiO_3$ belongs, the perovskite oxides, has dominated research in ferroelectricity and are by far the most well-studied class of ferroelectric materials. As one may expect from the susceptibility divergence in the Curie-Weiss law, these materials exhibit extremely high relative dielectric constants, which can exceed 1000. This saw the use of ferroelectrics in a variety of applications, mostly as transducers or low-volume discrete capacitors. Ferroelectrics have also found use in communications, where the nonlinear electro-optic effect results in an electrically controlled optical switch. Interestingly, the use of ferroelectricity as a non-volatile memory, where it is placed in the gate of a transistor and thus controls the threshold voltage with its polarization state, dates back to the the master's thesis of Dudley Allen Buck at MIT in 1952 [18].

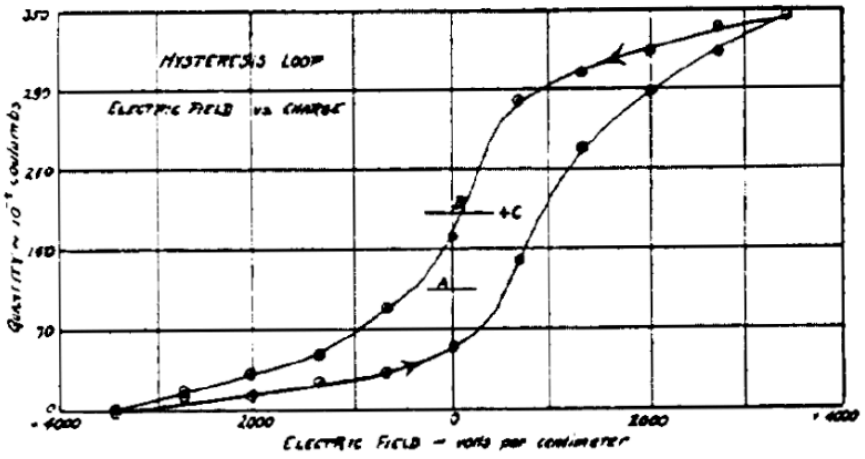

Figure 1.4: The first reported ferroelectric hysteresis loop, by Joseph Valasek on Rochelle salt. From [17].

Ferroelectricity in solids can also be analyzed in terms of their symmetries. A nonzero spontaneous (or remanent) polarization requires the breaking of inversion symmetry. Of the 32 crystallographic point groups, 21 are noncentrosymmetric, of which all but 1 are piezoelectric. 10 of these are pyroelectric, which is a superset of ferroelectrics. Ferroelectrics are often classified according to whether they are displacive, where the force from internal dipole fields overwhelms the restoring force of the lattice, or order-disorder, where permanent dipoles align as temperature is reduced [19]. In reality, the strain fields of the lattice and the unit cell dipole moments must be solved self-consistently, and it is impossible to draw a clear line between the two [16].

In the 1930s, Soviet physicist Lev Landau developed a phenomenological theory of phase transitions. It is a phenomenological theory which, assuming coarse-graining of fluctuating internal fields, provides a relationship between microscopic theory and measurable macroscopic quantities. Landau recognized that a phase transition which breaks symmetry must be accompanied by the development of a corresponding order parameter. The state of the system is then represented by a thermodynamic free energy, which is expanded in a Taylor series in that order parameter. This formalism gave rise to the Ginzburg-Landau theory of superconductivity, which was important in the development of that field. In 1949, A. F. Devonshire adapted Landau's theory to ferroelectricity. This theory is called the Landau-Devonshire theory, and it remains a cornerstone of analyzing ferroelectric behavior today [20]. Its central result is the form of the free energy functional, given in 1.5 below.

$$u = \alpha_0(T - T_C)P^2 + \beta P^4 + \gamma P^6 + ... - EP \tag{1.5}$$

The last term represents coupling to the electric field. From this free energy, one can calculate

the temperature dependence of the susceptibility, and derive the Curie-Weiss law in 1.4, as well as a variety of physical quantities. The hysteresis loop can also be explained in terms of the Landau-Devonshire theory. A system in one of the two energy minima can be driven into the other when an applied field tilts the energy landscape until the energy barrier between the minima (and thus one of the minima) disappears. Turning off the field now leaves the ferroelectric in the other minimum, which produces the observed hysteresis. This process is explained in much greater detail in further chapters.

Since the second world war, ferroelectricity has become an active field of scientific research, with many tens of thousands publications in the literature today. A large number of materials have been discovered which exhibit ferroelectricity, many which exhibit more exotic origins, such as electronic ferroelectrics [15]. Antiferroelectricity, analogous to antiferromagnetism, was proposed by Charles Kittel and discovered in a number of materials [21]. Numerous advancements were made in ferroelectric materials synthesis and characterization as well as in the theoretical descriptions of ferroelectricity, which are too numerous to cover here.

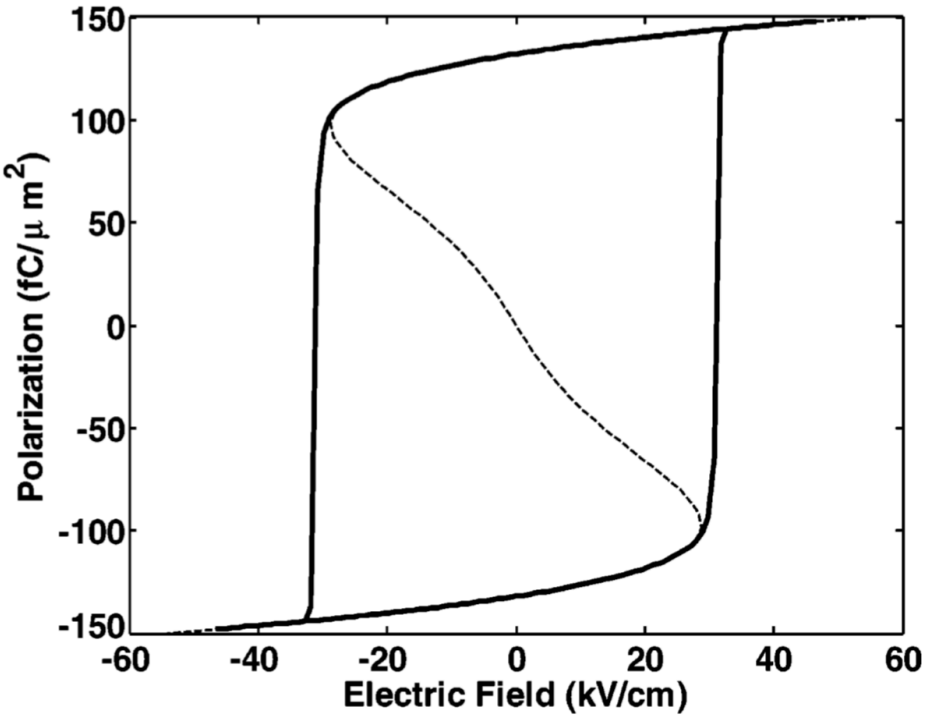

Figure 1.5: Hysteresis loop of a $BaTiO_3$ sample, with the proposed negative capacitance states shown with a dashed curve.

In 2008, searching for a way to combat the aforementioned "Boltzmann tyranny," Salahuddin and Datta noted that in the Landau-Devonshire theory, the equilibrium states of P cor-

responding to various values of E form an S-curve, which an experimental hysteresis loop encloses. This is conceptualized for $BaTiO_3$ in 1.5. The disappearance of the local minimum of the system at the coercive field is reflected in the S-shape of the dashed curve. A negatively poled ferroelectric subject to a positive electric field suddenly has no nearby states at the lower cusp of the "S," and the material is driven out of equilibrium to the other (remaining) minimum. The negative capacitance portion of the S-curve is necessary to produce the multiple solutions that result in hysteresis, but it had not been considered that those states could be stabilized with a series capacitor and used for voltage amplification.

In late 2010, experimental demonstration of ferroelectric negative capacitance was first reported. Khan et al. showed that the capacitance of a heterostructure comprised of ferroelectric lead zirconate titanate and dielectric strontium titanate could be increased beyond that of just the strontium titanate [22]. They reported a temperature-dependence which was totally consistent with Landau-Devonshire theory, and found that the Curie temperature was effectively lowered by the presence of strontium titanate. Similar characterization was performed soon after for a ferroelectric $Ba_{0.8}Sr_{0.2}TiO_3$-dielectric $LaAlO_3$ superlattice [23]. Almost simultaneously, Rusu et al. reported sub-60 mV/decade subthreshold slope in a polyvinylidene fluoride (PVDF) gated FET [24]. This work begins in this era, when relatively few experiments had been carried out on ferroelectric negative capacitance, and its existence was contentious. Since then, especially with the discovery of ferroelectricity in doped hafnium oxides, research involvement in negative capacitance has grown considerably, with the first industry results on negative capacitance transistors announced in 2017 [25].

Chapter 2

Direct Observation of Negative Capacitance

2.1 Introduction

The first demonstrations of negative capacitance involved two substantially different techniques. The work by A. Rusu et al. observed subthreshold slope in a ferroelectric-gated MOSFET below 60 mV/decade at room temperature [24]. The work by A. I. Khan et al. demonstrated a capacitance enhancement in a ferroelectric-dielectric stack as compared to the dielectric alone [22]. While both of these techniques are robust, they rely on indirectly observing the effects of negative capacitance - that is, voltage amplification - rather than a direct observation of capacitor charge changing in opposition to the voltage drop across it. The controversy surrounding the claim of passive, static negative capacitance provided the impetus to find a way to directly observe negative capacitance in an isolated ferroelectric capacitor. As the negative capacitance states of an *uncoupled* ferroelectric are unstable, it was natural to seek to observe them during the process of ferroelectric polarization switching. Thus the experimental setup in 2.1 was conceived. A voltage pulse above the coercive voltage is applied to a poled ferroelectric capacitor in series with a resistor R whose purpose is fourfold.

1. Limit the switching current, and therefore slow the rate of polarization switching, so that the transient can be measured using a standard oscilloscope.
2. Dominate the dissipation (ρ) of the ferroelectric so that the capacitor voltage closely follows the internal voltage, which relates the polarization state to the free energy.
3. Act as a current meter according to $V_S - V_F = IR$, allowing for extraction of the dynamic hysteresis loop after integration of current.
4. Provide an external parameter whose variation can provide insight into the nature of the observed negative capacitance transients.

By driving this simple series RC circuit with a standard voltage waveform generator and monitoring the node voltages, we are able to probe the switching dynamics of the ferroelectric capacitor and observe a negative capacitance.

In 2.2, we discuss the process of ferroelectric switching in the context of an energy landscape modified by an external field. In 2.3, we discuss the fabrication of the PZT films used in this experiment and briefly comment on material characterization through X-ray diffraction. Following this, the experimental setup is outlined in 2.4. The crux of the work, the negative capacitance transients, is presented in 2.5, and its identification with ferroelectric switching is established in 2.6. Scaling of the transients in response to changing the external resistance is discussed in 2.7. Finally, conclusions and proposed directions of future work are outlined in 2.9.

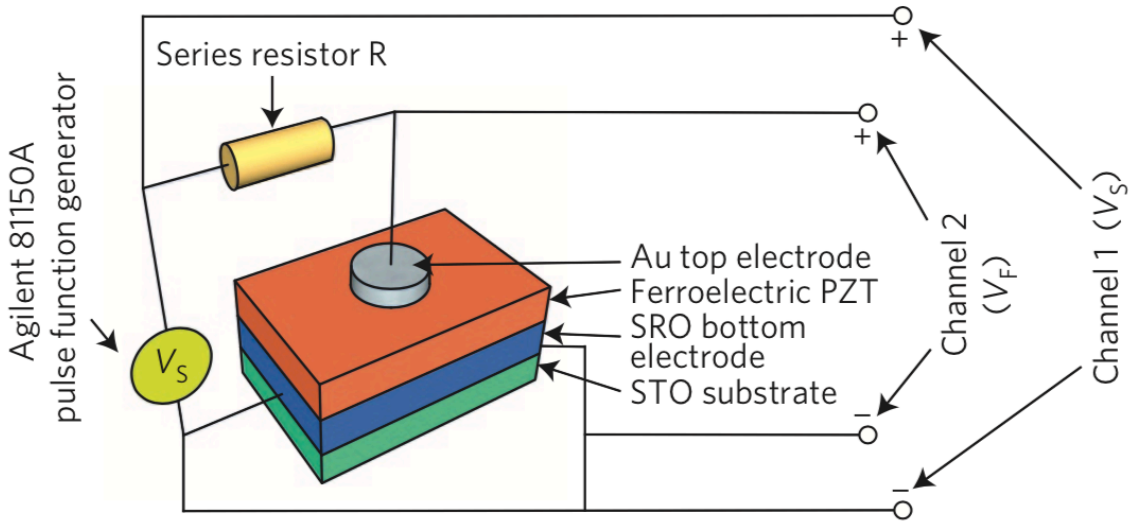

Figure 2.1: Schematic diagram of the experimental setup. The resistor consists of a $0 - 100k\Omega$ potentiometer, and the ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT) capacitor is deposited and patterned on a substrate of $SrTiO_3$ (STO). Not pictured is a parasitic cable capacitance that appears in parallel with the ferroelectric capacitor. From [26].

The idea of observing negative capacitance in a switching transient arises from consideration of the so-called "double well" Landau free energy landscape shown in 2.2. A quantitative calculation of the Landau free energy may be carried out from first principles by considering crystalline atomic potentials. Such a calculation may be useful for describing properties of a paraelectric-ferroelectric phase transition, but ferroelectric switching usually occurs via domain nucleation and growth [19]. As such, the energy barrier between the two sponta-

neously polarized states of a ferroelectric is far overestimated, as in practice it is unnecessary to depolarize the entire volume of the ferroelectric at once. However, as will be shown, under favorable conditions, the voltage response of nucleating domains can dominate the response of the overall material, and the material is qualitatively described by a double well energy landscape.

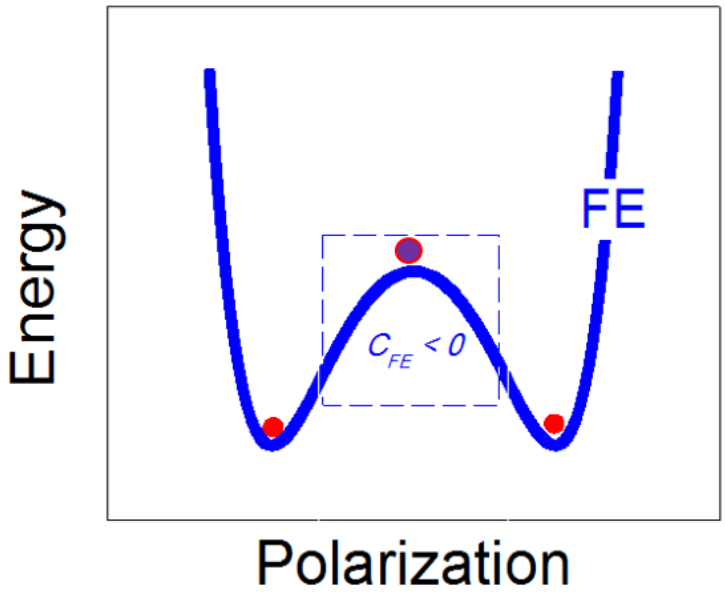

Figure 2.2: Qualitative depiction of energy landscape as a function of ferroelectric polarization with no applied voltage. The circles indicate critical points of the free energy functional, and the dotted box shows the region in which the ferroelectric capacitance is negative.

In fact, although the range of negative capacitance states can be arbitrarily small, its existence is guaranteed as a consequence of an energy landscape with two minima. A subtle distinction must be made here: the term polarization refers to the integrated polarization, in other words the net charge on the plates of a capacitor. We readily admit that spatial variation of polarization exists and that uncontrollability of the particular path in this high-dimensional phase space the ferroelectric takes is a legitimate concern. We merely demonstrate that it is possible to reliably force a ferroelectric material through a path such that $\frac{\partial Q}{\partial V}$ of the capacitor is less than zero. In particular, $\frac{\partial Q}{\partial V}$ is distinct from the determinant of the Hessian of the function relating the spatially varying polarization to the field, which can also be taken as a generalized definition of capacitance, though not the one relevant for voltage amplification.

2.2 Dynamics of Ferroelectric Switching for a Single Domain

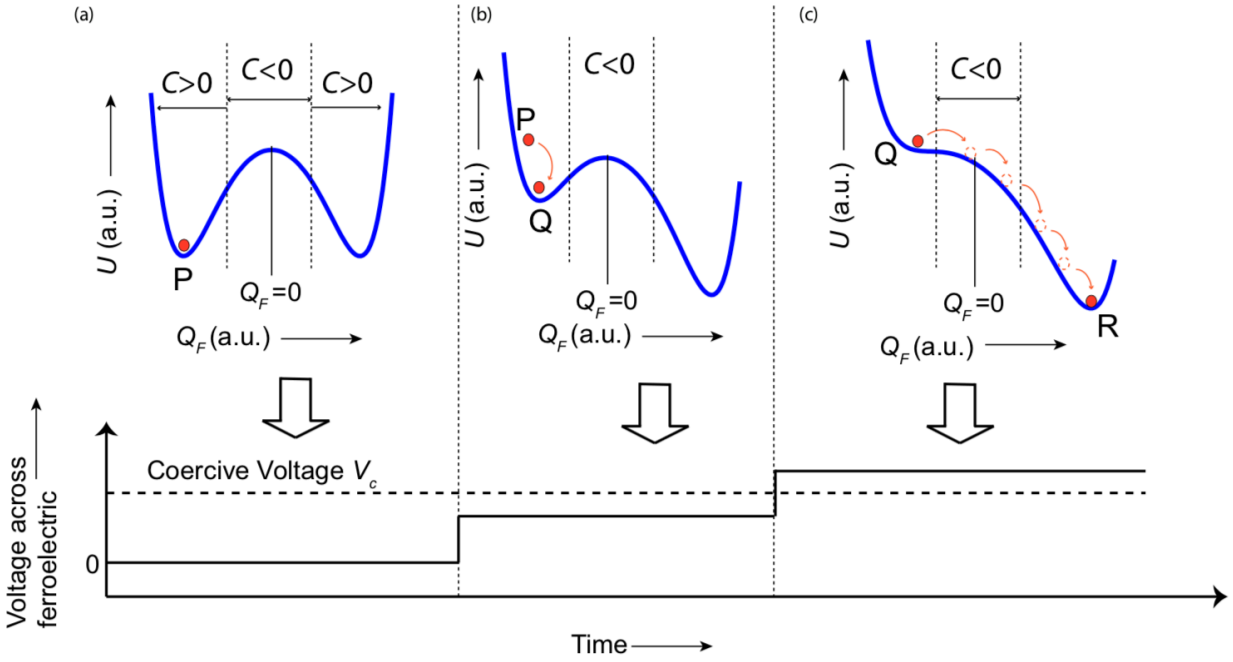

Figure 2.3: Tilting of the energy landscape under an applied voltage. (a) The ferroelectric under zero voltage. (b) The energy landscape tilts under the application of a field below the coercive voltage, though a barrier remains. Thermal switching may occur at long enough timescales. (c) Only the right-most minimum at R remains, and the material spontaneously traverses the energy landscape, which is the polarization switching.

We describe the switching process under the above assertion that the ferroelectric can behave qualitatively as a single domain. Consider a material at the point P shown in 2.3. At zero voltage, $V_F = 0$, this is the local minimum. As V_F rises slightly, the minimum moves slightly to the right, to point Q. This is often called the "dielectric response" of the ferroelectric, referring to the infinitesimal change of the polarization in response to an infinitesimal change in voltage. At this point, the true minimum of the system is the right-hand side well, and thermal fluctuations over a long enough timescale can cause ferroelectric switching. Finally, as V_F surpasses the coercive voltage V_C, the barrier and the local minimum disappear abruptly, and the material spontaneously moves to the point R. Note that the capacitance, which depends on the second derivative, is not affected by the applied field, which adds a linear term to the energy landscape. During this traversal, the material passes through the negative capacitance states. This is the viewpoint we take when interpreting the results of the experiment.

It is important to note that not every ferroelectric film will produce a signature of negative capacitance in a switching transient. The precise conditions under which this will occur is still an open question, but it is clear that an excessive variation of the coercive field will likely result in too few nucleation events, so that an insignificant fraction of the material is depolarized at any given time. This picture is analyzed in terms of the geometry of domain walls using a phase field simulation in [27].

2.3 Fabrication and Material Characterization

The thin films of PZT, ranging in thickness from 60 nm to 150 nm, were grown on either metallic $SrRuO_3$ (SRO) or $La(Sr_xMn_{1-x})O_3$ (LSMO) buffered STO substrates using the pulsed laser deposition technique. The close lattice matching of these materials allows for the deposition of crystalline films with low defect densities. The deposition temperature for SRO was 630 °C and for PZT was 720 °C. The O_2 partial pressure during deposition for both materials was 100 mTorr. The laser pulse energy was 100 mJ with a spot size of approximately 4 mm^2. Top electrodes (5 nm Au, 40 nm Ti, 5 nm Au) were patterned on top of the film using standard photolithography techniques. Gold is used both to make good contact with PZT and as a capping layer to prevent oxidation. The presence of Ti separated by Au does not have any effect compared to pure gold electrodes due to screening. The device geometry is also depicted in 2.1. The SRO is used as a bottom contact, and its thickness was chosen to ensure a good, low resistance contact. The PZT film thickness was chosen to minimize leakage and ensure robust ferroelectric properties.

The PZT film is structurally characterized by X-ray diffraction measurements. These measurements show peaks consistent with ferroelectric PZT. In particular, it is worth noting that the full-width half-maximum (FWHM) of the (002) peak for the samples that exhibit negative capacitance transients is low, on the order of 0.1°. A FWHM of 0.3° is more commonly encountered in our fabrication, and such samples do not show the negative capacitance transients. We hypothesize that the high number of defects corresponding to such a large FWHM result in too broad of a distribution of coercive fields. This would imply that almost all of the material switches via domain wall motion, and that domain nucleation events are low in number. In this case, a negligible portion of the material would be depolarized at any given time, and it would be unable to dominate the overall response.

2.4 Experimental Setup

The measurement circuit consists of a ferroelectric capacitor in series with an external resistance and a voltage function generator (Keysight 81150A), as depicted in 2.1. The ferroelectric capacitor, itself modeled as a nonlinear capacitor in series with an internal resistance, is accessed in a standard probe station (Everbeing 30080). The voltage at each node was monitored as a function of time using a standard 200 MHz oscilloscope (Agilent DSO1024A).

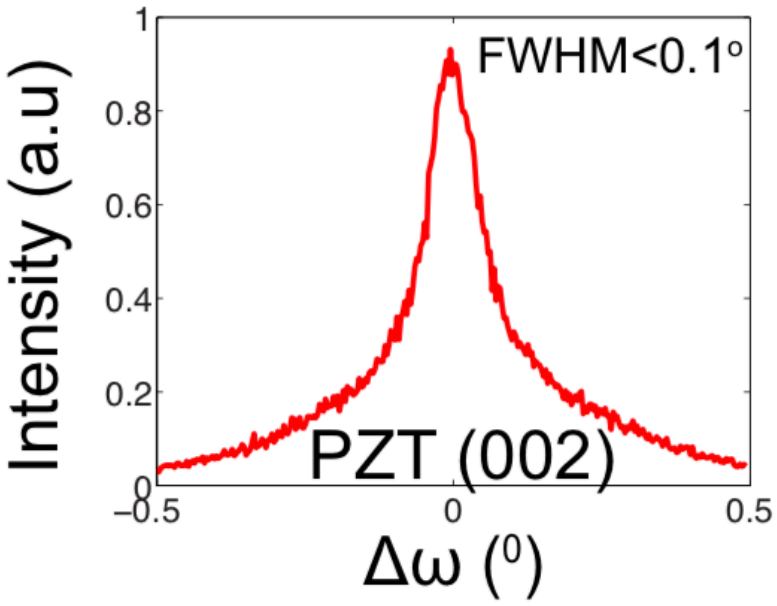

Figure 2.4: X-ray diffraction rocking curve measurement for the 60 nm PZT film primarily used for this work. The x-axis shows angular displacement from the center of the (002) peak for PZT. From [26].

At time $t = 0$, the voltage at the source changes sharply from zero to some nonzero switching voltage, V_S, which may be positive or negative. The rise time is 2.5 ns.

Additionally, the usual quasistatic polarization-electric field hysteresis loops and capacitance-voltage measurements of the samples were obtained using a multiferroic tester (Radiant P-PMF) and a semiconductor device analyzer (Agilent B1500), respectively. The samples show a remnant polarization of around 0.8 $\mu C/cm^2$ and coercive voltages on the order of 2 V. The coercive voltages may be asymmetric by 200 mV due to metal work function difference and charged defects, as is commonly encountered in ferroelectric hysteresis measurements [15]. The quasistatic hysteresis loops for various sweep rates are shown in 2.5.

A final point regarding the experimental setup concerns the parasitic capacitance introduced by the coaxial cables connecting the voltage source to the resistor and probe station. In order to accurately measure the current flowing through the ferroelectric capacitor, one must subtract the displacement current flowing through this capacitor. The equivalent circuit model of the setup is shown in 2.6. In order to determine the value of this parasitic capacitance, we applied voltage pulses to the probe station in an open circuit configuration (no sample on the stage) with a $50k\Omega$ resistor, and fitted the voltage transient according to $V_C(t) = V_S(1 - e^{-t/RC})$. V_S is varied to confirm linearity of the parasitic capacitance. The parasitic capacitance C_P is finally extracted to be 60 pF.

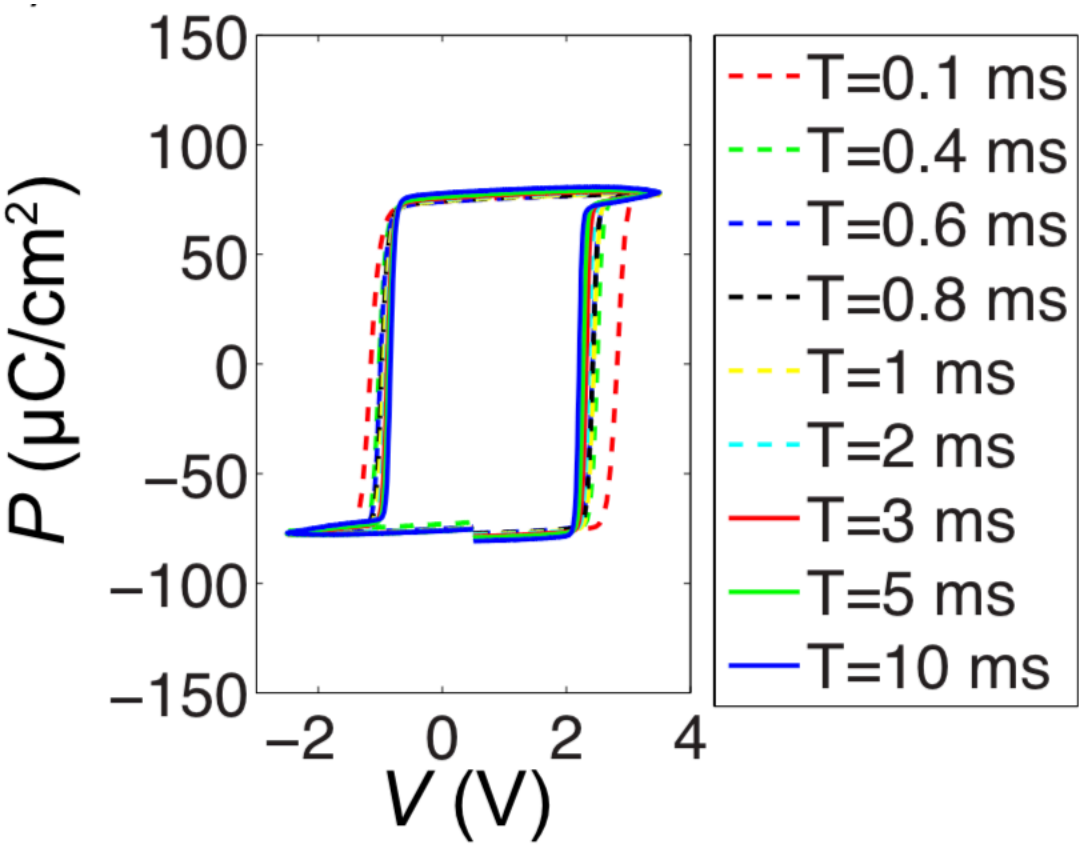

Figure 2.5: Quasistatic hysteresis loops for various sweep rates of the applied field. The measurements were taken using a Radiant P-PMF multiferroic tester. The nearly full closure of the loop and clear saturation indicate robust ferroelectric properties. From [26].

2.5 Negative Capacitance Transients

We now consider the experimental data from observing the switching process in a 60 nm PZT capacitor with electrode area $A = (30\mu m)^2$. The series resistance $R = 50k\Omega$, and the switching voltage is 5.4 V. The dependence of the switching transient characteristics on the applied voltage is discussed at length in 3. The salient properties of the switching transient are visible in 2.7. Prior to $t = 0$, a voltage of -5.4 V is applied to pole the ferroelectric polarization in the negative direction. This ensures that the switching pulse with amplitude 5.4 V will result in polarization reversal. The top left graph shows the source voltage marked with white dots and the voltage across the ferroelectric marked with green dots. Note that the dots are there only as visual markers; the experimental data are taken with a much

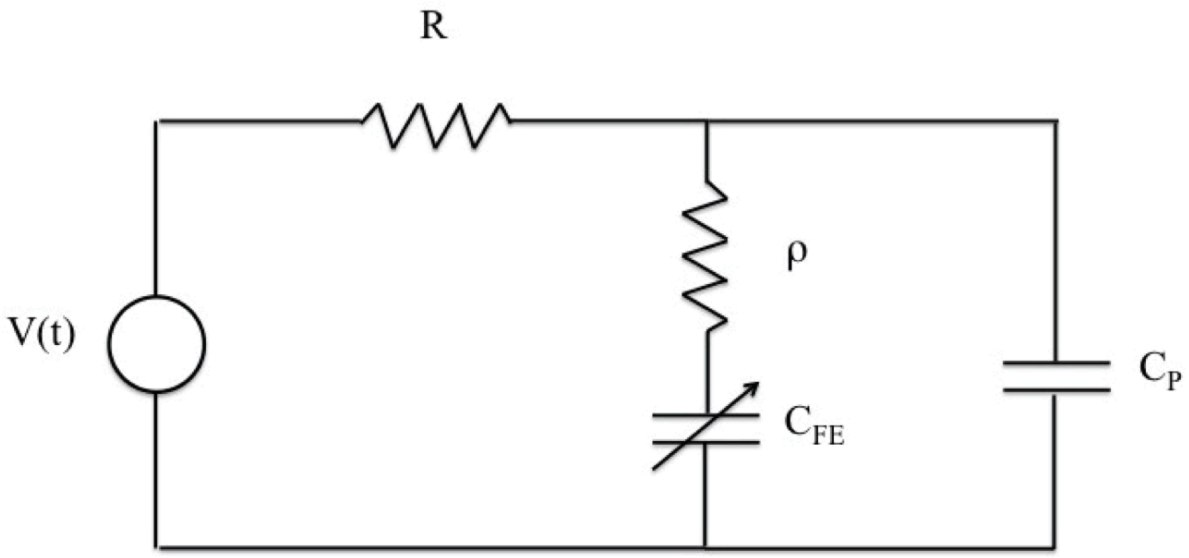

Figure 2.6: Equivalent circuit of the experimental setup, showing the parasitic cable capacitance appearing in series with the ferroelectric capacitor. Here ρ represents dissipation internal to the ferroelectric.

higher sampling frequency.

The middle left graph shows the corresponding current through the ferroelectric, and the bottom left is the change in the charge, i.e. the integral of the current. Once the source voltage is high, the ferroelectric voltage begins to rise with a normal RC-shaped transient until point A, when the voltage suddenly reverses until B, apparent in the close-up of the transient. In other words, the ferroelectric voltage changes in opposition to the source voltage! At the same time, the current through the ferroelectric is positive. Hence, dV and dQ are of opposite sign, and the capacitance in this region must be negative. A totally analogous situation occurs when the sign of the source voltage is reversed, and negative capacitance is apparent again in the opposite switching direction, between the points C and D.

The polarization $P(t)$ can be calculated by dividing the charge by the area $P(t) = Q(t)/A$ and plotted against the ferroelectric voltage $V_F(t)$ as in 2.8. We term this the *dynamic hysteresis loop*. Although the dynamic hysteresis loop exhibits negative capacitance and bears a qualitative resemblance to the theoretical predictions of a single-domain model, there is a significant quantitative departure that requires a spatially varying model to properly explain.

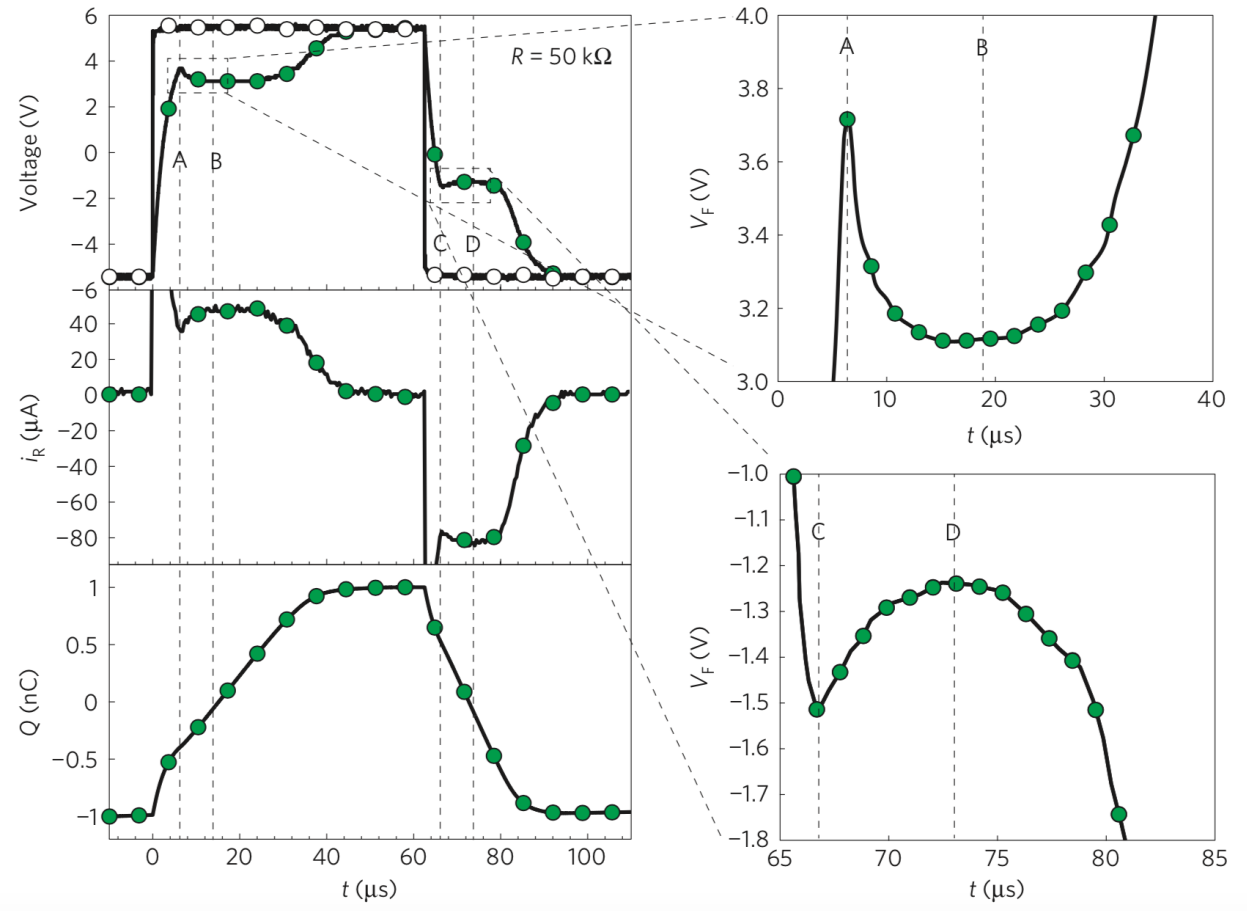

Figure 2.7: Switching dynamics of a 60 nm PZT capacitor. The source voltage is marked with white dots, and the ferroelectric transients are marked in green. The current is calculated from Ohm's law by measuring the voltage across the resistor, from which the parasitic displacement current $C_P \frac{\partial V_F}{\partial t}$ is subtracted to yield the ferroelectric current. This is integrated in the bottom figure to show the change in charge. The portions of the voltage transients which exhibit negative capacitance are shown in close-up on the right. From [26].

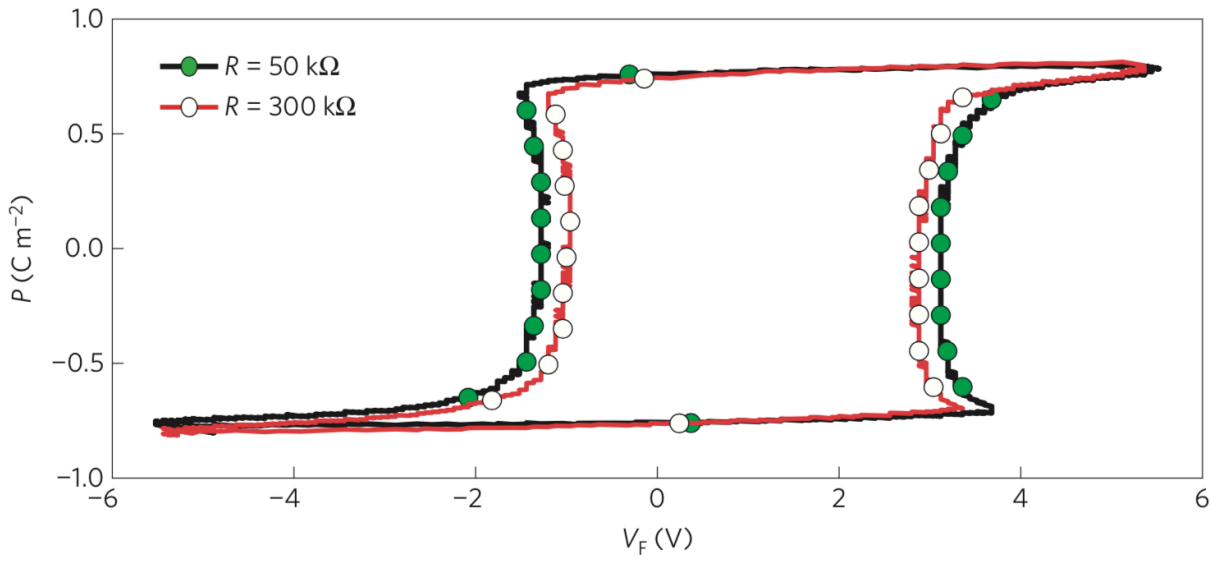

Figure 2.8: Dynamic hysteresis loops for the same 60 nm PZT sample in 2.7 for two different values of series resistance. Widening of the loop occurs for lower values of R, analogous to the widening of the quasistatic hysteresis loops with faster ramp rate. This widening is predicted by a simple single-domain model. The negative capacitance is apparent in the top left and bottom right corners of the dynamic hysteresis loops. From [26].

2.6 Identification of the Negative Capacitance Transient with Ferroelectric Switching

To firmly establish that the negative capacitance signature observed in the transient response is indeed the passing of the ferroelectric through the negative capacitance states depicted in the energy landscape of 2.1, a couple of observations can be made.

First, when a voltage pulse below the coercive voltage is applied, there is no negative capacitance in the transient response, which is visible only when the source voltage is above the coercive voltage. Second, if the ferroelectric is pulsed after the switching pulse, the second transient contains no signature of negative capacitance. This is shown in 2.9. Together, these observations establish that the negative capacitance signature is the result of ferroelectric polarization switching, and cannot be due to charged defects, etc.

2.7 Variation of the External Resistor

In order to understand the implications of varying the external resistor, it is worth considering the Landau-Khalatnikov equation [28], which is the simplest possible dynamical equation for

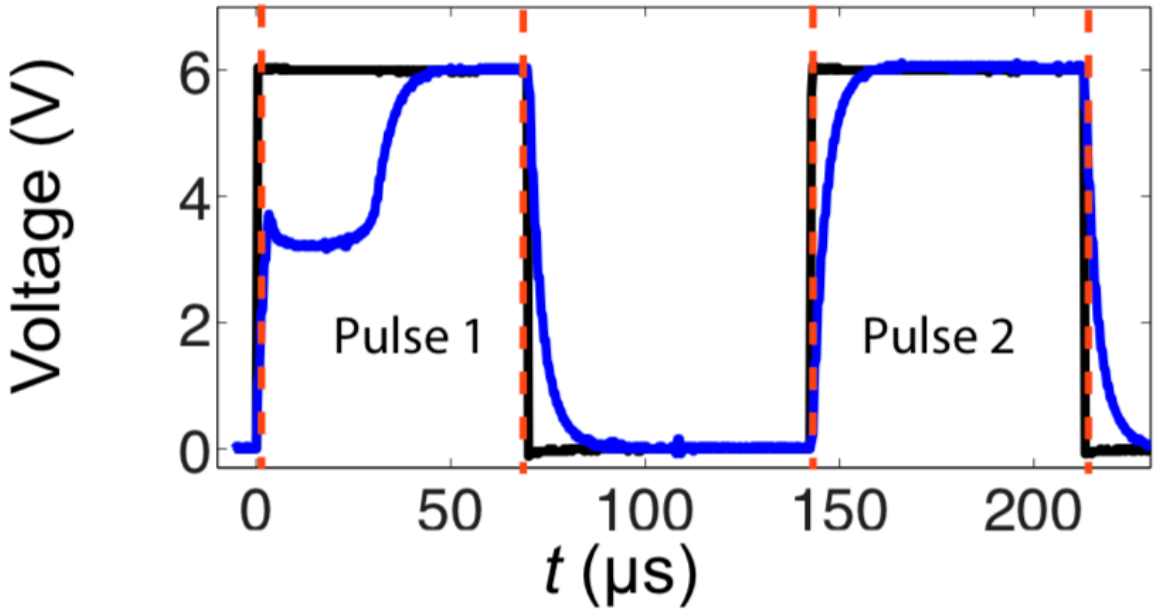

Figure 2.9: A train of switching pulses applied to the ferroelectric shows that the negative capacitance signature only occurs in the first transient, showing that it correlates with ferroelectric polarization switching. From [26].

a ferroelectric with a polarization-field relationship described by a Landau-Devonshire free energy density functional u.

$$\rho \frac{\partial P}{\partial t} + \nabla_P u = 0 \tag{2.1}$$

ρ represents a drag force proportional to the rate of change of polarization, and physically arises from energy dissipation within the ferroelectric in the form of thermal phonons. From a circuit perspective, this term manifests as a resistance in series with the nonlinear ferroelectric capacitor. Thus, modulo the effect of the parasitic cable capacitance, ρ appears in series with the external resistor. By comparing the external resistor with the duration of the transient and extrapolating to zero, one can obtain a very rough estimate of the value of ρ and the intrinsic speed of switching.

Given the lack of a properly defined time constant for a nonlinear capacitor, we use as a benchmark the duration for which the ferroelectric capacitance is negative. We call this duration t_1. As shown in 2.10, the extrapolated value of t_1 when the switching is limited only by internal resistance is 19.9 ns [29]. The value of that internal resistance is found to be 25 $k\Omega$, which corresponds to a resistivity of 375 Ω m. Comparison of experimental data with predictions made by the Landau-Khalatnikov equation are discussed in further detail

in 3.

2.8 Negative Capacitance Transients in Ferroelectric Hafnium Oxide

In 2011, T. S. Böscke et al. reported the existence of a ferroelectric orthorhombic phase in polycrystalline doped hafnium oxide, which has seen widespread use in industrial CMOS processes for over a decade as a high-κ gate dielectric [30]. Since the discovery of ferroelectricity in hafnium oxide, significant exploration of various dopants and annealing conditions has resulted in a rich library of ferroelectric and antiferroelectric material properties [31]. Because of the ease with which a ferroelectric can now be integrated into the gate stack of an industrial MOSFET [32], the engineering of negative capacitance in doped hafnium oxides is crucial for the deployment of this technology. To this end, the measurements described in 2.4 were repeated on Gadolinium-doped hafnium oxide (Gd:HfO_2) thin film capacitors in [33]. We recount the results of those experiments here.

The capacitors are formed by first using reactive sputtering to deposit 10 nm of TiN as a back contact onto a silicon substrate at room temperature. This is followed by atomic layer deposition (ALD) of Gd:HfO_2 with a Gd content of 3.4 cat% at 300 °C. A top contact layer is then formed, identical to the back contact. The ferroelectric phase anneal is carried out for 30 min. at 650 ° C in N_2 ambient. The rest of the top electrode layer, 10 nm Ti for adhesion followed by 50 nm of Pt, is deposited by electron beam evaporation to a shadow mask to create circular contacts of 200 μm diameter. Wet etching removes the initial top TiN layer. Contact to the back electrode is formed by applying a large voltage in the capacitor adjacent to the device under test, causing breakdown and creating a short to the back TiN layer.

Qualitatively, the transients are quite similar to those of the ferroelectric PZT samples. An initial rise of the ferroelectric voltage is followed by a negative capacitance portion where the voltage changes in opposition to the source, then stabilizes and rises again to meet the source. Again the apparent coercive voltage is seen to reduce with increasing resistance. This is equivalent to a widening of the hysteresis loop at higher resistances. As the external series resistance is increased, it dominates the internal resistance of the ferroelectric, whose voltage then more closely follows the S-curve of equilibrium states. That this is indeed predicted by the Landau-Khalatnikov equation is verified in 3.3.

2.9 Conclusions

We have demonstrated that a set of negative capacitance states are traversed during the switching of an isolated ferroelectric PZT capacitor. These states may be observed with a standard oscilloscope if the switching is deliberately slowed by the addition of a series resistor. The manifestation of these states is only present during ferroelectric polarization switching - their correlation with the quasistatic coercive voltage of the PZT films as well

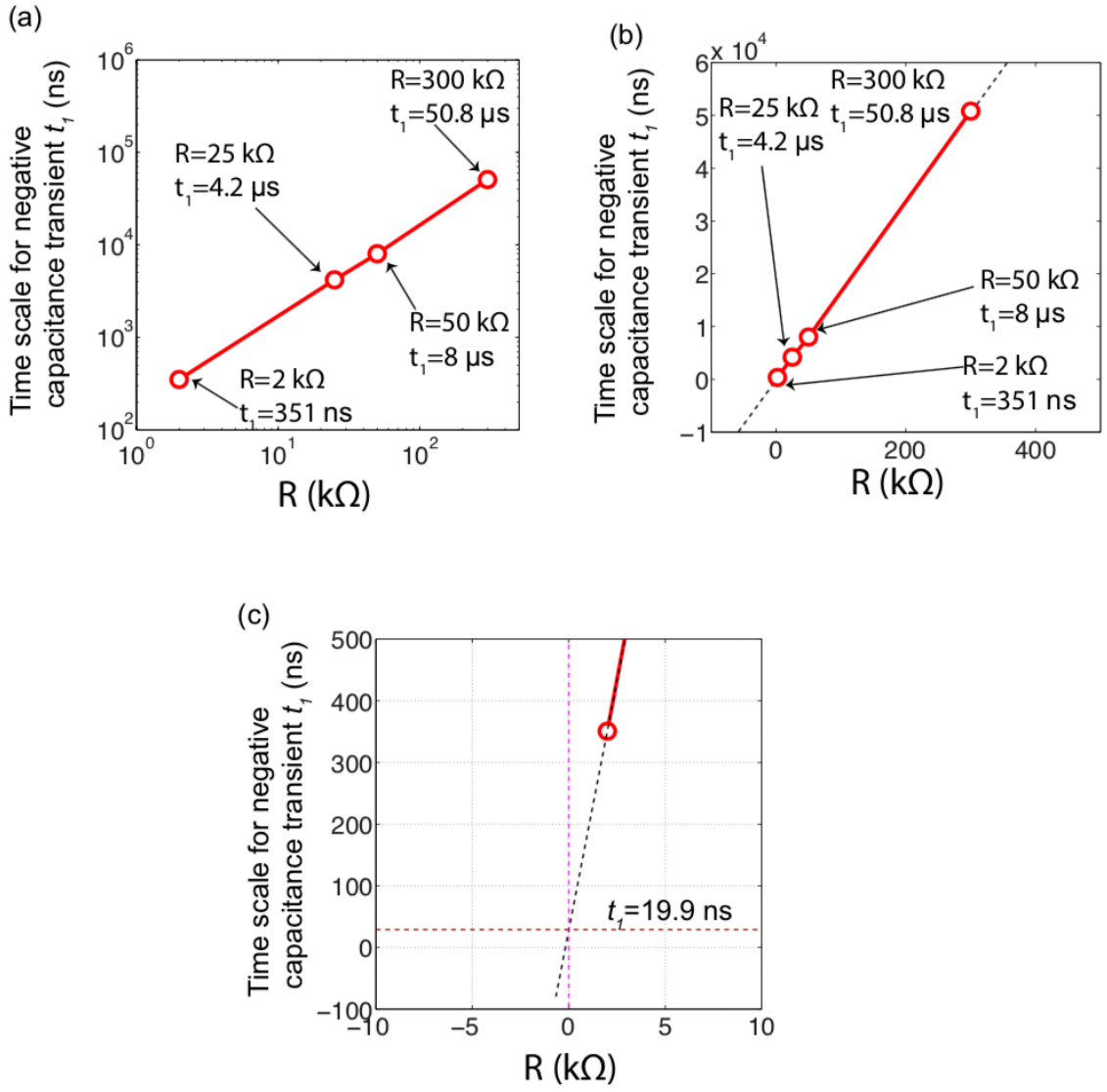

Figure 2.10: (a). Duration for which the ferroelectric capacitance is negative (t_1) for a switching voltage of +6 V, for varying values of resistance, plotted on a logarithmic scale. (b). The same data on a linear scale. (c). Extrapolation of the least squares linear fit to $R = 0$. The expected minimum value of t_1 at this switching voltage is 19.9 ns. ρ is estimated to be 375 Ω m which, as will be seen in 4, is a gross overestimate.

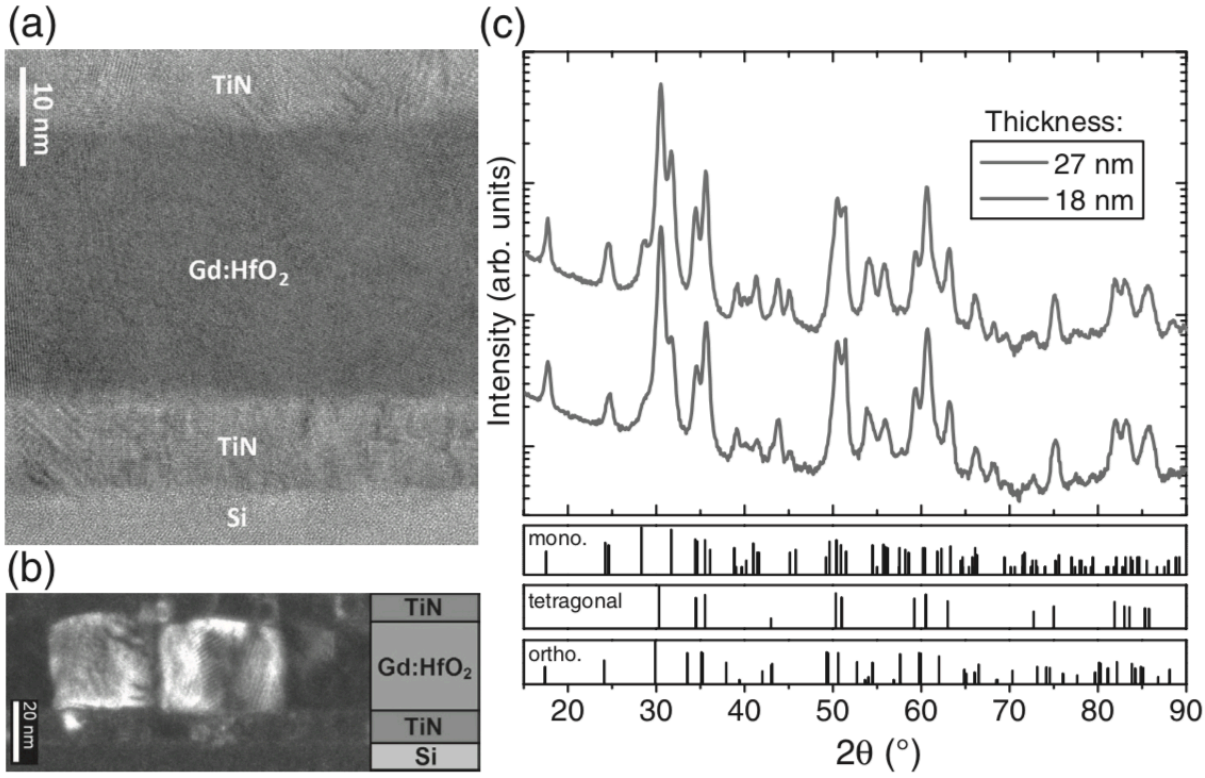

Figure 2.11: (a). TEM cross-section of a 27 nm Gd:HfO_2 capacitor. (b). Dark-field TEM shows grain boundaries orthogonal to the capacitor surface, implying a strain coupling between the hafnia and the capping layer. (c). Grazing-incidence X-ray diffraction for samples of 18 nm and 27 nm thicknesses, along with reference data for the expected crystalline phases present in the material. From [33].

as the history of previous switching events establishes this fact, and excludes explanations arising from extrinsic defect dynamics. Scaling of the external resistance predicts an intrinsic resistivity on the order of 375 Ω m.

The goal of these data is merely to establish the existence of the negative capacitance states. Inevitably, much more information about the ferroelectric is available from more careful analysis of the switching transients. The following chapter will discuss modeling efforts to explain more precisely the states of the ferroelectric during switching and to identify the physical processes which give rise to the observed phenomena. Such analyses can shed light on the switching processes and help identify properties that correlate with negative capacitance, but it is worth emphasizing that the negative capacitance states traversed during ferroelectric switching are likely not the same ones that can be stabilized by the depolarization fields in a heterostructure. As such, their usefulness in the design of negative capacitance transistors will be limited, and it will be necessary to exploit the charge-sensing

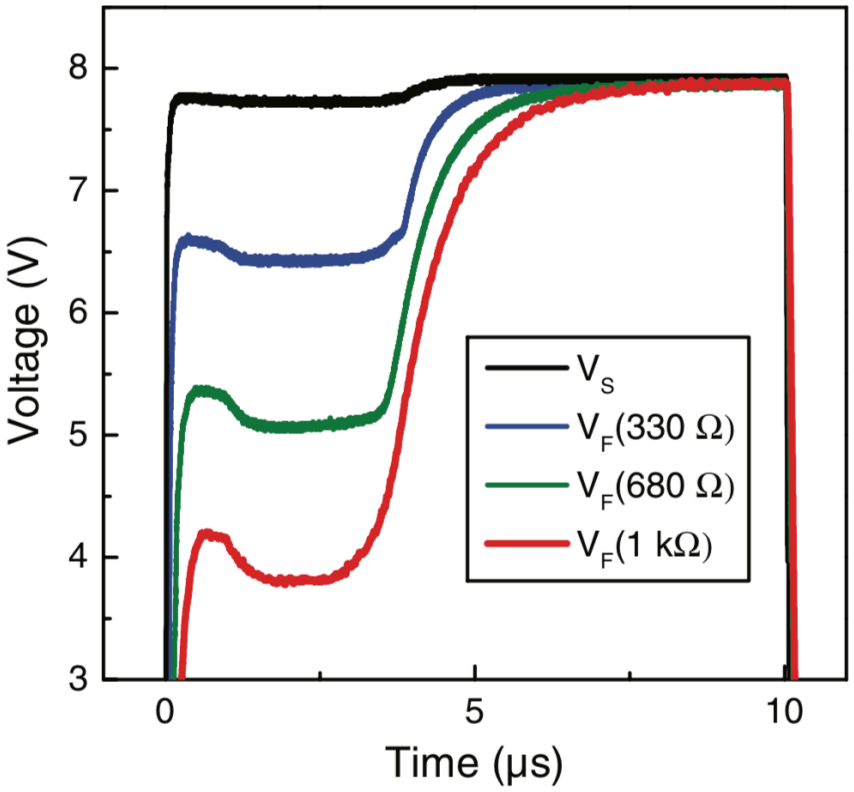

Figure 2.12: Switching transients for an 18 nm Gd:HfO_2 capacitor with different values of external series resistance. The negative capacitance signature is present in all of the transients, but its onset is at a reduced voltage for higher resistances. This is consistent with the predictions of the Landau-Khalatnikov equation. From [33].

properties of transistors themselves to measure the realizable values of negative capacitance in practice.

Chapter 3

Dynamics of Negative Capacitance in Isolated Ferroelectrics

3.1 Introduction

Previously we established in 2 the existence of negative capacitance states by direct observation of voltage switching transients in an isolated ferroelectric capacitor. It was noted that for a ferroelectric capacitor undergoing polarization reversal, the voltage across the capacitor changed in opposition to the current flowing through it, meaning that dQ and dV are of opposite sign, by definition negative capacitance. Placing a resistor in series with the ferroelectric capacitor allows one to observe the switching transient voltage across the ferroelectric as well as measure the current flowing through the circuit. The double-well energy landscape provides a rough description of the switching process, and why one may expect to observe negative capacitance during switching. However, a more detailed analysis is warranted.

The Landau-Khalatnikov (L-K) equation provides a simple dynamical model which is easily translated to a circuit equivalent. Solving the L-K equation yields a predicted voltage transient which is roughly qualitatively in agreement with experiment. Varying the magnitude of applied voltage, tracking the behavior of the transients, and making a quantitative comparison with the two phase Kolmogorov-Avrami-Ishibashi (KAI) model of ferroelectric switching, allows one to identify the negative capacitance portion of the transients with domain nucleation, and the flat portion of the transient immediately following it with domain wall propagation [34]. It is shown that the duration of these transients follows Merz's Law [35]. Furthermore, after fitting of the Avrami constants - the free parameters of the KAI model - a quantitatively accurate description of the positive capacitance portions of the transients is obtained. To definitively rule out the role of defects, the experiment is carried out at 100 K, well below the expected freeze-out temperature for defects in PZT [15].

KAI theory predicts the switching current in a ferroelectric capacitor without a series resistance while considering the effects of domains, but assumes instantaneous realization of

the applied voltage across the ferroelectric capacitor. The L-K equation, on the other hand, provides a definite relationship between polarization and electric field, but fails to account for domain effects. A phase-field model, like KAI theory, allows one to model spatial variation of polarization, but retains a continuous order parameter and a well-defined electric field [36]. Thus the two pictures can be reconciled, and the voltage transients can be reproduced with near-quantitative accuracy. It is seen here that the negative capacitance transient arises from accelerating domain wall growth - in other words an increasing depolarization of the ferroelectric film.

First, in 3.2 we outline the theory of the single-domain picture. Next, we consider the results of solving the L-K equation in 3.3. Then we describe the KAI model in some detail (3.4) and examine the ability of the theory to explain experimental results (3.5). Finally, we discuss phase-field modeling in 3.6 and provide concluding remarks in 3.7.

3.2 Single-Domain Theory: The Landau-Khalatnikov (L-K) Picture

The Landau-Khalatnikov equation, stated in 2.1 and repeated in 3.1 for convenience, constitutes the simplest possible dynamical description of a ferroelectric. The polarization is assumed to be uniform, and only the out-of-plane component is considered, as this is the component which manifests as charge on the capacitor plates, the experimentally relevant quantity. For a thin film ferroelectric, the spontaneous polarization points along the axis normal to the film [15].

$$\rho\frac{\partial P}{\partial t} + \nabla_P u = 0 \tag{3.1}$$

Here P is the out-of-plane component of polarization of the ferroelectric, u is the Landau-Devonshire free energy density, and ρ is a drag term which represents dissipation internal to the ferroelectric. u is usually expressed as a Taylor series in P as in 3.2. As usual, odd terms must vanish due to symmetry, and the last term describes coupling to the electric field.

$$u = \alpha P^2 + \beta P^4 + \gamma P^6 + ... - EP \tag{3.2}$$

The equilibrium states are calculated by setting $\frac{\partial u}{\partial P} = 0$ and are defined by 3.3, which, when plotted, results in the familiar S-curve.

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + ... \tag{3.3}$$

Thus the L-K equation simply states that there is an additional voltage proportional to the current flow. To map this model of a ferroelectric to the experimentally measured quantities, we must consider the equivalent circuit description of the experimental setup shown in 2.7. The L-K equation implies that the ferroelectric capacitor should be described by a nonlinear capacitor with a charge-voltage relationship derived from 3.3 in series with a

resistor. Additionally, we must consider the external series resistor and the parasitic cable capacitance, which draws displacement current.

The surface charge density on a capacitor is described by the well-known expression $\sigma = \epsilon_0 E + P$. Because of the high susceptibility of ferroelectric materials, especially PZT, the first term may be ignored, and the ferroelectric capacitor charge is just $Q_F = A_F P$, where A_F is the area of the ferroelectric capacitor. Similarly, the voltage is $V_F = E t_F$, where t_F is the thickness of the ferroelectric capacitor. The internal resistance must also scale with capacitor dimensions and is given by $\rho' = \rho t_F / A_F$. The resultant circuit equation up to sixth order is given by 3.4, where we also define the voltage on the capacitive component as V_{int}.

$$V_F = 2\alpha \frac{t_F}{A_F} Q_F + 4\beta \frac{t_F}{A_F^3} Q_F^3 + 6\gamma \frac{t_F}{A_F^5} Q_F^5 + \rho' \frac{\partial Q_F}{\partial t} \tag{3.4a}$$

$$V_F = V_{int} + \rho' \frac{\partial Q_F}{\partial t} \tag{3.4b}$$

3.4 describes the behavior of the ferroelectric capacitor. Defining I to be the current through the external resistor R, the equation for the total circuit is given by 3.5.

$$V_S = IR + \rho'(I - C_P \frac{\partial V_F}{\partial t}) + V_{int} \tag{3.5}$$

This forms the mathematical framework for the simulation results discussed in 3.3.

3.3 Results of L-K Simulations

The dynamical system described by 3.5 with parameters roughly corresponding to the switching transient experiments for PZT described earlier is solved with a standard fourth-order Runge-Kutta ordinary differential equation solver [37]. The ferroelectric polarization is initialized in the negative spontaneously polarized state. The source voltage is switched from -14 V to +14 V at time t = 0, and then back to -14 V at time t = 40 μs, well after the ferroelectric has switched. The resulting switching transients are depicted in 3.1. The negative capacitance portions of the transients are marked by the vertical dotted lines.

It is interesting to note the behavior of V_{int} with that of V_F, which corresponds to the experimentally measurable ferroelectric voltage. While V_{int} initially rises above 0 V and then goes below 0 V during the negative capacitance portion of the transient, exactly following the equilibrium states of Landau theory. V_F not only begins the negative capacitance transient at a higher voltage, but the drop over the negative capacitance portion is much less, and stays above 0 V. In other words, while the internal "perfect" nonlinear capacitor exhibits large-signal negative capacitance, what is measured is only differential negative capacitance.

Notably, there is a significant departure from experiment in the portion of the transient immediately following the negative capacitance portion. Instead of a gradual change of the slope of the ferroelectric voltage, and a long duration of almost constant voltage, the

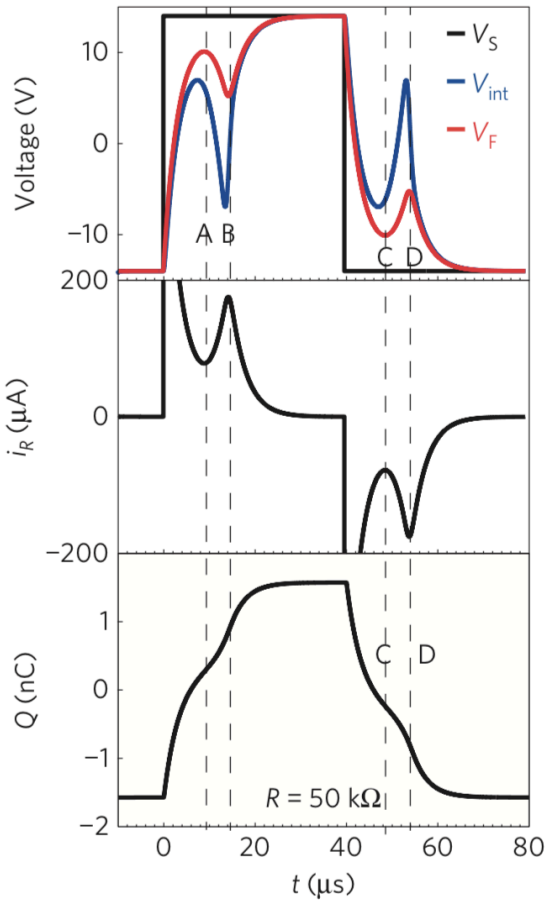

Figure 3.1: Switching transients for a ferroelectric capacitor with applied voltages of +/- 14 V. The top figure shows the internal voltage and the ferroelectric voltage alongside the source voltage. The middle figure shows the current flowing through the resistor. The bottom figure shows the charge on the ferroelectric capacitor. The value of the external resistor is 50 kΩ. From [26].

ferroelectric voltage changes sign abruptly and exhibits charging similar to a normal RC circuit. This strongly suggests that the second positive capacitance portion of the experimental switching transients in 2.7 corresponds to domain wall propagation, a phenomenon which is obviously absent in a single-domain description.

Once the parasitic capacitor current is subtracted off, the resistor current shown in the middle inset of 3.1 can be integrated to yield the ferroelectric charge, plotted in the bottom inset. There is not much to note here except the obvious changes in curvature corresponding to the sign changes of the capacitance. Again, these data may be plotted against the ferroelectric voltage(s) to yield dynamic hysteresis loops. This is carried out and depicted in 3.2.

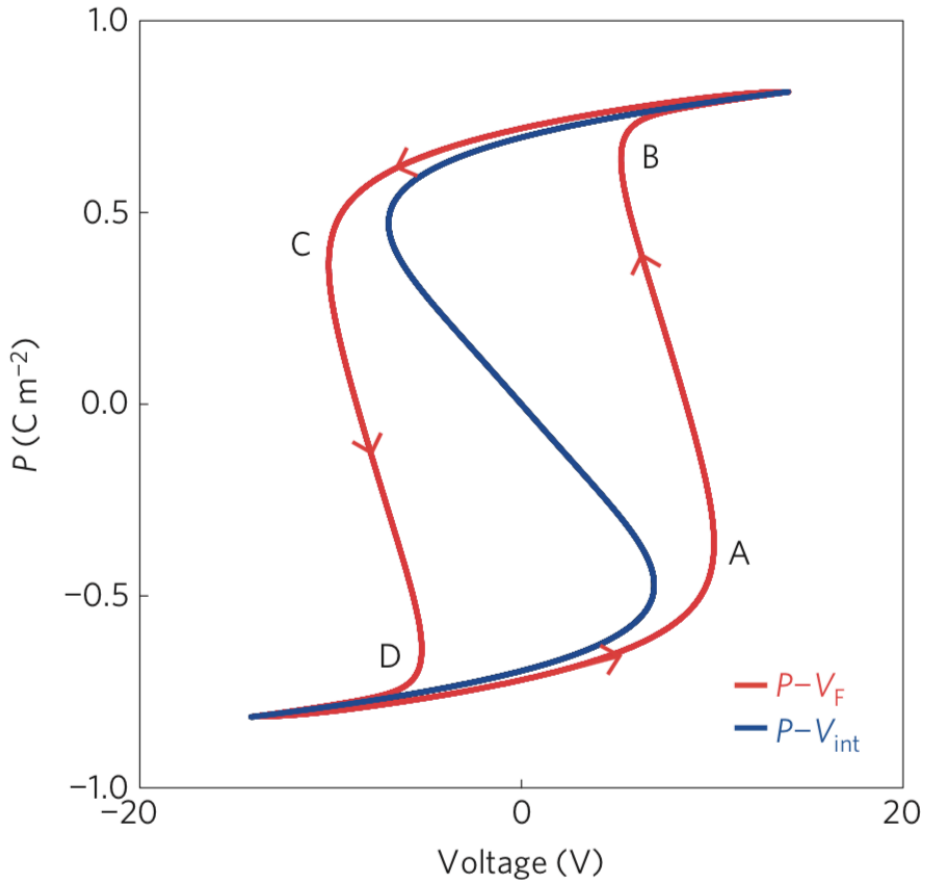

Figure 3.2: Dynamic hysteresis loops for the single-domain Landau-Khalatnikov ferroelectric. The loops are constructed from plotting the voltage transients with the simultaneous capacitor charge calculated from integrating the current. These are the same data in 3.1. From [26].

In contrast to the experimental dynamic hysteresis loops in 2.7, most of the switching portions of the V_F loop have negative capacitance. Again, this is expected from the lack of any domain dynamics in the model. The V_{int} curve just shows the equilibrium states of the Landau-Devonshire theory, independently of the switching dynamics.

Finally, we comment on the effect of varying the external series resistor, shown in 3.3. In the low resistance case ($R = 50k\Omega$), the value of the negative capacitance is lower compared to the high resistance case ($R = 300k\Omega$). The width of the hysteresis is also smaller. Both of these observations can be explained by considering the limit of large and small resistances. In the limit of a large resistance, the switching happens infinitely slowly, and V_F should follow V_{int} exactly. In the limit of no resistance, the switching is limited by ρ', and the source voltage appears instantaneously on the ferroelectric, implying a perfectly rectangular dynamic hysteresis loop with the width of the source voltage, which is necessarily higher than the coercive voltage bounding the S-curve of V_{int}.

3.4 Kolmogorov-Avrami-Ishibashi (KAI) Theory

Kolmogorov [38] and Avrami [39] independently considered a probabilistic phase transformation process under the assumptions of constant boundary velocity and either defect-mediated or homogeneous memoryless nucleation, which Ishibashi applied to ferroelectric switching using Kolmogorov's method [34]. Here, only the two spontaneously polarized states are considered, the jump between them infinitely sharp, aside from the notion of a small critical radius with which domains nucleate. A transition rate related to domain wall velocity and a pseudo-dimensional factor determine the functional form of the switching current in this model, where the susceptibility is completely dominated by domain wall motion. The dimensional factor is motivated by the different forms of domain patterns observed in ferroelectrics, shown in 3.4, in other words it is just the number of spatial dimensions along which the domain walls propagate. In reality, this connection to domain geometry is tenuous, and it is acknowledged in the original work that intermediate cases may exist [34].

Two caveats are necessary here: (1) Importantly, there is no definition given of a ferroelectric voltage, nor any considerations of a Landau free energy functional which depends on locally continuous variables. As such, it cannot predict the existence of a region of negative capacitance states - each point in the volume of the ferroelectric is approximated as always being in one of the two spontaneously polarized states. (2) The purpose of this comparison of KAI theory with experiment is to show that the second positive capacitance portion of the ferroelectric switching transients is well-described by this theory of domain wall motion, and that the transients overall scale according to Merz's Law (3.6) when not in the measurement setup-limited regime [35].

$$r = r_0 exp\{\frac{-E_a}{E - E_0}\} \tag{3.6}$$

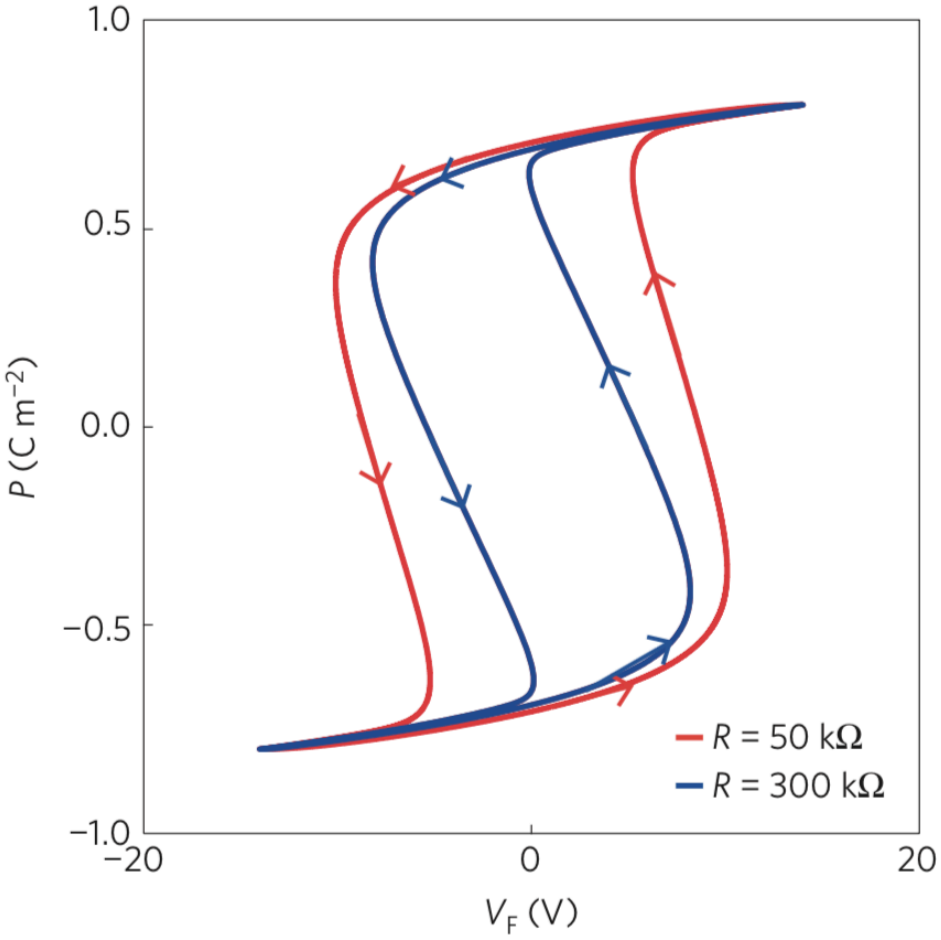

Figure 3.3: Dynamic hysteresis loops for two different values of series resistance, 50 kΩ and 300 kΩ. For a higher series resistance, the ferroelectric voltage more closely follows the internal voltage. From [26].

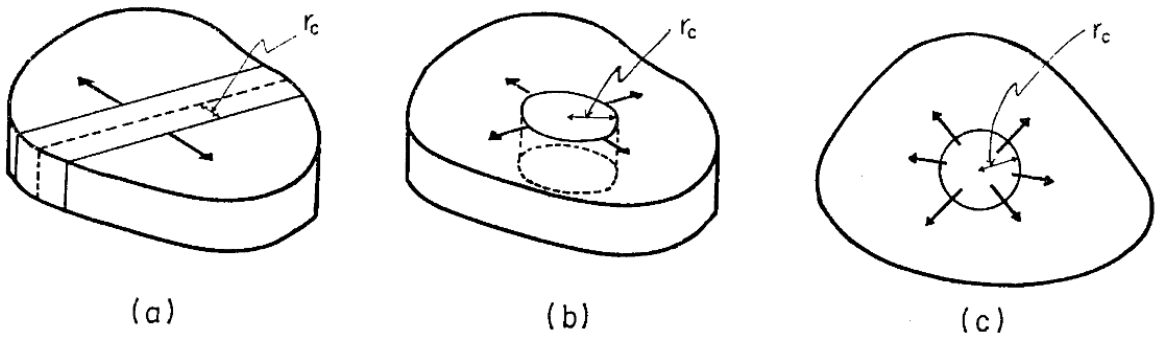

Figure 3.4: Shape of ferroelectric domains for dimensionality factors 1, 2, and 3, for (a), (b), and (c) respectively.

Here r is some rate, which in this case is either domain nucleation probability rate or domain wall velocity.

We briefly recount the derivation by Ishibashi of the switching current of a ferroelectric under a given applied field. It is assumed that the domain wall velocity v is constant for a given applied electric field, and follows a relationship according to Merz's Law. The nucleation rate is considered to either be homogeneous and constant over the unswitched volume, or is determined by a fixed number of nucleation centers representing defects with reduced coercive fields, in which case it is nonzero only for a short time t_1 at $t = 0$, the time the field is switched on.

We calculate the probability $q(t)$ that a given point P has not been switched at a time t. Furthermore we assume that a domain nucleates with a critical nucleus, whose radius is denoted by r_c. A domain formed at a time $\tau < t$ occupies a volume given by 3.7, for some geometrical constant C.

$$S(t, \tau) = C\{r_c + v(t - \tau)\}^n \tag{3.7}$$

Therefore, if a domain nucleates in a region of volume S centered around P at time τ, P will be switched at time t. This is illustrated in 3.5. The probability that this does not occur between τ and $\tau + \Delta\tau$ is just $1 - S(t, \tau)R(\tau)\Delta\tau$ for small $\Delta\tau$. $R(\tau)$ is a nucleation probability per unit time per unit volume at time τ. We write t and τ in terms of $\Delta\tau$. Define $i := t/\Delta\tau$ and $j := \tau/\Delta\tau$. Now we must consider the product of such probabilities for all values of τ from 0 to t, each of which depends on τ. This quantity, which is the probability that the point P has not switched by time t, is given by the expressions in 3.8. In going from 3.8a to 3.8b, we have taken the natural logarithm of both sides, converted the product into a sum, and expanded each term to first order in $\Delta\tau$.

$$q(t) = \prod_{i=0}^{j}[1 - R(i\Delta\tau)S(j\Delta\tau, i\Delta\tau)\Delta\tau] \tag{3.8a}$$

$$ln\{q(t)\} = -\sum_{i=0}^{j}[R(i\Delta\tau)S(j\Delta\tau, i\Delta\tau)\Delta\tau] \tag{3.8b}$$

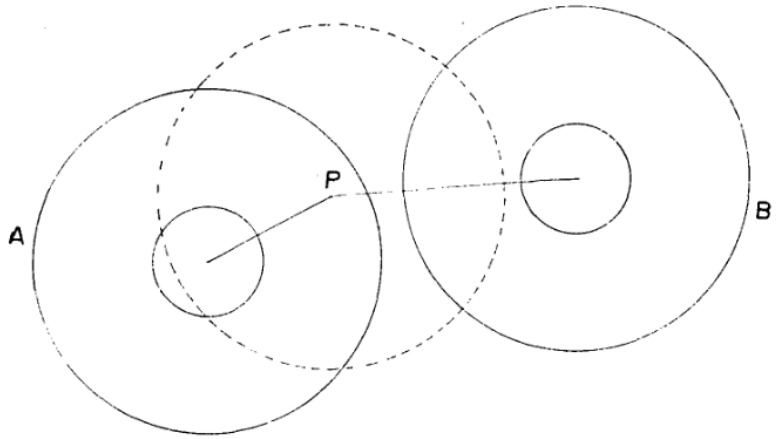

Figure 3.5: The point P is contained in the nucleation volume of size S centered on A, but not of the one centered on B. A is correspondingly inside the nucleation volume of size S centered on P, while B is not. The inner circles of the nucleation volumes indicate the size of the critical radius with which domains nucleate. From [34].

In the limit as $\Delta\tau \to 0$, we obtain the integral in 3.9.

$$ln\{q(t)\} = -\int_0^t R(\tau)S(t,\tau)d\tau \tag{3.9}$$

Finally, we define $x(t)$ to be the switched fraction of the ferroelectric at time t, which is clearly $x(t) = 1 - q(t)$, given in 3.10.

$$x(t) = 1 - exp\{-\int_0^t R(\tau)S(t,\tau)d\tau\} \tag{3.10}$$

The integral in the exponent evaluates to the expressions in 3.11, for constant nucleation we obtain 3.11a and for defect nucleation we obtain 3.11b. They are equivalent up to a multiplicative constant related to critical radius and differ by one in the dimensionality

factor. We do not attempt to characterize the nucleation one way or the other, as there may be intermediate cases, and because of the aforementioned impreciseness of the dimensionality factor.

$$ln\{1 - x(t)\} = \frac{-CR}{v(n+1)}\{(r_c + vt)^{n+1} - r_c^{n+1}\} \tag{3.11a}$$

$$ln\{1 - x(t)\} = -CRt_1(r_c + vt)^n \tag{3.11b}$$

This can be converted into an expression of the form in 3.12.

$$x(t) = 1 - exp\{K(t + t_0)^n\} \tag{3.12}$$

t_0 is r_c/v, which we find to be negligible. Thus the two parameters used in our fitting are K and n, henceforth referred to as the Avrami constants.

3.5 Fitting of Experimental Data to KAI Theory

The samples used in these experiments are identical to those used in 2 and we refer the reader to 2.3 and 2.4 for detailed information on the experimental methods. A schematic of the device is shown again for convenience. The low temperature measurements reported on here were done in a LakeShore TTPX probe station cooled with liquid nitrogen. A difference we mention is that electrodes of area $A = (62\mu m)^2$ are used, though this has no effect on the observed dynamics besides changing scaling the time constants.

A typical ferroelectric voltage response is shown in the blue curve of 3.7. The step response is divided into three main portions. (1) An initial rise to some voltage above the coercive voltage, whose value will depend on the series resistance and the amplitude of the source voltage pulse. (2) A negative capacitance portion, referred to as the "negative capacitance transient," whose duration is called t_1. (3) A final positive capacitance portion, in which V_F rises to meet the source voltage V_S. We define $t_2 = 1/K^{1/n}$ for the least error fit of the Avrami constants. The scaling of these times t_1 and t_2 with external parameters is used to characterize these transients in terms of the KAI theory. In 3.7, the red curve shows the result of fitting K and n to the t_2 portion of the transient. The fitting of the KAI model is carried out in the t_2 regime because for the kinds of experiments carried out to verify the KAI model, there is no large series resistance to make the earlier portions observable. This is clear from Ishibashi's analysis of the switching current at $t = 0$.

Now we verify that Merz's Law describes the data well. In this case, we expect t_1 and t_2 to scale according to 3.6, for some value of E_a. E_0 is chosen to compensate for the asymmetry of the hysteresis loop. Both t_1 and t_2 are seen to saturate in our experiments, so we use the saturated value as a measure of r_0. This is the central result of the comparison of our experiment to KAI theory, and it is shown in 3.8.

To firmly exclude the possibility of the negative capacitance signature arising from slow trapping and de-trapping events at defect centers, the experiment is carried out at 100 K. The

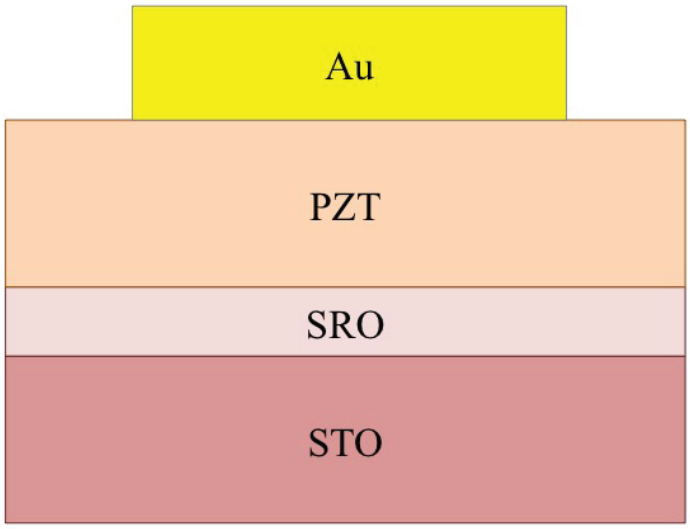

Figure 3.6: Schematic of the ferroelectric PZT capacitors used in this experiment. 10 nm of SRO is deposited on an STO substrate, followed by 60 nm of PZT, and finally a stack of 5 nm Au / 40 nm Ti / 5 nm Au, which is patterned into a top contact.

coercive field increases with decreasing temperature, as expected, and this affects the particular shape of the step response. Importantly, the negative capacitance signature remains, and therefore cannot be due to defect states, which would freeze out at such temperatures. This is depicted in 3.9.

In the previous work identifying negative capacitance in a ferroelectric capacitor, the external series resistance is typically chosen to lie in the hundreds of kΩ so that the dynamics occur on the scale of tens of microseconds. In principle, lowering the series resistance arbitrarily could reveal the intrinsic speed limitations of the material, i.e. provide a characterization of internal inertial and damping mechanisms. Instead, we find in 3.10 that the dynamics scale linearly with resistance down to about 500Ω at a switching field of 1.67 MV/cm, near the breakdown field of the PZT films. At this point, the speed of our measurement becomes limited by the circuit slew rate (330 mV/ns), and below 200Ω the signal becomes obscured by ringing at the source as well as time resolution of the oscilloscope. Nevertheless, we observe values of t_1 down to 30 ns, so that intrinsic switching occurs at least that fast. This would indicate a switching time in at worst the picosecond range for a transistor-scale device. A proper measurement of intrinsic switching speed in this manner would necessitate impedance matching and higher quality driving source [13]. For the purposes of negative capacitance transistors, the switching speed is irrelevant as the material is not operating in the hysteretic regime.

Our data here are consistent with the interpretation of the negative capacitance signature as arising from simultaneous nucleation events, where a fraction of the ferroelectric passes

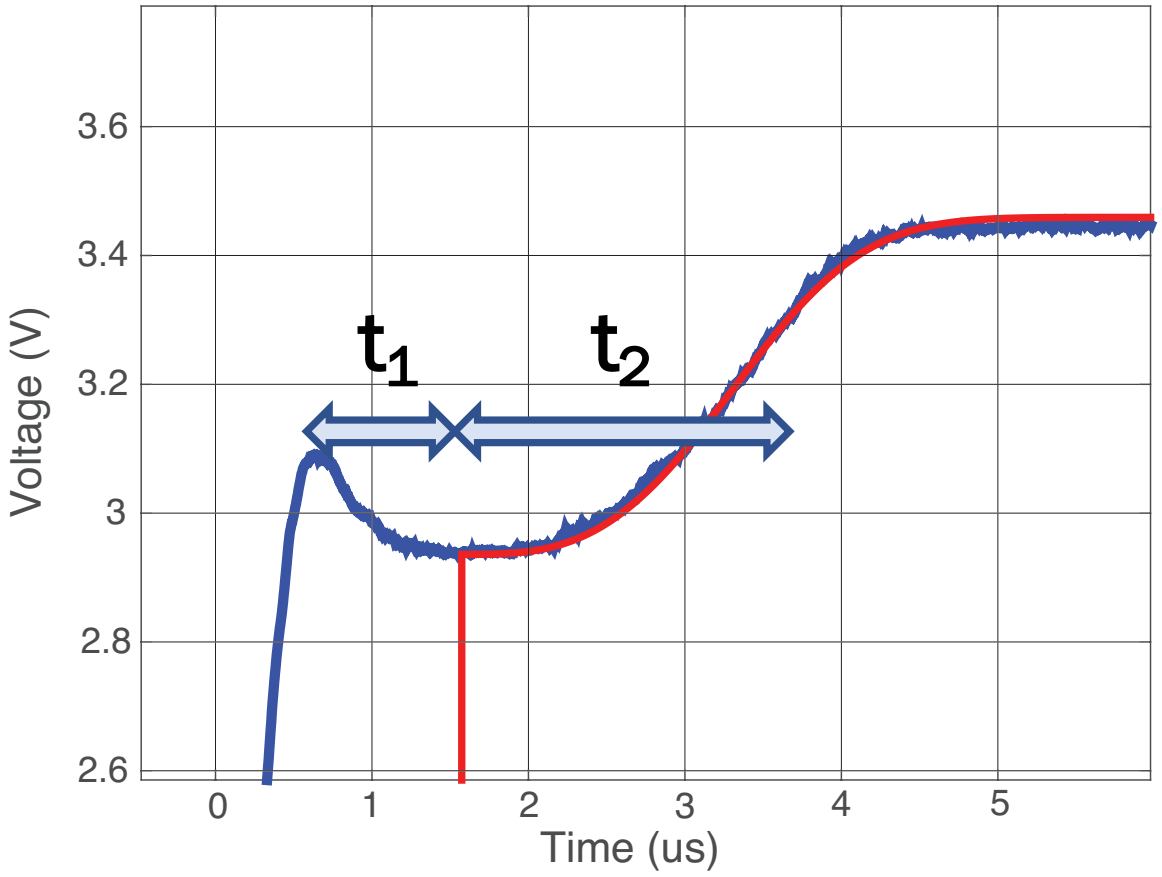

Figure 3.7: The blue curve shows a typical V_F for a switching ferroelectric. The source voltage V_S is +3.45 V, and the external resistance $R = 1053\Omega$. The red curve shows the ferroelectric voltage expected from this measurement according to best fit of the KAI model.

through the $P = 0$ state, in a span of time as low as 30 ns. We emphasize that the ferroelectric is not switching as a single domain, as there is clear evidence of domain wall motion. Given that the susceptibility diverges on the path from $+P_S$ to $-P_S$, it is entirely conceivable that even a small correlation among nucleation events could result in the negative capacitance contribution to the response overwhelmingly dominating the overall response of the PZT film. In fact, this notion is verified for the static negative capacitance case through atomistic simulation in [27], where it is shown that a negative local dielectric susceptibility in a depolarized fraction of the ferroelectric material dominates the overall response in the negative capacitance regime.

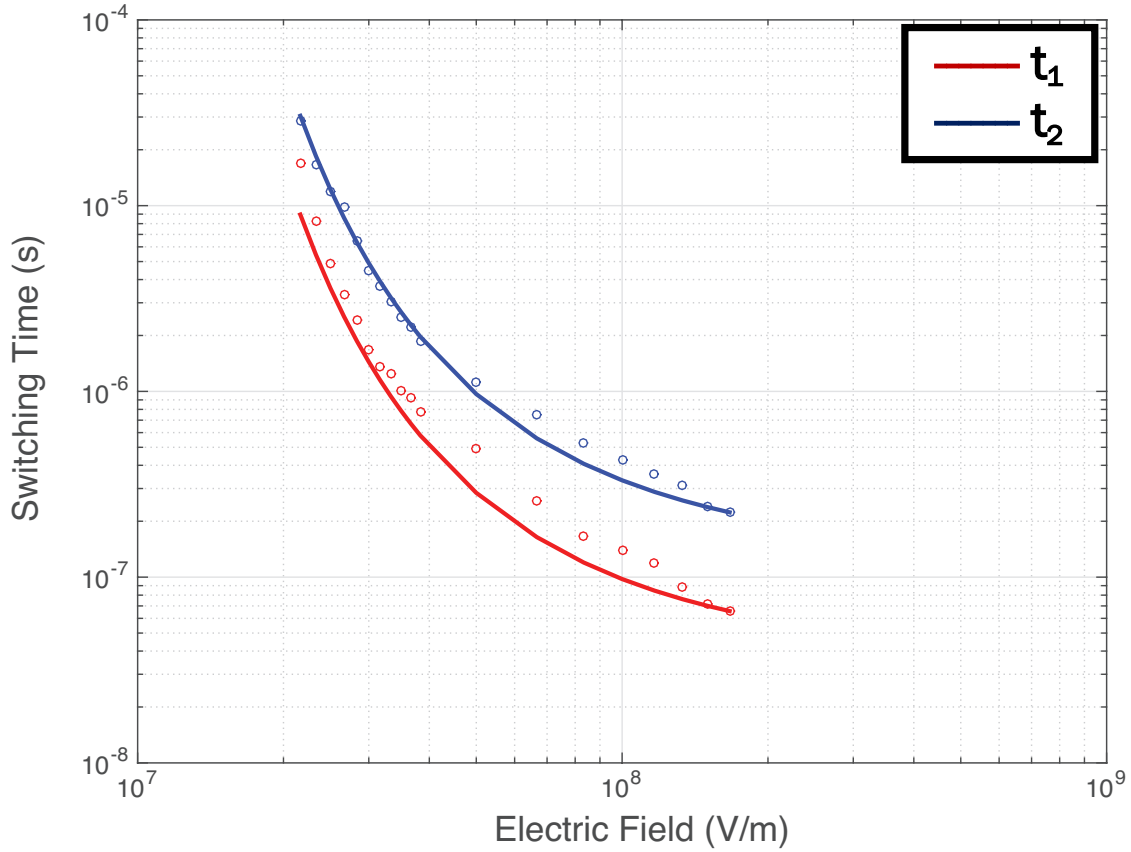

Figure 3.8: The dots indicate experimental values of t_1 and t_2 for different values of applied field. The trendlines indicate best fit to Merz's Law. Reasonably good agreement is obtained.

3.6 Phase-Field Modeling

As mentioned previously, while the Landau-Khalatnikov equation provides a definitely relationship between polarization state and electric field, it does not contain any information about the formation of domains. The Kolomogorov-Avrami-Ishibashi model, while giving an accurate quantitative description of the polarization switching current due to domain propagation, does not contain any information about the microscopic physics or the susceptibility. A phase-field model integrates the two aspects by generalizing the Landau-Khalatnikov equation to allow for spatial variation of the now-3D polarization, but at the cost of complexity. This work is described further in [40].

The polarization is described by the time-dependent Ginzburg-Landau (TDGL) equation, 3.13, which is closely related to the L-K equation [36].

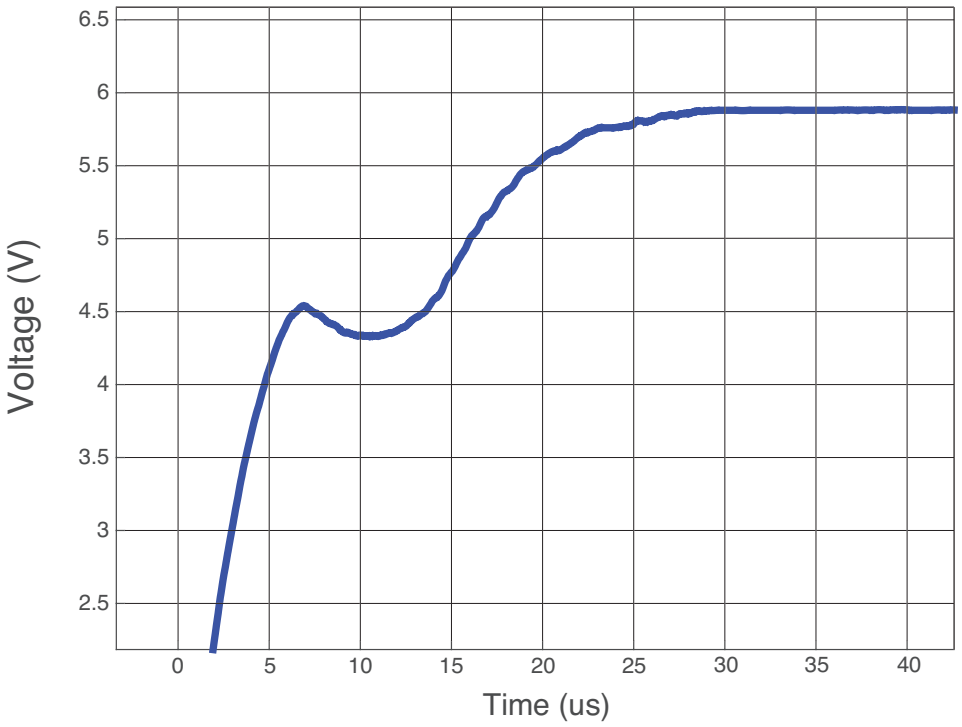

Figure 3.9: V_F as a function of time for a PZT capacitor at 100 K in response to a +5.8 V pulse. The parasitic capacitance of this experimental setup is much higher, on the order of 100 pF, yet the negative capacitance signature remains. The series resistance $R = 9600\Omega$.

$$\frac{\delta \vec{P}}{\delta t} = -L\frac{\delta F}{\delta \vec{P}} = -L\frac{\delta F_{local} + \delta F_{wall} + \delta F_{elec}}{\delta \vec{P}} \tag{3.13}$$

The free energy functional includes, as in the case of the L-K equation, a local internal energy, a coupling to the external electric field, but also a term F_{wall} which represents domain wall or gradient energy. The form of the free energy functional is given in 3.14. The factor L here is equivalent to $1/\rho$ in the L-K equation.

$$F_{local} = \int_\Omega \sum_{i=x,y,z} (\alpha_1 P_i^2 + \alpha_{11} P_i^4) + \sum_{i,j=x,y,z} \alpha_{21} P_i^2 P_j^2 + ...d\Omega \tag{3.14a}$$

$$F_{wall} = \int_\Omega G_{11} \sum_{i,j=x,y,z} (\partial_i P_j)^2 + ...d\Omega \tag{3.14b}$$

$$F_{elec} = \int_\Omega -\vec{E} \cdot \vec{P} d\Omega \tag{3.14c}$$

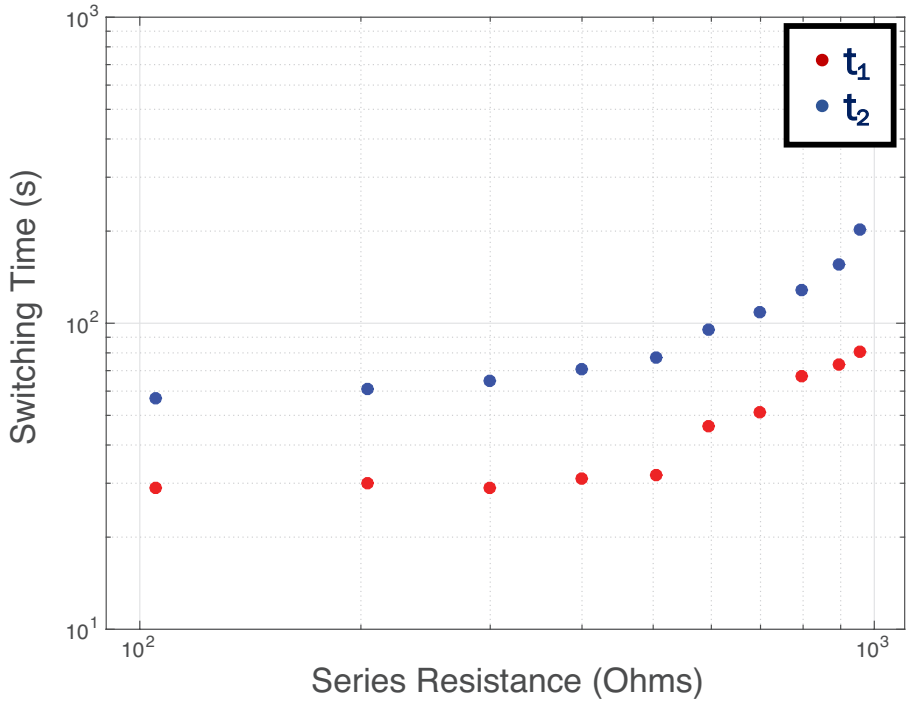

Figure 3.10: Dependence of characteristic switching times as a function of external series resistance. The system follows a linear scaling as one would expect, until the slew-limited region is reached.

Long-range dipolar and elastic interactions are ignored here for simplicity, although they could be included in a future work. Taylor expansions are carried out to sixth order with coefficients for $PbTiO_3$. With the external resistor, the ferroelectric voltage depends on both the source voltage and the current flowing in the circuit. This implicit definition of $\frac{\delta \vec{P}}{\delta t}$ makes the problem a differential-algebraic equation, rather than a proper differential equation. The distinction is important for numerical purposes, and the IDA (implicit differential-algebraic) solver from the Sundials package is used accordingly [41].

To explore the dynamics fully, we examine switching with both pinned defects and reduced-coercivity defects. Even though domain nucleation is absent in the first case but not in the second, we find no significant difference in ferroelectric dynamics between the two cases. 3.11 shows the simulated ferroelectric step response, which is similar to the experimental data shown in 2.4. In this simulation, 15 defects have been placed at random locations in the film. The simulation volume is 300 nm x 300 nm x 15 nm. Prior to application of the source voltage pulse, the ferroelectric is initialized in the opposite orientation. 3.12 visualizes the ferroelectric polarization at different points in the switching process. After the pulse is applied, reverse domains begin to grow increasingly and negative capacitance

is observed. As domain growth saturates, the ferroelectric voltage gradually rises to meet the source voltage. This demonstrates that the negative capacitance transients observed experimentally are consistent with a multidomain picture of ferroelectricity.

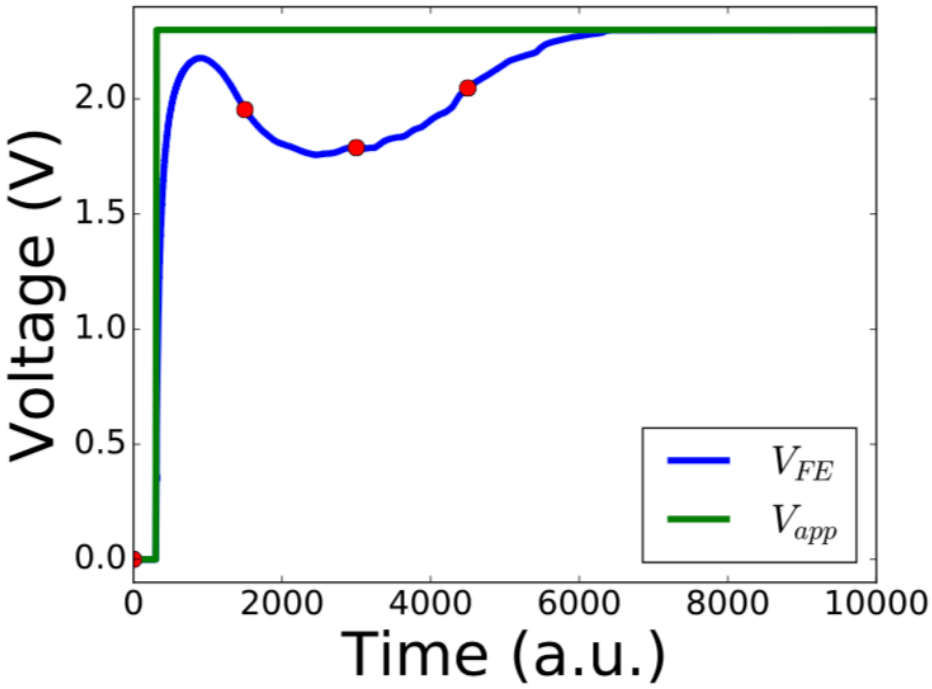

Figure 3.11: Transient response of a ferroelectric in a series RC circuit to a switching pulse, modeled by the TDGL equation. The ferroelectric voltage is indicated by V_{FE}, and the source voltage by V_{app}. The points marked on the trace correspond to 3.12 (a)-(d), from left to right. From [40].

3.7 Conclusions

The goal of the works in this chapter were to probe further into the RC step response experiments of 2 in order to understand how the data could be reconciled with various theoretical models. The L-K equation predicted some coarse aspects of the observed data, importantly the negative capacitance signature and a widening of the hysteresis loop with lower resistance, but was found to be inadequate for a quantitatively accurate description. Its conceptual importance is difficult to overstate, however, as it shows that hysteresis itself arises from the existence of unstable states in a double-well energy landscape. The KAI model, on the other hand, provides excellent quantitative accuracy in a certain region of the transient response, but cannot capture many physical details that are of interest. The

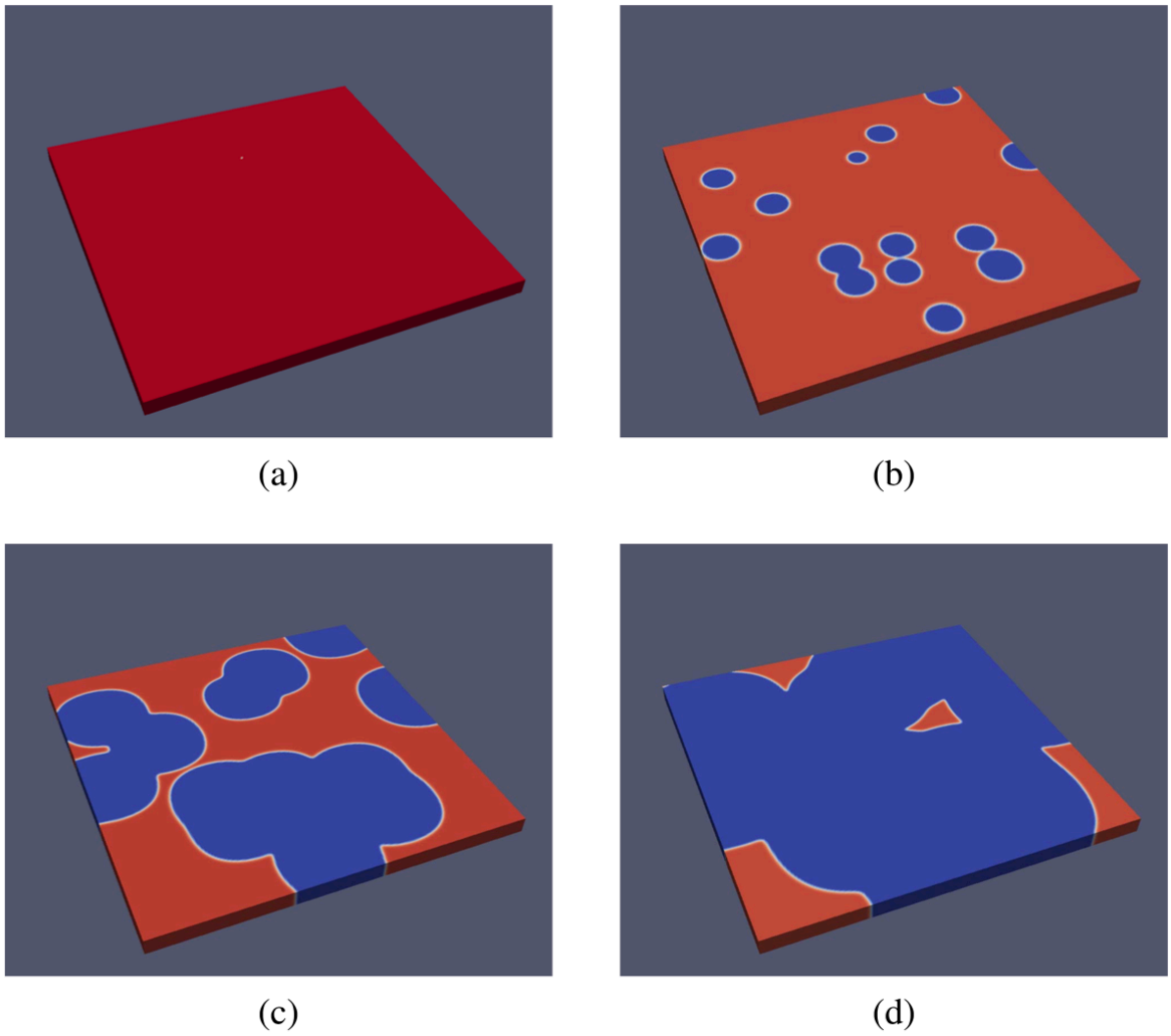

Figure 3.12: Visualization of the ferroelectric switching. The color indicates the out-of-plane component of the surface polarization. Red corresponds to "up" polarization and blue to "down" polarization. (a) The ferroelectric before switching is poled in the "up" state. (b) Negative capacitance is observed as the fraction of the material in the depolarized domain walls accelerates. (c) Domain wall propagation and now dominates the current. (d) Most of the ferroelectric is switched, and the ferroelectric voltage approaches that of the source. From [40].

multidomain phase-field model captures the best aspects of both pictures, and allows us to create a quantitatively accurate model that also gives an insight into the microscopic details of the switching process.

Chapter 4

Intrinsic Speed Limitations of Negative Capacitance Transistors

4.1 Introduction

Digital processors are driven by an internal clock, represented as a square voltage wave that drives the switching of various synchronous components of the architecture [42]. With each cycle of the clock, the program executes another step. What were the inputs to a given logic unit in the previous cycle suddenly appear as the processed values at the outputs, ready to be fed to the next stage of a pipeline. In order to maintain consistency between adjacent stages of a digital pipeline, there are protocols for the various delays allowed in the system. This is analyzed at the architecture level in terms of the abstractions of Boolean logic gates and information about the capacitance of interconnects. Looking below these abstractions, analysis at the device level in MOSFET-based architectures depends on the total gate capacitance, which includes parasitic capacitances [10]. When considering the introduction of a ferroelectric into the gate stack, any added response delay cannot change the overall transistor delay in order for successful integration. Thus the question of the intrinsic response delay of a ferroelectric is critical to realizing negative capacitance transistors.

To date, the fastest switching of ferroelectric polarization was realized by J. Li et al. in 2003 in a femtosecond laser-driven switching of a $Pb(Nb_{0.04}Zr_{0.28}Ti_{0.68})O_3$ ferroelectric in 220 picoseconds [43]. Given that the clock speeds of modern processors are around 3-4 GHz, a naïve consideration from this viewpoint is pessimistic - 220 ps is nearly the entire clock cycle. However, in a negative capacitance transistor, the time required for full switching is not relevant, as the switchable polarization must be substantially greater than the inversion charge in order to maintain amplification throughout the subthreshold regime. Therefore the right question is: "How long does it take to push an inversion layer's worth of charge through a ferroelectric?"

Previous attempts to answer this question in the context of negative capacitance devices have relied on the previously discussed Landau-Khalatnikov equation [28], which treats the

ferroelectric as a nonlinear capacitor in series with a resistor,

$$\rho\frac{\partial P}{\partial t} + \nabla_P U = 0 \tag{4.1}$$

Here U is the Landau free energy density, P is the polarization, and ρ represents heat dissipation within the ferroelectric. Since we are considering a thin film capacitor, we will analyze only a single component of polarization, the out-of-plane component, to which the spontaneous dipole moments are confined by the thin film geometry, and which also determines the circuit charge. U can be written as a Taylor series in P^2,

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 + ... - EP \tag{4.2}$$

Note that α must be negative for a ferroelectric.

A significant shortcoming of the above model is that ρ has to be been taken as an arbitrary fitting parameter. However, ρ has a definite physical meaning. It is the damping in the ferroelectric material and can be obtained from the full-width half maximum (FWHM) of the electromagnetic absorption spectrum. Therefore, a fully consistent analysis of ferroelectric dynamics requires one to consider both dissipation and inertia, which manifests as an inductance. We now demonstrate such an analysis for doped orthorhombic hafnium oxide (HfO_2), the leading candidate for CMOS integration of ferroelectricity. The resultant predicted delay of the material is on the order of 270 femtoseconds, similar to what will be obtained for high-κ HfO_2.

This chapter describes an attempt to answer that question by providing a rough but physically compelling theoretical framework with which to analyze the delay. The damped mass-spring picture is laid out in 4.2. These results are then implemented into a MATLAB simulation, using parameters taken or extracted from existing experimental work. The results of the simulation are then analyzed and discussed in the following sections, 4.3. Finally, the chapter is concluded and future directions of research are outlined in 4.4. This chapter is primarily based on [44], from which all figures are taken unless indicated.

4.2 Theory

Combining equations 4.1 and 4.2, we obtain the following dynamical equation for the polarization density,

$$E = \rho\frac{\partial P}{\partial t} + 2\alpha P + 4\beta P^3 + 6\gamma P^6 + ... \tag{4.3}$$

Now we show that the Landau-Khalatnikov equation above is formally equivalent to the slow speed limit of a classical nonlinear dipole oscillator, depicted in 4.1, and derive an equivalent circuit model. Consider Newton's second law applied to a damped dipole spring of charge q, separation x, and mass m in an external field E,

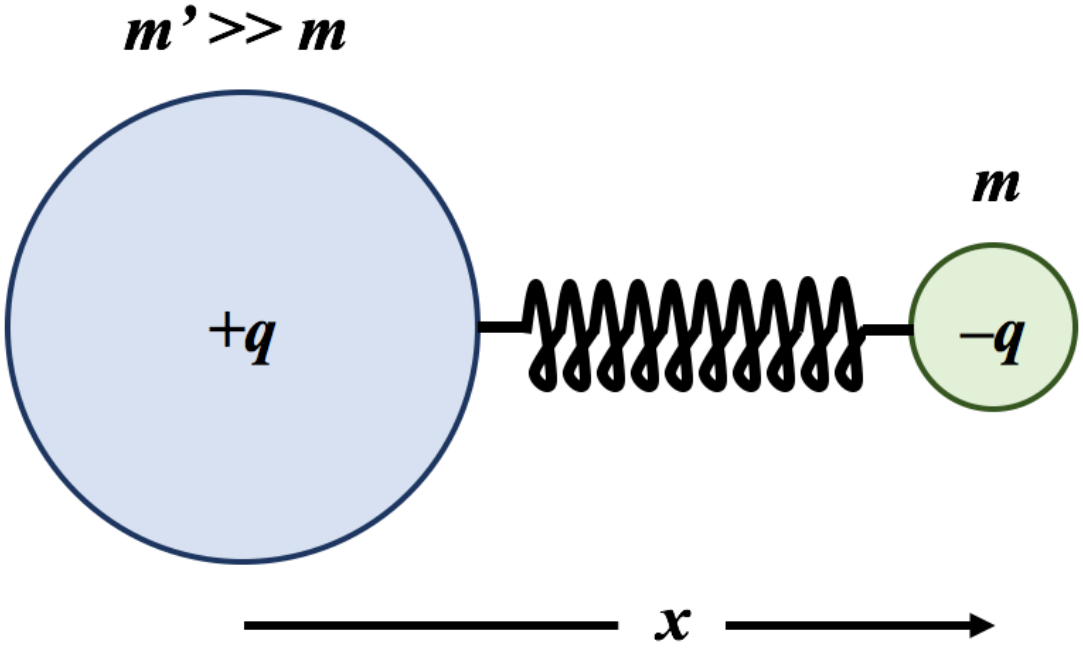

Figure 4.1: Charge-mass spring system used to model polarization. The situation shown where the smallest mass m is negatively charged is consistent with HfO_2.

$$\begin{aligned} m\frac{\partial^2 x}{\partial x^2} &= F_{damping} + F_{spring} + F_{external} \\ &= -\eta\frac{\partial x}{\partial t} - kx - k'x^3 - k''x^5 - ... - qE \end{aligned} \tag{4.4}$$

where η is the damping coefficient and k, k', etc. are the nonlinear spring coefficients. If we consider a non-interacting system of such dipoles with volume density N, we may define a polarization density $P = -Nqx$. Then 4.4 becomes

$$E = \frac{m}{Nq^2}\frac{\partial^2 P}{\partial t^2} + \frac{\eta}{Nq^2}\frac{\partial P}{\partial t} + \frac{k}{Nq^2}P + \frac{k'}{N^3q^4}P^3 + \frac{k''}{N^5q^6}P^5 + ... \tag{4.5}$$

Let us make the following identifications,

$$\rho = \frac{\eta}{Nq^2} \tag{4.6a}$$

$$\alpha = \frac{k}{Nq^2} \tag{4.6b}$$

$$\beta = \frac{k'}{N^3q^4} \tag{4.6c}$$

$$\gamma = \frac{k''}{N^5q^6} \tag{4.6d}$$

In addition, let us define l,

$$l = \frac{m}{Nq^2} \tag{4.7}$$

which one may identify as the "kinetic inductance" and has units of $H \cdot m$. With these substitutions, 4.5 becomes

$$E = l\frac{\partial^2 P}{\partial t^2} + \rho\frac{\partial P}{\partial t} + 2\alpha P + 4\beta P^3 + 6\gamma P^5 + ... \tag{4.8}$$

Note here that in the slow limit $\frac{\partial^2 P}{\partial t^2}$ can be made small, rendering 4.8 the same as 4.3. This shows that the traditional Landau-Khalatnikov equation is simply a slow limit approximation to the classical equation of motion.

In order to relate this to a circuit perspective, we scale the variables by the geometric dimensions of the ferroelectric capacitor, area A, and thickness d,

$$Ed = \frac{ld}{a}\frac{\partial^2(PA)}{\partial t^2} + \frac{\rho d}{A}\frac{\partial(PA)}{\partial t} + \frac{2\alpha d}{A}(PA) + \frac{4\beta d}{A^3}(PA)^3 + \frac{6\gamma d}{A^5}(PA)^5 + ... \tag{4.9a}$$

$$V = L\frac{\partial I}{\partial t} + RI + C^{-1}(Q)Q \tag{4.9b}$$

Thus the ferroelectric capacitor is equivalent to the series combination of an inductor, resistor, and nonlinear capacitor.

4.3 Simulation Results

Equation 4.9b now provides a well-defined way to extract the parameters of the equation l and ρ from fitting to the resonance peak (4.5 THz) and FWHM obtained from Fourier transform infrared spectroscopy (FTIR) of HfO_2 shown in figure 4.2 [45]. The extracted l corresponds to m of 47 amu per dipole, and the extracted ρ is 0.18 $W\dot{c}m$. The linear capacitance value in the model is determined from the low-frequency permittivity. The

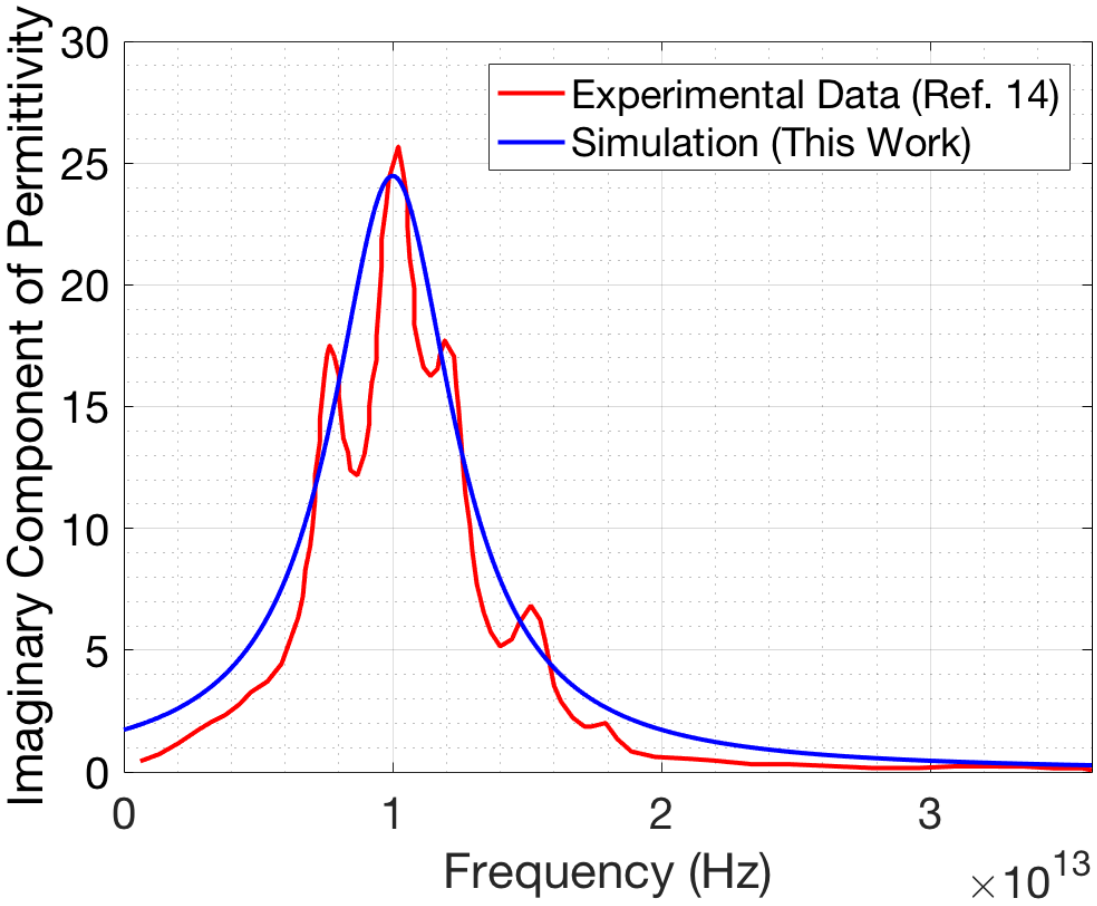

Figure 4.2: Experimental vs. simulated electromagnetic absorption spectra for HfO_2. Experimental data were obtained with FTIR. The right axis shows absorbed power equivalent to the imaginary component of the permittivity on the left axis. Adapted from [45].

nonlinear coefficients up to sixth order are fitted to the coercive field (E_C) and remnant polarization (P_r) from hysteresis loops [46].

It is important to note that, now, there is no flexibility to arbitrarily choose the value of ρ. Rather, the linewidth of the spectrum completely specifies ρ. This is to be distinguished from studies using the conventional Landau-Khalatnikov equation where ρ simply shows up as a resistor and, depending on the RC delay of a specific experiment, which is often determined by spurious elements such as cable capacitance, could easily be fitted to a wide range of values. Indeed, this practice in literature has led to much confusion as to the value of ρ. We hope that our work in this chapter will help resolve the ambiguity in the determination of ρ. Note also that, we expect these parameters to be representative of doped HfO_2 as well because the ferroelectricity is due to the motion of oxygen atoms and the resonance lineshape

should not be significantly affected by doping.

The dependence of ρ on N can be understood by noting that if the spring damping constant η and the charge q are held constant, a smaller lattice distortion is needed to yield a given polarization density. However, one may also expect the damping to increase with density, so it is impossible to validate such scaling relations with the limited experimental data at hand.

The extracted parameters are next used in 4.9a. The ferroelectric is initialized to be poled in the negative direction, and a field is turned on at t = 0 with a rise time of 100 fs. The field magnitudes are chosen to represent realistic operation, in the hundreds of mV. The switching transients are shown in figure 4.3 and summarized in figure 4.4

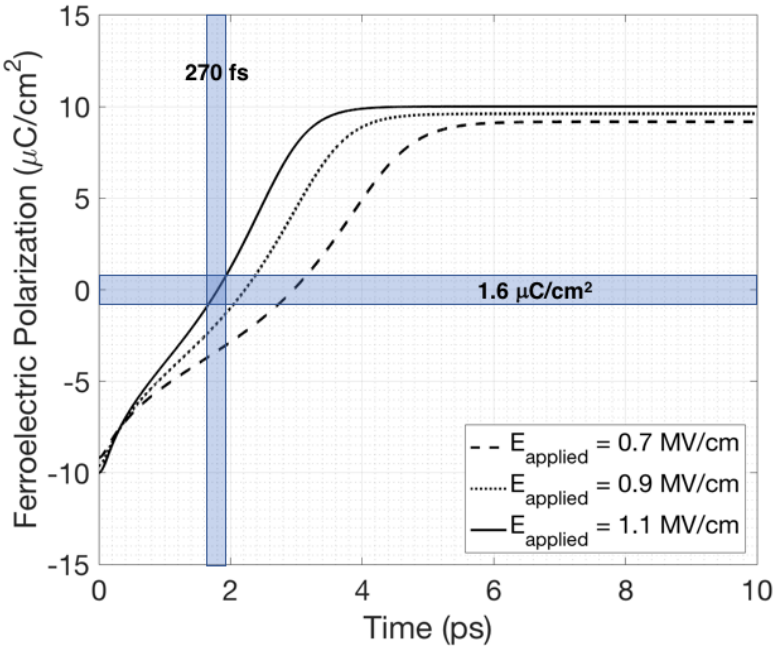

Figure 4.3: Switched charge as a function of time, starting from the negatively poled state for various applied fields. The coercive field (E_C) is 0.7 MV/cm, and each transient has been centered around 0 μC/cm^2. The horizontal bar represents typical surface charge density in inverted silicon [10], and the vertical bar indicates the time needed to switch that charge for an applied field of 1.1 MV/cm. The intrinsic delay is found to be around 270 fs.

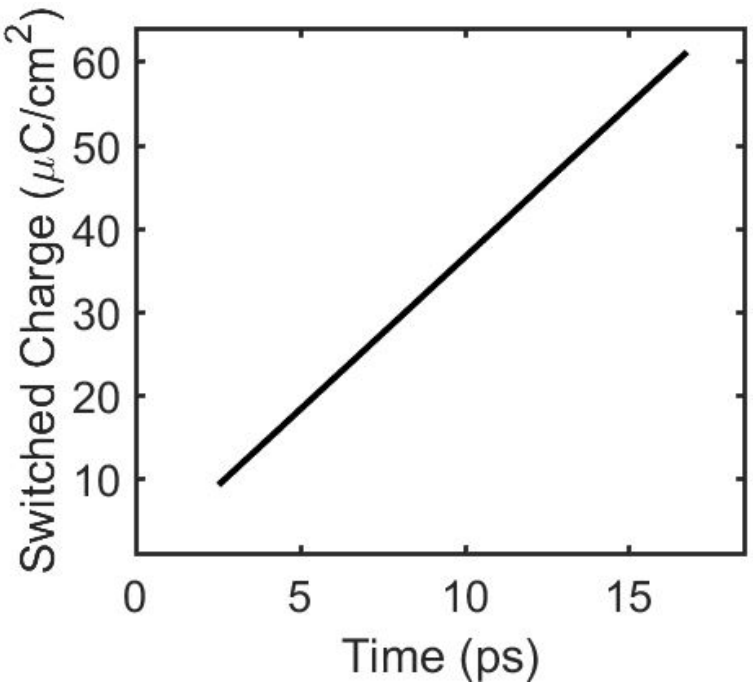

Figure 4.4: Switching times (duration until 86% of source voltage appears across the capacitive component) for various values of switched charge ($2P_r$) with an applied field of 1.1 MV/cm.

4.4 Conclusions

We have developed a theoretical framework to analyze the polarization response delay in ferroelectrics. By restoring the inertial term to the Landau-Khalatnikov equation, the dynamic constants for ferroelectric HfO_2, including ρ, were obtained from frequency dependent dielectric constant measurements and quasi-static hysteresis loops. In this way, ρ is not just a fitting parameter, but represents the experimentally measured loss. Furthermore, including the inertia of the lattice ions paints a complete picture of the ferroelectric dynamics and of the delay between application of the gate voltage and the ferroelectric charge response. Indeed, the consideration of inertia in ferroelectrics goes at least as far back as 1967 [47]. Particularly in the analysis of response delay, it is critical to include inertia.

Solving the modified Landau-Khalatnikov equation yielded preliminary predictions of intrinsic delay in doped HfO_2, which was found to be around 270 fs. The use of HfO_2 as a high-κ dielectric in standard CMOS fabrication [32], along with the ease with which its ferroelectric and even antiferroelectric properties can be tuned [31], is encouraging for simultaneously achieving capacitance matching and very low response delay in negative capacitance FETs.

Chapter 5

External Connection of a Ferroelectric Capacitor to Short-Channel FinFETs

5.1 Introduction

Moving toward the ultimate goal of using ferroelectric negative capacitance for voltage amplification in high-performance digital logic, we consider the effects of connecting an epitaxial ferroelectric capacitor to the gate of a MOSFET, specifically a short-channel Si FinFET. As noted before 4, many different microstates of the ferroelectric material can correspond to the same net polarization, so that the real value of capacitance will depend on the trajectory the material takes through its high-dimensional phase space. Furthermore, the ferroelectric energy landscape itself may be altered when coupled to the stabilizing capacitance [27]. Such considerations preclude successful capacitance matching using quasistatic hysteresis loops of isolated ferroelectric capacitors, and necessitate investigation into the behavior of ferroelectrics when coupled to a transistor. Fortunately, a transistor is itself an excellent charge sensor. If the underlying transistor characteristics are well understood, the transfer characteristics of the combined ferroelectric-FET system can yield insight into the charge-voltage behavior of the ferroelectric.

The simplest such experiment involves connecting a ferroelectric capacitor to the gate contact of a separately fabricated FET with a wire, which is the approach taken here. We henceforth refer to this composite device the negative capacitance FinFET (NC-FinFET). The ferroelectric capacitor is much larger than the short-channel FinFETs used in this experiment. As such, we do not expect to achieve good capacitance matching [48], where the absolute value of the negative capacitance is only slightly larger than the capacitance of the FET, so that there is a large amplification and no hysteresis. Large hysteresis in the I_dV_g is indeed observed for all drain voltages in both n-type and p-type FinFETs, as is extremely steep subthreshold slope - down to 8.5 mV/decade for over eight orders of magnitude of drain current.

Based on the measurements and equivalent circuit model of the NC-FinFET, we also

outline a general procedure for the extraction of the ferroelectric charge-voltage characteristics, the S-curve. We find that, due to the charge balance conditions, only a small fraction of the ferroelectric remanent polarization is switched in a NC-FinFET. We also briefly discuss efforts to simulate transfer characteristics of the NC-FinFET through a self-consistent solution of Berkeley SPICE Insulated-Gate-FET Model:Common Multi Gate (BSIM-CMG) model [49] and the Landau-Devonshire model for ferroelectric [20]. The simulated and experimental characteristics are found to be in excellent agreement. The results in this chapter are primarily from [50], from which all figures are taken unless noted.

5.2 Experimental Setup

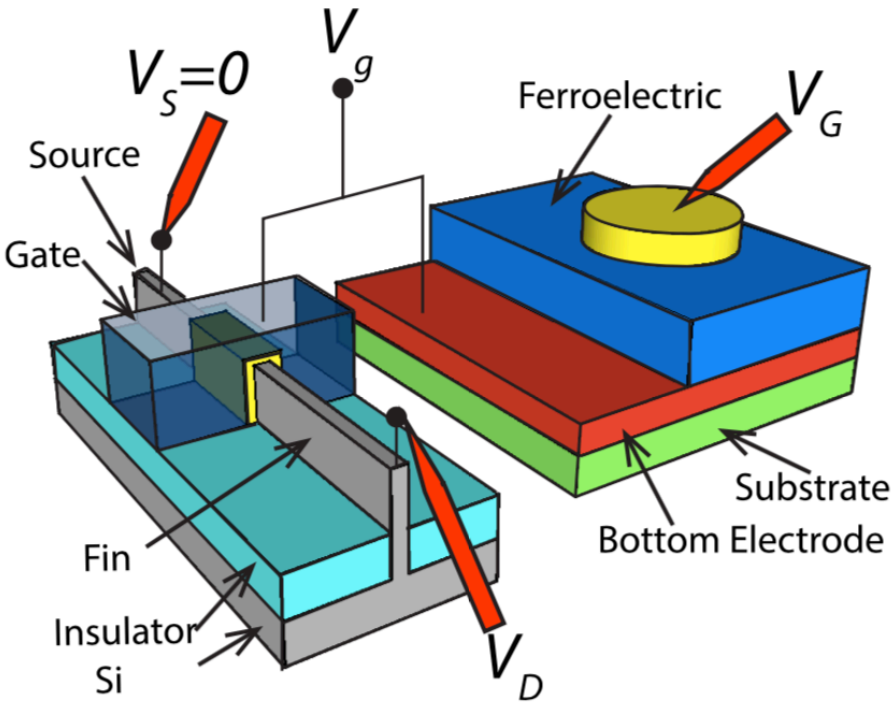

Figure 5.1: Schematic of the devices. On the left is a FinFET with the source and drain indicated. The source and body are both tied to ground. The gate terminal is connected to one terminal of the ferroelectric capacitor; this node is labeled V_g and referred to as the "internal gate." The other terminal of the capacitor, called the "external gate," is labeled V_G.

3.1 shows the experimental setup of the devices to be measured. The outer terminal of the ferroelectric capacitor we refer to as the "external gate," and is labeled V_G. The terminal containing the wire, which connects the other end of the ferroelectric capacitor to the gate of

the FinFET is called the "internal gate" and denoted by V_g. There are numerous practical issues regarding the use of an internal metal gate in a practical, fully integrated NC-FET. (1) Charge-trapping on the metal layer may cause dynamic variation of the threshold voltage. (2) Fin pitch requirements impose a restriction on the total thickness of the gate stack. (3) Most importantly, the electrical boundary conditions are changed compared the case of a heterostructure. Specifically, the stabilizing positive capacitor can only "see" the average polarization, which would promote stripe domain formation in the ferroelectric instead of the molten domain states expected to be involved in negative capacitance [27].

The ferroelectric material used is 250 nm of $BiFeO_3$ (BFO). The fabrication of the capacitors follows the same general procedure as the fabrication of the PZT capacitors in 2 and 3. First, metallic (La,Sr)MnO_3 is sputtered on a (001) $LaAlO_3$ substrate at room temperature to form the bottom contact. Then 250 nm of BFO is grown using the pulse laser deposition technique. Photoresist is spun-on, exposed, and developed to form the contact patterns. Au is then deposited as the top contact layer with electron beam evaporation at 300 °C and removed from undesired areas via liftoff. The electrode area for the devices used is $A = \pi(25\mu m)^2$.

The FinFETs were made by collaborators at Sematech using a high-κ metal gate CMOS fabrication process similar to that of [51]. The gate length (L_g) of the FinFET is 100 nm. The fin dimensions are 35 nm width and 25 nm height. The number of fins per transistor is 200. The gate oxide is made of dielectric HfO_2 with an equivalent oxide thickness (EOT) of 1.3 nm. All measurements were taken in an Everbeing 30080 probe station. An Agilent B1500 semiconductor device analyzer was used to perform the IV measurements. Additionally, a Radiant P-PMF multiferroic tester was used to obtain the $P - E$ hysteresis loop measurements.

5.3 Experimental Results

Quasistatic measurements of the I_D-V_G characteristics of the devices are shown in 3.2 for both nMOS and pMOS baseline FinFETs and NC-FinFETs. The baseline FinFETs show close to ideal subthreshold slope (SS), with a minimum of 62 mV/decade at room temperature. While the NC-FinFETs have a hysteresis window close to 5 V, the subthreshold slopes are extremely low, from 8.5-40 mV/decade. It's worth noting that these are upper estimates on the subthreshold slopes, several orders of drain current are often traversed between two data points during switching. In total, at least 7-9 orders of magnitude of drain current are traversed over 100-300 mV of gate voltage during ferroelectric switching, summarized in 5.1. This massive reduction of SS and hysteretic behavior is consistent with the expected capacitance mismatch due to the size mismatch between the ferroelectric capacitor and the baseline FinFET [48].

An equivalent capacitive circuit for NCFET was proposed in [48], where the ferroelectric was modeled as a capacitor with the S-shaped charge-voltage (Q-V_{FE}) characteristics given by Landau-Devonshire theory. Since the ferroelectric capacitor is connected externally to

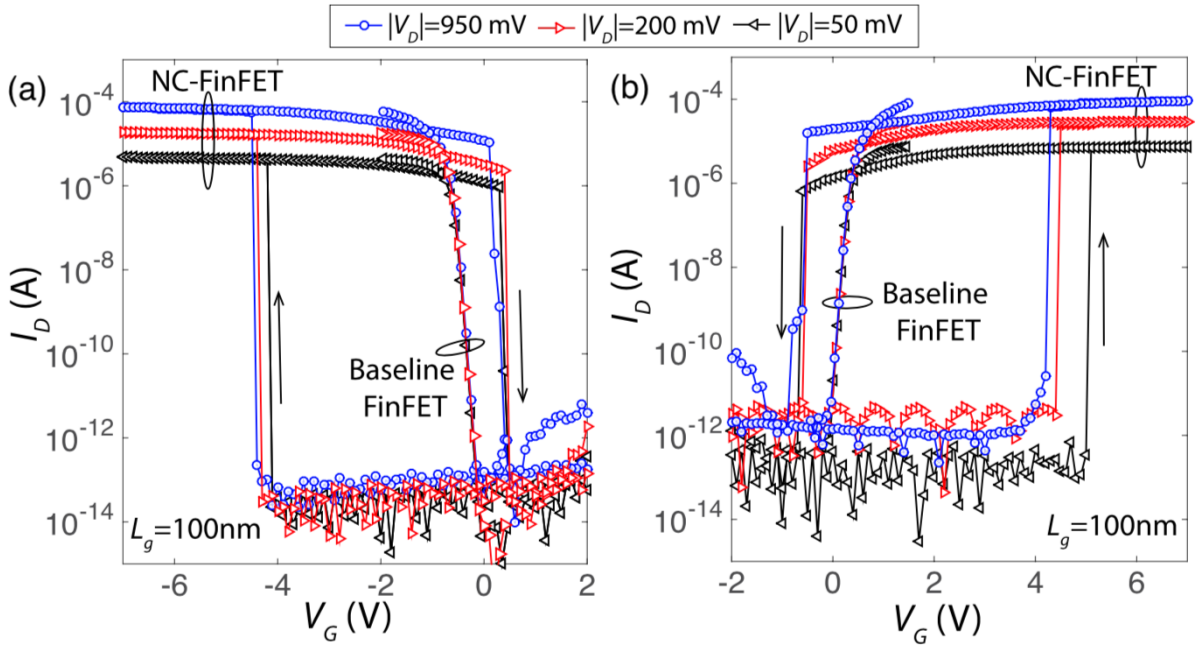

Figure 5.2: Transfer characteristics of the baseline FinFETs and the NC-FinFETs, showing pMOS devices in (a) and nMOS devices in (b). Characteristics are shown for three different values of drain voltage, $|V_D| = 50mV$, $200mV$, and $950mV$. The directions of the voltage sweeps for the NC-FinFETs are indicated with black arrows.

Device Type	V_D	Turn-on SS	Turn-off SS
p-type	-50 mV	12.4 mV/dec over 8 orders	25.5 mV/dec over 9 orders
	-200 mV	11.3 mV/dec over 9 orders	8.5 mV/dec over 8 orders
	-950 mV	11.7 mV/dec over 9 orders	40 mV/dec over 7.5 orders
n-type	-50 mV	13.6 mV/dec over 7 orders	16 mV/dec over 6 orders
	-200 mV	14.3 mV/dec over 7 orders	17.4 mV/dec over 6 orders
	-950 mV	18 mV/dec over 6.5 orders	50.2 mV/dec over 7 orders

Table 5.1: Summary of average subthreshold slopes for both pMOS and nMOS NC-FinFETs for different drain voltages.

the FinFET, our experimental setup allows us to compare the behavior of the ferroelectric when it is isolated and when it is in the circuit. To extract the ferroelectric Q-V_{FE} characteristics, we first consider the NC-FinFET equivalent circuit model, which is shown in 5.3. The baseline FinFET consists of oxide capacitance (C_{ox}), semiconductor capacitance (C_s), source capacitance (C_{source}) and drain capacitance (C_{drain}). $C_{source,ext}$ and $C_{drain,ext}$ are capacitances that occur due to fringing electric fields between the internal gate and source and drain, respectively. It has been shown that $C_{source,ext}$ and $C_{drain,ext}$ can be tuned to give better capacitance matching and thus higher performance in an NCFET [52]. On the basis of the experimental I_D-V_G curves and this NC-FinFET equivalent circuit model, we describe the following procedure to reconstruct the ferroelectric Q-V_{FE} relationship.

1. **Calculation of Q**. The capacitance of the baseline FinFET ($C_{baseline}$) was measured from the internal gate with the ferroelectric capacitor disconnected, and both source and drain connected to ground. 5.4 shows the measured C-V characteristics. Based on 5.3, $C_{baseline} = C_{source,ext} + C_{drain,ext} + (C_{ox}^{-1} + (C_s + C_{drain} + C_{source})^{-1})^{-1}$. Using the dimensions of the FinFET, $(C_{ox}^{-1} + (C_s + C_{drain} + C_{source})^{-1})^{-1}$ is calculated to be at most 55 fF. However, we can see from 5.4 that the measured $C_{baseline}$ has a weak dependence on V_g and is close to 1 pF, three orders of magnitude higher than the calculated device capacitance. This points to the fact that $C_{drain,ext}$ and $C_{source,ext}$ dominate the total baseline capacitance. The bias-dependent charge $Q(V_g, V_D) = C_{source,ext}V_g + C_{drain,ext}(V_g - V_D)$. From considerations described subsequently, we use $C_{source,ext} = 0.8\, C_{baseline}$ and $C_{drain,ext} = 0.2\, C_{baseline}$, which we clarify subsequently.

2. **Calculation of V_{FE}**. In order to calculate V_{FE}, we note that for a given I_D, V_g must be the same for the baseline device as the NC-FinFET, and use the relation $V_{FE} = V_G - V_g$. Thus, for a given applied V_G, the measured I_D also indicates the value of V_g and therefore implicitly of V_{FE}. We do not directly probe the internal gate during measurement of the NC-FinFET as this would introduce a large unwanted capacitance into the system.

Using these techniques, we are able to extract hysteresis loops for the ferroelectric during gate voltage sweeps for the NC-FinFET. The hysteresis loops for different values of drain voltages, $V_D = 50mV, 200mV, and 950mV$, are shown in 5.5. It is clearly visible that the ferroelectric capacitance is negative in certain regions of the hysteresis loop. These voltages are also where sub-60 mV/decade behavior is seen in the I_D-V_G characteristics, and confirms that the steep SS is due to negative capacitance of the ferroelectric.

The reason for the asymmetric choice of $C_{source,ext}$ and $C_{drain,ext}$ arises from the consideration that the ferroelectric Q-V_{FE} characteristics should not, to first order, depend on the drain voltage. Choosing $C_{drain,ext}$ to be 0.2 of $C_{baseline}$ most closely allows us to satisfy this condition. The choice to use $C_{source,ext}$ and $C_{drain,ext}$ as tuning parameters to achieve consistency of the ferroelectric Q-V_{FE} requires some justification, especially since one would expect $C_{source,ext}$ and $C_{drain,ext}$ to be equal based on the symmetry of the fabrication. As mentioned, it is clear from comparing the measurement in 5.4 to the maximum possible device capacitance that the external capacitances should dominate, so it is difficult to attribute this

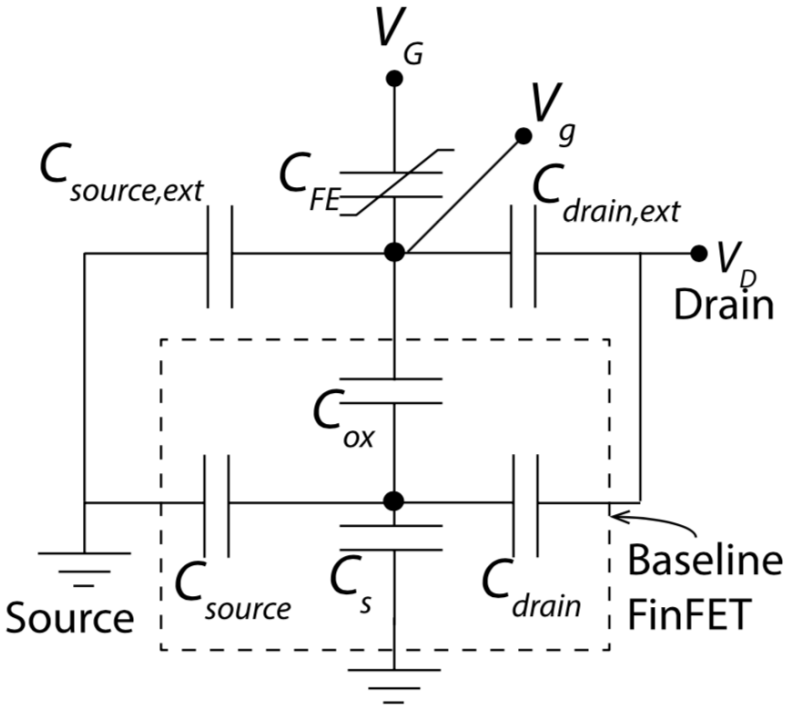

Figure 5.3: Equivalent capacitive circuit model of the NC-FinFET. The nonlinear element C_{FE} follows Landau-Devonshire theory.

drain dependence of the ferroelectric characteristics to a voltage-dependent drain-channel capacitance. There are multiple hypotheses that would explain this dependence, and it is impossible to rule any of them out with the available data. The only statement we can make conclusively is that the independence of ferroelectric characteristics from drain voltage imply a $C_{drain,ext} = 0.2C_{baseline}$.

Now we compare the behavior of the isolated ferroelectric with its behavior as part of the NC-FinFET. The hysteresis loop of the stand-alone capacitor is shown in 5.6, which was obtained with Radiant P-PMF Precision Multiferroic Tester. The hysteresis window is on the order of 6 V, while the hysteresis window of the NC-FinFET is 4.5-4.8 V. This reduction is consistent with expectations from basic capacitance matching considerations, where the positive capacitance is not enough to fully stabilize the negative capacitance, but reduces the depth of the energy wells. The remanent polarization of the stand-alone capacitor is 55 μC/cm^2, which is represents 1 nC of gate charge when scaled by capacitor area. However, the maximum charge which is switched during operation of the NC-FinFET is 2.3 pC, which is less than 0.25% of the nominal remanent polarization. This shows that the hysteresis behavior is determined by the points of instability where the positive FinFET capacitance is unable to stabilize the negative ferroelectric capacitance, and that charge balance conditions in the baseline device can significantly modify the effective ferroelectric characteristics.

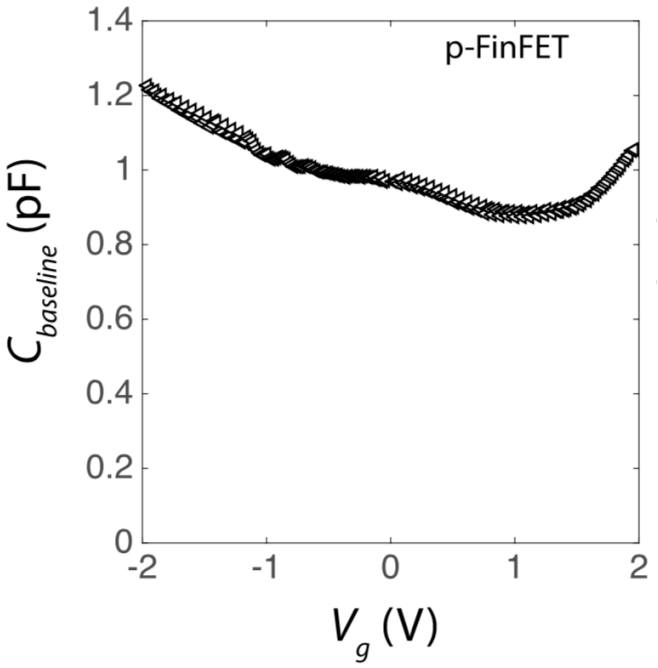

Figure 5.4: The capacitance of the baseline p-FinFET ($C_{baseline}$) measured with the ferroelectric capacitor disconnected, and the source and drain terminals shorted to body/ground. The weak dependence of $C_{baseline}$ on voltage as well its large value suggests that $C_{baseline}$ is dominated by $C_{source,ext}$ and $C_{drain,ext}$.

Simulation work based on the experimental data reported has been able to reproduce the I_D-V_G characteristics shown in 5.2. Measured baseline characteristics from a range of FinFETs of varying L_g are used to create a BSIM-CMG model, and a Landau-Devonshire model with coefficients up to fourth-order taken to match the extracted ferroelectric Q-V_{FE} characteristics in 5.5 are solved self-consistently to closely reproduce the NC-FinFET transfer characteristics [50]. This validates our methodology for analyzing negative capacitance FETs, which may be applied to other kinds of device structures.

5.4 Conclusions

To summarize, we have constructed an "artificial" NC-FinFET by connecting an epitaxial BFO capacitor to the gate of a short-channel (L_g = 100nm) FinFET. In this NC-FinFET configuration we observe extremely low subthreshold slopes, 8.5-40 mV/dec over 6-9 orders of magnitude of drain current at room temperature, well below the Boltzmann limit. This is a crude experiment in some sense - the size of the capacitors are mis-matched, the internal metal gate creates a somewhat different boundary condition than a heterostructure, and the

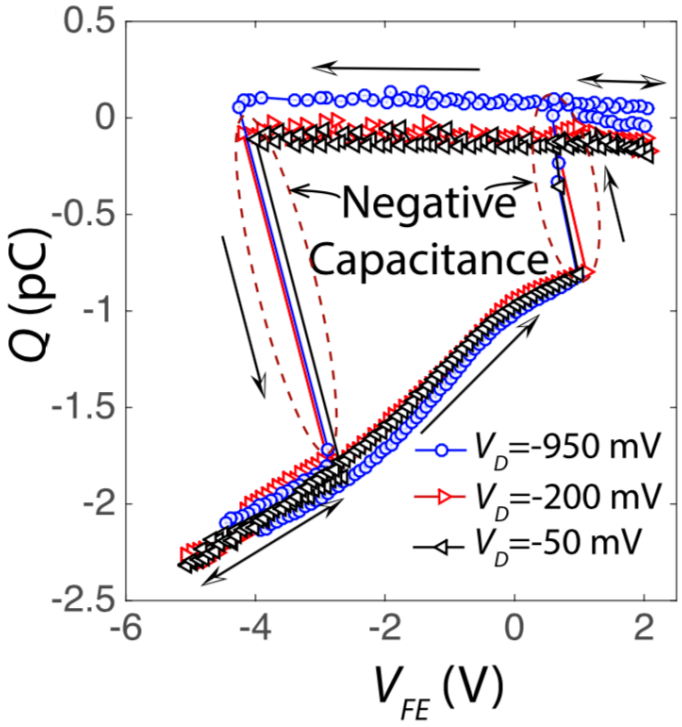

Figure 5.5: Extracted Q-V_{FE} characteristics for different values of drain voltage in the p-type NC-FinFET. Negative capacitance is apparent in both branches of the hysteresis loop.

material, BFO, is unlikely to be integrated into a foundry CMOS process line. However, the ability to independently probe the behavior of the baseline FET and the ferroelectric capacitor allows us to compare the behavior of the ferroelectric in the isolated state and in the NC-FinFET configuration, where we found that the effective remanent polarization was less than 0.25% of its value in the isolated configuration. We have thus provided an effective framework with which to analyze the behavior of negative capacitance devices. As it is unknown exactly how fabrication conditions and geometric factors will affect the negative capacitance behavior of ferroelectric films, practical device design will necessarily require a feedback loop between fabrication and simulation which will allow extraction and optimization of ferroelectric charge-voltage characteristics.

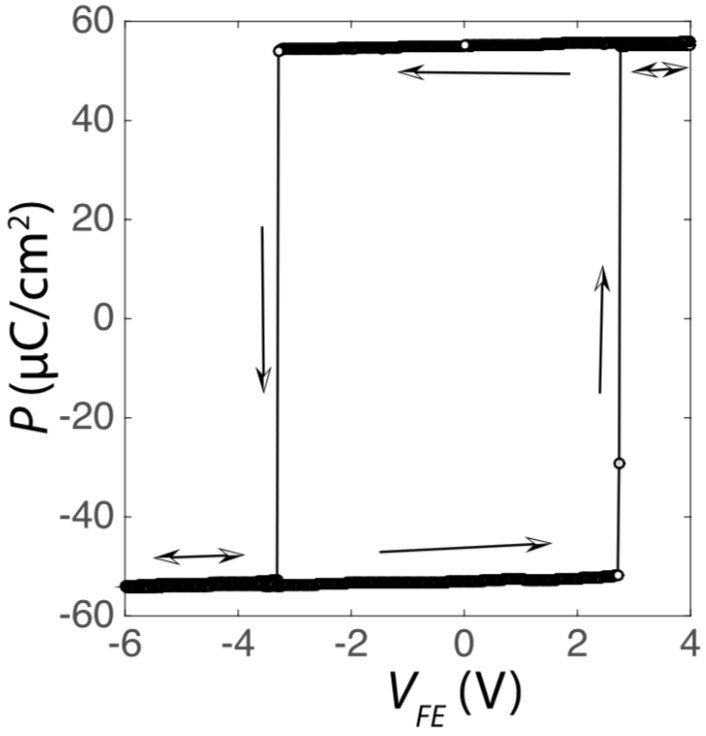

Figure 5.6: Q-V_{FE} characteristics for the BFO capacitor used in this experiment. The data are obtained with a multiferroic tester for the isolated capacitor using a quasistatic voltage sweep.

Chapter 6

Fabrication of Negative Capacitance FETs

6.1 Introduction

Thus far, all experiments described have involved the use of ferroelectric films fabricated into capacitor structures, coupled to other devices at a circuit level. The focus now shifts towards practical realization of negative capacitance FETs (NCFETs), using material systems and device structures of relevance to industrial scale foundries. It was previously noted that a practical realization of NCFETs will require investigation into how the depolarization fields of the semiconductor and interfacial dielectric renormalize the energy landscape of the ferroelectric. Attempts to calculate the distribution of the internal fields and the local susceptibilities from first principles have been successful at describing the qualitative field and temperature dependence of negative capacitance systems, but have been limited to extremely simple geometries and do not achieve quantitative accuracy [27]. Similar attempts using phase-field models do not give quantitatively accurate predictions [53] [40]. Our goal is to exploit the charge-sensing properties of fabricated transistors and, by comparison with large numbers of control devices, extract ferroelectric characteristics and project them onto simple ferroelectric models. These models are then used to re-optimize the NCFET gate stacks, and the design loop continues to its next iteration.

This strategy requires a well-controlled and well-understood baseline transistor process, as well as the ability to modify the gate layer deposition and ferroelectric properties. Except for ion implantation and atomic layer deposition, all fabrication work described in this section was carried out in the Marvell Nanofabrication Laboratory at the University of California, Berkeley. Ion implantation was performed by Innovion Corporation in San Jose, California. Atomic layer deposition was performed in a separate dedicated tool. The task of fabrication can roughly be divided into two major challenges: 1. The development of a transistor process, primarily consisting of oxidation, deposition, etching, and lithography [54]. 2. The development of the ferroelectric deposition process and characterization of its

electrical and material properties. The ferroelectric material system used is the rich family of doped hafnium oxides. The discovery of a ferroelectric phase in hafnium oxide is relatively recent [30], and its ferroelectric properties are somewhat different than the much more thoroughly studied perovskite oxides, such as PZT. Importantly, hafnium oxide is integrated into industrial CMOS processes as a high-κ dielectric [32], so integration of ferroelectric hafnium oxide requires only an adjustment of the thermal budget, not necessarily the introduction of new chemical compounds which could potentially contaminate the process.

The fabrication of transistors in a university cleanroom poses unique constraints on the process requirements. First, simplicity is valued. High throughput is not possible, and each iteration of the fabrication cycle takes considerable time, depending on the availability of tools. Thus, it is crucial to reduce the number of mask steps while still maintaining reasonable device performance. To this end, we employ the use of silicon-on-insulator (SOI) substrates, so that device isolation is automatic. Second, although it is important to explore the behavior of short-channel devices and the impact of short-channel effects on capacitance matching, high density is not required, nor is a large number of devices. This allows use of electron beam (e-beam) lithography, which allows for channel lengths comparable to production level devices without the complexity of state-of-the-art photolithography. Yield is also not a major concern. Finally, because the main advantage of NCFETs for high performance digital logic is in the subthreshold regime, the importance of a high on-current (I_{ON}) in the baseline process is secondary. This allows for some flexibility in terms of dopant activation and metal contact formation. Exploiting this trade-off is discussed in further detail subsequently.

6.2 Ferroelectricity in Hafnium Oxide

In 2011, T. S. Böscke et al. reported on the existence of a polar, ferroelectric orthorhombic phase in thin films of polycrystalline hafnium oxide [30]. Hafnium oxide was normally known to exist in three crystalline phases at standard pressure: (1) monoclinic at room temperature, (2) tetragonal above 2050 K, and (3) cubic above 2803 K [55]. Preliminary experimentation with doping of hafnium oxide was motivated by two reasons: (1) a desire to increase the crystallization temperature, as amorphous films have numerous advantages over polycrystalline films for use as gate dielectrics in conventional FETs. It was found that silicon doping could increase the crystallization temperature by several hundred K [32]. (2) It was found that doping could increase the tetragonal phase fraction and result in a higher dielectric constant [56]. The additional presence of a TiN capping layer provides for the stabilization of the ferroelectric orthorhombic phase for an Si content in the 2-5 mol% range. Antiferroelectric behavior is seen for higher concentrations, until normal dielectric behavior is eventually reached above ~10%. 6.1 depicts the rotational ionic distortion that accompanies the ferroelectric switching. The atoms rotate through the centrosymmetric phase which represents the top of the potential barrier between the two stable orientations of the net dipole moment along the c-axis.

It was soon discovered that a wide range of dopants - Si, Y, Gd, Al, Zr, Sr, Sc, La, Nb, N,

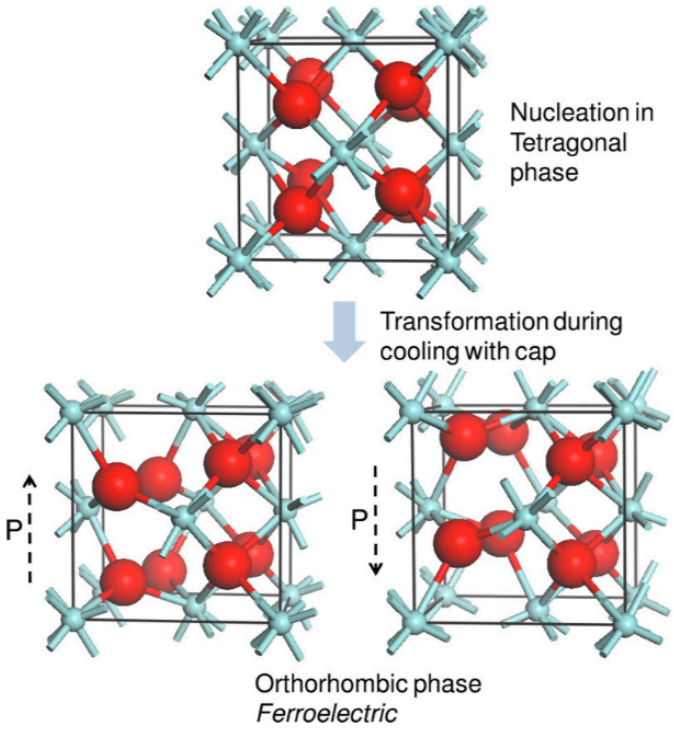

Figure 6.1: Schematic showing the positions of atoms in the unit cell of HfO_2. The orthorhombic phase is the result of a symmetry-breaking distortion of the tetragonal phase. Rotation of lattice atoms modulates the net electric dipole moment. The large red atoms are oxygen; the small blue atoms are hafnium. Figure adapted from [30]

and Ge among possible others - could stabilize the orthorhombic phase of hafnium oxide [57]. ZrO_2 can obtain an antiferroelectric phase, and the full range of compositions $Hf_xZr_{1-x}O_2$ (HZO) shows a continuous transition from dielectric to ferroelectric to antiferroelectric, with remanent polarization peaking at $Hf_{0.5}Zr_{0.5}O_2$ [46]. Such a wide array of electrical behavior in a class of materials already incorporated into semiconductor foundry processes has re-ignited interest in ferroelectric-based nonvolatile memories.

Ab-initio methods indicate that the remanent polarization of the orthorhombic state could, at the level of the unit cell, be as high as 51 $\mu C/cm^2$ [58], more than twice the maximum of what has been observed experimentally [59]. Investigation has been carried out regarding the microscopic composition of ferroelectric hafnium oxide by varying the composition and annealing conditions and analyzing the strength of the grazing-incidence X-ray diffraction signal corresponding to the monoclinic phase. It is found that, while this signature is decreased as ferroelectric properties become stronger, it is always present, indicating polymorphism [60]. Integration of a polycrystalline gate dielectric presents a potential challenge to the adoption of negative capacitance in an industrial process. Coarse length-scale

statistical variation of ferroelectric/dielectric properties is undesirable for aggressively scaled technologies. Another concern is leakage along grain boundaries [32]. Fortunately, for the case of negative capacitance there is no downside to using an interfacial layer of SiO_2 [48]. This interfacial layer would allow defect state densities to remain low. Because the EOT of the negative capacitance layer is negative, it is possible to maintain extremely small EOTs even for large physical thicknesses.

Our ferroelectric films are grown in a Fiji Ultratech/Cambridge Nanotech Atomic Layer Deposition system. We have primarily used $Hf_xZr_{1-x}O_2$ because of the high degree of tunability of the ferroelectric properties within the same material system. The precursors used are tetrakis(ethylmethylamino)hafnium and tetrakis(ethylmethylamino)zirconium, and they are held at a temperature of 75 °C. Water vapor is used for oxidation. The rate of growth of HZO is approximately 0.1 nm/cycle at a process temperature of 250 °C. The capping layer (TiN or W) is formed by sputtering. Phase formation anneal is carried out in nitrogen ambient at temperatures from 500-700 °C for 30 sec. It is found that when the Zr:Hf ratio is above one, the films exhibit antiferroelectric behavior, while ferroelectric behavior is observed at lower Zr concentrations. Electrical behavior is probed by forming capacitors using techniques similar to those discussed in 2.4. A representative P-E hysteresis loop for a ferroelectric sample is shown in 6.2 for two different annealing temperatures. In addition to composition, annealing conditions provide a significant knob with which to tune material parameters and electrical behavior.

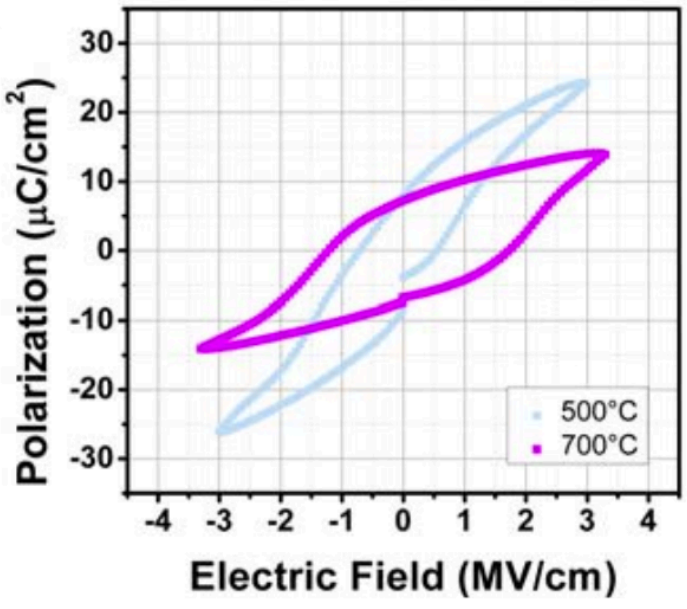

Figure 6.2: Polarization-electric field (P-E) hysteresis loops for a 10 nm film of $Hf_{0.5}Zr_{0.5}O_2$ capped with TiN. Figure adapted from [46].

HZO has also been noted for characteristics that do not scale perfectly with thickness, for example coercive field is seen to increase in thinner films [59]. This highlights the important of surface energy effects and strain imparted from the surrounding materials to stabilize the orthorhombic phase. It has also been reported that a newly-discovered rhombohedral phase in HfO_2 also shows ferroelectric behavior [61]. Our films are confirmed to be orthorhombic, however, as indicated by the grazing-incidence X-ray diffraction (GI-XRD) measurement shown in 6.3. Slight shifts of the diffraction peaks are observed for the thinner 5.5 nm film compared to the 10 nm film, again showing the dependence of the microstructure on surface effects.

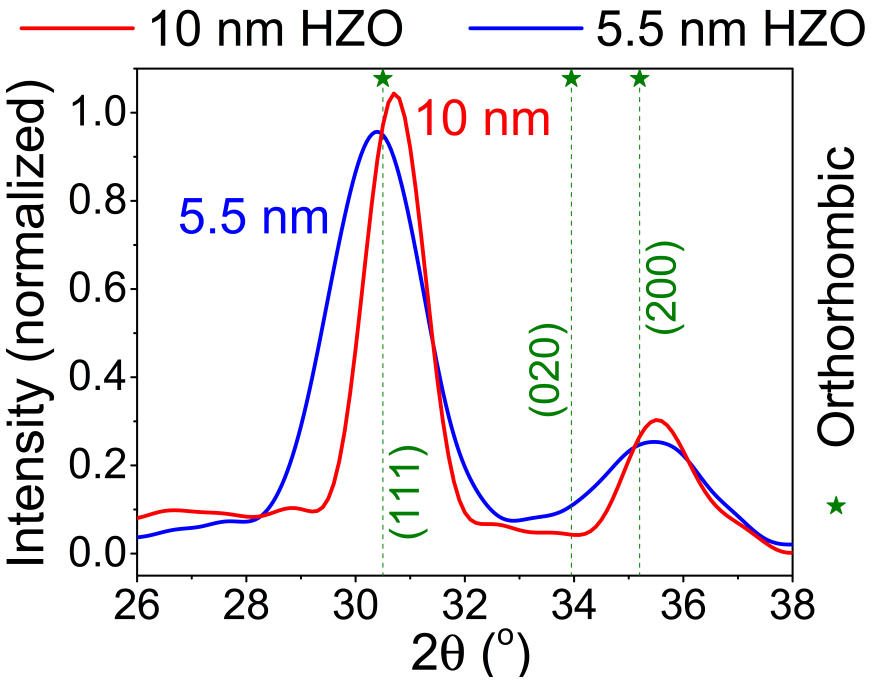

Figure 6.3: GI-XRD measurements for $Hf_{0.8}Zr_{0.2}O_2$ films of two different thicknesses. The stars indicate theoretically predicted peak positions. A slight dependence on film thickness is noted. Taken from [62].

6.3 Replacement Gate Process for Silicon-on-Insulator FETs

Now we discuss the process steps for the fabrication of replacement gate transistors [63] [64] on a silicon-on-insulator (SOI) substrate. Using a replacement gate process allows for dopant activation prior to deposition of the real gate layer. Because phase formation temperatures of HZO are well below the activation temperatures of As in Si [54] [46], this significant com-

plication of the fabrication process is necessary for good source/drain resistance properties. As discussed previously, this method is later abandoned in favor of reducing the number of steps required for a device fabrication cycle.

Silicon-on-insulator wafers are obtained from Soitec, Inc. and are the starting point of the process. SOI devices offer a number of advantages compared to bulk Si, including improved electrostatic control of the gate over the channel, lower parasitic substrate capacitance, lower power consumption for matched performance, excellent device isolation, and dynamic threshold voltage control through back-gate biasing [10] [65]. The well-known "smart cut" technique is used to create the SOI wafers [66]. An initial silicon wafer called the handle is oxidized to form the buried oxide (BOX), after which it is implanted with hydrogen atoms a fixed distance into the Si substrate. The oxidized surface of the handle is then bonded to a second silicon wafer, which essentially acts as a mechanical support. The handle is broken at the implanted layer by formation of gaseous microbubbles that create stress and promote fracture, so that only the device layer is left behind. The device layer is then polished by chemical-mechanical polishing (CMP).

A summary of the process flow starting from the 6-inch lightly p-type doped SOI wafer is shown in 6.4. Before deposition of the sacrificial gate stack, the device layer must be thinned to achieve the desired body thickness. Thinning is performed via dry thermal oxidation followed by silicon oxide etching in hydrofluoric acid (HF). Dry oxidation is performed in a Tystar furnace heated to 1050 °C. The Deal-Grove model (6.1), which predicts the time t needed to grow an oxide layer of thickness X_0, is used for an initial test growth [67]. X_0 is targeted according to the Si/SiO_2 consumption/formation ratio of 0.46 [54]. Inspection of oxide layer thickness is performed with ellipsometry and used to calibrate the oxidation process.

$$t = \frac{X_0^2}{A} + \frac{X_0}{B/A} - \tau \tag{6.1}$$

Here A and B/A are rate constants that depend on temperature according to the Arrhenius equation, and τ accounts for any initial oxide layer. After thinning of the device layer to ∼40 nm from an initial 100 nm, the sacrificial gate layers, consisting of 12 nm SiO_2 and 150 nm polycrystalline silicon (poly-Si), are deposited with dry thermal oxidation and low-pressure chemical vapor deposition, respectively. Unlike the device layer, the thicknesses of these layers are not critical to the device performance, although they may have second order effects via the fringing field capacitances.

Photolithography is performed on an ASML 5500/300 deep ultraviolet (DUV) stepper with 4X reduction and a minimum feature size of 250 nm. The gate definition is done using a thin 450 nm layer of DUV 210 photoresist, while all other photolithography steps are carried out with 900 nm of photoresist thickness. A 30 second pre-exposure bake is carried out, as is a 30 second post-exposure bake, both at 130 °C. After photoresist development, a hard-bake is performed under ultraviolet light at 70 °C for 30 sec. Reactive ion etching is performed to etch the poly-Si, sacrificial SiO_2, and SOI device layers for both active and gate patterning. Mass spectrometers in the reactive ion etching chambers allow for endpoint detection.

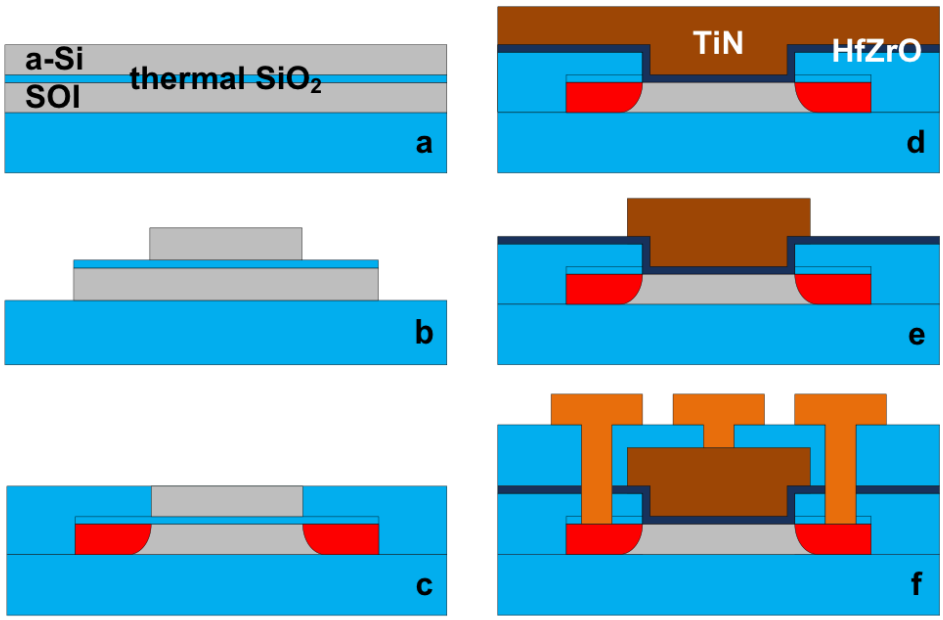

Figure 6.4: Summary of the replacement gate transistor process flow. (a) Sacrificial gate layers are grown/deposited on the SOI wafer. (b) The active area is defined and the wafer is etched down to the BOX, followed by gate definition and etching of the sacrificial polycrystalline silicon (poly-Si) layer. (c) After As ion implantation into the source/drain regions, silicon dioxide is deposited at low temperature. The wafer is polished to expose the sacrificial poly-Si. (d) The sacrificial gate layers, a-Si and SiO_2, are removed, and the real gate stack consisting of HZO and TiN is deposited. (e) The real gate is patterned and etched back. (f) Inter-layer dielectric is deposited, and contact holes are etched. After metal sputtering the contacts themselves are formed. Figure taken from [62].

Next, As ion implantation for the source and drain regions is performed. The implant dose is 1×10^{15} cm^{-2} and the implant energy is 8 keV. Rapid thermal annealing for dopant activation is performed at 950 °C. Following this, silicon dioxide is deposited with low-pressure CVD to cover the sacrificial gate stacks. The wafer then undergoes CMP to expose the sacrificial poly-Si layer, which is removed with reactive ion etching. The 12 nm thermal SiO_2 is removed with a quick 30 sec HF dip.

Rapid thermal oxidation is then performed at 1000 °C to produce roughly 2 nm of SiO_2 as an interfacial gate dielectric. The thickness of the SiO_2 is due to ramp rate limitations of the rapid thermal processing chamber. 5.5 nm of $Hf_{0.8}Zr_{0.2}O_2$ is then deposited by atomic layer deposition. The deposition cycle consists of 4 pulses of Hf precursor followed by 1 pulse of Zr precursor, which is repeated 11 times. The composition is chosen to give a remanent polarization somewhat lower than the maximum; predictions of a basic Landau-Devonshire model would suggest that too high a remanent polarization will result in too low of an

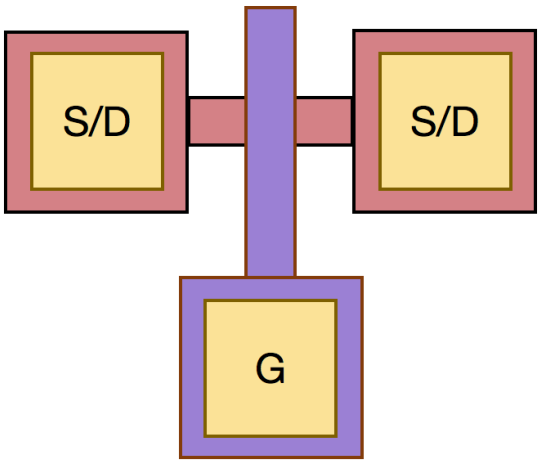

Figure 6.5: Overhead view of the basic device structure. The source/drain contacts are marked "S/D" and the gate contact is marked with a "G."

absolute value of negative capacitance [48]. 40 nm of TiN is sputtered, and the ferroelectric phase formation anneal is performed for 30 sec at 500 °C in nitrogen ambient. After the final gate patterning and TiN etch, 400 nm of interlayer dielectric (ILD) SiO_2 is deposited with plasma-enhanced CVD at 200 °C. Contact hole patterning followed by an HF etch exposes the gate, source, and drain contact areas. At this point, a 500 nm layer of TiN/Ti/Al is deposited via sputtering, which is then patterned and etched to form the contact pads. A 350 °C anneal for 15 mins is found to improve the parasitic source/drain series resistance. A false-colorized SEM micrograph of a completed device is shown in 6.6.

6.4 Gate-First Process for Silicon-on-Insulator FETs

Here, we briefly outline a self-aligned gate-first process using mixed-mode photolithography and electron beam (e-beam) lithography to define gate lengths down to 30 nm. The increased simplicity of the process allows for the fabrication of larger splits of gate insulator thicknesses and compositions. Taking on the complexity cost of incorporating e-beam lithography was necessary in order to investigate short-channel effects on capacitance matching in NCFETs. It is shown subsequently in 7 that the relative advantage of NCFETs over conventional FETs is boosted at shorter channel lengths.

As before, the device layer is thinned, only this time to 15 nm instead of 40 nm. The active layer is patterned and the exposed regions are etched down to the BOX. The gate stack is then deposited identically as before, with the following modificationls: (1) The interfacial dielectric is slightly nitrided to improve interface state density [68]. It is tuned to either 2 or 3 nm by varying the oxidation time. (2) Only 10 deposition cycles of ALD are performed

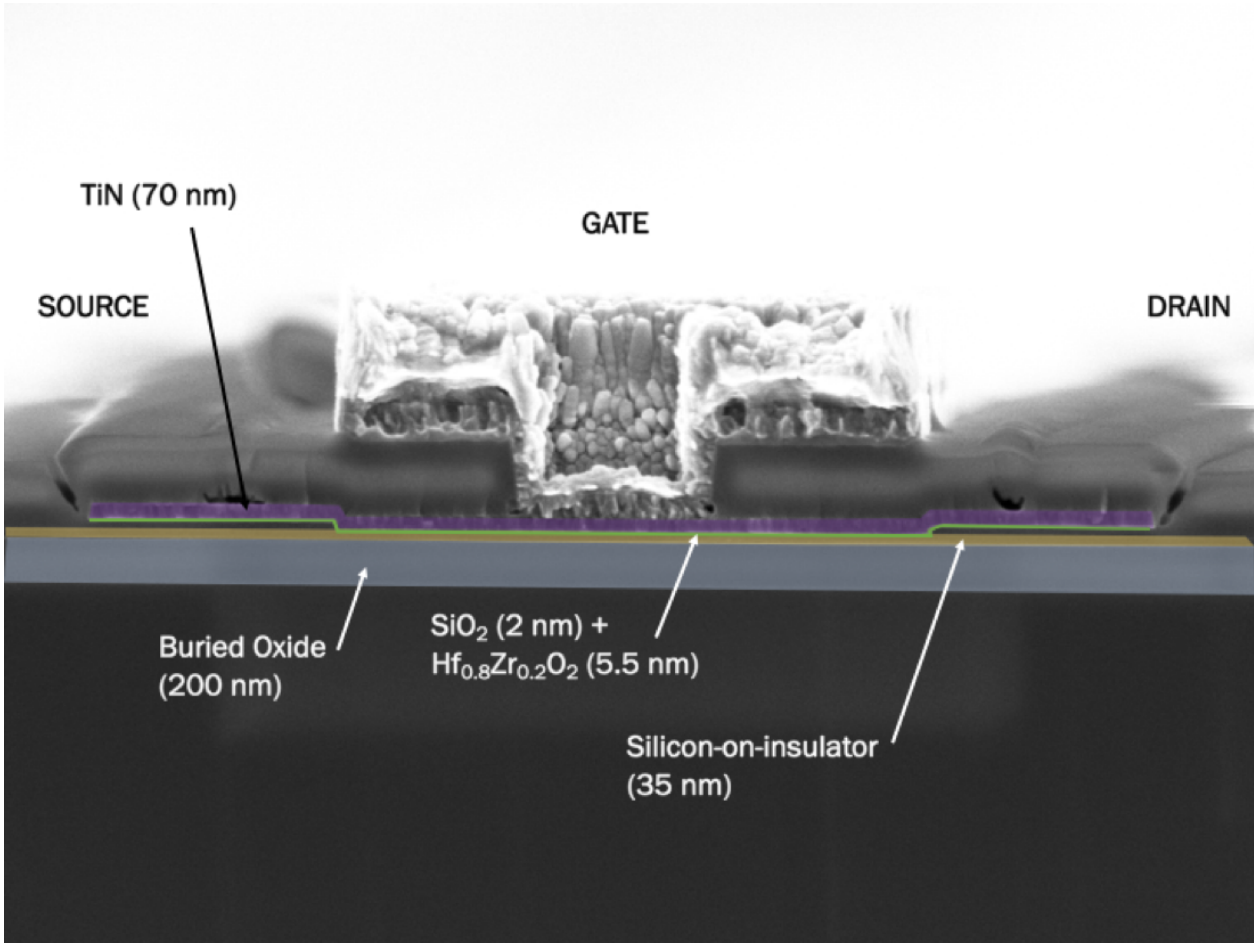

Figure 6.6: SEM micrograph of the completed FET, with various material regions indicated by color.

instead of 11 to yield 5 nm of $Hf_{0.8}Zr_{0.2}O_2$. (3) Tungsten is used in place of TiN. Tungsten has been shown to give more robust ferroelectric properties over TiN when used as a capping layer [69]. The phase formation anneal is carried out again at 500 °C. E-beam lithography and photolithography are carried out successively to define short-channel and long-channel FETs, respectively. After ion implantation, ILD deposition, and contact metallization are performed identically with the replacement gate process.

A major disadvantage of this process is a large series resistance, which makes investigation of NCFETs for analog applications difficult [13]. Much of this problem could be alleviated with two modifications: (1) The described layout has an unnecessarily large source/drain extension region, on the order of 10s of microns. (2) Migration to a Si:HfO_2 gate insulator, which has a much higher phase formation annealing temperature, typically in the range of 950 °C, a suitable temperature for dopant activation [59]. Further future modifications to the layout include the fabrication of RF transistors with waveguide structures leading to

the terminals and of content-addressable memory cells to explore applications of the normal hysteretic behavior of ferroelectrics to neuromorphic computing hardware [70].

Chapter 7

Characterization of Negative Capacitance FETs

7.1 Introduction

There are two main challenges presented by the characterization of our negative capacitance FETs. First, is the challenge of developing a fresh FET fabrication process, and using measurement data to diagnose the issues in that process. Second, we must deduce what the charge-voltage characteristics are of the ferroelectric when it is incorporated into the gate stack of the FET in a heterostructure. The requirement that the displacement field be continuous tends to depolarize the ferroelectric and alter its charge-voltage characteristics [15] [27]. The ability to infer ferroelectric charge-voltage characteristics from FET behavior thus depends on having a high degree of control over the baseline process, as in 5.

One potential major use of NCFETs is in analog circuits, where their superior output characteristics could offer an advantage over conventional FETs at a given technology node [71]. The output resistance can even be made negative [72]. Here the relevant quantities are the small-signal transconductances and output resistances at different bias points. While high frequency characterization is of key relevance, we describe briefly attempts to take similar measurements with a simpler setup at lower frequencies, to ease the future debugging process.

When characterizing the baseline devices, particular attention is paid to hysteresis arising from trapping/de-trapping of electrons. As hysteresis in the I_D-V_G characteristics is a signature of ferroelectric memory, it is important to be able to separate the effects of charge-trapping and ferroelectric polarization response. Fortunately, critical timescales for charge defects and ferroelectricity are quite different. The traps in our FETs are mostly unable to respond even at the kHz range of frequency, whereas ferroelectric behavior is completely unchanged. We also describe techniques to take measurements that discard the effects of traps.

Finally, when capacitance matching fails in an NCFET, the result is memory opera-

tion [48]. This occurs because the ferroelectric negative capacitance cannot be stabilized by the baseline FET capacitance and the hysteresis that characterizes isolated ferroelectrics dominates the behavior. However, information about the reliability of the ferroelectric material can still be obtained from such devices. We describe this process as well. Together, these techniques form an arsenal of tools with which to probe the underlying physics in our fabricated FETs.

7.2 Quasistatic Measurements

This section describes the measurements taken on the fabricated FETs that are ubiquitous to FET characterization. Terminal voltages are changed slowly, and currents are measured after transients have settled. The primary measurements made of this type are the I_D-V_G (transfer characteristics), I_D-V_D (output charateristics), and capacitance-voltage (C-V). The last measurement is not truly quasistatic, as a small AC voltage is applied on top of the quasistatically modulated bias. Especially in the measurement of transfer characteristics, it is critical to measure all terminal currents, including gate current. Since the key signature of negative capacitance in FETs is sub-60 mV/dec subthreshold slope, any quantities that could contaminate the drain current measurement must be controlled. Much of the work in this section is also in [71].

Experimental Setup

The tool used for all measurements in this section is a Keysight B1500 Semiconductor Device Analyzer. This is identical to the Agilent B1500 mentioned in 2. This tool incorporates a set of modularized measurement elements, which can be customized and upgraded, into a single scriptable interface. The most important of these are the source measurement units (SMUs), which are the input/output terminals. The tool controls the voltage on these terminals and simultaneously measures the current through them. The SMUs have a current noise floor in the 10-100 fA range, and can control voltage in increments of $\sim$10 mV. Although such a complex tool provides a wide range of capabilities, one major downside is the opaqueness of the measurement circuitry. 7.1 shows a typical I-V measurement of a ferroelectric-gated FET fabricated on a silicon-on-insulator substrate.

While the Everbeing 30080 probe station was adequate for the ferroelectric capacitor measurements described in 2 and 3, the sensitivity of the probe tips to external vibrations and light warranted use of a higher-end probe station for the more sensitive transistor measurements. Thus all FET measurements reported are performed on a Cascade Microtech Summit 200 probe station. Another advantage of this setup is a built-in temperature controller, which allowed us to precisely fix the temperature at 300 K, instead of being subject to weather fluctuations.

For low-temperature measurements, additional infrastructure is required, namely a vacuum probe station with a liquid nitrogen line. We used a LakeShore TTPX probe station,

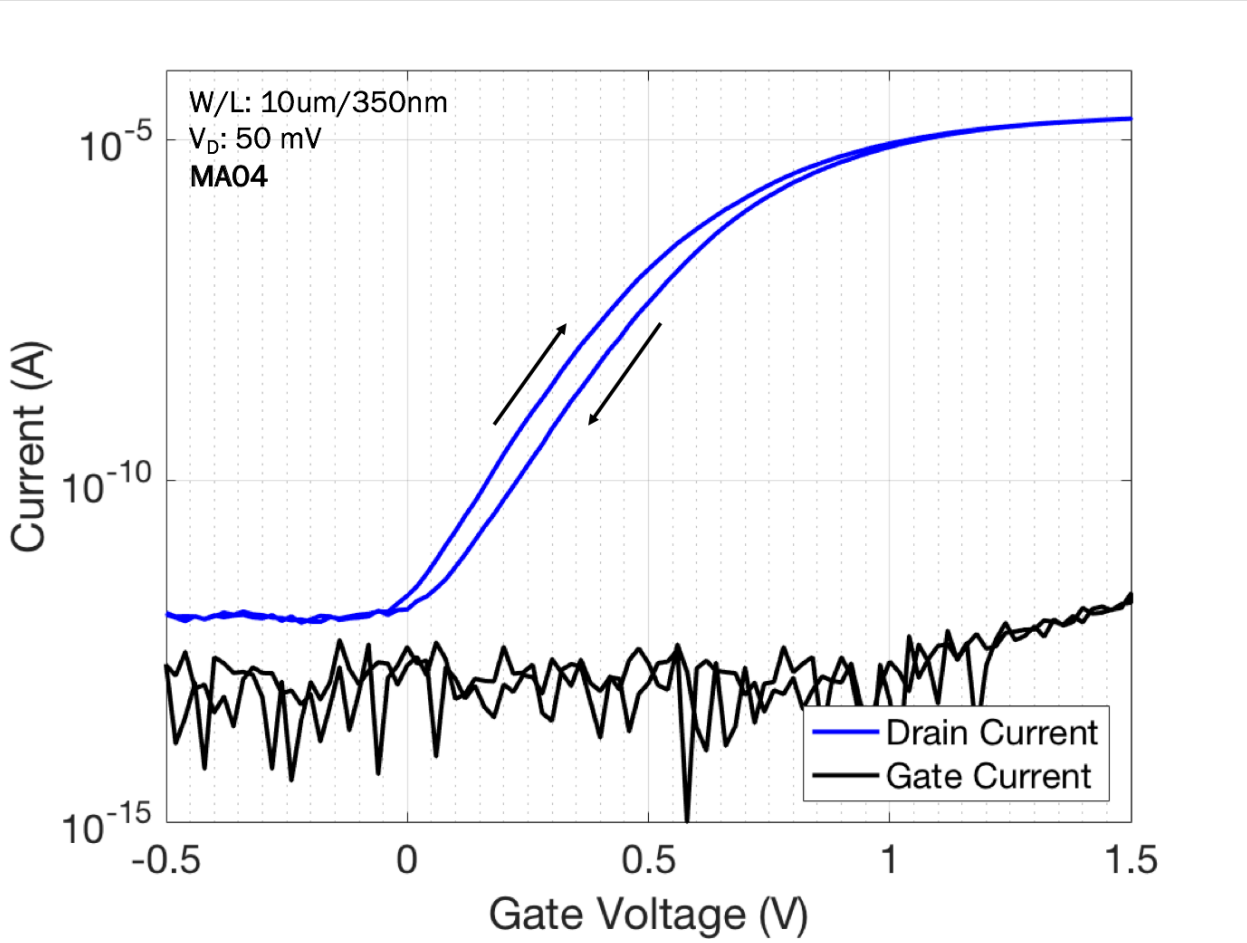

Figure 7.1: Transfer characteristics of a ferroelectric-gated FET without a post-metallization anneal. The threshold voltage shift in the reverse sweep compared to the forward sweep is due to channel-side charge injection. Gate current is shown to be significantly below drain current, even in the off-state, indicating potential leakage through the buried oxide (BOX).

which is mentioned in 3. We note that this probe station has a higher parasitic capacitance than both the Cascade and the Everbeing, and is therefore not ideal for fast transient measurements. 7.2 shows a photograph of the sample chamber of the LakeShore probe station for reference.

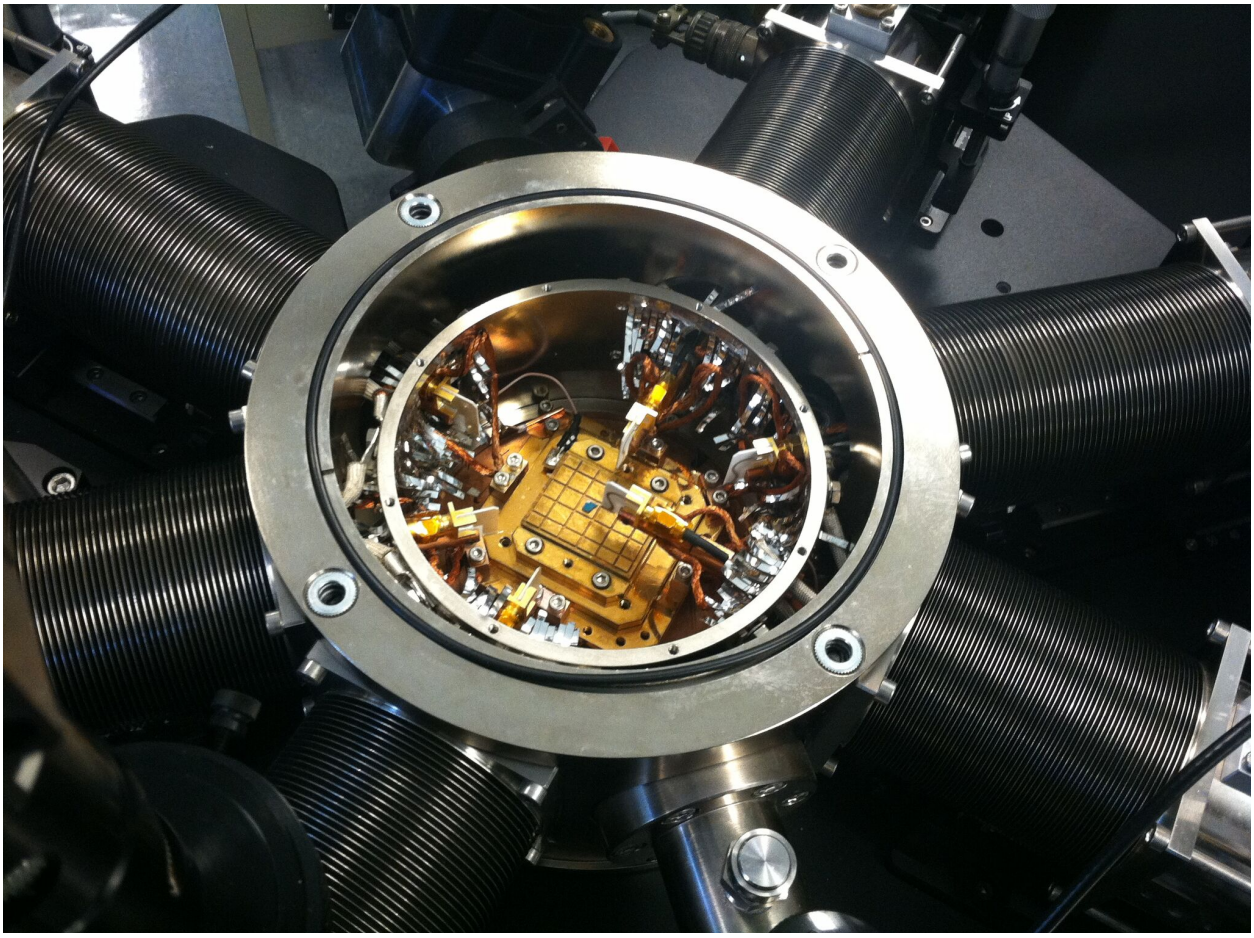

Figure 7.2: Photograph of the sample chamber in the LakeShore TTPX probe station.

Results

We now provide an overview of quasistatic characterization for the gate-first NCFETs whose fabrication is discussed in 6.4. These NCFETs are made with 5 nm of $Hf_{0.8}Zr_{0.2}O_2$ and 3 nm SiO_2 in the gate stack, and the gate patterning is done with mixed-mode photolithography and e-beam lithography. An identical process is carried out to fabricate reference transistors, which have 5 nm dielectric H_2 and 2 nm SiO_2 in the gate stack. The difference in interfacial oxide thickness will be important for identifying negative capacitance. First, we analyze the behavior of the long-channel devices. 7.3 shows on the left C-V measurements at 1 kHz and

1 MHz for both the NCFET and the reference device. Here, the source, drain, and body are all shorted to ground. We attribute the rightward shift of the C-V to poor contact resistance.

The NCFET, which has a thicker interfacial layer, shows smaller inversion capacitance as expected. However, in the middle region (between $V_G = 0.5$ V and $V_G = 0.8$ V), the slope of the C-V is steeper for the NCFET, resulting in a larger capacitance in the middle region. This enhancement in the intermediate region and the smaller capacitance in the inversion region establishes the negative capacitance effect. Resulting from this, a steeper subthreshold slope is seen systematically in the NCFET. The thicker interfacial layer is chosen so that the ability of the negative capacitance to compensate short-channel degradation can be detected. Additionally, it is expected that the relative improvement of the NCFET over the reference FET will be greater in the short-channel regime. Parasitic capacitances lowering the C_{max} to C_{min} ratio of the baseline device should, in principle, allow for easier matching of the negative ferroelectric capacitance to the baseline [73] [74] [75].

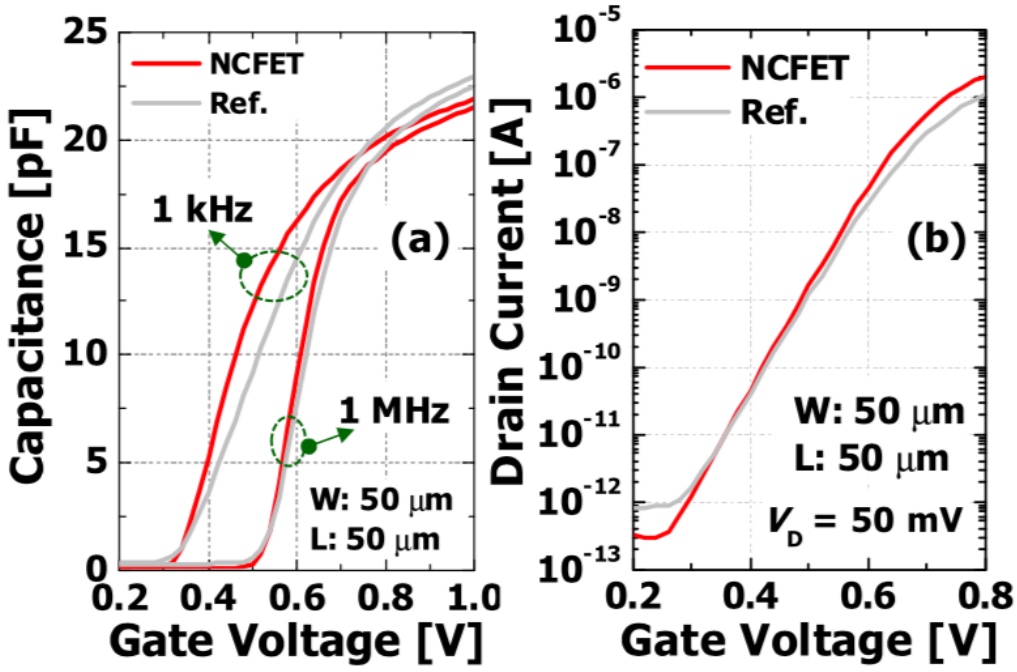

Figure 7.3: (a) Capacitance versus gate voltage for large-area transistors (W/L: 50 μm/50 μm). Data are taken at both 1 kHz and 1 MHz. (b) I_D-V_G data for the same devices. Reduced subthreshold slope over many orders of magnitude of drain current as well as higher on-current is observed. Figure adapted from [71].

The interface state density D_{it} is measured using the AC conductance method [68] [76], and it is found that D_{it} is in the 10^{12} cm^{-2} eV^{-1} range for both the reference FETs and

NCFETs, so that the subthreshold slope reduction cannot be attributed to a difference in interface state capacitance, C_{it}. C_{it} is thought to be the main mechanism degrading subthreshold slope even beyond the Boltzmann limit in our reference devices. Devices with lower D_{it} are found to also have lower subthreshold slopes.

It is important to note that the hysteresis seen in the transfer characteristics is strongly dependent on the range over which the gate voltage is swept. For hysteresis arising from charge-trapping, the hysteresis window is a monotonically increasing function of gate voltage sweep range [10]. For ferroelectric switching, there is a sudden onset of a counter-clockwise hysteresis at the coercive voltage from polarization reversal. The onset of ferroelectric hysteresis in transfer characteristics is discussed in more detail in 7.5. This dependence is apparent in 7.4, where in the reference FET, a large clockwise hysteresis is observed with the gate voltage is swept to 4 V. However, in the NCFET, ferroelectric switching results in a counter-clockwise hysteresis. Pulse-gated IV measurements are carried out precisely to capture the effect of the ferroelectric only.

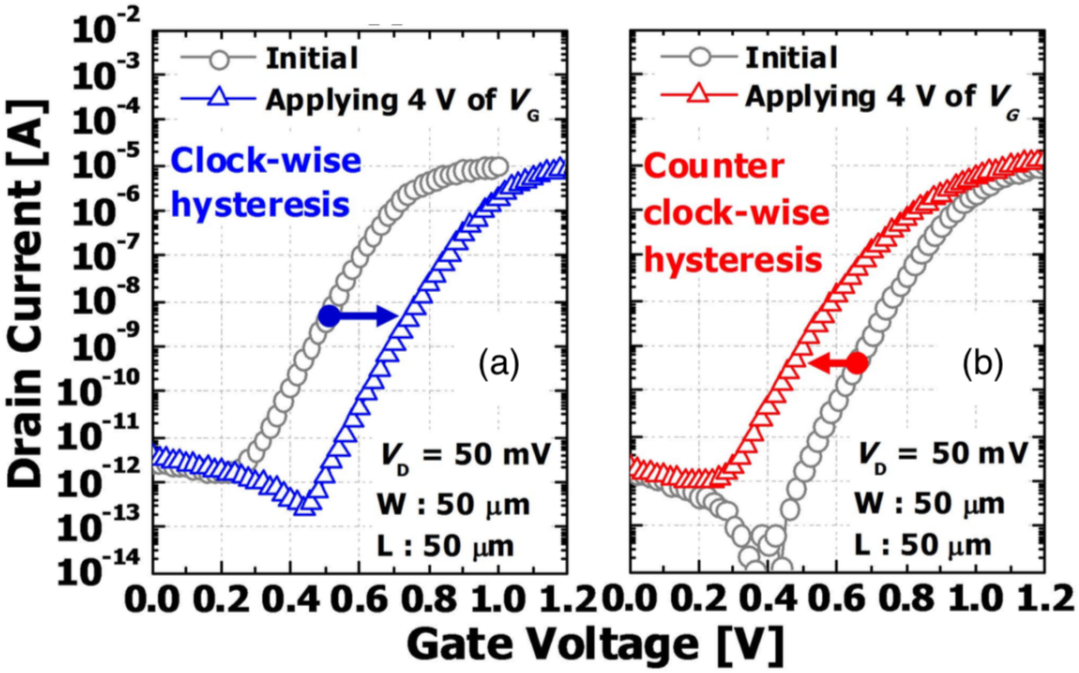

Figure 7.4: (a) Transfer characteristics for a reference FET when the gate voltage is swept over a large range, showing charge-trapping induced hysteresis. (b) Transfer characteristics for an NCFET when the gate voltage is swept over a large range. Counter-clockwise hysteresis from ferroelectric polarization switching is apparent. Figure adapted from [71].

As expected, the subthreshold slope for NCFETs is improved because an increasing drain coupling capacitance flattens the overall baseline C_G, leading to better capacitance match-

ing. The minimum subthreshold slope is attained at $L_g = 250$ nm, where the subthreshold slope goes below 60 for two orders of magnitude of drain current, well above the gate current. However, at even shorter channel lengths, the negative capacitance is not enough to overcome short-channel effects, and the subthreshold slope again degrades. Still, consistent improvement over the reference devices is maintained all the way down to $L_g = 30$ nm. A summary of the subthreshold slope improvements at short channel lengths are shown in 7.5.

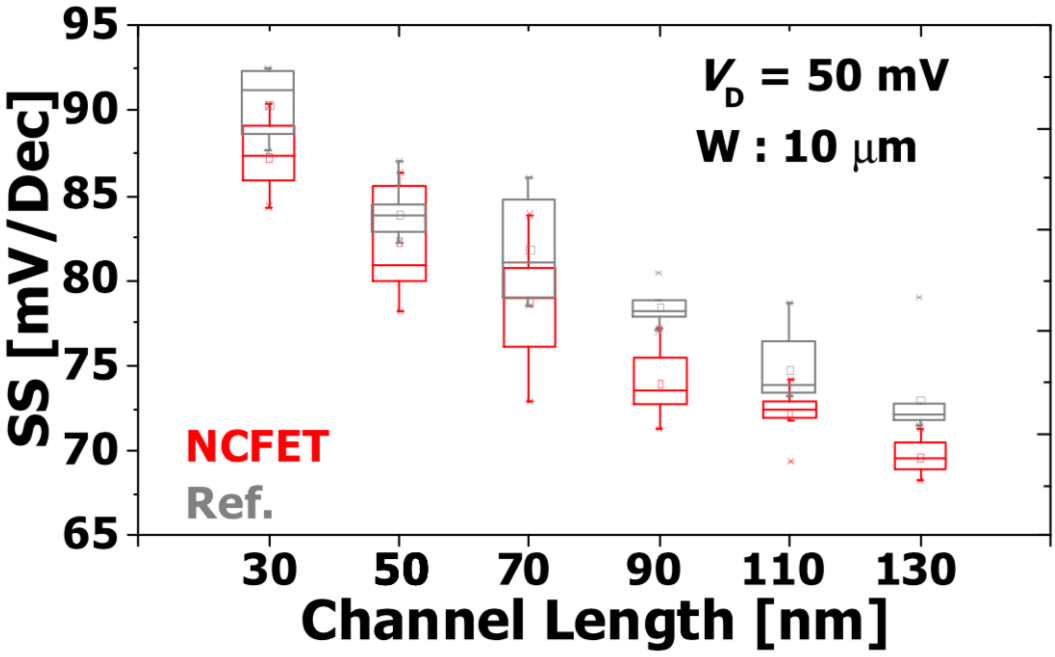

Figure 7.5: Minimum subthreshold slope for both reference FET and NCFETs as a function of L_g. Measurements are taken on multiple devices; the distributions are indicated by the error bars. Figure adapted from [71].

Aside from reduction of subthreshold slope, another major effect of negative capacitance is a reduction or even reversal of drain-induced barrier lowering (DIBL). The explanation for this is as follows: as the drain voltage is increased, the total charge in the channel is reduced. For a given gate voltage, this results in worse capacitance matching, meaning less voltage amplification. Therefore the tendency of the drain voltage to lower the barrier in the channel is compensated by the response of the ferroelectric. This behavior is also systematically observed and summarized in 7.2 for $L_g = 90$ nm devices. (a) and (b) show that the shift of threshold voltage is less for the NCFET device than the reference. (c) just tabulates this data and shows a lowering of DIBL from 82 mV/V to 47 mV/V for the NCFETs. The output characteristics are shown in (d), where a significant reduction of the output resistance is seen in the NCFETs over the reference FETs.

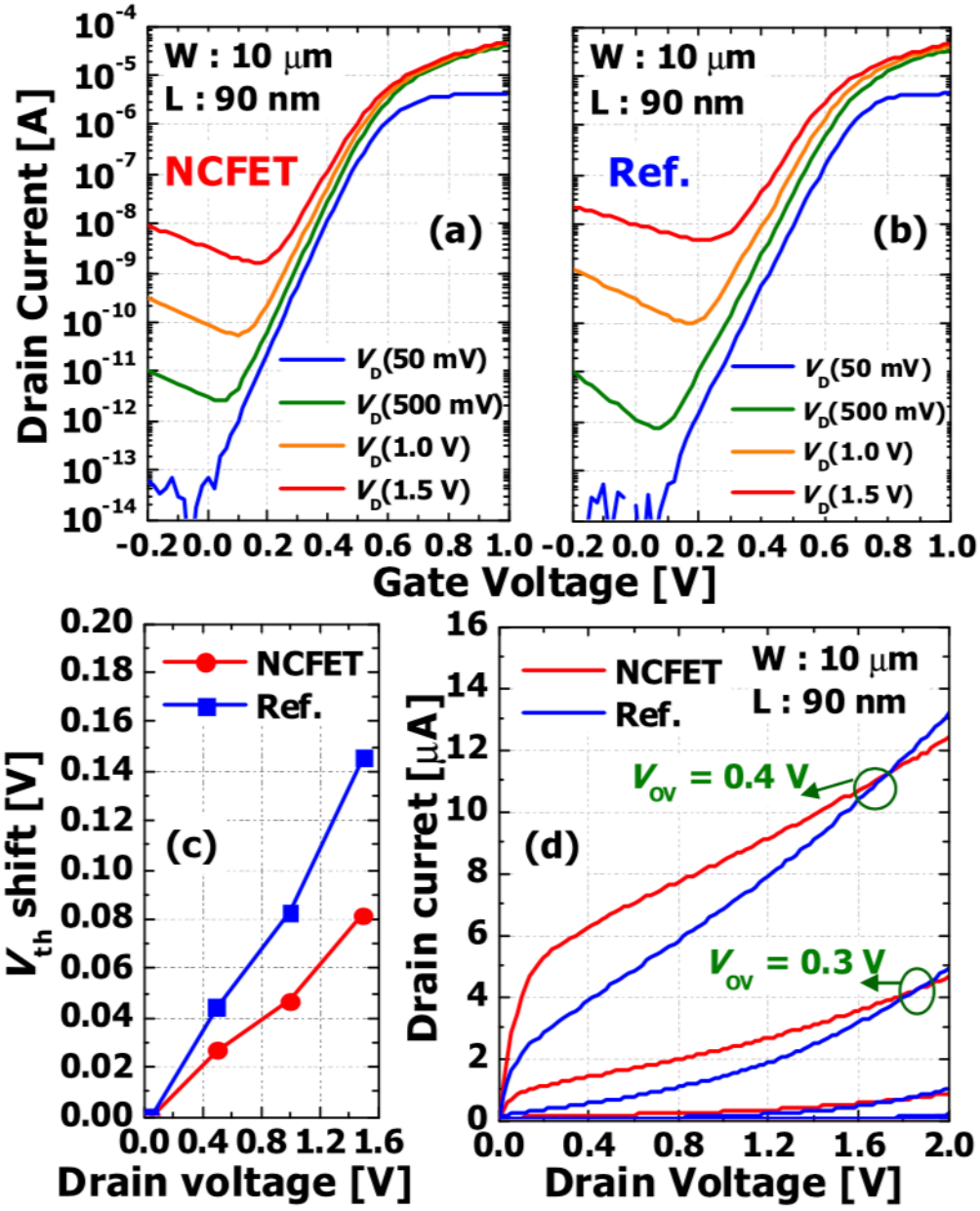

Figure 7.6: Comparison of drain-induced barrier between reference FETs and NCFETs, both at $L_g = 90$ nm. Transfer characteristics for the NCFETs and reference FETs are shown in (a) and (b), respectively. These data are summarized into one plot in (c). Output characteristics for various overdrive voltages are shown in (d). Figure adapted from [71].

7.3 Low-Frequency Transconductance Measurement

In order to provide a bridge between quasistatic I-V measurements and radio frequency (RF) scattering parameter (S-parameter) measurements, typically well past the GHz region of frequency, we attempt to measure the small-signal transconductance at frequencies in the kHz range, where we would expect little deviation from quasistatic behavior, and where the wavelength is sufficiently long for the lumped model to be valid. This removes the complication of incorporating a vector network analyzer, performing open-short calibrations, and modifying the layout to include waveguides in the metal layer to bring RF power into the device [77].

The small-signal transconductance g_m is defined as $\partial I_D/\partial V_G$. This can be cast into the language of two-port network theory for future comparison with RF network measurements. If the source terminal is grounded, the gate terminal is labeled 1, and the drain terminal is labeled 2, then the transconductance is just the admittance parameter Y_{21}. Two-port circuit parameters are usually reported in terms of S-parameters, which are the matrix coefficients relating the incident and reflected power wave amplitudes, which are related to Y_{21} according to 7.1 [78].

$$Y_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22}) - S_{12}S_{21}} \tag{7.1}$$

A schematic of the measurement setup is shown in 7.7. The DUT (device under test), in this case a FET, is connected via its drain terminal to a voltage waveform generator (Agilent 81130A) that applies a DC bias $V_{G,bias}$ in addition to a small-signal sine wave of amplitude ΔV_G and frequency f. The drain terminal is connected to the DC drain bias source $V_{D,bias}$, which is a Keithley 2720 DC voltage source. The source terminal is connected to a Ametek 7230 lock-in amplifier set to measure in the current (low-impedance) mode. The lock-in amplifier integrates the input current against a local oscillator whose frequency is set to f, and extracts the complex amplitude ΔI_D. The experiment was originally conceived with the lock-in amplifier operating in the more familiar voltage (high-impedance) mode being fed the output of a transimpedance pre-amplifier, but this was omitted due to problems with unreliable behavior of the instrument in setting the input current range.

The concurrent grounding of all instruments is assumed through shorting of the references via the coaxial shield lines, although this could be problematic, as discussed subsequently. The experimental setup is controlled through a LabView program that sends and reads input/output through serial and USB interfaces on the instruments. The DC gate bias is swept over a range of values, and the resultant ΔI_Ds are recorded at each bias point. The experiment is repeated for various small-signal amplitudes and frequencies, as well as DC drain biases. A typical measurement result is shown in 7.8 compared to the numerical derivative of the quasistatic I-V obtained as described previously. Reasonable agreement is attained. The numerically integrated transconductance data are plotted alongside the raw quasistatic I-V data in 7.9. The range of measurement is limited by current sensitivity of the lock-in amplifier.

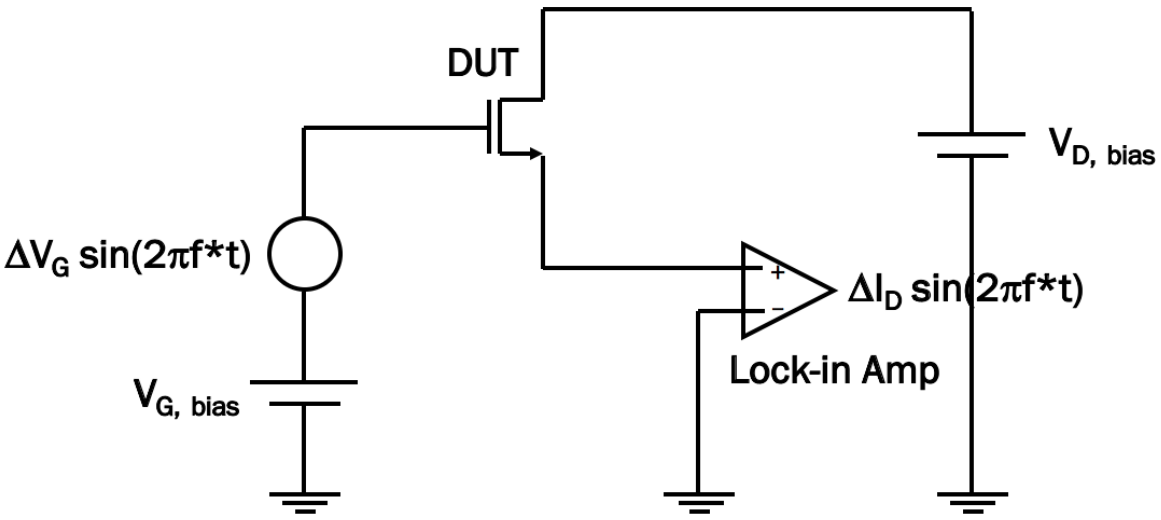

Figure 7.7: Schematic of the small-signal transconductance measurement setup. DUT stands for "Device Under Test." The small-signal amplitudes are used to calculated the transconductance.

Unresolved issues with the measurement setup appear as the frequency is increased even moderately. As seen in 7.10, there is a significant peak g_m variation as the frequency is changed. This is presumably due to bias temperature instability and may be resolved with a lower stress biasing scheme. More critically, there is significant reduction of the peak g_m corresponding to a single pole at ∼10 kHz. While the cable capacitance and probe station parasitics may be non-negligible, even a 100 kΩ gate resistance is not sufficient to explain a pole so low in frequency. The measured gate resistance is found to be no more than a few Ωs. Because this issue could not be resolved, these measurements were not continued beyond a preliminary stage.

7.4 Pulse-gated IV Measurement

Defect states at the interface of the semiconductor channel and the gate oxide are one of the key challenges to solve in a fabrication process. In industrial CMOS processes, the mid-gap D_{it} can be as low as a few 10^{10} cm^{-2} eV^{-1} [79]. Ideally, vacuum would not be broken from after cleaning of the silicon channel until deposition of the gate metal layer is complete. Unfortunately, the wafer must not only be exposed to the atmosphere, but transported outside the cleanroom after thermal oxidation of the interfacial oxide for atomic layer deposition of the hafnia. This results in a D_{it} typically 2 orders of magnitude higher than the industrial standard, leading to charge trapping and hysteresis, as well as a degradation of subthreshold

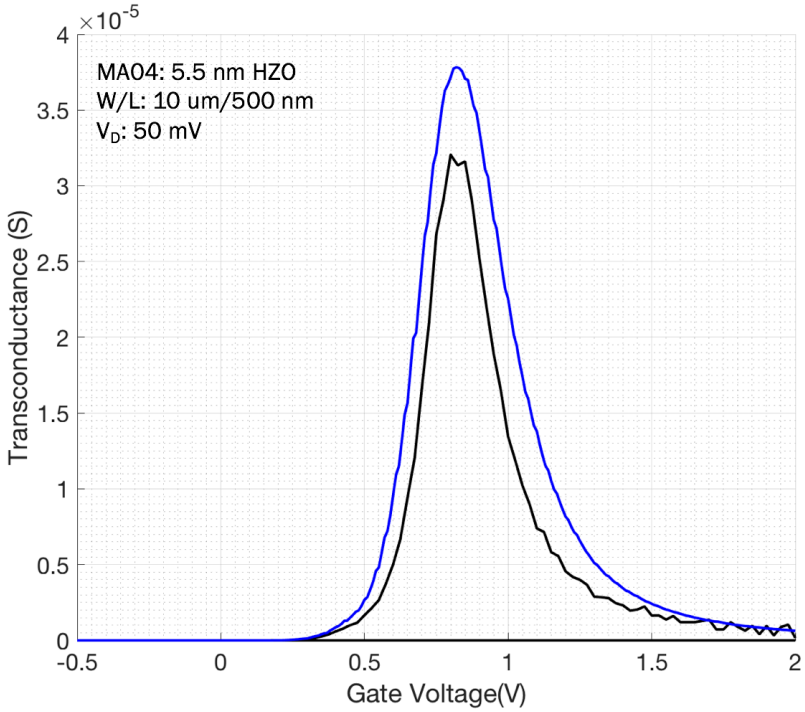

Figure 7.8: Typical transconductance measurement of an NCFET. Data taken with the transconductance measurement setup (blue) are plotted against numerically calculated values from a quasistatic measurement of the same device (black). $f = 1$ kHz.

slope. The standard technique to discard the effect of the interface states is to apply a voltage pulse to the gate, and measure the drain current before the interface states can respond, typically on the order of a few 100 μs or greater [10] [80]. We briefly describe the results of this pulse-gated I-V technique.

The primary challenge of pulsed I-V measurements is the current measurements. Because this is a transient measurement, the integration time for the current is limited, which makes measuring low current values difficult. Because the off-current of the fabricated transistors is several orders of magnitude below the instrument limitations, we are unable to measure the full subthreshold regime. Devices measured have $L_g = 500$ nm and $W_g = 50\mu$m and are from the same process as the devices in 7.2. 7.11 shows the quasistatic transfer characteristics versus those obtained with pulsed I-V. We use the fast I-V module of a Keysight B1500A Semiconductor Device Analyzer. Data are shown for both branches of the ferroelectric hysteresis. Two different sets of pulse parameters are used. In one case, the voltage pulse is held for 30 μs for transients to settle, and then the current is measured for 30 μs. In the second case, both hold and integration times are increased to 1 ms. In both cases,

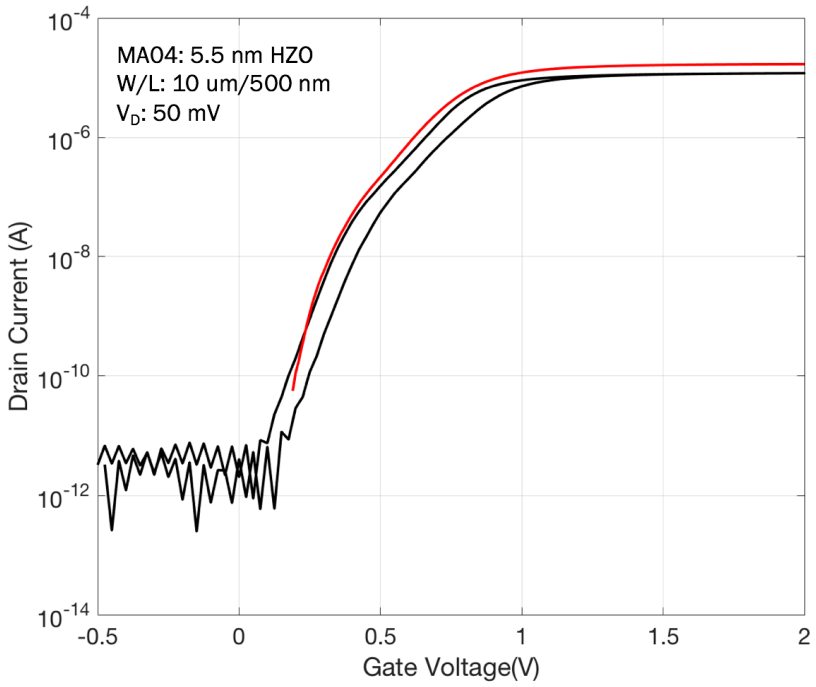

Figure 7.9: Numerically integrated values of the transconductance data in 7.8 are plotted in red alongside the raw measured quasistatic I-V data also corresponding to 7.8 (black). The reverse (right-hand) branch of hysteresis due to charge trapping is also shown.

the measurement becomes unreliable at ∼0.1 nA of drain current. All pulsed I-V curves are steeper than the quasistatic curves, confirming that there is significant degradation of subthreshold slope from C_{it}.

7.5 Ferroelectric FET Memory Characterization

In addition to being the primary candidate for negative capacitance, ferroelectric doped hafnium oxide has re-ignited interest in ferroelectric memories [59]. They offer a number of advantages over their perovskite predecessors: (1) Hafnium oxide is already integrated into industrial processes as a high-κ dielectric. (2) The higher coercive field leads to excellent retention. (3) Ferroelectricity has been observed down to thicknesses of just a few nm in HfO_2, which is promising for scalability.

We report on the ferroelectric FET memory operation of devices fabricated using the replacement gate process described in 6.3. In this batch, the HZO devices exhibited improved subthreshold slope over the reference FETs, but not sub-60 mV/decade. However,

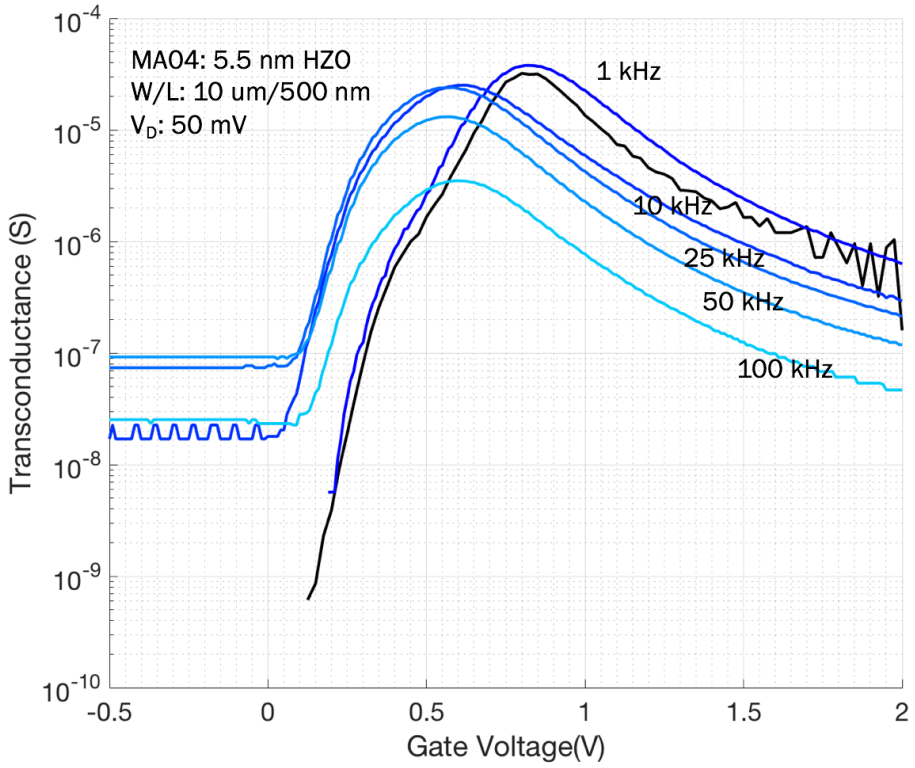

Figure 7.10: Transconductance data for a range of measured frequencies. The numerically differentiated quasistatic I-V curve is again shown in black. The measurements suffer from peak g_m variation and an unexplained pole at $\sim$10 kΩ.

good memory behavior was observed. Negative capacitance and hysteresis are not mutually exclusive [22]. If the capacitance is not matched at the zero polarization state, there will be hysteresis, but the remanent polarization states can be in the negative capacitance region of the ferroelectric. The reduction of subthreshold slope over the control along with the presence of hysteresis suggests that this is the case for these devices [62].

The memory behavior of these devices is remarkable primarily because of the large number of program/erase cycles before breakdown, which exceeds 10^7. Furthermore, recovery of the devices is seen after 24 hours. This indicates that the breakdown mechanism is most likely stress-induced leakage current of the interfacial dielectric. This is the first known observation of a program/erase endurance above 10^7 in hafnium-based ferroelectric FET memory. Other reports of high progam/erase endurance employ much thicker ferroelectric layers, typically on the order of 20 nm or greater [81] [82] [83] [84] [85].

We now report the standard memory cell characterization for the single n-type transistor cells with $L_g = 500$ nm and $W_g = 50\mu$m. The state of the memory is reported as the low-V_{DS} ($V_{DS} = 50$ mV) values of drain current I_D at $V_{GS} = 0$. In the program or "off" state, a large positive gate voltage has been applied, and the ferroelectric polarization is oriented

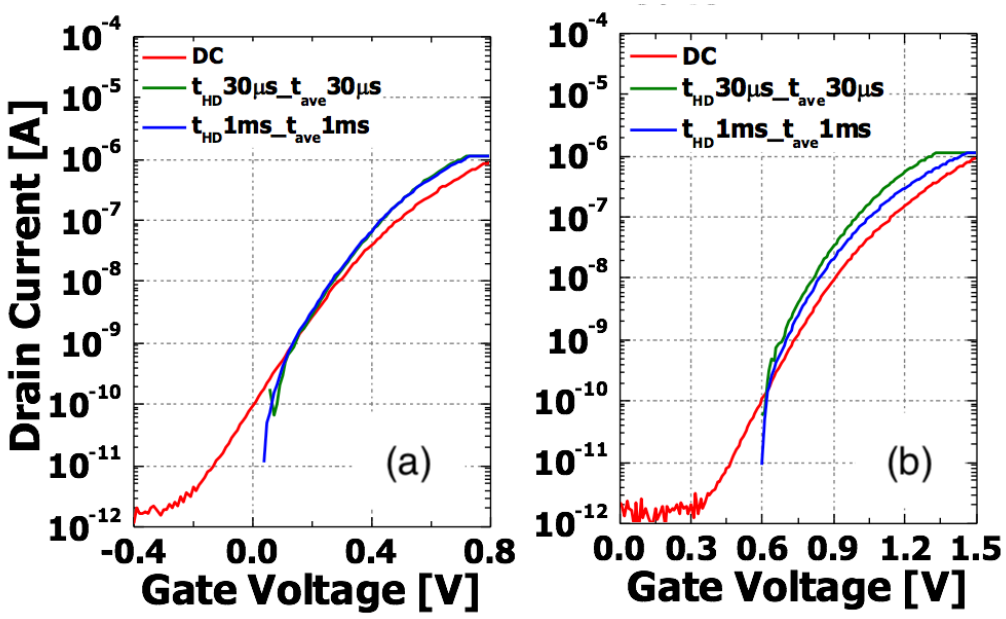

Figure 7.11: Transfer characteristics for left (a) and right (b) branches of the ferroelectric hysteresis. Pulsed I-V measurements for two different sets of pulse parameters are shown. t_{HD} is the time between the application of the gate voltage pulse and the measurement of the drain current when transients are allowed to settle. t_{ave} is the duration for which the current is measured.

towards the channel, causing the threshold voltage to shift to the right, lowering the 0 V V_{GS} value of I_D. In the erase or "on" state, a large negative gate voltage has been applied, and the ferroelectric polarization is oriented toward the gate contact, causing an increase of I_D at $V_{GS} = 0$ V. All devices have 1000 program/erase cycles applied to the gate before any characterization is performed, to account for the well-known ferroelectric wake-up effect in hafnium-based ferroelectrics [86].

The state is read by applying a small V_{DS} and measuring I_D. The sensitivity of the memory cell to disturbance caused by the read operation is minimal, as shown in 7.12.

Programming/erasing of the state is performed by applying 100 μs pulses of +/- 5 V at the gate, while grounding all other terminals. A program/erase cycle thus consists of two pulses, which are also separated by 100 μs. Repeated switching of the ferroelectric produces dielectric stress over the interfacial dielectric, which eventually causes soft breakdown, resulting in a large increase of gate current. A slight increase of the off current is seen over the course of cycling, but the on current is constant until breakdown occurs at ¿ 10^7 cycles. The data prior to breakdown are shown in 7.13.

After 10^7 program/erase cycles, almost no change in the transfer characteristics is seen. The black curve in 7.14 is the initial transfer curve, and the blue curve is after 10^7 pro-

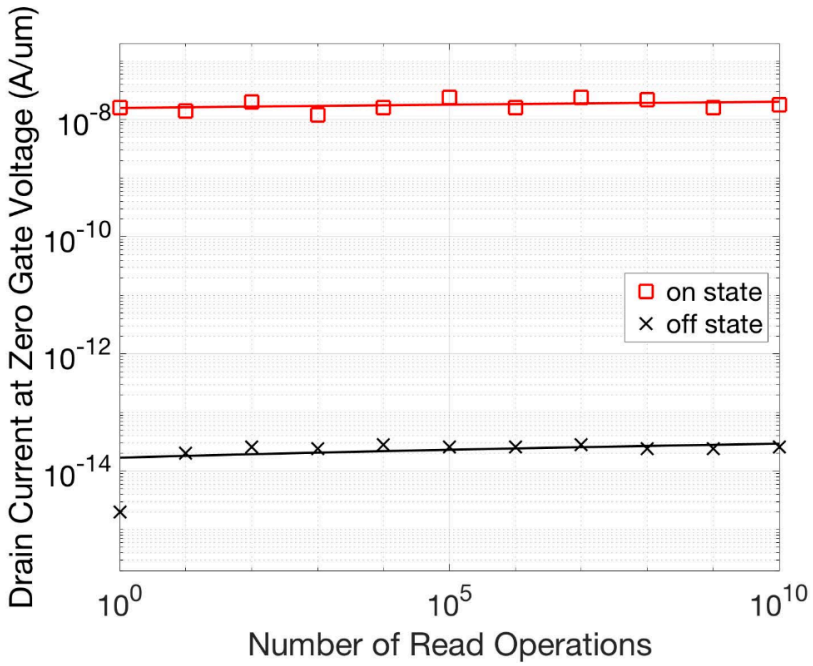

Figure 7.12: Read endurance of both the on and off states of the ferroelectric memory transistor. Measurements are taken at 300 K. The straight lines are linear fits to the experimental data. Figure adapted from [62].

gram/erase cycles. 7.15 shows the transfer characteristics before and after dielectric breakdown. The after breakdown data were taken 24 hours after breakdown occurred, allowing for recovery. A slight wake-up behavior is noted in the form of the threshold voltage shifting to the left. A degraded subthreshold slope is also noted in the after breakdown characteristics, probably from defects that were created in the gate dielectric stack during breakdown. We hypothesize that the recovery may be due to charge trapping in HZO at the localized soft breakdown spot [87]. Breakdown recovery may have significant practical benefit in increasing the number of endurance cycles at which the number of bits exceeds the limit of defective bits that the error-correction code is designed to handle.

Retention measurements are also performed at elevated temperatures of 55 °C and 85 °C. The data are shown in 7.16. Measurements are taken up to 10^5 sec and extrapolated to 10^9 sec, which is approximately 10 years. Almost no degradation is observed at 55 °C, and while there is noticeable loss of the on/off ratio at 85 °C, mostly via degradation of the on current, an on/off ratio of 10^4 is maintained.

Finally, we examine the dependence of the ferroelectric memory on pulse amplitude and duration, the main results of which are shown in 7.17. As expected, minimum pulse duration needed to program the memory state decreases with increasing pulse amplitude. However,

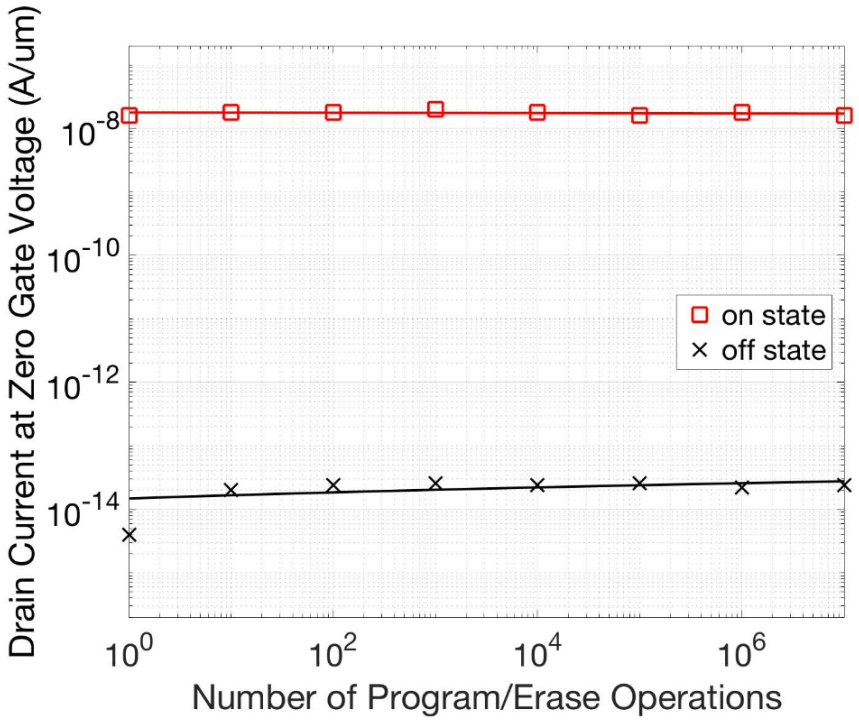

Figure 7.13: Program/erase endurance of both the on and off states of the ferroelectric memory transistor. Measurements are taken at 300 K. The straight lines are least-square error linear fits to the experimental data. Figure adapted from [62].

this comes at a cost of degraded program/erase endurance, which falls below 10^7 above 5 V of pulse amplitude.

7.6 Conclusions and Future Work

We have given an overview of the various methods used to characterize the behavior of our fabricated NCFETs. First, we described the standard methods of obtaining I-V and C-V curves, and demonstrated the results of taking these measurements on fabricated NCFETs. It was also discussed how negative capacitance operation could be deduced from these measurements. Subsequently in 8 it will be discussed how the ferroelectric "S-curve" characteristics may be extracted from these experiments.

Next, we described the construction of a setup to directly measure the transconductance by sinusoidally modulating the gate voltage and measuring the resultant response in the drain current with a lock-in amplifier. Future work could involve debugging the unexplained pole near 10 kHz that impedes any frequency-dependent measurements that may be carried out. However, reasonably good agreement with quasistatic measurements are obtained at 1

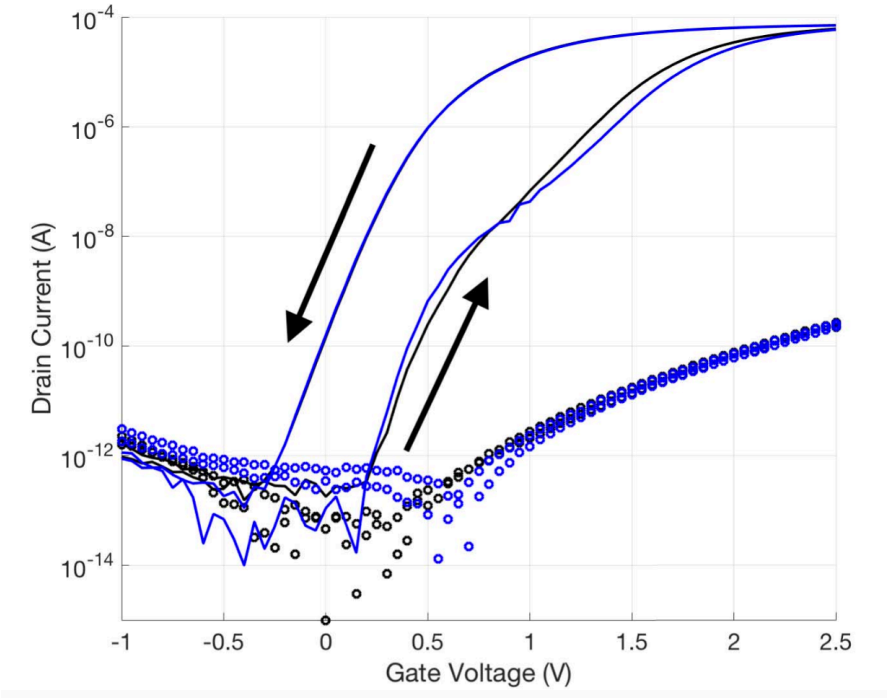

Figure 7.14: $I_D V_{GS}$ transfer characteristics before (black) and after (blue) application of 10^7 program/erase cycles. Arrows indicate the direction of the hysteresis as counter-clockwise. Figure adapted from [62].

kHz. One potential advantage of this method is that the source-drain current and gate-drain current should be in opposite phase, so separation of the two quantities can be done with a single measurement. The natural continuation of the transconductance work is to carry it out at GHz and higher frequencies, although this is a major undertaking that requires mask redesign, device fabrication, and the construction and calibration of a measurement setup with RF probes and a vector network analyzer. It will also be necessary to improve the contact and source/drain extension resistances to obtain characterization data meaningful for analog applications of negative capacitance.

Following this, results obtained from taking pulsed I-V measurements were discussed. A voltage pulse applied at the gate allows for measurement of the drain current before defect states can respond, effectively discarding their behavior from the characterization, which is found to improve the subthreshold slope.

Finally, we discussed memory-mode operation of the replacement gate transistors with 5.5 nm of ferroelectric $Hf_{0.8}Zr_{0.2}O_2$ in the gate stack. The memory cells were characterized for their read endurance, program/erase endurance, elevated temperature retention, breakdown recovery, and speed of response. It was found that the devices could be switched in 100

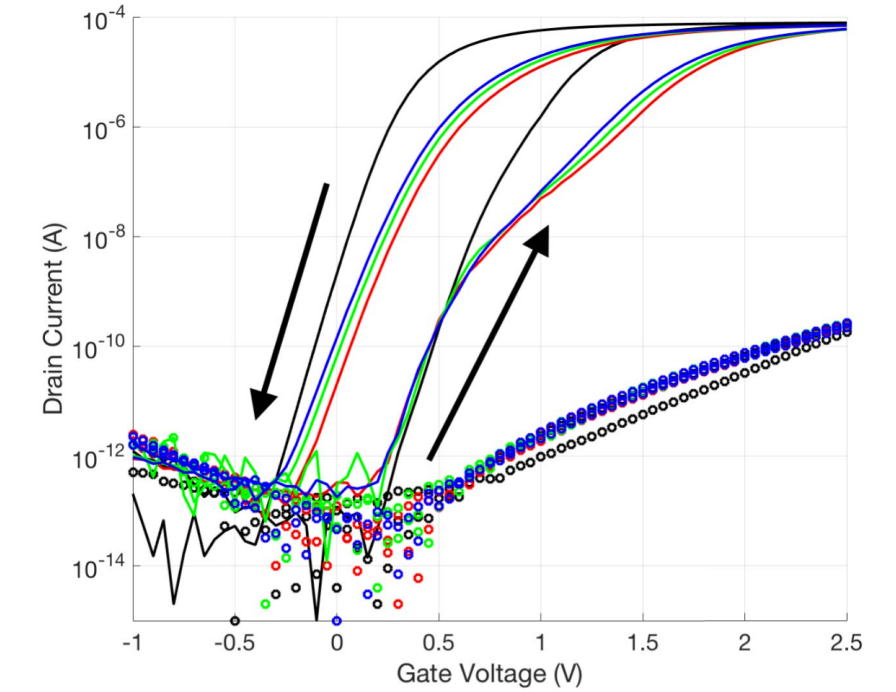

Figure 7.15: I_D-V_{GS} transfer characteristics before (black) and after (red, green, and blue) breakdown and recovery. The red, green, and blue curves correspond to the first, second, and third gate voltage sweeps after recovery, respectively. Figure adapted from [62].

ns with a 7 V pulse. The somewhat gradual dependence of the on/off ratio on pulse width inspired some investigation into the multi-level memory operation of these devices. Such devices have potential application as hardware for neural networks [70]. It was found that using pulse width to control the on/off ratio was not promising, as the device tends to saturate at a partially switched state after 1 or 2 pulses. Modulating the state by changing the amplitude of the program/erase pulse was somewhat more promising, although our devices presently suffer from significant variability issues in this application.

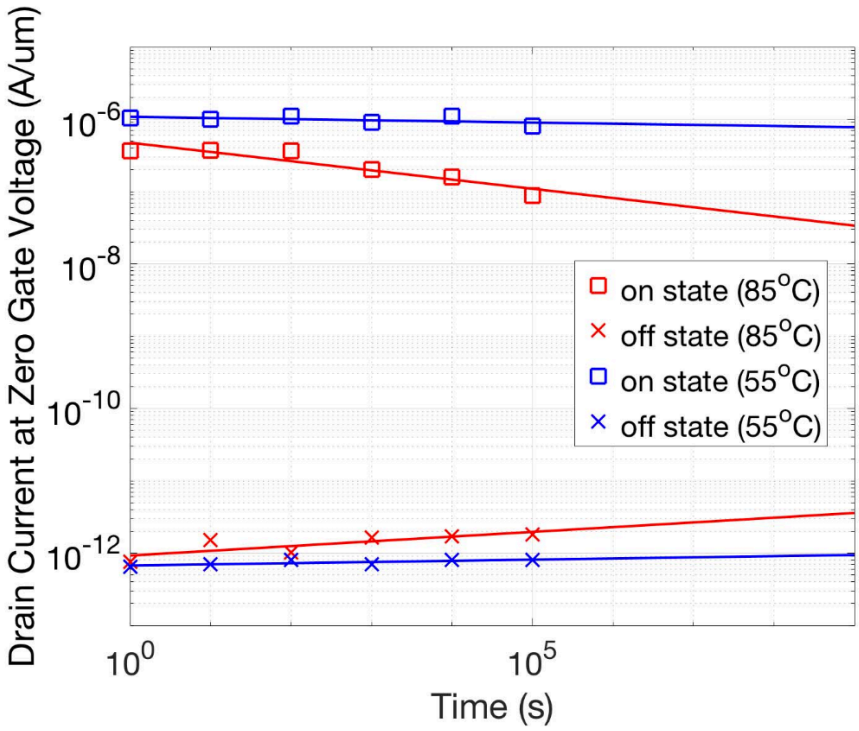

Figure 7.16: Retention of memory state as a function of time, measured to 10^5 sec and extrapolated to 10^9 sec ($\sim$ 10 years). Figure adapted from [62].

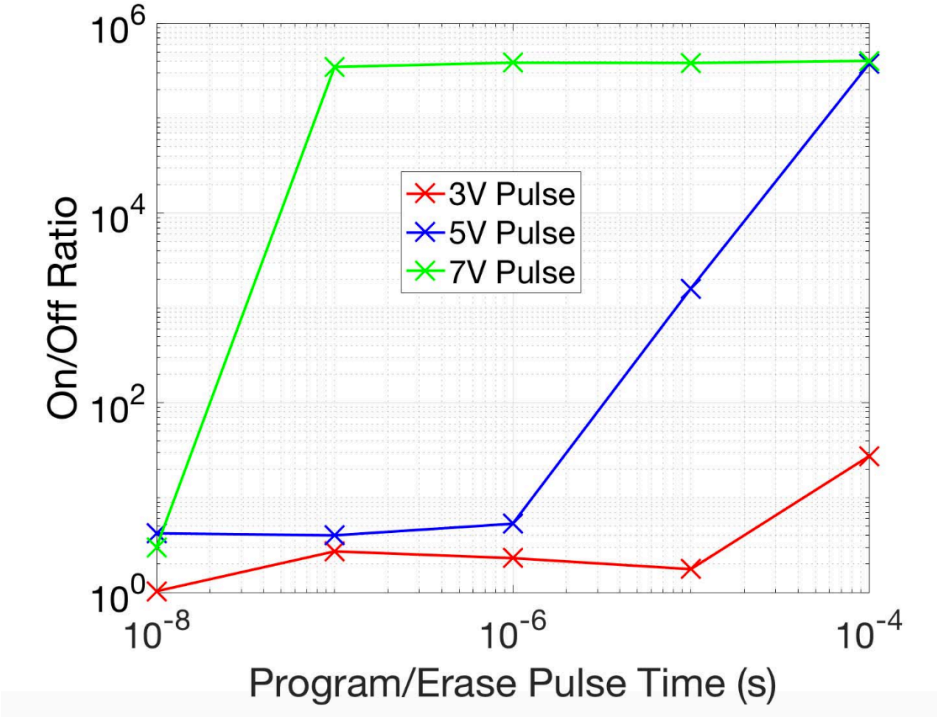

Figure 7.17: I_{ON}/I_{OFF} ratios as a function of pulse width for various pulse amplitudes. Higher pulse amplitudes can switch the ferroelectric faster, but at the cost of degraded program/erase endurance. Figure adapted from [62].

Chapter 8

Simulation of Negative Capacitance FETs

8.1 Introduction

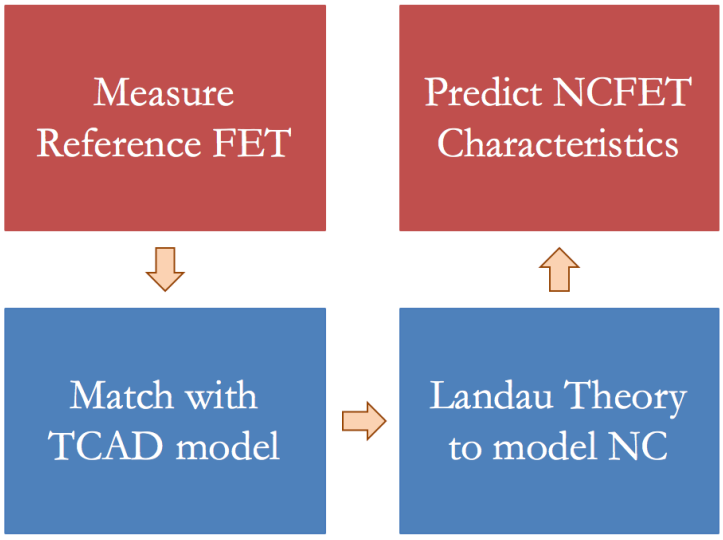

Figure 8.1: Flowchart of the design process for extracting ferroelectric characteristics.

Understanding capacitance matching in negative capacitance FETs requires the ability to separate out the variation and non-idealities of the underlying transistor from the behavior of the ferroelectric. This is non-trivial, as the two may affect each other. However, by controlling the experimental process and characterization measurements closely, one may hope to build models that accurately describe the observed characteristics, which can then be used to design the next round of fabrication and measurements, the results of which can

update the model, and so on. The ultimate goal of this loop is to gain insight into what conditions (device geometry and structure, process conditions, etc.) result in what kind of charge-voltage characteristics for the ferroelectric.

The simulation framework is as follows. First, the experimental devices are fabricated and their characteristics are measured. Second, a technology computer-aided design (TCAD) model using commercial software (Sentaurus) is developed, which reproduces the behavior of the reference FETs, which fabricated with a normal dielectric in the gate stack. The TCAD model provides the charge-voltage relationships for the baseline device, which cannot normally be measured directly because layout parasitics typically dominate. The TCAD model also provides the field distribution inside the transistor, which allows for the extraction of an effective "internal gate." Finally, a Landau-Devonshire model is created for the ferroelectric. This model (the internal gate voltage and gate charge as functions of the external gate voltage) is used to replace the gate dielectric with the Landau-Devonshire ferroelectric. Thus, for a given internal gate voltage value, which also determines the gate charge and the drain current, we calculate the voltage that would be dropped across the ferroelectric. This is the external gate voltage predicted for the NCFET. The ferroelectric model is adjusted to fit to the experimentally measured NCFET data and resolve any apparent inconsistencies. The adjusted model can now be used to simulate a variety of device structures, which guides design of the fabrication process. 8.1 illustrates this process with a flowchart.

8.2 Theoretical Framework

First, we quickly re-state the constitutive formalism of the ferroelectric material, the Landau-Devonshire theory. The free energy density is expanded in even powers of the polarization density, in this case to fourth order, and coupled to the electric field, shown in 8.1. Note that α must be negative for a ferroelectric [20] [15] [14].

$$u = \alpha P^2 + \beta P^4 - EP \tag{8.1}$$

Setting $\frac{\partial u}{\partial P} = 0$ gives the stationary states and the S-curve relationship between polarization and electric field (8.2).

$$E = 2\alpha P + 4\beta P^3 \tag{8.2}$$

The coefficients α and β are related to the coercive field E_C and the remanent polarization P_r by the definitions $P_r = P(E = 0)$ and $(\frac{\partial E}{\partial P})_{E=E_C} = 0$. 8.3 gives the solutions for the fourth-order case.

$$\alpha = \frac{-3\sqrt{3}E_C}{4P_r} \tag{8.3a}$$

$$\beta = \frac{3\sqrt{3}E_C}{8P_r^3} \tag{8.3b}$$

The voltage across the ferroelectric and the charge on the gate are calculated from E and P according to the standard results for a parallel-plate capacitor, $V_{FE} = E\, t_{FE}$ and $Q_{FE} = DA_{FE} = (\epsilon_0 E + P)A_{FE} \approx PA_{FE}$, where t_{FE} and A_{FE} are the thickness and area of the ferroelectric film, respectively, and D is the displacement electric field. For a bias point of the "internal" FET as given by the TCAD model, $V_{g,internal}$ and Q_g, the external gate voltage of the NCFET is given by the series condition $V_{g,external} = V_{g,internal} + V_{FE}$. Also according to the series condition, the charge on the external gate is taken to be $Q_{FE} = Q_{g,internal} + \Delta Q$, where $Q_{g,internal}$ is the charge on the internal gate. The parameter ΔQ represents an offset of the S-curve relative to the baseline characteristics, which arises from charged defect, strain, or composition gradients [15]. Additionally, we introduce a fringing field capacitance C_f that models coupling of the ferroelectric to the drain.

8.3 Results for Gate-First HZO NCFETs

First, we describe the development of the TCAD model, which is fairly straightforward. 8.2 shows part of the completed structure with a colormap of the electron mobility in the device layer. We focus on modeling of the $L_g = 90nm$ FETs with gate width $W_g = 1\mu m$. First the various material regions and their geometries are defined in a structure editor according to the fabrication process for the gate-first transistors described in 6.4. This consists of the silicon substrate, 200 nm of buried oxide (BOX), and a 30 nm silicon-on-insulator (SOI) device layer. Following this, the gate stack is defined, consisting of 2 nm SiO_2, the top 1 nm of which is nitrided, 5 nm of dielectric HfO_2 with a dielectric constant $\epsilon_r = 18$, and finally the tungsten gate metal with a work function of 4.8 eV. Ion implantation is then simulated in a process simulator, after which the interlayer dielectric (ILD) is defined.

The basic drift-diffusion model is used for transport. A basic doping-dependent model is used for the carrier mobility. Band-to-band tunneling is also modeled, as are the doping-dependent Shockley-Read-Hall (SRH) recombination and avalanche generation. These are sufficient to obtain excellent matching at low values of drain-source voltage (V_{DS}). Work is still currently ongoing to improve the TCAD model, particularly behavior at high V_{DS} values. The difficulty lies in accurately capturing the behavior at the onset of strong inversion, which is sensitive to the models used for mobility. Thus far the mobility models explored include the Caughey-Thomas model for high-field saturation, the Philips unified mobility model, including an extension to inversion and accumulation layers, and an interface charge model for scattering from defects near the surface [88]. A wide variety of effects may be considered, and it is unclear which are most relevant for the fabricated devices. Further investigation is required.

The results of the TCAD simulation are compared against experiment in 8.3. The TCAD model is closely matched to the experimental data for the reference FET. Plotting the drain current versus the voltage at the internal gate node - which is not a real node, but obtained from averaging the potential at the high-κ-SiO_2 interface - gives the characteristics of the internal transistor which is assumed to be common to both reference FET and NCFET. Of

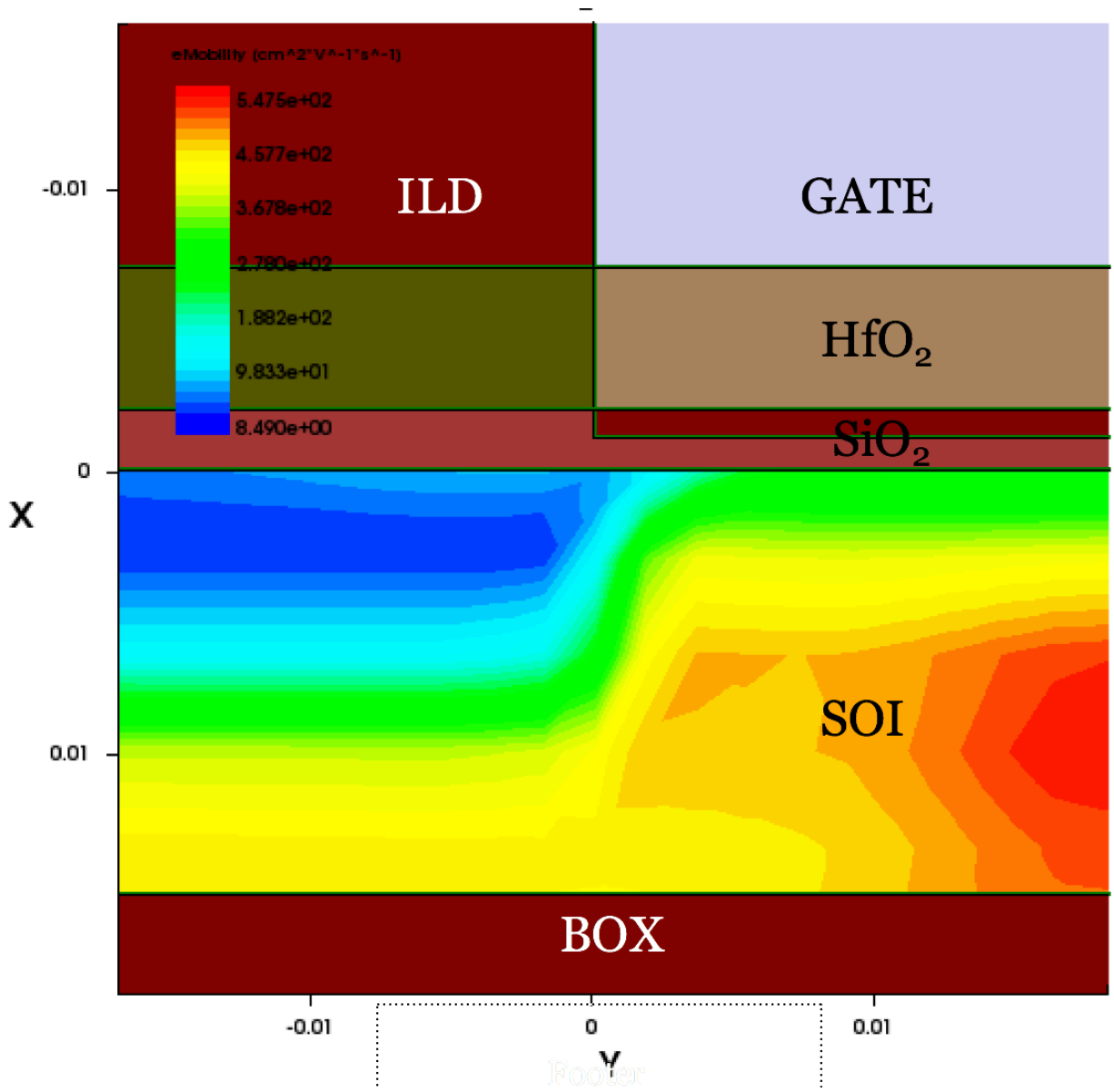

Figure 8.2: Visualization of the TCAD FET structure with various regions indicated. Colormap shows electron mobility in the SOI device layer.

course, discarding spatial variation in the interface potential is not always valid. Nevertheless, it is worth investigating to what extent one can use a fully lumped model for the ferroelectric.

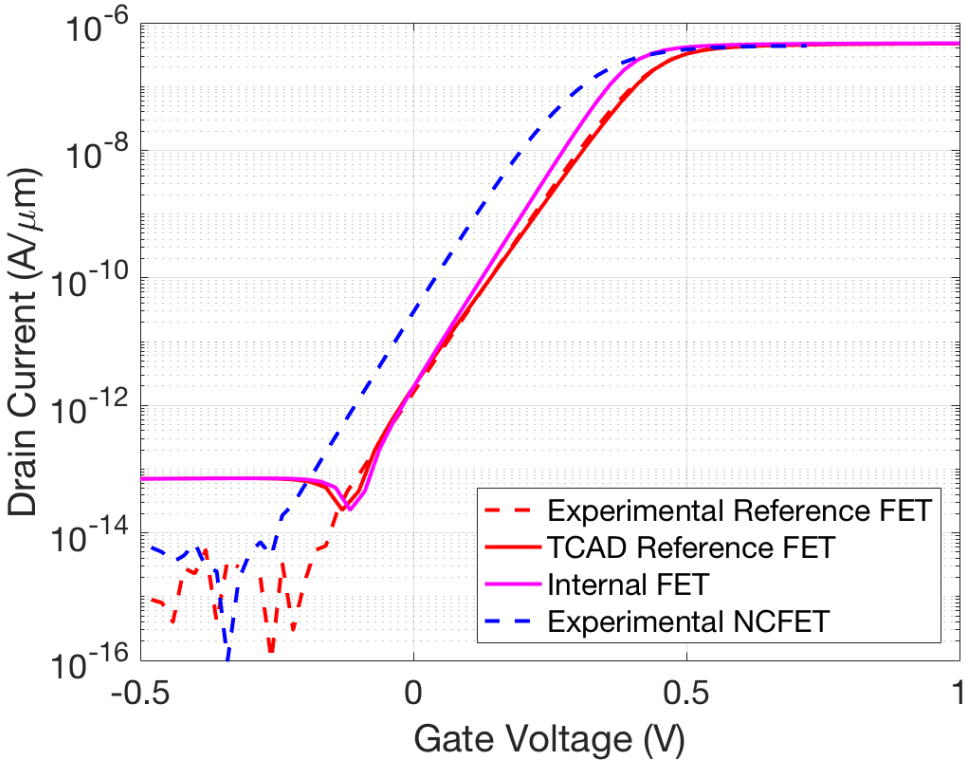

Figure 8.3: I_D-V_G characteristics from TCAD simulation versus experimental data. The TCAD is matched closely to the experimental data for the reference FET. Additionally the model yields the characteristics of the internal FET which is presumed to be common to both the reference FET and the NCFET.

At this point, the task is simply a matter of varying the ferroelectric model parameters so that the ferroelectric model plus the internal FET characteristics yield the correct NCFET characteristics. The free parameters are P_r, E_C, ΔQ, and C_f. ΔP is sometimes given instead of ΔQ; the two are related by the area of the channel $L_g W_g$. The first three parameters are optimized over to fit to the low V_{DS} characteristics of the NCFET, and then C_f is adjusted to match behavior over all V_{DS} values. The optimization consists of a simple brute force search over ranges guided by back-of-the-envelope calculations. We define an error metric, the distance between two I_D-V_G curves, as the standard L_2 norm, given by 8.4.

$$d^2 = \int (log|I_{D,fit}| - log|I_{D,meas}|)^2 dV_G \tag{8.4}$$

$I_{D,fit}$ and $I_{D,meas}$ are the fitted and measured values of drain current. In the first stage of optimization, any combination of P_r, E_C, and ΔQ that results in a sufficiently low error metric for the low V_{DS} characteristics is recorded as a solution. Then, C_f is swept over its range for every solution of the first stage. The error metric in this stage is a sum of error metrics for individual curves at $V_{DS} = 50$ mV, 500 mV, and 1 V. A close to optimal solution is shown in 8.4. We note that the band-to-band tunneling is not accurately modeled by the TCAD for the input data to the ferroelectric model in this case. $P_r = 0.7\ \mu C/cm^2$, $E_C = 0.175\ MV/cm$, $\Delta P = 0.4\ \mu C/cm^2$, and $C_f = 0.16\ fF/\mu m$.

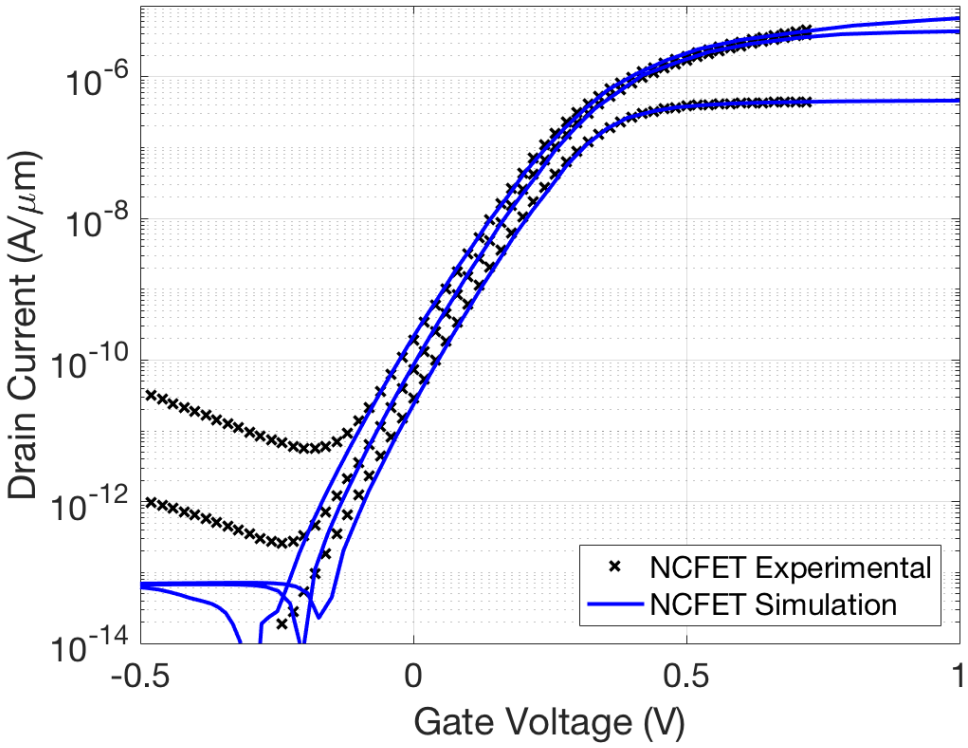

Figure 8.4: A near-optimal ferroelectric model that closely reproduces NCFET transfer characteristics. The three sets of curves are for $V_{DS} = 50$ mV, 500 mV, and 1 V.

It is worthwhile to examine the uniqueness of solutions in this space, both for the first and second stages. Without an explicit set of design constraints for some purported use of the model, it is impossible to definitively classify a given parameter set as a valid solution (i.e. good match) or not, in other words the choice of cutoff for the error metric is somewhat arbitrary. It is therefore sensible to look at the distribution of error metric in parameter space, concentrating on regions that are at least not grossly inaccurate. 8.5 looks at the distribution of solutions colored by their error metric in a P_r-E_C slice of parameter space. Encouragingly, good solutions tend to cluster around an optimal point away from which the

error increases gradually instead of being scattered randomly, suggesting that the inferred ferroelectric characteristics are more than just numerical flukes that periodically provide a good match. Existence and uniqueness means that the model is not over- or under-determined.

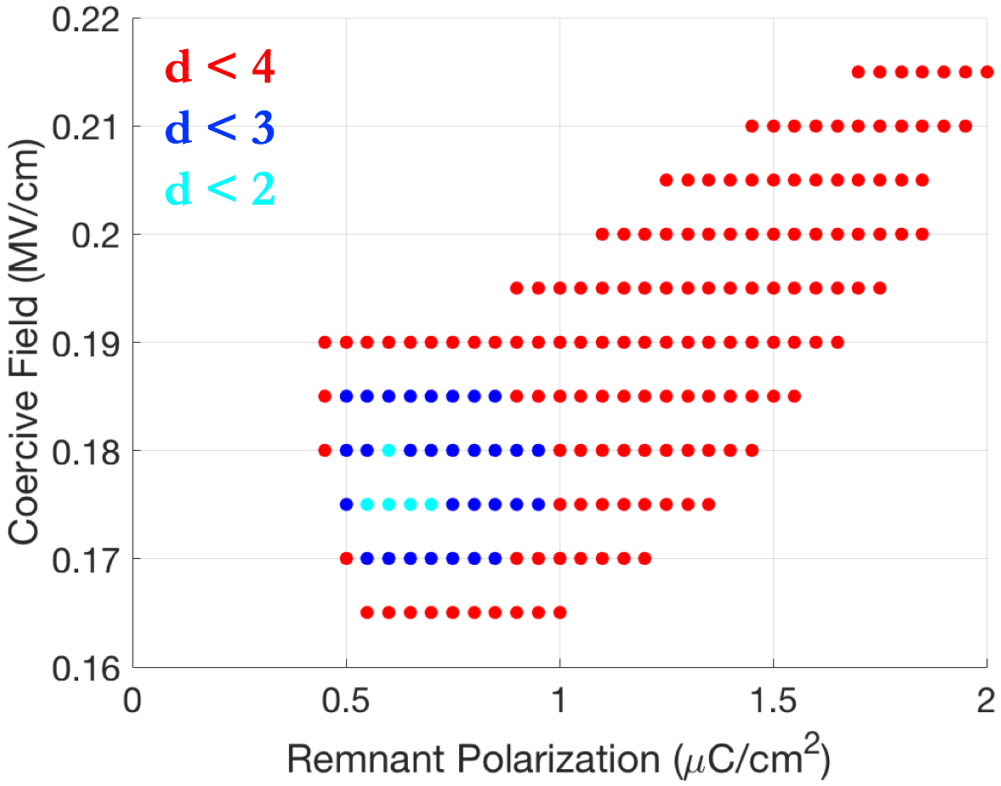

Figure 8.5: Distribution of solutions for the first phase of parameter optimization over P_r and E_C. d here is the error metric defined in 8.4.

The error metric d depends on extraneous variables like range of integration and should not be taken to have physical meaning. The chosen definition is meant to disproportionately weight good matching in the subthreshold regime. Even though results are given in terms of the log-error, optimization was done for both logarithmic error and linear error, whose definition is given in 8.5. Ultimately, a useful model will describe behavior well in both subthreshold and strong inversion.

$$d^2 = \int (I_{D,fit} - I_{D,meas})^2 dV_G \tag{8.5}$$

The way in which solutions are distributed in 8.5 shows the rough validity of the simplest model, which estimates an average voltage gain and a single value of negative capacitance for

the ferroelectric. This single value of negative capacitance would be proportional to $-P_r/E_C$, consistent with the fact that the $d < 4$ solutions all lie close to a line of constant P_r/E_C in P_r-E_C space. It is worth commenting on the unusually low values of P_r and E_C arrived at in these simulations, as they are approximately an order of magnitude below experimentally measured values in quasistatic P-E hysteresis loop measurements [46] [69] [30] [59]. The first point is that P_r and E_C are just familiar quantities with which to parameterize the ferroelectric characteristics; what is selected for in the optimization of the characteristics is the range of charge over which the capacitance is negative and what that value of negative capacitance is. As the ferroelectric exits the negative capacitance region, its capacitance remains approximately infinite for the range of voltages of interest. A ferroelectric charge-voltage characteristic derived from a Landau-Devonshire model cannot be valid far away from $P = 0$, as the capacitance goes monotonically to zero [20]. In the case where the behavior needs to be matched deep into the positive capacitance regime of the ferroelectric, an additional positive capacitance should be placed in series to represent the normal dielectric polarizability of the material.

Now we examine the distribution of solutions in the second phase of optimization, which varies C_f for different solutions of the first phase. 8.6 shows the distribution of solutions of the second phase against a slice of parameter space, now in P_r and C_f. Again the solutions are seen to cluster around a clear optimum in a relatively small region of parameter space.

8.4 Conclusions and Future Work

We have described the development of a TCAD model matched to experimentally measured I-V characteristics of gate-first HfO_2/W gate reference FETs. The TCAD model was then used to provide information about gate charge and internal potentials, which could be used to effectively replace the high-κ dielectric of the TCAD model with a lumped single-domain Landau-Devonshire model of a ferroelectric. We focused on results for a $L_g = 90$ nm FET with 2 nm SiO_2 and 5 nm HfO_2 for the gate stack. The NCFET whose characteristics are to be reconstructed from the Landau-Devonshire model has 5 nm of $Hf_{0.8}Zr_{0.2}O_2$ in place of the HfO_2. It was found that the inferred S-curve of the ferroelectric under these conditions is significantly renormalized from what one would naïvely expect from fitting a third-order polynomial to a P-E hysteresis loop taken on a metal-ferroelectric-metal (MFM) capacitor.

The most pressing future work is to fully match the TCAD model to the reference FET for all bias points. This is a critical step without which the high-V_{DS} matching of the NCFET has limited meaning beyond a conceptual exercise. The next immediate step is, once the TCAD model is fully calibrated, to re-run the optimization and make predictions for different FET fabrication conditions (for example, a thicker interfacial dielectric), carry out fabrication with those conditions, and verify the validity of the model, in other words carry out several iterations of the design loop. It may emerge that a lumped model is definitively insufficient to give quantitatively accurate predictions of charge-voltage characteristics, even if the order of the model is increased. In this case, it will be necessary to develop a full

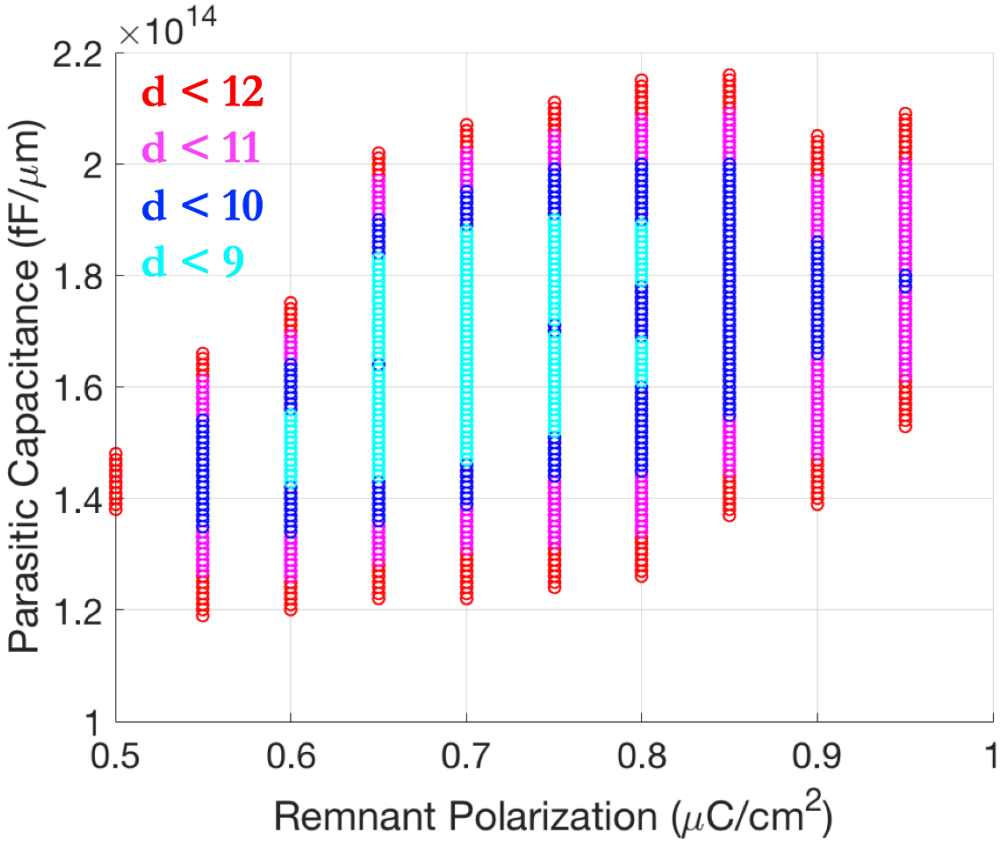

Figure 8.6: Distribution of solutions for the second phase of parameter optimization over P_r and C_f. d here is the error metric defined in 8.4.

Poisson's equation solver which can handle locally defined S-curve relationships within the ferroelectric material.

Beyond carrying out just quasistatic experiments, it will be useful for the model's capabilities to be extended to high frequencies, which will necessitate the inclusion of dynamics, including dissipation and inertia internal to the ferroelectric. Aside from adapting the model, it will be necessary to take characterize FETs at high frequencies over a range of DC bias points, which is a significant undertaking.

Chapter 9

Conclusions and Future Work

9.1 Conclusions

The key results in this work can be broadly categorized into two parts. In the first half, we focused on direct observation of negative capacitance in ferroelectric capacitors and on understanding the physics of their dynamics. In the second half, the focus shifted to a practical realization of negative capacitance FETs (NCFETs) with ferroelectric hafnium oxide integrated directly into the gate stack. This presents a different set of requirements, mainly ones of engineering performance rather than pure scientific inquiry, and requires more sophisticated techniques to extract the behavior of the ferroelectric material. We hope that the presented results form a useful framework for designing and characterizing negative capacitance devices. The main results are listed below.

1. *Direct Observation of Negative Capacitance.* Negative capacitance is observed in the switching transients of a ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ capacitor placed in series with an external resistor. When the ferroelectric is poled in a particular direction and a voltage pulse is applied to reverse the ferroelectric polarization, the transient voltage across the ferroelectric changes in opposition to the applied voltage, while the current through the circuit remains positive. This is by definition negative capacitance. The switching transients are integrated to give dynamic hysteresis loops, which represent the charge-voltage characteristics of a ferroelectric whose polarization switching is slowed down enough for the film to pass through the negative capacitance states.

2. *Dynamics of Negative Capacitance in Isolated Ferroelectrics.* The scaling of the negative capacitance transients of an isolated ferroelectric capacitor are examined. Comparison is made between a single-domain Landau-Devonshire model and the phenomenological Kolmogorov-Avrami-Ishibashi model of ferroelectric switching, and the shortcomings of both pictures are discussed. We then report on a full 3-D phase-field model for the ferroelectric, which manages to capture the physics described by both models.

3. *Intrinsic Speed Limitations of Negative Capacitance Transistors.* We construct a theoretical framework within which one can sensibly analyze the intrinsic speed limitations of negative capacitance transistors, in other words characterize the polarization response delay of the ferroelectric material itself. The Landau-Khalatnikov equation is generalized to include the inertia of the lattice ions. The parameters for this equation are extracted from the lowest resonance of the electromagnetic absorption of hafnium oxide. The ionic kinetic inductance allows for an unambiguous definition of the dissipation parameter. It is found that, for charge densities typical of FETs, for reasonable operating voltages, the time needed to switch a transistor is well under 1 ps, on the order of 270 fs.

4. *External Connection of a Ferroelectric Capacitor to Short-Channel FinFETs.* A coarse attempt at constructing an NCFET is made here which nevertheless reveals significant changes in the charge-voltage characteristics of a ferroelectric when it is connected in series with a FinFET. An epitaxial $BiFeO_3$ capacitor is connected through a wire to the gate terminal of a short-channel FinFET, called the internal gate. The drain current is used as a reference for the internal gate voltage, and the characteristics of the baseline FinFET are compared to that of the composite system, the NC-FinFET, which is observed to have a large hysteresis in the transfer characteristics, as well as subthreshold slopes as low as 8.5 mV/decade over 6-9 orders of magnitude of drain current. The ferroelectric charge-voltage characteristics are also found to have changed dramatically, with less than 0.25% of the remanent polarization seen in the isolated capacitor switching during NC-FinFET operation.

5. *Fabrication of Negative Capacitance FETs.* We describe the fabrication process for negative capacitance FETs on silicon-on-insulator substrates with doped ferroelectric hafnium oxide in the gate stack. After a brief overview of ferroelectricity in doped hafnium oxides, we describe the characterization and engineering of the ferroelectric material itself. Then we outline the replacement gate transistor process used for the first few rounds of fabrication. Finally, we describe the simplified gate-first process used in subsequent fabrication cycles.

6. *Characterization of Negative Capacitance FETs.* The characterization techniques and results of negative capacitance and reference transistors is recounted. Standard current-voltage and capacitance-voltage measurement techniques are described using a semiconductor device analyzer and the signatures of negative capacitance, reduced subthreshold slope below the Boltzmann limit, improved on-current, and reduced drain-induced barrier lowering are reported. The construction of a setup to directly probe the small-signal transconductance is described, as is the pulsed I-V method for obtaining transfer characteristics free from the effects of charge traps. Finally, characterization of the memory mode of operation of ferroelectric-gated FETs is reported.

7. *Simulation of Negative Capacitance FETs.* We describe efforts to extract the effective charge-voltage characteristics of a lumped model ferroelectric described by Landau-

Devonshire theory. First, a TCAD model is created that effectively reproduces the behavior of the reference FETs. This TCAD model supplies internal voltage and charge characteristics that are fed into the ferroelectric model, which is then tuned according to the experimental results of the NCFETs. Distribution of model solutions within the parameter space are shown and analyzed.

Collaborator Contributions

Asif Islam Khan was responsible for fabricating the ferroelectric PZT and BFO samples used in 2, 3, and 5. Samuel Smith wrote the code for the phase-field simulator in 3.6. Alexander J. Rosner was primarily responsible for obtaining the numerical solutions to the modified Landau-Khalatnikov equation derived in 4. Golnaz Karbasian and Ajay K. Yadav performed the materials characterization for the ferroelectric hafnium oxide used in 6. Sangwan Kim, Golnaz Karbasian, and Daewoong Kwon were all involved in developing the fabrication processes and device characterization.

9.2 Future Work

1. *Predictive Capacitance Matching in Negative Capacitance FETs.* The fabrication characterization simulation design loop outlined in the last three chapters of this work are still in a nascent stage. Given a certain device geometry, fabrication conditions, and ferroelectric composition and annealing, it is still an open question as to what the charge-voltage relationship of the ferroelectric will be. This is a critical problem for the realization of industrial-scale production of NCFETs. As usual, the protocol is to start with the simplest possible model and gradually add complexity until all the relevant physics have been captured.

2. *Poisson Solver with Negative Capacitance and Transport.* The inability to integrate a Landau-Devonshire model within a TCAD framework is a serious drawback, making spatially-varying ferroelectric models which require self-consistency cumbersome and time-consuming. A TCAD framework which allows for arbitrary definition of a charge-voltage relationship would be of great use in achieving predictive capacitance matching.

3. *Antiferroelectric Negative Capacitance.* Doped hafnium oxides exhibit a rich variety of material properties, among them antiferroelectricity [89], in which a ferroelectric phase can be induced with an electric field. These materials exhibit characteristic double hysteresis loops in polarization-electric field measurements. The hysteretic behavior of antiferroelectrics suggests that they should also possess negative capacitance states, although there has been almost no investigation into this possibility.

4. *Negative Capacitance FETs for Analog Circuits.* Most work on negative capacitance has focused on the application of negative capacitance to high-performance digital logic due to

lowering of subthreshold slope. Reduction or even reversal of drain-induced barrier lowering could have significant implications for analog circuits. The cancellation of short-channel effect through reverse DIBL presents an opportunity to design analog circuits using aggressively scaled and high-volume production CMOS platforms and thereby reach unprecedented performance at high frequency in silicon.

5. *Negative Capacitance for Broadband Antennas.* In conventional antenna circuits, an inductor is used to match the primarily capacitive impedance of the antenna structure. This places a trade-off between efficiency and bandwidth that could be overcome by the use of a negative capacitor instead of an inductor [90]. In particular, this could allow electrically small antennas to surpass the Chu-Harrington limit [91] [92]. Whether or not negative capacitance can be stabilized in this manner is an open question.

6. *Ferroelectric Memory for Neural Networks.* High information density hardware that can be integrated in close proximity to the processing unit could be of great utility in hardware for machine learning, specifically neural networks [70]. The partially switched states of a ferroelectric-gated FET could be a candidate for such a structure, particularly for inference engines which would not require a high program/erase endurance [93]. Controlling the switched state could require a feedback circuit due to variability, and a proper energy efficiency analysis for such a mode of operation is needed.

7. *Generalized Negative Compressibility.* A range of unstable states which arises from degeneracy in the ground states of thermodynamic systems is by no means specific to ferroelectrics. Indeed, ferroelastic inclusions in composite materials have been shown to enhance mechanical damping by orders of magnitude [94]. It is natural to explore the possibility of stabilized negative compressibility in conjugate variables besides polarization and electric field. For example, ferromagnets are also bi-stable systems [95], and in principle there could exist a range of negative magnetic susceptibility states. Inductive coupling as in a transformer could lead to a negative inductance, which could be used as a passive current amplifier.

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