Novel Processing Schemes for Material Systems on Amorphous and Flexible Substrates

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By

Kevin Chen

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Committee in charge:
Professor Ali Javey, Chair
Professor Ming Wu
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Abstract

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With the rise of the Internet of Things (IOT), demand for novel devices and sensors for a variety of applications has exploded, and as a result, there is a need for the development of new processing schemes and materials systems to accommodate the expanding needs of these applications. In particular,

Chapter 2 explores the growth of III-V semiconductors with quality approaching that of epitaxial thin films directly onto amorphous substrates using a new growth mode known as template liquid phase (TLP) crystal growth. The fundamental theory and limitations of TLP growth are explored and the toolboxes necessary for enabling this method to be widely used such as in-situ doping and growth of ternary III-V compounds are demonstrated. Proof of concept demonstrations of multilayer growth for 3D integration, transistors and phototransistors for electronic and optoelectronic integration, and transfer onto plastic for flexible applications are shown.

Chapter 3 extends the concept of using liquid metals to the field of flexible and deformable electronics. As an analogy to solid state electronics, where materials with varying electronic properties (metallic, semiconducting, insulating, etc) are connected together to form functional devices, the concept of "liquid state electronics" is introduced. Liquids, being able to conform to any shape, can enable electronic devices which can sustain extremely large amounts of deformation. By using microchannels to prevent intermixing, liquid-liquid heterojunctions composed of liquid metal (InGaSn) as the interconnect and ionic liquids as sensors are demonstrated.

Chapter 4 focuses on the usage of solution processed carbon nanotubes for enabling high-performing flexible electronic devices. First, a method for n-type doping of carbon nanotubes for CMOS applications is introduce using fixed charge in silicon nitride films. An extension of this doping method to other materials systems, in particular 2D WSe_2 is demonstrated as well. The usage of carbon nanotubes in printed electronics for enabling large scale, high throughput, flexible electronics manufacturing is explored, with >97% pixel yield in a 20×20 active matrix backplane array being achieved. A proof of concept demonstration of tactile pressure mapping using the printed nanotube active matrix backplane is shown as a potential application of such devices.

To my family and friends

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Chapter 1 Introduction

1.1 Need for novel processing and growth methods

As electronics become a larger part of our lives, in addition to continuous scaling of transistor size, there has arisen a need for devices with unique functionalities that cannot be achieved using traditional processing techniques and materials systems.

Silicon has been the backbone for electronics more or less since the beginning of the modern era. Indeed, the highest performance memory and logic units are all based upon silicon transistors. However, for certain applications such as high frequency electronics or optoelectronics, silicon is not as ideal as other materials systems such as III-V compound semiconductors. In this regards, it would be ideal to be able to combine these two materials systems onto the same chip to take advantage of the unique capabilities of each. However, in order to achieve such a goal, current technology relies on methods such as epitaxial transfer and wafer bonding, where the III-V material is grown on an epitaxial substrate and subsequently transferred onto silicon. For many applications as well as scalability purposes, it would be much more ideal to be able to directly grow the III-V materials selectively directly onto the device substrate. The challenge here is that due to lattice mismatch between silicon and nearly all III-V semiconductors, high quality epitaxial growth cannot be achieved. Thus, a growth method which can be done on an amorphous substrate which is not restricted by lattice matching is required.

In addition to III-V integration onto Si for high performance electronic and optoelectronic devices, there has been much interest in the field of flexible electronics for many applications such as wearable, robotic, and healthcare applications. For such applications, many processing challenges must be overcome, the key being how to be able to successfully fabricate, as well as scale, devices on a flexible substrate. Novel materials must also be developed for such substrates for both transistors for circuit and processing components as well as sensing layers for unique functionalities. Such materials must be able to operate under significant amounts of bending, as well as be able to be processed as low temperatures due to the lower thermal budgets of traditional flexible substrates. In addition, high performance must still be maintained so as to not limit the application space.

1.2 III-V semiconductor growth on amorphous substrates

III-V semiconductors are promising materials for a wide variety of electronic and optoelectronic applications due to their high electron mobilities as well as direct band gaps which can be tuned by changing the elemental composition of the material. Indeed, many state of the art devices ranging from high frequency electronics, solar cells, LEDs, and lasers all are based upon III-V compound semiconductors due to these reasons. However, III-V semiconductors are limited in their application space due to two main factors: cost and the need for an epitaxial substrate. While III-V semiconductors hold many advantages over silicon and other semiconducting materials systems, the raw materials themselves are inherently more expensive, making devices fabricated on III-V wafers to be typically limited to applications where cost is not a major issue. In this regards, the use of III-V thin films on arbitrary substrates has been proposed as an alternative solution. However, in order to grow the highest quality III-V materials, the growth

must be done using an epitaxial method such as metal-organic chemical-vapor-deposition (MOCVD) on a lattice-matched substrate, which typically is also a III-V material.

In order to remove this lattice-matched substrate requirement, one possible alternative growth method is template liquid phase (TLP) crystal growth. The method involves patterned deposition of the group III metal onto a substrate followed by encapsulation with silicon oxide. At growth temperatures where the group III is in the liquid state, it is exposed to a group V gas which diffuses into the liquid group III. Supersaturation of the group V in the group III leads to supersaturation and subsequent precipitation of a nucleus. As the nucleus continues to grow, it absorbs the surrounding group V in the liquid, decreasing the group V concentration nearby to be below the supersaturation level, which prevents the formation a second nucleus within this "depletion zone". As the depletion zone can be orders of magnitude larger than the film thickness, this allows for the growth of full area thin films with grain sizes orders of magnitude larger than the film thickness, or in the case of films patterned to be smaller than the depletion zone, crystals which have near single-crystalline quality.

Using this growth method, many III-V compounds can be grown by changing the group III metal or group V gas. Example compounds shown in this thesis include InP, GaP, InSb, and InAs. In addition, ternary III-V's can also be achieved by introducing multiple group V gases during the growth process, such as AsH_3 and PH_3 for the growth of InAsP. Using a similar method, by introducing a dopant gas such as GeH_4 for Ge doping or by utilizing a spin-on glass containing dopants such as Sn or Zn for the encapsulation layer enables in-situ doping capabilities for tuning the electrical properties as desired.

1.3 Liquid-state devices

In addition to being used for III-V growth, the low melting point of the group III metals also have enabled the development of electronic devices based on liquid-phase components. In particular, the eutectic alloy of indium and gallium is actually a liquid metal at room temperature, with the addition of a small amount of tin further decreasing the melting point down to -19 °C. Unlike mercury which is also a liquid metal at room temperature, InGa and InGaSn are non-toxic, making them ideal for wearable applications. Using these liquid metals, simple wearable devices based upon resistance change due to changes in geometrical deformation such as pressure and strain sensors have been achieved.

Furthermore, microfluidic technology can be utilized to create "heterojunctions" with different liquids with different electronic functionalities. By decreasing the microfluidic channel dimensions, the capillary pressure can be increased such that the liquid metals will not penetrate into smaller channels, allowing for subsequent injection of a second liquid component which is immiscible with the liquid metals to form a functional heterojunction. In this manner, the liquid metals can be utilized as electrical interconnects while the second liquid, such as an ionic liquid, can enable chemical which cannot normally be achieved using only a metal.

The usage of all-liquid electronic components enables devices to be able to sustain extreme amounts of strain and deformation, only being limited by the substrate material for creating the microchannels. Typical materials such as polydimethylsiloxane (PDMS) can be stretched by over 100%, allowing liquid-state electronic devices to be comfortably worn.

1.4 Solution deposited carbon nanotube electronics

While liquid-state electronics can enable extreme deformation for simple sensor applications, more complex flexible sensor systems must still be built based upon solid-state materials systems. The key challenge for many flexible electronics devices is that typically, polymers are used as the substrate to enable the flexibility. As polymers typically have relatively low thermal stability, many processing technologies which involve high temperatures must be excluded. In this regards, solution processed carbon nanotubes (CNTs) provide a promising solution. Being deposited at room temperature via a solution dropcast process, CNT based thin film transistors (TFTs) can still achieve mobilities greater than 50 cm^2/V s.

One major application that can be enabled by these high performance CNT-TFTs is large area flexible stimuli mapping. By using the CNT-TFTs to create an active matrix backplane array, various sensors can be integrated onto a flexible polyimide substrate for multiplexed sensing and mapping. Example sensors include sputtered InP for temperature, amorphous silicon for light, and a laminated pressure sensitive rubber sheet for tactile pressure.

In addition to their use as TFTs for creating an active matrix backplane, certain applications may also require simple circuit processing. In this regards, doping of normally p-type CNT-TFTs is necessary. One potentially promising doping process is chemical field effect doping via positive fixed charges in thin films such as silicon nitride. These positive fixed charges are able to invert the CNT channel to achieve n-type conduction, enabling CMOS operation via selective doping. This chemical field effect doping mechanism can be widely applied to a variety of materials systems and in addition to CNTs, doping of two-dimensional materials such as WSe_2 have also been demonstrated.

The room temperature deposition of the CNTs also enable them to be compatible with high throughput production processes such as roll-to-roll printing. Such printing processes such as gravure printing can achieve speeds on the order of meters per second at very low cost to enable applications which require extremely large format electronics as well as disposable electronic applications.

Chapter 2 Templated Liquid Phase Crystal Growth

2.1 Introduction to III-V growth on non-lattice-matched substrates

III-V semiconductors have many positive traits that make them ideal for use in electronic and optoelectronic properties such as high electron mobilities and direct band gaps. However, the cost of III-V wafers makes them unattractive for many products. In addition, rather than using III-V wafers, it is preferable to have a thin III-V device layer upon a different substrate for applications such as monolithic integration with silicon or for flexible electronic systems. In recent years, with the advancement of the silicon on insulator (SOI) platform, a similar concept for other semiconductors known as semiconductor X on insulator (XOI) or any other arbitrary substrate (XOY) has emerged.

In the field of photovoltaics, III-V semiconductors have been shown to have superior performance over silicon due to their direct band gap. However, due to the significantly increased cost of III-V wafers and epitaxial substrates over silicon, III-V wafer based solar cells are not commercially viable except for rare applications such as space exploration where performance is valued over cost per unit power. However, high quality single crystalline thin film III-V solar cells on amorphous substrates significantly reduces the amount of III-V materials used, making them more attractive for large scale use. Similarly, in the field of optoelectronic devices, III-V's benefit greatly from their direct band gaps which span a large range of energies. For many applications monolithic integration of III-V optoelectronic devices is desired to take advantage of the advanced silicon computing platform combined with the superior optical properties of III-V optoelectronics. Besides optoelectronic device applications, III-V semiconductors are also very desirable for digital and analog circuits. Due to their high electron mobilities, III-V semiconductors offer superior transistor performance over silicon. In addition, direct growth of III-V semiconductors on amorphous substrates would enable an easy pathway towards three dimensional integration of devices.

One major method of growth III-V thin films is via vapor-solid epitaxial growth methods such as molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD). For homoepitaxy or pseudomorphic epitaxy, where the same or a closely lattice matched material is grown, virtually defect free III-V heterostructures can be achieved with thicknesses on the order of a few nanometers and atomically sharp interfaces. This precision enables the growth of complicated electronic and optoelectronic device structures such as vertical cavity surface emitting lasers (VCSELs) where even nanometer scale imperfections can significantly degrade device performance. However, in metamorphic epitaxy, where two epitaxial layers are not lattice matched, dislocations and other defects will form beyond very thin layers in order to reduce stress, leading to much lower quality films. In order to overcome this constraint, thick buffer layers may be used to gradually reduce the stress in order to grow high quality device layers. Typically, for III-V growth, the buffer layers will be compositionally graded with each subsequent buffer layer bringing the film closer to the lattice constant of the desired device layer. While the use of buffer layers can be useful in helping obtain high quality III-V layers on top of lattice-mismatched substrates, direct growth of high quality crystals on amorphous substrates is much more challenging. This arises from the fact that unlike a single crystalline epitaxial

substrate, where the substrate provides the crystal orientation and structure for growth, the nucleation of crystals on amorphous substrates is typically random. As such, different nuclei on an amorphous substrate will have different nucleation orientations, leading to a polycrystalline material as the various nuclei grow and coalesce. Furthermore, due to more or less isotropic growth rates in all directions, growth on amorphous substrates will typically result in thin films with grain sizes that are on the order of the film thickness.

One growth method which has enabled direct growth of single crystalline III-V's onto amorphous substrates is vapor-liquid-solid growth (VLS). In VLS, the group III and V precursors are introduced in the vapor phase and supersaturate a metal catalyst such gold, resulting in the precipitation of a III-V nuclei. As growth proceeds after nucleation, continued supersaturation and precipitation out of the catalyst nanoparticle leads to nanowire (NW) growth with the catalyst droplet being pushed upwards. As the nucleation of the NWs occur at the liquid-solid interface of the catalyst droplets, the catalyst nanoparticle effectively provides the epitaxial "seed" for NW crystal growth, enabling growth to be conducted on an amorphous substrate. However, without a true epitaxial substrate, the NWs will typically grow in all directions without alignment. In addition, growth of other geometries outside of NWs cannot be done using traditional VLS growth.

In recent years, a new growth mode known as thin-film vapor-liquid-solid (TF-VLS) growth has demonstrated such potential. Compared to traditional VLS growth, where both group III and group V precursors are introduced in the gas phase, the group III element is first pre-deposited onto the growth substrate and confined with a thin evaporated SiO_x capping layer. As the group III elements typically have a very low melting point, these deposited films transform into the liquid phase during growth where the group V element is introduced in the gas phase and diffuses through the SiO_x cap into the liquid group III film. Similar to VLS growth, once the group III becomes supersaturated with the group V element, nucleation and precipitation of a III-V crystal will occur. These nuclei will continue to grow the full film has been fully converted. The key advantage in the TF-VLS growth mode as compared to traditional vapor-solid growth on metal foils is that due to the diffusion of the group V in the liquid melt towards the nuclei, a surrounding volume of the melt around each nuclei will become depleted of the group V element. This "depletion zone" effectively prevents the formation of another nucleus within a certain radius of each nucleus, leading to the growth of grains that are significantly larger than the film thickness. Compared to VS growth of III-V's where grain sizes are typically on the order of the film thickness, TF-VLS grown InP has been shown to have grains on the order of hundreds of μm for film thicknesses of just a few μm. As will be shown here, by modifying the TF-VLS growth scheme for growth of patterned thin films which are smaller than the depletion zone rather than full area thin films, single crystalline III-V semiconductors can be grown directly onto amorphous substrates.

2.2 Templated Liquid Phase Growth of InP

The following subchapter has been previously published in a similar format in:
K. Chen, R. Kapadia, *et al*. Direct growth of single crystalline III-V semiconductors on amorphous substrates. *Nature Communications*, **7**, 10502, (2016).

Due to their high electron mobilities and direct band gaps, III-V compound semiconductors are ideal for many electronic and optoelectronic applications such as high performance transistors[1–3], photovoltaics[4,5], LEDs[6] and photodetectors[7]. The development of epitaxial growth techniques such as molecular beam epitaxy[8], metal-organic chemical vapor deposition[9], and pulsed laser deposition[10] have enabled the growth of single crystalline III-V thin films with excellent performance for device applications. In order to obtain such high quality single crystalline thin films, the growth must be done on a closely lattice-matched substrate[11]. The growth of single crystals onto amorphous substrates would further enable new applications, such as providing a simplified pathway for heterogeneous integration of III-V devices onto application specific substrates. However, deterministic synthesis of single-crystalline semiconductors on amorphous substrates presents a fundamental challenge in the field of materials science—one that arises from the thermodynamics and kinetics of nucleation and crystal growth. Specifically, the slow kinetics governing coalescence of two grains into a single grain dictates that any single crystalline structure on an amorphous substrate must be grown from a single nucleus. Thus, for single crystalline growth, the first nucleus that forms must grow to fill the desired volume before another nucleus is formed. Within most growth approaches, the relative nucleation and growth rates are difficult to control, and the maximum grain size attainable is often on the order of the material thickness, resulting in nanocrystalline structures for nanoscale thickness materials[12].

Due to the tremendous technology-driven need for single crystalline semiconductors on amorphous substrates, a number of synthesis techniques have been explored in recent years. These approaches include (i) epitaxial growth of thin films on single-crystalline substrates followed by selective layer transfer to a desired substrate[2,4], (ii) vapor-liquid-solid (VLS)[13–17] vapor-solid[18,19], or aerosol-based[20] nanowire growth, For GaN in particular, the usage of "pre-orienting" layers to conduct local hetero-epitaxy has also been demonstrated[21,22]. While such approaches have resulted in broadening the scope and functionality of various electronic materials with unique properties, direct growth of single-crystalline semiconductors with *user-defined* geometries and dimensions on amorphous substrates has yet to be demonstrated. Such an approach would offer major advantages in terms of compatibility with traditional device processing technology, scalability and processing cost. In addition, it would provide a direct pathway to three dimensional integration of electronic materials and devices with appreciable levels of complexity.

Here, we introduce templated liquid phase (TLP) crystal growth (Fig. 1a) as a synthetic approach for growth of high-performance, nano- and micro-scale single-crystalline compound semiconductors with user-defined geometries on arbitrary substrates. Indium phosphide is chosen as a model III-V material system due to its importance in a wide variety of fields, from high-speed electronics to lasers and photovoltaics[5,7,13,23]. Thermally grown SiO_2 and glass are selected as examples of amorphous materials on which TLP crystal growth can be performed.

2.2.1 TLP Growth and Crystal Quality

For TLP growth of InP, indium metal is first lithographically patterned onto a Si/SiO_2 or glass substrate with a thin (1-10 nm) MoO_x nucleation layer, and subsequently encapsulated by

evaporated SiO_x (Supplementary Fig. S1). Growth is carried out in a low pressure furnace at 500-535 °C in the presence of phosphine (PH_3) and H_2. At the growth temperature, In is transformed into the liquid phase, but remains mechanically confined by the SiO_x template. Phosphorous diffuses through the SiO_x cap, and supersaturates the liquid In, precipitating out in the form of an InP nucleus. The key feature of this growth mode is that a phosphorous depletion zone forms around each growing nucleus, preventing further nucleation. Previously, we have shown that for continuous In thin films, this depletion zone can be on the order of hundreds of μm, leading to ultra-large grain sizes[24,25]. Here, we show that through pre-patterning the indium in mechanically confined templates such that the phosphorous depletion zone from the first nucleus occupies the entire template, *single crystalline* InP growth in user-defined geometries can be achieved.

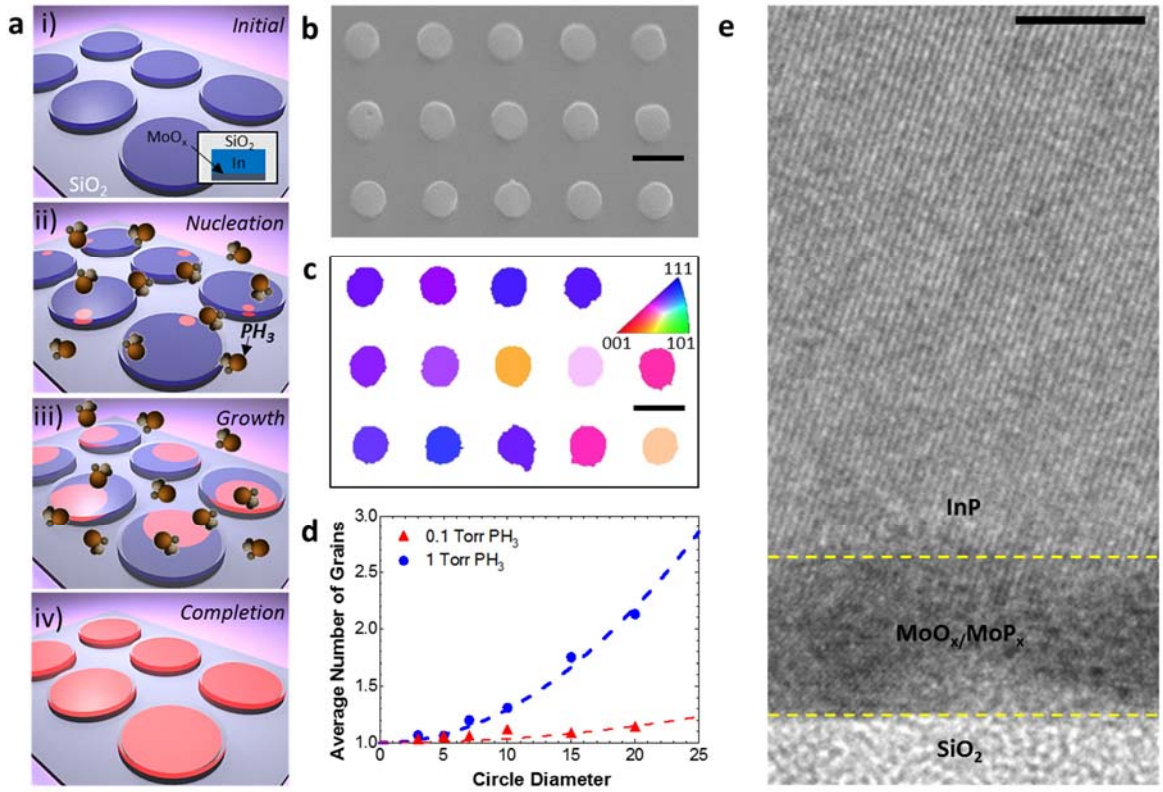


Figure 1: Growth mechanism of single crystalline InP. (a) Schematic of the process flow for TLP crystal growth. (b) SEM images of an array of 7 μm InP circles and (c) their corresponding EBSD maps. The scales bars are 10 μm. (d) The average number of grains per circle, measured via EBSD vs. the circle diameter, showing a quadratic dependence. (e) TEM cross sectional image of a portion of a patterned InP thin film showing the well defined InP lattice on top of a MoO_x/MoP_x layer on amorphous SiO_2. The scale bar is 5 nm.

Scanning electron microscope (SEM) images of the InP crystal arrays shaped into circles, rings, and squares grown via TLP crystal growth are shown in Figure 1b and Supplementary Figure S2. Critically, the original In template geometry is maintained after growth, allowing for deterministic shape control of InP crystals. The stoichiometry of the films is confirmed by electron dispersive spectroscopy (EDS) to be 1:1 In:P. X-ray diffraction (XRD) spectroscopy on an array of InP circles (Supplementary Fig. S3) displays only peaks corresponding to zincblende InP, indicating that all of the In has converted to InP. The crystallinity of the InP patterns with lateral dimensions of ~5-

7 μm is confirmed via electron backscatter diffraction (EBSD) mapping, showing that excluding twinning, each individual pattern is a single crystal but with different crystal orientations (Figure 1c, Supplementary Fig. S2, Methods, Supplementary Note 1). In addition, from the orientation distribution obtained from EBSD, it can be seen that there is a preferential texturing of the growth in the [1 0 n] direction , where n ranges between 1 and 2 (Supplementary Fig. S4).

To study the effect of growth conditions and InP feature size on the number of grains, InP circles with diameters varying from 3-20 μm were patterned using TLP crystal growth at two different PH_3 partial pressures. From Figure 1d and Supplementary Figure S5, it can be seen that the number of grains per circle increases according to a quadratic relation with the circle diameter, *d*, which can be fit by the equation:

$$N_{\text{grains}} = 1 + \beta d^2 \quad (1)$$

N_{grains} is the average number of grains per circle and β is a proportionality factor that takes into account growth parameters such as P flux, the geometry associated with nucleation, and the resulting average nucleation rate (Supplementary Fig. S6, Supplementary Note 2). As expected from our model, there is also a strong dependence of the number of grains on the PH_3 partial pressure. As the PH_3 partial pressure is lowered, the P flux into the liquid decreases, resulting in a reduced nucleation rate and larger P depletion zones (Supplementary Note 2). This is reflected in a drop in β from 3×10^{-3} to 4×10^{-4} as the PH_3 partial pressure is reduced from 1 to 0.1 Torr, allowing the average number of grains per feature to be maintained at near unity even for diameters as large as 20 μm.

Transmission electron microscopy (TEM) was used to examine the crystallinity of the InP patterns. From the cross-sectional TEM image of an InP sample shown in Figure 1e, it can be seen that a crystalline InP lattice sits on top of the amorphous SiO_2 substrate with a thin MoO_x/MoP_x nucleation layer in between, clearly showing the non-epitaxial nature of TLP crystal growth.

To demonstrate the versatility of the TLP crystal growth technique, the world's smallest version of the *Lorem Ipsum* placeholder text is written in crystalline InP lettering with a stroke width of 150 nm (Figure 2a). In addition, a single-crystalline Berkeley "*Cal*" logo with dimensions of 80×60 μm is shown in Figure 2b with its structural, compositional, and optoelectronic properties characterized via EBSD, EDS mapping, and photoluminescence (PL) imaging (Figure 2c, Supplementary Fig. S7), respectively. While letters are used for demonstration purposes, the geometric degrees of freedom available to grow single crystalline materials with TLP crystal growth are of great significance for the fabrication of practical electronic and photonic devices.

One major advantage of TLP crystal growth is ease of scalability. Unlike traditional III-V growth where both group III and V elements are introduced in the vapor phase, only the group V element is in the vapor phase, and the geometry is fixed by the template. This allows for simple reactor designs which can be easily scaled up to large scales. Furthermore, as growth only occurs when both group III and group V elements are present, the templates essentially provide a self-limiting growth mechanism, preventing unwanted thickness or compositional variation across a wafer. As a demonstration, Figure 2d-2f shows an optical image of arrays of InP circles outlined by InP bars, grown across a full 4" Si/SiO_2 wafer using a simple cold-wall furnace.

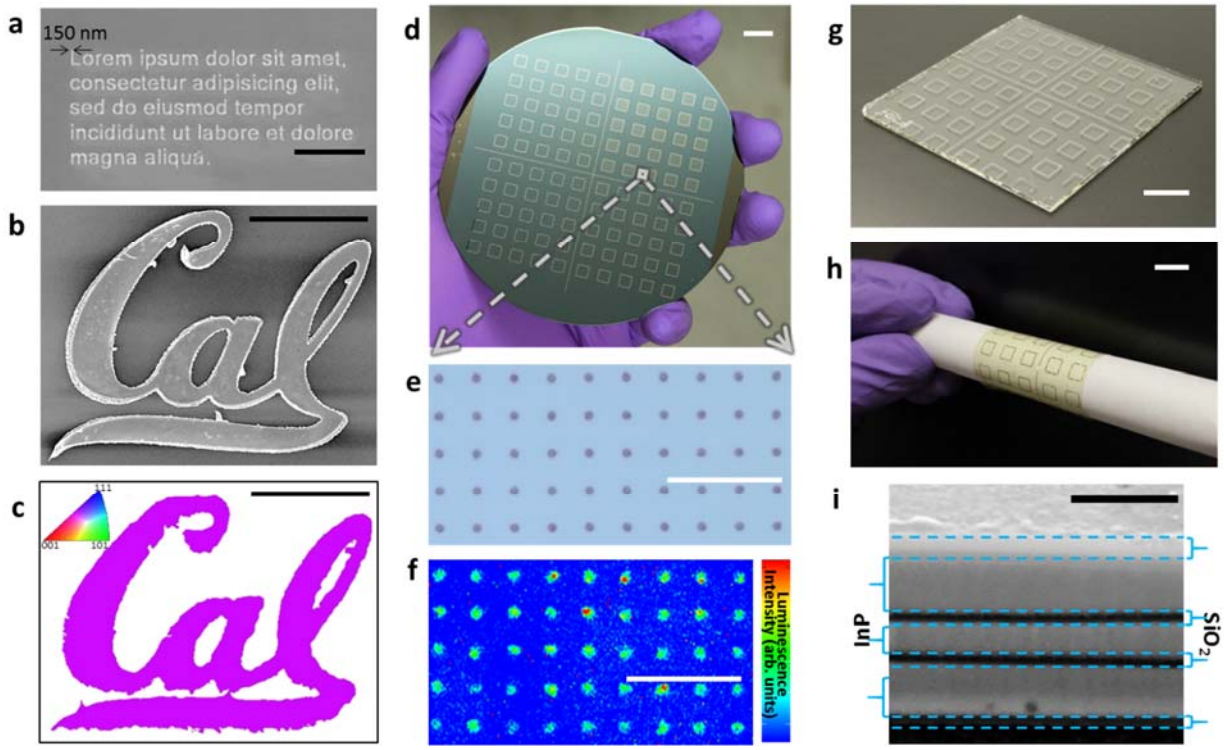


Figure 2: Scalability and growth on "novel" substrates. (a) SEM image of InP text with a linewidth of 150 nm. The scale bar is 3 µm. (b) An SEM image and corresponding (c) EBSD map of a single crystalline UC Berkeley "*Cal*" logo grown via TLP crystal growth. The scale bars are 30 µm. (d) An optical image of a 4" Si/SiO_2 wafer patterned with arrays of 3 µm diameter InP dots located within each square InP box. The scale bar is 1 cm. (e) Zoomed in optical image of an array of dots on the wafer and (f) their corresponding PL image. The scale bars are 50 µm. (g) An optical image of patterned InP dots grown on a ~6×6 cm borosilicate glass slide. The scale bar is 1 cm. (h) An optical image of the patterned InP dot array transferred onto a PET substrate wrapped around a glass tube with a diameter of 1.5 cm. The scale bar is 1 cm. (i) Cross sectional SEM image of three layers of InP grown with 30 nm of SiO_x between each layer. The scale bar is 500 nm.

The relatively low temperature required for TLP crystal growth also allows for a broad range of substrates upon which single crystalline III-V's can be grown. As an example, InP circles were directly written onto a borosilicate glass slide (Figure 2g) and their optical quality was verified via PL imaging (Supplementary Fig. S8). In addition, the grown InP can be fully transferred onto plastic substrates for applications where a flexible substrate is desired. As an example, Figure 2h and Supplementary Figure S9, show an optical image and the corresponding PL image, respectively, of the InP circle arrays transferred onto a polyethylene terephthalate (PET) substrate using polyamic acid[26].

A unique feature of the TLP crystal growth process is that complex 3D architectures can be achieved, beyond the limits of traditional processes. For instance, multilayers of InP single-crystals separated by amorphous SiO_x layers can be grown in one cycle by starting with substrates consisting of multilayer In/SiO_x layers, as demonstrated in the cross-sectional SEM image in Figure 2i. This can have broad implications for future design of monolithic 3D electronics.

2.2.2 In Situ Doping

A critical component of semiconductor growth is the ability to tune the optical and electrical properties; in particular, the doping concentration. To explore this capability, GeH_4 gas was introduced into the growth chamber during growth to achieve controlled in-situ *n*-type Ge doping of InP. Figure 3a shows the normalized PL spectra of InP single crystals grown under different partial pressures of GeH_4. Significant blue-shifting of the PL peak versus a lightly doped reference wafer (Supplementary Fig. S10) as the GeH_4 partial pressure increases is observed due to the Burstein-Moss effect, indicating increased electron concentrations[27–29]. The electron concentrations, approximated from the PL peak energies (Methods), are plotted vs. the GeH_4 partial pressure in Figure 3b indicating that TLP grown InP can be doped up to a degenerate level of ~1.3×10^{19} cm^{-3}, near the upper limit of electron doping in InP[30]. From the PL spectra, the Urbach tail parameter is also extracted and plotted vs. the carrier concentration level in Figure 3c[31]. The Urbach tail parameter is an important figure of merit regarding the band edge sharpness arising from crystal defects, thermal vibrations and charged impurities[32,33]. As can be seen, the Urbach tails of our non-epitaxial TLP grown samples are similar to the values reported in literature for InP single crystal wafers at various respective levels of doping[34,35].

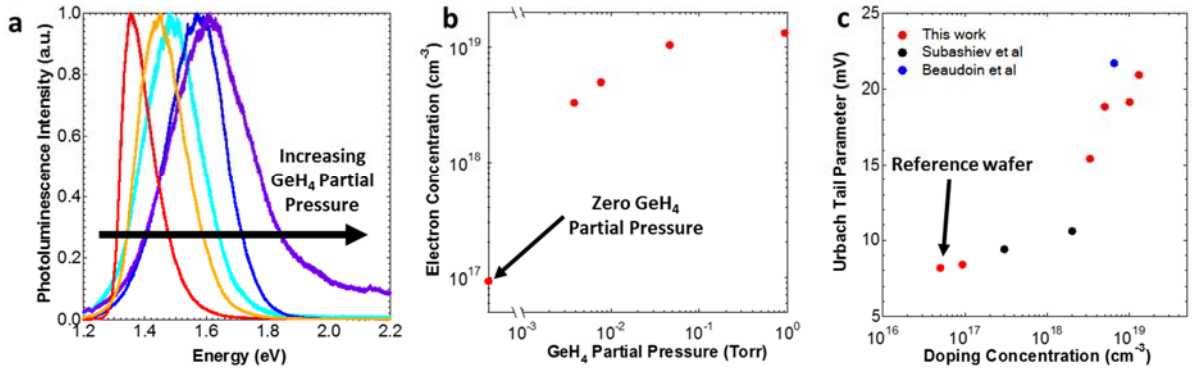


Figure 3: In-Situ Doping. (a) PL spectra of five InP samples grown with GeH_4 pressures of 0, 3.9, 7.7, 46, and 900 mTorr of GeH_4. As the GeH_4 partial pressure is increased, the peak of the PL spectra blue-shifts, signifying higher electron concentrations. (b) A plot of the electron concentration, approximated from the peak position of the PL spectra using the Burstein-Moss effect, as a function of the GeH_4 partial pressure. (c) The Urbach tail parameter is plotted vs. the approximated doping level showing that the crystal quality is on par with that of single crystalline wafers/films at different levels of doping.

2.2.3 Electronic Characterization

The electronic quality and practical utility of TLP InP in the shape of microwires (μWires) were explored by fabricating long-channel Schottky n-type metal-oxide-semiconductor field effect transistors (MOSFETs) with top gates (Figure 4a-c). The transfer and output characteristics of an InP transistor on a Si/SiO_2 substrate with a gate length of 3 μm and body thickness of ~125 nm are shown in Figures 4d and e, respectively. The device exhibits an ON-current of 120 μA μm^{-1} at $V_{GS} = V_{DS} = 2$ V with an ON/OFF current ratio of $>10^5$ and peak extrinsic transconductance of 100 S μm^{-1}, which is excellent for a long channel device. An effective electron mobility of $\mu = 675$ cm^2 $V^{-1}s^{-1}$ is extracted from device simulations (Methods), which compares favorably with unpassivated InP nanowire/microwire MOSFETs in literature[9], illustrating the excellent electronic

quality of the InP grown here. In addition, top-gated InP photo-MOSFETs were also fabricated on Si/SiO_2 substrates using the device structure above except that a transparent indium tin oxide (ITO) gate electrode is used with a channel length of L_G = 20 μm. The device electrical characteristics were measured under dark and under steady state illumination from a bandpass filtered white light source with an optical intensity of 15.6 mW cm^{-2}. The device exhibits a strong photoresponse (Figure 4f) with a peak responsivity of ~700 A W^{-1} at V_{GS} = 3.4 V (Figure 4g). Furthermore, the specific detectivity (D^*) of this device displays a maximum of ~8.4×10^{11} Jones at room temperature, comparable to state-of-the-art single crystalline epitaxial InGaAs detectors[14].

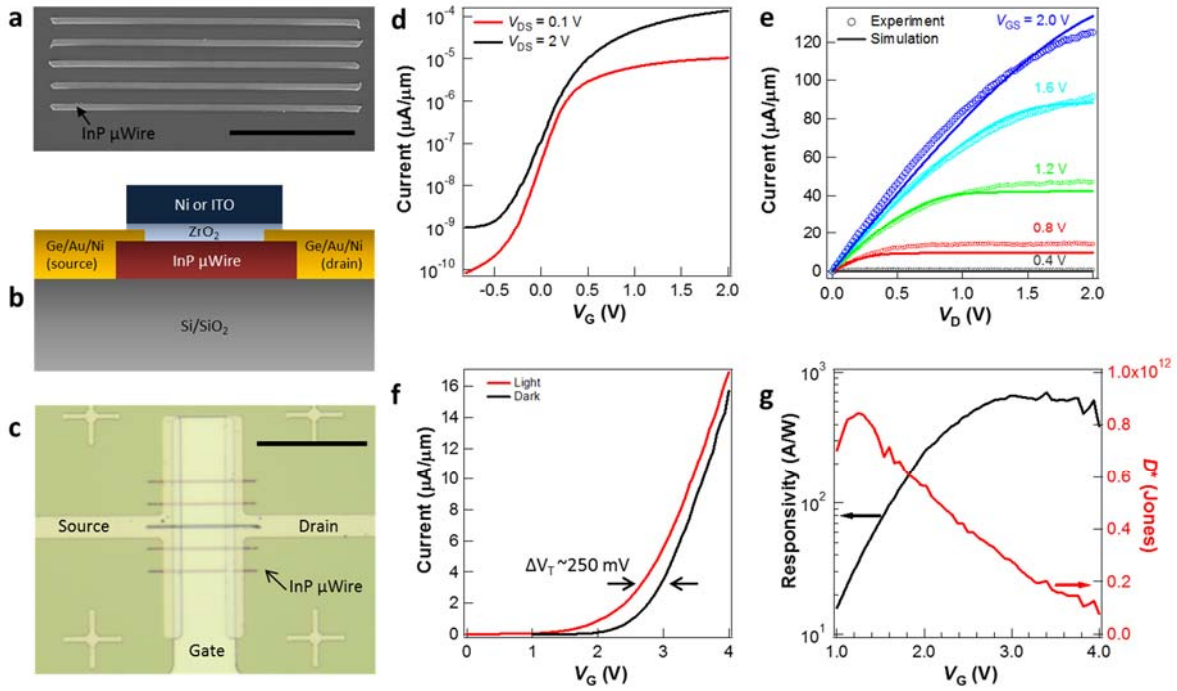


Figure 4: Electronic Characterization. (a) An SEM image of typical 1 μm wide InP μWires used for MOSFET fabrication. The scale bar is 20 μm. (b) A cross sectional schematic of the InP MOSFETs along with the (c) an optical image of a MOSFET with 5 μwires as the channel. The scale bar is 50 μm. (d) The transfer I_{DS}-V_{GS} and (e) output I_{DS}-V_{DS} curves of an InP transistor with a single μWire as the channel and a 3 μm gate length. (f) The transfer characteristics of a photo-MOSFET in dark and exposed to 15.6 mW cm^{-2} of light, showing a large threshold voltage shift of ~250 mV. (g) The responsivity and detectivity of the photo-MOSFET are plotted vs. the gate voltage bias.

2.2.4 Discussion:

In conclusion, we have demonstrated a technique that enables direct "writing" of optoelectronic-quality single-crystalline III-V semiconductors on amorphous substrates. The elimination of the requirement for lattice matched substrates as well as the improved scalability of this growth mode enables ubiquitous integration of III-V semiconductors for a wide range of applications on user-defined substrates. While InP was used as a model growth system in this work, the TLP crystal growth method is one that, from a thermodynamic and kinetic point of view, is expected to be applicable to other technologically important III-V's. As an example, proof of concept

demonstrations using the TLP process to grow GaP and InSb are shown in Supplementary Figure S11. In addition, single crystals grown via the TLP growth process may potentially be utilized as a virtual substrate in epitaxial growth processes, allowing for the realization of high-quality semiconductor heterostructures grown directly onto amorphous substrates. Future work on control of crystal orientation of individual patterns may further extend the tunability of the TLP growth mode, for instance, by making nucleation of a specific orientation thermodynamically favorable through surface engineering of the nucleation layer or via the introduction of geometric constraints using principles from graphoepitaxy[12].

2.2.5 Experimental and Theoretical Details:

2.2.5.1 Patterning and growth of InP.

First, a clean Si wafer with a 50 nm thick thermal oxide was lithographically patterned with the desired InP shape (Supplementary Fig. S1a). For the glass sample in Figure 2g, a borosilicate glass slide was patterned instead. A thin 1-10 nm thick MoO_x layer was evaporated (Supplementary Fig. S1b) followed by evaporation of In of the desired thickness and a 10-100 nm thick SiO_x layer (Supplementary Fig. S1c). As SiO_2 has a high surface energy for nucleation[24], the MoO_x layer helps to promote nucleation of the InP[25]. To obtain a smooth In film, the evaporation of the In and SiO_x bilayer was done with the substrate chuck cooled to <150 K using liquid N_2. The whole MoO_x/In/SiO_x stack was then lifted off (Supplementary Fig. S1d). After liftoff, angled evaporation was utilized to coat the exposed side regions of the In with SiO_x with thicknesses ranging from 4-50 nm (Supplementary Fig. S1e, f). During the growth, the SiO_x template confines the liquid In so that the resulting InP crystal has the same shape as that of the original In pattern. Growth of the InP patterns for EBSD crystal analysis and transistors were carried out in a hot-wall chemical vapor deposition (CVD) tube furnace. 10% PH_3 in H_2 was used as the phosphorous source and was further diluted to the desired dilution. Growth of the 4" wafer, sample on glass, and doping dependent studies were done in a cold-wall CVD system. 10% GeH_4 in H_2 was used as the Ge dopant source. The samples were grown for 10-20 minutes at pressures of 100-300 Torr (partial PH_3 pressure of 0.1-10 Torr) and growth temperatures ranging between 500-535 °C.

2.2.5.2 EBSD characterization.

EBSD characterization was carried out in an FEI Quanta scanning electron microscope with an Oxford Instruments EBSD detector. Analysis of the maps were done by the Oxford Aztec and Tango software programs. Orientation maps were generated and plotted using the inverse pole figure color scheme. Twin boundary removal was done by ignoring the <111> 60° rotational boundaries within the crystals and plotting the surface orientation of each grain.

2.2.5.3 Photoluminescence spectra and imaging.

PL spectra were taken by a HORIBA LabRAM HR800 tool with a 532 nm excitation wavelength. For PL imaging, a red LED was used as the excitation light source and images were taken by an Andor silicon CCD camera through an optical microscope with a GaAs wafer used to filter out the irradiation wavelengths.

2.2.5.4 Electron Concentration Extraction.

The electron concentration, n, can be approximated using the equation[27]:

$$n = 10^{19}\left(\frac{\Delta E}{16.9}\frac{m}{m_0}\right)^{3/2} \quad (2)$$

where ΔE is the shift of the PL peak energy from an undoped reference (1.34 eV taken from a 5×10^{16} cm^{-3} doped reference wafer, Supplementary Figure S10) and m/m_0 is the ratio of the effective electron mass of InP to the free electron mass.

2.2.5.5 Urbach tail fitting.

The absorption at the band edge, is related to the photoluminescence spectra by the van Rossbroeck-Schockley equation by[27]

$$\alpha(v) \propto \frac{P(v)\left(e^{hv/kT}-1\right)}{v^2} \propto e^{\frac{hv-E_g}{E_0}} \quad (3)$$

where $P(v)$ is the PL intensity as a function of frequency v, h is Planck's constant, and kT is the thermal energy (25.6 mV at room temperature). E_0, the slope at the absorption band edge, is the Urbach tail parameter, which describes the sharpness at the band edge and is a good indicator of crystal and optoelectronic quality.

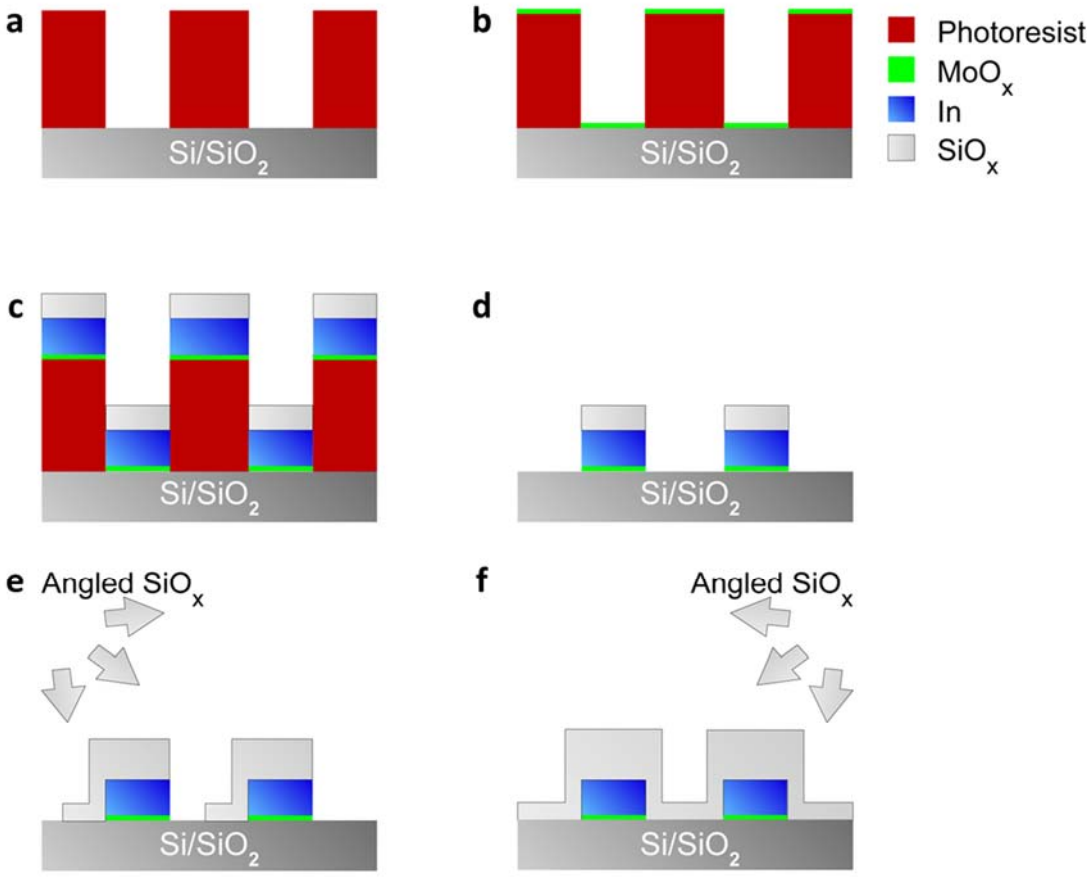
2.2.5.6 Device fabrication.

InP microwires with dimensions of 1 μm×50 μm×125 nm were grown using TLP crystal growth as described above. Photolithography was used to lithographically define the source/drain contacts followed by evaporation of 3/10/40 nm of Ge/Au/Ni and liftoff. The source/drain contacts were subsequently annealed at 375 °C for 5 minutes to alloy the Ge with InP in the contact regions to improve contact resistance. 10 nm of ZrO_2 was then deposited via atomic layer deposition at a temperature of 200 °C. Finally, photolithography was used once again to define the gate electrode. For the MOSFETs, 40 nm of Ni was evaporated as the top gate metal while for the photo-MOSFETs, 30 nm of ITO was deposited via sputtering instead to allow optical access to the channel.

2.2.5.7 Sentaurus simulations.

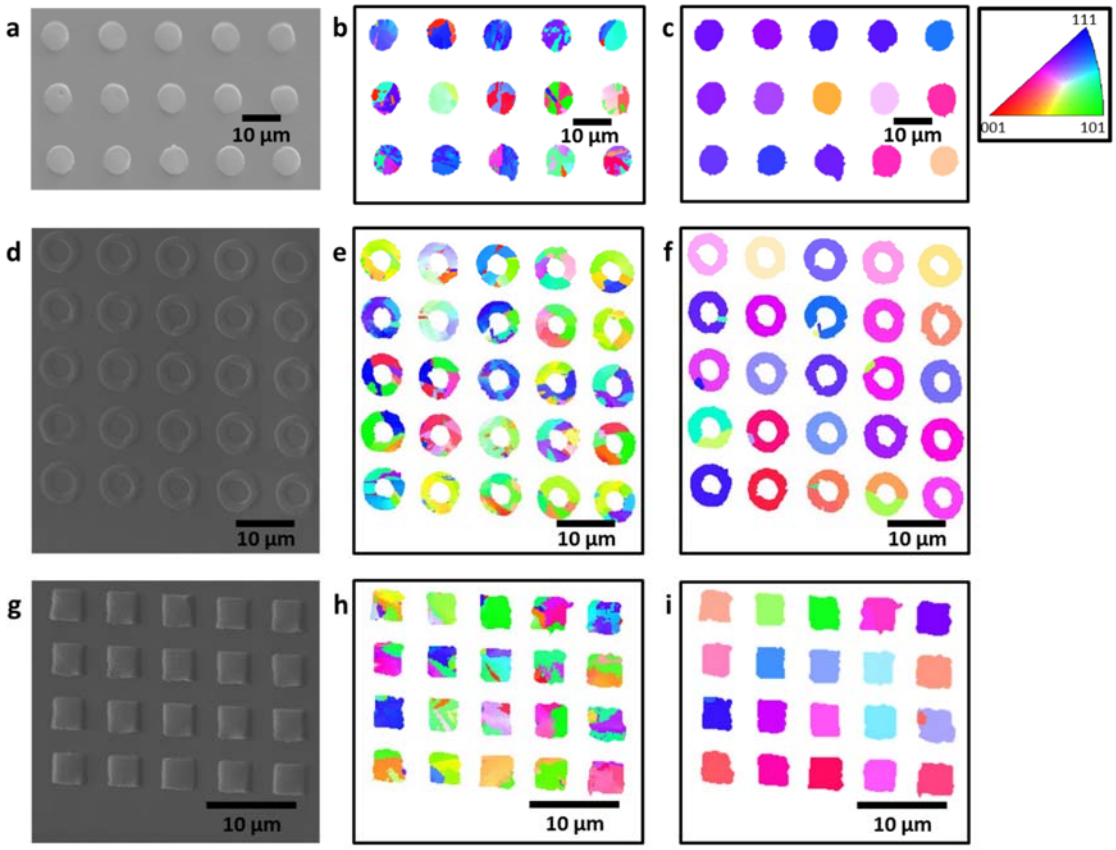
Detailed semi-classical drift-diffusion simulations were carried out utilizing the Sentaurus Device simulator to accurately model the device performance. The parameter extraction was carried out by first matching the subthreshold region (-0.2 V<V_{GS}<0.15 V) utilizing InP/ZrO_2 surface interface traps and gate work function as the fitting parameters and performing a least squares error fit, enabling accurate simulation of the mobile charge vs. gate voltage. The mobility and series resistance of the device were extracted by minimizing the least squares error for all the I_{DS}-V_{DS} curves (0 V<V_{DS}< 2 V) for V_{GS} = 0.4, 0.8, 1.2, 1.6, and 2 V simultaneously.

2.2.5.8 Sample preparation for TLP crystal growth.



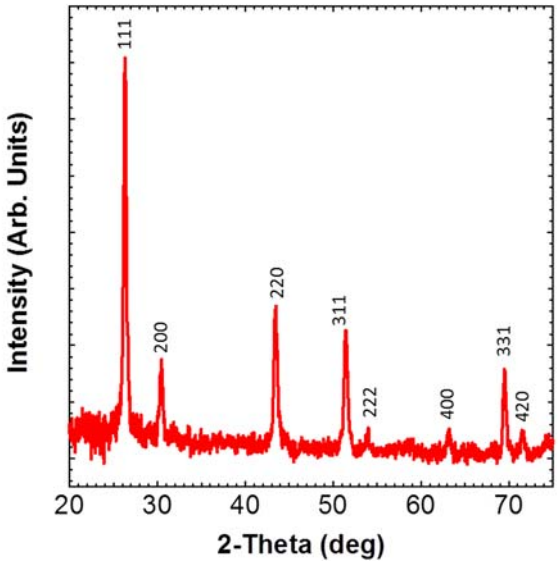
Supplementary Figure S1: (a) The sample is first patterned via photolithography and (b) a thin 1-10 nm thick MoO_x layer is evaporated. (c) Then, a bilayer of In and SiO_x is evaporated while the substrate chuck is cooled below 150° C using liquid N_2. (d) After evaporation, the whole stack is lifted off and (e, f) SiO_x is evaporated from 2-3 angles in order to fully encapsulate the In.

2.2.5.9 EBSD map of various grown shapes.



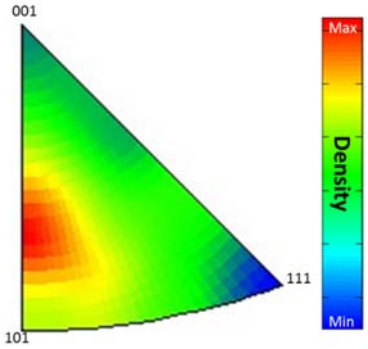
Supplementary Figure S2: (a) SEM image of patterned InP circles along with corresponding EBSD maps (b) before and (c) after removal of the <111> 60° twin boundaries. (d) SEM image of patterned InP rings along with corresponding EBSD maps (e) before and (f) after removal of the <111> 60° twin boundaries. It can be seen that some of the rings consist of two grains. (g) SEM image of patterned InP squares along with corresponding EBSD maps (h) before and (i) after removal of the <111> 60° twin boundaries. One of the squares consists of two grains, while the rest are all single crystals. The samples were grown at a partial PH_3 pressure of 10 Torr.

2.2.5.10 X-ray diffraction characterization.



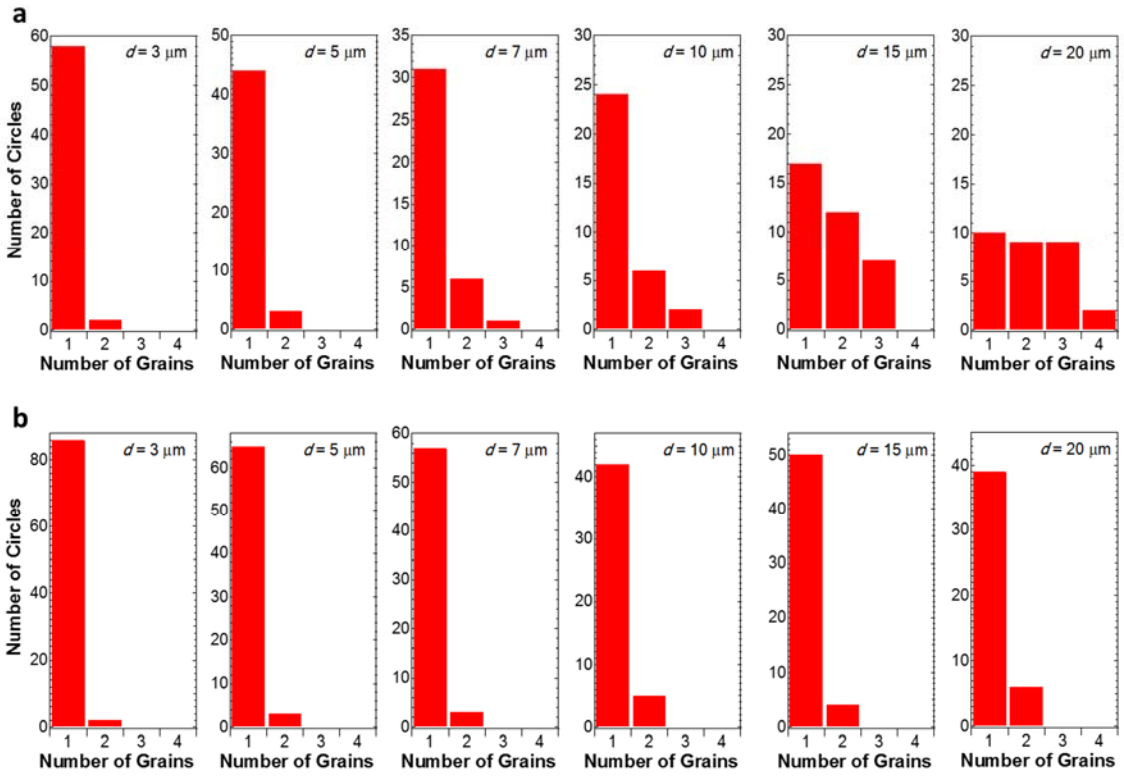
Supplementary Figure S3: XRD diffractogram of an array of InP circles displaying only peaks from the zincblende phase, indicating complete conversion of In into InP, within the resolution limit of XRD.

2.2.5.11 Orientation Distribution Inverse Pole Map.



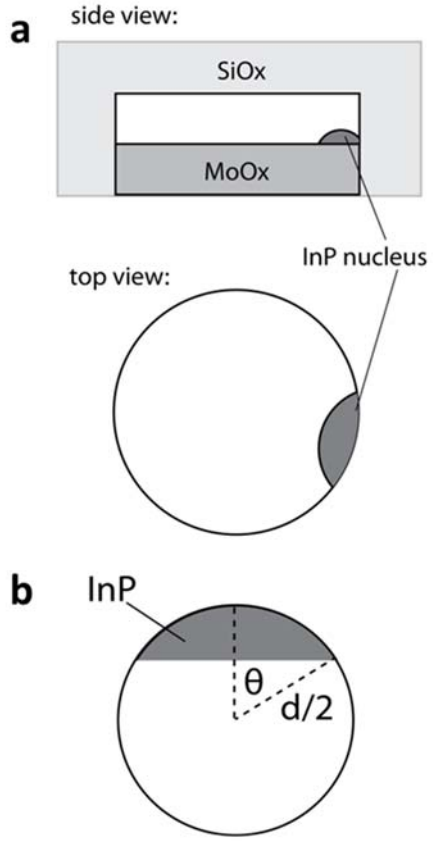
Supplementary Figure S4: The orientation distribution in the normal direction of an array of InP circles obtained from EBSD indicate a slight preferential orientation in the [1 0 n] direction, with n ranging between 1 and 2.

2.2.5.12 Histograms of Circle Grains.



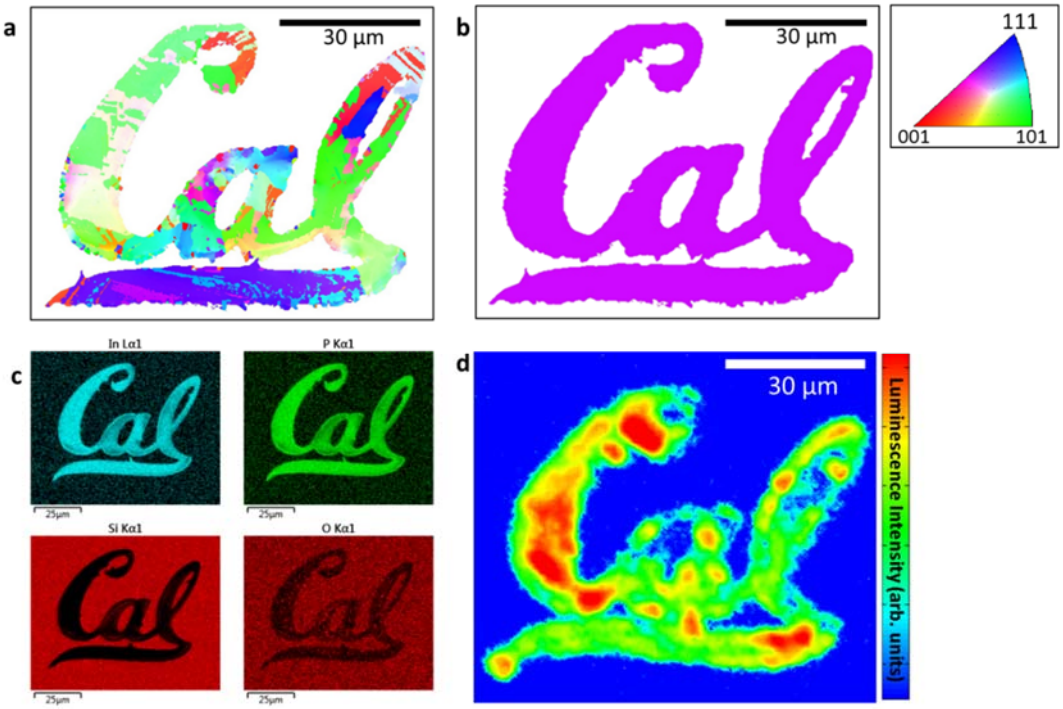
Supplementary Figure S5: (a,b) The statistical distribution of the number of circles vs. number of grains plotted as histograms for PH_3 partial pressures of (a) 1 Torr and (b) 0.1 Torr for circles of diameter 3 µm, 5 µm, 7 µm, 10 µm, 15 µm, and 20 µm.

2.2.5.13 Nucleation model



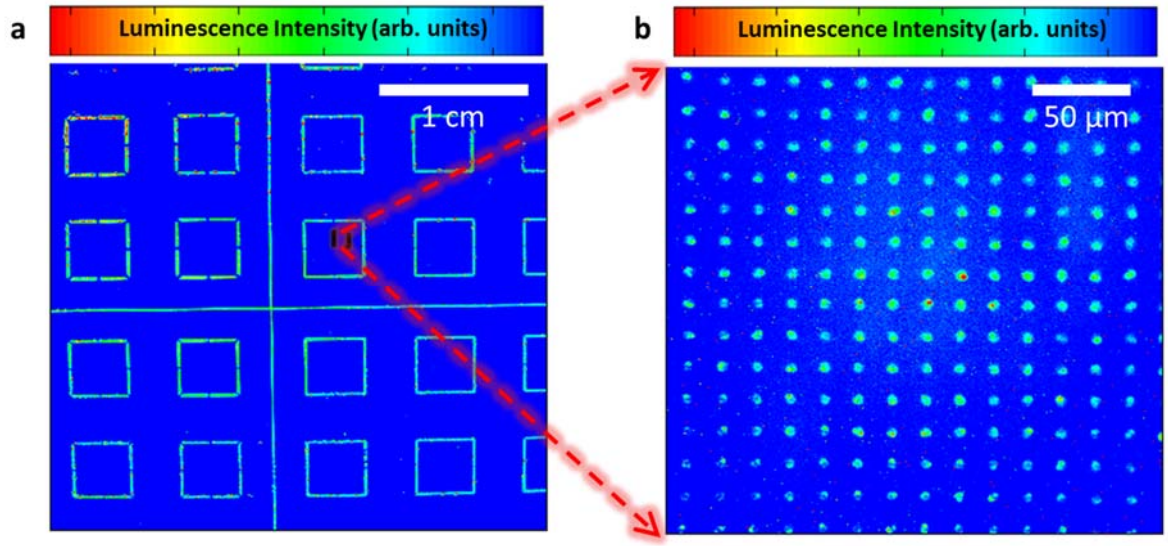
Supplementary Figure S6: (a) Nucleation along the edges of the circles. (b) The geometry assumed in computing the results in Eqn. (6) of Supplementary Note2. The growing nucleus is assumed to block nucleation sites as it advances. This, in turn, will reduce the net nucleation rate within the circle (all other factors being equal). Equation (6) of Supplementary Note 2 is derived by noting that the total area of the nucleus increases approximately linearly with time, and this enables one to compute $\theta(t)$, and thereby the edge length available for nucleation of additional grains. d is the diameter of the circle.

2.2.5.14 Characterization of Single Crystal "*Cal*"



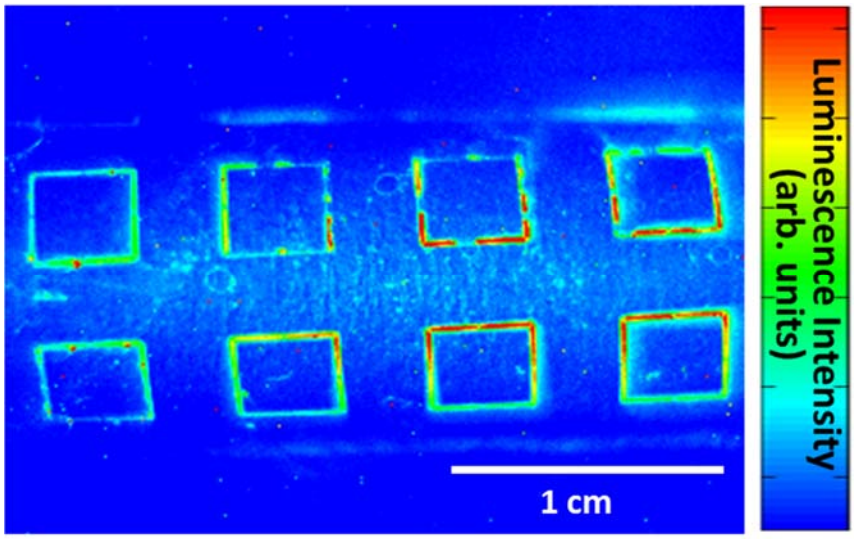
Supplementary Figure S7: (a) EBSD map of the "*Cal*" shown in Figure 2b before and (b) after twin boundary removal. (c) The EDS elemental map of the region containing the single crystal "*Cal*" for In, P, O, and Si. The intensity of each color (versus black background) indicates the amount of that element mapped within the region. The extracted InP stoichiometry shows an In to P ratio of 1:1. (d) The PL image of the single crystalline InP "*Cal*" showing that it is optically active.

2.2.5.15 PL imaging of patterned InP grown on borosilicate glass.



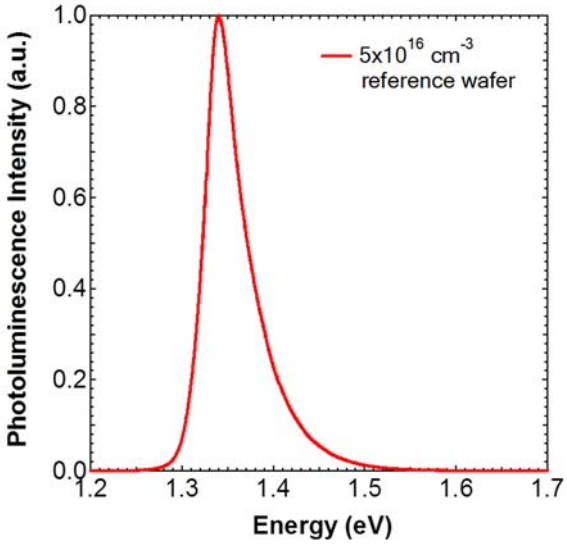
Supplementary Figure S8: (a) The PL image of a ~4x4 cm patterned area of 3 µm InP circles within large InP square frames grown on borosilicate glass along with (b) a zoomed in PL intensity map of the actual circle arrays.

2.2.5.16 PL imaging of InP circle arrays transferred onto plastic



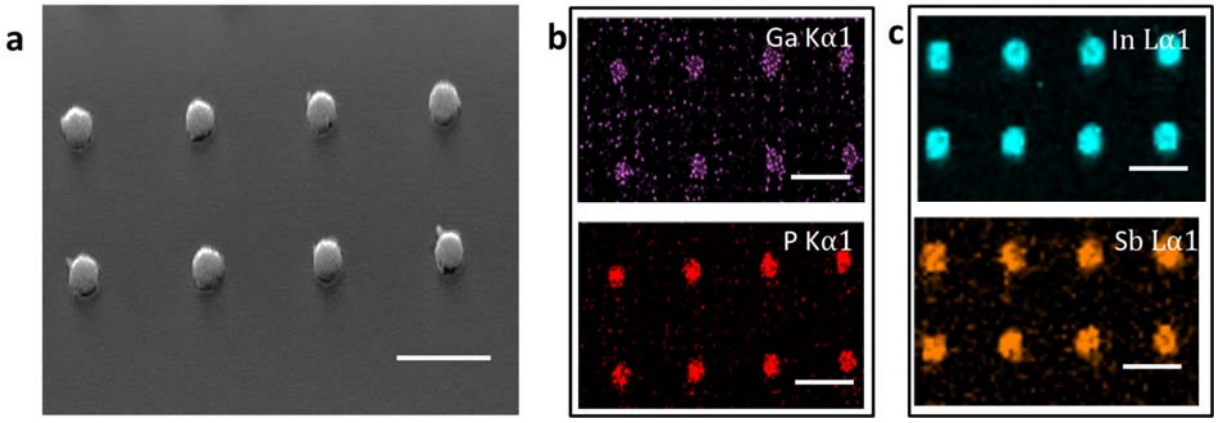
Supplementary Figure S9: PL imaging of InP circle arrays transferred onto plastic. As the polyimide used in the transfer process does slightly fluoresce in the infrared regime, a weak outline of the test tube upon which the plastic substrate is wrapped around is also seen in the PL image.

2.2.5.17 PL spectra of an InP reference wafer.



Supplementary Figure S10: PL spectra of an InP reference wafer. PL spectra of a single crystal InP reference wafer with a doping level of 5×10^{16} cm^{-3}

2.2.5.18 TLP Growth of GaP and InSb.



Supplementary Figure S11: a) SEM image of patterned GaP circles and b) the corresponding EDS maps of the region for Ga and P. c) EDS maps of In and Sb of a similarly patterned region of InSb. Scale bars for all images are 5 μm.

2.2.5.19 Supplementary Note 1: Twinning within InP

From EBSD measurements results shown in Supplementary Figure S2 and Supplementary Figure S7, it can be seen that the crystals have <111>60° rotational twin boundaries, which is commonly seen in the growth of III-V materials[36] and in particular InP due to its low stacking fault energy. Previously, nanowires grown via the vapor-liquid-solid (VLS) growth mode often exhibit stacking fault[37-39] due to this reason. Upon using the Tango analysis software to disregard twin boundaries in the EBSD analysis, it is revealed that the individual features grown in this work do show up as single crystals, indicating that all features do indeed grow out from a single nucleus.

Despite the existence of the twin boundaries, it can be seen from Urbach tail measurements, as shown in Figure 3c, that the Urbach tail parameter is on par with a single crystalline reference wafer, as well as reported Urbach tail parameters in literature for single crystalline InP[34,35]. In addition, the electronic and optoelectronic characterization in Figure 4 of devices made from the single crystals grown via the TLP crystal growth method are still of extremely high quality, on par with commercial single crystalline InGaAs photodetectors[40].

2.2.5.20 Supplementary Note 2: Nucleation model for number of grains per circle vs. size

Consider the nucleation of the InP solid phase within In liquid supersaturated with P. The nucleation process is a stochastic one, in which the nucleation rate, Γ, is time dependent, $\Gamma = \Gamma(t)$. Within this model, the probability that *k* grains nucleate between the time $t = 0$ and $t = \tau$ is given by:

$$P(k,\tau) = \frac{e^{-N(\tau)}}{k!} N(\tau)^k, \text{with } N(\tau) = \int_0^\tau dt\Gamma(t) \tag{1}$$

We define the time $t = 0$ to be that time at which the first grain nucleates in the circle and t_{growth} to be the time at which the disk is completely transformed.

The distribution governing the number of grains nucleated after the first is given by $P(k, t_{\text{growth}})$, and the final average number of grains within the circle, N_{grains}, is given by:

$$\begin{aligned} N_{\text{grains}} &= 1 + \langle k \rangle \\ &= 1 + N(t_{\text{growth}}) \end{aligned} \tag{2}$$

Consider now the case that nucleation takes place at a constant rate per available nucleation site in the "corners" of the circles (See Supplementary Fig. S6). Under these circumstances, the nucleation rate can be written as

$$\Gamma(t) = \alpha(t)\gamma_0 \pi d \tag{3}$$

where $\alpha(t)$, a dimensionless quantity, is the fraction of the edge length available for nucleation at time t, πd is the total edge length available for nucleation at time $t = 0$, and γ_0 is the average nucleation rate per unit of edge length throughout the growth process.

Further progress can be made if one assumes a growth geometry for the initial nucleus, and that the time to form the first nucleus is small in comparison to the total growth time.

In the experiments, the SiO_x cap on the top of the In circles is designed to be much thicker than that on the sides (Supplementary Figure S1). As such, it can be assumed that the P is only entering through the sides of the In circles, so that the number of P atoms entering the liquid, per unit time, $\dot{n}_{\mathrm{P}}$ is given by:

$$\dot{n}_{\mathrm{P}} = J_{\mathrm{P}} \pi h d \tag{4}$$

where h is the original thickness of the In circle, d the original diameter of the circle, and J_{P} the average flux rate of the P through the SiO_x during the growth. Given this average flux rate, the time for the first nucleus to completely transform the circle is:

$$t_{\mathrm{growth}} \approx \frac{d}{4 J_{\mathrm{P}} \Omega_{\mathrm{In}}}, \tag{5}$$

Using the geometry shown in Supplementary Figure S6, one finds:

$$\begin{aligned} \langle k \rangle &= N\left(t_{\mathrm{growth}}\right) \\ &= \frac{\pi}{8} \frac{\gamma_0}{J_{\mathrm{P}} \Omega_{\mathrm{In}}} d^2, and \\ N_{\mathrm{grains}} &= 1 + \frac{\pi}{8} \frac{\gamma_0}{J_{\mathrm{P}} \Omega_{\mathrm{In}}} \end{aligned} \tag{6}$$

So the average number of grains in the circles should increase with diameter according to $N_{\mathrm{grains}} = 1 + \beta d^2$, with β depending on the imposed growth conditions.

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2.3 TLP Growth of Ternary III-V's

The following subchapter will submitted for publication in a peer reviewed journal.

In the previous section, the growth of binary III-V semiconductors such as InP, GaP, and InSb was demonstrated via TLP growth onto amorphous substrates such as SiO_2. However, one major advantage of III-V semiconductors is the tunability of their band gaps and electronic properties via different stoichiometries of ternary and quaternary alloys[1]. Here we show that the TLP crystal growth process can be used not only for binary III-V compounds, but also ternary compounds. As an example materials system, we demonstrate the growth of ternary $InAs_xP_{1-x}$ with varying stoichiometries from x=0 to x=1. InAsP is a direct bandgap semiconductor with band gaps ranging from 0.36-1.35 eV, making it a good candidate for communications at the 1.55 µm wavelength as well as other infrared applications. In addition, it has a high electron mobility ranging from ~2000-20,000 $cm^2/V{\cdot}s$, which is good for high performance transistors as well[2,3]. However, it has historically not been used in commercial applications due to a lack of a lattice matched substrate for which it can be grown on[1,4]. By using TLP, we are able to grow high quality InAsP thin films directly on amorphous substrates, providing a pathway for the integration of InAsP without concern for lattice matching.

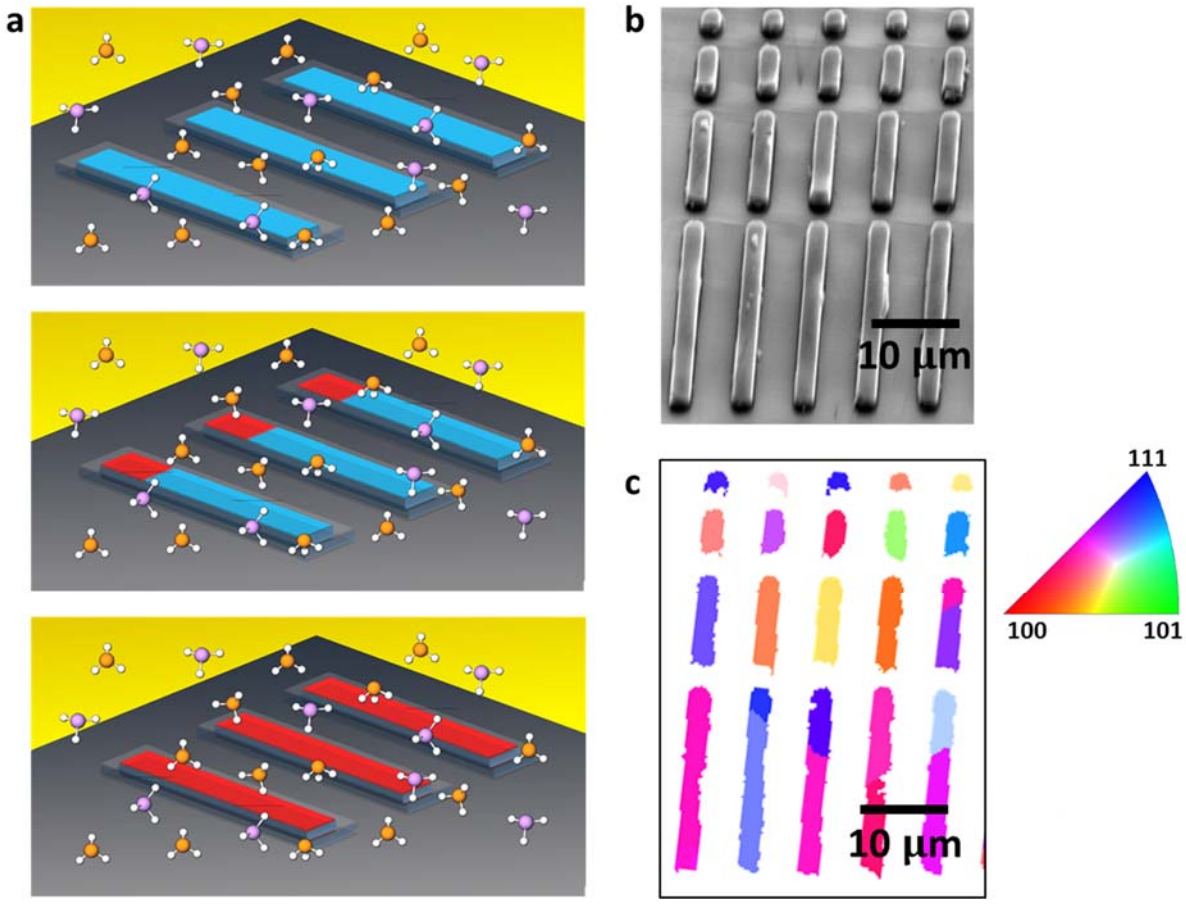


Figure 1: TLP growth overview. a) Schematic of the TLP growth process. b) SEM image of a TLP grown InAsP MW array. c) EBSD map of the corresponding array in (b).

Figure 1a shows a schematic of the TLP growth process. Metal indium is first deposited and patterned via photolithography onto a Si/SiO_2 wafer with a 2-8 nm thick MoO_x nucleation layer. Angled evaporation is used to fully encapsulate the patterned indium with SiO_x. To grow the ternary compound, the sample is placed into a growth chamber and heated up in the presence of arsine (AsH_3) and phosphine (PH_3) gas as the As and P sources. Growth is carried at out at a temperature of 565 °C, where the As and P will diffuse through the SiO_x cap and supersaturate, leading to nucleation and growth of patterned InAsP crystals. More details of the sample preparation and growth can be found in the Methods section. Figure 1b shows a scanning electron microscope image of InAsP microwires grown via the TLP crystal growth process. As can be seen from the corresponding electron backscatter diffraction (EBSD) map in Figure 1c, if twin boundaries are excluded, the crystals are essentially "single crystals", indicating that each individual microwire grew out from a single nucleus, similar to that of TLP grown binary crystals (EBSD map before averaging the orientation of twin boundaries shown in Supplementary Figure S1).

2.3.1 Stoichiometry Control

In order to tune the stoichiometry of the InAsP, different flow ratios of AsH_3 and PH_3 can be used. In our growth system, 2% AsH_3 and 1.6% PH_3 diluted in H_2 gas are used. Note that all flow rates and ratios referenced in the rest of this work will be referring to these diluted concentrations rather than pure AsH_3 and PH_3 concentrations. Electron dispersive spectroscopy (EDS) was used to extract the stoichiometries of microwire samples grown with AsH_3:PH_3 ratios of 0.005, 0.01, 0.025, 0.1, and 0.3.

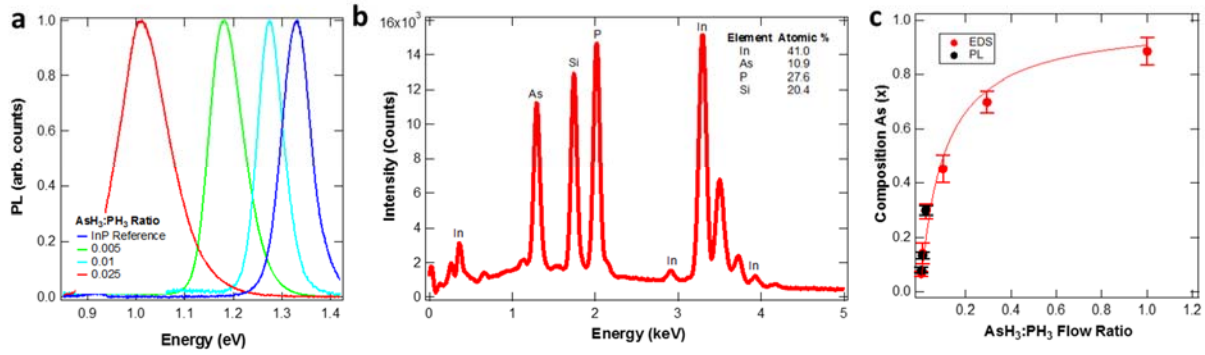


Figure 2: Composition tunability. a) PL spectra taken from InAsP patterned films grown with AsH_3:PH_3 ratios of 0.005, 0.01, and 0.025 as well as from a reference InP wafer. b) Representative EDS spectra from a sample grown with an AsH_3:PH_3 ratio of 0.05. c) As composition (x) versus AsH_3:PH_3 flow ratio extracted via PL and EDS measurements.

An example EDS spectra taken from a sample grown with an AsH_3:PH_3 flow ratio of 0.05 is shown in Figure 2b, with a stoichiometry of $InAs_{0.28}P_{0.62}$. The Si signal measured via the EDS comes from the Si wafer substrate underneath. In addition, to EDS measurements, photoluminescence measurements were used to verify the InAsP compositions. Figure 2a shows the photoluminescence (PL) spectra taken from three different microwire samples grown with AsH_3:PH_3 ratios of 0.005, 0.01, and 0.025. The PL spectrum taken from an InP wafer is also included for reference. The PL peak positions of these three InAsP samples are 1.28, 1.18, and 1.01 eV.

The stoichiometries can be extracted from these peak positions by assuming that the band gap at room temperature can be approximated by the equation[5]:

$$E_G = 0.356 + 0.675x + 0.32x^2\ eV \quad \text{(eq. 1)}$$

where x is the As composition in the film. Using this approximation, these peak positions correspond to $InAs_xP_{1-x}$ films with x = 0.05, 0.14, and 0.28, respectively.

Figure 2c plots the As percentage (with respect to As+P) versus the AsH_3:PH_3 flow ratio during growth, measured via EDS as well as photoluminescence (PL) measurements ranging from AsH_3:PH_3 ratios of 0.005-1. The compositions extracted from PL and EDS are very similar, within 1-3% As of each other, which is within error of the two extraction methods, indicating that the extracted stoichiometries are accurate. As can be seen from these measurements, TLP can be utilized to grow InAsP thin films with any arbitrary As and P composition by simply changing the relative flow ratios of the group V precursor gases during grown, demonstrating the tunability of the TLP growth process for ternary InAsP growth. The actual ratio of As:P in the resulting films is approximately an order of magnitude larger that the AsH_3:PH_3 flow ratios, most likely due to the much lower cracking temperature of AsH_3 versus PH_3 as well as a difference in diffusion rates of As and P through the SiO_x cap. The trend for the stoichiometry versus the flow ratios of AsH_3 and PH_3 show a non-linear relationship, which is consistent with ternary epitaxial growth techniques. In the vapor-liquid phase transition, As and P have been discovered to have different sticking coefficients, which result in different rates at which As and P atoms impinging on the liquid In surface actually become incorporated into the liquid melt. This change can be approximately modeled by[4]:

$$x = \frac{aR}{1+aR} \quad \text{(eq. 2)}$$

Where *a* is a fitting factor taking into account the different sticking ratios of As and P and *R* is the AsH_3:PH_3 ratio. Fig. 2c displays a fit of the EDS data based upon this model, with *a*=11.7. It should be noted that the fit does not describe the data very well at higher As concentrations. One possible explanation for this is that in addition to a stoichiometry change arising from the vapor-liquid transition, there is a similar change in the liquid-solid transition, which is not taken into account in the simple model above. In addition, the existence of the SiO_x encapsulation layer may also change the expected behavior as As and P will have different diffusion coefficients through the SiO_x.

2.3.2 Stoichiometry Variation

Due to the stoichiometry change in the liquid-solid transformation as mentioned above, one area of concern is the stoichiometry variation of the InAsP within a given crystal as the difference in stoichiometry will also lead to a change in the stoichiometry of the liquid solution itself. This problem is one that is also present in liquid phase epitaxy (LPE) of ternaries[6]. In LPE, one way this problem is accounted for is by having a sufficiently thick solid solution such that the overall stoichiometry of the source solution does not change significantly throughout the growth[7]. In TLP growth however, the whole liquid In pattern is consumed and transformed during growth. In order to check the compositional uniformity of the growth in the TLP growth InAsP crystals, an EDS line scan was done across the length of a microwire as shown in Figure 3a. As can be seen, the P and As counts along the length of the wire stay approximately constant until near the end of the wire when the As composition drastically increases. This is also verified via PL measurements

taken along a second micro-wire from center to edge, as shown in Figure 3b. Until the end of the wire, the peak position stays approximately constant at 1.25 eV until the end of the wire, when the peak position drops to 1.2 eV. This excellent compositional uniformity across most of the microwire is most likely due to the fact that unlike LPE growth, the liquid melt is constantly being replenished from the gas phase so that the composition of the liquid melt does not change drastically over time. Only until the very end of the growth, near the end of the microwire, does the composition begin to change more significantly as the supply of As and P from the vapor phase is unable to balance out the rate of change in stoichiometry in the melt. While this may be problematic in certain applications, due to the ability to grow any arbitrary geometry, it can be overcome by designing the growth patterns and devices such that the ends of the growth where the stoichiometry shifts significantly are not part of any active device or that they are part of the metal contact areas.

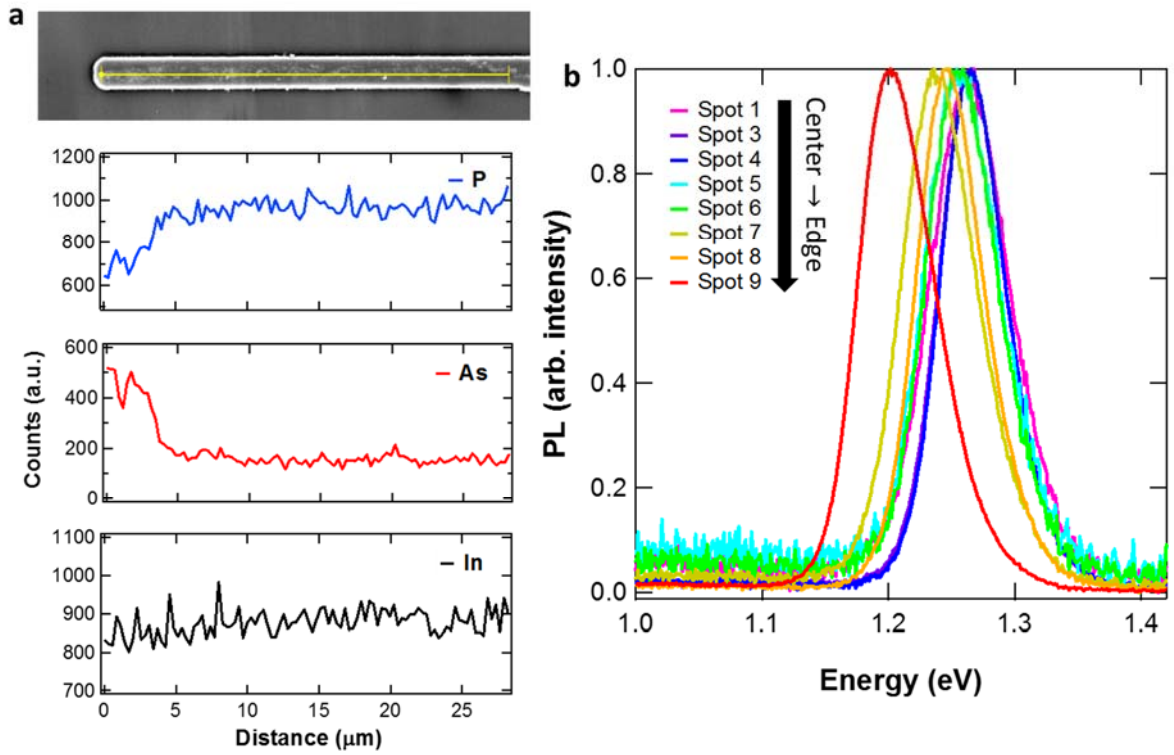


Figure 3: Composition Variation. a) SEM image of an InAsP MW grown with an AsH_3:PH_3 flow ratio of 0.005 along with the EDS counts for P, As, and In along the length of the MW. b) PL spectra taken along a different InAsP MW grown using the same conditions.

2.3.3 Full Area Thin Film Growth

In addition to growing patterned thin films, full area III-V thin film ternary compounds can also be grown on amorphous substrates using a similar growth mode known as thin-film vapor-liquid-solid (TF-VLS) growth. In TF-VLS, similar to TLP, the group III metal is first blanket deposited onto the substrate and then encapsulated on top with evaporated SiO_x. As a proof of concept demonstration, InAsP is once again used as a model material system. For TF-VLS growth, 1.5 μm of In was blanket evaporated onto a sputtered Mo substrate on Si and encapsulated with 80 nm of SiO_x, evaporated in-situ with the In. Since a much thicker In film is used with full area In coverage

rather than patterned, a higher growth temperature of 750° C is used to increase the growth rate to account for the significantly larger volume of In that must be converted. Figure 4a shows a false-colored cross-sectional SEM image of an InAsP film grown with a flow ratio of 1:200 sccm of AsH_3:PH_3. X-ray diffraction (XRD) and PL measurements were used to measure the stoichiometry of films with various AsH_3:PH_3 flow ratios. For XRD measurements, the (311) peak positions of InAs and InP thin films, grown using TF-VLS with either only AsH_3 or PH_3 flow, were measured to be 49.897° and 51.625°, corresponding to lattice constants of 6.058 and 5.869 Å, respectively. From the XRD measurements of the intermediate stoichiometries with different AsH_3:PH_3 flow ratios (Fig. 4b), Vegard's law was then utilized using the InAs and InP measurements as reference points. In all cases, the FWHM of the samples are around 0.2° as compared to the instrument broadening of ~0.1°, which can be attributed to slight variations in composition within the sample.

To verify the accuracy of the XRD extraction, PL measurements were also done on samples grown with AsH_3:PH_3 ratios of 0.005, 0.01, 0.025, and 0.05. Figure 4c shows the PL spectra taken from multiple spots across InAsP samples grown under these conditions. The standard deviation among the PL peak positions is 5, 2.4, 5.8, and 8.2 meV for AsH_3:PH_3 ratios of 0.005, 0.01, 0.025, and 0.05, respectively, once again verifying the compositional uniformity of the growth method. As can be seen from the plot of the extracted As composition versus AsH_3:PH_3 flow ratio in Fig. 4d, the extracted compositions from XRD and PL are all within 2% of each other, which is well within error of the measurement and extraction methods used.

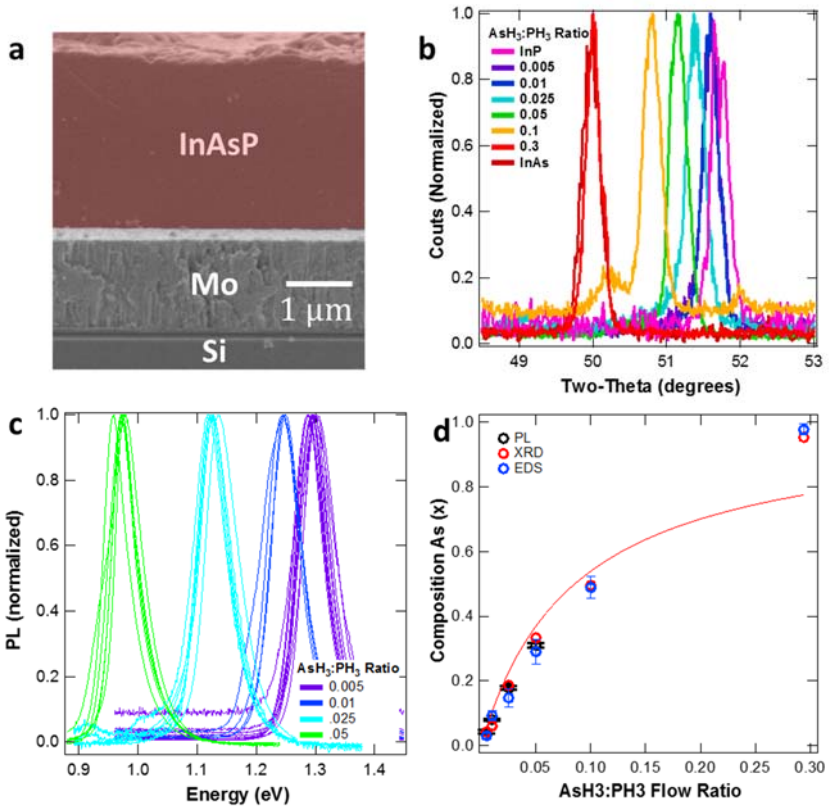


Figure 4: Full area film growth. a) Cross sectional SEM image of an InAsP film grown via TF-VLS. The InAsP is false-colored in red. b) XRD spectra of the (311) peak taken from films grown under different AsH_3:PH_3 flow ratios with an 80 nm thick SiO_x encapsulation layer. c) PL

spectra taken from InAsP thin films grown with AsH_3:PH_3 ratios of 0.005, 0.01, 0.025, and 0.05. d) As composition (x) versus AsH_3:PH_3 ratio extracted from PL and XRD measurements.

Compared to the patterned InAsP grown via TLP growth, the trend of composition versus AsH_3:PH_3 ratio shows a similar, nonlinear, trend. However, the AsH_3:PH_3 flow ratio required to reach nearly 100% As is much lower. This is most likely due to the very different growth temperature used, which can affect the percentage of AsH_3 and PH_3 which are cracked, as well as the incorporation ratios of As and P in the vapor-liquid and liquid-solid phase transformations.

In addition to testing different AsH_3:PH_3 ratios to vary the stoichiometry, the effect of the SiO_x capping thickness was also explored. Starting with the same thickness of 1.5 μm In, only 40 nm of SiO_x was evaporated to encapsulate the In rather than 80 nm. Growth was once again carried out with multiple samples in AsH_3:PH_3 ratios of 0.005, 0.01, 0.025, 0.05, 0. 0.1, and 0.3 at 750 °C. XRD and PL measurements were utilized to extract the average composition and compositional uniformity across the different growth conditions and plotted in Supplementary Fig. S2. Overall, the decrease in SiO_x encapsulation thickness results in a more As rich film, which can be explained by different diffusion rates of As and P through the SiO_x cap. In addition, the standard deviation in the extracted compositions across multiple points also increases with the thinner SiO_x cap. This is most likely due to the fact that compared to thermal SiO_2, the evaporated SiO_x is more porous, and so the thickness and porosity of the SiO_x may be less uniform with the thinner encapsulation layer. This points towards the fact that the film stoichiometry uniformity may be able to be further improved in the future via thicker SiO_x encapsulation layers or using other encapsulation materials which may yield more conformal/uniform films.

In conclusion, we have demonstrated here the extension of the TLP and TF-VLS growth modes beyond simple binary III-V semiconductors. By flowing two different group V precursors simultaneously, ternary compounds can also be grown via these two methods. The stoichiometry of the film can be well controlled by tuning the flow ratios of the two group V precursors as well as the SiO_x encapsulation layer thickness. The TLP and TF-VLS growth methods allow for control of film size and geometry ranging from sub-micron patterns up to large-area films with excellent composition uniformity. The extension to ternary compounds allows for a wide variety of band gaps and lattice constants to be achieved, making these growth methods good candidates for direct growth of device layers or virtual substrates on amorphous substrates or for direct integration with silicon-based electronics. While InAsP was used as an example materials system in this work, the concept should be able to be extended to other ternary or even quaternary compound semiconductors by changing either the group III metal or the group V precursor gases.

2.3.4 Experimental and Theoretical Details

2.3.4.1 Sample preparation

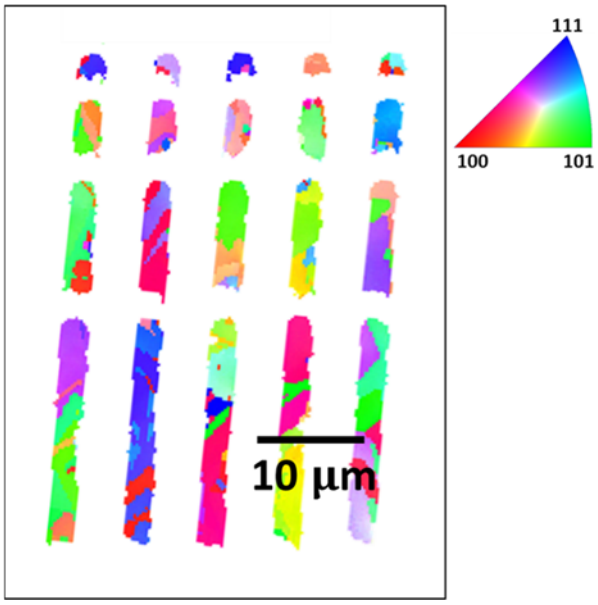
For TLP growth, photolithography is first used to define features on a Si/SiO_2 wafer. Thermal evaporation is used to deposit 2-8 nm of MoO_x followed by 200 nm of In and 40 nm of SiO_x via electron beam evaporation. For the In and SiO_x evaporation, the sample chuck is cooled down to <120 K by flowing nitrogen gas cooled via liquid N_2 through the chuck to ensure a smooth film is obtained. Subsequently, three angled evaporations are utilized to conformally coat all sides with SiO_x (30 nm per evaporation).

For TF-VLS growth, 1 μm of Mo metal is sputtered onto a Si/SiO_2 wafer as a wetting layer. Then, 1.5 μm of In and either 40 or 80 nm of SiO_x is evaporated via electron beam evaporation.

2.3.4.2 InAsP growth

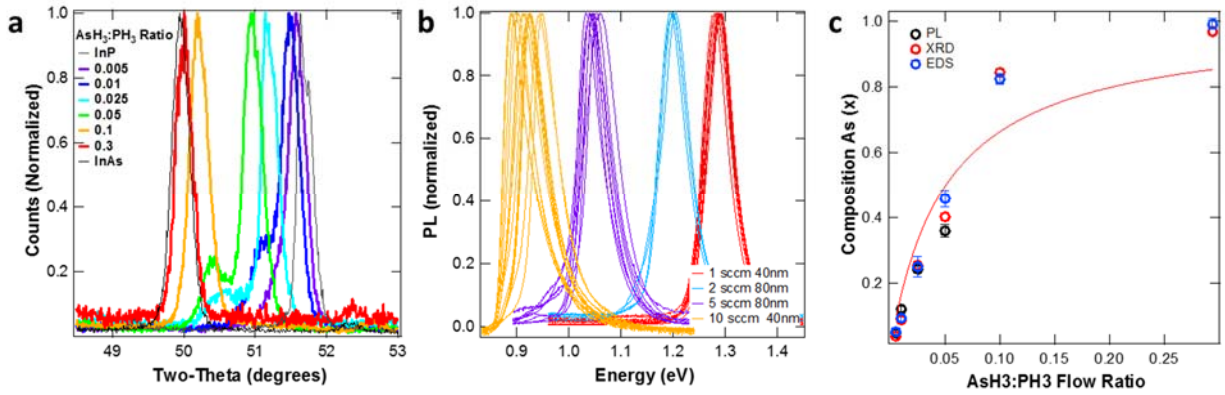
For TLP growth, samples are grown in an AIXTRON Black Magic PECVD chamber. After pumping down the chamber, the AsH_3 and PH_3 (diluted to 2% AsH_3 and 1.6% PH_3) are introduced into the chamber at room temperature. The AsH_3 flow ranges from 1-50 sccm while the PH_3 flow rate was kept at between 50-200 sccm. Pure hydrogen was also introduced at rates between 0-20 sccm in order to maintain a total gas flow rate of 220 sccm in all growths. After the chamber pressure stabilized for one minute at a growth pressure of 200 mbar in all runs, the chamber was heated up to 565° C with a ramp rate of 300° C/min. For TF-VLS growth, the temperature was further ramped up to 750° C at a ramp rate of 100° C/min. Growth occurred at the set growth temperature for 20 minutes. After 20 minutes, the chamber was cooled down to 250° C while maintaining the same pressure/flow rates after which the system was purged by N_2 gas and let cool down to 65° C in vacuum before venting.

2.3.4.3 EBSD before twin boundary averaging



Supplementary Figure S1: EBSD of MWs. EBSD map of the MWs in Fig. 1c before averaging of the twin boundaries.

2.3.4.4 Effect of Oxide Thickness



Supplementary Figure S2: a) XRD spectra of the (311) peak taken from films grown under different AsH_3:PH_3 flow ratios with an 40 nm thick SiO_x encapsulation layer. b) PL spectra taken from InAsP thin films grown with AsH_3:PH_3 ratios of 0.005, 0.01, 0.025, and 0.05. c) As composition (x) versus AsH_3:PH_3 ratio extracted from PL and XRD measurements.

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Chapter 3 Liquid State Devices for Deformable and Flexible Electronics.

3.1 Introduction

In the previous chapter, growth of III-V semiconductors by taking advantage of the low melting point of the group III metals was explored via a vapor-liquid-solid mechanism. In addition to growth of III-V's, the low melting point of the group III metals can enable them to be used for many other applications. In particular, by alloying the group III metals In and Ga together, an InGa eutectic which is a liquid at room temperature can be obtained. Unlike other liquid metals such as mercury, In and Ga are non-toxic, making them ideal candidates for "liquid-state" electronic devices in flexible and stretchable electronics applications. Sensors utilizing liquids confined in soft templates as the sensing component present the ideal platform for such applications, as liquids are inherently more deformable than solids. However, to date, liquid-based devices have been limited to metal lines based on a single liquid component given the difficulty in the fabrication of liquid-based junctions due to intermixing.

To form more advanced functional electronics, it would be ideal to be able to separate the sensing component from the interconnect component so that each can be optimized for their respective roles. In the following section, a new platform is demonstrated for the fabrication of liquid-liquid "heterojunction" devices, presenting an important advancement towards the realization of liquid-state electronic systems. The device architecture and fabrication schemes presented are generic for different sensing liquids, enabling demonstration of sensors responsive to different stimuli. As a proof of concept, multiple sensors optimized towards sensing temperature, humidity and oxygen by using different ionic liquids are achieved, exhibiting high sensitivity with excellent mechanical deformability arising from the inherent property of the liquid phase.

3.2 Liquid-State Electronics

The following subchapter has been previously published in a similar format in:
H. Ota, K. Chen, *et al*. Highly-deformable liquid-state heterojunction sensors. *Nature Communications*, **5**, 5032, (2014)

Electronic devices and sensors which exhibit large amounts of mechanical deformability have many applications in smart wallpapers[1-2], physiological body sensors[3-7], and human-machine interfaces for prosthetics[8-10] and robotics[11-14]. In this regard, tremendous advancements have been made in engineering solid-state electronic materials and devices on elastic substrates[1, 6, 9-10, 15-22]. Recently, sensors based on using liquid active components embedded within soft elastomeric substrates have shown much promise for such applications as liquids present the ultimate limit in deformability. Previous works have shown InGa eutectic metal can be patterned as conductive electrodes[14, 18-22] and configured as pressure sensors[14], capable of withstanding up to 250% strain without failure.

One limiting factor in the fabrication of more sophisticated liquid based sensors is the inability to combine multiple liquids into one device due to intermixing. Through modeling and experiments, we present the design requirements for the device architecture and the liquid properties needed to overcome this barrier and enable heterojunction confinement without intermixing. As a proof of concept and to show the generic nature of our design, we utilize multiple different ionic liquids as the active sensing liquid to sense different stimuli including temperature, humidity, and oxygen gas sensing, with excellent performance characteristics even when under deformation.

3.2.1 Selection of liquids

Galinstan is a eutectic metal, composed of 68.5% Ga, 21.5% In and 10% Sn. It exhibits high electrical conductivity (3.40×10^6 S/m)[21], low vapor pressure (<100 pPa at 25 °C)[23], and is nontoxic[22]. These physical properties present Galinstan as an ideal liquid metal for liquid-state device applications. While Galinstan makes for an excellent conductor, it alone is not sufficient to achieve sophisticated liquid-based electronic devices. For the realization of liquid-state devices, and eventually systems, controlled heterojunctions must be made between different liquid components[24], analogous to metal/semiconductor or semiconductor/semiconductor junctions seen in traditional solid-state devices. More generally, junctions represent the fundamental building-blocks for any device technology. With this in mind, we present a fabrication platform for the controlled formation of liquid-liquid "heterojunctions" using immiscible liquids. As example systems, we demonstrate the functionality of liquid heterojunctions for temperature, humidity and oxygen gas sensing. Here, Galinstan is used as the source/drain metal electrodes to contact an ionic liquid, which serves as the active sensing element. Four different ionic liquids were used to enable the desired sensing functionalities, including 1-Ethyl-3-methylimidazolium trifluoromethanesulfonate ([EMIM][Otf]), 1-Hexyl-3-methylimidazolium chloride ([HMIM][Cl]), 1-Butyl-3-methylimidazolium hexafluorophosphate ([BMIM][PF6]) and 1-Butyl-1-methylpyrrolidinium bis(trifluoromethylsulfonyl)imide ([BMPYR][NTf2]). The first two ionic liquids are hydrophilic and the latter two are hydrophobic. While the resistivity of Galinstan has minimal dependence on the various stimuli explored in this work, the conductance and capacitance of the ionic liquids are highly responsive to the desired stimuli, thus providing a reliable sensor technology that can undergo severe forms of mechanical deformation without degradation or irreversible change in electrical properties.

In this liquid-liquid "heterojunction" concept, it is critical to prevent intermixing of the two liquid components, especially during fabrication as well as when the completed devices undergo mechanical deformation. To prevent breakdown of liquid heterointerfaces, two important design considerations are made. First, the two liquids are selected such that they are immiscible. Second, the layout and dimensions of the polydimethylsiloxane (PDMS) microfluidic template, which dictate the device architecture, are properly engineered.

For the metal electrodes, we chose Galinstan due to the reasons stated previously. For the active sensing elements, ionic liquids were chosen since they are immiscible with Galinstan. Furthermore, ionic liquids generally have a high boiling point[25], low vapor pressure[26], and are non-flammable[27]. A high boiling point and low vapor pressure are critical to the stability of the device while operating at elevated temperatures. Given the extremely small volume of liquid (~315 nL) contained in the active region of the device, high vapor pressure liquids such as water readily evaporate through the PDMS substrate. Since ionic liquids have a nearly negligible vapor pressure, they are non-volatile without any noticeable loss through the PDMS microfluidic template for temperatures up to 80 ºC.

3.2.2 Device architecture and fabrication scheme

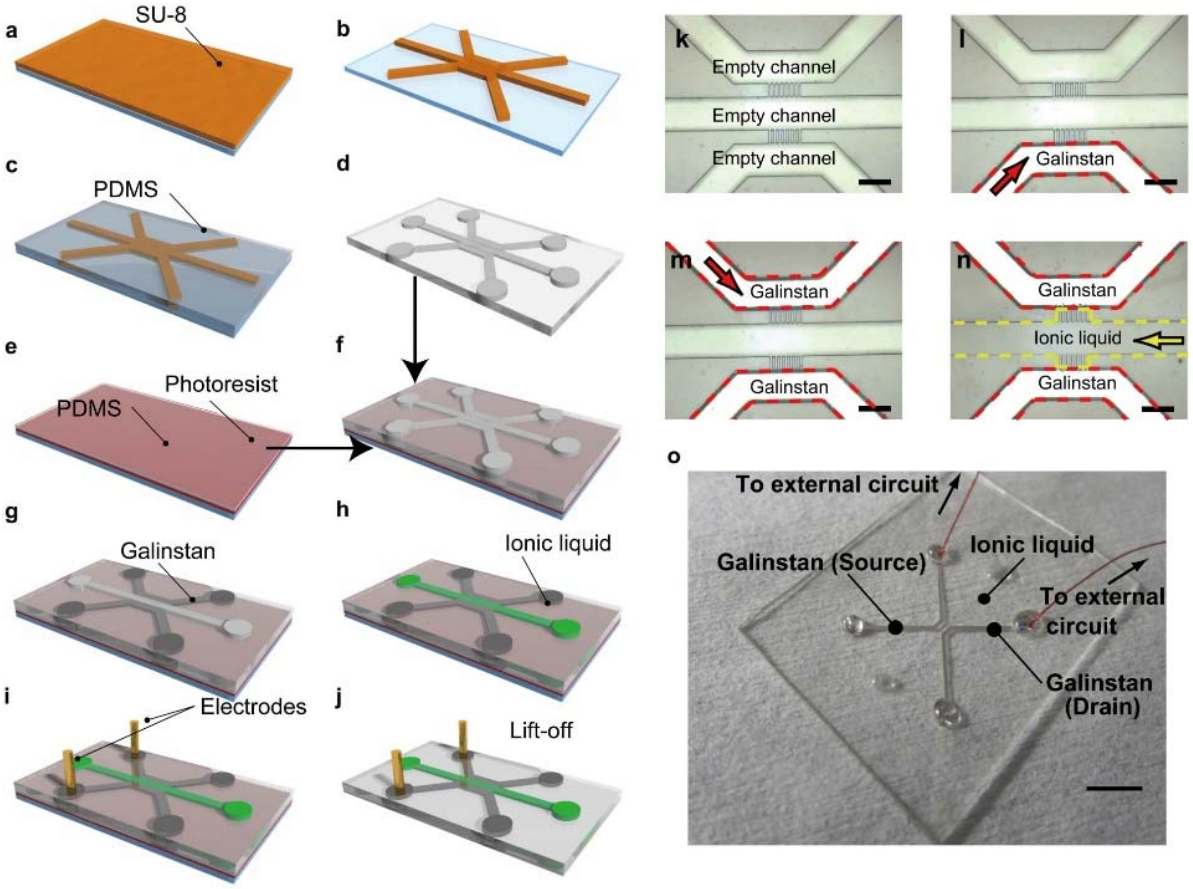


Figure 1 Liquid heterojunction device fabrication. a-j, Fabrication process flow. **k-n,** Step-by-step optical microscope images taken after injection of each liquid component (scale bar, 500

μm). **o,** Fully fabricated liquid heterojunction device consisting of an ionic liquid active channel and GaInSn source/drain electrodes (scale bar, 2.5 mm).

The device was fabricated via traditional microfluidic process technology (Fig. 1a-n). The PDMS channels were patterned and cured on an SU-8 master mold. The patterned PDMS was then bonded onto a second unpatterned PDMS substrate to complete the formation of the microchannels. After bonding, Galinstan and the ionic liquid were injected into the channels sequentially using a syringe pump. Finally, the channels were sealed off using silicone rubber. An optical image of a fully fabricated device is shown in Figure 1o.

To prevent the liquids from interpenetrating during the fabrication process or due to applied strain, we implemented high flow resistance structures at the interface of the two liquids[14]. Rather than one continuous junction connecting Galinstan and the ionic liquid, the two liquids are connected via a series of "heterojunction" microchannels 30 μm wide, 31 μm high, and 200 μm long (Fig. 1 k-o). These channels, termed as junction channels, introduce regions of high flow resistance which prevent the two liquids from interpenetrating. For maximum robustness, it is ideal to design the junction channels with minimal width and height. To tune the contact area between the Galinstan and ionic liquid (*i.e.,* total junction width), the number of junction channels can be changed.

Next, we explore the device design rules needed to enable fabrication of the liquid heterojunctions. The first criterion is that Galinstan must not penetrate into the junction channels (designated for ionic liquids) during injection. Two variables that affect this criteria are the total pressure P_T of Galinstan, and the capillary pressure P_C at the junction channel interface. The total pressure is composed of the static pressure P_S, which is constant for our structure, and the dynamic pressure P_D, which depends on the Galinstan injection velocity, v, as described by the equation:

$$P_D = \frac{1}{2}\rho v^2$$

Here, ρ is the density of Galinstan (6.44 g/cm^3), and v is controlled by the volume injection rate of the syringe pump. The capillary pressure is the pressure drop across the Galinstan-air interface and is calculated using the equation:

$$P_C = 2\cos(\theta)\gamma\left(\frac{1}{h}+\frac{1}{w}\right)$$

In this equation, θ is the contact angle of Galinstan on PDMS, measured to be 134° using a Kruss contact angle analyzer (Fig. 2a), which is in line with reported values of 120-140° in literature[28]. The phenomenological parameter γ is a measure of the force between the Galinstan and the PDMS surface, and w and h are the width and height of the junction channel, respectively. In order for Galinstan to not enter the junction channels during injection, P_T must be less than P_C (Fig. 2b).

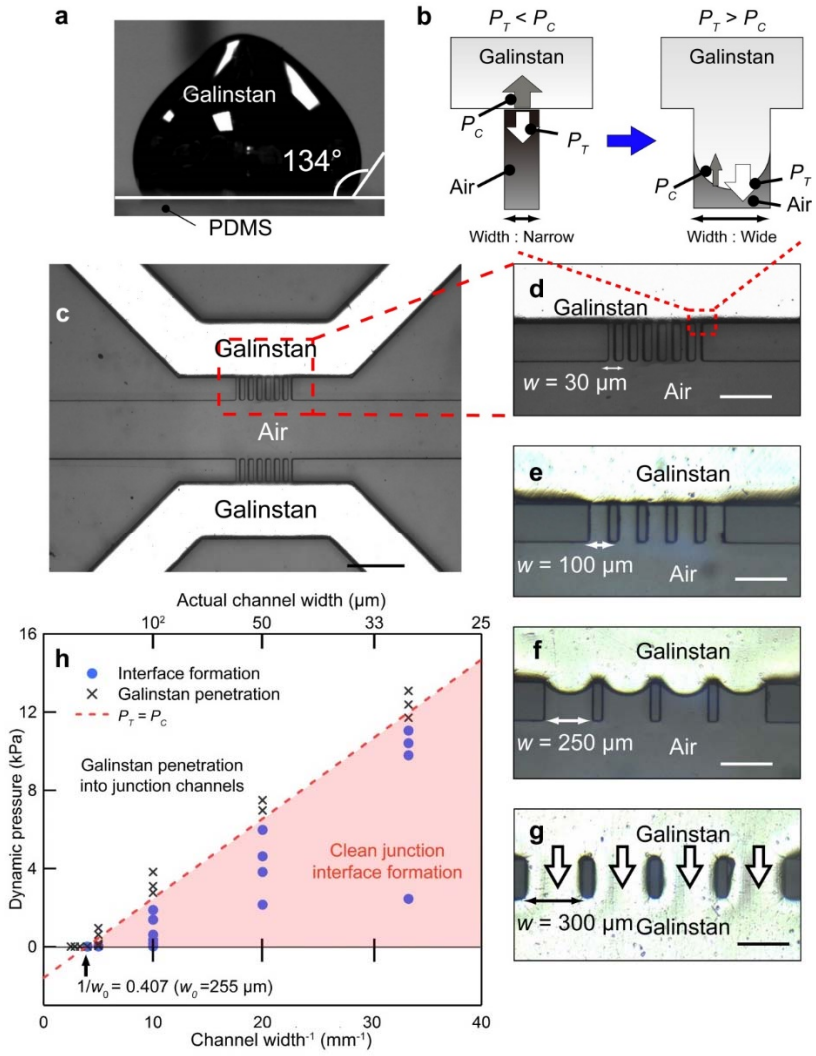


Figure 2 Design considerations for the fabrication of liquid heterojunctions. a, Contact angle of Galinstan on oxygen plasma-treated PDMS, measured to be 134°. **b,** Schematic illustrations of narrow and wide junction channels during Galinstan injection, depicting the relationship between the capillary pressure (P_C) and total pressure (P_T). For the narrow junction channels, where $P_T<P_C$, the heterojunction is successfully formed. However, for the wide junction channels, where $P_T > P_C$, Galinstan penetrates into the junction channels, preventing controlled formation of the heterojunction. **c,** Optical image of a device after Galinstan injection (scale bar, 500 μm). The separation of Galinstan from the junction channel edge (before the injection of ionic liquid) is maintained for devices with junction widths **d,** 30, **e,** 100 and **f,** 250 μm. **g,** In the case of a device with w=300 μm, Galinstan penetrates into the area designated for the ionic liquid. Scale bars for **d-g** are 250 μm. **h,** The relationship between dynamic pressure and the inverse of the junction channel width. Different dynamic pressures at each channel width correspond to different injection velocities of Galinstan. W_0 is the structural limit extracted from the x-intercept of the linear regression of the experimental lower bounds of dynamic pressure for which Galinstan penetrates into the junction channels.

To further shed light on the model above and experimentally obtain the quantitative parameters needed for successful device fabrication, we varied w and v to modulate P_C and the dynamic pressure component of P_T, respectively. Specifically, w was varied from 30-300 μm while the height and length were fixed at 31 μm and 200 μm, respectively. The injection rate for Galinstan was varied from 25 to 1900 μL/min. Optical microscope images of representative devices with different w fabricated using v= 27 mm/sec are shown in Fig. 2c-g. As evident from the images, Galinstan is confined to the designed electrode regions when w<250 μm (Fig. 2d-f). However, the Galinstan interface does not maintain its integrity when w>250 μm (Fig. 2g). While it is possible to use the pressure of the ionic liquid injection to push the Galinstan back to its own territory for channels with w~250 μm where there is partial invasion into the junction channels, we find that doing so does not result in sharp junctions (Supplementary Figure S1). Thus, it is best to use w as the main fabrication parameter for creating well defined junction interfaces. Figure 2h shows the relationship between dynamic pressure (obtained by varying v) and the inverse of the junction channel width, w^{-1} in determining the fabrication success of the devices. The linear regression, extracted from the experimental lower bounds of dynamic pressure for Galinstan penetration into the junction channels, corresponds to the limit at which $P_C = P_T = P_D + P_S$. From the slope of the regression line, we extract γ = 600±86 (mN/m), which is comparable to previously reported values of 624-630 mN/m[18]. The x-intercept of the regression indicates the structural limit of the junction channel width (W_0), extracted to be 255 μm. This represents the maximum junction width for which Galinstan diffusion into the active device area can be blocked as v, and thereby P_D, approaches zero.

In addition to proper channel design, the order of liquid injection during the fabrication process is important. Ionic liquids have a low contact angle with PDMS (Supplementary Figure S2) which means that P_C is directed in the same direction as P_T. As a result, ionic liquids invade all patterned channels, including those designated for the Galinstan electrodes (Supplementary Figure S3), via capillary pressure if injected first, regardless of the junction channel dimensions or injection velocity. On the other hand, given the high contact angle of Galinstan on PDMS (~134º), it can be controllably injected into the designated regions as long as the proper design parameters for the junction channels are incorporated as previously discussed. Thus, Galinstan is injected prior to the ionic liquid. After Galinstan patterning, the ionic liquid is injected into the active channel region to complete the liquid heterojunction. Once again, due to the direction of the capillary pressure, the ionic liquid naturally diffuses into the junction channels until it interfaces with Galinstan, completing the controlled formation of liquid-liquid junctions between Galinstan and the ionic liquid. While other liquid parameters such as viscosity may play a slight role, their effects are minimal (Supplementary Figure S2). Liquid-state devices exhibit excellent mechanical deformability. Figures 3a-d illustrate optical images of a device undergoing 90% uniaxial strain with the liquids maintaining their confinement and junction interface. Above 90% strain, the device failed (Supplementary Figure S4) though it should be noted here that the failure was due to the solid PDMS substrate rather than that of the liquid heterojunction. Figures 3e-l demonstrate the mechanical stability of the device as it undergoes various other forms of deformation: bending (Fig. 3h), twisting (Fig. 3i), grasping (Fig. 3j) and tying (Fig. 3k). The substrate withstood all deformations and the structure of the liquid heterojunction was maintained as shown in Fig. 3l. The results demonstrate the unique feature and potential of liquid-state device technology, taking advantage of the inherent mechanical property of the liquid phase.

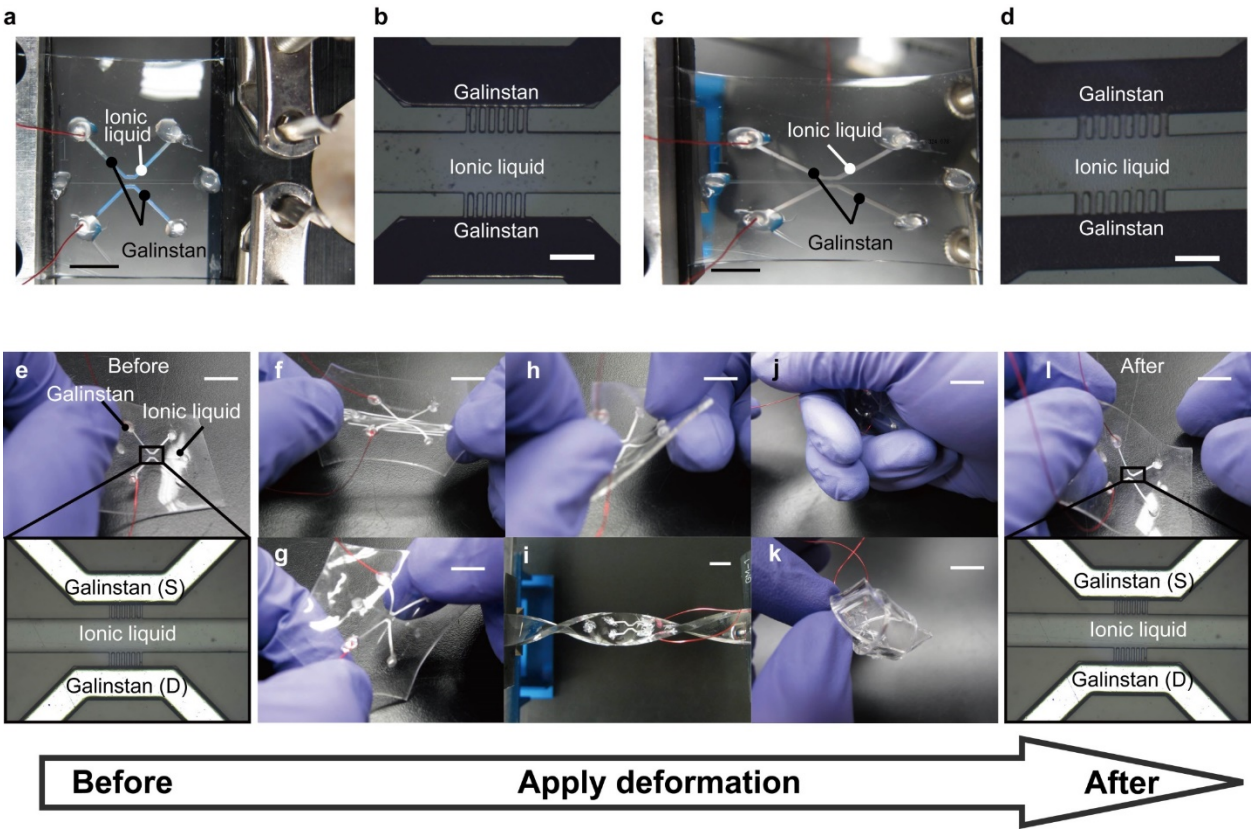


Figure 3 Mechanical deformation of the liquid heterojunction device. a, b, Optical images of a device with no strain applied using [EMIM][Otf] as the ionic liquid (a, scale bar is 5mm; b, scale bar is 500 μm). **c, d,** Optical images of the device stretched by 90% perpendicular to the axis of the junction channels, showing that the liquid confinement and heterointerface are well maintained (c, scale bar is 5mm; d, scale bar is 500 μm). **e-l,** Optical images of a device as it undergoes various forms of deformation (scale bar is 5 mm). After undergoing all the various user-applied deformations, the separation of the liquids in the channels was well maintained (**l**).

3.2.3 Temperature sensing

The fabricated liquid heterojunctions are electrically active and can be configured as functional devices. As a proof-of-concept, here we utilize our Galinstan/ionic liquid/Galinstan heterojunction device as a temperature sensor. The device operates as a temperature sensitive constant phase element (nonideal capacitor) and resistor in series, with the two Galinstan regions acting as the source/drain metal electrodes and the ionic liquid ([EMIM][Otf]) channel acting as the temperature-sensitive active component (Fig. 4a). Note that Galinstan exhibits minimal temperature response (Supplementary Figure S5) and acts as the passive element of the device. Sensing experiments were performed by placing the samples inside an oven while varying the temperature from 25-69 °C. Both the capacitance, C, and conductance, G, of the sensor were extracted via capacitance-voltage measurements as a function of temperature (Supplementary Figure S6).

Figures 4b and c shows the temperature dependence of C and G, normalized to their values at 25 °C (C_o and G_o, respectively). Both capacitance and conductance increase with temperature. Specifically, as the temperature is increased from 25 °C to 69 °C, conductance and capacitance

values increase by ~272% and 144%, respectively. Notably, the sensor response is linear for the explored temperature range of 25-69 °C with a sensitivity of 3.9% change in conductance per degree Celsius. As shown in Figure 4b, the sensor response between temperature loading and unloading (i.e., temperature hysteresis loop) is highly identical, thus exhibiting minimal hysteresis. In addition, the response is highly stable over multiple temperature cycling (Fig. 4d) with a standard deviation in the sensor output of <2.5% for 10 measurement cycles (temperature was cycled between 25°C and 80°C) which is within the error of the oven temperature reading. Based on the standard deviation of 2.5% for multiple cycling and the sensitivity of 3.9%/ºC, the minimum detectable temperature change using [EMIM][Otf] is (2.5%)/(3.9%/°C)=0.64°C. Two other ionic liquids, [BMIM][PF6] and [BMPYR][NTf2], were also configured into a similar device structure (Supplementary Figure S7), exhibiting temperature sensitivities of 9.3 %/°C and 7.4 %/°C for conductance, respectively. These results show the generic nature of our process scheme, and its compatibility with different active ionic liquids for fabrication of functional liquid-state devices. Not only can the sensitivity of a given sensor be optimized by changing the ionic liquid, but more importantly, different chemical sensing functionality can be obtained as discussed later in this manuscript.

The sensitivity of our temperature sensor compares favorably with other stretchable temperature sensors reported in literature based on solid-state materials. For instance, temperature sensors based on wrinkled[17] and wavy metal lines[6] exhibit sensitivities of ~0.2 and 0.53 %/°C, respectively, for the same temperature range. In this regard, our sensor with [BMIM][PF6] as the active ionic liquid presents a 17-46x enhancement in sensitivity over previous works.

The high sensitivity of our temperature sensor is due to the ion transport properties of the ionic liquid. The conductance of ionic liquids are known to drastically increase with temperature[27]. Ion transport is a thermally activated process[25], with enhanced ion mobility at elevated temperatures (Fig. 4a). In addition, ion dissociation (*i.e.,* generation) is enhanced at high temperatures[30], leading to an increase in charge carriers (Fig. 4a). Both effects lead to increased conductivity with temperature. The temperature dependence of the capacitance is associated with the change in the double layer formed by the ionic liquid. The exact mechanism, however, is not well established and different explanations have been proposed in literature. One proposed explanation is that the free vacancies in the ionic liquid increase with temperature[30]. Another theoretical model has shown that complex molecules in the double layer dissociate as the temperature increases[31]. Lockett and Sedev report that the increase in temperature causes an increase in the number of ions available for adsorption at the double layer, which leads to an increase in capacitance with temperature[32]. Nevertheless, our experimental trend of increasing capacitance with temperature is consistent with those reported in literature[30-32]. As can be seen in Figure 4c, the change in conductance of our sensor quickly follows the change in temperature of the oven, measured via a thermometer. This means that the measured response time of our sensor is limited by the temperature ramp time of the oven (on the order of 0.4 °C/sec).

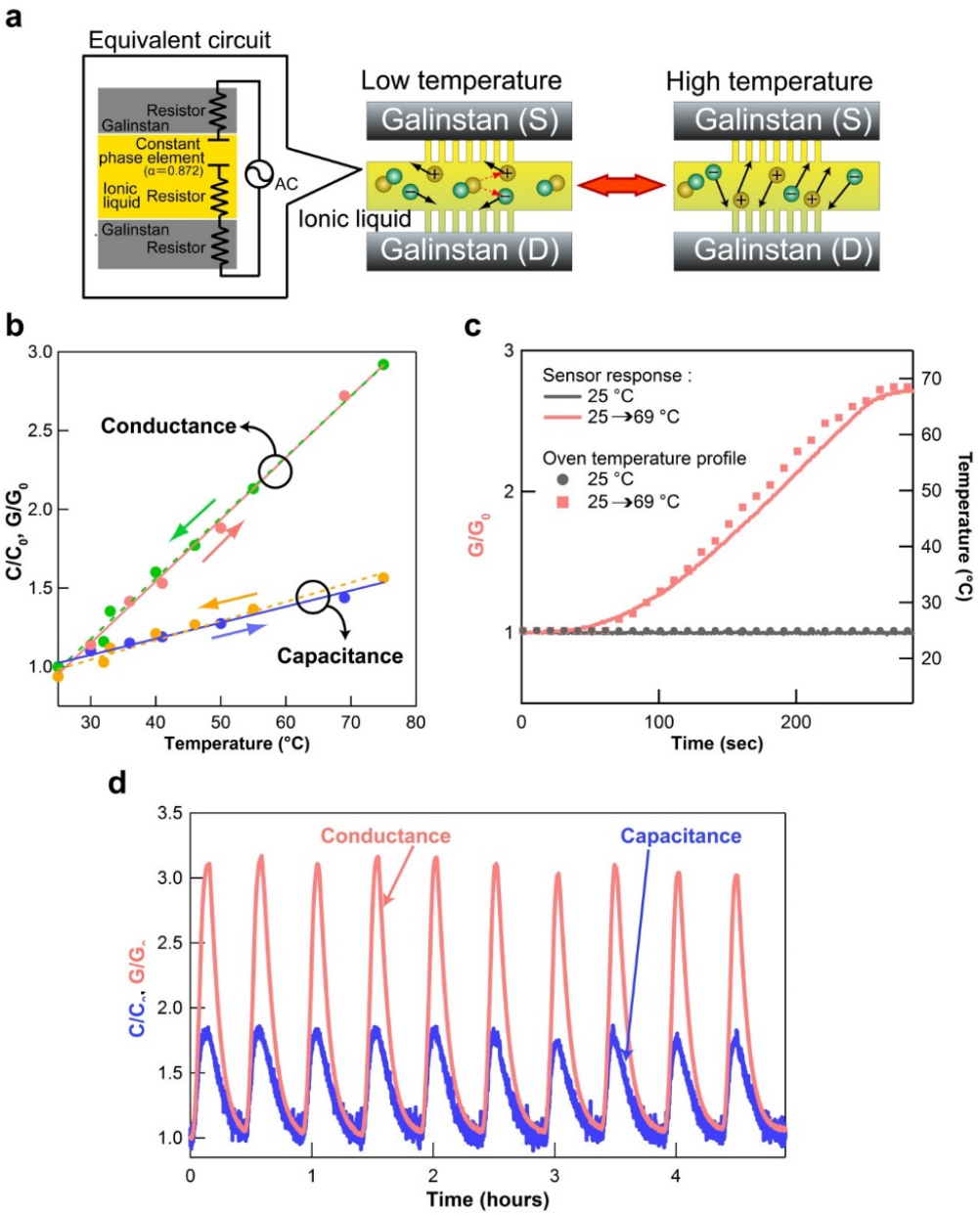


Figure 4 Liquid-state heterojunctions as temperature sensors. a, The equivalent circuit of the device. The mobility and number of dissociated ions in the ionic liquid increase with increasing temperature, which leads to an increase in conductance (middle and right schematics). **b,** Measured conductance, *G* (red, temperature loading, green temperature unloading), and capacitance, *C* (blue, temperature loading, yellow temperature unloading), of the sensor as a function of temperature. The data points are normalized by the values at 25 °C (G_o and C_o, respectively). **c,** Time-dependent measurements of the sensor (solid lines) as the oven temperature is increased (square marks). The response of the sensor closely matches the oven temperature profile, measured by a thermocouple. **d,** Normalized conductance and capacitance, *G* and *C*, of the sensor for 10 temperature loading and unloading cycles (temperature cycled between 25°C and 80°C). All data is obtained using [EMIM][Otf] as the ionic liquid component of the sensors.

3.2.4 Deformation effects on the heterojunction sensor

The stability of the sensor functionality using [EMIM][Otf] under stretching and twisting deformations is illustrated in Figure 5. As depicted in Fig. 5a, the conductance and capacitance increase by 13% and 8%, respectively as the device undergoes 30% uniaxial stretch perpendicular to the axis of the junction channels. On the other hand, when the device is stretched by 30% along the axis of the junction channels, the conductance and capacitance decrease by 13% and 1%, respectively (Supplementary Figure S8). When the device is stretched perpendicular to the axis of the junction channels, the widths of the junction channels increase while their lengths decrease, leading to an increase in conductance and capacitance. However, when the device is stretched along the axis of the junction channels, the junction channels become elongated and thinner, thus leading to a drop in conductance and capacitance. The changes in conductance and capacitance of our device due to deformation are consistent with expected geometric changes in the device dimensions (Fig. 5b and Supplementary Figure S9). Fig. 5c depicts the device operation when the sensor is twisted by 60° which results in a 1% drop in conductance and 4% increase in capacitance. It should be noted that the changes in C and G by strain are fully reversible.

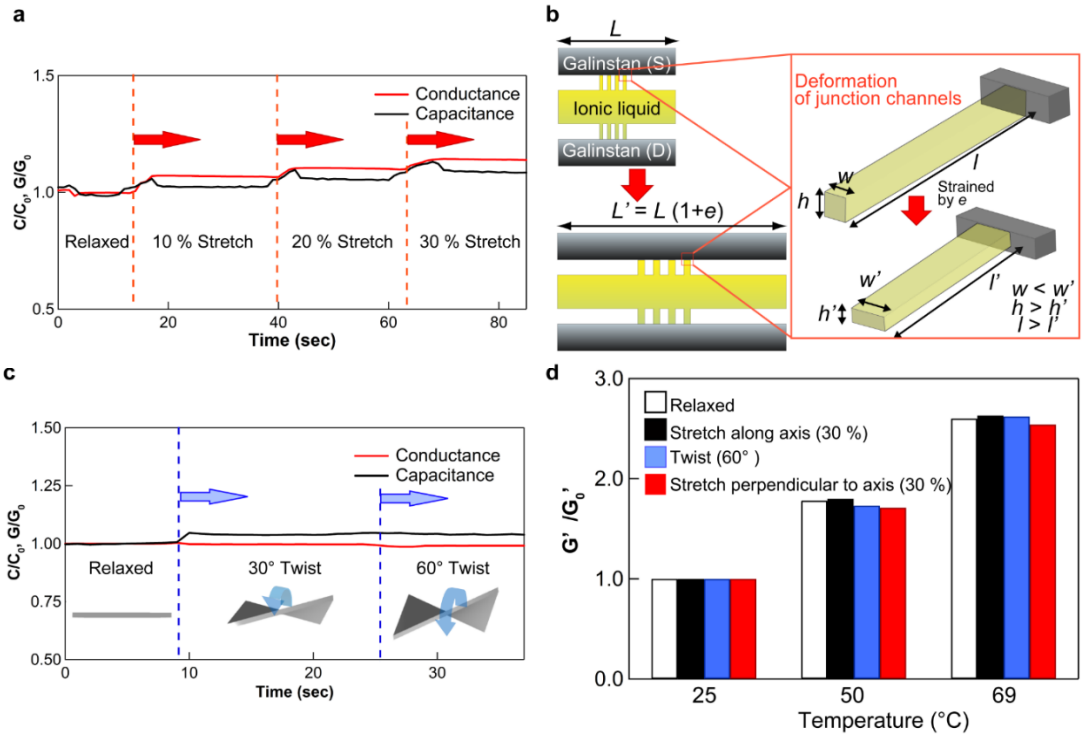


Figure 5 Temperature sensing while under various modes of deformation. a, The relative conductance and capacitance as a device is stretched by 10, 20, and 30% perpendicular to the axis of the junction channels. Here, [EMIM][Otf] is used as the ionic liquid. **b,** A schematic of the relative structural change of the junction channels when the device is stretched perpendicular to the axis of the junction channels by *e*. *e* is defined to be the change in length (ΔL) divided by the original length (L) of the whole sensor. **c,** The ratio of the relative conductance and capacitance of a device when twisted by 30° and 60° at 25 °C. **d,** Conductance, G' of the device at 25, 50 and 69 °C as it undergoes various forms of deformation. G_0' represents the conductance of the device at 25 °C for the corresponding deformation state.

We also explored the temperature sensitivity of the sensor as it is mechanically deformed. Fig. 5d shows the response of conductance with respect to temperature while the device is stretched 30% along and perpendicular to the axis of the junction channels as well as twisted by 60°. Since the change caused by the deformations is significantly smaller compared to the temperature sensitivity, the sensor can operate with reasonable accuracy (up to ±2 °C error for the applied strains and temperature range) even under various forms of mechanical deformations. For practical applications, sensors can be calibrated for different deformations – matching those that they encounter for the targeted use to further enhance the sensor accuracy. For instance, standalone strain sensors based on liquid Galinstan metal lines[14] can be integrated on the same substrate. As previously reported[14], the resistivity of patterned Galinstan lines changes with strain. Since the resistivity of Galinstan has minimal dependence on temperature, such a sensor can selectively monitor strain, thus providing a calibration pathway for the output signal of the temperature sensors as a function of strain.

3.2.5 Humidity and oxygen gas sensing

We also explored the use of liquid-state heterojunction devices for humidity and oxygen gas sensing using different ionic liquids as the active component. Previous studies have shown the high sensitivity of ionic liquids to different molecular species depending on their chemical properties. The sensitivity is often attributed to enhanced ion conductivity and/or concentration[33, 34]. On the other hand, hydrophobic ionic liquids show minimal sensitivity to humidity, with the response decreasing with increasing hydrophobicity[35, 36]. We observe the same trend in the conductance and capacitance of our liquid-state heterojunction devices (Fig. 6a). Specifically, we explored the humidity response of [EMIM][Otf], [BMIM][PF6] and [BMPYR][NTf2] with ascending hydrophobicity. [EMIM][Otf] exhibits the highest sensitivity to humidity, with a 1.7% change in conductance per 1% increase in humidity (Fig. 6a, b). This sensitivity is remarkably high given that the commercial humidity sensors, which are usually based on capacitive sensing, have sensitivities of ~0.3% [32.25]. On the other hand, [BMPYR][NTf2] shows the least response with a sensitivity of <0.2% change in conductance per 1% increase in humidity for the explored humidity range of 13 % to 87 %. This minimal sensitivity to humidity makes [BMPYR][NTf2] the more optimal ionic liquid for temperature sensing applications since the humidity level often changes with temperature. Considering the high sensitivity of [BMPYR][NTf2] to temperature as shown in Supplementary Figure S7, a humidity change from 13 % to 87 % leads to a temperature reading inaccuracy of only ± 1.6 °C for this sensor.

Finally, the oxygen sensitivity of the liquid-state devices is examined as depicted in Fig. 6c,d. All three ionic liquids exhibit increase in conductance and capacitance in response to oxygen with [EMIM][Otf] exhibiting the highest sensitivity of 1.0% increase in conductance per 1% increase in oxygen concentration. As shown here, using different ionic liquids as the sensing element can yield tuned response to various stimuli. For each type of stimuli, the sensing can be optimized by choosing the proper ionic liquid. In the future, multiple liquid heterojunction sensors, each with a different ionic liquid may be multiplexed into a fully integrated system to sense different stimuli with calibrated response.

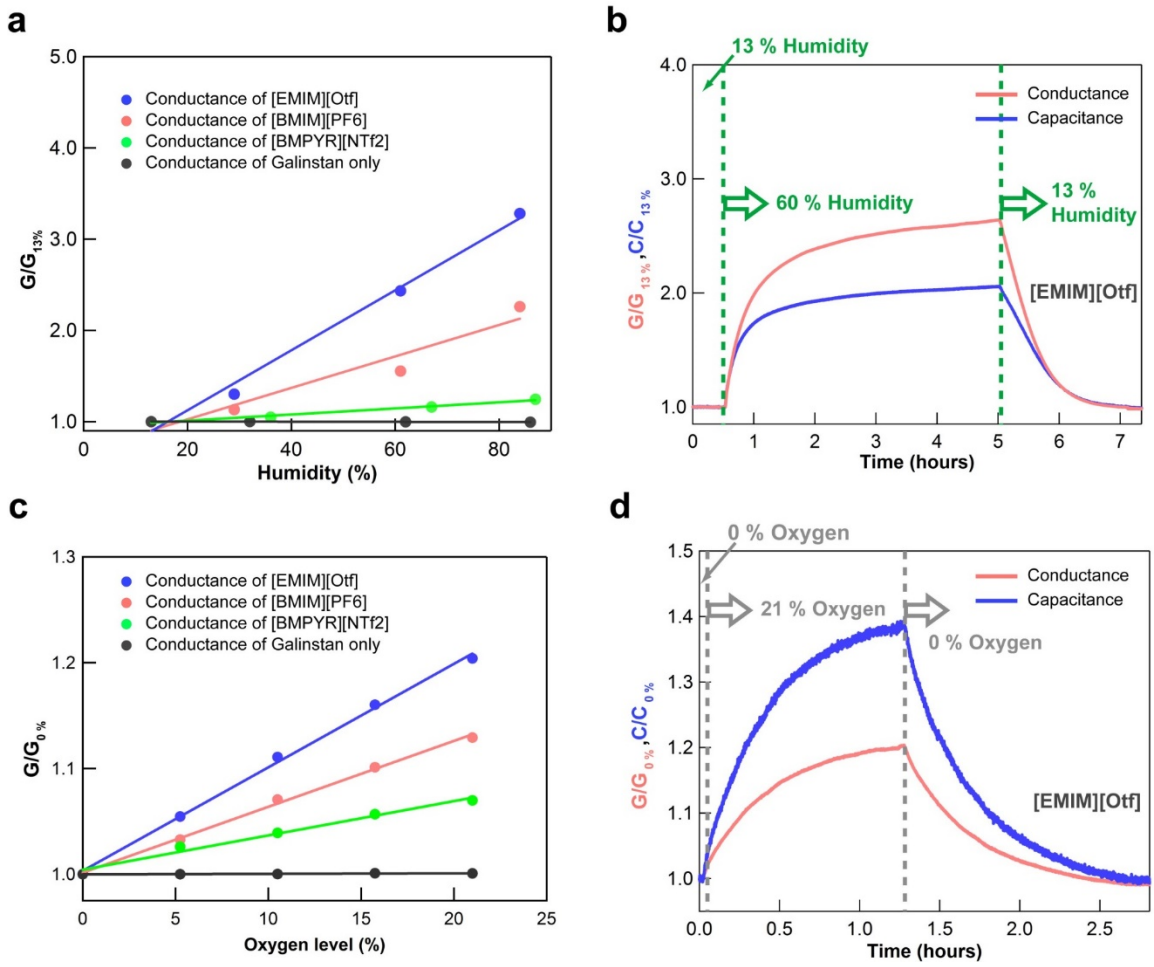


Figure 6 Liquid-state heterojunctions as oxygen and humidity sensors. **a.** Measured conductance of devices made with three different ionic liquids as a function of humidity. **b.** Measured conductance and capacitance of a sensor with [EMIM][Otf] as the active ionic liquid for one loading and unloading cycle between 13 % and 63 % humidity. The data points are normalized by the values at 13 % humidity and 25 °C ($G_{13\%}$ and $C_{13\%}$, respectively). **c.** Measured conductance of the sensor as a function of oxygen concentration. **d,** Measured conductance and capacitance of a sensor with [EMIM][Otf] as the active ionic liquid for one loading and unloading loop between 0 % and 21 % oxygen. The data points are normalized by the values at 0 % oxygen (100 % nitrogen) at 25 °C ($G_{0\%}$ and $C_{0\%}$, respectively).

3.2.6 Discussion

In conclusion, the work here presents a platform for exploring liquid-state devices based on "heterojunctions" of complementary liquids embedded in soft templates. Through modeling and experiments, we map the design parameters needed to enable formation of controlled liquid heterointerfaces, without intermixing. Given the inherent mechanical deformability of the liquid phase, the use of liquid-state device technology presents a natural platform for conformal electronics. Specifically, the work enables exploration of new devices that can undergo extreme levels of mechanical deformation without fracture or delamination that is often associated with solid-state materials. Moving forward, exploring the size scaling limits of the device may be of

interest depending on the targeted application. Specifically, in this work, the microfluidic channels used for the injection of the liquids were 31 μm thick and 500 μm wide. However, previous reports have demonstrated fabrication of liquid channels down to ~100 nm in height and width. Thus, it should be possible to scale down the all-liquid sensors to significantly smaller dimensions than those presented in this work. Furthermore, opportunities exist in exploring a wide range of liquid heterojunctions for fabricating various sensors and electronic device components, including diodes and transistors. Overall, the work presents an important step towards the potential realization of liquid-state electronic systems that offer new form factors and functionality.

3.2.7 Experimental and Theoretical Details

3.2.7.1 Preparation of the SU-8 Mold

SU-8 (SU-8 2075, MicroChem) was spin-coated onto a silicon handling wafer at 500 rpm for 5 seconds and then 2000 rpm for 30 seconds (Fig. 1a). The SU-8 was then baked at 90 °C for 10 minutes and patterned using photolithography with a transparency mask. After exposure, the sample was baked again at 90 °C for 10 minutes followed by development using propylene glycol monomethyl ether acetate (Sigma Aldrich). This process yielded SU-8 microchannel mold patterns (Fig. 1b) 31±2 μm high, measured via a 3D confocal laser microscope (Olympus LEXT OLS4000). To aid in the liftoff process of the PDMS, the SU-8 mold was then treated with trichloro(1H,1H,2H,2H-perfluorooctyl)silane (Sigma Aldrich) to prevent adhesion of PDMS to the silicon handling wafer.

3.2.7.2 Temperature Sensor Fabrication

PDMS (Sylgard 182, Dow Corning) mixed with a base to curing agent ratio of 13:1 was poured onto the SU-8 mold to a thickness of approximately 1 mm and cured on a hot plate at 90 °C for 10 minutes (Fig. 1c). After curing, the patterned PDMS was cut and peeled off from the SU-8 mold (Fig. 1d). On a separate clean glass slide, S1818 photoresist (MicroChem) was spin coated at a speed of 4000 rpm for 30 seconds and then baked on a hot plate at 90 °C for 90 seconds. PDMS mixed with the 13:1 base to curing agent ratio was then spun onto the slide at 500 rpm for 1 minute yielding a PDMS thickness of ~100 μm (Fig. 1e). The sample was then cured on a hot plate at 50 °C for 6 hours. This substrate, along with the PDMS substrate patterned using the SU-8 mold, were both exposed to an oxygen plasma (Diener Electronic Nano) at 120 W for 90 seconds and then bonded together (Fig. 1f). Galinstan (Rotometals) was injected into the microfluidic channels using a PHD 2000 syringe pump (Harvard Apparatus) at a speed of 25-1900 μL per minute (Fig. 1g). The ionic liquids, 1-Ethyl-3-methylimidazolium trifluoromethanesulfonate ([EMIM][Otf]), 1-Butyl-3-methylimidazolium hexafluorophosphate ([BMIM][PF6]), 1-Butyl-1-methylpyrrolidinium bis(trifluoromethylsulfonyl)imide ([BMPYR][NTf2]), or 1-Hexyl-3-methylimidazolium chloride ([HMIM][Cl]) (Sigma Aldrich), were then injected into the middle channel (Fig. 1h). To prevent bubble formation, the Galinstan and ionic liquid were injected soon after oxygen plasma treatment of the PDMS substrate so that the contact angles between the ionic liquid and PDMS were as small as possible. This allows us to obtain the highest possible capillary pressure for injection of the ionic liquid into the thin junction channels. Based on observations through a microscope, bubbles were not observed in the heterojunctions. It is expected that any small microbubbles that do form by chance will slowly diffuse out of the channels through the PDMS template, given the known permeability of

PDMS to air molecules[37]. Copper wire electrodes were inserted into the openings of the channel (Fig. 1i) which were then sealed off with a room temperature vulcanizing (RTV) silicone (RTV Sealant 734 Flowable Sealant, Dow Corning). Finally, acetone was used to remove the photoresist layer bonding the sample to the glass slide and the completed temperature sensor was peeled off (Fig. 1j)

3.2.7.3 Analysis of the Nyquist plot

The impedance of the devices were measured by a potentiostat (604C, CH instruments). The devices were measured in a two-electrode configuration, with the reference and counter electrode leads connected together. The Nyquist plot was measured at an applied DC bias of 0 V, with a 10 mV AC voltage superimposed. The measurement frequency ranged from 1 kHz to 100 kHz for [EMIM][Otf], and 1kHz to 10kHz for [BMIM][PF6] and [BMPYR][NTf2], respectively. A model of electrolyte resistance *R* and double layer capacitance *C* in series was used to fit the Nyquist Plot. To account for the nonideal behaviors of capacitance, a constant phase element was used instead of a capacitor.

3.2.7.4 Temperature sensing measurement

To measure the temperature dependence of the sensor, the fabricated device was put in an oven (Oven model 3511FS, Fisher scientific) at room temperature and the oven was turned on to the temperature set point after closing the oven door. The conductance and capacitance of the device were monitored using an Agilent B1500A semiconductor device analyzer as the temperature ramped up to the set point. To test the effect of stretching and twisting on device performance, the temperature sensor was mounted onto a homebuilt apparatus capable of both stretching and twisting the device. The conductance and capacitance of the device was monitored as the device was stretched by up to 30% and twisted by up to 60°. When doing the temperature dependence studies of the temperature sensor while under strain, the whole apparatus containing the strained device was placed in the oven and the conductance and capacitance were monitored as the oven temperature was increased.

3.2.7.5 Oxygen sensing measurement

O_2 was mixed with N_2 (99.998%) using two flowmeters to obtain the desired O_2 concentrations. The gases were flowed through a quartz tube containing the sensor with a total volumetric flow rate of 1 L/min. The humidity and temperature were maintained within $\pm 1\%$ and $\pm 1°C$, respectively, during the measurement. Electrical measurements were performed using the same methods as for temperature sensing.

3.2.7.6 Humidity sensing measurement

In order to control humidity, two air lines for dry air and air with high moisture content (obtained by bubbling dry air through a water bath) were connected to a quartz tube containing the liquid-state heterojunction sensor. The total volumetric flow rate of dry and moist air was maintained at 1 L/min using a flowmeter. The humidity was controlled by altering the ratio of dry and moist air. The temperature and humidity were monitored by using a commercial temperature/humidity sensor (EK-H5, SENSIRION). Electrical measurements were performed using the same methods as for temperature sensing.

3.2.7.7 Model construction

The model used to calculate the conductance and capacitance is a series connection of a resistor and a constant phase element (CPE) which has a power-law frequency dependence described by the equation[32]:

$$Z_{CPE} = Z_0 (i\omega)^{-\alpha} = \frac{Z_0}{\omega^{\alpha}}\left(cos\frac{\pi\alpha}{2} - isin\frac{\pi\alpha}{2}\right) \quad \text{(eq. 1)}$$

In this equation, ω is the AC frequency. Z_0 and α are positive constants. In this study, α was extracted from a Nyquist plot(Supplementary Figure S6, 7). Considering Z_{CPE}, the modified impedance is defined as follows:

$$Z = Z' + Z''i = R + \frac{Z_0}{\omega^{\alpha}}\left(cos\frac{\pi\alpha}{2} - isin\frac{\pi\alpha}{2}\right) \quad \text{(eq. 2)}$$

Based on eq. S2 and the measured impedance, we can get Z_0.

$$Z_0 = (-Z'') \times \frac{\omega^{\alpha}}{sin\frac{\pi\alpha}{2}} \quad \text{(eq. 3)}$$

Using Supplementary Equation 2 and 3, the modified capacitance (C) and conductance(G) are as follows;

$$C = \frac{\omega^{\alpha-1}}{Z_0 sin\frac{\pi\alpha}{2}} \quad \text{(eq. 4)}$$

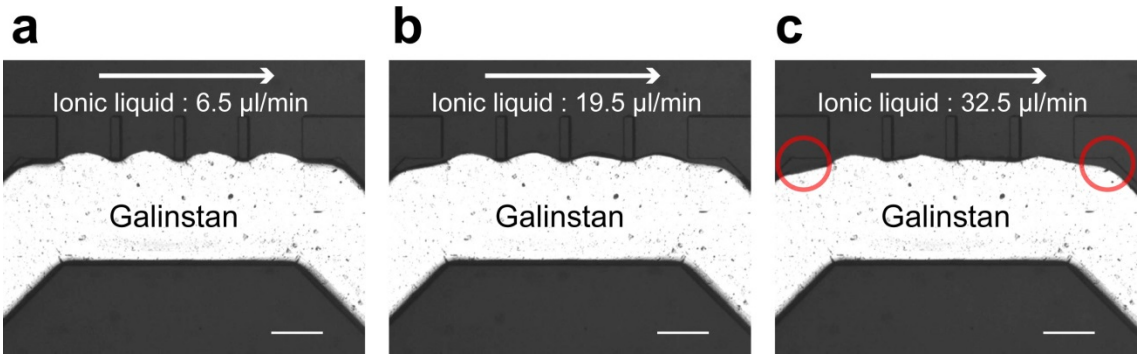
$$G = \left(Z' - \frac{Z_0}{\omega^{\alpha}} cos\frac{\pi\alpha}{2}\right)^{-1} \quad \text{(eq. 5)}$$

3.2.7.8 Resistance change due to strain.

When stretching by 30% perpendicular to the axis of the junction channels, the length of the channels decreased by 4.9% while the width increased by 25% (Supplementary Figure S9 **a** and **c**). On the other hand, while stretching 30% along the axis of the junction channels, the length increased by 6.7% while the width dropped by 2.3% (Supplementary Figure S9 **b** and **d**). Assuming the volume of the ionic liquid is kept constant, this means that the height of the channel decreased by 15.9% and increased by 4.1% for stretching perpendicular to and along the junction channel axis, respectively.

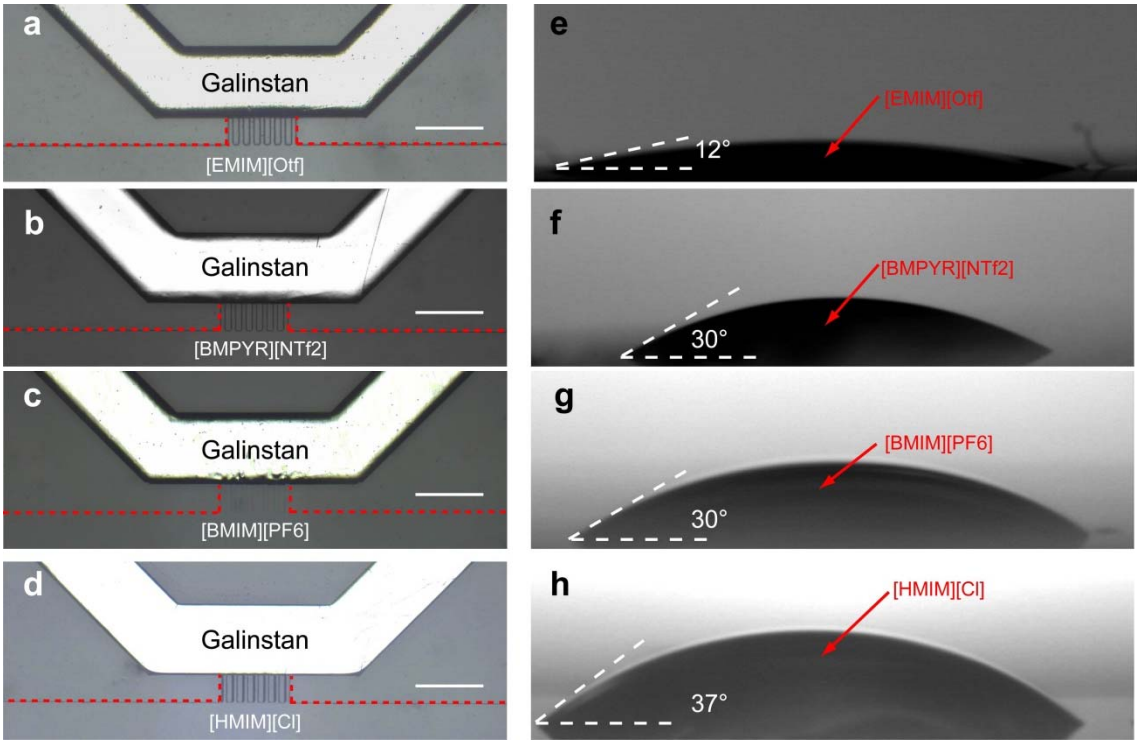
In our study, the measured conductance is composed of the resistance of the junction channels in series with the resistance of the main ionic liquid channel. The size of the main ionic liquid channel (500 μm length and 19500 μm width) is significantly larger than that of the junction channels (channel length and width of 200 μm and 30 μm, respectively). Therefore, we can assume that the change in conductance of our device is dominated by the change in dimensions of the junction channels. Using a normal geometric conductance model where the conductance is proportional to the width and height and inversely proportional to the length, the expected change in conductance would be a 10.5% increase when stretching perpendicular to the junction channel axis and a 12.3% decrease when stretching along the junction channel axis, which is in line with our electrical measurements using [EMIM][Otf].

3.2.7.9 Effect of ionic liquid injection velocity on junction interface.



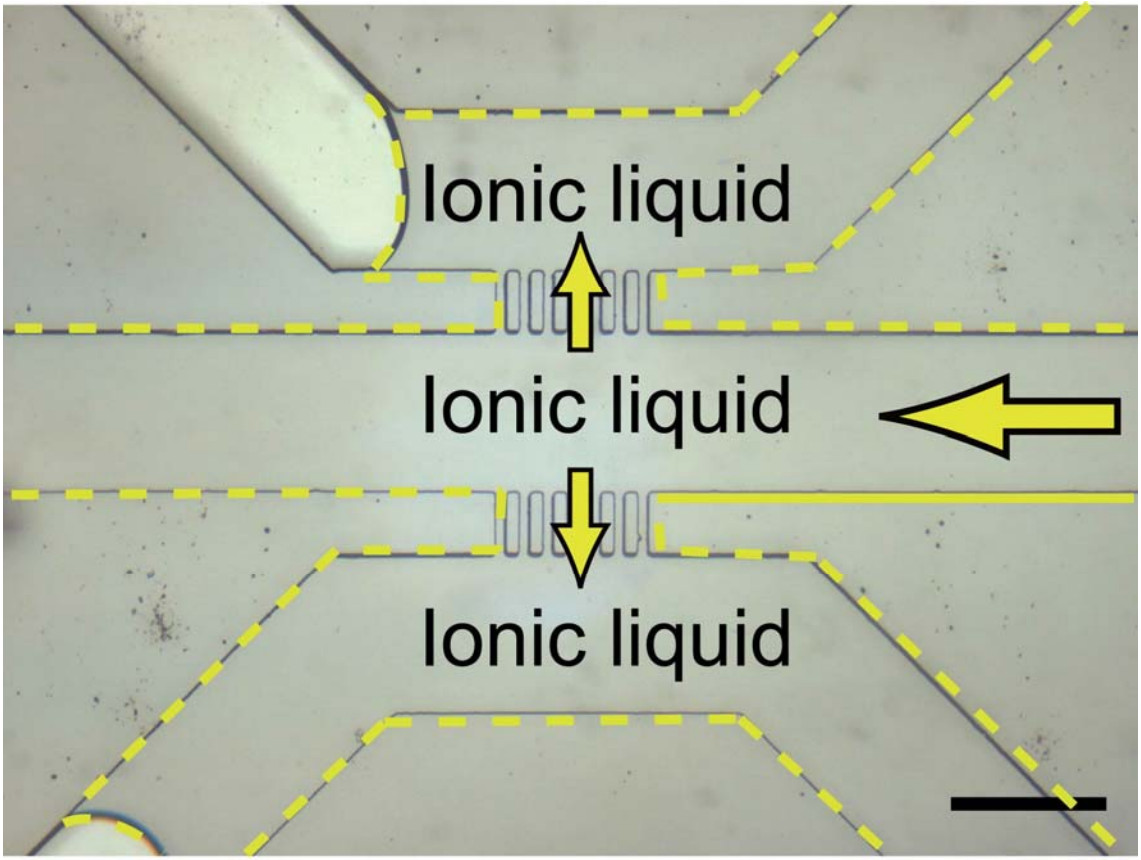
Supplementary Figure S1. The volumetric flow rate of ionic liquid is **a.** 6.5, **b.** 19.5, and **c.** 32.5 µm/min. As the ionic liquid flow rate is increased to >32.5 µL/min, it begins to invade the Galinstan channels. Here, the junction channel width is 250 µm (scale bar, 250 µm).

3.2.7.10 Contact angle and heterojunction formation of different ionic liquids



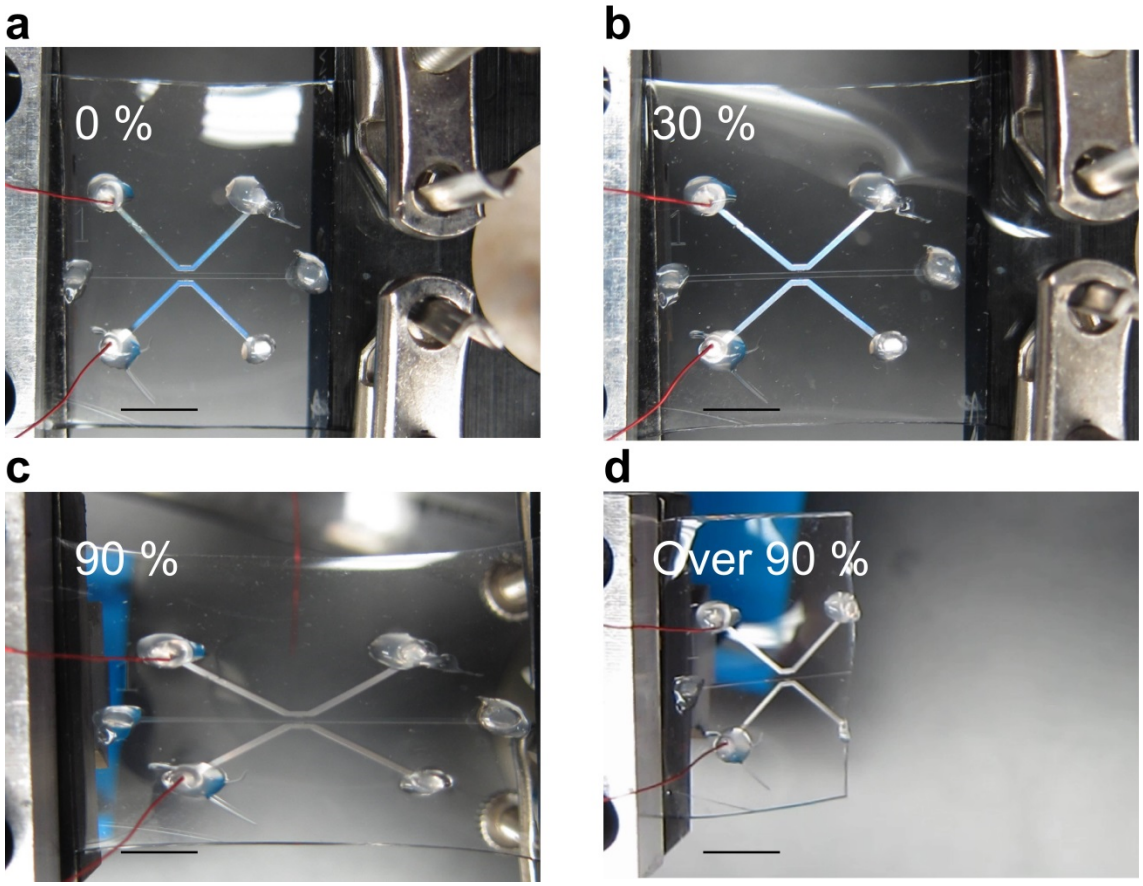
Supplementary Figure S2. Optical microscope images of fabricated devices using a, [EMIM][Otf]; b, [BMPYR][NTf2]; c, [BMIM][PF6]; and d, [HMIM][Cl] as the active channel ionic liquid. The corresponding contact angle images for the four ionic liquids on oxygen plasma-treated PDMS substrates are shown in **e-h**, respectively. In all cases, the contact angle between the ionic liquids and PDMS were less than 90°, thus enabling the successful fabrication of the liquid heterojunction (scale bar, 500 μm). Note that the viscosity of [EMIM][Otf], [BMIM][PF6], [HMIM][Cl] and [BMPYR][NTf2] at 298K are reported to be 45, 74, 213, and 7826cP, respectively[29]. These results show that the viscosity of the ionic liquid does not affect the junction formation.

3.2.7.11 Importance of liquid injection order



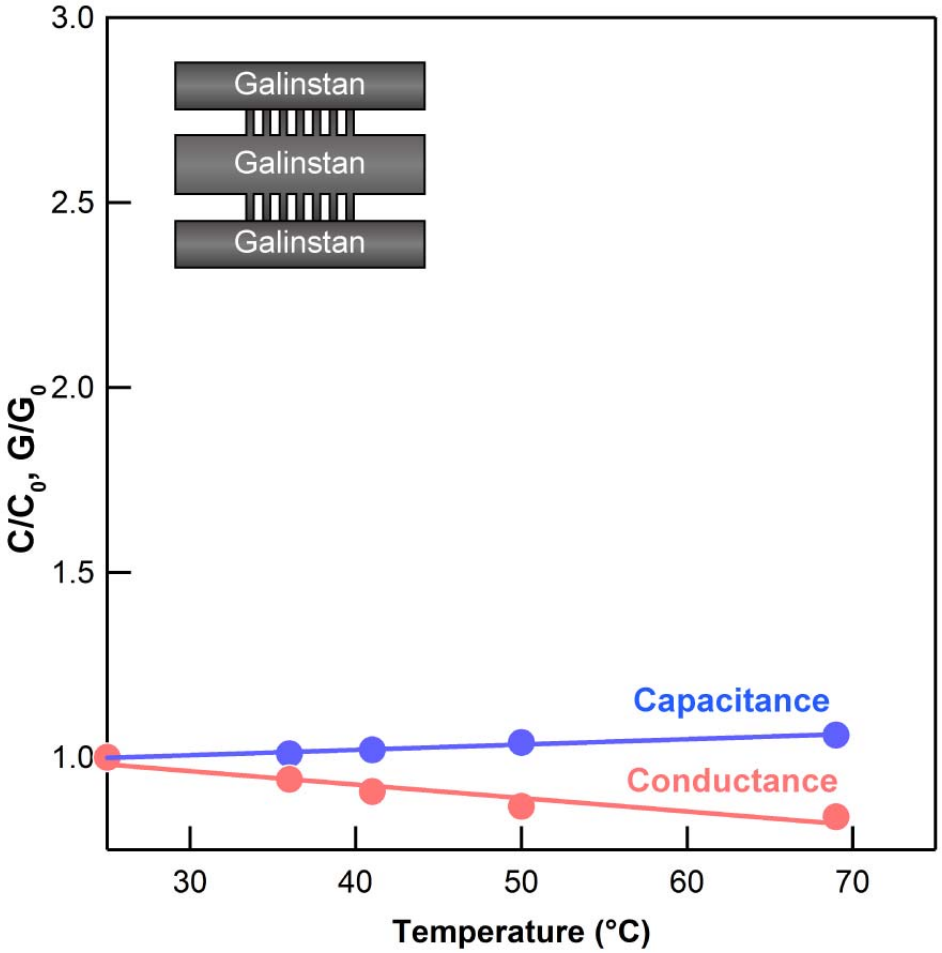
Supplementary Figure S3. Optical image of a failed device for which [EMIM][Otf] was injected before Galinstan. The [EMIM][Otf] penetrates into all patterned channels due to capillary pressure. (scale bar, 500 μm)

3.2.7.12 Stretching limit of the liquid heterojunction devices.



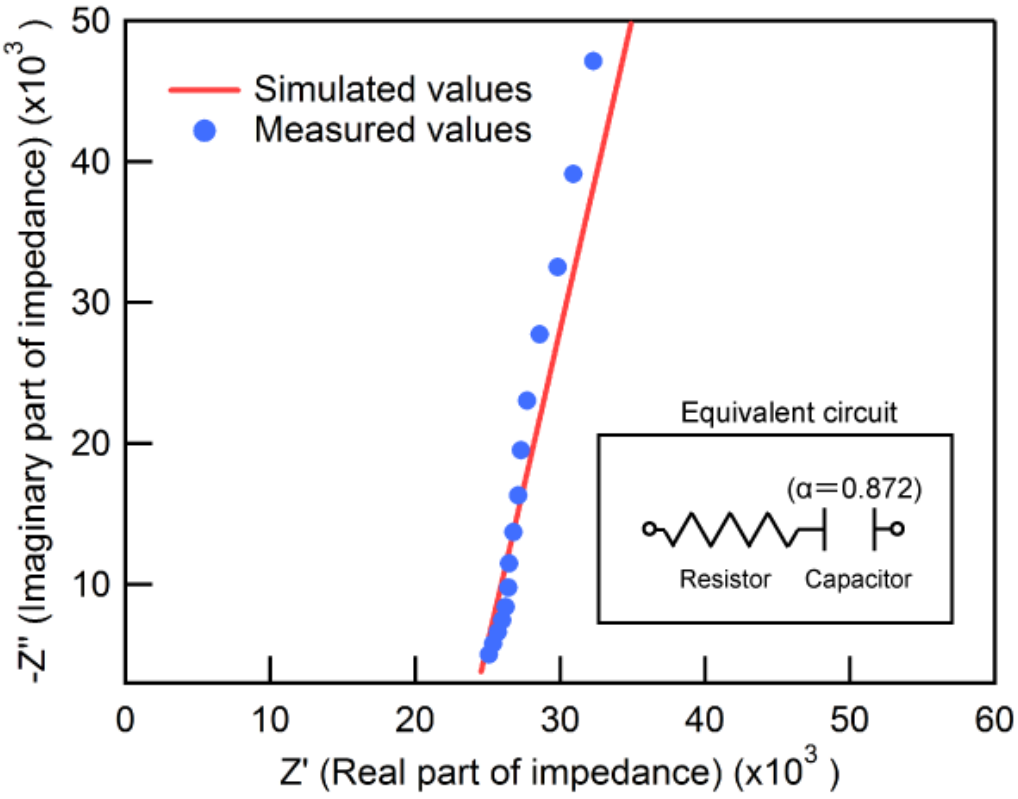
Supplementary Figure S4. Optical images of a device **a,** when relaxed, and stretched by **b,** 30%, **c,** 90% and **d,** more than 90% perpendicular to the axis of the junction channels. Above90% strain, the PDMS substrate broke while the liquid junction maintained its integrity (scale bar, 5 mm).

3.2.7.13 Galinstan control device



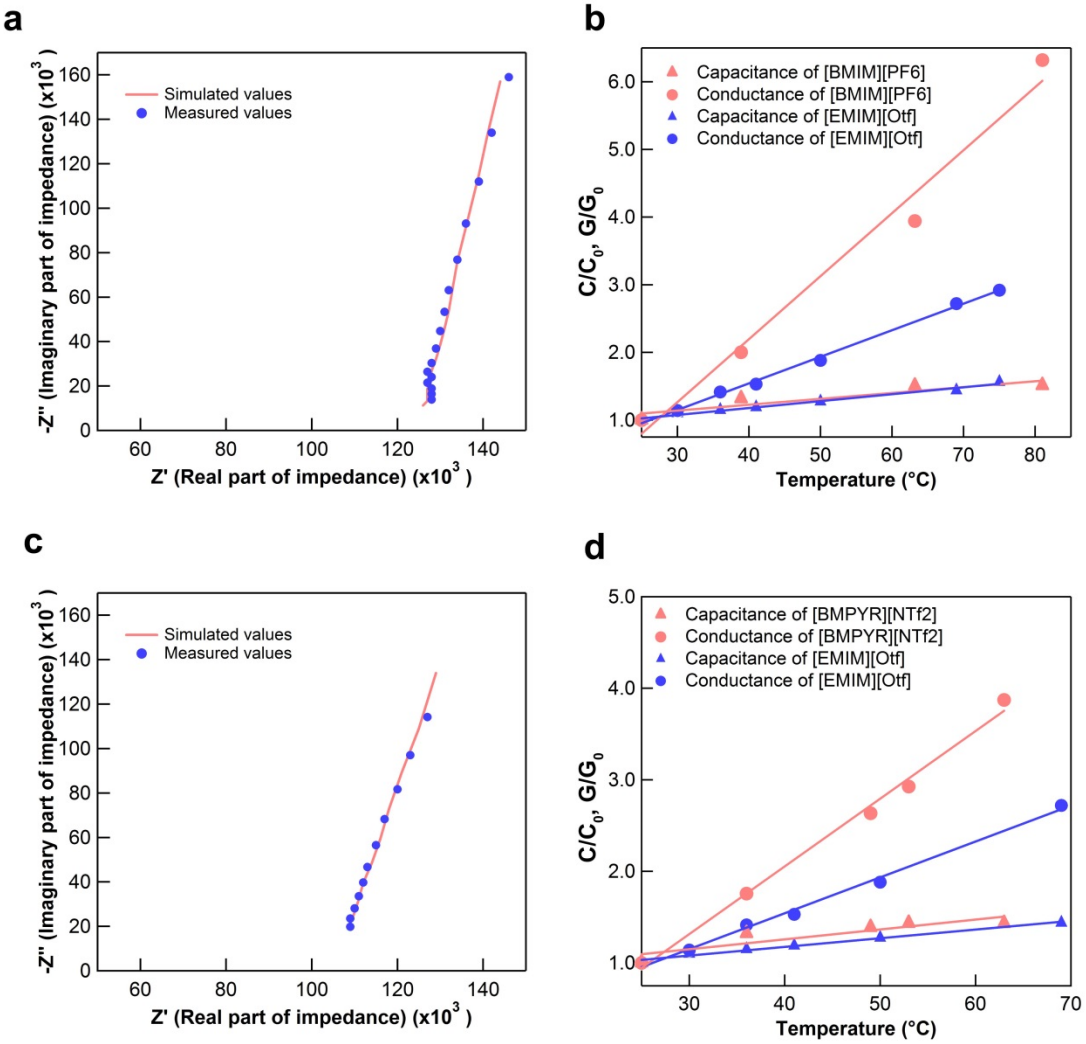
Supplementary Figure S5. Control device with only Galinstan, showing minimal dependence on temperature.

3.2.7.14 Nyquist Plot



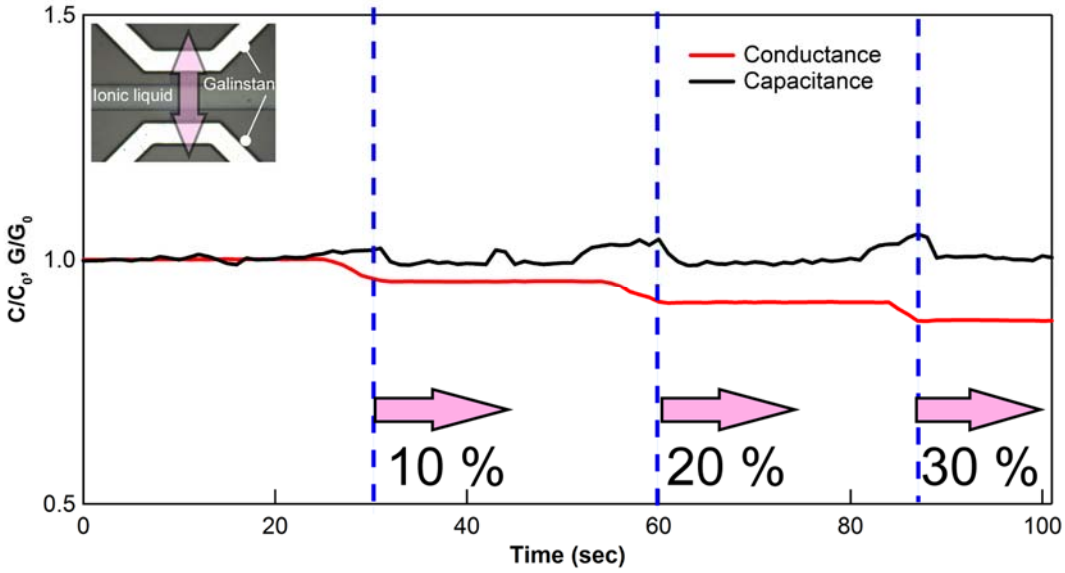
Supplementary Figure S6. Nyquist plot of the liquid heterojunction sensor using [EMIM][Otf] and Galinstan.

3.2.7.15 Temperature sensing of liquid-state devices using [BMIM][PF6] and [BMPYR][NTf2] as the active channel ionic liquids.



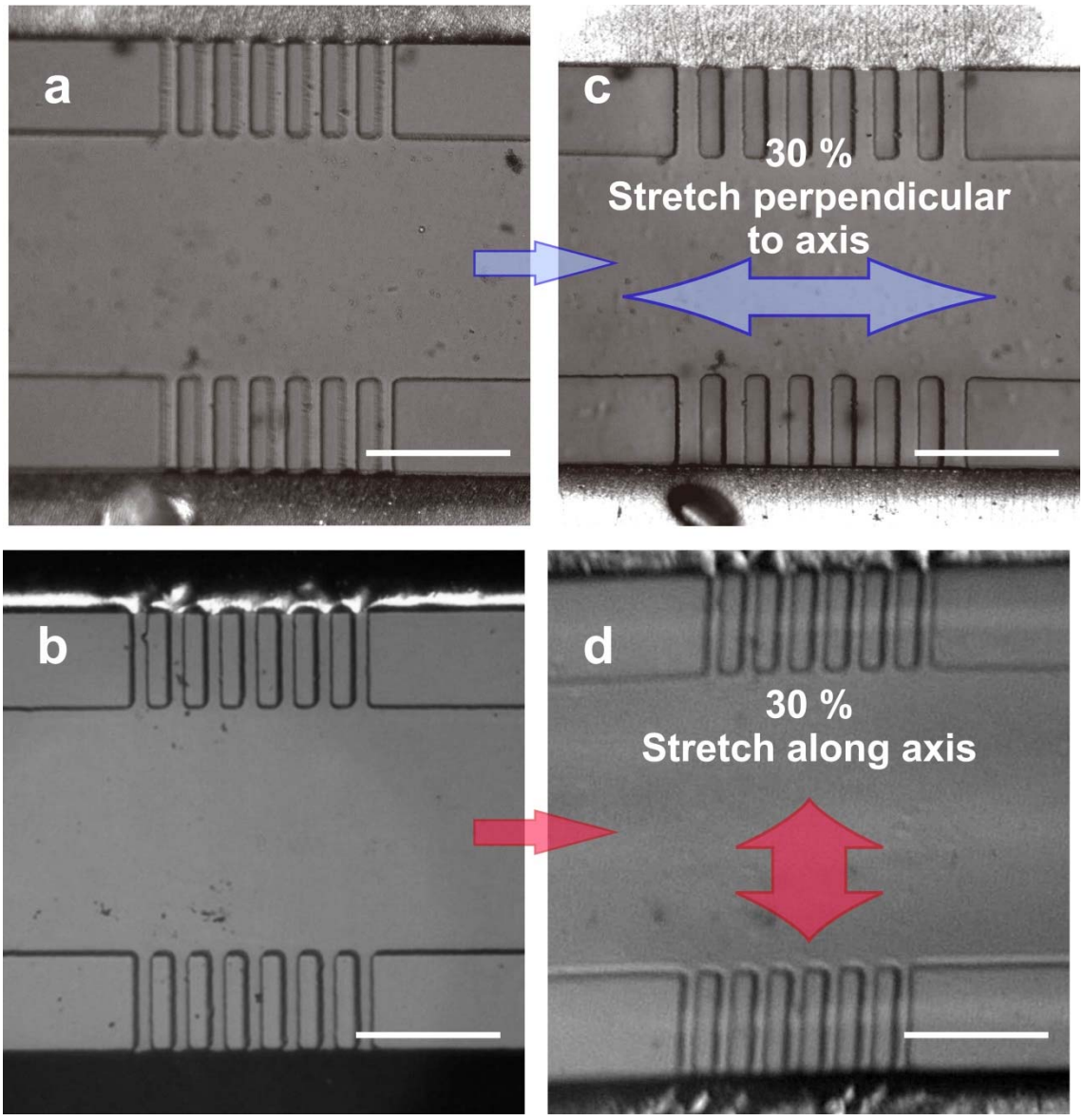
Supplementary Figure S7. a, Nyquist plot of a sensor using [BMIM][PF6], and **b,** the corresponding conductance and capacitance as a function of temperature. **c,** Nyquist plot of a sensor using [BMPYR][NTf2], and **d,** the corresponding conductance and capacitance as a function of temperature. The data points are normalized by the respective values of the devices at 25 °C (G_o and C_o, respectively).

3.2.7.16 Sensor response to strain along junction channel axis



Supplementary Figure S8. Conductance and capacitance of a liquid-state heterojunction sensor using [EMIM][Otf] in the active channel while stretched by 30% along the junction channel axis at 25 °C. G_o and C_o are the conductance and capacitance, respectively, of the device while not stretched at 25 °C.

3.2.7.17 Stretching of sensor along different axis



Supplementary Figure S9. a, and **b,** Optical microscope images of liquid-heterojunction devices with no applied strain. Optical images of the same devices when stretched by 30% **c,** perpendicular to and **d,** along the axis of the junction channels(scale bar, 300 μm).

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Chapter 4 Advancements in Carbon Nanotube Electronics for Flexible Applications

4.1 Introduction

In the previous chapter, the usage of liquid metals and ionic liquids for creating flexible electronic sensors was described. While liquid-state electronics does offer extreme flexibility and deformability, it is still necessary to utilize conventional solid state materials for more complicated systems. For flexible electronics, there are two major constraints in terms of materials which can be used. The first is the low thermal budget of flexible substrates, which are typically polymers. This limits the maximum processing temperature to be somewhere between 100-300 °C, depending on the choice of substrate. The other major constraint is that the system must be able to perform well under strain when the devices are flexed and bent.

In this regard, one promising materials system for enabling flexible electronics is solution processed carbon nanotubes (CNTs). Purified semiconducting nanotube solutions can be dropcast at room temperature to form a monolayer network of nanotubes. In addition, solution processed CNT based thin film transistors (TFTs) can have mobilities greater than 50 $cm^2/V\ s$, which is one of the highest for room-temperature processed materials systems. In this chapter, two main aspects of CNT TFTs will be discussed. First, a doping method for enabling both n-type and p-type CNT-TFTs via chemical field effect will be introduced to allow for the fabrication of CMOS circuits. In addition to CNTs, this doping method is demonstrated on other materials systems as well, in particular the two dimensional material WSe_2. The second half of this chapter will cover the usage of CNT-TFTs for printed electronics using gravure printing. Gravure printing can enable high throughput processing on the order of meters per minute with large area substrates, making it an ideal method for low cost disposable electronics as well as large format (meter-scale) flexible electronics.

4.2 Fixed Charge Doping of CNTs for CMOS Applications

The following subchapter has been previously published in a similar format in:
T.-J. Ha, K. Chen, *et al*. Highly uniform and stable n-type carbon nanotube transistors by using positively charged silicon nitride thin films, *Nano Letters*, **15,** 392–397, (2015).

Single-walled carbon nanotubes (SWCNTs) are promising electronic materials for thin film transistors (TFTs) due to their excellent electrical properties[1–3] and ease of processing for large scale production[4–12]. In particular, solution processed semiconductor-enriched nanotubes have been configured as high performance TFTs on mechanically flexible[10,13] and rigid substrates[5,14,15] with high ON/OFF current ratios[16] and carrier mobilities[1]. Given the high uniformity of the process[5], system-level applications have been explored, including active-matrix backplanes for driving flexible organic light-emitting diode displays[13,14,17] and large-area sensor networks capable of mapping external stimuli[18]. Despite the tremendous progress in this field, to date, most works have focused on *p*-type TFTs given the difficulty to form stable and robust electrical contacts to the conduction band of carbon nanotubes. However, for many practical applications, *n*-type transistors in addition to their *p*-type counterparts are needed to enable complementary metal-oxide-semiconductor (CMOS) circuits, thus lowering power consumption[19] which is critical for large area systems[1919][19]. In this regard, a wide range of schemes have been explored in the past. A few examples include the use of low work function metal contacts[20–23] for enhanced electron injection and surface charge transfer doping by electron withdrawing polymers[24,25] or molecular species[26,27]. However, many of these approaches suffer from insufficient air stability for reliable long term operation[19] although significant improvements have been made through encapsulation[28,29]. As an alternative, metal oxide encapsulation[30–32] has been recently reported to electron-dope nanotubes, presenting one potentially promising approach.

4.2.1 Fixed Charge in SiN_x

Here, we explore "physicochemical field-effect" *n*-doping of carbon nanotubes by silicon nitride (SiN_x) thin films. SiN_x deposited by plasma-enhanced chemical vapor deposition (PECVD) is well known to exhibit positive fixed charges[33,34,35]. These fixed charges arise from $^{+}Si{\equiv}N_3$ dangling bonds within the nitride, known as K^+ centers[36] and the sheet density can be controllably tuned to between 10^{11}-10^{13} cm^{-2} by changing the deposition conditions or conducting post deposition treatments[34,37]. This property of SiN_x has been used in the past to induce surface band bending of Si solar cells[38–40], thus providing a robust surface passivation scheme for reduced surface recombination of minority carriers. More recently, we adopted this concept to controllably *n*-dope 2-D semiconductors, such as WSe_2[35]. Unlike surface charge transfer doping that is often explored for nanoscale inorganic and organic materials, the fixed charges in SiN_x induce field-effect doping of the underlying semiconductor. Since the fixed charge density can be as high as 10^{13} cm^{-2}, high doping levels at the surface of the underlying semiconductor can be achieved. Here, by depositing SiN_x thin films on top of carbon nanotubes, we are able to obtain *n*-type transistors with comparable mobilities and ON currents as their *p*-type counterparts, and ON/OFF current ratios of up to 10^6. In particular we demonstrate *n*-type transport behavior for both single nanotube and networked transistors with high yield and long term stability in air. We also demonstrate the compatibility of our approach for CMOS logic by fabricating a proof-of-principle inverter based on *p*- and *n*-type SWCNT-TFTs on the same substrate through patterned deposition of SiN_x.

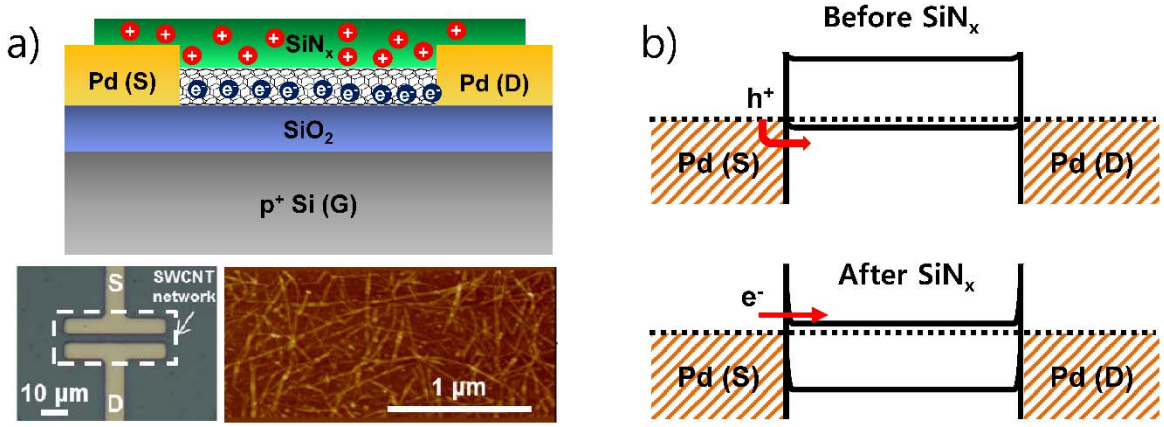


Figure 1: SiN_x field-effect doping of carbon nanotubes. a) Cross sectional schematic of a SWCNT TFT *n*-doped with a thin film of SiN_x (top). An optical microscope image of a representative transistor (bottom left) and an AFM image of the SWCNT network inside the channel (bottom right) are also shown. b) Qualitative band diagram of a nanotube transistor in the ON-state before (top) and after (bottom) SiN_x field-effect doping.

The effect of SiN_x on the electrical properties of nanotubes is first examined by fabricating TFTs based on random networks of semicondor-enriched SWCNTs. SWCNT TFTs (Fig. 1a) are fabricated on a degeneratly *p*-doped silicon substrate which functions simultaneously as the back gate electrode with a 50 nm thick thermally grown silicon dioxide (SiO_2) serving as the gate dielectric. After cleaning in acetone, methanol and isopropyl alcohol, the SiO_2 surface was treated with an oxygen plasma at 120 W for 2 minutes. Poly-L-lysine (0.1% w/v in H_2O, Sigma Aldrich) solution was then drop-cast onto the SiO_2 for 5 minutes and subsequently rinsed in deionized water to functionalize the surface for SWCNT deposition. Then, 99% semiconducting SWCNT suspension (NanoIntegris Inc.) was deposited by drop-casting for 10 minutes followed by a rinse with DI water to remove the excess nanotube solution. This results in a densely packed SWCNT network with a density on the order of ~30-60 nanotubes per square micron on the poly-L-lysine treated SiO_2 surface as shown in the atomic force microscope (AFM) image of Figure 1a. Assuming an average diameter of 1.4 nm and length of 1 μm, this corresponds to a surface coverage area of ~4-9%. Source/drain (S/D) contacts were patterned by photolithography, electron-beam evaporation of Ti/Pd (0.5/40 nm) thin films, and lift-off of the resist in acetone. Subsequently, the SWCNT network was patterned to confine them to the channel region (i.e., space between the S/D electrodes) by using photolithography and O_2 plasma etch. To dope the samples, SiN_x was deposited via PECVD using an Oxford Plasmalab 80plus PECVD System operating at a frequency of 13.56 MHz. The deposition process was kept the same for all runs with a process temperature of 150 °C, power density of 40 mW/cm^2, and a pressure of 900 mTorr with 10% SiH_4 (diluted in Ar) at 100 sccm and NH_3 at 30 sccm. As the K^+ centers are expected to reside within the first 20 nm of the SiN_x film interface[40], a deposition time of 340 seconds was used to obtain a film thickness of ~100 nm for all samples to ensure high uniformity from device-to-device and batch-to-batch. No change in the electrical properties was observed for SiN_x thicknesses of >100 nm (Supplementary Fig. S1).

Figure 1b shows the qualitative band diagrams for a SWCNT device before and after SiN_x deposition, depicting the contact properties for charge injection. It should be noted that polarity (*n*- versus *p*-type) of transistors is governed by the properties of the electrical contacts rather than the channel doping type. Specifically, the source contact determines which carrier type can be injected into the channel. In the ON-state of a *p*-type transistor, the source contact provides injection of holes into the channel while electrons are injected for the case of an *n*-type device. Before SiN_x deposition, the Schottky barrier (SB) height to the valence band of SWCNTs is small due to the use of high work function Pd S/D contacts, thus allowing for efficient hole injection while presenting a large SB height to the conduction band for electron injection. Thereby, as-made devices exhibit *p*-type characteristics. After SiN_x deposition, the positive fixed charges within SiN_x are expected to induce field-effect doping of the underlying SWCNTs. By using the optimal stoichiometry, the fixed positive charge density in SiN_x, corresponding to the electron doping level in SWCNTs, can be high enough to sufficiently thin the SBs to the conduction band, thereby allowing for efficient electron tunneling from the contacts into nanotubes. Thus, *n*-type transport can be expected for SiN_x coated devices.

4.2.2 Experimental Results

Figures 2a-b show the transfer (drain current, I_{DS}, versus gate voltage, V_{GS}) and output (drain current, I_{DS}, versus drain voltage, V_{DS}) characteristics of a representative SWCNT TFT with a channel length and width of 4 μm and 50 μm, respectively. The device is electrically measured before and after SiN_x deposition. Clear polarity conversion from *p*- to *n*-type transport is observed upon SiN_x deposition. The electrical properties are nearly symmetric for both cases with the ON-current for the *n*-channel transport being ~2x lower than that of the *p*-channel prior to SiN_x. The linear behavior of the output characteristics at low V_{DS} (Fig. 2b) for the *n*-TFT suggests efficient injection of electrons at the source contact, which is facilitated by sufficient thinning of the SBs by SiN_x doping as depicted in the band diagram of Fig. 1b. At the same time, the doping level is still at a level to allow for gate modulation of the conductance of ultrathin nanotubes with $I_{ON}/I_{OFF}\sim10^4$ (Fig. 2a). As a result, high performance *n*-type TFTs are obtained.

Importantly, the obtained *n*-type TFTs exhibit excellent air-stability. Figure 2c shows the transfer characteristics of a device immediately after SiN_x deposition as well as after 15 and 30 days in ambient air. Owing to the robustness of the silicon nitride, the device is highly stable in air without any noticeable change in the electrical properties. This is in distinct contrast to the surface charge transfer doped nanotubes obtained by deposition of molecular[26] species on the surface. In addition to air stability, the devices also exhibit similar levels of stability when stressed under device operation conditions (i.e., bias stressing) compared to their undoped counterparts (Supplementary Fig. S2). Such stability is essential for any practical device technology and presents an important advance in the field of carbon nanotube electronics. The use of inorganic nitride rather than organic species presents a more robust platform for the fabrication of complex systems over large-areas, where multiple process steps are required.

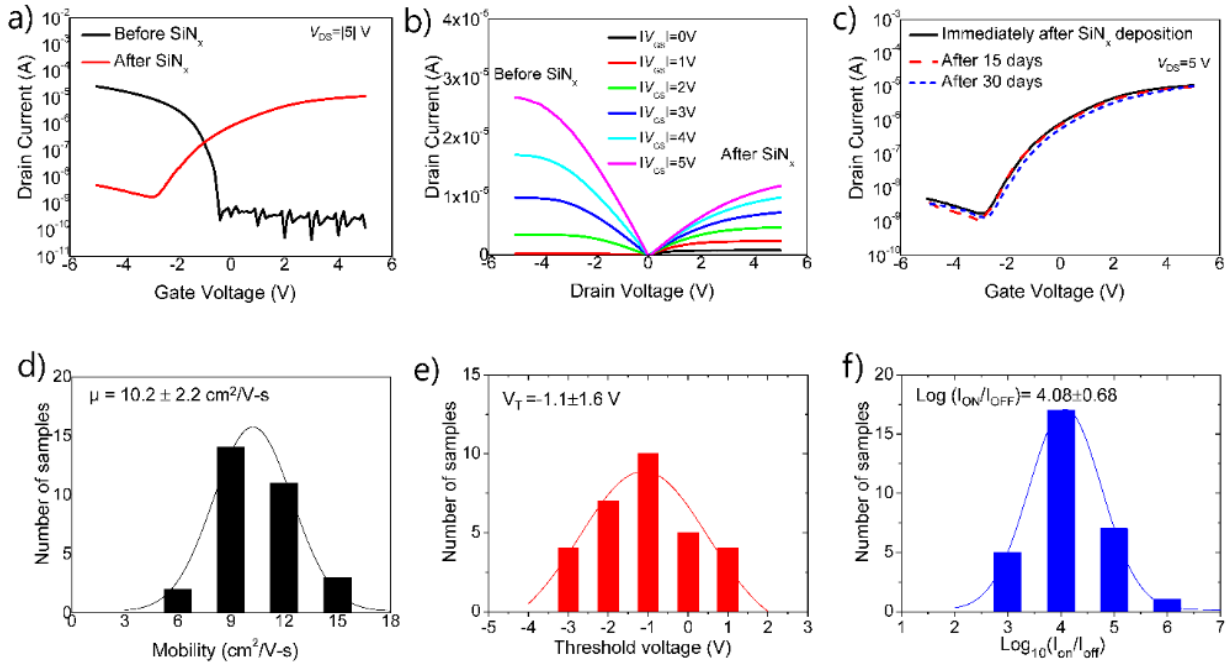


Figure 2: SWCNT *n*-type TFTs. a) Transfer and b) output characteristics of a representative SWCNT TFT (gate length of 4 μm and width of 50 μm) before and after SiN_x deposition. c) Transfer characteristics of an *n*-type TFT immediately after SiN_x deposition (solid black curve), as well as after 15 (dashed red curve) and 30 days (dashed blue curve), showing virtually no change in performance. Histograms of the d) electron mobility, e) threshold voltage, and f) log of the ON/OFF current ratio for 30 *n*-type TFTs.

The uniformity of SiN_x doping, and the enabled devices, is essential for exploring practical applications. The electrical properties of 30 SWCNT TFTs coated with SiN_x are measured and analysed. The average and standard deviation of mobility, threshold voltage and log ON/OFF current ratio are extracted as 10.2±2.2 cm^2/V-s (Fig. 2d), -1.1±1.6V (Fig. 2e) and 4.08±0.68 (Fig. 2f), respectively. Notably, the ~20% variation in mobility of our *n*-type TFTs is similar to that of the as-made *p*-type TFTs[13], suggesting that SiN_x field-effect doping does not induce further device-to-device variation. The obtained device uniformity is respectable given that the fabrication processing was performed in an academic laboratory, and yet sufficient for exploring certain system-level applications, such as active-matrix back-planes for driving sensor arrays[18] or displays[13].

The effect of metal contacts on the electrical properties of SiN_x coated SWCNT TFTs is also characterized. TFTs with Pd, Au, Al, and Ni as the S/D contacts are fabricated. In all cases, *n*-type transistor behaviour is obtained regardless of the metal contact choice (Supplementary Fig. S3). However, Pd contacted devices exhibit the highest ON-state current densities, corresponding to the lowest contact resistance for electron injection after SiN_x deposition. Although Pd has the highest work function among the metals explored here and thus results in the largest SB height for electrons, it still provides the lowest contact resistance for electron injection after doping with SiN_x. Pd has been shown previously to exhibit one of the lowest contact resistances to metallic nanotubes due to its strong wettability with SWCNTs[2,41,42]. Given that electron injection in SiN_x coated nanotube TFTs is obtained by tunnelling through the

thinned SBs at the contacts rather than thermionic emission over the barrier, the contact resistance is largely dependent on the width of the SBs and the interface quality (i.e., metal wettability[41,42]). While the former depends on the doping concentration, the latter depends on the choice of the metal contact. In this regard, similar to the case of metallic nanotubes, Pd offers the best interface with SWCNTs[26,43].

SiN_x stoichiometry affects the obtained fixed charge density[35]. Film stoichiometry and hydrogen content were determined by Rutherford backscattering spectrometry (RBS) and hydrogen forward scattering (HFS) using a 2.79 MeV alpha beam. RBS measurements were carried out at a backscattered angle of 165°. Quantitative hydrogen profiling was performed by HFS in a forward scattering geometry with the detector positioned at 150° with respect to the incident beam. The sample was tilted so that the sample normal made a 75° angle with the incident beam and a 13 μm thick Mylar foil was placed in front of the detector to stop the scattered alphas. The collected spectra were analyzed using the SIMNRA software code[44]. From RBS (Fig. 3a) and HFS measurements (Fig. 3b), we observed that SiN_x films are hydrogenated with a hydrogen areal density of 2.75×10^{18} atoms/cm^2 corresponding to a film stoichiometry of $Si_{0.39}N_{0.35}H_{0.26}$. This composition is in line with literature for the deposition parameters used[45].

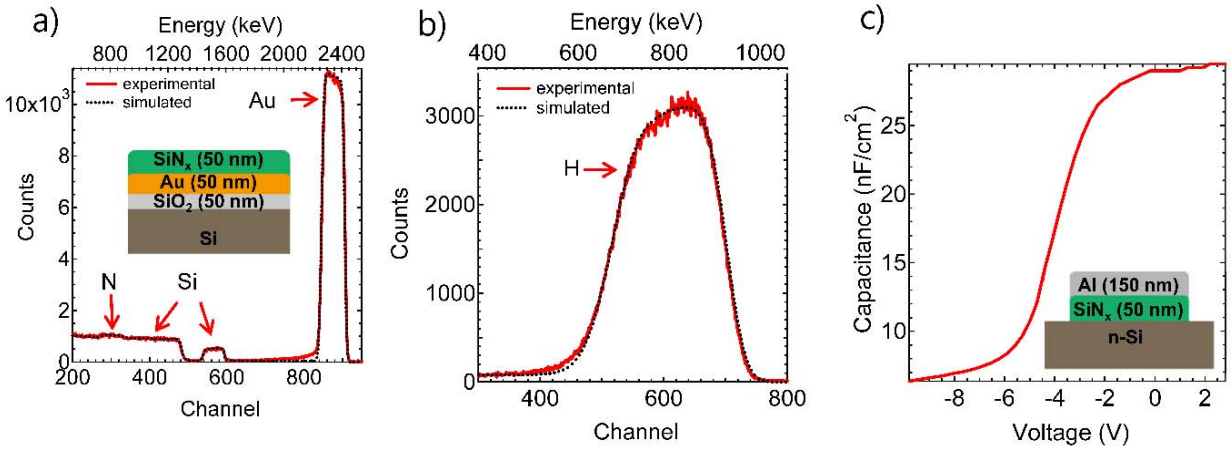


Figure 3: Material characterization of SiN_x thin films. a) RBS spectrum of SiN_x deposited on Au on a Si/SiO_2 wafer. b) Hydrogen distribution within the sample obtained from hydrogen forward scattering. The simulated fit to the experimental data from SINMRA codes yields a stoichiometry of $Si_{0.39}N_{0.35}H_{0.26}$. c) Capacitance-voltage measurement of the MIS structure shown in the inset.

To determine the fixed charge density within this nitride film, capacitance-voltage (*C-V*) measurements were carried out on a metal-insulator-semiconductor structure of Al, PECVD SiN_x and *n*-type Si (resistivity of 10-30 Ω·cm) as shown in Figure 3c. The device area is ~650×650 μm^2. The fixed charge density, Q_F can be extracted from the flatband voltage of the device using the equation $Q_F = C_{SiN_x}(\phi_{MS} - V_{FB})/q$ where C_{SiN_x} is the accumulation capacitance, ϕ_{MS} ~ -0.23 V is the work function difference between Al and the Si wafer, q is the elemental unit of charge, and V_{FB} is the flatband voltage. A V_{FB} of -4.4 V was extracted from the second derivative of the measured *C-V* plot, corresponding to the peak of $d^2(1/C_{SiN_x}^2)/dV^2$. Using this analysis, the fixed charge density in the nitride is ~7×10^{11} cm^{-2}, in line with the reported values in literature[45]. This fixed charge must be compensated by the carbon nanotube film with an

effective coverage area of 4-9% as approximated via AFM images. Assuming that the film is approximately a monolayer of SWCNTs with average diameter of 1.5 nm, the doping level induced by the silicon nitride fixed charge is on the order of 5×10^{19}-1×10^{20}cm^{-3}.

Given the near symmetric electrical properties of *n*- and *p*-type SWCNT TFTs and high device-to-device uniformity for both polarities, CMOS circuitry can be explored. As a proof-of-concept, a CMOS inverter using a *p*-type TFT (i.e., without SiN_x) and an *n*-type TFT obtained by SiN_x coating is fabricated as schematically illustrated in Figure 4a. Patterned SiN_x deposition was obtained during PECVD by using a shadow mask, thus providing a simple and facile approach for fabricating *p*- and *n*-type SWCNT-TFTs on the same substrate. Figure 4b shows the transfer characteristics of the CMOS inverter, exhibiting a maximum DC gain of ~6.2 at an operation voltage of 4 V with a noise margin of 1.68 V. In the future, more sophisticated CMOS circuits can be obtained by fabricating transistors with local back-gates.

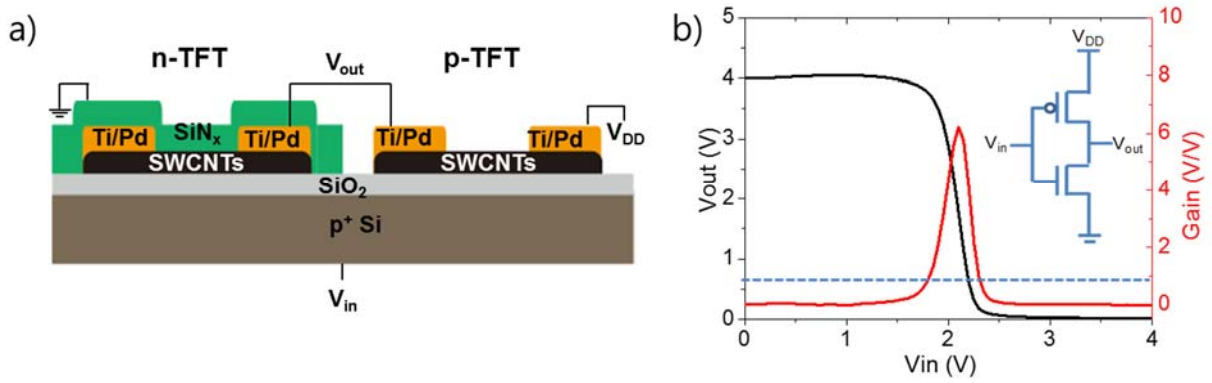


Figure 4: a) Cross sectional schematic of a CMOS inverter fabricated by connecting *n*- and *p*-type nanotube TFTs on the same substrate as obtained by patterned deposition of SiN_x thin films. b) Transfer characteristics of a CMOS nanotube inverter showing a gain of ~6.2.

SiN_x field-effect doping is also tested on single nanotube devices in addition to the random network TFTs discussed above. Single SWCNT FETs were fabricated by spin-coating the semiconductor-enriched nanotube suspension onto the poly-L-lysine modified SiO_2, resulting in a low density of assembled nantoubes on the surface. AFM was used to map the surface and locate inividual SWCNTs in respect to pre-fabricated alignment marks. Pd S/D contacts were subsequently fabricated on individual SWCNTs using electron-beam lithography. Figure 5a and b show the optical and AFM images of a device consisting of a single tube (diameter, ~1.4 nm), respectively. The channel length (i.e., S/D spacing) for this device is ~200 nm. As expected, the device without SiN_x coating exhibits *p*-type switching characteristics (Fig. 5c). After SiN_x deposition, polarity conversion to *n*-type is observed with similar ON currents for both cases. Furthermore, $I_{ON}/I_{OFF} > 10^5$ is observed for both cases. The results suggest that SiN_x field-effective doping is also compatible with single nanotube devices. Importantly, the similar ON-state current for both polarities suggests that the nanotube quality remains pristine after SiN_x deposition, with PECVD processing not inducing defects in SWCNTs.

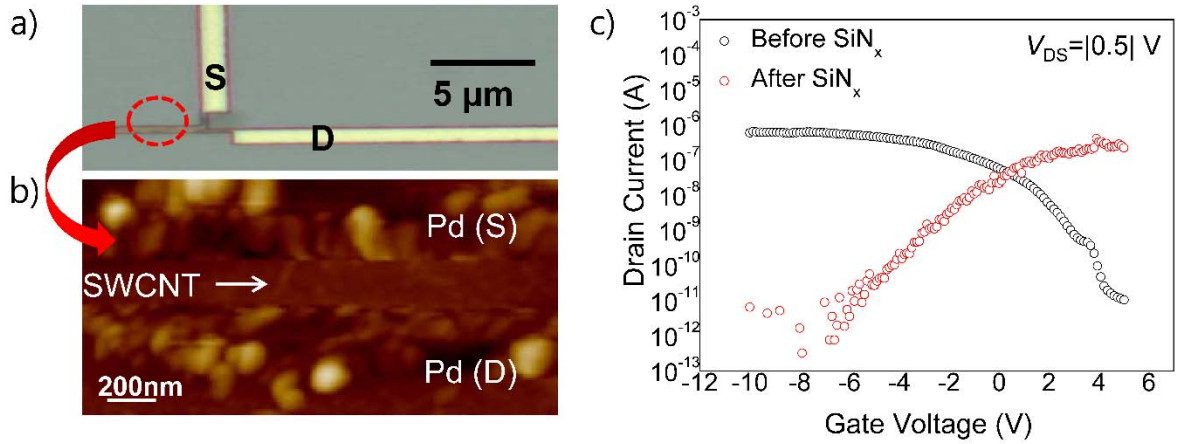


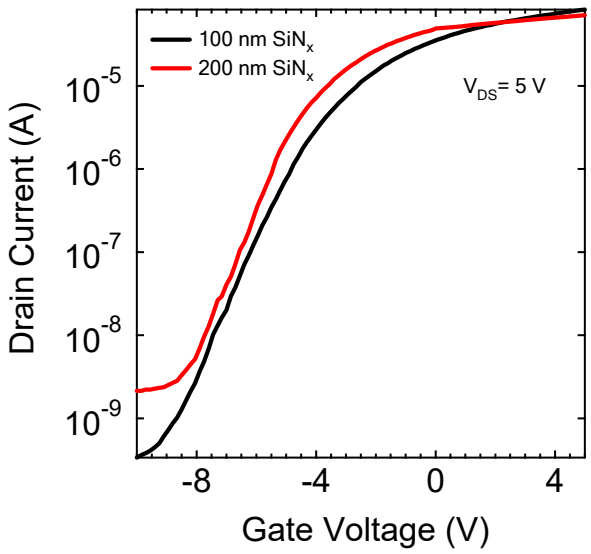
Figure 5: Single nanotube devices. a) Optical microscope and b) AFM images of a back-gated transistor based on an individual SWCNT. c) Transfer characteristics of the device before and after SiN_x deposition.

4.2.3 Discussion

In conclusion, a new air-stable doping concept for SWCNTs is demonstrated by using SiN_x thin films deposited by PECVD. The fixed positive charges within SiN_x act to *n*-dope the underlying nanotubes via field-effect, which is in distinct contrast to the charge transfer doping commonly explored in the past. Given the large knowledge base and infrastructure built around SiN_x thin film passivation in the silicon solar cell industry, this doping concept presents a reliable and easy to process route towards obtaining high performance SWCNT *n*-type transistors. Specifically, the obtained *n*-type SWCNT TFTs exhibit excellent device-to-device uniformity with comparable electrical characteristics to their *p*-type counterparts. As a proof of concept, a CMOS invertor is demonstrated using two SWCNT TFTs. In the future, the doping level of SWCNTs can be tuned by changing the stoichiometry of the nitride by changing PECVD process parameters, thus changing the fixed charge density. Furthermore, this doping concept can be extended to *p*-doping of carbon nanotubes by using other insulators with fixed *negative* charges. The work presents an important advance towards realization of CMOS circuitry based on nanotube TFTs for large-area electronic applications, where random networks of SWCNTs have shown to be a promising material system.

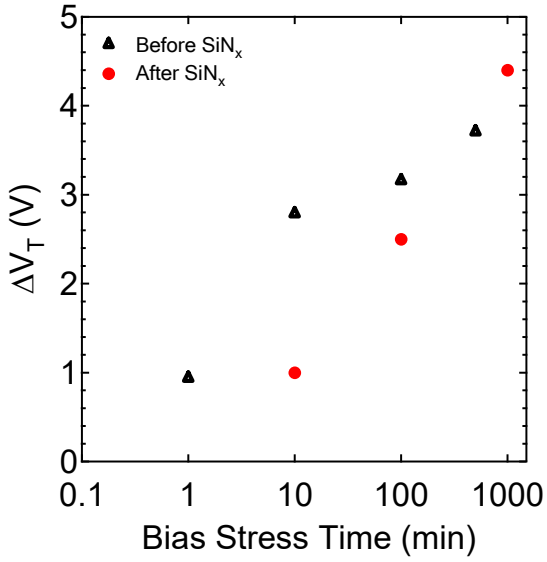
4.2.4 Experimental and Theoretical Details

4.2.4.1 Thickness effect of SiN_x



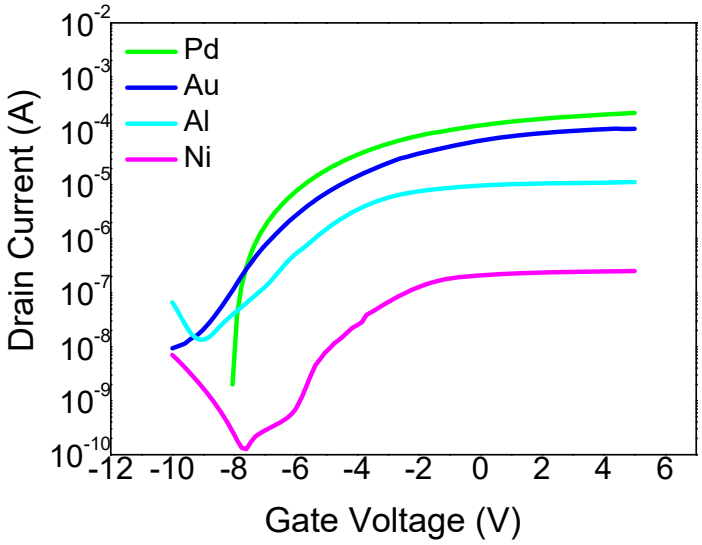
Supplementary Figure S1: Transfer characteristics of a representative SWCNT TFT after 100 nm of SiN_x thin film deposition (black curve) and after an additional 100 nm of SiN_x (total 200 nm; red curve), showing minimal difference in the transfer characteristics.

4.2.4.2 Bias Stress Testing



Supplementary Figure S2: Change in the threshold voltage versus the initial zero stress threshold voltage after bias stress testing of representative SWCNT TFTs before SiN_x deposition and after. The devices were placed under a bias stress of 10 V gate voltage and 10 V drain voltage.

4.2.4.3 Effect of different contact metals



Supplementary Figure S3: Transfer characteristics of SWCNT TFTs after SiN_x deposition with Pd, Au, Al, and Ni S/D contacts. Regardless of the metal contact, the SWCNT devices all exhibit n-type behavior after SiN_x with Pd exhibiting highest ON-state current, corresponding to best SWCNT/metal interface.

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4.3 Extension of SiN_x Fixed Charge Doping to WSe_2

The following subchapter has been previously published in a similar format in:
K. Chen, *et al*. Air stable n-doping of WSe_2 by silicon nitride thin films with tunable fixed charge density. *APL Materials*, **2**, 092504 (2014).

Two dimensional (2D) layered materials have generated much interest due to the ability to obtain atomically well-defined layers with thicknesses down to a single layer, providing a potential pathway to ultra-scaled transistors with excellent gate control[1–4]. In addition, they may enable new electronic and optoelectronic device architectures with unique functionalities[5,6]. Transition metal dichalcogenides (TMDCs) as a class of 2D materials in particular, exhibit a wide range of electronic properties ranging from metallic to insulating[7], with many being semiconductors with intrinsic carrier mobilities >100 $cm^2/V\ s$[8] even when scaled down to a monolayer in thickness. It should be noted that the measured mobility is high for a sub-1nm thick semiconductor when compared to silicon or III-V semiconductors of similar thicknesses[9], owing to the lack of surface native oxides and in principle atomically smooth surfaces which reduce surface roughness scattering of carriers. Due to this range of available materials, transistors have been made consisting of entirely 2D materials, exhibiting proof of concept for the scaling potential of layered materials[10]. However, one challenge of TMDCs is that they generally exhibit a high degree of Fermi level pinning[11], resulting in it being very difficult to contact both the conduction band and valence band for the same material. In this regard, degenerate doping of the source/drain contacts, similar to what is often used in conventional 3D semiconductors is the most effective route for injecting electrons or holes with low contact resistances. Furthermore, controlled n- and p-doping of TMDCs is critical for enabling various device structures. Doping of TMDCs via surface charge transfer doping has been demonstrated in the past using a variety of electron donating or withdrawing molecular species[8,12,13]. While the previous works have demonstrated the proof-of-concept viability of *n*- and *p*-doping for TMDCs, development of air-stable and scalable dopant processes is still of significant need.

4.3.1 Experimental Results

In this work, we present a robust *n*-doping method for WSe_2 by depositing thin films of silicon nitride on the surface using plasma enhanced chemical vapor deposition (PECVD). PECVD nitride has been widely used for field-effect passivation of silicon solar cells[14–16] and is an air stable[14,17] and scalable process[18]. Silicon nitride, as grown by PECVD, contains a high density of positive charge centers which originate from $^{+}Si{\equiv}N_3$ dangling bonds known as K^+ centers[19], shown in Figure 1a, with their density being controllable by the deposition process parameters. This characteristic is utilized in Si solar cells which induces a favorable surface band bending of Si, and thus reduces the surface recombination velocity of carriers. In fact, the field-effect induced band bending can be so severe as to cause surface inversion of *p*-body silicon[20–22]. Here, we apply the same concept to WSe_2 devices. We observe strong field-induced electron doping of WSe_2 by SiN_x coating (Figure 1b), with the electron sheet density being user-tunable, up to the degenerate limit by controlling the stoichiometry of the PECVD SiN_x. Notably, given the small thickness of WSe_2 (from monolayer up to ~10 nm explored here), the entire body of WSe_2 can be inverted to *n*-type by utilizing this surface-induced field-effect doping scheme. This has enabled us to fabricate stable *n*-type WSe_2 transistors with excellent performance. More generally, the approach here presents a route towards controlling the electronic properties of TMDCs by simply depositing thin films of charged dielectrics on the surface.

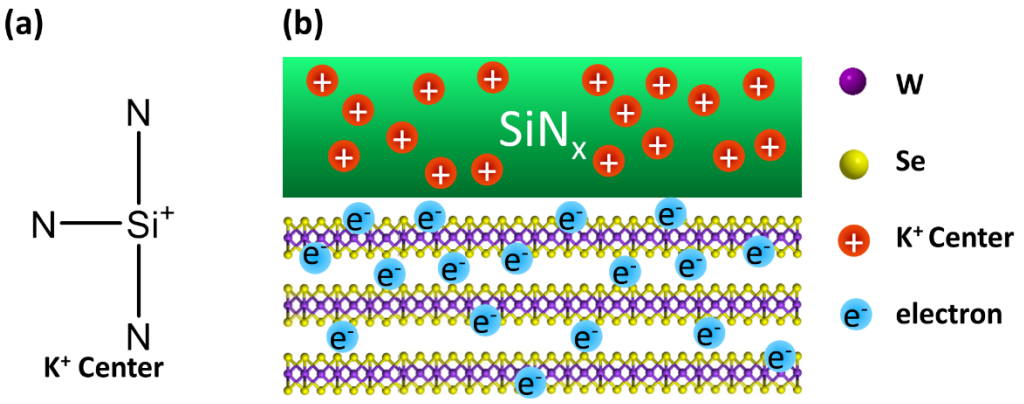

Figure 1: (a) Diagram of the positively charged K^+ center found inside silicon nitride, originating from $Si^+{\equiv}N_3$ dangling bonds. (b) Schematic of the doping mechanism of the SiN_x. The positively charged K^+ centers act as fixed charges which attract electrons inside the WSe_2, thus inverting the material.

Deposition of the SiN_x was done using an Oxford Plasmalab 80plus PECVD system at 13.56 MHz frequency. The deposition temperature, pressure, and time were kept constant for all processes at 150 °C, 900 mTorr, and two minutes, respectively, which results in a SiN_x thickness of ~50 nm. Silane (SiH_4, 10% in Ar) and ammonia (NH_3) were used as the process gasses and the concentrations were varied to obtain different film stoichiometries and amount of fixed charge. In this paper, the NH_3/SiH_4 ratio refers to the ratio of NH_3 to the 10% SiH_4 in Ar gas mixture. The four different NH_3/SiH_4 gas flow ratios explored were 1/10, 1/2, 1/1, and 3.3/1, corresponding to absolute NH_3/SiH_4 flow rates of 30/300, 50/100, 100/100, and 100/30 sccm, respectively.

To test the effect of different ratios of NH_3 to SiH_4 on the doping of WSe_2, back-gated WSe_2 transistors were fabricated with the device structure shown in figure 2a. First, WSe_2 (HQ Graphene) was mechanically exfoliated onto a heavily doped *p*-type silicon wafer (resistivity 0.001-0.005 Ωcm) with 260 nm of thermal silicon oxide, which acts as a universal back gate. To ensure that the thickness of the WSe_2 did not contribute significantly to device to device variation, the WSe_2 flakes used for devices were kept approximately constant between 5-10 nm in thickness via optical contrast[23]. After exfoliation, Au source (S) and drain (D) contacts were patterned and deposited using photolithography and electron-beam evaporation, respectively. Finally, SiN_x (~50 nm in thickness) was deposited via PECVD on top of the entire sample to dope the devices.

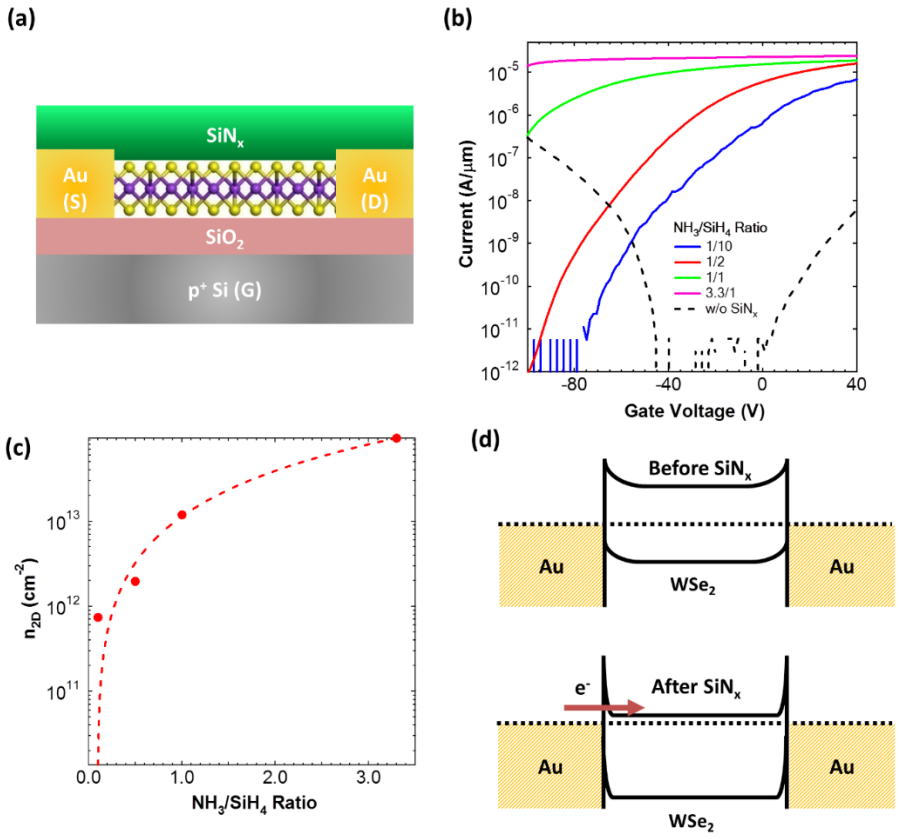

Figure 2: (a) Schematic of the back gated WSe_2 device structure used to test the effect of NH_3/SiH_4 ratios during nitride deposition on doping. (b) Width normalized transfer characteristics of four back gated WSe_2 devices with nitride deposited using different NH_3/SiH_4 ratios. As the NH_3/SiH_4 ratio is increased, the doping level increases. To minimize the effect of device to device variation, the WSe_2 thickness was kept within the range of 5-10 nm. A representative transfer characteristic curve of a device before nitride deposition is also shown for reference. (c) Extracted two dimensional electron sheet charge densities for the four nitride deposition conditions at zero gate bias. (d) Qualitative band diagrams of the back gated devices before and after SiN_x deposition. After SiN_x deposition, the Schottky barrier width at the metal/WSe_2 contact decreases, thus enabling efficient injection of electrons by tunneling.

The width normalized transfer characteristics of the WSe_2 devices at V_{DS}= -1 V after nitride deposition are shown in figure 2b for multiple NH_3/SiH_4 process concentrations corresponding to different SiN_x stoichiometries. All devices were fabricated with a channel length of 2 μm. A representative I_{DS}-V_{GS} curve for a device before SiN_x deposition is also shown. As expected, the as-made device exhibits ambipolar transfer characteristics with slightly higher *p*-channel conductance, corresponding to close to mid-gap Schottky barriers at the source/drain metal contacts. This behavior is similar to other previous reports on WSe_2 devices with Au metal contacts[8]. Upon deposition of SiN_x, the devices exhibit *n*-type transfer characteristics with a shift in the threshold voltage towards a more negative voltage. This result is indicative of electron doping of WSe_2 by SiN_x. The electron doping effect depends on the NH_3/SiH_4 ratio used during SiN_x deposition. As the NH_3/SiH_4 concentration ratio was increased, the devices become more

heavily *n*-doped with higher *n*-channel conductance. Specifically, for NH_3/SiH_4 ratios of >1/1, WSe_2 becomes degenerately doped with minimal gate dependence in the transfer curves (Fig. 2b). The two dimensional electron sheet densities (n_{2D}) of the devices can be estimated from $n_{2D}=(I_{DS}L)/(q\mu WV_{DS})$[13] where I_{DS} is the drain current at zero gate voltage, L and W are the lengths and widths of the devices, respectively, q is the electron charge, V_{DS} is the applied drain voltage, and μ is the field-effect mobility. It should be noted that this calculation does not take into account the effect of contact resistance, which may underestimate n_{2D}, especially for the lower doped devices. From figure 2c, it can be seen that the sheet density varies from 7.4×10^{11} to 9.5×10^{13} cm^{-1} for the explored NH_3/SiH_4 ratio. The ability to tune the electron concentration in WSe_2 by orders of magnitude by simply changing the stoichiometry of SiN_x presents a facile doping scheme. Figure 2d depicts a qualitative band diagram of the effect of SiN_x on WSe_2. As the devices become increasingly doped by the fixed charges in SiN_x, the Fermi level moves closer to the conduction band, shifting the threshold voltage negatively as well as reducing the width of the metal/WS_2 Schottky barrier. The thinner barrier enables greater electron injection by tunneling through the barrier and hence forms a practical ohmic contact for electrons (Fig. 2d).

Figure 3a shows the transfer characteristics at V_{DS} = -0.05 and -1V of a WSe_2 back-gated transistor two weeks after deposition of SiN_x with a NH_3/SiH_4 ratio of 1/2, which corresponds to a WSe_2 sheet electron density of 2×10^{12} cm^{-2} (Fig. 2c). This electron sheet density is high enough to provide a low resistance metal contact to the conduction band of WSe_2 while still allowing for gate control of the channel. The transfer characteristics of the device before doping is included for reference. An optical microscope image of the actual device is shown in the inset. This *n*-type FET exhibits a peak field-effect mobility of ~70 $cm^2/V\cdot s$ as extracted using the analytical equation $\mu=G_mL/(WV_{DS}C_{ox})$. Here, G_m is the transconductance, $C_{ox}=1.33\times10^{-8}$ F/cm^2 is the calculated gate oxide capacitance for 260 nm of SiO_2, and W and L are the width and length of the channel, respectively. Figure 3b shows the output characteristics of the same device after nitride deposition. As can be seen, the curves are linear at low V_{DS}, indicating that the contact is near ohmic.

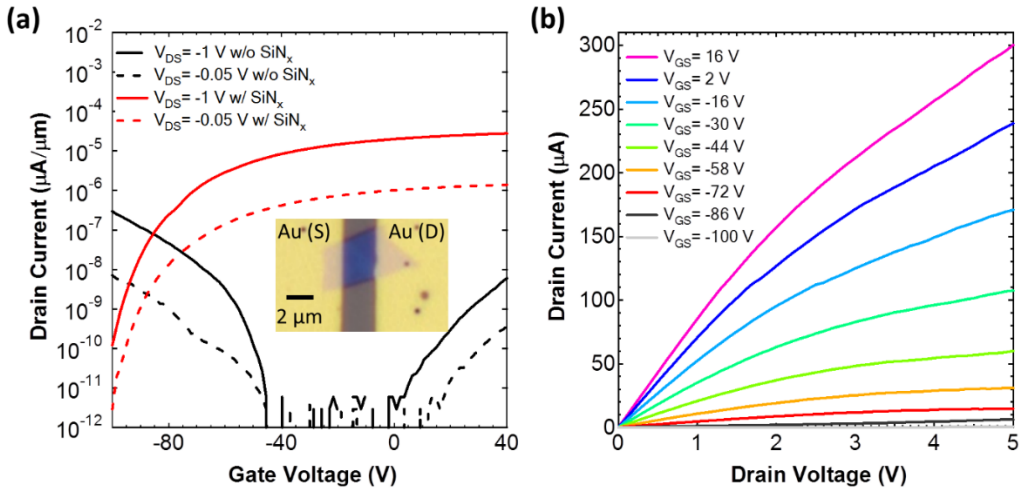

Figure 3: (a) Transfer characteristics of a WSe_2 back-gate FET before and after SiN_x deposition at a NH_3/SiH_4 concentration ratio of 1/2. An optical image of the device is shown in the inset. (b) Output characteristics of the device post SiN_x deposition.

To understand the effect of the NH_3/SiH_4 concentration during deposition on the doping level, the fixed charge density present inside the nitride was extracted using capacitance-voltage (*C-V*) measurements. A metal insulator semiconductor (MIS) structure with an Al gate on top of SiN_x, shown in the inset of figure 4a, was fabricated for the *C-V* measurements**.** First, the SiN_x was deposited via PECVD onto a lightly doped n-type silicon wafer with resistivity between 10-30 Ω-cm. Then, 500×500 μm squares of Al (150 nm in thickness) were deposited onto the nitride using a shadow mask via thermal evaporation. As can be seen in figure 4a, the flat band voltages of the MIS structures shift more negatively as the NH_3/SiH_4 ratio is increased for deposition. In all cases, the flat band voltage is negative with respect to the expected flat band voltage of Al and the lightly doped *n*-type wafer, given by the work function difference of $\phi_{MS} \sim -0.23$ V. This indicates the presence of positive fixed charge inside the nitride as expected. The flat band voltage , V_{FB}, can be determined as the peak of $d^2(1/C_{nitride}^2)/dV^2$ where $C_{nitride}$ is the accumulation capacitance of the MIS structure[24]. For 1/10, 1/2, 1/1 and 3.3/1 NH_3/SiH_4 ratios, the measured V_{FB} are approximately -4.3, -6.2, -7.4, and -9.1 V, respectively. The fixed charge density can be calculated from the shift in the V_{FB} using the equation $Q_F=C_{nitride}(\phi_{MS}-V_{FB})/q$ assuming that the fixed charge is equally distributed throughout the nitride where q is the electron charge. The calculated fixed charge densities vs. the NH_3/SiH_4 gas flow ratio used during deposition is plotted in figure 4b. As can be seen, the fixed charge densities increase monotonically as the ratio of NH_3 to SiH_4 is increased, which results in the higher doping levels observed in these devices.

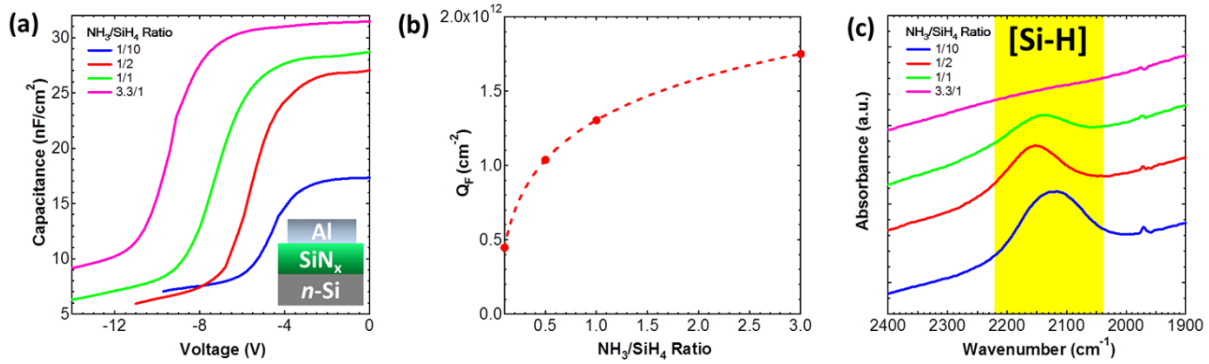

Figure 4: (a) Capacitance-voltage (*C-V*) curves for silicon nitride films deposited at different NH_3/SiH_4 concentration ratios. The device schematic is shown in the inset. (b) Plot of the extracted fixed charge density in the silicon nitride films as a function of NH_3/SiH_4 ratio. As the ratio is increased, the fixed charge density increases. (c) Fourier transform infrared spectroscopy of the Si-H stretching mode at ~2100 cm^{-1}. As the NH_3/SiH_4 ratio is increased, the Si-H bond density drops and the peak shifts to higher wavenumbers, corresponding to a more nitrogen rich nitride films and larger concentration of K centers.

Fourier transform infrared spectroscopy (FTIR) measurements were conducted on SiN_x films deposited at different NH_3/SiH_4 concentration ratios to measure the relative amounts of Si-H bonds. Figure 4c shows the FTIR spectra at ~2100 cm^{-1}, which corresponds to the Si-H stretching mode[25]. As can be seen, the integrated Si-H peak intensity drops as the NH_3/SiH_4 ratio is increased, indicating a reduced amount of Si-H bonds. In addition, the peak position shifts from ~2129 cm^{-1} at 1/10 NH_3/SiH_4 to ~2190 cm^{-1} at 3.3/1 NH_3/SiH_4 which corresponds to an

increase in the N_3Si-H bonding configuration component of the Si-H stretching mode[26] which has a peak position at 2220 cm^{-1}. This peak shift also indicates a stoichiometry change from silicon rich to a more nitrogen rich SiN_x[27]. The drop in integrated peak intensity and shift towards higher wavenumbers has been correlated with an increased density of dangling bond K centers[27].

Due to the use of a plasma during the nitride deposition, it is possible that the surface of the WSe_2 can be damaged. To explore the effect of the PECVD deposition on the integrity of WSe_2, a back-gated monolayer WSe_2 transistor with Pd S/D contacts was fabricated. As the device is a single layer, any surface damage would result in drastic changes to its electronic and optoelectronic properties. An optical image of the device after doping is shown in figure 5a. The transfer characteristics of the monolayer before and after nitride deposition using an NH_3/SiH_4 ratio of 1/2 are plotted in figure 5b. Just as with the thicker WSe_2 devices, the monolayer device shows good *n*-type behavior after nitride deposition. To further explore the effect of the PECVD on the WSe_2, photoluminescence (PL) and Raman spectroscopy (HORIBA LabRAM HR800, 532 excitation wavelength) were carried out before and after nitride deposition. To ensure that no damage or measurement artifacts would result from sample heating, the laser power used was 0.8 mW. As seen in figure 5c, after SiN_x deposition, a red shift of 16 meV is observed in the PL peak energy in addition to a 35x decrease in the peak intensity. This observation is consistent with the previous gated PL measurements of monolayer TMDCs and can be attributed to the formation of negatively charged trions from excitons due to the increase in electron concentration[28–30]. Similarly, in figure 5d, a 5x decrease in the Raman intensity as well as a peak shift of 0.7 cm^{-1} of the E_{2g}^1 raman peak can be attributed to a softening of the vibrational modes due to the increase in electron concentration, which has been observed in monolayer MoS_2 devices[12,31]. Overall, no unexpected change in the electronic and optoelectronic properties of the monolayer WSe_2 were observed after SiN_x deposition, indicating that the deposition process does not affect the crystalline integrity of the WSe_2.

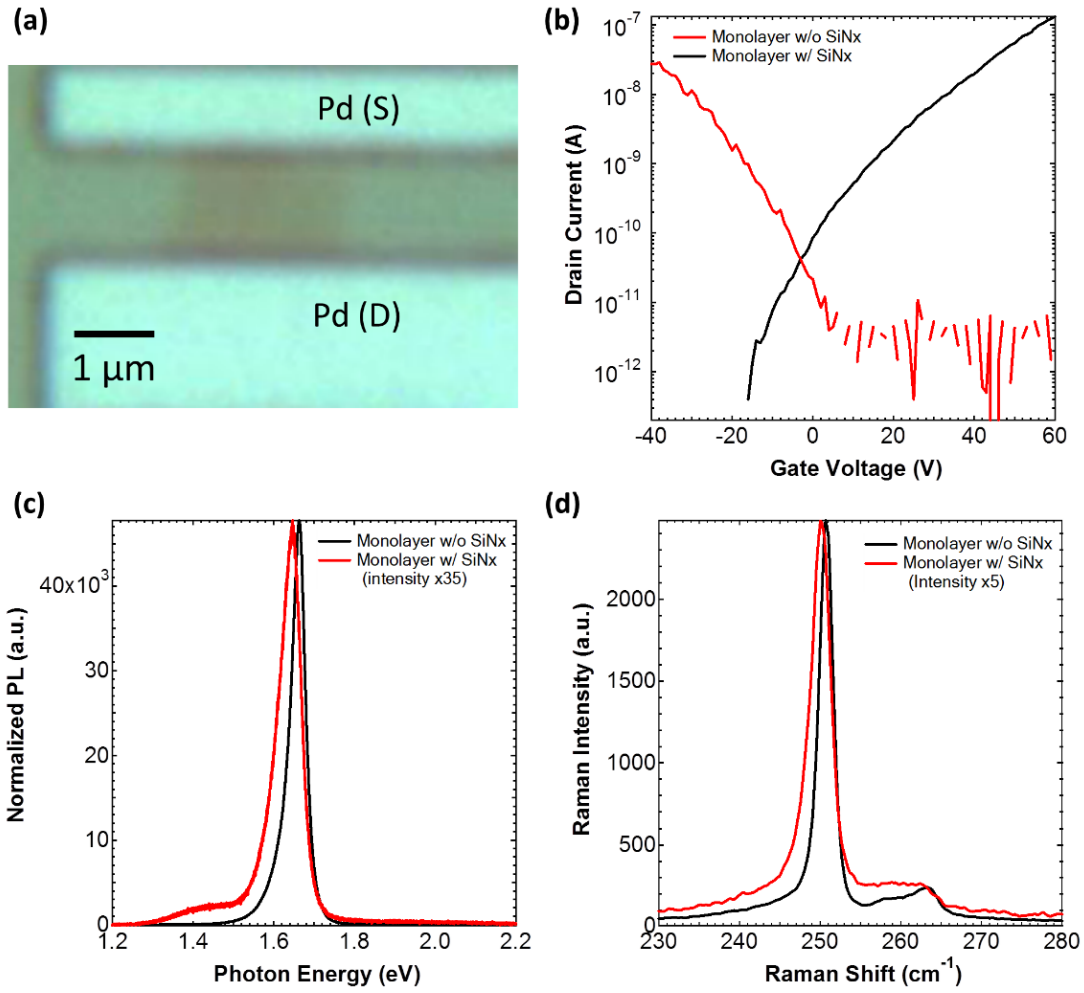

Figure 5: (a) Optical image of a monolayer WSe2 back-gated transistor after SiNx deposition. (b) Transfer characteristics of the device before and after SiNx deposition. (c) Photoluminescence and (d) Raman spectra (excitation wavelength of 532 nm) of the monolayer before and after SiNx deposition indicating no damage to the flake occurred during nitride deposition.

4.3.2 Discussion

In conclusion, we have demonstrated an air stable n-doping scheme for TMDCs using PECVD SiN_x with tunable fixed charge density arising from positively charged $^{+}Si{\equiv}N_3$ dangling bonds. By tuning the gas flow ratios of NH_3 and SiH_4, different densities of fixed charge within the nitride up to $1.75{\times}10^{12}$ cm^{-2} are demonstrated, allowing for a controlled method to change the doping concentration via field-effect. Using this doping scheme, WSe_2 n-MOSFETs were fabricated, exhibiting a high electron mobility of ~70 cm^2/Vs. Similar to that of modulation doping utilized in high electron mobility transistors where the dopant atoms are away from the actual channel material, field-effect doping can enable high doping concentrations in TMDCs without causing damage to the lattice nor experiencing a drop in mobility due to ionized impurity scattering. Given the ease of processing of SiN_x and its stability as an inorganic thin film, the approach here presents a robust route towards controlled doping of thin layers of TMDCs. In the future, the use of dielectrics with negative fixed charges can be explored as a complementary *p*-doping scheme.

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4.4 Fully Printed CNT backplanes for tactile pressure mapping

The following subchapter has been previously published in a similar format in:
C. Yeom, K. Chen, *et al*. Large-Area, Compliant Tactile Sensors Using Printed Carbon Nanotube Active-Matrix Backplanes. *Advanced Materials*, **27**, 1561–1566, (2015).

Fabrication of devices and sensors on flexible substrates allows for conformal coverage of electronic systems on nonplanar surfaces[1,2], thus enabling new functionalities. Potential applications include flexible displays[3–7], wearable electronics[1,8–14], interactive surfaces[2,11,15], and electronic wallpapers[16]. In many applications, large-area coverage of electronics beyond the size limits of conventional batch processing is desirable. In this regard, the use of printing processes is of tremendous advantage. Over the past several years, significant progress has been made in the development of printing techniques based on organic molecules[17–19] and polymers[20–23], nanoparticles[24,25], nanowires[26,27] and single-walled carbon nanotubes (SWCNTs)[28–32]. The printed devices have been readily configured as the building blocks for various electronic systems[3,18,32,33]. Each material system and printing technique presents unique advantages and disadvantages, depending on the specific needs of the targeted application. For instance, partly and fully-printed SWCNT transistors have been reported in the past[28,30,31,33], exhibiting excellent electrical properties[33], high air-stability[33], with low sensitivity to strain due to their miniaturized diameters[31]. Particularly, we recently demonstrated multi-step gravure printing of thin film transistors (TFTs) utilizing semiconductor-enriched SWCNTs as the active channel material with printed Ag source/drain/gate electrodes and inorganic/organic high-κ gate dielectrics[31]. Building on these recent advancements, here, we demonstrate fabrication of an active-matrix backplane consisting of a 20×20 SWCNT TFT array through a printed process scheme. Backplanes are the critical component for any multi-pixel system, such as displays or sensor arrays since they reduce the number of addressing lines in an arbitrarily large m×n matrix from m×n to just m+n. In addition, active matrices offer significant advantages over passive matrices in terms of power consumption and contrast, which are critical for increased scaling[34] and resolution[35]. As an example demonstration, we integrate the printed SWCNT active-matrix backplane with tactile sensor arrays for large-area pressure mapping. The demonstrated system presents a scalable route toward realization of user-interactive surfaces, capable of spatial and temporal mapping of stimuli over large-areas.

4.4.1 Carbon Nanotube Active Matrix Backplane

The fabrication of the active matrix backplane is performed by using a custom-built roll-to-plate gravure printing tool (Supplementary Figure S1a). The backplane consists of a 20×20 pixel matrix with an area of 45 cm^2, limited by the size of the tool used in this work, although the gravure printing process is known to be scalable to much larger sample areas[32,36]. Each pixel consists of a printed SWCNT TFT integrated with a pressure sensor on top, with the TFT used to address the pixel for the signal readout. The printer uses a dual camera setup to align the substrate with the engraved plate so that each subsequent printed layer can be properly aligned to the layers underneath with an alignment accuracy of down to 10 μm. The engraved plates consist of small cells etched into chrome plated copper plates which are filled with the desired ink. The design of the cells is critical to minimize ink bleeding outside of the desired printing areas (Supplementary Figure S1b, S1c). If not designed properly, it can lead to variation in TFT performance due to

variation in the channel length, and in the worst case scenario, shorting of the source and drain (S/D) electrodes, affecting pixel yield and reliability.

Figure 1a depicts the fabrication process for the flexible TFT backplane. First, solution processing is used to assemble a random network of semiconductor-enriched SWCNTs onto a poly(ethylene terephthalate) (PET) substrate. The PET is initially cleaned with oxygen plasma and then surface functionalized with poly-*L*-lysine (0.1% w/v in H_2O, Sigma Aldrich) by immersion for 5 min followed by a rinse with deionized (DI) water. This surface functionalization serves as an adhesion layer for subsequent SWCNT assembly. A 99% semiconductor-enriched SWCNT solution (NanoIntegris, Inc.) is dropcast onto the PET surface for 2 hours and then rinsed off with DI water. After SWCNT deposition, the S/D electrodes of the TFT are printed onto the substrate by using silver nanoparticle ink (PG-007AA; Paru Corporation, Korea) with a channel length and width of 100 μm and 1.25 mm, respectively. After the S/D deposition, a dielectric layer (~1 μm in thickness) is printed over the channel regions of the TFTs by using a commercial ink composed of high-κ barium titanate ($BaTiO_3$) (BTO) nanoparticles embedded within a poly(methyl methacrylate) (PMMA) binder (PD-100; Paru Corporation, Korea). This dielectric layer is then used as a hard mask to pattern and etch the SWCNTs. Specifically, the sample is exposed to oxygen plasma (120 W for 2 min) to etch away the SWCNTs not covered by the S/D and BTO/PMMA layers so that the CNTs are only present in the active regions of the TFTs. A second, BTO/PMMA layer (~2 μm in thickness) is then printed over the channel to minimize the gate leakage current as the first BTO layer is partially damaged during the oxygen plasma etch. To ensure no pinholes exist between the drain lines and the gate lines of the backplane, a third BTO/PMMA layer (~1 μm) is printed over the metal interconnect overlap regions of the matrix (Supplementary Figure S2). Finally, the top gate layer, composed of the same Ag nanoparticle ink as the S/D lines is printed over the BTO/PMMA gate dielectric to complete the fabrication of the active matrix. The gate electrodes overlap S/D by ~50 μm on each side. More details of the fabrication process can be found in the experimental section and Table T1 in supporting information.

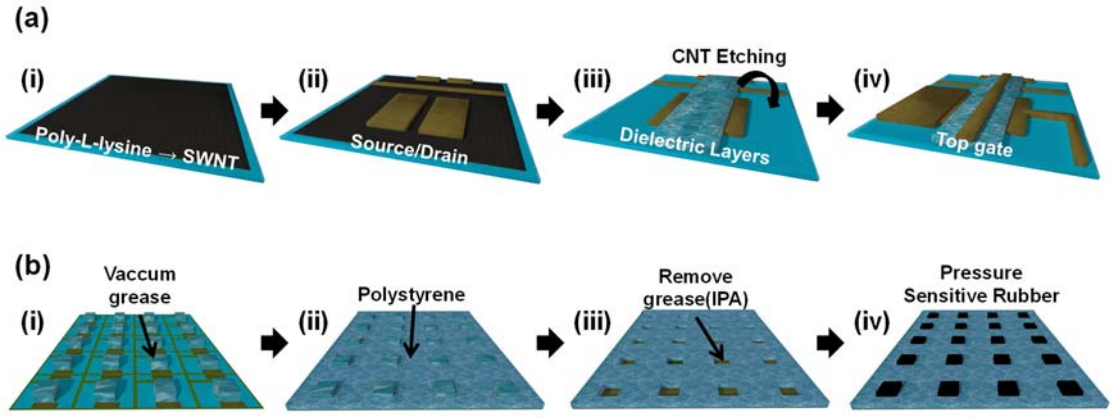


Figure 1: Fabrication of the pressure sensor array: a) First, a 99% carbon nanotube suspension was dropcast onto the PET surface after surface functionalization with poly-L-lysine. The S/D metal layer was then printed onto the SWCNT coated surface followed by a BTO dielectric layer over only the S/D channel region. After O_2 plasma etching of the SWCNTs, two more BTO layers were printed followed by printing of the gate metal layer. **b**) vacuum grease was dropped onto the source pads of the printed backplane which was then coated with a layer of polystyrene solution.

After annealing for twenty minutes at 150 °C, the vacuum grease was removed with isopropyl alcohol and individual squares of PSR were placed inside the vias.

In order to demonstrate the use of printed TFTs as an active matrix backplane for a sensor network, pressure sensors are integrated on top of the backplane using a pressure sensitive rubber (PSR: PCR Technical). The PSR acts as a variable resistor in this setup between the source of the transistor and ground. As the applied pressure increases, the resistance of the PSR drops, allowing the normally insulating rubber to be conductive. The change of conductance in the PSR is due to the reduction of the spacing between conductive carbon particles embedded in the film, thus enhancing the tunneling current upon induced pressure.

Figure 1b shows the process flow for integrating the pressure sensors. First, vacuum grease (Dow Corning) is dropcast onto the source pad of each TFT in the matrix, and then fully coated with a solution composed of polystyrene (M_W~350,000, Sigma Aldrich) and diethylene glycol monoethyl ether acetate (99%, Sigma Aldrich) via drop casting and spreading using an air gun as an insulating layer. The polystyrene solution is cured onto the backplane by baking the sample at 150 °C for 20 minutes. The vacuum grease is then removed using isopropyl alcohol, thus opening up the source pads of each pixel for integration with the PSR. The depth of these vias in the polystyrene insulating layer, measured using a profilometer (NanoSystem Co.,Ltd, NV-2200), is approximately 27 μm (Supplementary Figure S3). PSR films cut to a slightly smaller size than the vias are picked and placed individually into the vias as the through via contact. Finally, a silicone rubber coated with a layer of conductive carbon is laminated on top of the completed device as a universal ground output.

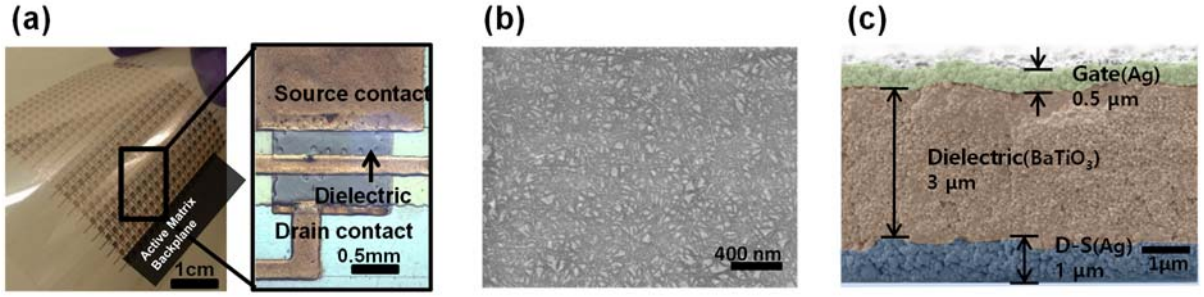


Figure 2: Images of printed SWCNT TFT array: a) An optical image of a printed active matrix backplane along with a zoomed in image of a single TFT pixel. **b)** An SEM image of the PET surface after SWCNT deposition. **c)** False color cross sectional SEM image of the printed TFT.

Figure 2a shows an optical image of the printed TFT backplane before PSR integration, along with a zoomed-in image of a single TFT pixel. Figure 2b shows a scanning electron microscope (SEM) image of the PET film after SWCNT deposition, showing a clear high density percolation network of nanotubes. From the cross-sectional SEM image in Figure 2c, it can be seen that the S/D lines are ~1 μm thick, the total dielectric thickness is ~3 μm, and the thickness of the top gate is ~0.5 μm.

After the fabrication was concluded, the transfer characteristics of individual TFTs in the backplane were analyzed. All devices were measured at room temperature in ambient conditions. Figure 3a depicts a drain current vs. gate voltage (I_{DS}-V_{GS}) graph of a representative TFT at drain voltages of -1 and -5 V. Figure 3b shows the I_{DS} -V_{GS} plots of the 388 working TFTs out of a total

of 400 in the backplane at a drain voltage of -5 V. It is important to note that the yield of the working TFTs in the backplane, printed in ambient conditions, was 97%. The main failure modes for the devices were short circuits between the source and drain contacts or pinholes in the BTO gate dielectric, which can be attributed to printing in an uncontrolled environment, where fluctuations in temperature and humidity can change the spreading and printing properties of the inks and particles in the air can obstruct the ink.

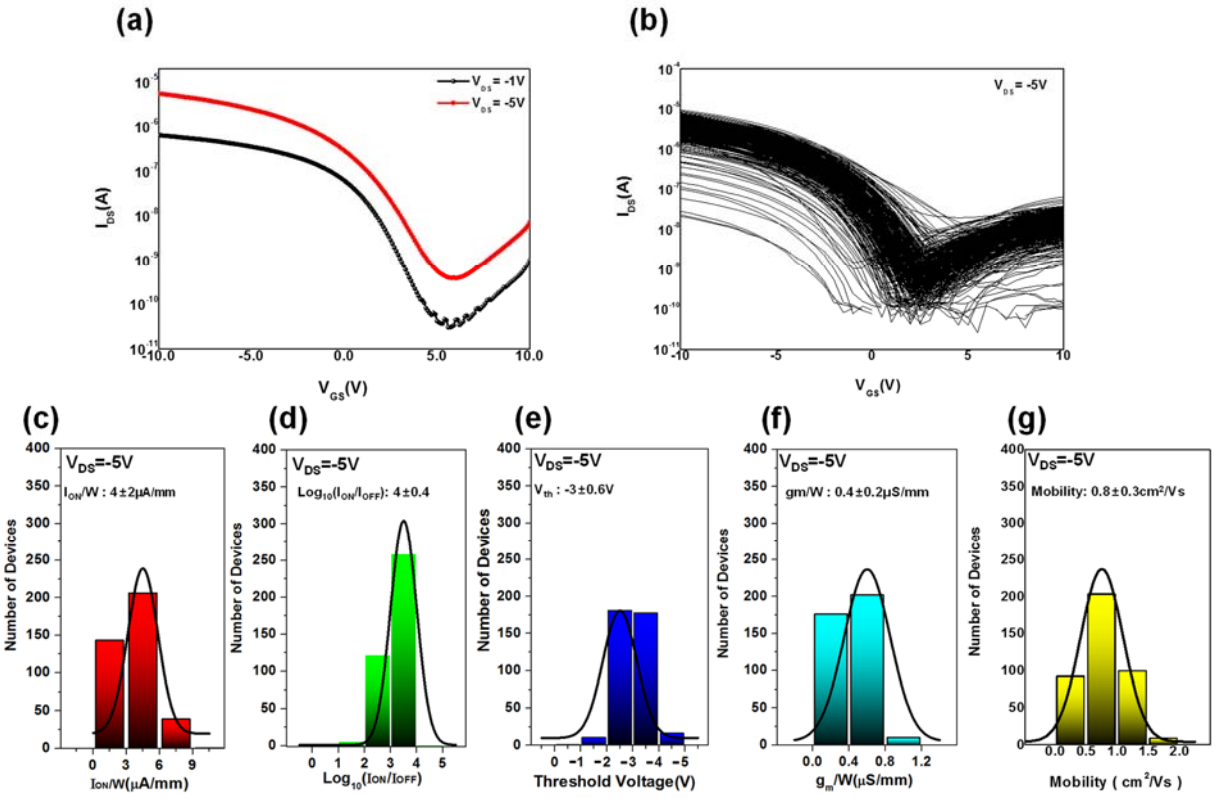


Figure 3: Electrical characterization of TFTs: a) Transfer curve of a representative TFT in the array at a drain voltage of -1 and -5 V. **b)** Transfer curves of the 388 working TFTs in the printed backplane at a drain voltage of -5 V. **c-g)** Histograms of the TFTs showing the statistical distribution of **c)** normalized on current, **d)** log of the on/off ratio, **e)** threshold voltage, **f)** transconductance**,** and **g)** field effect mobility. Channel length and width of the devices are 100 μm and 1.25 mm, respectively.

Figures 3c-g show the statistical histograms for the 388 working TFTs. At a drain voltage of -5 V, the average on-current density normalized per unit width of the TFTs was measured to be 4 ± 2 μA/mm (Figure 2c). The TFTs also have an average on/off current ratio of ~10^4 (Figure 3d) which facilitates a low enough off current level for distinguishing between pressure loading and unloading. The average threshold voltage of the TFTs is -3 ±0.6 V (Figure 3e). The negative threshold voltage, indicating enhancement mode behavior of the TFTs, is important for the operation of the backplane. Otherwise, a positive gate voltage must be applied to the pixels that are not being accessed to avoid signal cross-talk between the pixels while the backplane is being mapped. While the subthreshold swings of the TFTs do result in a non-zero current level at zero-bias in our devices, this zero-bias current level is sufficient to allow for mapping of applied pressure as demonstrated later. The average transconductance and field effect mobility of the TFTs

are calculated to be 0.4 ± 0.2 μS/mm (Figure 3f) and 0.8 ± 0.3 cm^2/V s (Figure 3g), respectively. The mobility calculations were done using a parallel plate model following the equation: $\mu = Lg_m/(|V_{DS}|C_{OX}W)$ where g_m is the transconductance, L and W are the channel lengths and widths of the TFTs, respectively, V_{DS} is the applied drain bias of -5 V, C_{OX} is the capacitance per unit area, measured to be 9.5 nF/cm^2 using an LCR meter and parallel-plate capacitor test structures. We speculate that the mobility is lower than our previous work on printed TFTs possibly due to different printing conditions which result in different layer thicknesses/overlap areas increasing parasitics as well as partial damage to the nanotube channel due to the use of oxygen plasma to etch away carbon nanotubes not within the TFT channels in order to minimize crosstalk between pixels despite coverate by the BTO/PMMA dielectric layer. In the future, printing conditions can be better optimized and a thicker dielectric can be printed to serve as a more robust hard mask.

4.4.2 Pressure Sensor Integration and Mapping

Figure 4a shows the equivalent circuit diagram of a single pixel in the array, consisting of a TFT with its source connected to ground through the PSR, which acts as a variable resistor. Figure 4b, shows the pressure response of a representative pixel with an applied drain voltage of -5 V in the array. Here, the pixel consists of a TFT with its source connected to ground through the PSR, which acts as a pressure sensitive variable resistor. The response time of the pixel is limited to operations below ~15 Hz due to the response time of the PSR[37], which is still sufficient for many applications such as human tactile pressure sensing. As more pressure is applied, the PSR becomes more conductive and thus the on current of the pixels increase. The pixels are sensitive to pressures ranging from ~1 kPa up to 20 kPa, with a linear sensitivity of ~800%/kPa (Figure 4c), corresponding to pressures similar to that of a light human touch.

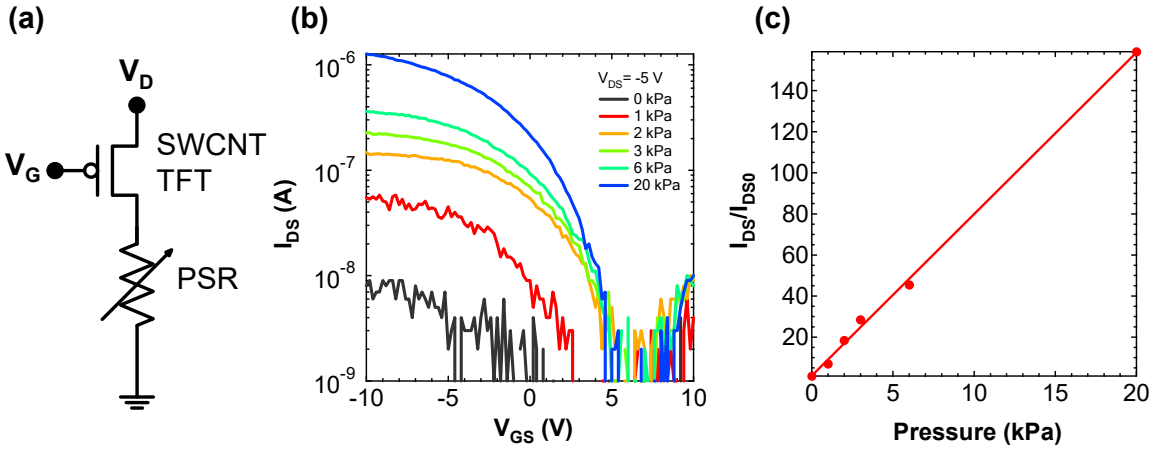


Figure 4: Single pixel pressure sensing: a) Equivalent circuit diagram of a single pixel in the TFT array with the PSR acting as a variable resistor in series with the SWCNT TFT. **b)** Transfer curves of a representative pixel with varying amounts of applied pressure (from 0 to 20 kPa) at a drain voltage of -5 V. **c)** Plot of the ratio of on current (at a gate voltage of -10 V) vs applied pressure. I_{DS0} is the drain current at zero applied pressure (at 0 kPa).

To conduct pressure mapping using the whole array, a block of polydimethylsiloxane (PDMS) (Sylgard 184, Dow Corning), is cut out in the shape of a "*C*" and placed on top of the sensor array (Figure 5a and b). The mapping is done by applying -5 V on the drain (column select) and -10 V

on the gate (row select) lines as shown in Figure 5c and then measuring the current out of the PSR common ground for each pixel. Figure 5d-f show the output current maps of the sensor matrix without applying pressure, with only the PDMS C slab (~0.7 kPa), and with 6.5 kPa of pressure applied onto the PDMS slab (total 7.2 kPa). As expected, when no pressure is applied, all of the pixels are in the off-state, with on currents <100 nA. When a pressure of 0.7 kPa was applied, some pixels begin to turn on, but no clear response is observed as the applied pressure is below the sensing threshold of 1 kPa for the pixels. When 7.2 kPa was applied, the output current of the pixels underneath the PDMS block increases up to ~1 μA while the output current of the pixels not underneath the PDMS mostly remain <100 nA, reflecting the applied pressure.

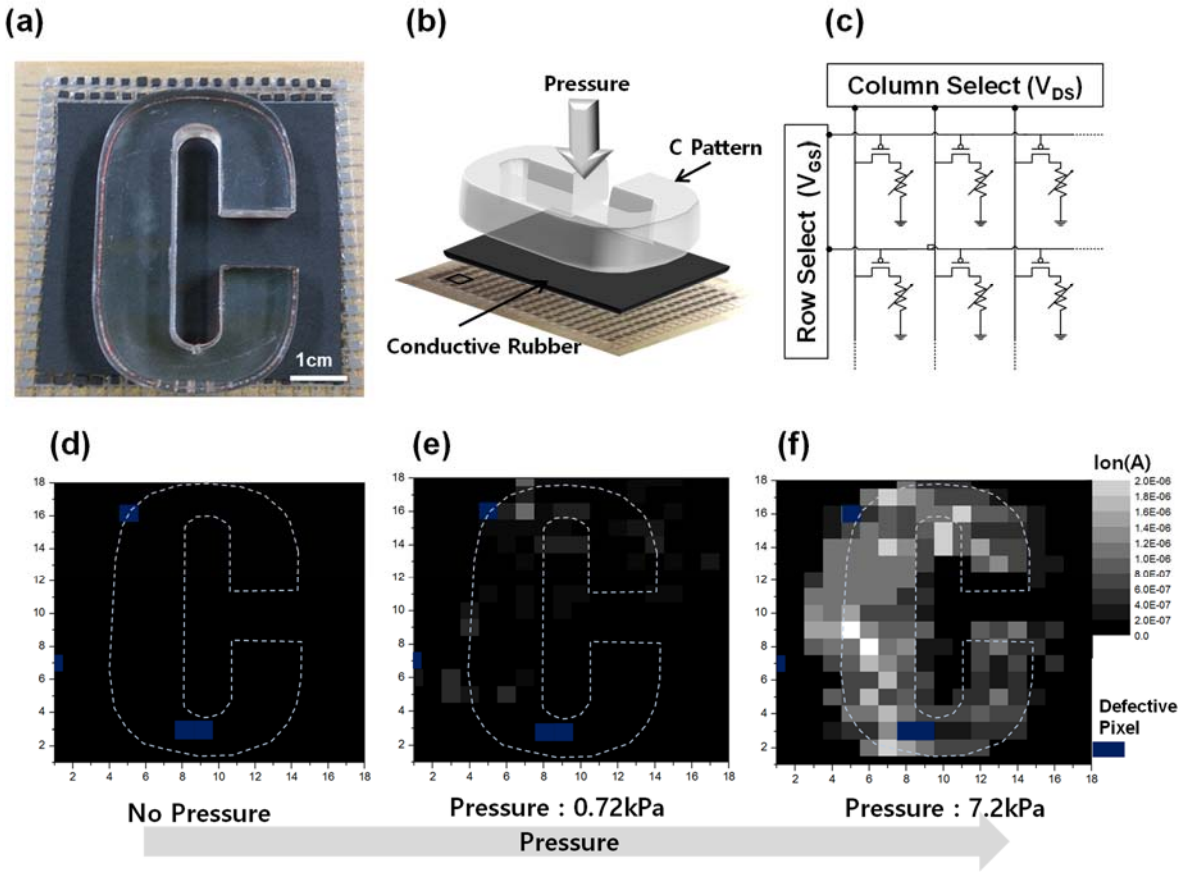


Figure 5: Pressure mapping: a) Optical image of the printed TFT backplane with the PDMS slab in the shape of a C, placed on top of the universal ground sheet. **b)** Schematic drawing of the measurement method for mapping pressure. **c)** Equivalent circuit diagram of the pressure sensitive array. Drain voltages act as the column select while gate voltages act as the row select to control each individual pixel. **d-f)** Output currents of the array at applied pressures of **d)** 0 kPa, **e)** 0.7 kPa, and **f)** 7.2 kPa.

Since the backplane is fabricated on a flexible substrate, one advantage is that it can be bent to cover non-planar surfaces. To test the operation of our devices under such circumstances, the I_{DS}-V_{GS} behavior of a representative TFT on the backplane was measured while it was flat and subsequently wrapped around a cylinder with a radius of ~1.85 cm. As can be seen in Figure 6,

there is virtually no change in the transfer characteristics of the transistor. The ability for the TFTs to operate while under strain comes from the excellent mechanical properties of the carbon nanotubes which we have used as the active channel material, as well as the organic binder components of the printed Ag and BTO inks. This shows that our printed backplane may be operated while laminated conformally around nonplanar surfaces, preventing potential crosstalk between lateral strain and the applied tactile pressure in the vertical direction being measured.

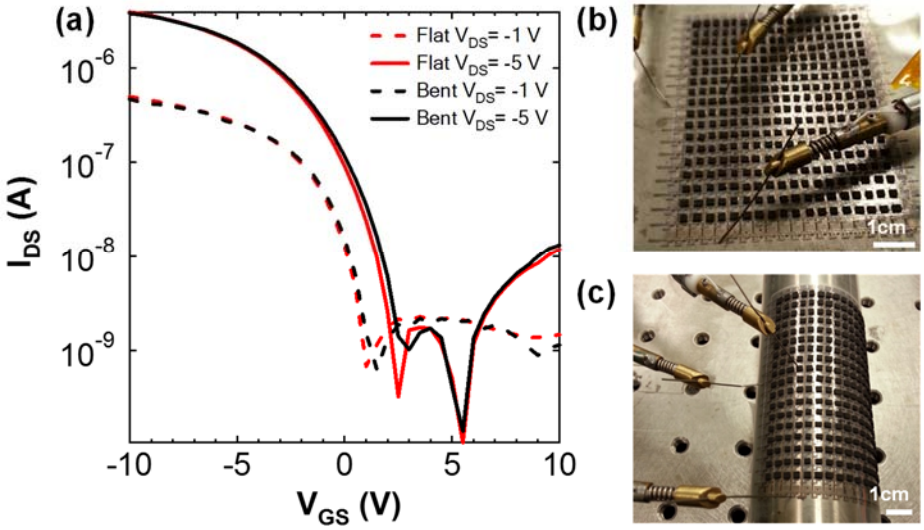


Figure 6: TFT performance under strain: a) Transfer curves of a representative TFT while flat and when bent around a rod with a radius of curvature of ~1.85 cm. **b)** Optical image of the device measurement while flate and **c)** when bent around the rod.

4.4.3 Conclusion

In conclusion, we have demonstrated a pressure sensor array capable of mapping out the applied pressure over an area using a printed active matrix TFT backplane. We are able to achieve a yield of 97% out of 400 individual TFTs with very reasonable performance variation between the transistors. While only a pressure sensor array is described in this work, the active matrix backplane could be integrated with a variety of other sensors such as photodetectors[1] or implemented as the backplane for a flexible display[4,15]. Also, the TFTs in the backplane see virtually no change in performance while under strain, allowing it to be used in applications where it may be placed onto a non-planar surface. It is also important to note that while the roll-to-plate gravure process used in this work limits the size of the backplane, all methods reported here can be transferred into a fully printed roll-to-roll gravure printing process[36] that could scale up the production of the backplane and sensor network to arbitrarily large sizes for truly ubiquitous sensor networks.

4.4.4 Experimental and Theoretical Details

4.4.4.1 Printing of the Active Matrix Backplane:

A blank PET substrate was first exposed to oxygen plasma at 120 W for 2 minutes. Poly-*L*-lysine solution was dropcast onto the substrate for 5 minutes and then rinsed with DI water and dried with N_2 gas. The 99% semiconducting CNT solution was then dropcast onto the surface for two hours and then rinsed with DI water and dried with N_2 gas. The PET substrate with CNTs everywhere was then attached to the roller of the printer. To print the S/D layer, the silver ink composite was dropped onto one edge of the engraved plate. Using a doctor blade, the ink was spread out into the wells of the plate with all excess ink removed. The engraved plate was then brought into contact with the PET substrate on the roller with an applied force of 5 kg and then passed under the roller with a speed of 100 mm/s. After printing, the PET substrate was detached from the print roller and baked in an oven at 150 °C for 30 seconds. To print the first BTO layer, which is only placed over the channels between the source/drain pads, the PET substrate was once again attached to the roller. Using an alignment camera on the printer, the engraved plate was aligned to the substrate using two alignment marks at the ends of the printed areas. The BTO ink solution was then spread into the engraved plate and then printed onto the PET in the same manner as the S/D layer except the contact force was increased to 8 kg and printing speed lowered to 50 mm/s. The PET substrate was then baked at 150 °C for one minute. Then the substrate was placed into an oxygen plasma system and exposed to oxygen plasma for 2 minutes at 120 W to etch away all of the CNTs that are not covered by the S/D or BTO layer. Afterwards, a second BTO layer was printed onto the substrate in a continuous line covering both the overlap between the gate metal lines and S/D metal lines in the transistor regions as well as the interconnect regions. A third BTO layer was printed using the same engraved plate and conditions as the first BTO layer, except the alignment was offset to cover the metal interconnect regions to ensure the removal of any pinholes. Finally, the gate layer was printed on and a final 150 °C bake in an oven for one hour was done. All printing pressures and print speeds for each layer can be found in Supplementary Table T1.

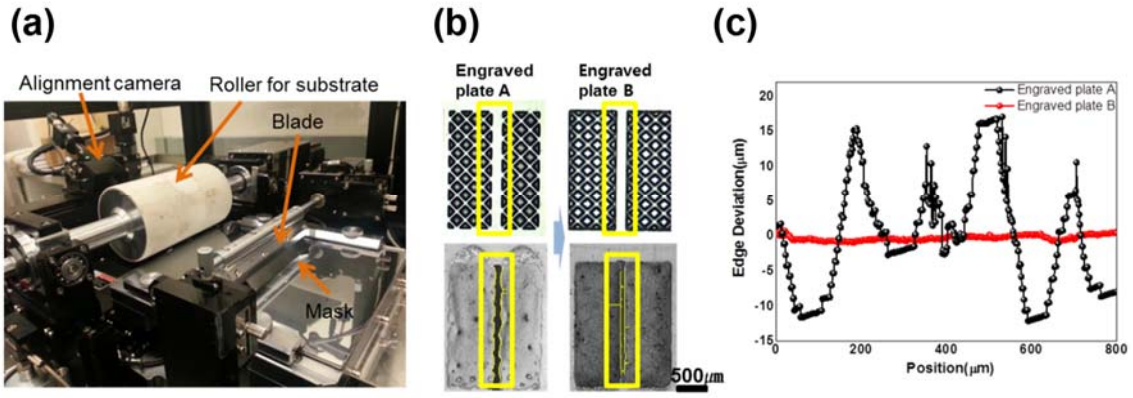
4.4.4.2 Integration of the pressure sensors:

First, vacuum grease was dropped onto the source contacts of each pixel. Then, a solution of polystyrene and diethylene glycol monoethyl ether acetate was spread out over the entire backplane and cured for 20 minutes in an oven at 150 °C. Using isopropyl alcohol, the vacuum grease was removed to expose the source contacts. Small PSR pieces were individually placed into the source vias. Finally, a sheet of PSR is laminated over the device to complete the fabrication process. The PSR is coated with a layer of conductive carbon tape on the top side to act as the universal ground output of the sensor array.

4.4.4.3 Device measurement:

All of the current vs. voltage measurements are taken using an Agilent B1500A semiconductor device parameter analyzer. To collect the I_{DS}-V_{GS} data shown in **Figure 2**, the gate and drain probes were placed at the ends of their respective lines in the array while the source probe was placed directly onto the source contact of each pixel. To obtain the pressure mapping plots, the source probe is connected to the conductive carbon tape, away from the active sensing area to avoid applying pressure to the PSR and I_{DS}-V_{GS} measurements were taken of each pixel with the pressure applied. The on currents at V_{GS} = -5 V and V_{DS} = -5 V were then plotted.

4.4.4.4 Design of the gravure engraved plates



Supplementary Figure S1: Design of the gravure engraved plates. a) Optical images of an engraved plate design with non-contiguous line edge (top left) and the engraved plate used in this paper with a continuous line edge (top right) along with images of the respective patterns printed onto the PET substrate. b) Line edge roughness of the printed patterns from the two engraved plates extracted from the optical images.

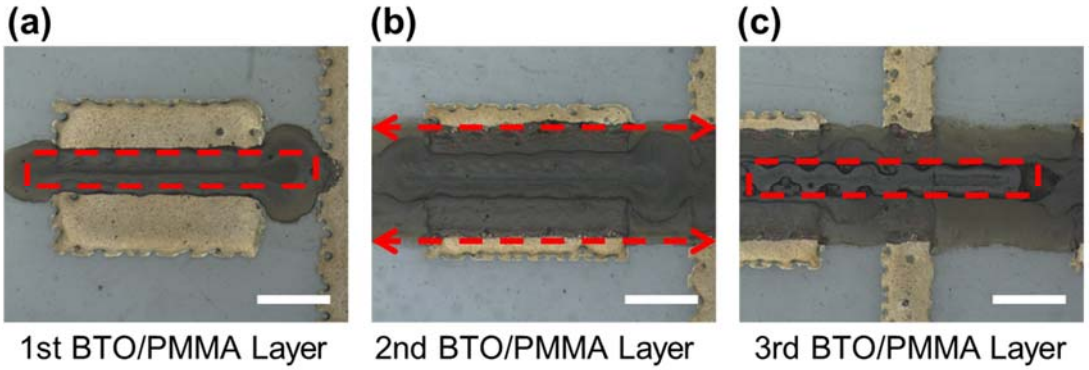
4.4.4.5 Discussion D1: Plate design

Proper design of the gravure engraved plates is critical for minimizing line edge roughness and increasing device yield. The engraved plates consist of halftone wells etched into a chromium plated copper plate. The rheological behavior of the inks during the transfer from the engraved plate onto the substrate is affected strongly by the design of the halftone patterning. When using a pattern with a noncontiguous line edge, the printed ink can spread out from the sides of the engraved plate into the unpatterned areas, causing severe line edge roughness of over ten microns. However, by implementing a continuous line edge into the engraved plate pattern, the inks are unable to spread easily, allowing the line edge roughness to be contained to within one or two microns.

4.4.4.6 Table T1: Ink formulations, print speeds, pressure, and annealing conditions used for the various printed layers of the active matrix backplane.

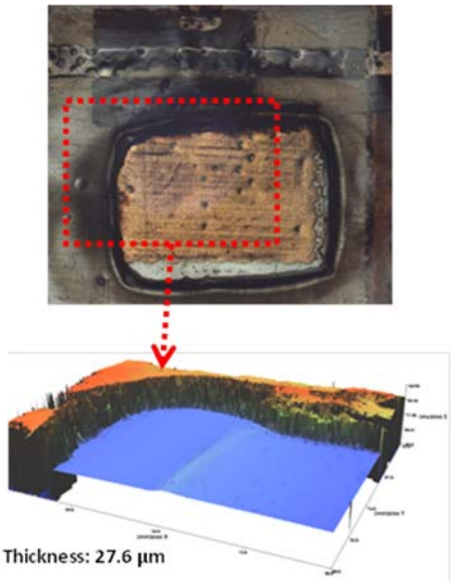
Layer	Ink Formulation	Print Speed (mm/s)	Printing Force (kg)	Annealing Conditions
S/D	PG-007AA	100	5	150 °C for 30 sec
First BTO Layer	PD-100:Butyl Carbitol (10:8)	50	8	150 °C for 60 sec
Second BTO	PD-100:Butyl Carbitol (5:1)	50	8	150 °C for 60 sec
Third BTO	PD-100:Butyl Carbitol (10:8)	50	8	150 °C for 60 sec
Gate	PG-007AA:Ethylene Glycol (10:1)	50	10	150 °C for 1 hour

4.4.4.7 Printing of the BTO gate dielectric



Supplementary Figure S2: Optical microscope images of a pixel after printing of the a) first, b) second, and c) third BTO layers. Scale bars are all 500 µm. First, a thin BTO layer is put between the S/D area (red box in Fig. S2a). After etching the SWCNTs, the second BTO layer cover whole row along the S/D electrodes (indicated with arrows in Fig. S2b) and the third BTO layer is printed over the gate line (red box in Fig. S2c).

4.4.4.8 Thickness of polystyrene encapsulation



Supplementary Figure S3: Optical image of a via through the polystyrene layer (top) and a profilometer measurement of the via (bottom) shown to be 27.6 µm.

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Chapter 5 Conclusion

As advancements in electronics continues, devices with more varying capabilities will arise, necessitating the development of novel processing techniques. In this this dissertation, multiple novel materials processing and growth techniques have been presented as potential methods for achieving such goals, whether it be for III-V integration on silicon, stretchable electronics, or flexible electronics systems.

In Chapter 2, a novel growth method enabling the direct growth of III-V thin films onto amorphous substrates with near-epitaxial quality is described. Simple transistors and phototransistors are demonstrated to have excellent electronic and optoelectronic performance. The method is scalable up to wafer-scale production as well as can enable growth of multiple layers for 3D electronics. Furthermore, the method is shown to be compatible with in-situ doping techniques as well as the growth of ternary III-V semiconductors with controllable stoichiometries, making it a versatile growth technique enabling the integration of III-V compound semiconductors onto arbitrary substrates.

In Chapter 3, the usage of liquid metals was extended from enabling III-V growth to introduce a new flexible and deformable electronics platform based upon liquid-state components rather than solid-state. In particular, a method for introducing liquid-liquid heterojunctions enables the usage of multiple liquids for various functionalities such as passive interconnects and active sensing channels. Due to the components being in the liquid state, such sensors can undergo extreme amounts of deformation, only being limited by the polymers which enclose them in the form of microchannels.

In Chapter 4, different processing schemes for enabling flexible electronics were further explored. In particular, the usage of solution process carbon nanotubes as the active channel material in flexible TFTs was emphasized. As CNTs are typically p-type as processed, a method for n-type doping was first explored. By using fixed charge which exists in PECVD deposited silicon nitride films, chemical field effect doping occurs when the films are deposited onto CNTs, turning them n-type. This doping mechanism was further extended to other materials systems, in particular the 2D material WSe_2, demonstrating that the process is generic for doping of any materials system, and not just limited to CNTs. Finally, the processing of CNT TFTs by using a printing process rather than traditional CMOS processing (i.e. photolithography, vacuum deposition processes, etc) was explored for high throughput, large format, and low cost applications. A CNT-TFT active matrix backplane was fully printed using silver ink for metal electrodes and a barium titanate oxide gate dielectric with 97% pixel yield. By integrating pressure sensors onto this backplane, mapping of tactile pressure was demonstrated.