Mathematical Compact Models of Advanced Transistors for Numerical Simulation and Hardware Design

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by

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Abstract

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Mathematical compact models play a key role in designing integrated circuits. They serve as a medium of information exchange between foundries and designers. A compact model, which is a set of long mathematical equations based on the physics of each transistor, is capable of reproducing the very complex transistor characteristics in an accurately, fast, and robust manner. This dissertation presents the latest research on compact models for advanced transistor technologies: FinFETs, Ultra-thin body SOIs (UTBSOIs), Gate-All-Around (GAA) FETs, and Negative Capacitance (NC) FETs.

Since traditional transistor scaling had reached limitations due short-channel effects and oxide tunneling, the introduction of FinFET and UTBSOIs in high-volume manufacturing at 20nm, 14nm and 10nm technology nodes had let the electronic industry to keep obtaining performance and density advantages in technology scaling. For smaller nodes such as 5nm, and 3nm, GAA FETs transistors are expected to replace traditional transistors. Production ready compact model for current and future FinFETs are presented in this thesis. The Unified Compact Model can model FinFETs with realistic fin shapes including rectangle, triangle, circle and any shape in between. A new quantum effects model will also be presented, it enables accurate modeling of III-V FinFETs. Shape agnostic short-channel effect model for aggressive L_G scaling and body bias model for FinFETs on bulk substrates are also included in this work. This computationally efficient model is an ideal turn-key solution for simulation and design of future heterogeneous circuits.

For extremely scaled technologies, NC-FETs are quickly emerging as preferred candidates for digital and analog applications. The recent discovery of ferroelectric (FE) materials using conventional CMOS fabrication technology has led to the first demonstrations of FE based NC-FETs. The ferroelectric material layer added over the transistor gate insulator help in several device aspects, it suppress short-channel effects, increase on-current due voltage amplification, increase output resistance in short-channel devices, etc. These exciting characteristics has created an urgency

for analysis and understanding of device operation and circuit performance, where numerical simulation and compact models are playing a key role.

This thesis gives insights into the device physics and behavior of FE based negative capacitance FinFETs (NC-FinFETs) by presenting numerical simulations, compact models, and circuit evaluation of these devices. NC-FinFETs may have a floating metal between FE and the dielectric layers, where a lumped charge model represents such a device. For a NC-FinFET without a floating metal, the distributed charge model should be used, and at each point in the channel the FE layer will impact the local channel charge. This distributed effect has important implications on device characteristics. These device differences are explained using numerical simulation and correctly captured by the proposed compact models. The presented compact models have been implemented in commercial circuit simulators for exploring circuits based on NC-FinFET technology. Circuit simulations show that a quasi-adiabatic mechanism of the ferroelectric layer in the NC-FinFET recovers part of the energy during the switching process of transistors, helping to minimize the energy losses of the wasteful energy dissipation nature of conventional transistor circuits. As circuit load capacitances further increase, V_{DD} scaling becomes more dominant on energy reduction of NC-FinFET based circuits.

To my family: Past, Present and Future.

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could improve it.

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marked me a lot and encourage me to keep teaching.

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Finally, I would like to remember my dear friend Patricio Mora. He was my best friend in my childhood, we did bike a lot. Sadly you passed away during my study at Berkeley, but before that you showed the entire world how strong you were. Pato, was the best cyclist Chile could have had, he hold many national records on track cycling, and no one could beat him in the road. The last 10 years of his life he fought cancer as a true warrior, you never gave it up, and no one could have done so. I want to thank you for letting me study so far away from you, I know it was difficult for you, and I am sorry for not being there as much as you needed. I am happy we got to say goodbye. Just after the week you passed away, I got to bike, for real, and to later compete. I would always think about you when I am riding and have chats as we did as kids. Thank you for being my inspiration all these years. We will meet again my friend.

Chapter 1

Introduction

Since the early 60's, the entire semiconductor industry, including design and fabrication of semiconductor devices and circuits, have become one of the most important industry driving the economy, reaching to a $339 Billion industry in 2016 [3]. Indeed, the semiconductor industry is widely recognized as a key driver and technology enabler for the whole electronics value chain [2]. However, the biggest impact of the semiconductor industry may not be in the economic aspect but in the profound social effects of it in our lives. We are constantly rethinking and changing most of our living styles of the past decades due new semiconductor products and services. Nowadays, technology is strongly present in every aspect of our lives. We use semiconductor technology to travel, to communicate, to learn, to do business, to diagnostic diseases, and to live in comfort; therefore, it is clear that needs and demands for technology will keep on rising.

The main factor of the rapidly increasing impact of semiconductor industry is the constant transistor miniaturization. The minimum feature size has been reduced over three order of magnitude since the 60's, as shown in figure 1.1, reaching the nanoscale regime in the past few years [30]. The ever-increasing density of transistors per chip, called Moore's Law [56], has allowed the constant addition of new functionality under the same footprint of semiconductor. In the same direction, each new generation of scaled-down transistors could actually perform better and better, called Dennard's Law [20], leading to faster products or designs where energy is better utilized. To understand the impact of semiconductor scaling in our lives, let's compare two familiar products shown in figure 1.2: the Nokia 3310 and the iPhone X [4]. The Nokia 3310, a popular phone of the year 2000, used an ARM7TDMI processor with a minimum feature transistor size of $1\mu m$, approximately. It contained around half a million transistors with a die size of $68.51mm^2$. The phone was quite simple, it used GSM mobile technology, it had a 84x84 pixel pure monochrome display, and, off course, it had the popular Snake II game. 17 years later, the iPhone X was launched [4]. It uses an Apple A11 Bionic chip, with a minimum feature transistor size of 10nm. It contains over 4.3 billions transistor with a die size of $87.66mm^2$. This phone is

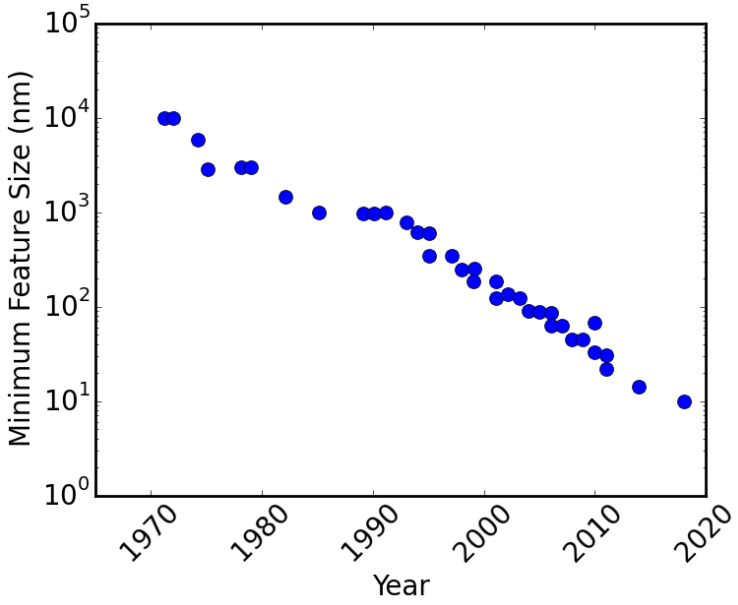

Figure 1.1. The gate length of transistor has been continuously shrank from 10μm to 10nm [30].

much more complex than the Nokia 3310, it has six-core CPUs, three-core graphics processing units (GPU) (mainly to support computational photography functions), neural network hardware ("Neural Engine"), and many many more functions. In summary, the aggressive scaling of semiconductor technology have drastically changed the same base-line product, a cellphone, in our life time, from just be able to do calls, send texts, and playing Snake, to having live calls to people around the world, send Animojis and other important machine learning tasks.

Designing an Integrated Circuit (IC) requires a mathematical compact model (or Spice model) for circuit simulation [13]. Using design rules and the SPICE models, provided by foundry partners, design teams can simulate, design and test their IC architectures. A compact model, which is a set of long mathematical equations based on the physics of each transistor, is capable of reproducing the very complex transistor characteristics in an accurate, fast, and robust manner. In the implementation of circuit simulators, compact models are preferred over other numerical approaches (figure 1.3) because the former can offer, in addition to good computational efficiency, good accuracy [66]. The good accuracy of a compact model mainly relies in the amount of physics and the assumptions behind its mathematical derivation. For example, FinFETs are constructed in the nano-scale regime; therefore, accurate compact models must include several physical effects: charge quantization, gate oxide tunneling, gate capacitance degradation, SCEs, etc.

Figure 1.2. Left: Nokia 3310, 2000, with half million transistors. Right: iPhone X [4], 2017, with more than 4.3 billion transistors.

1.1 Mathematical Models for FinFETs and UTB-SOIs

The constant reduction of minimum feature size has been accompanied by the incorporation of new transistor geometries and materials, figure 1.4, creating the increasing need of new and faster compact models. Several device structures are modeled in this thesis are shown in figure 1.5. For example, Intel has introduced the FinFET structure at 22nm node. UTBSOI has been also recently adopted in sub-20nm IC technologies [55, 65, 59] as an alternative to FinFET technology [7, 88, 47], as both technologies are replacements of the conventional bulk planar technology. Compact models for these two new architectures are presented on this thesis. For the FinFET device, several effects are included, such as 3-dimensional nature of the transistor, bulk effects, quantum mechanical effects, etc. For the UTBSOI, the main effect included is the back-side inversion, which plays a key role in device performance and characteristics. For even smaller nodes, gate-all-around (GAA) FETs are the main transistor candidate for ultimate scaling. In GAA FETs the gate wraps the channel from all the sides improving short-channel effects and increasing on current [42]. Nowadays's GAA structures have taken different shapes like cylindrical FET also named as nanowire (NW) transistors or vertically stacked horizontal Si nanowires [53], all modeled by the proposed Universal FinFET Model.

Most of the compact models are based on a "core model", which is a model obtained using a long-channel assumption, so called gradual-channel-approximation

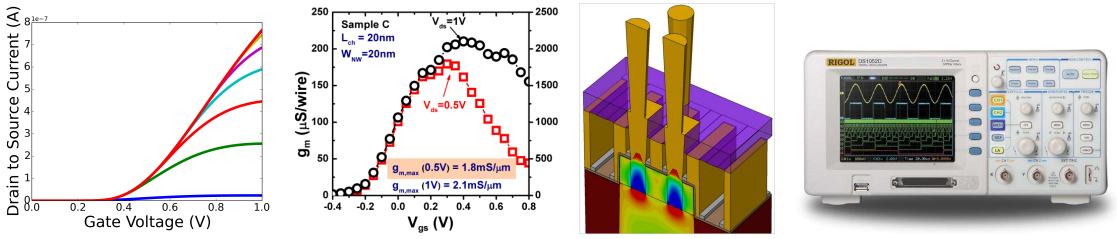

Figure 1.3. Compact Model vs.: Look-Up Table, TCAD Simulation, and Experiment. The advantage of compact models, for hardware design, over other design and simulation approaches are accuracy (∼1% RSM), simulation robustness (smooth and continuous), speed ($\sim 10\mu s$), and affordability (open source).

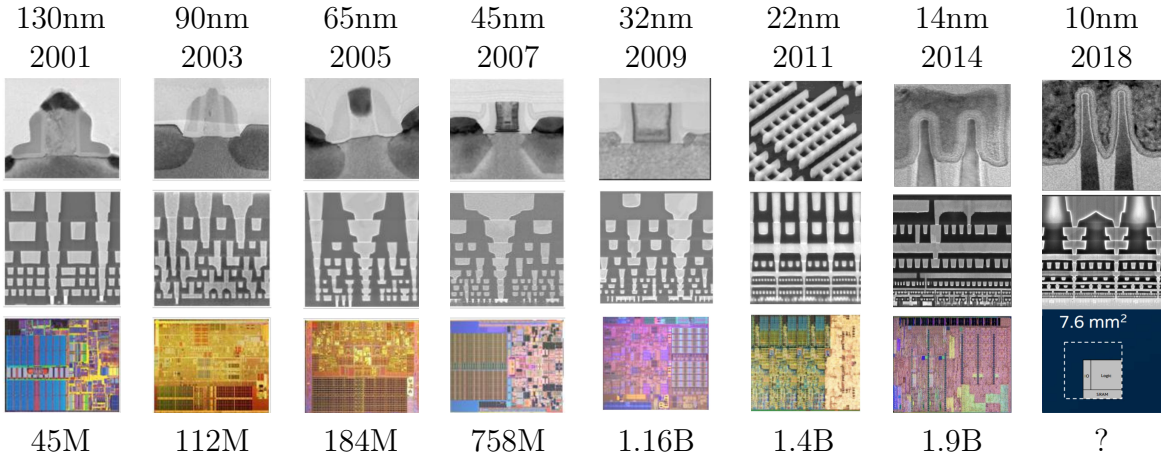

Figure 1.4. Technology node, year, device, metal layers, die, and number of transistor for different Intel processes.

(GCA) [69], and simplifying other physical effects like charge quantization or gate oxide tunneling. Figure 1.6 shows a simplified diagram of a compact model. First, a charge model is obtained by solving Poisson's equation. Once charge model is obtained, drain current is calculated from transport equations. A core model is crucial for the completed compact model because it gives the basis of a mathematical framework which is continuous and smooth, a key requirement for a robust model. In this context, core models are further improved by the inclusion of correction terms that represent advanced physical effects [66, 28]. Regularly, core models are obtained by solving Poisson's equation under the GCA condition and assuming Boltzmann's statistics for the carriers. Even though the use of GCA condition and Boltzmann's statistics alleviates the difficulty in obtaining a solution from Poisson's equation, a direct analytical solution is only available for the cases of undoped double-gate (DG) [84] and cylindrical (Cy) gate-all-around (Cy-GAA) FETs [16], where the three-dimensional Poisson's equation can be reduced to a one-dimensional form. If depletion charges

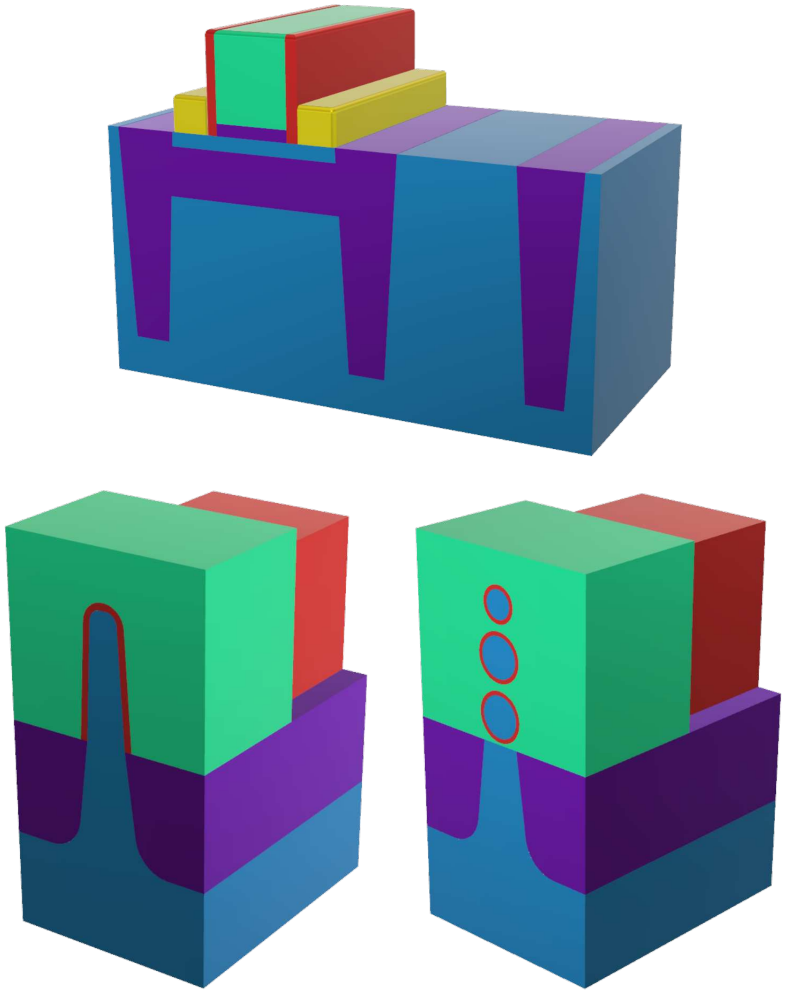

Figure 1.5. Cross-sectional views of device structures modeled in this thesis: UTBSOI, FinFETs, and GAA FETs.

arisen from dopants are included, Poisson's equation becomes highly non-linear. It is then more challenging to obtain a direct analytical solution [29, 54, 28, 51, 50]. However, in realistic FinFETs, doping is needed to be used for multiple threshold voltage devices that are required in contemporary system-on-chip (SoC) technologies for better power-performance-area trade-off [48], thus core models including doping effects must be developed. Finding a direct analytical solution becomes even more difficult to obtain for complex FinFET geometries because they lack structural symmetry [91]. Indeed, compact models for asymmetric geometries, such as triple-gate (TG), rectangular (Re) GAA , or Pi-gate FETs, are rarely found in literature and are only accomplished by the extensive use of fitting parameters or numerical techniques [86, 91, 57, 58]. However, some of these asymmetric geometries offer simpler fabrication processes than other symmetric geometries [70]. Therefore, it is impor-

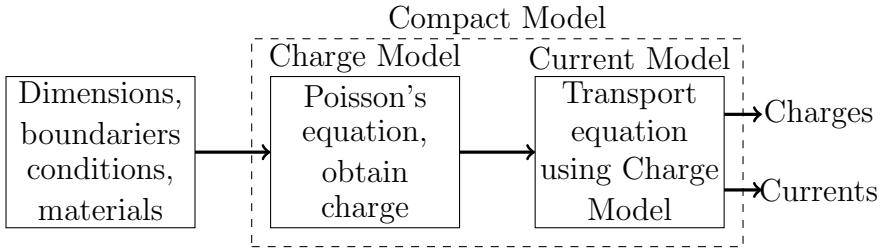

Figure 1.6. Simplified flow of a compact model development.

tant to develop a physical-based core model for FinFETs with complex geometry, for comprehensive understanding and circuit design.

1.2 Negative Capacitances FETs

As the semiconductor industry is reaching extremely small features, Moore's Law [56] and Dennard's Law [20] have been coming to an end, creating the need of new transistor concepts. This is the reason why we are all very familiar with the idea that one of the industry's biggest concern today is about power consumption and one of the best way is to reduce the power supply voltage V_{DD} because power is proportional to V_{DD}^2 squared. Figure 1.7 shows the subthreshold characteristic of different device technologies. The last generation of planar transistors have approximately 100mV/dec of subthreshold swing. FinFET significantly improves the subthreshold swing; indeed, today a FinFET technology gets very close to the theoretical 60mV/dec of swing. However, the entire industry need to reduce the V_{DD} even further. It would be great to reduce the subthreshold swing to be lower than the 60mV/dec; even further, an amplification of the current in the strong bias condition is needed to obtain a good I_{on} while using much lower V_{DD}. In other words, a transistor with the capability of amplifying the gate voltage is needed, i.e., when a voltage of 0.5V is applied to the gate, the channel will see 0.7V volt and the total current in all regimes is amplified. One promising way to do this amplification is using Negative-Capacitance FET [80, 10], where a conventional transistor structure is changed by including a ferroelectric (FE) material in the gate stack. NC-FETs are quickly emerging as promising devices to achieve sub-60 mV/decade sub-threshold slope and high I_{on} [80, 10] to further continue Moore's Law [56] and Dennard's Law [20] for few node more. NC transistor structure is shown in figure 1.8. Under the gate metal there is a ferroelectric material, in this case, hafnium zirconium oxide. It seats on an interfacial oxide and that sits on the silicon substrate. Hafnium zirconium oxide is an acceptable or safe material to use in the IC fabs. Hafnium oxide is a standard material used today as a high-K dielectric; then, by doping it with some zirconium (or other doping that can achieve the same result) it is possible to make

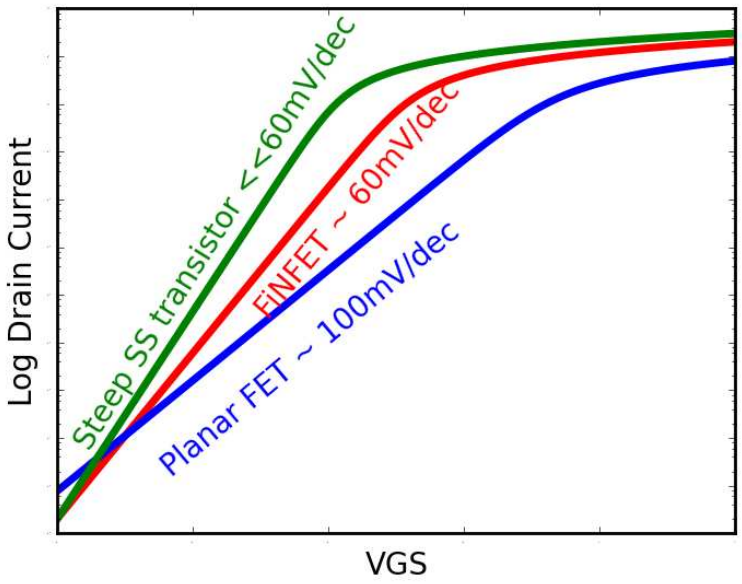

Figure 1.7. Subthreshold characteristic of different device technologies. Devices with Sub 60mV/dec are needed for further V_{DD} scaling.

the Hafnium zirconium oxide ferroelectric [62, 61, 60]. A ferroelectric characteristic is shown in figure 1.9 The slope of figure 1.9 represents the capacitance of the ferroelectric material. In the middle region, as voltage is increased charge decreases; therefore, the ferroelectric is in the negative capacitance regime. This characteristic is the one that Professor Salahuddin [80] used to propose the negative capacitance concept. The amount of people that work on this concept keeps growing year by year and new advances have been reported. In IEDM 2017, Globalfoundries is presenting their NC-FinFETs using standard FinFET fabrication [9]. The working principle of a NC transistor can be simply explained using a two capacitor network. The top capacitor is the one having the ferroelectric material, hafnium zirconium oxide, called C_{FE}. The bottom capacitor C_{mos} is the conventional MOS transistor, where the starting point of the C_{mos} capacitor is at the interface of the hafnium zirconium oxide and the interfacial oxide, and the end point is the channel capacitance itself, including the transistor channel-body capacitance all together. Having two capacitors in series, what determines the voltage at that interface interfacial oxide and ferroelectric is the voltage divider:

$$V_{INT} = \frac{C_{FE}}{C_{FE} + C_{MOS}} V_G \tag{1.1}$$

Since $C_{FE} < 0$, we can obtain a total voltage amplification. This is what can give us a swing better than 60mV/dec, even more, an amplification in the strong inversion as well. Figure 1.10 shows results from IEDM 2015 where this concept has

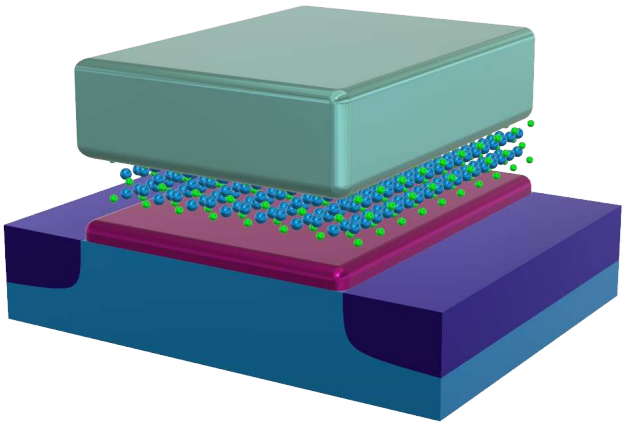

Figure 1.8. Negative Capacitance transistor structure in a conventional planar technology. Ferroelectric material is between interficial layer and metal gate.

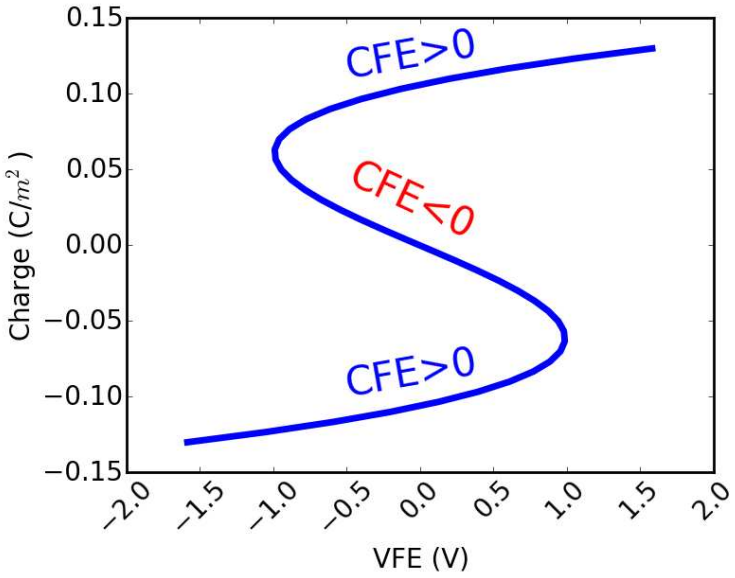

Figure 1.9. Charge as a function of ferroelectric voltage from Landau-Devonshire Theory of Ferroelectrics. Slope represents capacitance sign.

been already measure experimentally. This thesis goal is to present different device simulation and compact models for the NC-FinFETs. Using them, details of the working principles of NC-FETs can be understood and simulated.

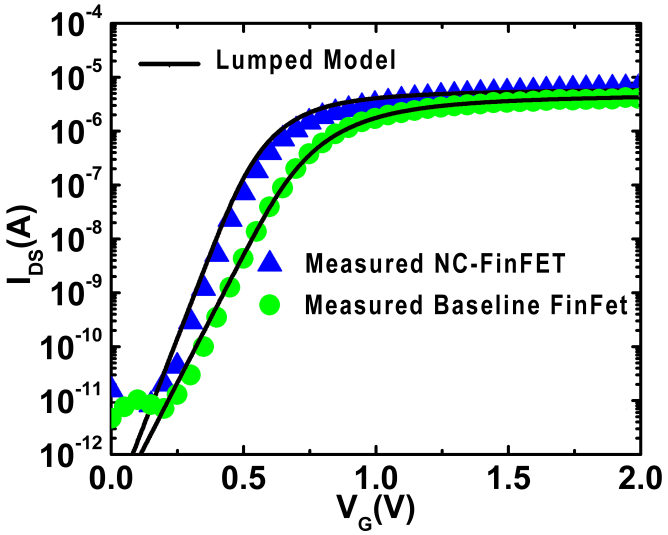

Figure 1.10. NC-FinFET versus base-line FinFET. Sub 60mV/dec is obtained using the NC-FinFET structure [46, 38].

Chapter 2

Model for Double-Gate FinFETs

2.1 Introduction

The core model used in previous versions of BSIM-CMG was based on a solution of Poisson's equation for a long-channel double-gate FinFET, assuming a finite doping in the channel to mimic the doped channels currently used in FinFET fabrication [48]. It is challenging to obtain a direct analytical solution of the Poisson equation of doped FinFETs due to the high non-linearity of the equation; therefore, to overcome this limitation, perturbation approach was used to approximately solve the Poisson's equation in the presence of body doping [29, 28]. The work presented in this chapter shows improvements from models in [29, 28], and the final implementation of the proposed code is implemented in Verilog-A code for the BSIM-CMG108 version [1].

Figure 2.1 shows a 2-D cross-section of a double-gate FinFET which is being used as a reference for the model derivation. Poisson's equation, assuming gradual channel approximation (GCA), Boltzmann's distribution for the inversion carriers, and considering only mobile carries (e.g. electrons in an NMOS FinFET), can be expressed as:

$$\frac{\partial^2 \psi\left(x,y\right)}{\partial x^2} = \frac{q}{\varepsilon_{\rm ch}}\left(n_i e^{\frac{\psi(x,y)-\psi_B-V_{\rm ch}(y)}{V_{\rm tm}}} + N_{\rm ch}\right) \tag{2.1}$$

where $\psi(x,y)$ is the electrostatic potential in the channel, q is the magnitude of the electronic charge, n_i is the intrinsic carrier concentration, $\varepsilon_{\rm ch}$ is the dielectric constant of the channel (fin), $V_{\rm tm}$ is the thermal voltage given by k_BT/q, where k_B and T are the Boltzmann constant and the temperature, respectively; $V_{\rm ch}$ is the quasi-Fermi potential of the channel ($V_{\rm ch}(0)$ =$V_{\rm s}$ and $V_{\rm ch}$(L) =V_d) which only has a y spacial dependence, $N_{\rm ch}$ is the channel doping, and ψ_B=$V_{\rm tm}\ln\left(N_{\rm ch}/n_i\right)$. Note that equation (2.1) is a 1-dimensional Poisson equation, the other two dimensions have been neglected due the long length of the channel (GCA condition) and the symmetry of the double-gate structure in the z direction. In other FinFET geometries,

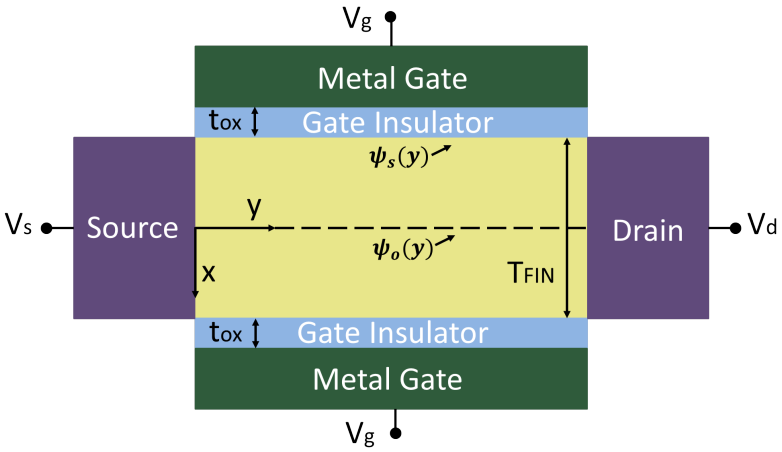

Figure 2.1. Schematic of a symmetric Double-Gate FinFET.

where channel length is short and fin cross-sections are complex, full three-dimensional Poisson equation must be solved.

Figures 2.2, 2.3 and 2.2 shows fin potential versus fin position obtained from equation (2.1) for different conditions. Equation (2.1) has been solved numerically using finite element method to generate the fin potential data (see appendix A for details). Using these results, there are several points that must be contrasted with conventional planar MOSFETs. For example, as show by figures 2.2 and 2.3, the center potential is not fixed as in the case of the bulk potential in planar MOSFETs. Indeed, center potential has a different value depending on the bias condition and it tends to a fixed value in the strong operation regime. In addition, FinFETs may not require the use of high doping concentration for the channel to counter short channel effects. In this context, lightly doped fins consequently increase carrier mobility and reduce device variability coming from random dopant fluctuations. The use of lightly doped channels implies that potential in the subthreshold region is mostly flat, as shown by figure 2.2, which makes the mobile carries and subthreshold current to be proportional to the fin thickness. Thus, in order to decrease leakage, fin thickness must be scaled down. Including dopants in the channel can also be a good option for multiple threshold FinFETs [48]. Figure 2.3 show how the potential changes when a heavily doped fin is used. The potential in the subthreshold region is bent due the ionized dopants, which change the threshold of the device depending on the amount of dopants and thickness of the fin. Finally, another important point to notice is that as thickness of the fin is decreased, the potential in the center of the channel increases as shown by figure 2.3. An increment of the center potential increases the amount of mobile carriers in the center of the fin where mobility is larger than the surface, thus higher mobility could be obtained for those carriers. Figures 2.2, 2.3 and 2.2 were obtained by a numerical solution which is not suitable for a compact modeling

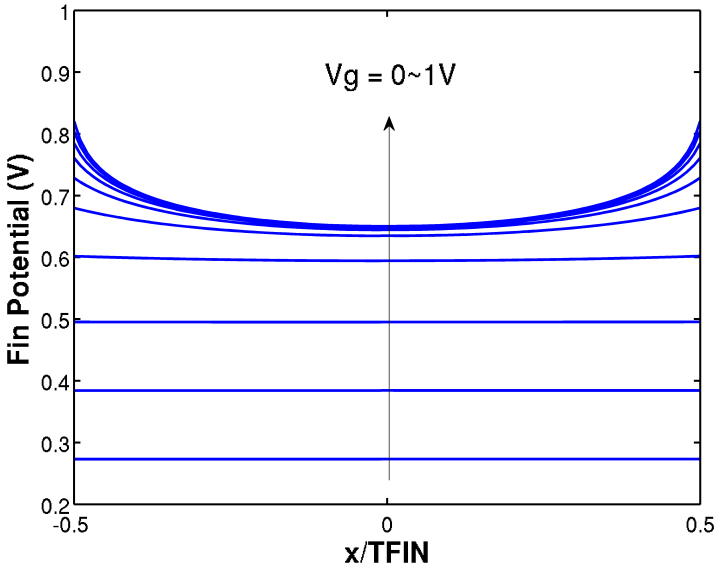

Figure 2.2. Fin potential versus position obtained from the numerical solution of equation (2.1) for a lightly doped fin. $N_{ch} = 1\times10^{15} cm^{-3}$, $TFIN = 20nm$, $t_{ox} = 1nm$ and $V_{ch} = 0V$ have been used for simulation.

perspective; therefore, a compact model would be presented starting from equation (2.1).

2.2 Model Derivation

In order to obtain the potential in the channel for equation (2.1), ψ is written following the perturbation approach [28]:

$$\psi\left(x,y\right) \cong \psi_1\left(x,y\right) + \psi_2\left(x,y\right) \tag{2.2}$$

Here, ψ_1 is the potential contribution due to the inversion carriers and without the effect of the ionized dopants, $N_{\rm ch}$, and is given by

$$\frac{\partial^2\psi_1(x,y)}{\partial x^2} = \frac{qn_i}{\varepsilon_{\rm ch}} e^{\frac{\psi_1(x,y)-\psi_B-V_{\rm ch}(y)}{V_{\rm tm}}} \tag{2.3}$$

and ψ_2 is the potential contribution due to the presence of the ionized dopants $N_{\rm ch}$, and without the effect of the inversion carriers. It is the perturbation potential and is given by

$$\frac{\partial^2\psi_2(x,y)}{\partial x^2} = \frac{qN_{\rm ch}}{\varepsilon_{\rm ch}} \tag{2.4}$$

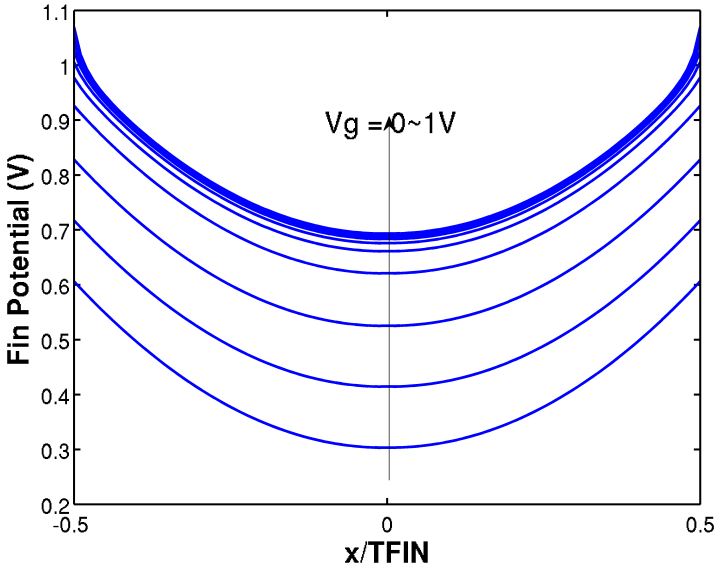

Figure 2.3. Fin potential versus position obtained from the numerical solution of equation (2.1) for a doped fin. $N_{ch} = 5 \times 10^{18} cm^{-3}$, $TFIN = 20nm$, $t_{ox} = 1nm$ and $V_{ch} = 0V$ have been used for simulation.

The geometrical symmetry of a double-gate FinFET leads to the fact that the vertical component of the electric field $\mathcal{E}_x$ at the center of the channel is zero, then it is possible to integrate (2.3) twice to obtain $\psi_1(x, y)$ as a function of the potential in the center of the body $\psi_0(y)$:

$$\psi_1(x,y) = \psi_0(y) - 2V_{\text{tm}} \ln\left[\cos\left(\sqrt{\frac{q}{2\varepsilon_{\text{ch}}V_{\text{tm}}}\frac{{n_i}^2}{N_{\text{ch}}}e^{\frac{\psi_0(y)-V_{\text{ch}}(y)}{V_{\text{tm}}}}} \times \frac{x}{2}\right)\right] \tag{2.5}$$

In order to find ψ_2, it is also possible to apply $\mathcal{E}_x = 0$ at the center of the channel and setting $\psi_2(x = 0, y) = 0$. Then, integrating (2.4) twice, it is possible to obtain

$$\psi_2(x,y) = \frac{qN_{\text{ch}}x^2}{2\varepsilon_{\text{ch}}} \tag{2.6}$$

The surface potential ψ_s at any point y along the surface is obtained by evaluating the sum of ψ_1 and ψ_2 at the surface of the fin:

$$\psi_s(y) \cong \psi_1(-T_{\text{fin}}/2, y) + \psi_2(-T_{\text{fin}}/2, y) \tag{2.7}$$

Gauss's law and the boundary conditions at the channel-insulator interface lead to a second important equation:

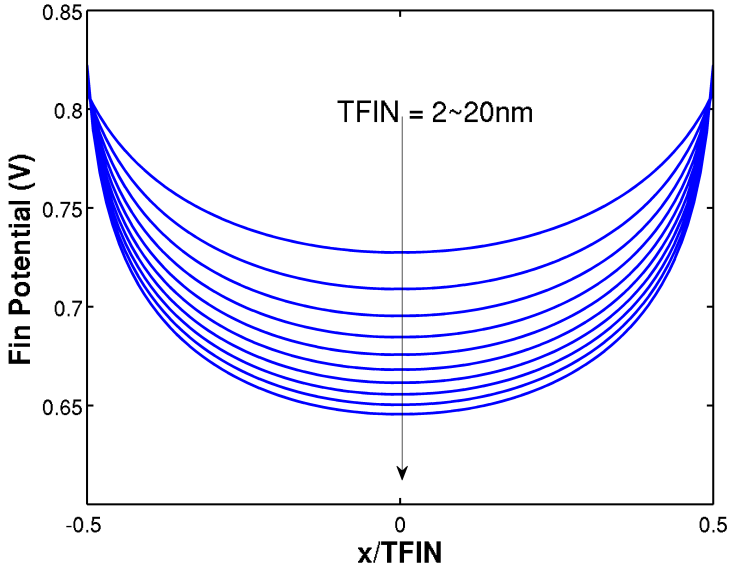

Figure 2.4. Fin potential versus position obtained from the numerical solution of equation (2.1) for different fin thickness at strong inversion bias. $N_{ch} = 1 \times 10^{15} cm^{-3}$, $V_{ch} = 0V$, $TFIN = 20nm$, $t_{ox} = 1nm$ and $V_g = 1V$ have been used for simulation. As TFIN decreases, center potential increases, which increases the number of mobile carriers in the center of the fin.

$$V_{\text{gs}} = V_{\text{fb}} + \psi_s(y) + \varepsilon_{\text{ch}}\mathcal{E}_{\text{xs}}/C_{\text{ox}} \tag{2.8}$$

where V_{gs} is the gate voltage, V_{fb} is the flat-band voltage, C_{ox} is the gate oxide capacitance per unit area, given by $\varepsilon_{\text{ox}}/T_{\text{ox}}$, where ε_{ox} and T_{ox} are the oxide dielectric constant and oxide thickness, respectively, $\mathcal{E}_{\text{xs}}$ is the vertical component of the electric field at the surface, which can be obtained by integrating (2.1):

$$\mathcal{E}_{\text{xs}} = \sqrt{\frac{2qn_i}{\varepsilon_{\text{ch}}}\left[V_{\text{tm}}\left(e^{\frac{\psi_s(y)}{V_{\text{tm}}}} - e^{\frac{\psi_0(y)}{V_{\text{tm}}}}\right)e^{\frac{-\psi_B - V_{\text{ch}}(y)}{V_{\text{tm}}}} + e^{\frac{\psi_B}{V_{\text{tm}}}}\left(\psi_s(y) - \psi_0(y)\right)\right]} \tag{2.9}$$

Equations (2.7) and (2.8) represent a self-consistent system of equations that can be used to obtain ψ_0 and ψ_s. However, through a change of variable, given by

$$\beta = \sqrt{\frac{q}{2\epsilon_{ch}V_{tm}}\frac{n_i^2}{N_{ch}}e^{\frac{\psi_0 - V_{ch}}{V_{tm}}}}\frac{T_{FIN}}{2} \tag{2.10}$$

equations (2.7) and (2.8) can be written as a single equation:

$$f(\beta) \equiv \ln(\beta) - \ln(\cos(\beta)) - \frac{V_{\rm gs}-V_{\rm fb}-V_{\rm ch}}{2V_{\rm tm}} + \ln\left(\frac{2}{T_{\rm fin}}\sqrt{\frac{2\varepsilon_{\rm ch}V_{\rm tm}N_{\rm ch}}{q{n_i}^2}}\right) + \frac{2\varepsilon_{\rm ch}}{T_{\rm fin}C_{\rm ox}}\sqrt{\beta^2\left(\frac{e^{\frac{\psi_{\rm pert}}{V_{\rm tm}}}}{\cos^2(\beta)}-1\right)+\frac{\psi_{\rm pert}}{{V_{\rm tm}}^2}\left[\psi_{\rm pert}-2V_{\rm tm}\ln(\cos(\beta))\right]} = 0 \tag{2.11}$$

where ψ_{pert} is given by ψ_2 evaluated at $x = T_{fin}/2$. Equation (2.11) is an implicit equation in β which must be solved using numerical methods. Then, once β is calculated, the surface potential and the charge in the channel can be obtained. Figure (2.5) shows the surface potential obtained from equation (2.11) and the numerical solution of equation (2.1) for different doping concentrations. The amount of doping in the channel determines the threshold voltage of the device as shown by figure 2.6 which represents the mobile charge density obtained from proposed compact model and the numerical solution of equation (2.6) for different doping concentrations. In the case of lightly doped DG FinFETs, the thickness of the channel determines the amount of mobile carrier charge density in the channel in a linear manner as shown in figure 2.7.

Solving equation (2.11) using numerical methods is not practical for compact modeling applications because the use of them increase the computation time and may cause convergence problems [90]. Therefore, equation (2.11) is solved by first using an analytical approximation for the initial guess, followed by two quartic modified iteration [81]. This approach makes the model numerically robust and accurate (see Appendix B). The surface potentials at the source end ψ_s and drain end ψ_d are calculated by setting $V_{\rm ch}$=V_s and $V_{\rm ch}$=V_d, respectively. For a lightly doped body, (2.11) can be simplified further [28] to speed up the simulation. This option can be selected in the BSIM-CMG model by setting the parameter COREMOD. A separate model has been derived for the cylindrical gate geometry, which has been discussed in detail in [87].

In order to complete the core model, the drain to source current $I_{\rm ds}$ model in BSIM-CMG is obtained from a solution of the drift-diffusion equation, assuming a long-channel double-gate FinFET:

$$I_{\rm ds}(y) = \mu(T)\, W Q_{\rm inv}(y)\frac{dV_{\rm ch}}{dy} \tag{2.12}$$

where $\mu(T)$ is the low-field and temperature-dependent mobility, W is the total effective width, and $Q_{\rm inv}$ is the inversion charge per unit area in the body. Equation (2.12) includes drift and diffusion transport mechanisms through the use of the quasi-Fermi potential.

Integrating both sides of (2.12), and considering the fact that under quasi-static operation $I_{\rm ds}$ is constant along the channel, it is possible to express (2.12) in its integral form:

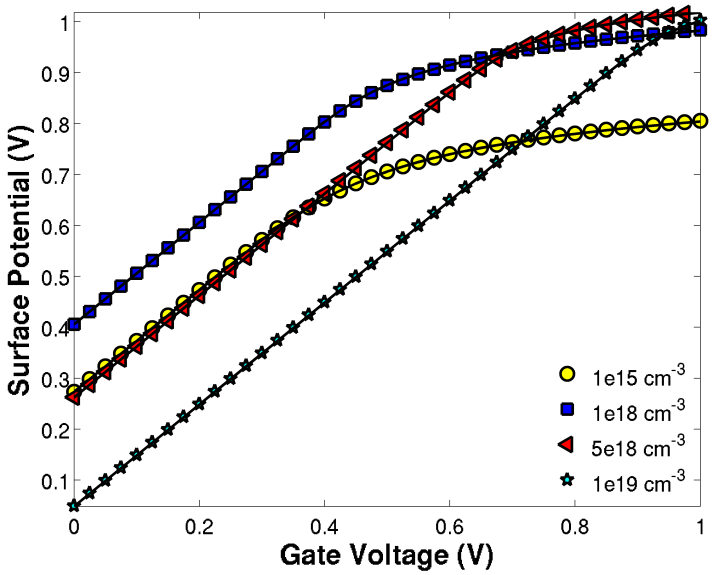

Figure 2.5. Surface potential versus V_G of DG FinFETs ($T_{Fin} = 20nm$) at $V_{DS} = 0.0V$ obtained from the proposed model (lines) and numerical simulations (symbols) for different channel doping.

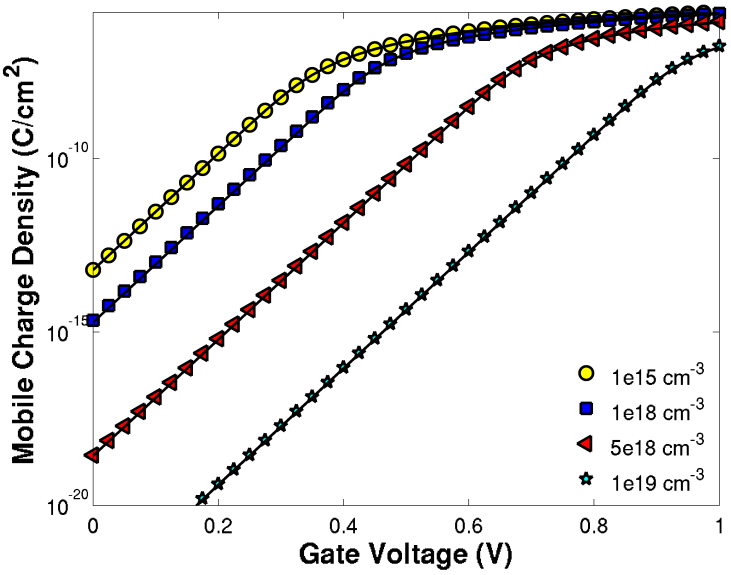

Figure 2.6. Mobile electron charge density versus V_G of DG FinFETs ($T_{Fin} = 20nm$) at $V_{DS} = 0.0V$ obtained from the proposed model (lines) and numerical simulations (symbols) for different channel doping.

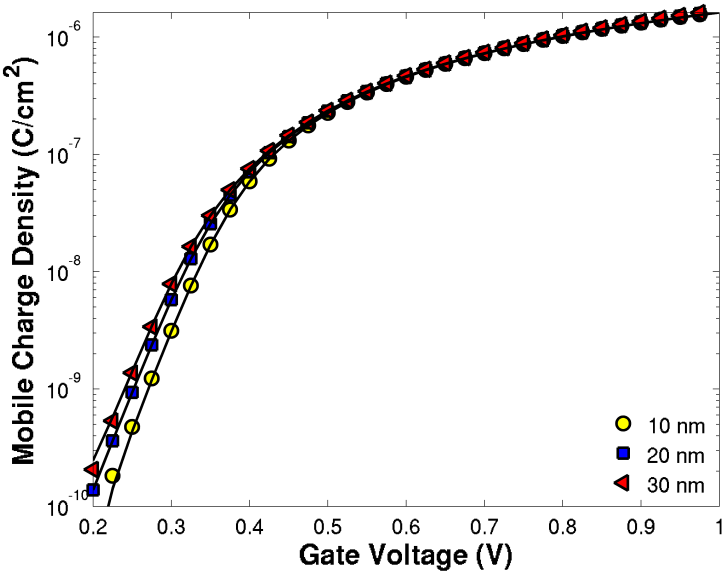

Figure 2.7. Mobile electron charge density versus V_G of DG FinFETs (using intrinsic Fin channel) at $V_{DS} = 0.0V$ obtained from the proposed model (lines) and numerical simulations (symbols) for different Fin thickness.

$$I_{\rm ds} = \frac{W}{L}\mu\left(T\right)\int_{Q_{\rm invs}}^{Q_{\rm invd}} Q_{\rm inv}\left(\frac{dV_{\rm ch}}{dQ_{\rm inv}}\right)dQ_{\rm inv} \tag{2.13}$$

where L is the effective channel length, $Q_{\rm invs}$, and $Q_{\rm invd}$ are the inversion charge densities at the source and drain ends, respectively, given by

$$Q_{\rm inv,d/s} = C_{\rm ox}\left(V_{\rm gs} - V_{\rm fb} - \psi_{d/s}\right) - {\rm Q_{bulk}} \tag{2.14}$$

Here, $Q_{\rm bulk}$ is the fixed depletion charge and is given by $qN_{\rm ch}T_{\rm fin}$ and $\psi_{d/s}$ are obtained by solving (2.11). The term $dV_{\rm ch}/dQ_{\rm inv}$ in (2.13) can be calculated as a function of $Q_{\rm inv}$ using a simple, but accurate, implicit equation for $Q_{\rm inv}$ [28]:

$$Q_{\rm inv}\left(y\right) \approx \sqrt{2qn_i\varepsilon_{\rm ch}V_{\rm tm}}\; e^{\frac{\psi_s(y)-\psi_B-V_{\rm ch}(y)}{2V_{\rm tm}}}\sqrt{\frac{Q_{\rm inv}\left(y\right)}{Q_{\rm inv}\left(y\right)+Q_0}} \tag{2.15}$$

where ${\rm Q_0}={\rm Q_{bulk}}+5{\rm C_{fin}V_{tm}}$, with ${\rm C_{fin}}=\varepsilon_{\rm ch}/{\rm T_{fin}}$. Using this approximation, equation (2.13) can be integrated analytically, leading to the following basic equation for $I_{\rm ds}$:

$$I_{\rm ds} = \mu\left(T\right).\frac{W}{L}.\left[\frac{Q_{inv,s}^2 - Q_{inv,d}^2}{2C_{\rm ox}} + 2V_{\rm tm}(Q_{\rm inv,s} - Q_{\rm inv,d}) - V_{\rm tm}Q_0{\rm ln}\left(\frac{Q_0+Q_{\rm inv,s}}{Q_0+Q_{\rm inv,d}}\right)\right] \tag{2.16}$$

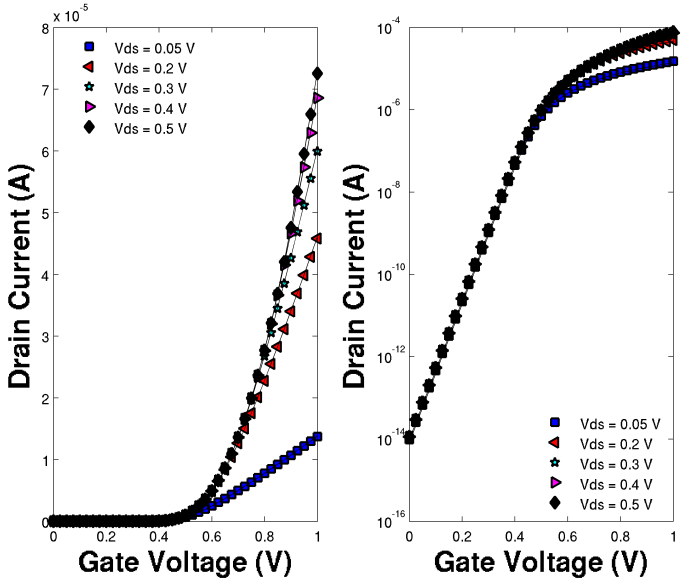

Figure 2.8. Drain current versus V_G of DG FinFETs (using intrinsic Fin channel) at different V_{DS} values obtained from the proposed model (lines) and numerical simulations (symbols). Linear (left) and logarithm (right) scales are shown. $HFIN = L = 1\mu m$, $t_{ox} = 1nm$, $N_{ch} = 1 \times 10^{18} cm^{-3}$, $\mu_e = 100 cm^2 V^{-1} s^{-1}$, and a gate work-function equal to $4.6eV$ have been used for the simulations.

Note that Q_{inv} charges are calculated using (2.11) and (2.13). Figure 2.8 shows an example drain current obtained from the proposed model and numerical simulations. It shows that BSIM-CMG model captures the behaviour of FinFET under all bias conditions: subthreshold, triode, and saturation conditions.

2.3 Conclusion

An explicit surface potential solution has been developed for the implicit model equation derived for BSIM-CMG and implemented in BSIM-CMG108 [1]. The explicit solution is obtained by first deriving a continuous approximate solution of the implicit surface potential equation. It is constructed considering the asymptotic behaviour of the implicit equation under subthreshold and strong inversion conditions. The explicit equation is then completed by updating it using two quartic modified iterations. The explicit model is smooth and continuous and solves convergence problem observed in earlier solution under extreme conditions of doping and width combinations. The proposed model has been tested for variety of doping, temperature, geometry and bias conditions. The model shows excellent accuracy and convergence thereby ready for use in production level design kits.

Chapter 3

Unified FinFET Compact Model

3.1 Introduction

Due to its excellent low power and scaling characteristics, FinFET technology [34] has been adopted in all sub-20nm IC technologies [7, 63, 88, 47] as a replacement of the conventional bulk planar technology. For FinFET transistor technology, the Compact Model Coalition (CMC) has chosen BSIM-CMG [73] as the first and only industry-standard compact model for advanced circuit design. Fast speed, numerical robustness, and good accuracy of a compact model relies on several factors such as the amount of physics in the model or the kind of algorithm used to solve the physical equations. BSIM-CMG compact model includes several physical effects [73, 13]: device geometry effects, charge quantization, gate oxide tunneling, gate capacitance degradation, short-channel effects, etc. It can be used to model different structures as those shown in figure 3.1. Figure 3.2 shows a general diagram of BSIM-CMG compact model. The compact model must be able to calculate terminal (drain, source, gate, bulk/back) currents and charges, which are then utilized by circuit simulator engines to solve a complete circuit under various analyses such as dc, ac, or transient. Terminal voltages are taken as electrical inputs for the compact model (Figure 3.2); thereafter, the model calculates the charge density in the channel of the simulated transistor, part that also requires threshold voltage (V_{TH}) and subhtreshold-swing (SS) calculations. After charge densities are calculated, these quantities are used by the transport model to obtain charge currents for each terminal. The terminal charge model assigns total charge quantities to each terminal, based on the charge density across the device [73]. The following sections are intended to give a background foundation of the new compact models for charge and current modeling that complement the current features of BSIM-CMG [73, 13].

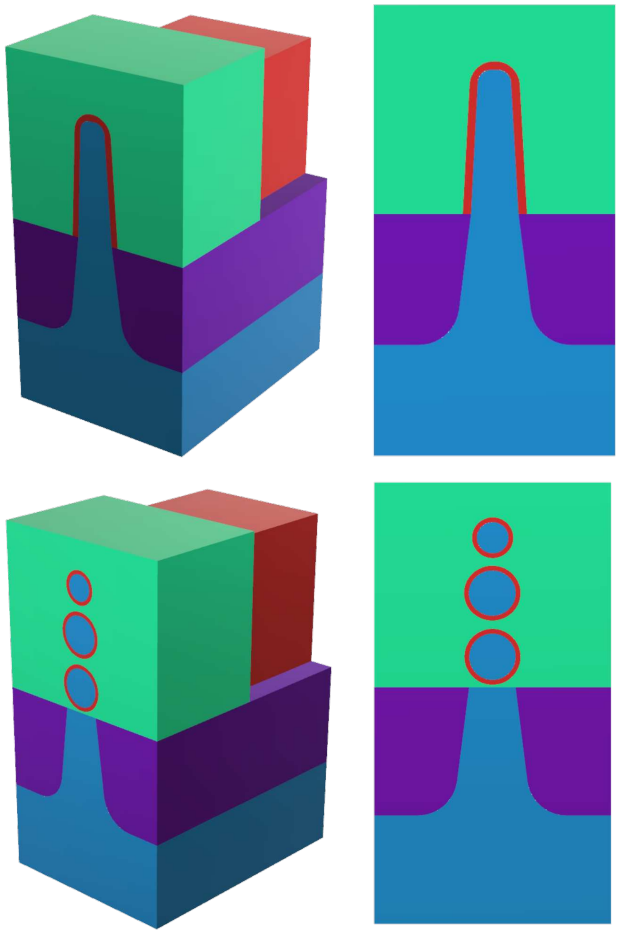

Figure 3.1. 3-dimensional schematic of a FinFET with a complex fin cross-section (top) and GAA FET. The fin shape is similar to industry FinFETs reported in [11, 7].

3.2 Core Model

Most of the device's compact models are based on a "core model", which is a model obtained using a long-channel assumption, so called the gradual-channel-approximation (GCA) [69]. Other advanced physical effects, like charge quantization, are later added as correction terms. The core model of a compact model is a crucial part of the final completed compact model because it gives the basis of a mathematical framework which is continuous, smooth, and numerically robust, which are the key requirements to achieve convergence in circuit simulators.

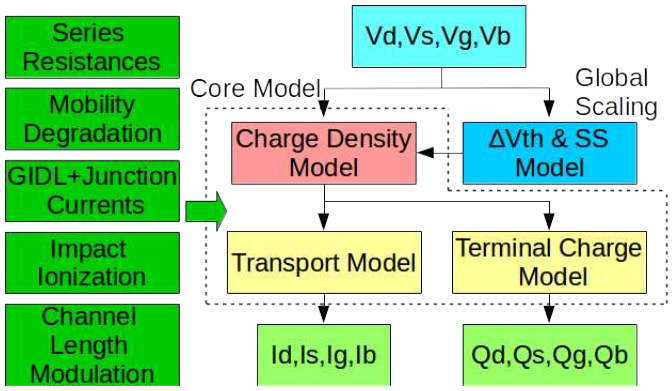

Figure 3.2. General structure of BSIM-CMG compact model calculation flow and model dependence. Core Model is complemented with real device effects sub-models and global scaling model (Not all sub-models are shown).

3.2.1 Unified FinFET Model

The typical rectangular cross-section of FinFETs is hardly found on industry FinFETs. Indeed, whether intentional or due to manufacturing variation, industry FinFET cross-sections are non-uniform and similar to Rounded Trapezoidal shapes [11, 7], as shown by figure 3.1. In order to capture fin shape effects on device performance, a compact model for FinFETs with complex cross-sections is important. In this section, the unified FinFET compact model is presented for devices with complex fin cross-sections. FinFETs structures such as Double-Gate, Cylindrical Gate-All-Around, Rectangular Gate-All-Around or Rounded Trapezoidal Triple-Gate FinFETs, are all modeled under the same framework. A single unified core model is used for different FinFET structures as those shown in figure 3.1, and only model parameters are different for each FinFET structure, which are pre-calculated for each device type and dimension. The proposed core model can be used with Short-Channel-Effects sub-models in a similar manner as being done in previous version of BSIM-CMG models [73]. The model presented in this section has been incorporated to BSIM-CMG [27].

Several compact models have been proposed for FinFETs with complex cross-sectional shapes. The work presented in [91] developed compact models for different undoped or lightly doped FinFETs shapes utilizing a combination of the compact models for DG [84] and Cy-GAA FinFETs [16]. In [17], a compact model for undoped or lightly doped FinFETs was extended to model FinFETs with different cross-sectional shapes by obtaining an equivalent channel thickness for each structure. Another compact model has been proposed for FinFET devices with different cross-sectional shapes [25],[26], where new models for doped FinFETs were developed in a universal model framework. In this section, based on the approach presented in [27], a new normalized unified FinFET core model is presented [27]. The new nor-

malized charge model is obtained from the solutions of the Poisson equation for DG and Cy-GAA FinFETs, which leads to a single closed form relationship between the mobile charge and the applied terminal voltages given as follows [27]:

$$v_G - v_o - v_{ch} = -q_m + \ln(-q_m) + \ln\left(\frac{q_t^2}{e^{q_t} - q_t - 1}\right) \tag{3.1}$$

where v_o and q_t are represented by:

$$v_o = v_{FB} - q_{dep} - \ln\left(\frac{2qn_i^2 A_{ch}}{v_T C_{ins} N_{ch}}\right) \tag{3.2}$$

$$q_t = (q_m + q_{dep}) r_N \tag{3.3}$$

In the previous equations, v_G and v_{ch} are the normalized gate and channel potentials expressed by:

$$v_G = \frac{V_G}{v_T} \tag{3.4}$$

$$v_{ch} = \frac{V_{ch}}{v_T} \tag{3.5}$$

q_m and q_{dep} are the normalized mobile and depletion charges:

$$q_m = \frac{Q_m}{v_T C_{ins}} \tag{3.6}$$

$$q_{dep} = \frac{-qN_{ch}A_{ch}}{v_T C_{ins}} \tag{3.7}$$

r_N is given by:

$$r_N = \frac{A_{Fin} C_{ins}}{\varepsilon_{ch} W^2} \tag{3.8}$$

A_{ch} is the area of the channel, N_{ch} is the doping in the channel, W is the channel width, and C_{ins} is the insulator capacitance per unit length. It is important to notice that in the right side of equation (6.1) there are three terms that determine the behaviour of the charge in the channel. A linear term, which is important in the strong inversion, the first logarithm term, which is important in the subhtreshold region, and the last logarithm term, which is important in the moderate inversion. Therefore, equation (6.1) can represent the mobile carrier concentration in the channel for all bias condition in a continuous and smooth manner, crucial for circuit simulation success.

The normalized drain current is obtained from the solution of the Poisson-carrier transport equation [27] and it is represented by:

$$i_{DS} = \left[\frac{q_m^2}{2} - 2q_m - q_H \ln\left(1 - \frac{q_m}{q_H}\right)\right]\Bigg|_{q_{m,S}}^{q_{m,D}} \tag{3.9}$$

where q_H is equal to:

$$q_H = \frac{1}{r_N} - q_{dep} \tag{3.10}$$

The drain current normalization is given by:

$$i_{DS} = \frac{-I_{DS}L}{\mu_m v_T^2 C_{ins}} \tag{3.11}$$

Equation (3.9) has three terms that determine the behaivor of the current under different bias conditions. The first term, quadratic, is important in the saturation and triode conditions, the second term, linear, is important in the triode and subthreshold conditions, and finally, the last term, logarithm, is important in the subthreshold and moderate inversion conditions. This shows that equation (3.9) represent the drain current characteristics in all regions of device operation, that is, subthreshold, linear, and saturation regions, in a continuous and explicit expression. Considering each region of operation, the proposed model can be reduced to simple expressions. In the subthreshold region, the drain current is approximately given by

$$I_{DS} \approx \frac{\mu}{L} v_T^2 C_{ins} \exp\left(\frac{V_G - V_{TH}}{v_T}\right) \times \left(1 - \exp\frac{-V_{DS}}{v_T}\right) \tag{3.12}$$

where V_{TH} is the threshold voltage of FinFETs [26]. Note that (3.12) is independent of C_{ins} for undoped devices, thus, (3.12) can be further be simplified to:

$$I_{DS} \approx A_{ch} \frac{\mu}{L} v_T q \frac{n_i^2}{N_{ch}} \exp\left(\frac{V_G - V_{FB}}{v_T}\right) \times \left(1 - \exp\frac{-V_{DS}}{v_T}\right) \tag{3.13}$$

Using equation (3.13) it is possible to conclude that to decrease the leakage in lightly doped FinFETs, A_{ch} must be scaled down. The drain currents in the linear and saturation regions are approximately given by

$$I_{DS} \approx \frac{\mu}{L} C_{ins} \left(V_G - V_{TH} - V_{DS}/2\right) V_{DS} \tag{3.14}$$

$$I_{DS} \approx \frac{\mu}{2L} C_{ins} \left(V_G - V_{TH}\right)^2 \tag{3.15}$$

Equations (3.14) and (3.15) are the very well known equations from the quadratic model for conventional long-channel CMOS MOSFETs.

Using the presented results, it should be noted that only four different model parameters are needed for the modelling of FinFET devices: A_{ch}, N_{ch}, W, and C_{ins}. Using these parameters, a FinFET with simple cross-section, such as DG FinFET,

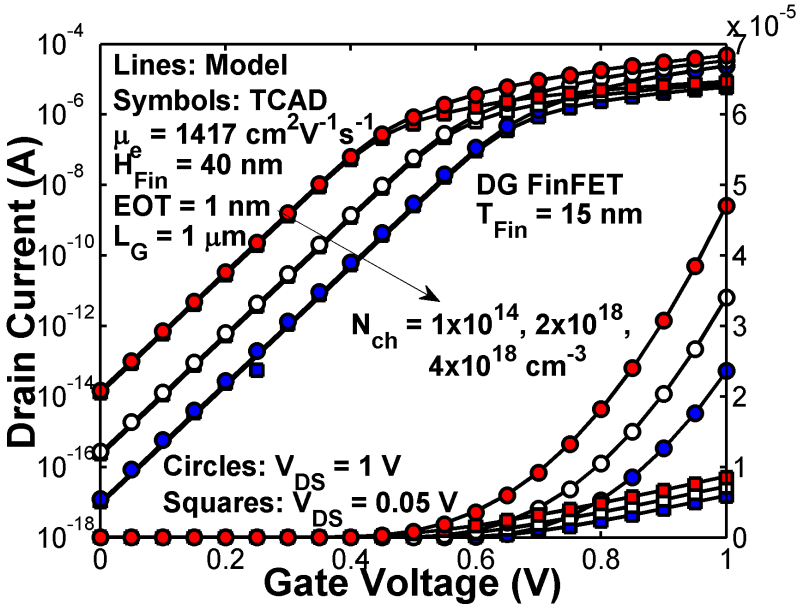

Figure 3.3. Drain current versus gate voltage of DG FinFETs at $V_{DS} = 0.05V$ (squares) and $V_{DS} = 1V$ (circles) obtained from the proposed model (lines) and numerical simulations (symbols) for three different channel doping: $N_{ch} = 1 \times 10^{14} cm^{-3}$ (red symbols), $N_{ch} = 2 \times 10^{18} cm^{-3}$ (empty symbols), and $N_{ch} = 4 \times 10^{18} cm^{-3}$ (blue symbols). $\mu = 1470 cm^2/Vs$, $L_G = 1\mu m$, $T_{CH} = 15nm$, $H_{CH} = 40nm$, $EOT = 1nm$, and metal gate work-function equal to $4.6eV$ have been used.

can be accurately modelled for different channel doping concentrations as shown in figure 3.3. The model parameters used for DG FinFETs are given as follows [27]:

$$A_{ch} = H_{Fin} T_{Fin} \tag{3.16}$$

$$W = 2H_{Fin} \tag{3.17}$$

$$C_{ins} = \frac{\varepsilon_{ins}}{EOT} W \tag{3.18}$$

$$N_{ch} \tag{3.19}$$

A Trapezoidal Triple-Gate FinFET is a good example of a FinFET with a complex cross-section. Indeed, the industry transistors reported in [11] and [7] have fin cross-sections similar to trapezoidal shapes. The proposed model can be used to model these type of devices through the use of the following four model parameters:

$$A_{ch} = H_{Fin} \frac{(T_{Fin,top} + T_{Fin,base})}{2} \tag{3.20}$$

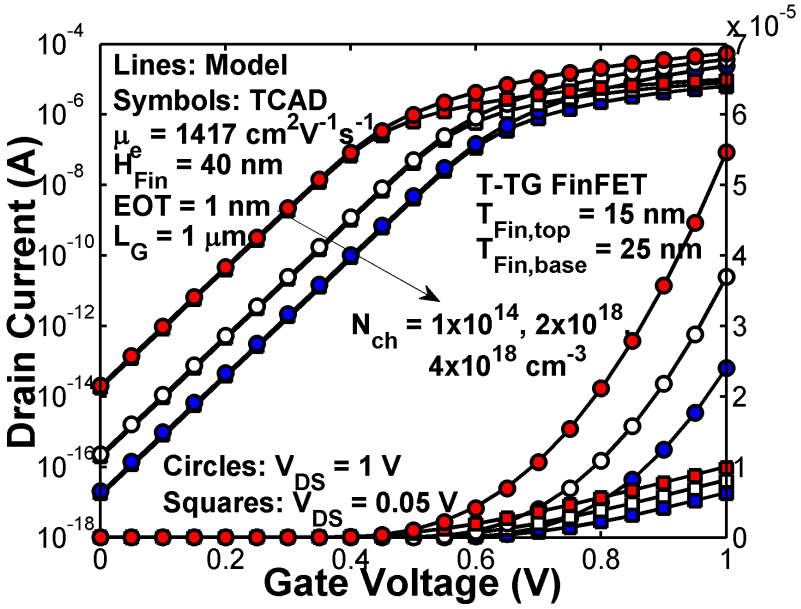

Figure 3.4. I_D versus V_G of Trapezoidal Triple-Gate FinFETs ($T_{Fin,TOP} = 15nm$ & $T_{Fin,BASE} = 25nm$) at $V_{DS} = 0.05V$ (squares) and $V_{DS} = 1V$ (circles) obtained from the proposed model (lines) and numerical simulations (symbols) for three different channel doping: $N_{ch} = 1 \times 10^{14} cm^{-3}$ (red symbols), $N_{ch} = 2 \times 10^{18} cm^{-3}$ (empty symbols), and $N_{ch} = 4 \times 10^{18} cm^{-3}$ (blue symbols).

$$W = 2\sqrt{\frac{(T_{Fin,base} - T_{Fin,top})^2}{4} + H_{Fin}^2} + T_{Fin,top} \tag{3.21}$$

$$C_{ins} = \frac{\varepsilon_{ins}}{EOT} W \tag{3.22}$$

$$N_{ch} \tag{3.23}$$

Using these parameters, Trapezoidal Triple-Gate FinFETs can be accurately modelled as shown in figure 3.4, where a T-TG FinFET has been doped at different doping concentrations as it is used in chips with multi-threshold voltage levels.

In the case of a channel dimension variation, the model can accurately predict the trend of current changes as shown by figure 3.5. Note that a $T_{Fin,top}$ variation is more important for the on-current than a $T_{Fin,base}$ variation. In addition, the off-current linearly varies as function of $T_{Fin,top}$ or $T_{Fin,base}$, as expected.

The proposed model accurately models experimental long channel FinFETs without the use of fitting parameters as shown by figures 3.6 and 3.7, which compare the proposed core compact model and the data from a fabricated long channel FinFET. Note that only the mobility model has been additionally included to the

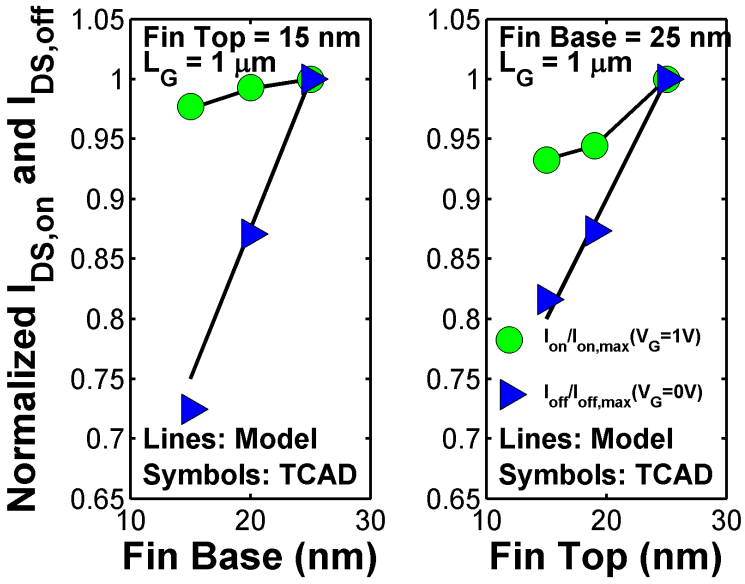

Figure 3.5. Normalized ($I_{DS}/I_{DS,MAX}$) on (circles) and off (triangles) drain currents.

core model in the figures. The accuracy of the proposed model is tested by the drain current and its derivatives agreement between the data and model. This is very important test because g_m and g_{DS} are crucial quantities in the ultimate performance of circuits constructed from these FinFETs.

3.2.2 Bulk Bias Effect

The fact that most of industry FinFETs are fabricated over bulk substrates [7, 63, 88] implies that additional effects must be taken into account by the core model. The channel fin is fully depleted till the punch-though implant, which is the p^+ implant under the channel for the NMOS FinFET shown in Fig. 6.1. The voltage applied at the body produces a small change in the depletion at the fin/punch-though region, which makes the threshold voltage dependent on body bias. This effect can be captured by adding an additional term, Δq_{dep}, in the core model:

$$v_G - v_o - \Delta q_{dep} - v_{ch} = -q_m + \ln(-q_m) + \ln\left(\frac{q_t^2}{e^{q_t} - q_t - 1}\right) \tag{3.24}$$

where Δq_{dep} is given by:

$$\Delta q_{dep} = -\frac{\gamma}{2v_T}\left(\sqrt{2\psi_b - V_{CH}} - \sqrt{2\psi_b}\right) \tag{3.25}$$

γ is the body effect parameter and ψ_b is defined as $\psi_b = v_T \ln(N_{ch}/n_i)$. Fig. 3.8 shows numerical simulation of a tri-gate FinFET for different body biases showing good agreement of the proposed model and TCAD simulations.

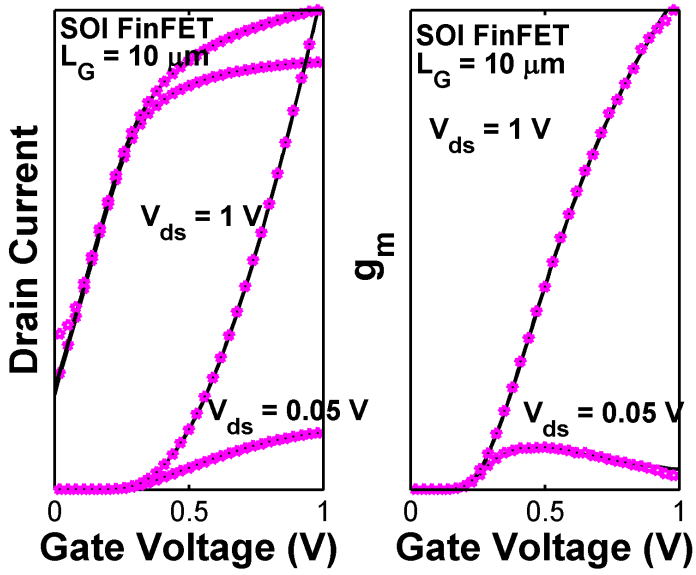

Figure 3.6. Drain current versus gate voltage (left figure) of a long channel SOI FinFET obtained from experimental data and from the proposed model only using the ideal unified long channel core model. Transconductance (right figure) also shows good agreement between model and experimental data. Symbols are the experimental data and lines the proposed model.

Another important effect to capture in bulk FinFETs is the presence of majority carriers in the channel fin for accumulation and depletion conditions, holes for NMOS FinFETs that are injected from bulk terminal. Applying Gauss law boundary condition at the insulator interface, it is possible to find the relation between bias and charges:

$$v_G - v_{FB} - \phi_s = -(q_a + q_d + q_m) \tag{3.26}$$

where is ϕ_s is the normalized surface potential (ψ_s/v_T), q_a is the normalized charge in the accumulation region and q_d is the normalized charge coming from the depletion region. q_m can be directly obtained from equation (3.24). In the accumulation and depletion regions, q_m can be neglected; therefore, an expression for $q_a + q_d$ for planar conventional MOSFETS [15], as a function of the surface potential, can be obtained using the Poisson equation solution neglecting mobile charges:

$$v_G - v_{FB} - \phi_s = -sgn(\phi_s)\frac{\gamma}{\sqrt{v_T}}\sqrt{e^{-\phi_s} + \phi_s - 1} - q_m \tag{3.27}$$

Equation (3.27) is obtained from planar conventional MOSFETS [15], but using a normalization variable suitable for FinFETs and the definition of γ from equation (3.25), equation (3.27) can be extended to bulk FinFETs. Using the proposed channel

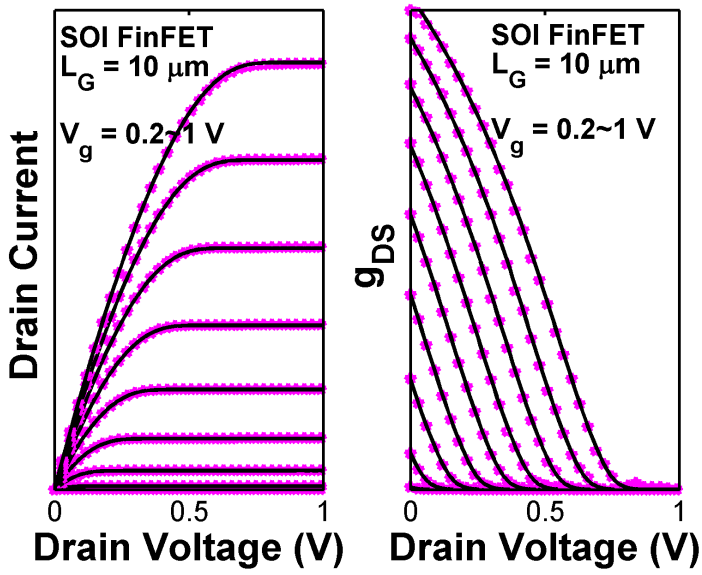

Figure 3.7. Drain current versus drain voltage (left figure) of a long channel SOI FinFET obtained from experimental data and from the proposed model only using the ideal unified long channel core model. Output conductance (right figure) also shows good agreement between model and experimental data. Symbols are the experimental data and lines the proposed model.

charge models, terminal charge models can be obtained using Ward-Dutton charge partition approach [64]. Figure 3.9 shows the gate capacitance of a fabricated FinFET versus gate voltage, the model can accurately capture strong inversion, depletion, and accumulation regions.

3.2.3 Quantum Effect on Capacitance/Charge

Equation (6.1) was obtained by solving the Poisson equation assuming Boltzmann's distribution for the mobile carrier and without taking care of quantum-mechanical (QM) confinement effects. While calculating charge, there are two significant QM effects that must be considered in FinFET devices. The first effect is a carrier structural confinement coming from the small area of the fin channel which mainly affects in the form of a threshold voltage shift (ΔV_{TH}) that can be treated with an additional bias-independent term, as already implemented in BSIM-CMG [73, 13]. The second effect is a carrier electrical confinement coming from the electric field at the insulator interface. Therefore, it is bias dependent and it must be added to the core model. Electrical confinement splits the energy levels at the fin-insulator

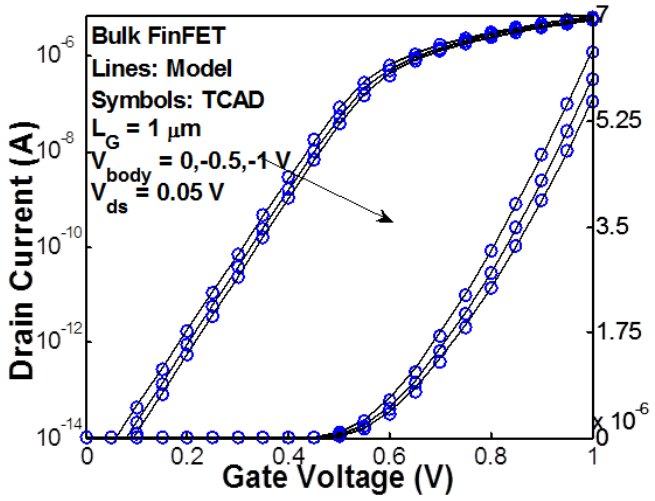

Figure 3.8. Drain current versus gate voltage of a Bulk Trapezoidal trig-gate FinFET with rounded corners for different body bias values. $TFIN, top = 20nm$, $TFIN, bottom = 50nm$, $HFIN = 25nm$, $10nm$ corner curvatures, $N_{ch} = 1x10^{15}cm^{-3}$, $EOT = 1nm$, and gate workfunction equal to 4.6 eV were used for the simulation and model. In order to highlight the body bias effect a short fin was used .

interface and it can be modeled via triangular well [82]:

$$E_n = \left(\sqrt{\frac{\hbar}{2m_c}} \frac{3}{2} \pi q E_s \left(n + \frac{3}{4} \right) \right)^{2/3} \tag{3.28}$$

$\hbar$ is the Planck constant, m_c is the carrier effect mass in the confinement direction, and E_s is the electrical field at the semiconductor-insulator interface. In the same manner as [78], the energy split can be treated as band-gap increase (ΔE_g) due to the splitting. Thus, n_i^{QM} is expressed as:

$$n_i^{QM} = n_i^{CL} e^{\frac{\Delta E_g}{2kT}} \tag{3.29}$$

ΔE_g can be approximated as the lowest sub-band E_n and the surface potential E_s can be expressed as a function of qm and q_{dep}; therefore, replacing n_i^{QM} into the core model, it results in the following formula:

$$\begin{aligned} v_G - v_o - \Delta q_{dep} - v_{ch} = -q_m + \ln\left(-q_m\right) \\ + \ln\left(\frac{q_t^2}{e^{q_t} - q_t - 1}\right) + \alpha_{QM} \left(q_m + q_{dep}\right)^{2/3} \end{aligned} \tag{3.30}$$

with α_{QM} given by:

$$\alpha_{QM} = \frac{1}{kT} \left(\frac{9\hbar\pi q}{8\sqrt{2m_c}} \frac{v_T C_{ins}}{W_{eff} \varepsilon_{ch}} \right)^{2/3} \tag{3.31}$$

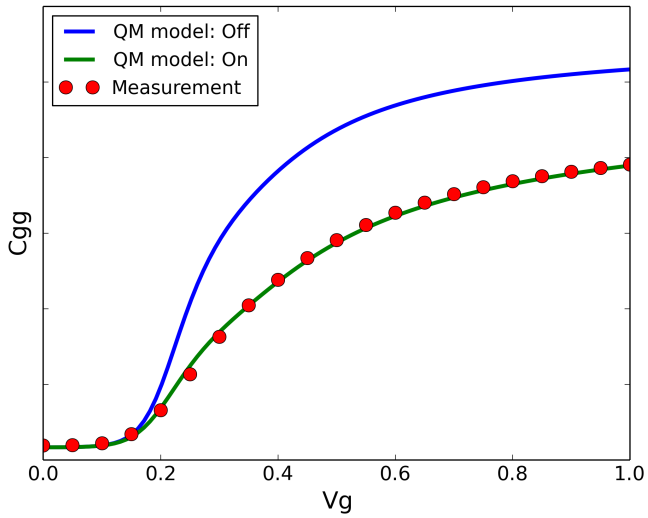

Figure 3.9. Gate capacitance (C_{gg}) versus gate voltage at $V_{ds} = 0V$ obtained from proposed model with and without quantum confinement effects (lines), and from measured data (symbols).

Table 3.1. Field penetration length λ

Device Geometry	λ
Double-Gate [83]	$\sqrt{\frac{\varepsilon_{ch}}{2\varepsilon_{ins}}\left(1+\frac{\varepsilon_{ins}}{4\varepsilon_{ch}}\frac{T_{fin}}{t_{ins}}\right)T_{fin}t_{ins}}$
Cylindrical-Gate/Nano-wire [8]	$\sqrt{\frac{8\varepsilon_{ch}R^2\ln\left(1+\frac{t_{ins}}{R}\right)+\varepsilon_{ins}4R^2}{16\varepsilon_{ins}}}$
Unified FinFET [27]	$\sqrt{\frac{\varepsilon_{ch}A_{ch}}{C_{ins}}\left(1+\frac{A_{ch}C_{ins}}{2\varepsilon_{ch}W_{eff}^2}\right)} \approx \sqrt{\frac{\varepsilon_{ch}A_{ch}}{C_{ins}}}$

Figure 3.9 shows the gate capacitance (C_{gg}) with and without quantum mechanical confinement effects versus measured data. The bias dependence of QM effects degrades capacitance and charge control in the fin channel. Model has been implemented in Verilog-A (see Appendix C).

In the case of III-V transistors, quantum effects are very important. Figure 3.10 shows BSIM-CM modeling InGaAs FinFETs [40, 35]:

3.3 Global Scaling Model

The previous section was devoted to obtain a core model for the long-channel bulk FinFET transistor. Using this framework, it is possible to extend it to short-channel devices by considering the electrical effect of source and drain terminal over the electrical potential of the device, i.e. considering all 3-dimensional effects. Sub-

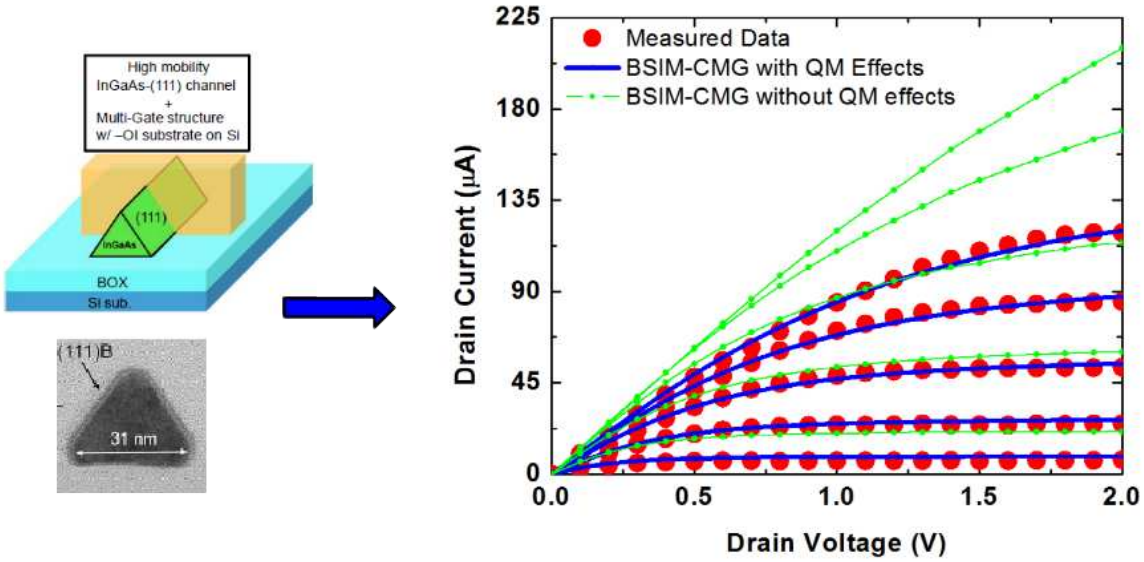

Figure 3.10. The unified model accurately models the triangular fin InGaAs FinFETs [40, 35]. With the quantum effects model turned off, the model over-predicts channel charge and hence current

threshold swing (SS) and threshold voltage (V_{TH}) are two electrical quantities that are important for circuit designs, which are extremely sensitive to the device's gate length and fin dimensions. The threshold voltage of long-channel devices is implicitly captured in the core model. A model for short channel is obtained using $\Delta V_{TH} = V_{TH,L} - V_{TH,L\to\infty}$, which is incorporated in the core model as a correction term. A model for ΔV_{TH} can be obtained by solving the 3-dimension Poisson equation in the subthreshold region and measuring the difference of the top of the potential barrier between a short and a long channel transistor. ΔV_{TH} has already been modeled for double-gate [83] and cylindrical-gate [8] FinFETs, resulting in models that depend on terminal voltages, gate length, and the parameter λ, so called field penetration length. λ captures the extent to which the electric field from the drain/source regions can penetrate into the channel, i.e., how it influences the source-to-channel potential barrier. For complex fin cross-sections, a compact expression for λ is difficult to obtain from the Poisson equation. Hence, results of [83, 8] are unified into a single λ [27], using the parameters for the unified model, as shown in Table 3.1. SS model also depends on terminal voltages, channel gate length, and λ. It is important to notice that a device with lower λ will exhibit better immunity to short-channel effects. Results of FinFET gate scaling are shown in Fig. 4.4 confirming excellent scaling capabilities of the BSIM-CMG model.

Finally, BSIM-CMG model, including the new models presented in this work, has been validated with experimental data from Intel 14 nm FinFET technology [63].

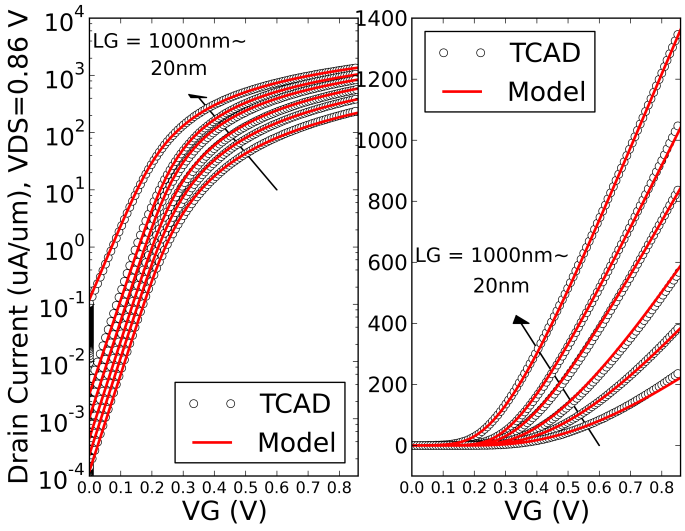

Figure 3.11. Drain current versus gate voltage of FinFETs devices with $L_g = 20, 50, 250, 500, 1000nm$. BSIM-CMG model accurately captures the FinFET short-channel characteristics.

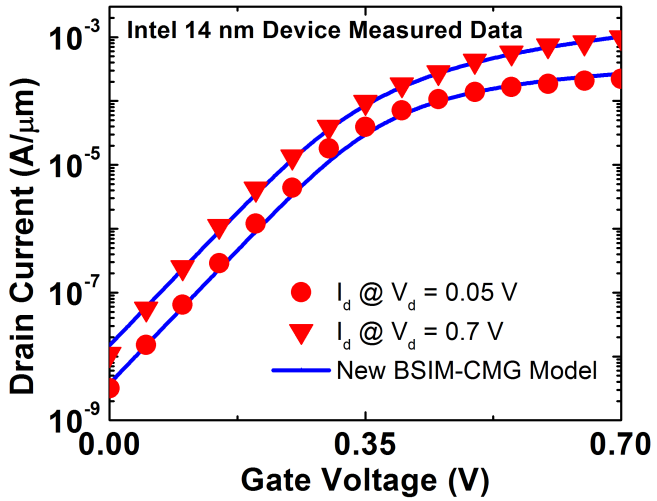

Figure 3.12. Intel 14 nm FinFET device modeled with new BSIM-CMG model. Experimental data from [63].

The results of the validations are shown in Fig. 3.12.

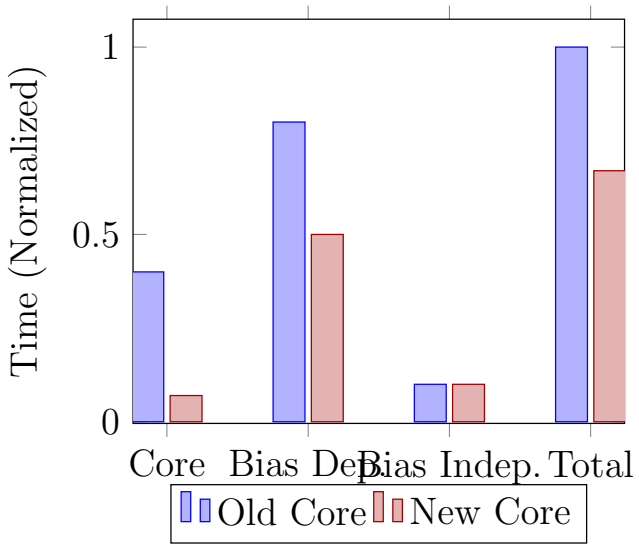

Figure 3.13. Calculation time of core model, bias dependent calculations, bias independent, and total BSIM-CMG Verilog-A code. Over ∼30% speed improvement is achieved with the new proposed model.

3.4 Speed Results

Implicit model is implemented using a physics based intial guess with two quartic iterations (see Appendix C and [1]). Figure 3.13 shows the results of BSIM-CMG implementation in Verilog-A language. ∼30% speed improvement is achieved with new model.

3.5 Benchmark Tests

Quality of a compact model is an important criteria in circuit simulations. An easy way to check the quality of a model is to check its asymptotic behavior in extreme conditions e.g. large bias and temperature range etc. A more comprehensive way is to test the model on benchmark tests which are now considered standard tests for any compact model [13]. These tests are especially important for a compact model which is to be used in RF and analog circuit designs. Fig. 3.14- 3.17 show the BSIM-CMG model results on different benchmark tests and it can be seen that BSIM-CMG passes all the tests. Model have been implemented in Verilog-A (see Appendix C and [1])

3.6 Conclusion

A new core model is introduced into the industry standard compact model, BSIM-CMG, enabling modeling of FinFETs with complex fin cross-sections. Bulk

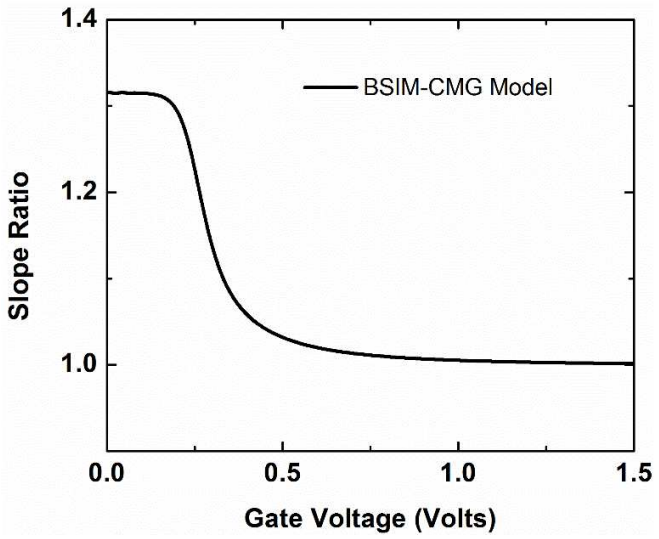

Figure 3.14. Slope ratio calculated using BSIM-CMG model at room temperature. $T_{fin} = 15$ nm, $L = 1$ μm and $N_{fin} = 10$. This test checks if a compact model takes care of the different drain-to-source voltage dependence of drain-to-source current in weak- and strong-inversion regions.

bias effect, presented in industry bulk FinFETs, affecting threshold voltage modulation, has been incorporated into the new core model. Bias dependent quantum mechanical confinement effects, capturing the degradation of gate capacitance, has been directly incorporated to the new model as well. A new field penetration length definition, for advanced FinFETs, has been presented and it permits BSIM-CMG to accurately calculate drain current for short channel FinFETs. The new modeling features presented in this work haven been already incorporated into the production ready compact model that will be soon publicly release as BSIM-CMG version 109.0.0 targeting 14nm node technology.

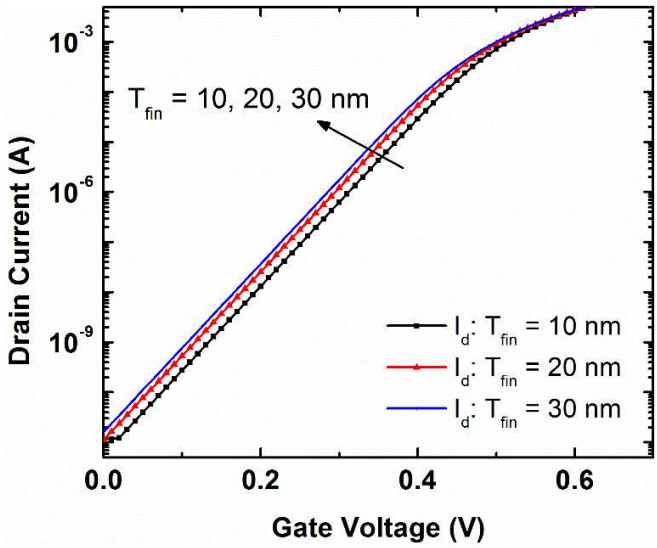

Figure 3.15. Sub-threshold current simulated from BSIM-CMG model. Current increases with increase in fin thickness due to volume inversion effect. In the sub-threshold region of thin-body transistors, the gate bias moves the energy bands not just at the surface but across the full body-thickness of the device. This causes inversion to occur in the full body thickness of the device as opposed to only the surface in case of bulk MOSFETs. This phenomenon is called volume inversion. It occurs only in the sub-threshold region as in strong inversion the carriers at the surface screens the electric field from reaching deep inside the silicon body.

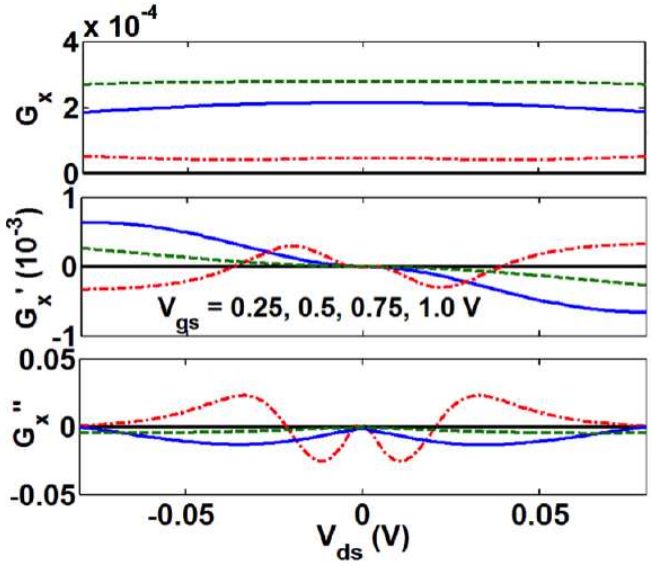

Figure 3.16. Results of Gummel symmetry test from BSIM-CMG model. The model shows smooth and continuous derivatives of drain-current and passes symmetry test. Gummel symmetry test is a standard way of testing the symmetry of drain-current model.

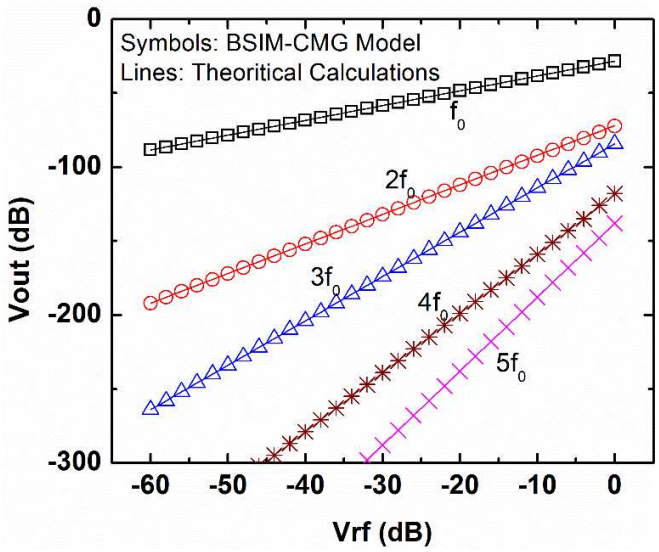

Figure 3.17. Harmonic balance simulation results showing fundamental (f_0) , second ($2f_0$), third ($3f_0$), fourth ($4f0$) and fifth-harmonic ($5f_0$) from BSIM-CMG model, which match very well with theoretical calculations. $f_0 = 1$ MHz and $V_g = 1$ V. If a compact model has singularities in drain-current derivatives, it will produce unphysical harmonic balance simulations results. Theoretically second harmonic is proportional to square of the input signal, third harmonic is proportional to cube of the input signal and so on .

Chapter 4

Variability Modeling

4.1 Introduction

The increasing process variations that have accompanied process technology scaling must now be explicitly considered in IC design. In this chapter, a methodology for predictive modeling of FinFET variability using the newest version of BSIM-CMG standard compact model is presented. This work emphasizes the extraction of a single parameter set of the compact model for FinFETs (figure 6.1), which together with the models three physical fin shape parameters enables circuit variability simulation.

Previous sections shown very good results where the proposed model can accurately model transistors of different geometrical shapes, gate lengths, and channel materials. However, capturing device variability is an even more challenging, yet necessary, problem. In FinFETs, we can have different source of device variability, see figure 4.3. Fin shape determines area and total effective with of the device, which affect every aspect of the electrical parameters. The fin shape is determine by the fabrication process to create the fin and can include several steps as etching and material depositions. Source and drain technology in FinFETs is different than conventional planar CMOS, indeed, epi deposition, and S/D geometries are crucial on device performance. Another example about variability source are the doping concentration and profile at s/d region. Finally, gate technology include additional source of variability that mainly affect threshold voltage. From these examples, it is possible to notice that the source of variability in FinFETs are coming mainly from device geometries variations. Therefore the objective of this chapter is to capture these variations using the proposed model by adding variability source directly into the model using the unified model parameters. The entire variability process can be summarized in figure 4.1. It contains the following steps:

1. **Nominal global extraction**: Extraction of a single parameter set for nominal devices under different gate lengths. Proposed model, using a single parameter set, can describe FinFET behaivor from long to short channel devices. TCAD

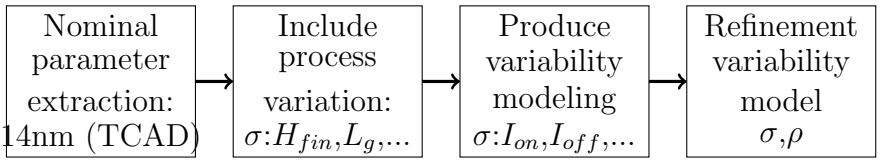

Figure 4.1. Variability Modeling

simulation have been used in this step; however, experimental data can be used as well.

2. **Include process variation**: Obtain device geometry variations from manufacturer's estimation including variation parameters of fin dimensions, channel length, doping, work function, etc.

3. **Produce variability modeling** Proposed compact can take geometry variations as input parameters and generate electrical parameter variation distributions, such as I_{on}, I_{off}, V_{th}, SS, etc. It is very important to point out that complex correlation are well estimated by the proposed model, such SS and V_{th} correlation which is highly dependent in subtle variation of fin geometry and channel length.

4. **Refinement of variability model**: In the case that more accurate results are needed, it is possible to refine the global parameter extraction including not just nominal device but extreme devices. For example, a single parameter set can be re-extracted including nominal and devices with highest and lowest I_{off}. A device with lowest I_{off} is normally a results of a larger gate length, thinner EOT, and smaller fin area. On the other hand, larger I_{off} are normally obtained for FinFETs with larger area, shorter gate length, and thicker EOT.

4.2 Description of the Unified Model

The new Unified FinFET Model [27, 23] has three physical fin shape parameters (Table 4.1): A_{ch}, the cross-sectional area of the fin; W_{eff}, the effective electrical width of the fin; and C_{ins}, the total gate insulator capacitance. The new model, with these three parameters, can describe the electrical behavior of realistic FinFETs with complex fin cross sections such as those reported in [7, 63] (Fig. 6.1). Short channel effects (SCEs), such as drain induced barrier lowering (DIBL) and subthreshold swing (SS) degradation, are accurately modeled with a new field penetration length [27] described by λ, which is determined by the same three fin shape parameters:

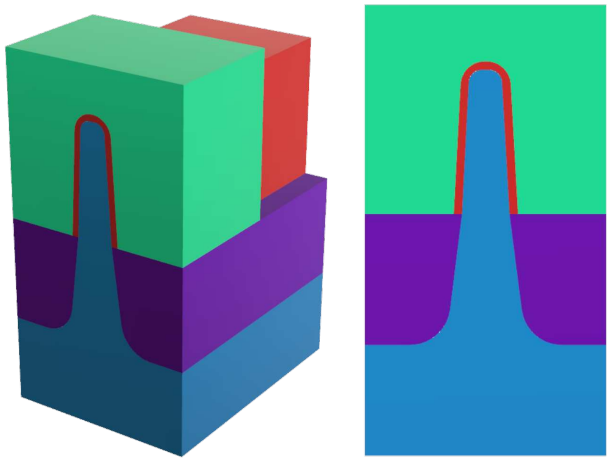

Figure 4.2. A 3-dimensional schematic of a Bulk FinFET together with its complex Fin cross-section. The fin shape has been set to be similar to industry FinFETs reported in [7, 63].

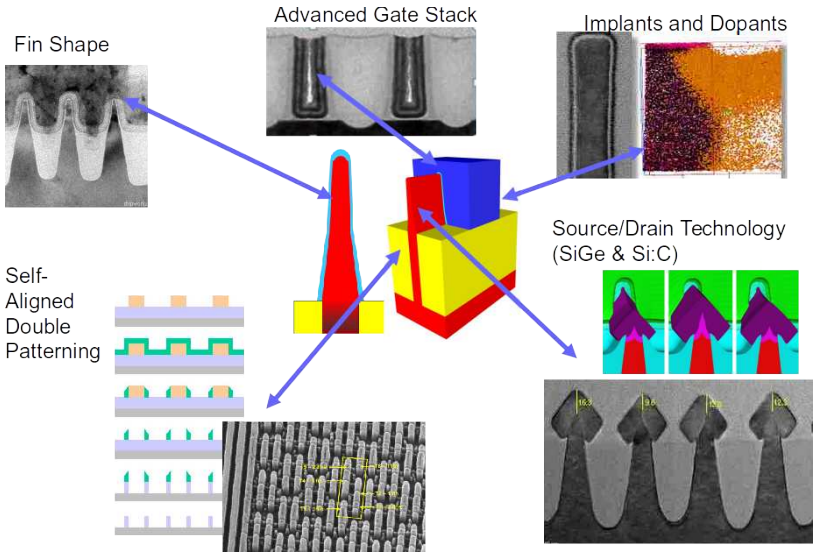

Figure 4.3. Different source of device variability.

$$\lambda = \sqrt{\epsilon_{ch} \frac{A_{ch}}{C_{ins}} \left(1 + \frac{A_{ch} C_{ins}}{2\epsilon_{ch} W_{eff}^2}\right)} \tag{4.1}$$

Table 4.1. Structural parameters of FinFET under study, similar to the device in [63]. The three Unified Model fin shape parameters (*) are also shown.

Parameter	Value
L_G	$20nm$
$HFIN$	$42nm$
$TFIN, TOP$	$7nm$
$TFIN, BL$	$7nm$
$TFIN, BR$	$7nm$
EOT	$0.8nm$
$NBODY^*$	$1 \times 10^{15} cm^{-3}$
C^*_{ins}	$3.87nF/m$
A^*_{ch}	$4.78 \times 10^{-16} m^2$
W^*_{eff}	$92nm$

4.3 Device Simulation and Model Parameter Set Up

Figure 6.1 shows the schematic of a 14nm FinFET used for this study. Fin dimensions, in Table 4.1, were chosen to approximate those reported in [63]. Device parameters not available in [63] were taken from ITRS [6] where TCAD [31] is used to obtain the electrical characteristics of the FinFET HP 14nm node targets. A single set of BSIM-CMG model parameters is extracted to accurately capture the TCAD generated nominal I-V characteristics from long-channel to short-channel devices (Fig. 4.4). Using this nominal model and three fin shape parameters corresponding to the extreme (nominal $\pm 10\%$) of each parameter in Table 4.1, 6561 IV curves, for different V_g and V_d biases, can be generated with the model. The model generated highest and lowest I_{off} curves as shown in Fig. 4.5. They agree very well with the highest and lowest I_{off} curves among the 6561 TCAD generated IV curves, which process took several days. Figures 4.6, 4.7, and 4.8 show that the model generated scatter plots match the TCAD generated scatter plots very well in extreme values, correlations and shapes. It is very important to note that the Unified Model generates the variations simply by varying the three shape parameters and dopant concentration, not by the conventional tedious fitting of model to statistical TCAD or silicon data.

4.4 10nm vs. 14nm Variability Using Predictive Modeling

To demonstrate the ease of this model based variability modeling methodology, we include metal gate work-function, source resistance and drain resistance as addi-

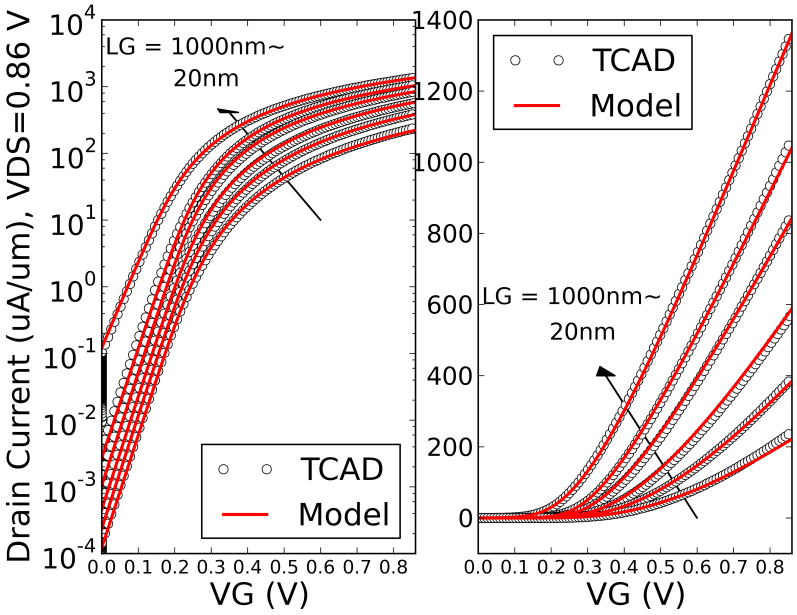

Figure 4.4. IDS-VG of FinFETs with L_G= 20, 50, 250, 500, 1000nm. BSIM-CMG model accurately captures the FinFET characteristics.

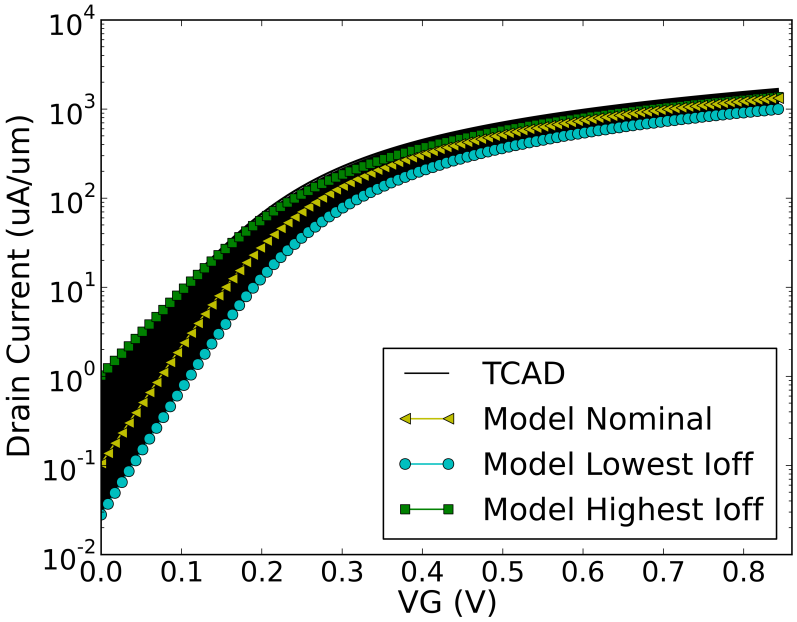

Figure 4.5. IDS-VG generated by TCAD varying each parameter in Table 4.1 from -10% to +10%. Model generated nominal, lowest and highest I_{off} curves are also shown.

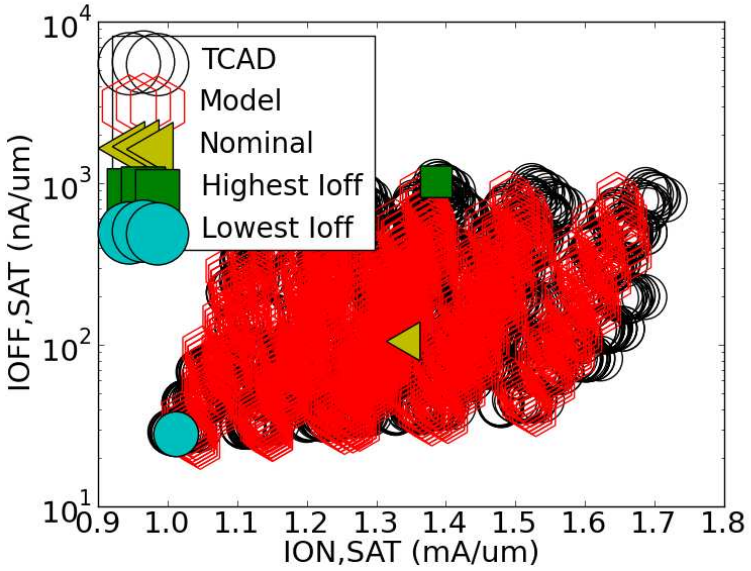

Figure 4.6. Scatter plot of I_{on} vs. I_{off} obtained by TCAD and by BSIM-CMG model. The model shows excellent agreement in correlations, extreme values, and shapes of scatter plot. Correlations are $\rho_{TCAD} = 0.36$, $\rho_{Model} = 0.35$.

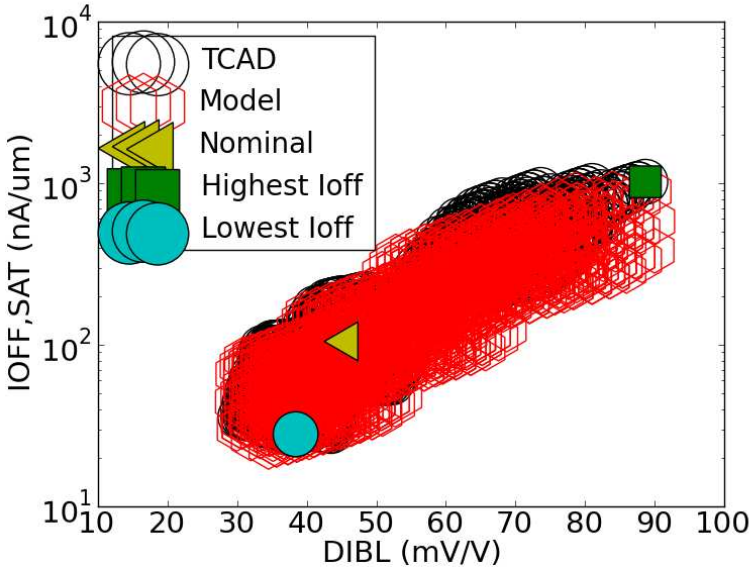

Figure 4.7. Scatter plot of I_{off} vs. DIBL obtained by TCAD and by BSIM-CMG model. The model shows excellent agreement in correlations, extreme values, and shapes of scatter plot. Correlations are $\rho_{TCAD} = 0.91$, $\rho_{Model} = 0.85$.

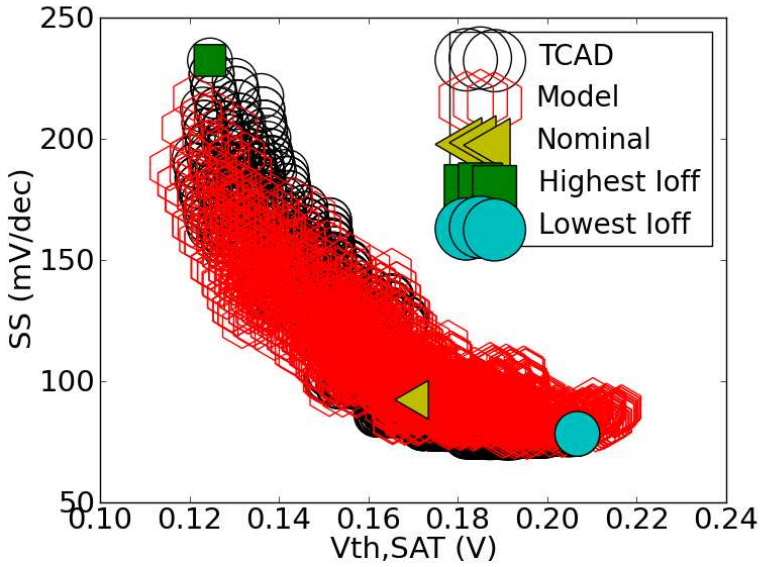

Figure 4.8. Scatter plot of SS vs. $V_{TH,SAT}$ obtained by TCAD and by BSIM-CMG model. The model shows excellent agreement in correlations, extreme values, and shapes of scatter plot. Correlations are $\rho_{TCAD} = -0.89$, $\rho_{Model} = -0.85$.

tional sources of variability. Each model parameter in Table 4.1 is generated with a σ equal 5% of its nominal value. In the case of 10nm node, we assume that TFIN and EOT are scaled down, as shown by figure ref14vs10, but the carrier mobility and S/D resistance remain the same as 14nm. Figs. 4.10-4.12 show that the 10nm node would have similar variability as the 14nm node if parameter variations remain the same for both technologies. I_{on} increases due EOT and L_G scaling. The inclusion of gate work-function variation significantly increases the I_{on}-I_{off} correlation over that in Fig. 4.6 because both are simple functions of threshold voltage, and it significantly reduced the I_{off}-DIBL correlation, as shown by figure 4.11, because I_{off} is sensitive to threshold voltage while DIBL is insensitive to it.

4.5 14nm Node SRAM Variability Evaluation

The effects of process variations are most profound on SRAM due to their tight margins of operation. SRAM schematic is shown by figure 4.13, their margins are a good example for the use of the proposed variability modeling methodology. Figure 4.14 shows 40000 butterfly curves generated with variability sources described in figure 4.14 in approximately 4500 CPU seconds. The static noise margin distribution can be easily extracted from figure 4.14, and results are presented by figure 4.15. A physics based compact model that speedily and accurately describes transistor variability is

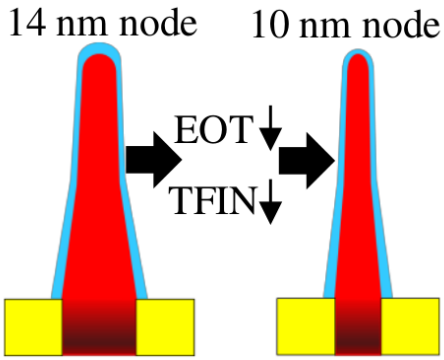

Figure 4.9. 14nm FinFET from Fig. 1 and assumed 10nm node FinFETs (EOT = 0.7nm, TFIN = 5nm). Assume same carrier mobility and S/D resistance

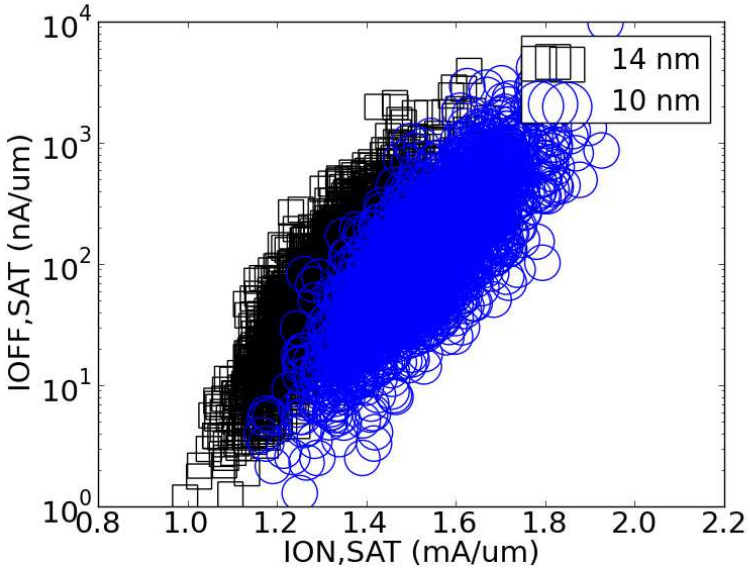

Figure 4.10. 14nm and 10nm nodes scatter plot I_{on} vs. I_{off} generated by Monte Carlo simulations using predictive new model. Correlations are $\rho_{14nm} = 0.84$, $\rho_{10nm} = 0.81$.

a key element on SNM distribution generation, since the large number of SRAM cells in a chip implies that some cells will exhibit behavior well out of the tail of the metric distribution , i.e., as far as 7σ.

4.6 Conclusion

New physics model can efficiently and accurately model complex and subtle FinFET variations using only physical shape parameters. It can predictively model

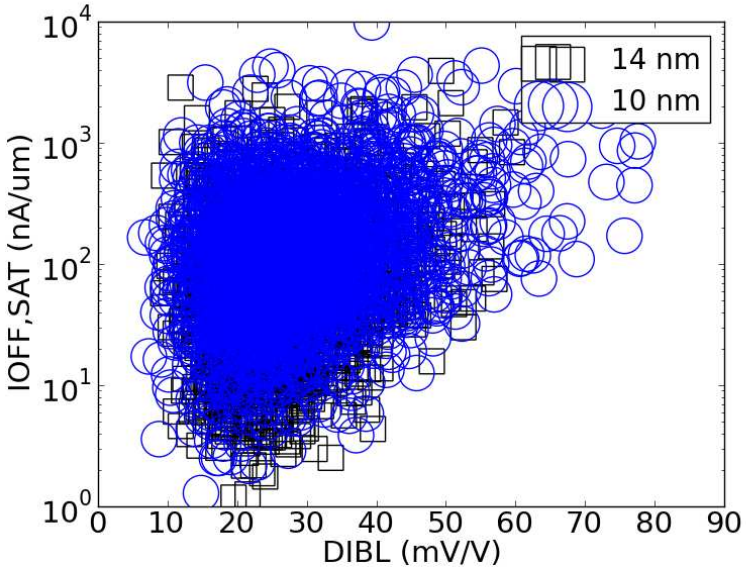

Figure 4.11. 14nm and 10nm nodes scatter plot I_{off} vs. DIBL generated by Monte Carlo simulations using predictive new model. Correlations are $\rho_{14nm} = 0.21$, $\rho_{10nm} = 0.27$.

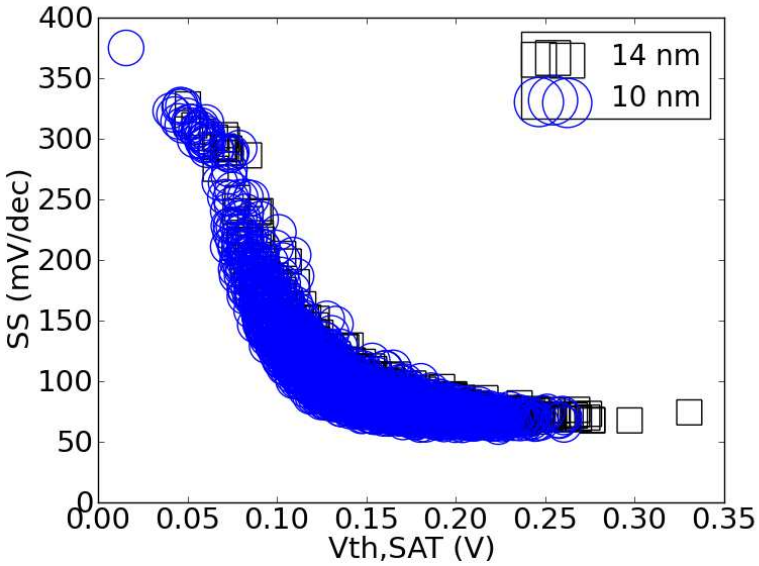

Figure 4.12. 14nm and 10nm nodes scatter plot SS vs. $V_{TH,SAT}$ generated by Monte Carlo simulations using predictive new model. Correlations are $\rho_{14nm} = -0.75$, $\rho_{10nm} = -0.79$.

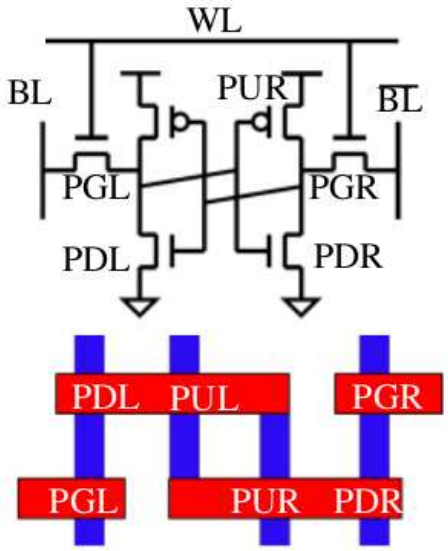

Figure 4.13. (a) Schematic of 6T SRAM bit cell. (b) layout with 1-1-1 fin.

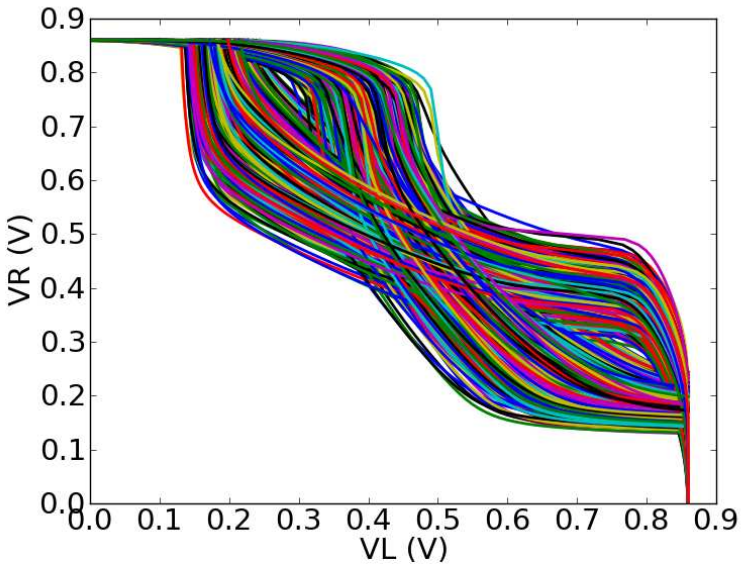

Figure 4.14. 40000 butterfly curves used to extract static noise margin for the 6T SRAM bit cell. They are generated by the new model in $\tilde{4}500$ CPU seconds for the 14nm node FinFET with variability described in Fig. 6.

future FinFET technology variability using assumed device shape variation. It also enables speedy statistical circuit simulation using predictive variability model or a model confirmed with TCAD or silicon data.

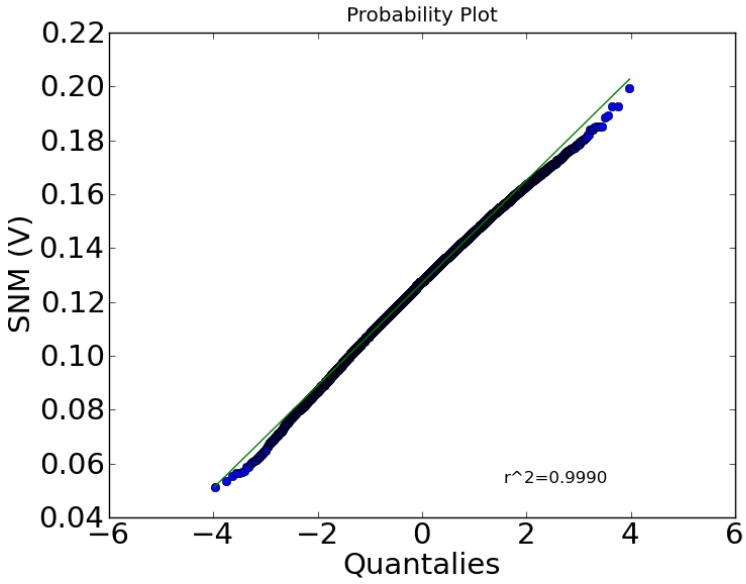

Figure 4.15. Static noise margin distribution.

Chapter 5

Model for Independent Gate MOSFETs

5.1 Introduction

Independent multi-gate MOSFETs (front- and back-gate) are enabling new novel applications wherein the back-gate can be in depletion or inversion. Indeed, ultrathin Body silicon-on-insulator (UTBSOI) technology has been developed with excellent low power, scaling and, variability characteristics [18]. UTBSOI has been recently adopted in sub-20nm IC technologies [55, 65, 59] as an alternative to FinFET technology [7, 88, 47], as both technologies are replacements of the conventional bulk planar technology. For UTBSOI transistor technology, the Compact Model Coalition (CMC) has chosen BSIM-IMG [52, 37, 43, 14] as one of the first industry-standard compact model for advanced circuit design.

The compact model for independent multi-gate MOSFETs (figure 5.1) is obtained from the Poisson's solution with front- and back-gate boundaries conditions [52, 21, 67, 74]. Once front- and back-surface potentials are obtained, they can be utilized to obtain the mobile charge in the channel that eventually leads to the computation of the drain current of the device. It is well known that the Poisson's solution for these devices lies in trigonometric and hyperbolic domains, making the desired numerical robustness extremely difficult; however, fast speed, numerical robustness, and accuracy are fundamental characteristics of compact models for circuit design and technology development. An industry compact model must be able to calculate terminal (drain, source, front/back-gate) currents and charges, which are then utilized by circuit simulator engines to solve a complete circuit under various analyses such as DC, AC, transient, etc. This work presents a new analytical model for the core model of BSIM-IMG compact model for UTBSOI technologies. It is based in

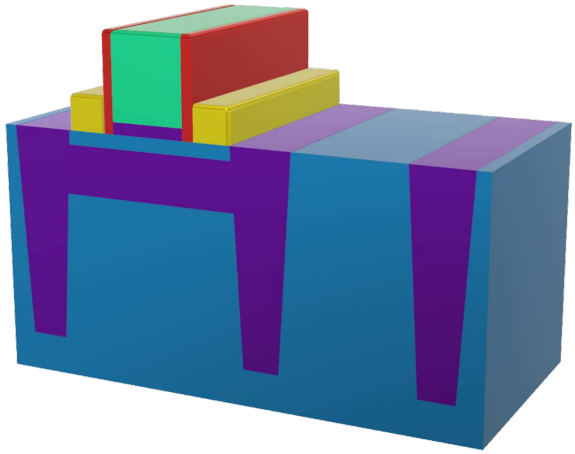

Figure 5.1. 3-dimensional schematic of a ultra-thin-body silicon-on-insulator device.

an accurate initial guess, followed by three first order Newton-Raphson's iteration updates.

5.2 Independent Multi-Gate MOSFETs

Figure 5.1 shows a 3-dimensional schematic of UTBSOI, similar to that demonstrated in [18]. It has a traditional planar structure similar to conventional bulk MOSFETs, with source, drain, and gate contacts in the top; however, the silicon channel layer is thin (Fin), and placed between front/back insulators, where the additional back gate serves as a potential modulator of the silicon fin. This additional tuning feature can be use in several contexts, for example, as a threshold voltage modulation or device variability control [18, 33].

Figures 5.2 and 5.3 show structural and energy band cross-sectional view of a UTBSOI, respectively, where it is easy to appreciate front and back gates, silicon insulator layer (or Fin), and back and front insulators (EOT_f and EOT_b).

Figure 5.3 represent the ideal structure taken as a reference for the derivation of the core model, this model must be able to capture potential in the front and back silicon-insulator interfaces; thus, making possible the calculation of back/front charges and mobile charge in the channel. In a different manner compared to conventional FinFETs, front- and back-gate potentials can produce different set of bias conditions as shown in figures 5.4 to 5.7. Figure 5.4, shows the first case, where channel is in the substhreshold condition and it is fully depleted, this is accomplished when back and front channels are turned off due the low potential at both gates. The second bias case is when the front potential is large enough for inversion but the back-gate is not, figure 5.5 shows that there is inversion in the front gate, but back gate is still off and in the subthreshold condition. The third case, figure 5.6, show the case

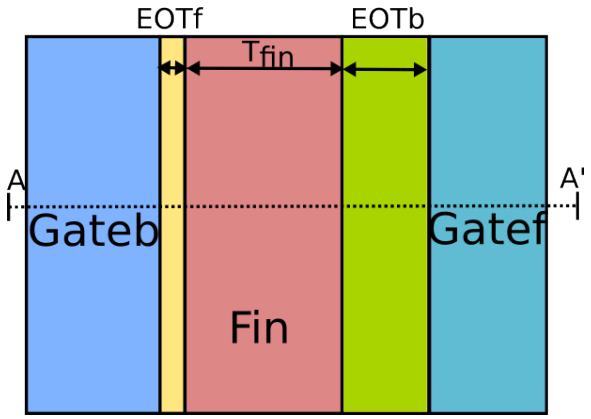

Figure 5.2. 1-dimensional cross-sectional view of a UTBSOI with independent potential control of the channel from front and back gates.

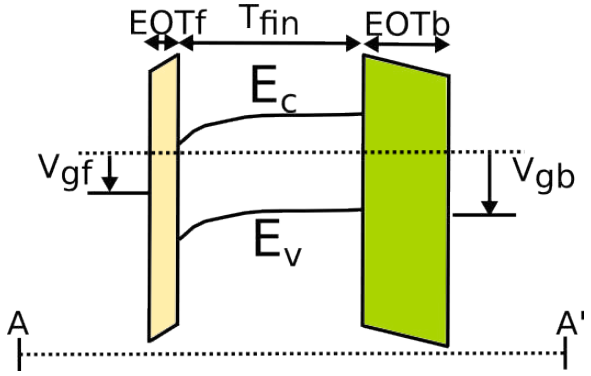

Figure 5.3. 1-dimensional cross-sectional view of the energy diagram of a UTBSOI. Two different boundary conditions defines the energy shape in the semiconductor channel.

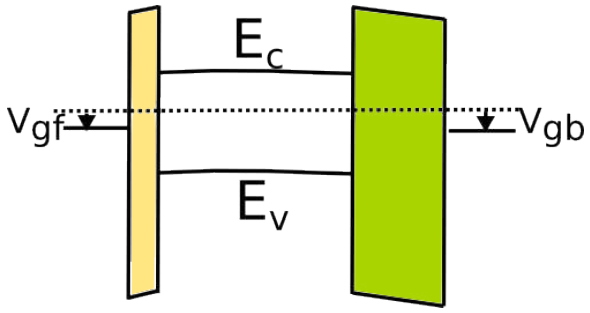

Figure 5.4. 1-dimensional cross-sectional view of a UTBSOI where channel is in the substhreshold condition.

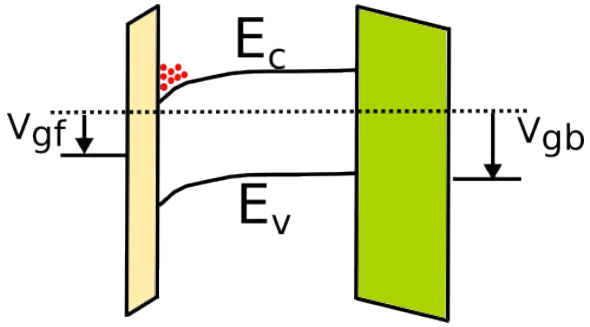

Figure 5.5. 1-dimensional cross-sectional view of a UTBSOI where only front surface is in strong inversion condition.

where front potential is not large enough to produce front charge inversion but back gate can induce inversion in the back channel. Finally, figure 5.7 shows the last case where both, front and back, channels are in inversion condition due the large potential at both gates. All four configurations must be captured in an accurate and robust manner by a core compact model so it can be used for circuit simulation and design. In the following sections, the core compact model used in BSIM-IMG is described in detailed.

5.3 Core Model

There is an extensive work in literature showing different development of core compact models for UTBSOI devices. The work presented in [52] represent a robust solution that simplifies the Poisson's equation, with a single variable equation that can be solved for devices where front inversion is the dominant component for the current. In [21], a compact model with three different solution regions was presented, it take into account hyperbolic and trigonometric domains, having a difficult numerical challenge related to the mathematical implementation of the model to keep

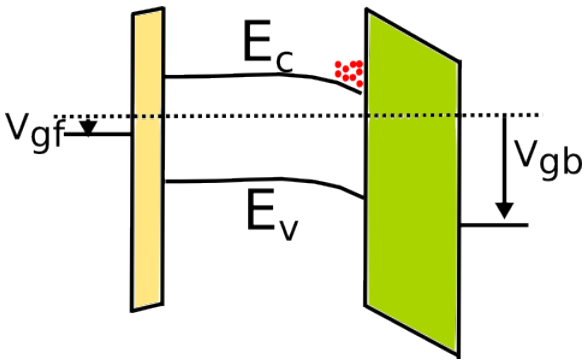

Figure 5.6. 1-dimensional cross-sectional view of a UTBSOI where only back surface is in strong inversion condition.

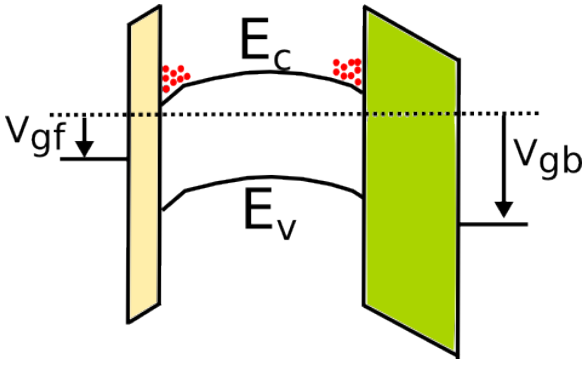

Figure 5.7. 1-dimensional cross-sectional view of a UTBSOI where back and front surfaces are in strong inversion condition.

accuracy and track of the analytic solution. The work presented in [67] proposed a set of three equations that can be solved simultaneously to obtain the solution for back and front potentials. Based on the work of [67], [74] removed the extra unknown of [67], leading to a single variable compact model which can be used to obtain the potentials in UTBSOI devices. In [75], authors present an analytical form for the implicit model presented in [74]. It consists of four steps: a initial guess, a first order correction step, two intermediate correction steps, and finally, two second order corrections. This work proposes a new analytical solution for [74], including a new initial guess followed by three first order correction steps, reducing the overall computation complexity of previous models while keeping good computation speed.

The 1-dimensional Poisson's equation (neglecting channel doping) for the cross-sectional section of a UTBSOI device (figure 5.3) can be written in the following form:

$$\frac{\partial^2\phi}{\partial x^2} = -\frac{\rho(\phi)}{\varepsilon_{\mathrm{ch}}} = \frac{qn_i}{\varepsilon_{\mathrm{ch}}} e^{\frac{\phi - V_{ch}}{v_T}} \tag{5.1}$$

where ϕ is the electrostatic potential in the fin, q is the magnitude of the electronic charge, n_i is the intrinsic carrier concentration, $\varepsilon_{\mathrm{ch}}$ is the dielectric constant of the channel (fin), v_T is the thermal voltage given by k_BT/q, where k_B and T are the Boltzmann constant and the temperature, respectively; V_{ch} is the quasi-Fermi potential of the channel ($V_{ch}(0) = V_{\mathrm{s}}$ and $V_{ch}(\mathrm{L}) = V_d$). The next step is to apply boundary conditions at each semiconductor-insulator interfaces. This is done using Gauss's law boundary condition which gives two boundary conditions:

$$\varepsilon_{EOTf}\frac{V_{gf} - V_{fbf} - \phi_{sf}}{EOTf} = -\varepsilon_{ch}\frac{\partial\phi_{sf}}{\partial x} \tag{5.2}$$

$$\varepsilon_{EOTb}\frac{V_{gb} - V_{fbb} - \phi_{sb}}{EOTb} = \varepsilon_{ch}\frac{\partial\phi_{sb}}{\partial x} \tag{5.3}$$

Note that the total charge in the channel can be expressed by the following formula:

$$Q_m = -\varepsilon_{ch}\frac{\partial\phi_{sf}}{\partial x} + \varepsilon_{ch}\frac{\partial\phi_{sb}}{\partial x} \tag{5.4}$$

Integrating once the 1-dimensional Poisson's equation with respect to potential and after variable normalization as in [74], it is possible to obtain the following two expressions:

$$\alpha^2 = k_f^2(x_f - \phi_f)^2 - A_0e^{\phi_f} \tag{5.5}$$

$$\alpha^2 = k_b^2(x_b - \phi_b)^2 - A_0e^{\phi_b} \tag{5.6}$$

where model variables are defined in Table 5.1. Integrating the electric field using α and then, using algebraic manipulations [74], it is possible to obtain the following equation:

$$\begin{aligned}\alpha\coth(\alpha/2)(k_f(x_f - \phi_f) + k_b(x_b - \phi_b)) + \\ k_fk_b(x_b - \phi_b)(x_f - \phi_f) + \alpha^2 = 0\end{aligned} \tag{5.7}$$

Table 5.1. Model Variables

Variable	Definition
x_f, x_b, v_T	$\frac{V_{GF}-\Delta\Phi_f}{v_T}, \frac{V_{GB}-\Delta\Phi_b}{v_T}, \frac{kT}{q}$ (Thermal Voltage)
ϕ_f, ϕ_b	$\frac{\varphi_f}{v_T}$, $\frac{\varphi_b}{v_T}$
$C_{ox,f}$, $C_{ox,b}$, C_{ch}	$\frac{\varepsilon_{ox,f}}{EOT_f}$, $\frac{\varepsilon_{ox,b}}{EOT_b}$, $\frac{\varepsilon_{ch}}{T_{ch}}$
k_f, k_b, $k_{eq,f}$, $k_{eq,b}$	$\frac{C_{ox,f}}{C_{ch}}$, $\frac{C_{ox,b}}{C_{ch}}, \frac{k_b}{k_f k_b+k_f+kb}$, $\frac{k_f}{k_f k_b+k_f+kb}$
A_0	$\frac{2qn_i\varepsilon_{ch}}{C_{ch}v_T}$
q_m	$\frac{Q_m}{v_T C_{ch}}$

The previous three equations form a system of three variables and three equations which can be solved to obtain back and front potentials. Note that if $\alpha^2 < 0$: $\coth, \sinh \rightarrow \cot, \sin$. However, these equations can be combined into a single variable equations as follows [74]:

$$f(\phi_f) = (k_f(x_f - \phi_f) + \alpha \coth(\alpha/2))(k_f(x_f - \phi_f) + k_b(x_b - \phi_b)) - A_0 e^{\phi_f} = 0 \tag{5.8}$$

with:

$$\phi_b = \phi_f - \ln(k_f(x_f - \phi_f) + \alpha \coth(\alpha/2)) + \ln\left(\frac{\alpha}{\sinh(\alpha/2)}\right)^2 \tag{5.9}$$

Equation (5.8) represent a single variable implicit equation that must be solved for the condition $f(\phi_f) = 0$; thus, for different values of ϕ_f, f must be minimized. The challenge relies in the hyperbolic and trigonometric nature of f for different values of ϕ_f. For example, figure 5.8 shows the evaluation of $f(\phi_f)$ for different values of ϕ_f. Note that for the hyperbolic region there is a single minimum value (single solution); however, in the trigonometric region, there are several values of ϕ_f where $f(\phi_f) \sim 0$, all of these conditions are few mV away from each other making the solution of (5.8) very sensitive to the initial iteration point. Indeed, the minimum value of α^2 must be bounded by $-4\pi^2$ [75]. This implies a challenging issue, because traditional iterative methods used in compact models, such as Newton-Raphson's method, may bring the solution to a false state producing discontinuities in the final compact model.

5.4 Initial Guess

The first step to obtain an analytical solution for (5.8) is to obtain an initial guess equation for the back and front potential in the subthreshold region. This can be done by neglecting inversion in the channel, and assuming a linear channel potential [52]:

$$\phi_{f,sub} = x_f + k_{eq,f}(x_f - x_b) \tag{5.10}$$

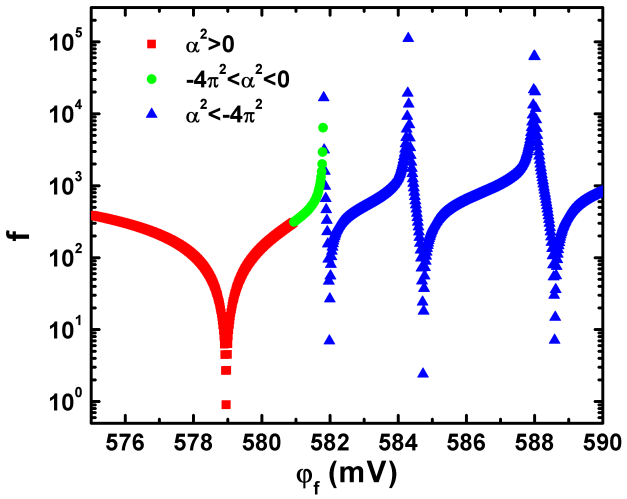

Figure 5.8. Evaluation of $f(\phi_f)$ for different values of ϕ_f. True versus false solutions are apart by few mV proving that the initial guess is extremely important to obtain good model convergence. $V_{GF} = 1$V, $V_{GB} = -0.5$V, $EOT_f = 2.4$nm, $EOT_b = 12$nm, $T_{ch} = 12$nm, $\Delta\Phi_f = -82$mV, and $\Delta\Phi_b = -82$mV.

$$\phi_{b,sub} = x_b + k_{eq,b}(x_b - x_f) \tag{5.11}$$

Figure 5.9 shows a comparison of the approximation (5.10) in the subthreshold region for the front potential. The next step is to obtain a close approximation for the potential in the strong inversion condition ($\phi_{f,sat}$). This is obtained in two steps, first a rough approximation is calculated ($\phi_{f,sat0}$) and then an update to this value is obtained. $\phi_{f,sat0}$ can be obtained by solving (5.5) for the lower limit value of α^2, which is bounded to $-4\pi^2$:

$$-4\pi^2 = k_f^2(x_f - \phi_{f,sat0})^2 - A_0 e^{\phi_{f,sat0}} \tag{5.12}$$

An accurate solution for $\phi_{f,sat0}$ requires numerical iteration; therefore, an approximation is used to obtain an estimation to its value:

$$\phi_{f,sat0} \simeq \ln\left((k_f^2(x_f - \phi_0)^2 + 4\pi^2)/A_0\right) \tag{5.13}$$

where ϕ_0 is given by:

$$\phi_0 = \ln\left(4\pi^2/A_0\right) \tag{5.14}$$

Note that ϕ_0 is the minimum value of $\phi_{f,sat0}$. Figure 5.10 shows that the value of $\phi_{f,sat0}$ is very close to the front saturation potential; however, as shown in figure 5.8, even mV of difference between initial guess to final solution may produce wrong solutions. $\phi_{f,sat0}$ is obtained assuming $\alpha^2 = -4\pi^2$; therefore, the next step is to obtain

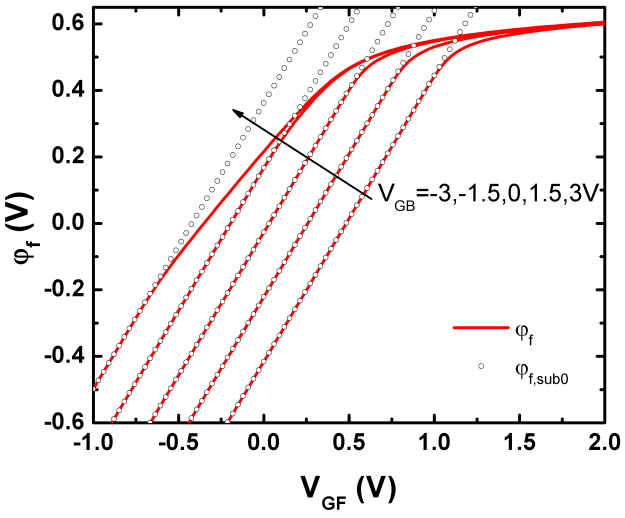

Figure 5.9. Front surface potential approximation in the subthreshold bias condition versus front surface potential solution. $EOT_f = 2.4$nm, $EOT_b = 12$nm, $T_{ch} = 12$nm, $\Delta\Phi_f = -39$mV, and $\Delta\Phi_b = 0.45$V.

a more accurate value for α^2 at saturation condition which is then used to calculate an updated value for $\phi_{f,sat}$.

It can be noticed that ϕ_0 closely corresponds to the potential value at the on set of strong inversion. Once front potential reach saturation, back potential also tends to saturate for larger front gate voltages. Then, using the same assumptions as those used to obtain equation (5.11), but now utilizing ϕ_0 value at the front gate-insulator interface, it is possible to obtain an approximation for the back surface potential when front surface potential is saturated:

$$\phi_{b,sat} = (\phi_0 + k_b x_b)/(1 + k_b) \tag{5.15}$$

Using these results, an initial guess for ϕ_b can be calculated as:

$$\phi_{b,guess} = \min(\phi_{b,sub}, \phi_{b,sat}, \phi_0) \tag{5.16}$$

Figure 5.11 shows the initial guess for the back potential versus the final solution, where saturation potential is correctly estimated. $\phi_{b,sat}$ and equation (5.6) can be used to estimate the value of α^2_{sat} for cases where $\alpha^2 > 0$:

$$\alpha^2_{sat^+} = k_b^2(x_b - \phi_{b,sat})^2 - A_0 e^{\phi_{b,sat}} \tag{5.17}$$

Equation (5.11) is a good approximation for cases where $\alpha^2 > 0$ because in those cases $e^{\phi_{b,sat}}$ is small and the value of α^2 is mainly determined by the first term in (5.11).

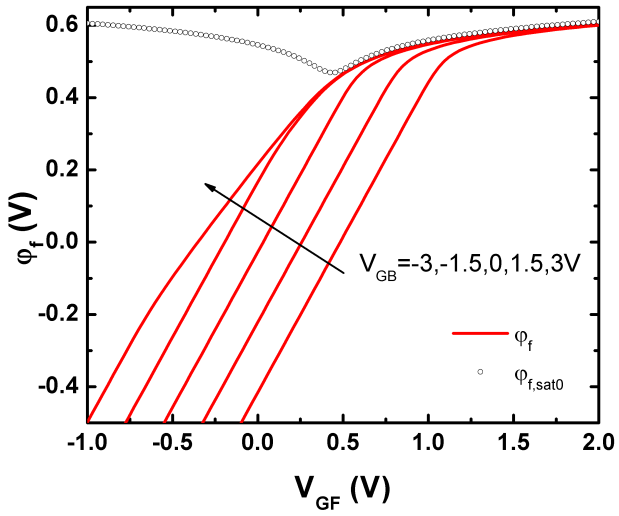

Figure 5.10. Initial front surface potential approximation in the strong inversion bias condition ($\phi_{f,sat0}$) versus front surface potential solution. $EOT_f = 2.4$nm, $EOT_b = 12$nm, $T_{ch} = 12$nm, $\Delta\Phi_f = -39$mV, and $\Delta\Phi_b = 0.45$V.

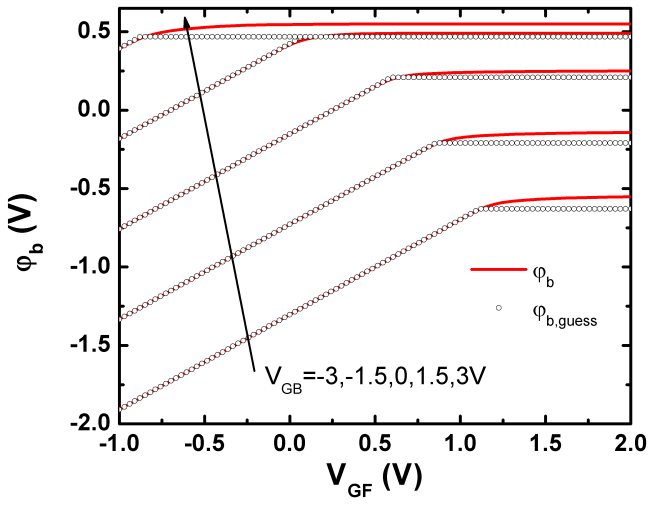

Figure 5.11. Back surface potential guess versus final solution. $EOT_f = 2.4$nm, $EOT_b = 12$nm, $T_{ch} = 12$nm, $\Delta\Phi_f = -39$mV, and $\Delta\Phi_b = 0.45$V.

For cases where $\alpha^2 < 0$, i.e. where the exponential term is large, an approximation for $\alpha \coth(\alpha/2)$ can be used [75]:

$$\alpha \coth(\alpha/2) \simeq \frac{(1/6 - 1/\pi^2)\alpha^4 + 2(1 + \pi^2/3)\alpha^2 + 8\pi^2}{\alpha^2 + 4\pi^2} \tag{5.18}$$

Replacing $\alpha \coth(\alpha/2)$ in (5.7) by (5.18) and assuming $x_f - \phi_f = q_1 \simeq 40$ (strong inversion condition), α^2_{sat} can be obtained for $\alpha^2 < 0$:

$$\alpha^2_{sat^-} = \frac{-T_1 + \sqrt{T_1^2 - 4T_0T_2}}{2T_0} \tag{5.19}$$

with T_0, T_1, and T_2 defined by:

$$T_0 = (1/6 - 1/\pi^2)q_t + 1 \tag{5.20}$$

$$T_1 = (2 + 2\pi^2/3)q_t + k_1q_1k_2q_2 + 4\pi^2 \tag{5.21}$$

$$T_2 = 4\pi^2(2q_t + k_1q_1k_2q_2) \tag{5.22}$$

where $q_2 = x_b - \phi_{b,guess}$ and $q_t = q_1k_1 + q_2k_2$. Figure 5.12 shows the values of α^2 for different front and back bias range and those obtained by $\alpha^2_{sat^+}$ and $\alpha^2_{sat^-}$. Although $\phi_{f,sat0}$ was obtained using $\alpha^2 = -4\pi^2$ the actual value for α^2 at saturation condition can largely differ from this approximation due the exponential dependence of α^2 on ϕ_f. $\alpha^2_{sat^+}$ and $\alpha^2_{sat^-}$ can be used to calculate $\phi_{f,sat}$ using equation (5.5) and appliying a single second order Newton-Raphson's iteration with initial guess equal to $\phi_{f,sat0}$. Now it is possible to unite the subthreshold approximation and the saturation approximation in a smooth manner with:

$$\phi_{f,guess0} = \frac{\phi_{b,guess} + k_f x_f}{1 + k_f} \tag{5.23}$$

$$\phi_{f,guess} = \phi_{f,guess0} - \ln(1 + \exp(\phi_{f,guess0} - \phi_{f,sat})) \tag{5.24}$$

Equation (B.7) is an updated version of (5.10) which includes the effect of back gate inversion. The initial guess for ϕ_f is shown in figure 5.13, close values to those calculated using final solution for (5.8) are obtained in the subthreshold and strong inversion conditions. The initial guess presented by equation (5.24) is used as the starting point to solve equation (5.8).

5.5 Iteration Update

Since the initial guess obtained by equation (5.24) is very closed to the final solution, only first order Newton-Raphson's updates ($\Delta\phi_f = -f/f'$) are needed to improve the accuracy of the solution which requires the calculation only of $f(\phi_f)$

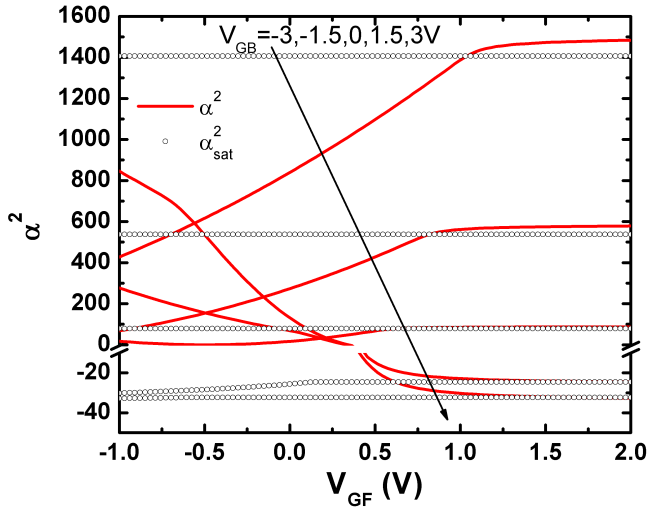

Figure 5.12. Approximate saturation values of α^2 versus α^2 final solution. $EOT_f = 2.4$nm, $EOT_b = 12$nm, $T_{ch} = 12$nm, $\Delta\Phi_f = -39$mV, and $\Delta\Phi_b = 0.45$V.

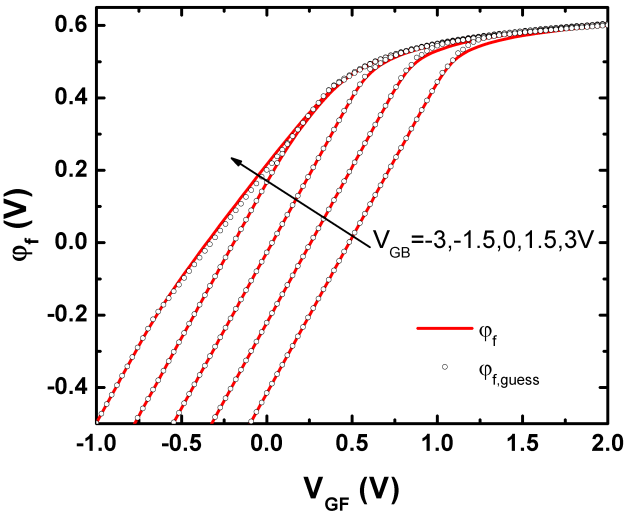

Figure 5.13. Front surface potential initial guess versus final solution. $EOT_f = 2.4$nm, $EOT_b = 12$nm, $T_{ch} = 12$nm, $\Delta\Phi_f = -39$mV, and $\Delta\Phi_b = 0.45$V.

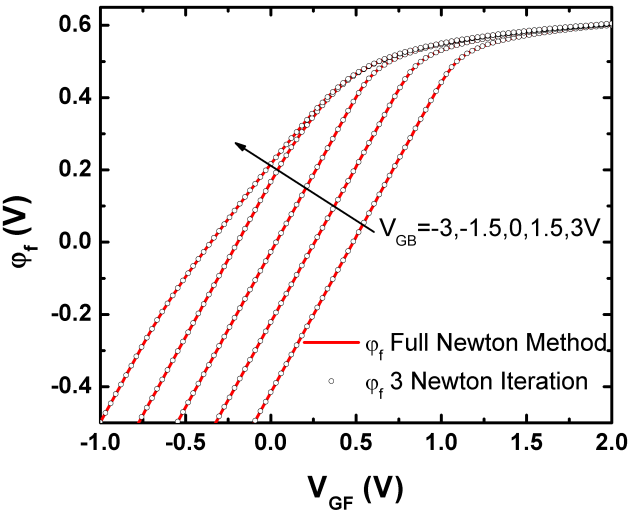

Figure 5.14. Front surface potential solution after three Newton-Raphson's iterations applied to initial guess versus full Newton solution. Full Newton method is implemented taking care the cases where α^2 turns less than -4π. $EOT_f = 2.4$nm, $EOT_b = 12$nm, $T_{ch} = 12$nm, $\Delta\Phi_f = -39$mV, and $\Delta\Phi_b = 0.45$V.

and its derivative $f'(\phi_f)$. The number of iterations needed is obtained by doing an extensive analysis of the proposed model accuracy under different device and bias conditions. It is found that using three iterations, an error of the order of μV is obtained. Figure 5.14 shows the excellent accuracy of the proposed analytical model. If same iterations are applied to an initial guess without updating $\phi_{f,sat}$, for example, using $\phi_{f,sat} = \phi_{f,sat0} - 2$mV in equation (5.24), Newton-Raphson's method does not converge because initial guess is not close enough to the final solution, as shown in figure 5.15. This proves the importance of a very accurate initial guess.

In summary, the proposed analytical model is obtained using the following procedure:

1. Calculate initial guess for back gate surface potential using (5.16).

2. Obtain $\phi_{f,sat}$ by updating $\phi_{f,sat0}$ with a second order Newton-Raphson's iteration of equation (5.5) using α^2_{sat+} (equation (5.17)) or α^2_{sat-} (equation (5.19)), for positive or negative values of α^2, respectively.

3. Calculate initial guess for front gate surface potential using (B.7) and (5.24).

4. Apply three first order Newton-Raphson's iterations to equation (5.8) with initial guess (5.24).

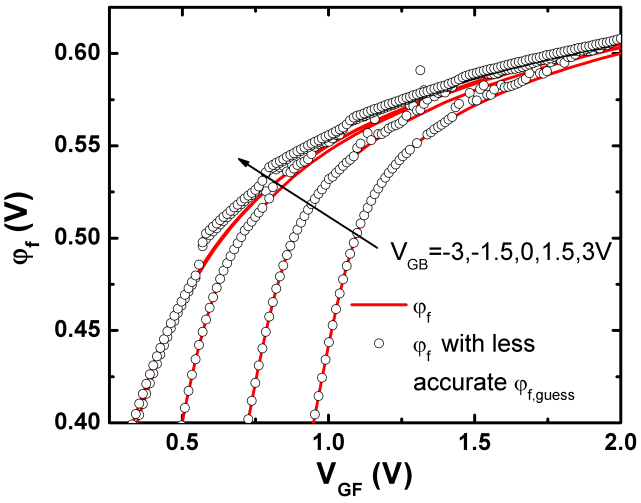

Figure 5.15. Front surface potential value after three Newton-Raphson's iterations applied to initial guess using $\phi_{f,sat} = \phi_{f,sat0} - 2\text{mV}$ versus front surface potential final solution. $EOT_f = 2.4\text{nm}$, $EOT_b = 12\text{nm}$, $T_{ch} = 12\text{nm}$, $\Delta\Phi_f = -39\text{mV}$, and $\Delta\Phi_b = 0.45\text{V}$.

Since the proposed analytical model only requires simple calculation updates and only first order Newton-Raphson's updates to the core equation (5.8), its speed is comparable to previous version of BSIM-IMG [37], which does not include back-side inversion. Indeed, compared to the model presented in [37], less than 10% extra computation time is obtained using the proposed model under different simulation scenarios (DC, AC, transient, etc.), a good trade-off considering the new features in the proposed model.

Once surface potentials are obtained, the total mobile charge is calculate using the mobile charge equation proposed in [75]:

$$q_m = \frac{k_f(x_f - \phi_f) - \alpha\coth(\alpha/2)}{1 - (\alpha^2/\sinh(\alpha/2)^2)(\exp(\phi_f)/A_0)} \tag{5.25}$$

Figure 5.16 shows the mobile charge versus front gate voltage for various back gate voltages. Simulation are obtained using finite difference method showed in Appendix D. Charge is accurately calculated using (5.25) from subthreshold to strong inversion condition. Note that back inversion is captured as well for large back bias condition.

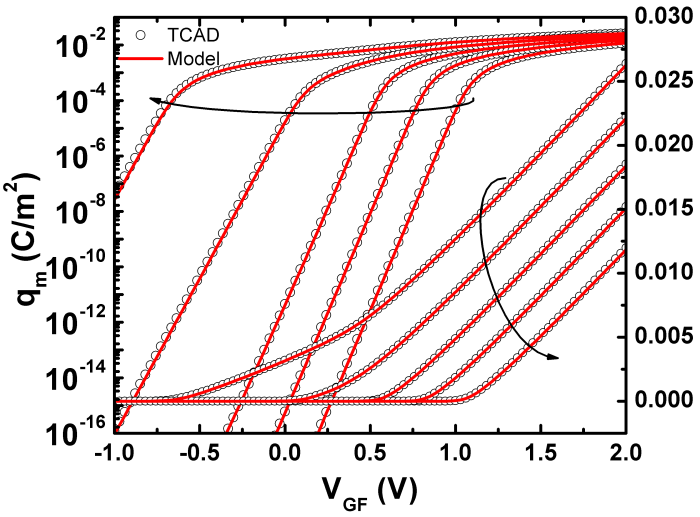

Figure 5.16. Mobile charge obtained from proposed front surface potential solution and TCAD for different V_{GB} values (-3, -1.5, 0, 1.5 and 3V). $EOT_f = 2.4$nm, $EOT_b = 12$nm, $T_{ch} = 12$nm, $\Delta\Phi_f = -39$mV, and $\Delta\Phi_b = 0.45$V.

5.6 Complete Model

The presented model for the mobile charge is incorporated into the industry-standard BSIM-IMG model [37]. Additional real device effects are incorporated to the final model in BSIM-IMG. As explained in [37], several extra models are added to the core and drain current models such as drain-induced barrier lowering, velocity saturation, short-channel effects, self-heating effect, front/back mobility-field dependence, substrate-depletion effect, etc. Figures 5.17 and 5.18 shows simulations of the complete BSIM-IMG model using the proposed analytical core model, with all real device models included, versus measured pmos data. The good accuracy demonstrates the capabilities of the proposed model as an industry standard compact model.

The inclusion of back-side inversion is a fundamental new feature in BSIM-IMG. Indeed, it is needed to obtain correct values of capacitances for cases where large forward bias is applied to back gate as shown by figures 5.19 and 5.20.

5.7 Conclusion

A new analytical model for the surface potential solution of independent multi-gate MOSFETs was presented in this work. The analytical solution is obtained by first deriving an accurate approximate solution (initial guess) of the implicit surface potential equation. It is constructed considering the behaviour of the implicit equation

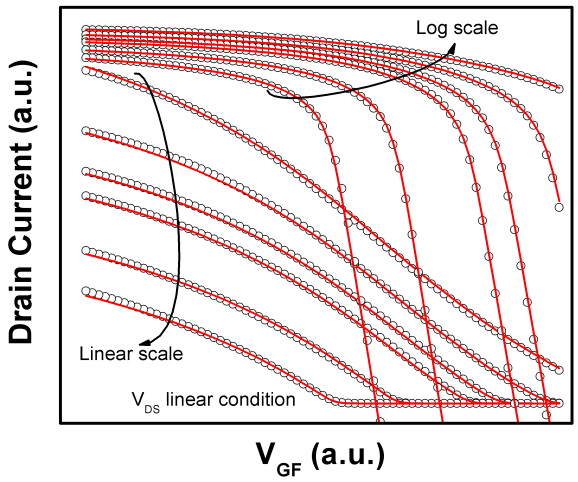

Figure 5.17. BSIM-IMG model versus measured data of $I_{DS} - V_{GF}$ characteristics at different values of V_{GB} at linear V_{DS} bias condition.

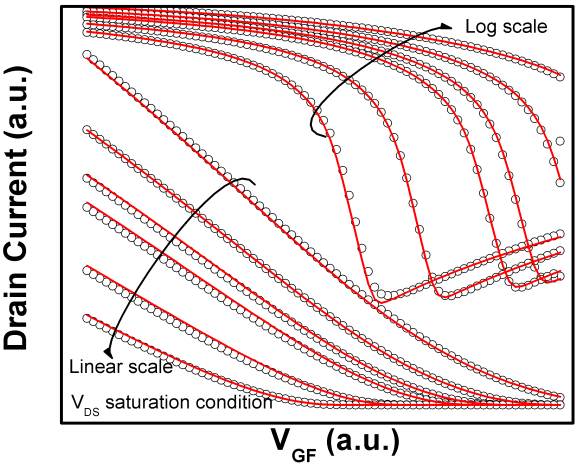

Figure 5.18. BSIM-IMG model versus measured data of $I_{DS} - V_{GF}$ characteristics at different values of V_{GB} at saturation V_{DS} bias condition.

under subthreshold and strong inversion conditions. The initial guess equation is then completed by updating it using three first order Newton-Raphson's iterations. The proposed analytical model is smooth, continuous, and it add less than 10% extra computation time compared to previous BSIM-IMG model. The model shows

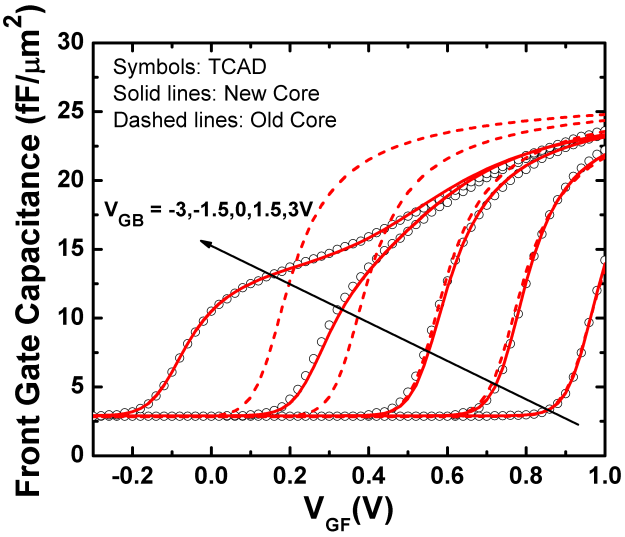

Figure 5.19. New BSIM-IMG model versus TCAD data of front gate capacitance at different values of V_{GB}. Previous version of BSIM-IMG model [43] is plotted as reference. EOT_f = 1nm, EOT_b = 20nm, T_{ch} = 6nm, $\Delta\Phi_f = -39$mV, and $\Delta\Phi_b = 0.45$V. TCAD and BSIM-IMG model include real device effects such as back gate depletion, quantum effects, etc. [43, 49].

excellent accuracy and convergence thereby ready for use in production level design kits.

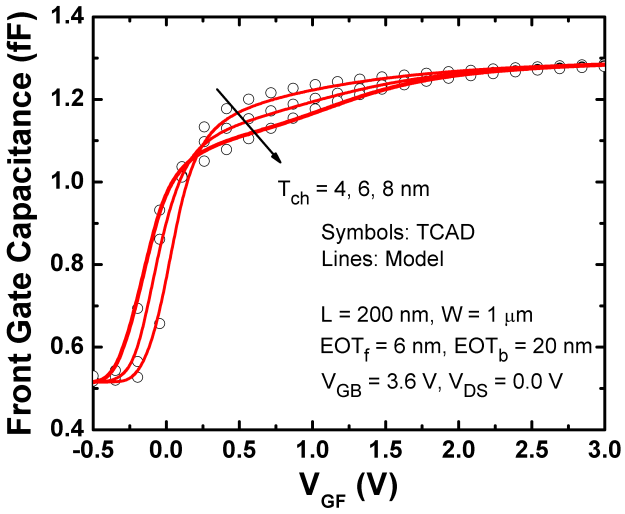

Figure 5.20. New BSIM-IMG model versus TCAD data of front gate capacitance at different values of T_{ch}. TCAD and BSIM-IMG model include real device effects such as back gate depletion, quantum effects, etc. [43, 49].

Chapter 6

Model for Negative Capacitance FETs

6.1 Introduction

Negative capacitance FETs (fig. 6.1) are quickly emerging as promising devices to achieve sub-60 mV/decade sub-threshold slope and high I_{on} [80, 10]. With recent experimental demonstrations of FE based NC-FETs [46, 45], there is an urgent need for analysis of device operation and circuit performance via compact models. In our previous work [38], we presented a lumped charge model NC-FinFETs. In this work we derive new insights into the device operation by analyzing and modeling both devices with floating metal gate and without it. The distributed charge model needs to be used for device without the floating metal. Significant differences in the characteristics of these two types of NC-FinFETs will be presented.

6.2 Unified Compact Model

The unified compact model, BSIM-CMG accurately predicts the charge and current voltage characteristics of different FinFETs and gate-all-around structures [23]. BSIM-CMG's core equation is a single unified charge model (UCM), a closed form relationship between the mobile charge (Q_m) and the applied terminal voltages (V_G,V_D,V_S,V_B) given in a normalized form as follows:

$$v_G - v_o - v_{ch} = -q_m + \ln(-q_m) + \ln\left(\frac{q_t^2}{e^{q_t} - q_t - 1}\right) \tag{6.1}$$

where v_{ch} is the normalized channel potential. v_o and q_t are defined in table 6.1.The UCM requires only four different model parameters [23]: insulator capacitance (C_{ins}),

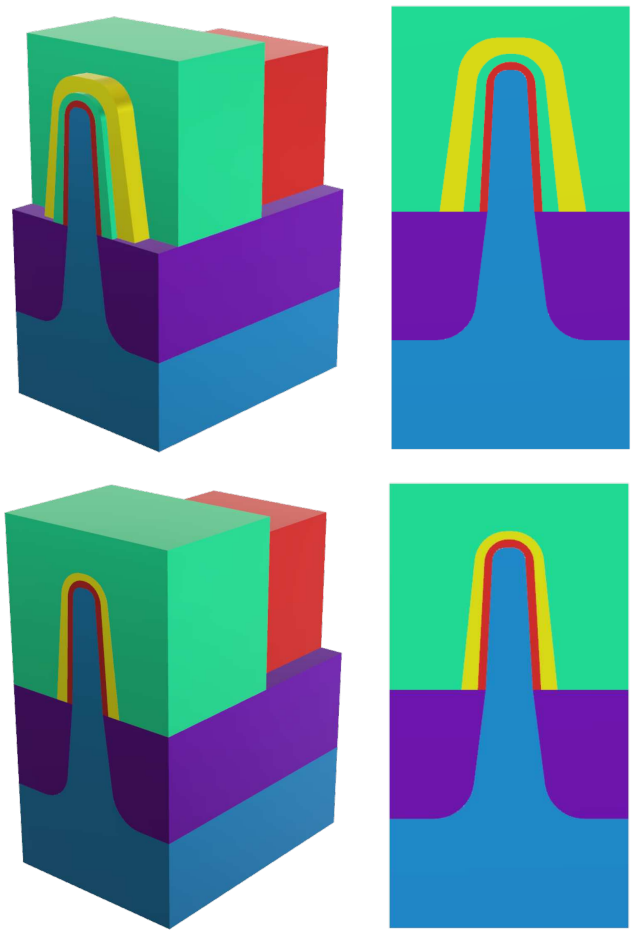

Figure 6.1. Schematic of NC-FinFETs: 3D and 2D device cut. Lumped NC-FinFET (top) has a floating gate between insulator and FE. The distributed NC-FET (bottom) does not have a floating gate.

channel area (A_{ch}), channel doping (N_{ch}) and effective channel width (W_{eff}). Using these parameters, we accurately modeled the characteristics of a 14nm node Ultra-Low-Power FinFET [36], which is the baseline FinFET technology used in this work.

6.3 Ferroelectric Material Model

A compact model of FE materials, which captures the negative capacitance correctly, is obtained using the Landau Khalatnikov (LK) equation [44]. LK expresses the relationship between electric-field (E) and polarization (P) of a FE:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \tag{6.2}$$

Table 6.1. Unified compact model and FE model variables

Variable	Definition
v_G, v_{ch}, v_T	$\frac{V_G}{v_T}$, $\frac{V_{ch}}{v_T}$, $\frac{kT}{q}$ (Thermal Voltage)
q_m, q_{dep}	$\frac{Q_m}{v_T C_{ins}}$, $\frac{-qN_{ch}A_{ch}}{v_T C_{ins}}$
v_o	$v_{FB} - q_{dep} - \ln\left(\frac{2qn_i^2 A_{ch}}{v_T C_{ins} N_{ch}}\right)$
q_t	$(q_m + q_{dep})r_N$
r_N	$\frac{A_{Fin}C_{ins}}{\varepsilon_{ch}W_{eff}^2}$
a_0	$2\alpha t_{FE} C_{ins}/W_{eff}$
b_0	$4\beta t_{FE}(v_T C_{ins}/W_{eff})^3/v_T$
c_0	$6\gamma t_{FE}(v_T C_{ins}/W_{eff})^5/v_T$

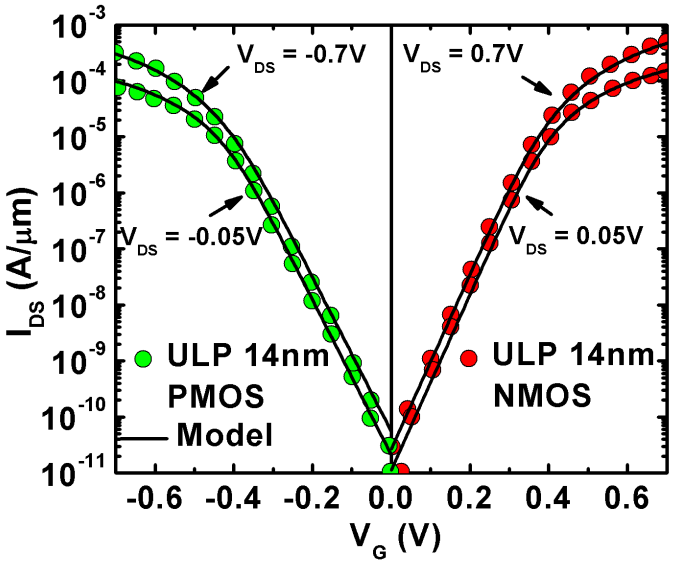

Figure 6.2. 14nm Ultra-Low-Power FinFETs [36] versus the fitted BSIM-CMG Model.

where α, β, and γ, are material parameters. Equation (8.1) captures the energetically unstable region where the capacitance is negative (red dots in fig. 6.3). The negative capacitance regime of FE materials can be stabilized by connecting it in series with a positive capacitance [80] such as the gate capacitance of the FinFET in the FE NC-FinFET system. The charges in the two series capacitors are equal, i.e., $P = L_G Q_{ch}$, where Q_{ch} is the channel (dopant and mobile) charge per unit length. It is therefore possible to model such a system replacing v_G in (6.1) with $v_G - v_{FE}$ where v_{FE} is the normalized FE voltage from (8.1):

$$v_{FE} = -(a_0 q_{ch} + b_0 q_{ch}^3 + c_0 q_{ch}^5) \tag{6.3}$$

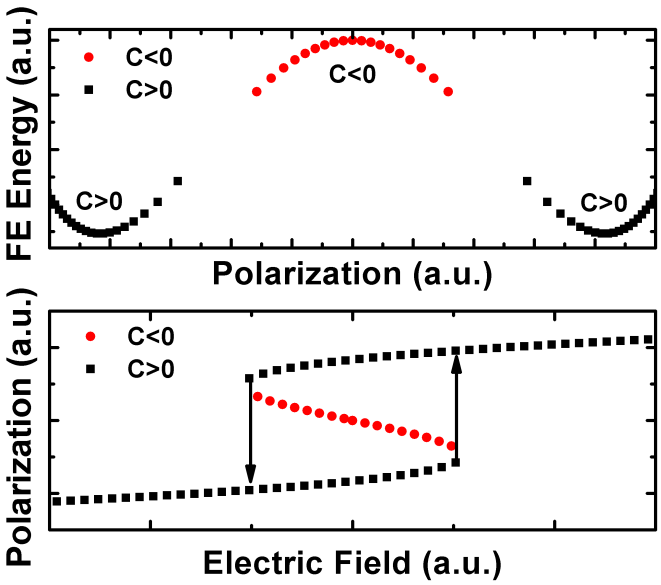

Figure 6.3. Energy landscape and polarization of the FE with red dots showing the negative capacitance regime.

where a_0, b_0, and c_0 are defined in table 6.1. The model simulates the behavior of the $V_{DS} = 0V$ NC-FinFET connection (figs. 6.4 and 6.5). The compact model captures how the FE thickness (t_{FE}) can be used to stabilize the negative capacitance (avoiding the hysteresis by making $-C_{FE} > C_{mos}$), and to adjust the voltage gain, which is $|C_{FE}|/(|C_{FE}| - C_{mos})$[10]. The concept of voltage amplification is illustrated in Fig. 6.5. Because V_{FE} is negative, the voltage across C_{mos} in Figs. 6.4 and 6.5 is larger than V_G. This is the gist of why NCFET can operate at lower voltage. There is no significant voltage gain unless C_{mos} is comparable to $-C_{FE}$.

6.4 Lumped NC-FinFET Model

In a NC FinFET with a floating metal gate, the charge used to calculate v_{FE} is the average charge in the gate:

$$q_G = \frac{1}{L_G}\int_0^{L_G}(q_m + q_{dep} + q_{parasitics})dx \tag{6.4}$$

$v_G - v_{FE}$ is the voltage of the floating gate, i.e., the gate of the underlying FinFET. Since calculating q_G requires q_m, it and q_G cannot be obtained explicitly using (6.1) and (6.4); therefore, they are calculated self-consistently by the simulator using an internal model node for the floating gate [38]. The normalized current can be calculated

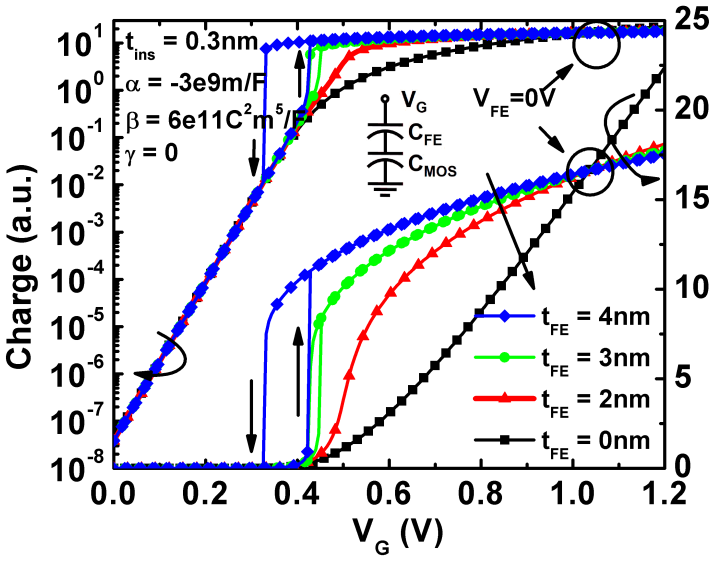

Figure 6.4. Channel charge versus V_G for different t_{FE} obtained from the model. Note that all curves meet at a given V_G where $V_{FE} = 0V$ (see fig. 6.5). $C_{parasitic} = 0$ in Figs. 6.4 to 6.7.

as in a regular FinFET [23]:

$$i_{DS} = \int_0^{v_{DS}} q_m dv_{ch} \tag{6.5}$$

Figs. 6.6 and 6.7 show the current-voltage and FE voltage simulated characteristics of lumped FE NC-FinFETs for different t_{FE} values. Drain current is amplified when a FE layer is used. The current amplification is proportionally to t_{FE} for V_G values close to threshold voltage. When t_{FE} is too thick, the device is no longer stable and there is an anticlockwise hysteresis present in the current.
Figs. 6.8 and 6.9 show the current-voltage and FE voltage characteristics of the lumped NC-FinFETs for different parasitic capacitance values. The parasitic capacitances increase the charge available in the subthreshold region, producing a boost in the voltage amplification before onset of inversion (fig. 6.9). The model has been validated against experimental data obtained from a NC-FinFET with excellent agreement (fig. 6.10) [38].

6.5 Distributed NC-FinFET Model

Equation (6.1) can be used to model NC-FinFETs without a floating gate by replacing v_G by $v_G - v_{FE}$ and using the local channel charge along the channel to

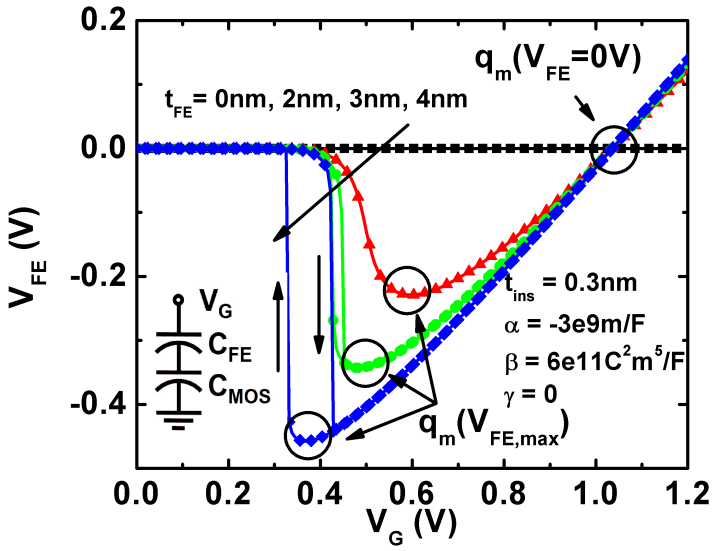

Figure 6.5. V_{FE} versus V_G for different t_{FE} obtained from the model. At $V_{FE} = 0V$, $q_m = -(-a_0/b_0)^{0.5}$. V_{FE} peak is obtained at $q_{m,V_{FEPEAK}} = -(-a_0/(3b_0))^{0.5}$, making $V_{FE,max}$ linearly dependent on t_{FE}.

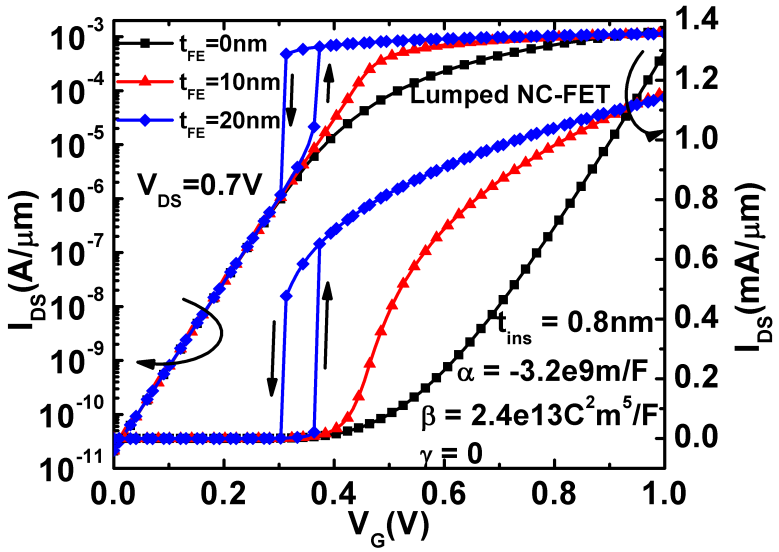

Figure 6.6. Lumped model generated $I - V$ of NC-FinFETs for several t_{FE}. Anti-clockwise hysterisis is present for FE NC-FinFET with overly large t_{FE}.

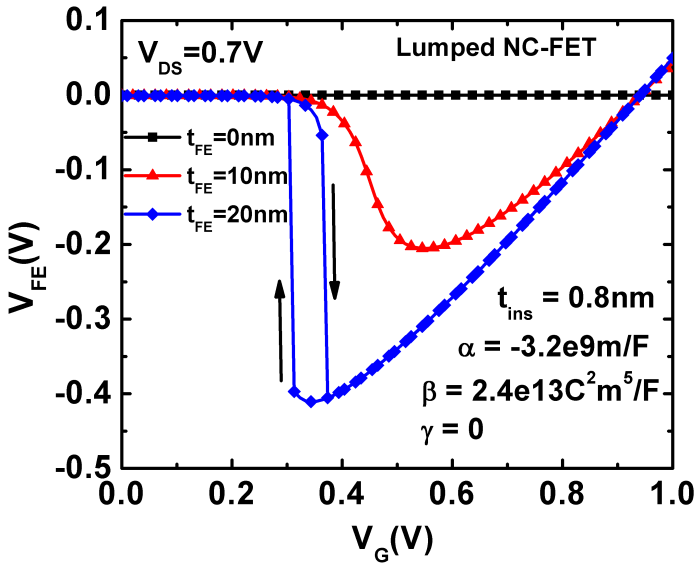

Figure 6.7. Modeled V_{FE} versus V_G of lumped NC-FinFETs for different t_{FE}. For $t_{FE} = 10nm$ the FE is not stabilized, producing anticlockwise hysteresis.

determine the local v_{FE}. If the resulting system does not produce hysteresis characteristics, equation (6.5) can be used directly to obtain the drain current. When hysteresis is present, the drain current must be obtained considering the hysteresis at each point of the channel. This can be implemented using Gauss-Legendre quadrature:

$$i_{DS} = \int_0^{v_{DS}} q_m dv_{ch} \approx \sum_{i=1}^{n} q_m(v_{ch,i}) w_i \tag{6.6}$$

where $v_{ch,i}$ is given by $v_{ch,i} = (v_D - v_S)(x_i + 1)/2 + v_S$, n represents the number of Gauss points used for the integration, and x_i and w_i are the abscissas and weights of the Gauss-Legendre quadrature. Fig. 6.11 shows the drain current versus gate voltage of distributed NC-FinFETs for different t_{FE} values. The FE material causes a current amplification; however, it is different than the case of a lumped configuration. Compared to the lumped configuration, the strong inversion current slope (transconductance) of the distributed device is not largely affected by t_{FE} thickness. In addition, the hysteresis transitions are smoother than the lumped case. The model captures this distributed nature of the device by evaluating the charge and V_{FE} along the channel length (fig. 6.12). Including parasitic capacitance also improves the subthreshold swing of the device for the same reason it does to the lumped configuration.

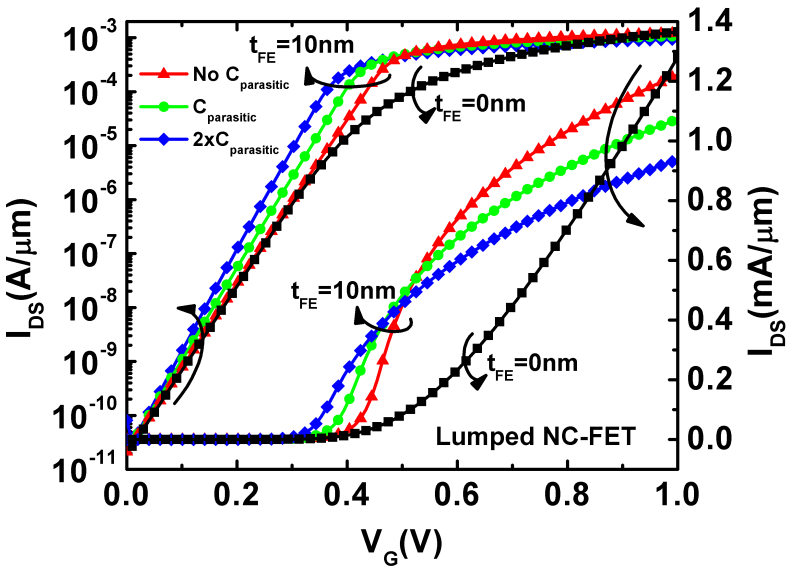

Figure 6.8. Model generated $I-V$ of lumped NC-FinFETs for different $C_{parasitic}$. The larger C_{mos} increase the voltage gain in the subthreshold region.

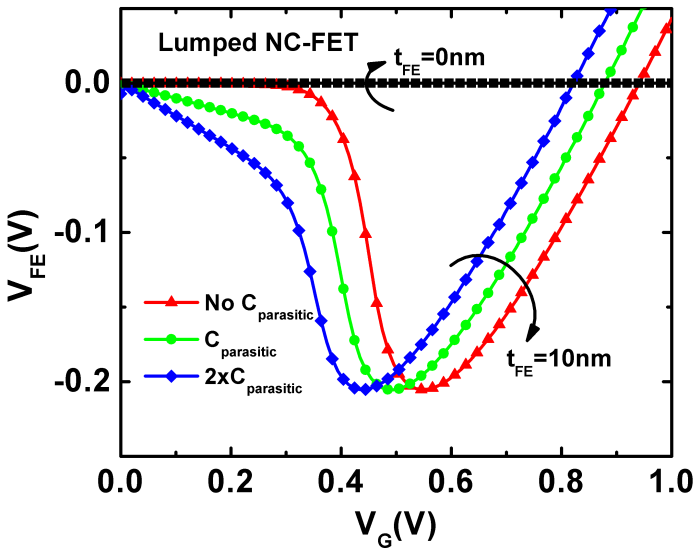

Figure 6.9. Model generated V_{FE} versus V_G of lumped NC-FinFETs for different $C_{parasitic}$. Note that the peak magnitude of V_{FE} is not affected.

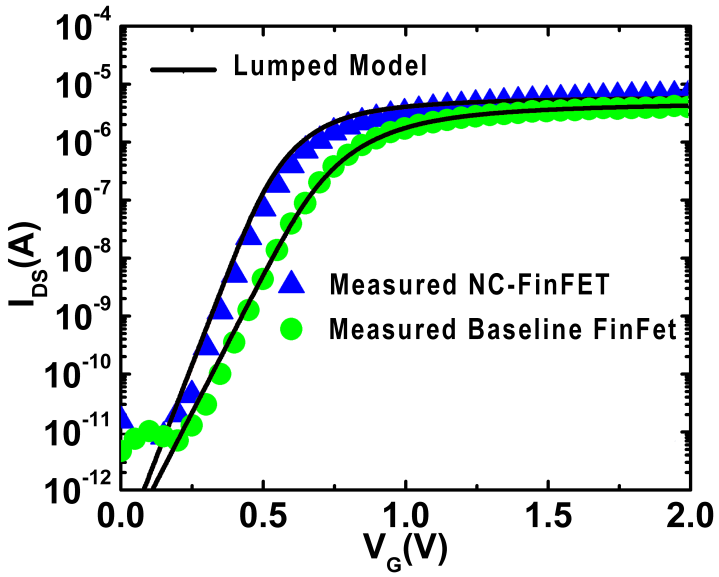

Figure 6.10. Experimental validation of the lumped model against FE NC-FinFET [46, 38].

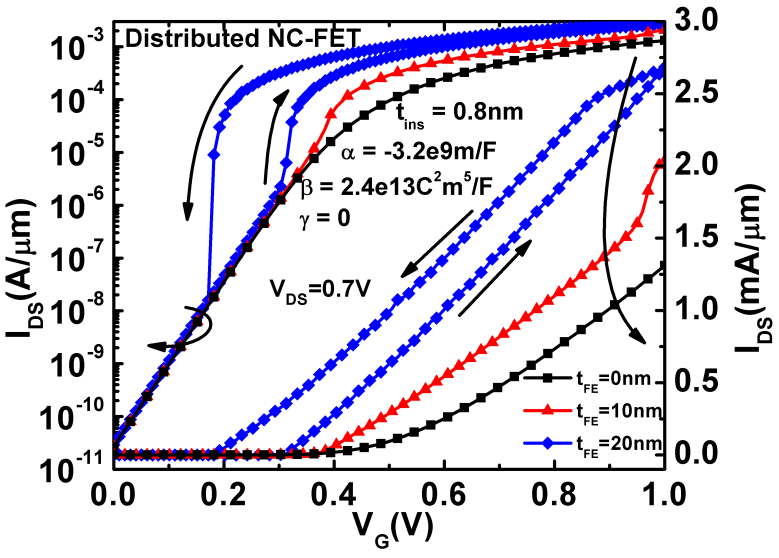

Figure 6.11. Modeled $I-V$ of distributed NC-FinFETs for different t_{FE}. Hysterisis is present overly large t_{FE} but smoother than the case of lumped NC-finFET.

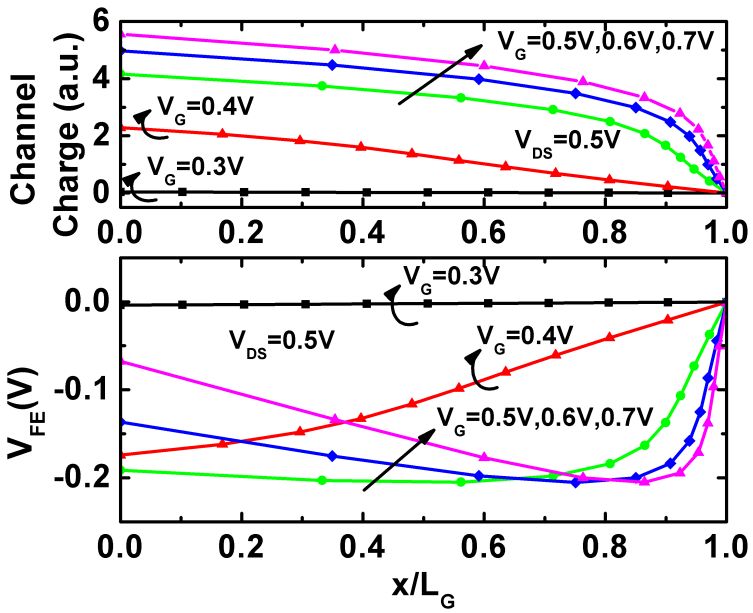

Figure 6.12. Channel charge (Top) and ferroelectric voltage along the channel length for different gate voltages in the distruted charge NC-FinFET shown in fig. 6.11 with $t_{FE} = 10nm$.

6.6 Lumped versus Distributed NC-FinFETs

Fig. 6.13 shows a comparison of the drain current versus gate voltage in lumped and distributed device configurations. The subthreshold swing improvement is similar in both cases. On the other hand, the lumped device current becomes saturated at larger voltages, where the distributed configuration, shows an approximately linear increment of current for larger gate bias. The transconductance of lumped device has a larger peak than the distributed one (fig. 6.14); where the latter has a transconductance with lower value but approximately constant at higher bias windows. The differences in device characteristics are attributed to the totally different FE voltage and charge distribution in the device.

6.7 Time-Dependent Ferroelectric Model

Using the Time-Dependent LK model, it is possible to expresses the relationship between electric-field (E) and polarization (P) of a FE:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - \rho_{FE}\frac{dP}{dt} \tag{6.7}$$

The above equation include a new term, ρ_{FE}, which is a resistivity-like parameter that can be use to represent FE switching speed. It is very important to notice that

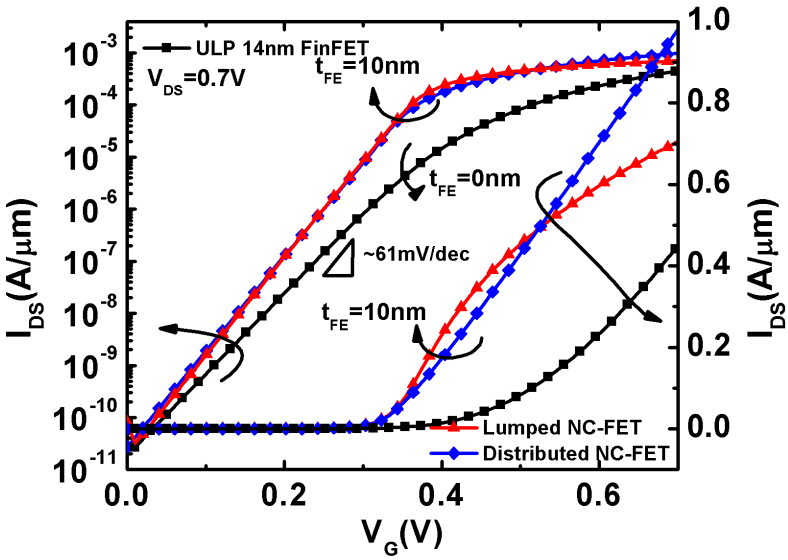

Figure 6.13. $I-V$ lumped and distributed NC-FinFETs. Subthreshold behaviors are similiar; however, strong inversion characteristics are different.

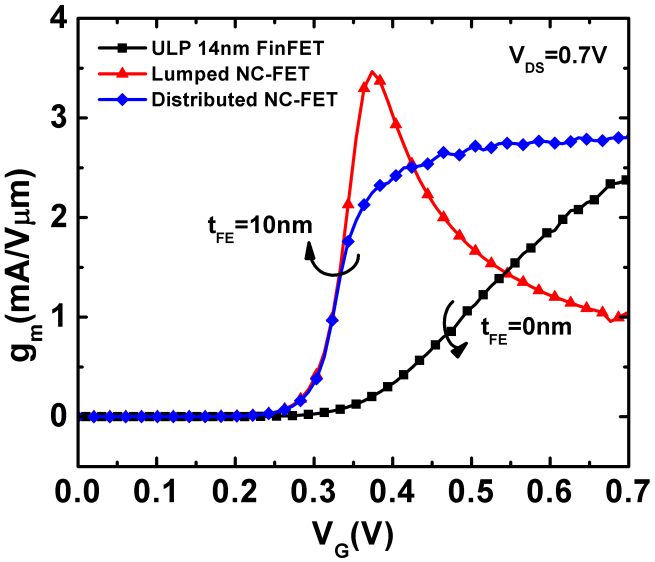

Figure 6.14. Transconductance (g_m) versus gate voltage in lumped and distributed configurations. A larger larger g_m peak is presented in the lumped device compared to the distributed configuration; however, the larger peak rapidly decreases as V_G increases.

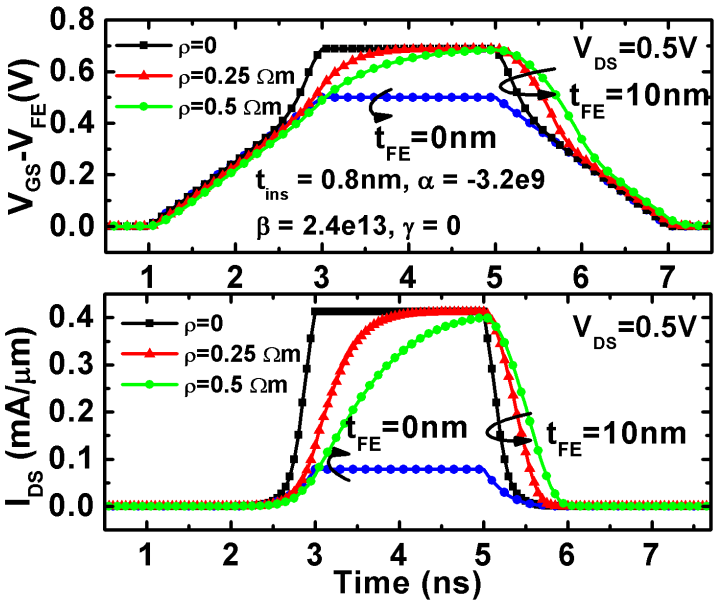

Figure 6.15. Simulation of lumped NC-FinFETs including resistive term in LK equations for FE. Model can capture the extra device delay.

in this chapter, the values used for ρ_{FE} are just to see model behaivor and do not represent real values since it has been demonstrated that intrinsic values of ρ_{FE} are very small [12]. Figures 6.15 and 6.16 show simulations of NC-FETs including the resistive term (with lumped model). The hysteresis-like drain current characteristics are due the extra resistive term in the FE model.

6.8 Model Robustness

The robustness of the lumped model has been already verified in a commercial circuit simulator [38]. Here, the distributed model is implemented in Verolog-A code [19] and tested in a commercial circuit simulator. Fig. 6.17 shows the results of 17-stage ring-oscillator circuit simulations using the distributed charge model. Simulations converge in similar speed rates compare to BSIM-CMG model, validating the its functionality for IC simulation and design.

6.9 Conclusion

Lumped and distributed compact models for NC-FinFETs have been presented in this work. The models capture the characteristics that make NC-FET a candidate for future low power transistor due the possibility of achieving less than 60mV/dec

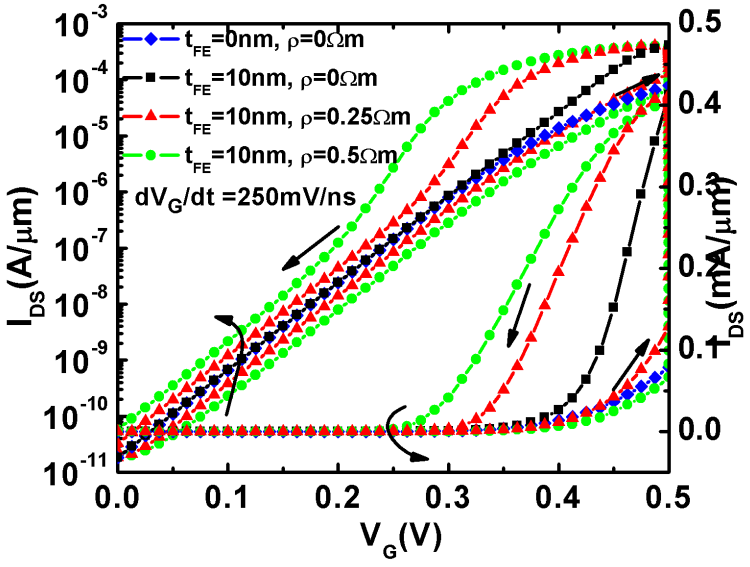

Figure 6.16. Simulation of lumped NC-FinFETs including resistive term in LK equations for FE. Delay induces hysterisis-like I-V curve simulations.

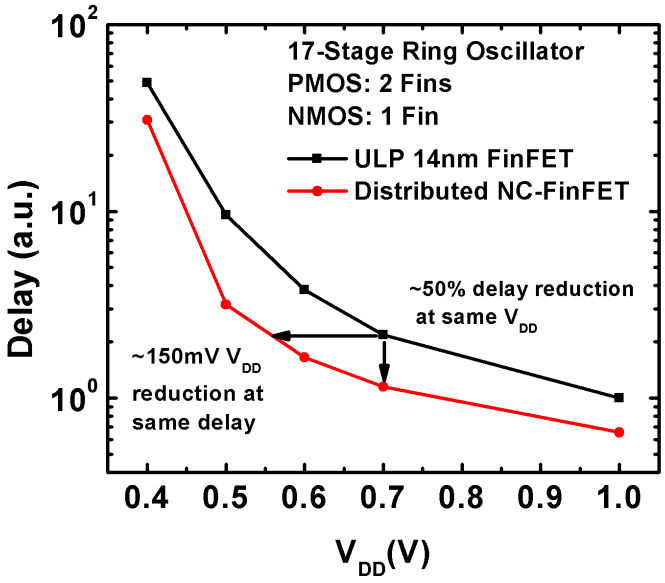

Figure 6.17. Delay versus supply voltage of 17-stage ring-oscillator. This example shows the benefits trends, not the maximum potential improvement.

and higher on-current. Floating metal gate case is modeled via lumped compact model, while a distributed compact model is used for devices without floating metal. Clear $I - V$ and g_m differences between lumped and distributed devices are present in the strong inversion condition. The proposed models are implemented and tested in circuit simulators.

Chapter 7

Numerical Simulation of Negative Capacitance FETs

7.1 Introduction

This chapter present a numerical simulation approach for Negative-Capacitance transistor. Most of the numerical simulation of NCFETs are based on a TCAD simulation couple to a ferroelectric system but using a metal interface between these two systems. The advantage of that approach is the simplicity. When a metal is used, the polarization of the ferroelectric is constant along the channel (assuming single domain approximation); therefore, a single ferroelectric voltage is calculated using the average charge of the transistor. This allows to first simulate a base-line device using any type of numerical simulation and then, when results are obtained, recalculate the effective V_G as if the ferroelectric is present. The drawback of this approach is that NCFETs in real application will not have a metal gate between interfacial layer and ferroelectric material. Indeed, a more realistic NC transistor structure is shown in figure 7.1, where under the gate metal there is a material ferroelectric material, in this case, hafnium zirconium oxide. It sits on an interfacial oxide and that sits on the silicon substrate. Therefore, simulations that want to describe in a more realistic way, need to include the effect of different effective polarization across the channel. The work presented in [68] presented a fully coupled 3-D simulation of NC-FinFETs with (lumped) and without internal metal gate (distributed); however, the distributed simulation had some convergence difficulties and I-V curves for this case were not presented. The simulation approach study by [22] solved a 2-D simulation of NC-UTBSOI transistor using a monolayer MoS_2 semiconductor material for the channel. However, other materials were not included in the study, such as silicon of different channel thickness, the most important material for the next generation

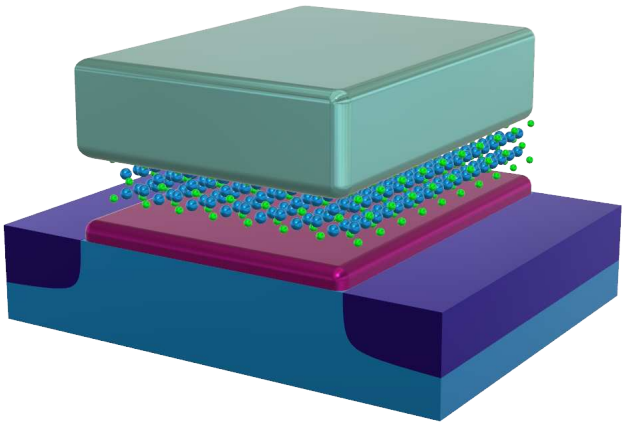

Figure 7.1. Negative Capacitance transistor structure in a conventional planar technology.

of nano-scale devices. This chapter presents a quasi 2-D numerical simulation of NC-FinFETs, capturing short-channel effects and device dependence of drain current characteristics.

7.2 Quasi 2-Dimensional NC-FET Simulation

A 2-dimensional transistor coupled at each mesh point to a 1-dimensional Laundau ferroelectric model is presented in this section. Figure 7.2 shows a schematic of the proposed approach. The transistor structure is solved self-consistently with boundary condition at source, drain, front gate, and back gate. The key point to include the simulation is to update the potential boundary condition at each point of the interfacial layer mesh with a value calculated with a 1-dimensional Landau-Khalatnikov ferroelectric model [44]. Figure 7.3 shows the proposed concept. The first simulation assumes a constant value of potential at the interfacial layer, as in the case of a metal gate material over the layer. After first simulation is obtained, the displacement values at the interfacial layer boundary are use to obtain the ferroelectric voltage (V_{FE}) at each point of the mesh. Using the values of V_{FE} along the channel, the potential boundary condition at the interfacial layer is updated ($V'_{G,i} = V_{G,i} - V_{FE,i}$ with $i = 0, .., n$ node) and a new 2-D device simulation is calculated. This step is repeated until the values of V_{FE} do not change any more with respect to the previous iteration update. Figure 7.4 shows the results of a NC-FinFET transistor using the proposed approach. Good convergence is obtained for different structure dimensions and ferroelectric parameters. One of the main objective of this simulation is

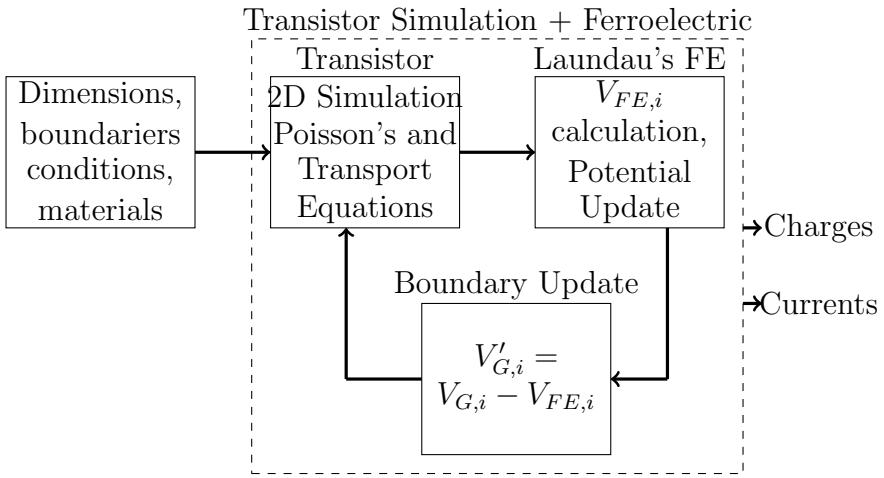

Figure 7.2. Self-consistence diagram of 2D transistor simulation with ferroelectric.

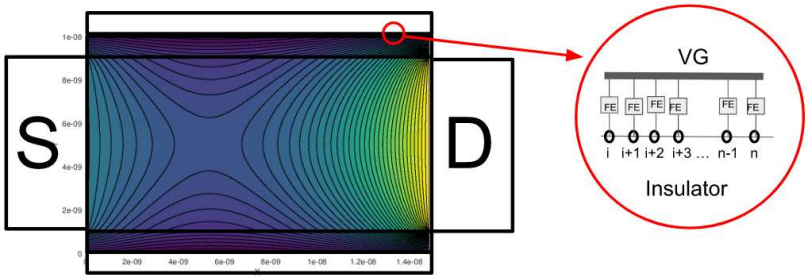

Figure 7.3. Diagram of 2D transistor simulation with ferroelectric. Boundary conditions at insulator-ferroelectric interface are updated using Laundau's calculations.

to understand the electrostatic behavior of NC-FETs therefore simple drift-diffusion mechanism is used to obtain the drain current, where a constant material mobility is used for the calculations.

7.3 NC-FET L_G Scaling

Most of the literature on NC-FETs focuses on capability of NC-FETs to obtain under 60mV/dec swing characteristics. However, even if 60mV/dec cannot be achieved, substantial improvements can be obtained as gate lengths are reduced, making NC-FETs perfect candidates for extremely scaled technologies. As gate length is reduced at a constant Fin thickness $T_{ch} = 6nm$, and $EOT = 0.6nm$, conventional FinFET characteristics are worsened due short-channel effects as shown in figure 7.5. However, using a NC-FinFET structure with a ferroelectric layer (hafnium zirconium oxide in the presented simulation) of thickness $t_{FE} = 3nm$, remnant polarization

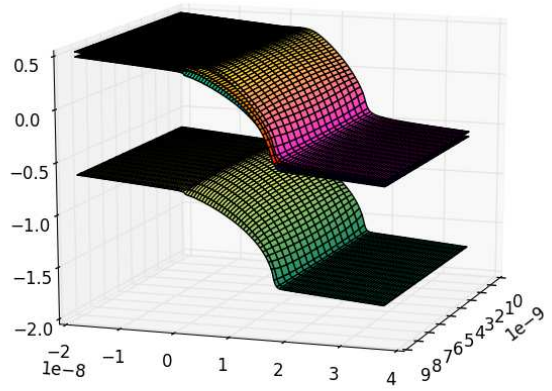

Figure 7.4. Numerical results of the quasi 2-Dimensional NC-FET simulation. The figure shows conductance and valence bands together with quasi-fermi levels of electrons and holes. $V_{DD} = 1.05V$.

$P_R = 15\mu C/cm^2$ and coercive field $E_C = 1.4MV/cm$ [71], short-channel effects are largely reduced as shown in figure 7.6.

The off drain current (I_{OFF}) is largely reduced when a NC-FinFET structure is used, figure 7.7, allowing the scaling of NC-FinFETs to smaller nodes than conventional FinFETs. The I_{OFF} improvement is mainly comming from the reduction of subthreshold swing for the NC-FinFETs as shown in figure 7.8. NC-FinFETs present better SS than conventional FinFETs; indeed, SS of NC-FinFET at 6nm node is similar to the SS of regular FinFET at 10nm node. Other electrostatic characteristics of transistors are superior for the NC-FinFET structures, such as threshold voltage (figure 7.9) and DIBL (figure 7.10).

The ferroelectric voltage (V_{FE}) across the channel is shown in figures 7.11 and 7.12 for the linear and saturation bias case, respectively. Both figures shows that a distributed approach is needed for the simulation of NC-FiNFETs as V_{FE} largely changes from source to drain. Indeed, the ferroelectric polaritaziton may drastically change from source to drain as shown figure 7.13 and 7.14. Both figures show that the NC-FinFET described in this chapter is electrostatically in the negative-capacitance region; however, source and drain characteristics change drastically. Source side shows a positive gate voltage amplification ($V_{FE} < 0$) while drain a negative gate voltage amplification ($V_{FE} > 0$).

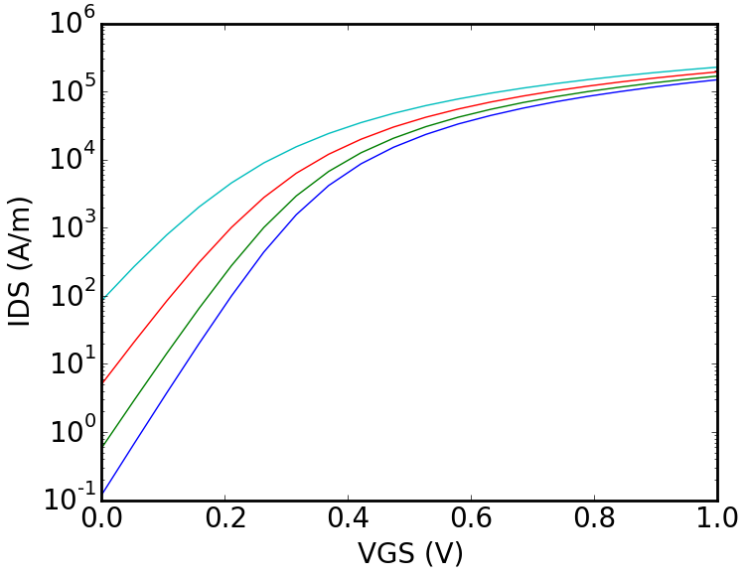

Figure 7.5. Drain current characteristics of FinFETs for different technology nodes ("10/9", "8/7", "6/5", and "4/3" nodes) with physical $L_G = 16nm, 14nm, 12nm, 10nm$. $V_{DD} = 1.05V$.

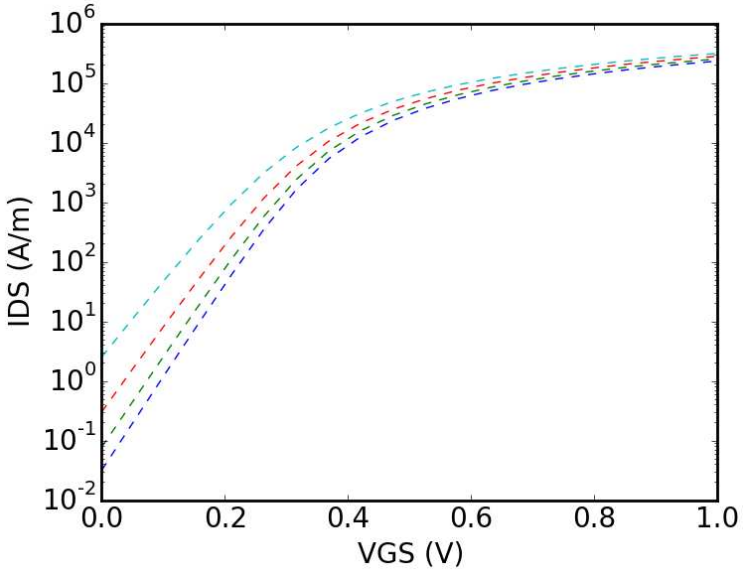

Figure 7.6. Drain current characteristics of NC-FinFETs for different technology nodes ("10/9", "8/7", "6/5", and "4/3" nodes) with physical $L_G = 16nm, 14nm, 12nm, 10nm$. $t_{FE} = 3nm$, $P_R = 15\mu C/cm^2$ and $E_C = 1.4MV/cm$. $V_{DD} = 1.05V$.

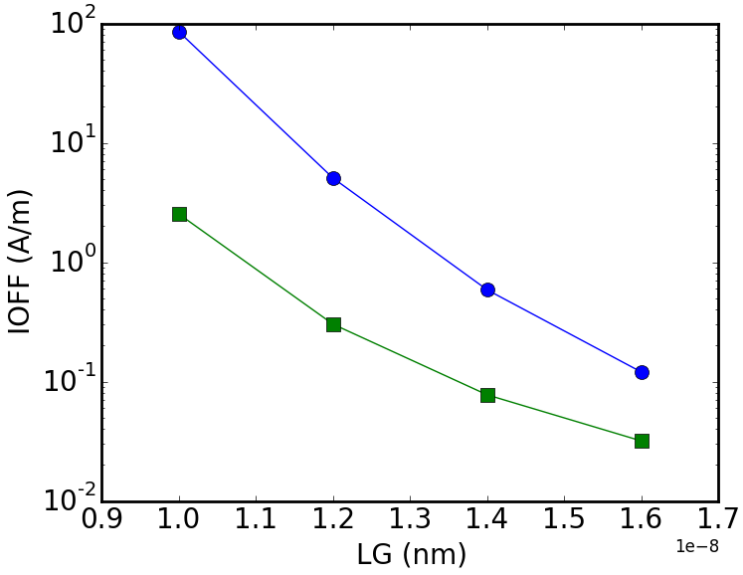

Figure 7.7. I_{OFF} for FinFETs (blue circles) and NC-FinFETs (green squares) for different technology nodes ("10/9", "8/7", "6/5", and "4/3" nodes) with physical $L_G = 16nm, 14nm, 12nm, 10nm$. $t_{FE} = 3nm$, $P_R = 15\mu C/cm^2$ and $E_C = 1.4MV/cm$. $V_{DD} = 1.05V$.

7.4 NC-FET with Low Coercive Field: lowering effective EOT

A large coercive field is needed for large voltage amplification; however, one point that needs to be mentioned is the fact that the ferroelectric material in NC-FETs is replacing the high-k material of the base-line transistor. Indeed, there are several reports where different high-k materials (such as hafnia or hafnium zirconium oxide) become ferroelectric under different fabrication condition and doping. Therefore, even if the coercive filed of the obtained ferroelectric material is low, the effective EOT of the new device will be lower than the base-line device, reducing short-channel effect as well. The above statement is correct if positive capacitance condition in ferroelectric is not reached for the bias conditions of the NC-FET. In other words, even if the ferroelectric does not amplify the gate voltage, it acts as a transparent dielectric material, where voltage is not dropped and the final capacitance of the MOS structure is only defined by the initial interfacial layer. This may explain the results recently show by Globalfoundries at IEDM 2017 [9]. From their results, the remnant polarization is $P_R = 22\mu C/cm^2$ and coercive field is $E_C = 0.25MV/cm$, approximately. Figure 7.15 shows simulations of the drain current comparison of base line FinFET and NC-FinFET where high-k material is replaced by a ferroelectric material with parameters similar to those reported in [9]. We can see that the difference of NC-FinFETs at

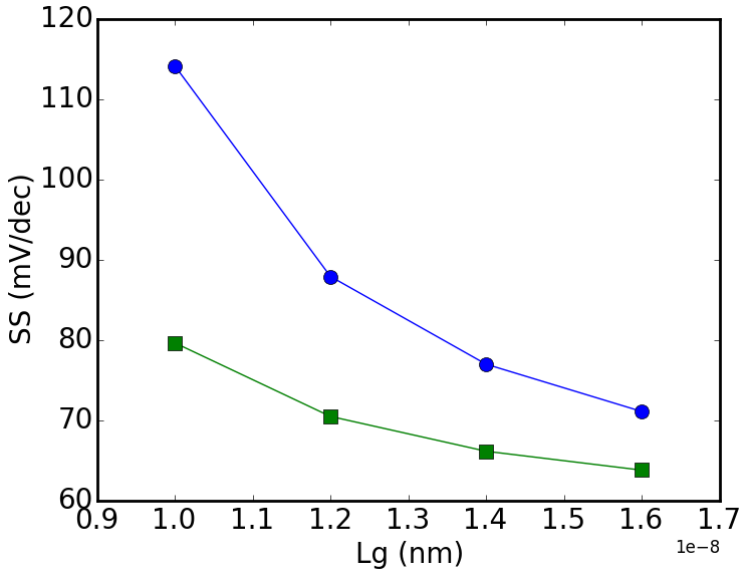

Figure 7.8. Subthreshold swing for FinFETs (blue circles) and NC-FinFETs (green squares) for different technology nodes ("10/9", "8/7", "6/5", and "4/3" nodes) with physical $L_G = 16nm, 14nm, 12nm, 10nm$. $t_{FE} = 3nm$, $P_R = 15\mu C/cm^2$ and $E_C = 1.4MV/cm$. $V_{DD} = 1.05V$.

different FE thickness is very small, and the main improvement of the device with respect to the base-line device is due the lowering of the effective EOT as shown in figure 7.16, where subthreshold swing is shown for both devices as well. A SS improvement of approximately 5mV/dec is achieved with the ferroelectric of a weak coercive field, mainly due reduction of the effective EOT. DIBL is also improved with respect the baseline, as shown in figure 7.17, where DIBL characteristics are weakly dependent on FE thickness. The little amplification of the applied voltage can be observed in figure 7.18. Less than 0.1V amplification is obtained for $t_{FE} = 5nm$, in addition, the FE does not reach positive capacitance region; therefore, the FE acts as an electrically transparent material where effective EOT is reduced with respect to the base-line FinFET with high-k material.

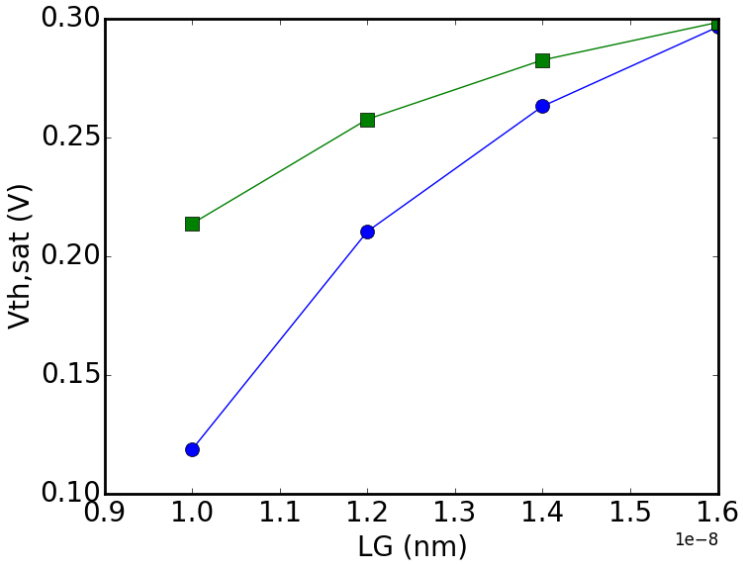

Figure 7.9. Threshold voltage for FinFETs (blue circles) and NC-FinFETs (green squares) for different technology nodes ("10/9", "8/7", "6/5", and "4/3" nodes) with physical $L_G = 16nm, 14nm, 12nm, 10nm$. $t_{FE} = 3nm$, $P_R = 15\mu C/cm^2$ and $E_C = 1.4MV/cm$. $V_{DD} = 1.05V$.

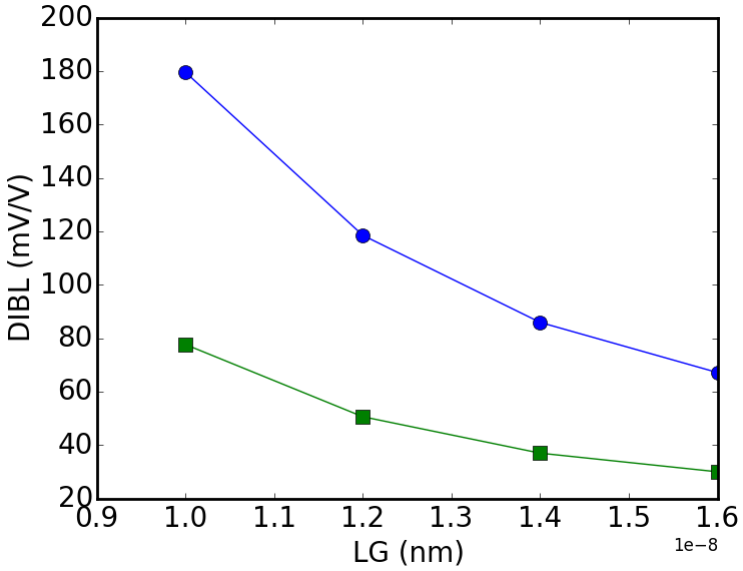

Figure 7.10. DIBL for FinFETs (blue circles) and NC-FinFETs (green squares) for different technology nodes ("10/9", "8/7", "6/5", and "4/3" nodes) with physical $L_G = 16nm, 14nm, 12nm, 10nm$. $t_{FE} = 3nm$, $P_R = 15\mu C/cm^2$ and $E_C = 1.4MV/cm$. $V_{DD} = 1.05V$.

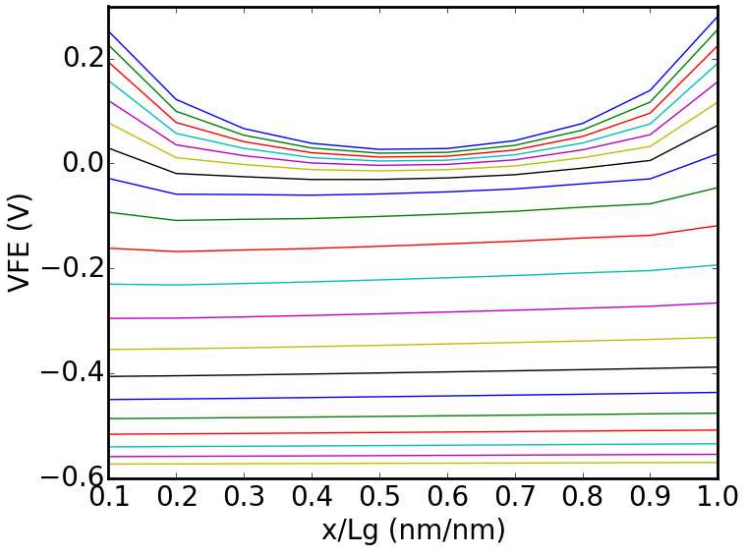

Figure 7.11. Ferroelectric voltage (V_{FE}) of a NC-FinFET for different gate voltages ($V_G = 0$ to $1V$) with $L_G = 16nm$. $t_{FE} = 3nm$, $P_R = 15\mu C/cm^2$ and $E_C = 1.4MV/cm$. $V_{DD} = 0.05V$. Top curve represents lowest V_G value.

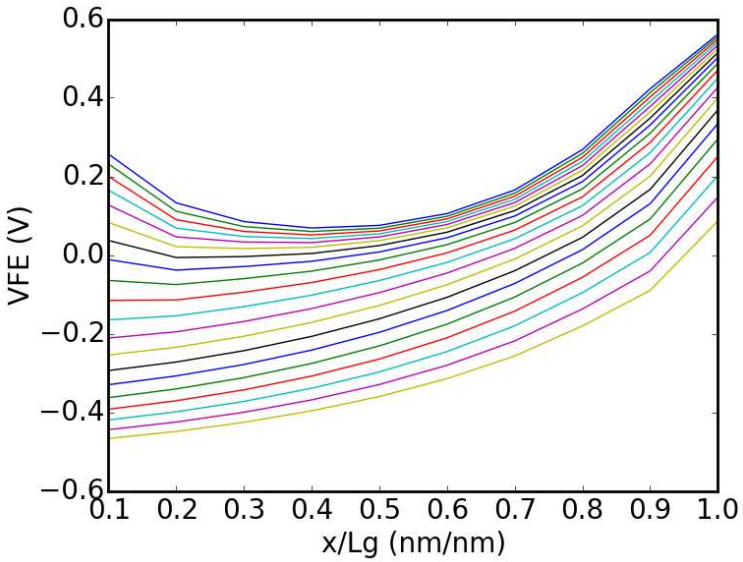

Figure 7.12. Ferroelectric voltage (V_{FE}) of a NC-FinFET for different gate voltages ($V_G = 0$ to $1V$) with $L_G = 16nm$. $t_{FE} = 3nm$, $P_R = 15\mu C/cm^2$ and $E_C = 1.4MV/cm$. $V_{DD} = 1.05V$. Top curve represents lowest V_G value.

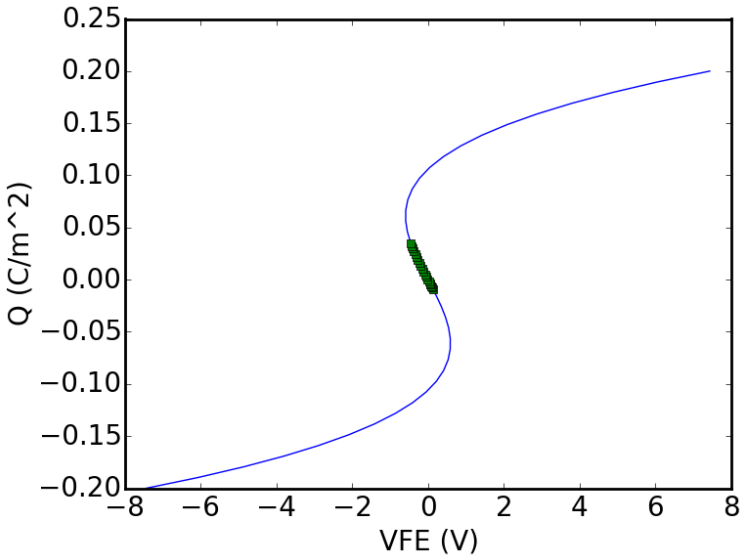

Figure 7.13. Charge versus Ferroelectric voltage (V_{FE}) at source side of a NC-FinFET for different gate voltages ($V_G = 0$ to $1V$) with $L_G = 16nm$. Symbols are ferroelectric charge from simulation and lines from Landau-Khalatnikov model.

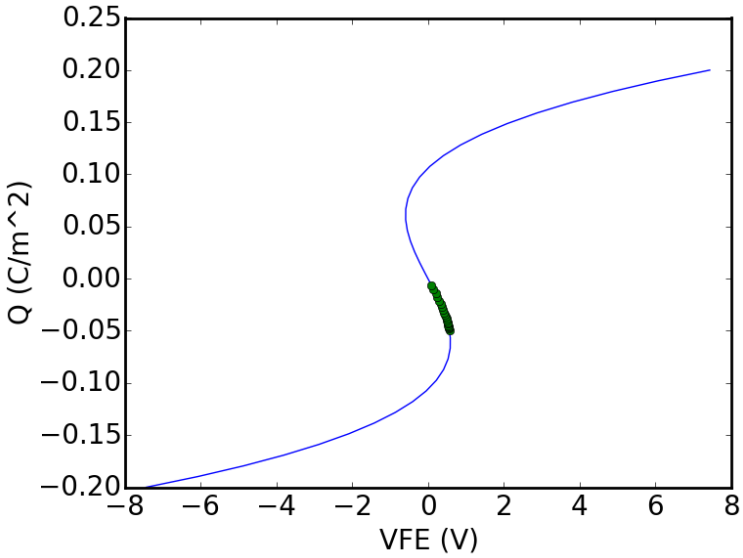

Figure 7.14. Charge versus Ferroelectric voltage (V_{FE}) at drain side of a NC-FinFET for different gate voltages ($V_G = 0$ to $1V$) with $L_G = 16nm$. Symbols are ferroelectric charge from simulation and lines from Landau-Khalatnikov model.

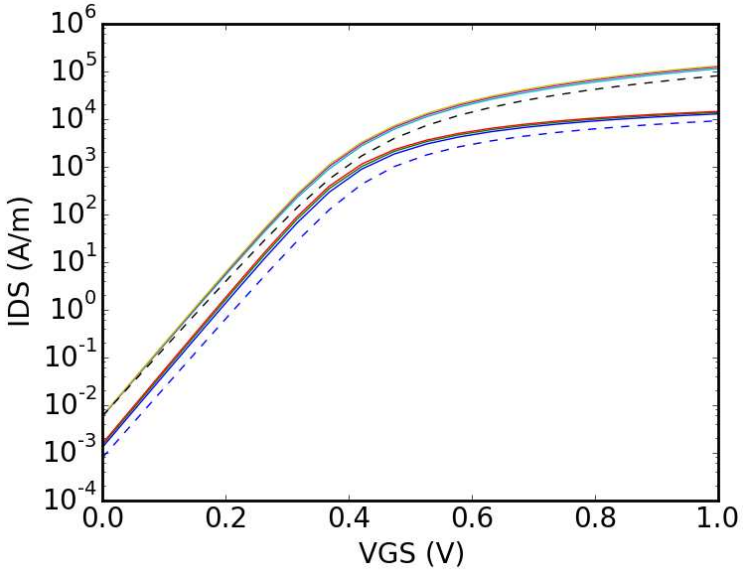

Figure 7.15. Drain current characteristics of a base-line FinFET (dash lines) with EOT=0.8nm, 0.5nm interfacial layer and 1.5nm high-k material, and NC-FinFETs (lines) with different FE thickness $T_{FE} = 0, 3nm, 5nm$ and interfacial layer of 0.5nm. $V_{DD} = 0.05, 1.05V$.

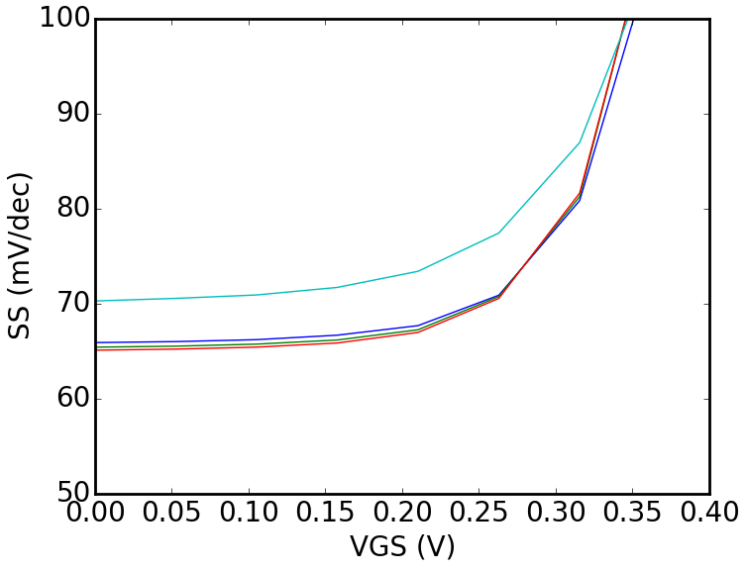

Figure 7.16. Subthreshold swing characteristics of a base-line FinFET (top line) with EOT=0.8nm, 0.5nm interfacial layer and 1.5nm high-k material, and NC-FinFETs (lower lines) with different FE thickness $T_{FE} = 0, 3nm, 5nm$ and interfacial layer of 0.5nm. $V_{DD} = 1.05V$.

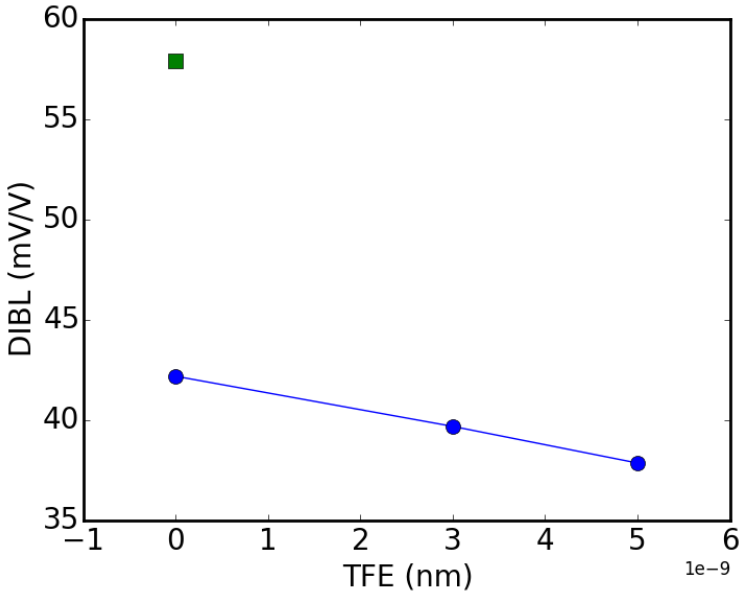

Figure 7.17. DIBL of a base-line FinFET (greem square) with EOT=0.8nm, 0.5nm interfacial layer and 1.5nm high-k material, and NC-FinFETs (blue circles) with different FE thickness $T_{FE} = 0, 3nm, 5nm$ and interfacial layer of 0.5nm. $V_{DD} = 1.05V$.

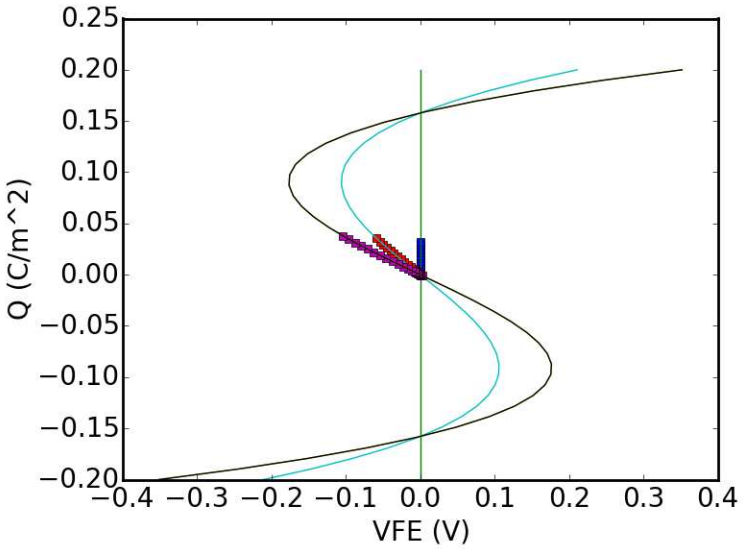

Figure 7.18. Charge versus Ferroelectric voltage (V_{FE}) at source side of a NC-FinFET for different gate voltages ($V_G = 0$ to $1V$) and $T_{FE} = 0, 3nm, 5nm$. Symbols are ferroelectric charge from simulation and lines from Landau-Khalatnikov model. $V_{DD} = 1.05V$.

Chapter 8

Energy Analysis of Negative Capacitance FETs

8.1 Introduction

This chapter presents the quasi-adiabatic energy characteristic of Negative Capacitance (NC) FinFETs [80]. For the last few decades researchers have been talking about adiabatic IC systems using device and circuit approaches such as energy recovery logic or CMOS adiabatic circuits [89, 85]. However, these approaches face many challenges due requirements of high-Q inductors, overall circuit area increases, design complexity is higher, special power supplies are required, or circuit speed reduces. Therefore, there has been no commercial implementation of adiabatic circuits for VLSI systems. The difficulty of implementing an adiabatic IC system relies on the charge and discharge mechanism of CMOS technology, which wastefully dissipate energy as heat, mostly when switching. In standard CMOS technology, in order to bias a transistor at a given gate voltage V_{cc}, a specific amount of charge $Q_{G,V_{cc}}$, need to be put on the gate capacitor. The gate capacitor stores this energy, which is later drained when the transistor returns to its original bias state. The drained energy is converted to heat and wasted in the process. Theoretically, there is not first principle theorem that forces us to throw away energy in circuits, anywhere, but no one has found a good replacement of CMOS technology that can actually recover part of the energy while functioning.

In the following sections, it is shown that NC-FinFETs [80] devices are potential candidates to achieve quasi-adiabatic VLSI systems. NC-FinFETs have a medium integrated in the gate stack, the ferroelectric (FE) material. When an NC-FinFET is being charged, the FE material is the one that delivers an amplification of the input voltage, by providing extra charge (or energy). Then, when the transistor returns to a

previous bias state, not all of the charge (or energy) is drained but some of it is stored in the FE layer. In addition, gate voltage amplifications allows for circuits to use a lower supply voltage, producing significant overall energy reduction. The following sections shows how NC-FinFETs let to quasi-adiabatic circuit configurations. The compact model for NC-FinFET is presented in the section II. Energy simulation results for a single NC-FinFET are shown in section III. Ring oscillator simulations are presented in section IV. Finally, conclusions are presented in section V.

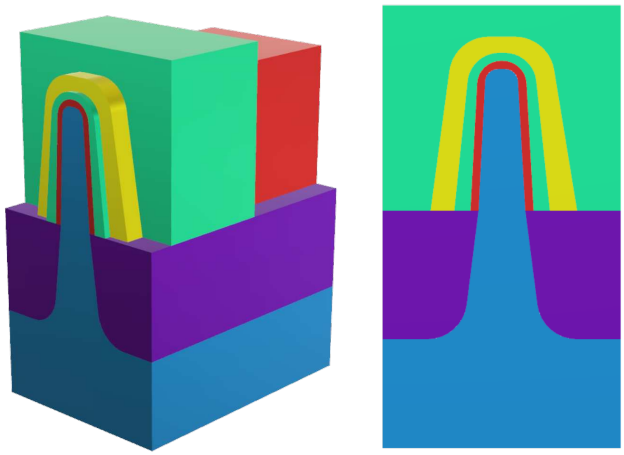

Figure 8.1. Schematic of a NC-FinFET with a lumped configuration (floating metal gate between insulator and ferroelectric layer).

8.2 SPICE Model for NCFETs

This work uses the NC-FinFET SPICE compact model presented by [41, 39, 24]. In this model, the physics of ferroelectric layers (Fig. 8.2) is modeled by Landau-Khalatnikov (L-K) equations [44]. L-K equations are solved self-consistently with three-dimensional FinFET SPICE model [41, 23]. L-K equations express the relationship between energy per unit volume (U_{pu}), the polarization ($P = Q_{FE}/A_{FE}$, Q_{FE} and A_{FE} being the charge and area of the FE layer), and the electric field (E) of a FE:

$$U_{pu} = \alpha_1 P^2 + \alpha_{11} P^4 + \alpha_{111} P^6 - PE \tag{8.1}$$

where α_1, α_{11}, and α_{111}, are material parameters such as those obtained from experimental data published in [46, 45]. Using L-K equation, the energy of the FE layer and the electric field, can be expressed using the total gate charge of the transistor (Q_G):

$$\begin{aligned} U_{FE} = \beta t_{FE} \left(\alpha_1 \left(\frac{Q_G}{\beta}\right)^2 + \alpha_{11} \left(\frac{Q_G}{\beta}\right)^4 + \alpha_{111} \left(\frac{Q_G}{\beta}\right)^6 \right) \\ -t_{FE}^2 Q_G E_{FE} \end{aligned} \tag{8.2}$$

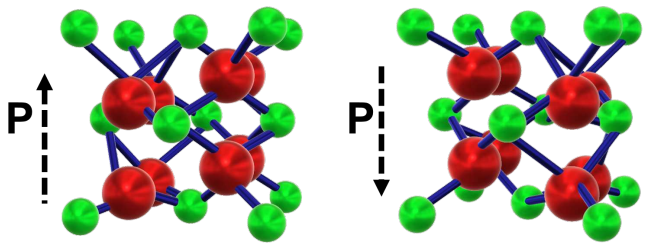

Figure 8.2. Schematic of two different polarization states of an orthorhombic phase ferroelectric, where large atoms are oxygen and small atoms are hafnium [72].

where t_{FE} is the FE thickness and $\beta = L_G W_{eff} N_{FIN}$, with L_G, W_{eff}, and N_{FIN} being the gate length, channel effective width, and number of fin, respectively. E_{FE} is the FE electric field expressed as:

$$E_{FE} = 2\alpha_1 \frac{Q_G}{\beta} + 4\alpha_{11} \left(\frac{Q_G}{\beta}\right)^3 + 6\alpha_{111} \left(\frac{Q_G}{\beta}\right)^5 \tag{8.3}$$

The FE voltage can then be obtained as $V_{FE} = t_{FE} E_{FE}$. Using the L-K equations to obtain V_{FE}, the FE model is self-consistently coupled to the FinFET BSIM model by calculating the internal gate voltage using $V_{G,internal} = V_G - V_{FE}$ [41, 39, 24]. The base-line transistor used in this study is the high performance 14 nm FinFET [36] which is modeled by the industry standard compact model BSIM-CMG [23]. Therefore, a BSIM-CMG model similar to that extracted for 14nm ULP devices is used in conjunction with a ferroelectric model to simulate NC-FinFETs at 14 nm node technology (Fig. 8.3).

8.3 Single NC-FinFET Energy Simulation Analysis

Fig. 8.7 shows a diagram of the configuration used to simulate a single NC-FinFET and calculate energy flows. Input voltage is ramped from 0V to 0.45V, keeping V_{DD} =0.45V. First, a NC-FinFET without parasitic capacitance is being considered. At each cycle, the applied voltage makes the internal gate voltage to sweep from 0V to a maximum of ∼0.5V (Fig. 8.5), and later gets back to its initial state of 0V. The amplification take places mainly in the on-state region, where the voltage gain, given by $|C_{FE}|/(|C_{FE}| - C_{FinFET})$[32], is significant because C_{FinFET} is comparable to $-C_{FE}$. Details on energy calculations and simulation set-up are presented in Appendix E. The FE layer delivers 0.08 aJ to induce a voltage amplification at each cycle, energy that is recovered when the FE come backs to its initial bias state, i.e., part of the energy drained by the transistor is recovered by the FE

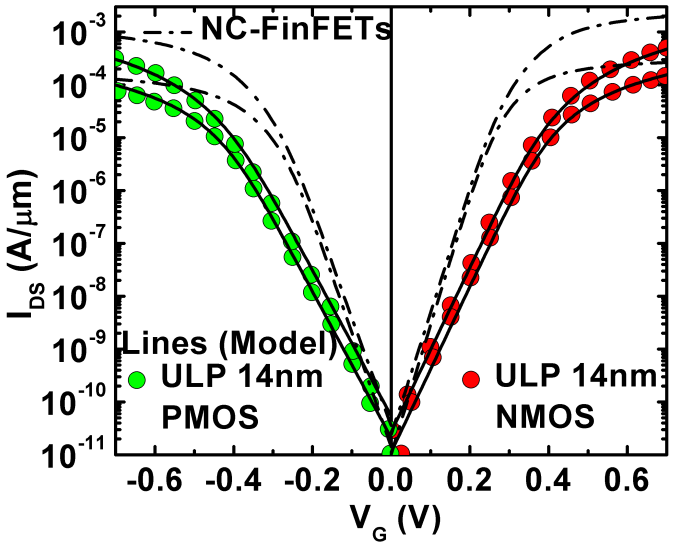

Figure 8.3. Drain current versus V_{GS} for nmos and pmos base-line 14nm ULP FinFET [36], and NC-FinFETs with parasitic capacitance. $\alpha_1 = -3 \times 10^9 m/F$, $\alpha_{11} = 6 \times 10^{11} C^2 m^5/F$, and $\alpha_{111} = 0$.

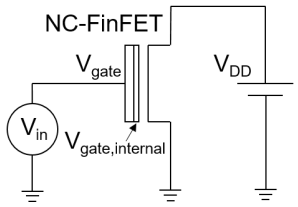

Figure 8.4. Single NC-FinFET set-up simulation.

layer (Fig. 8.6). This basic mechanism produces a quasi-adiabatic system, where part of the energy needed to bias the transistor at a given voltage is later recovered while it goes to the initial bias state. S single NC-FinFET, with parasitic capacitances, is also used to calculate energy flows. Input voltage is ramped from 0V to 0.45V, and V_{DD} =0.45V and 0.01V are considered. When V_{DD} =0.45V, there is a gate voltage amplification in the on-state (∼0.7V) and off-state (-0.1V) as well (Fig. 8.8). The amplification take places mainly in the on- and off-state regions, where the voltage gain, given by $|C_{FE}|/(|C_{FE}| - C_{FinFET})$[32], is significant because C_{FinFET} is comparable to $-C_{FE}$. The parasitic capacitance plays a key role in the gate voltage amplification at each bias condition [39], they can come, for example, from fringing or channel overlap capacitances. Indeed, they are important on reducing subthreshold swing and increasing on-state current by helping matching C_{FinFET} with $-C_{FE}$.

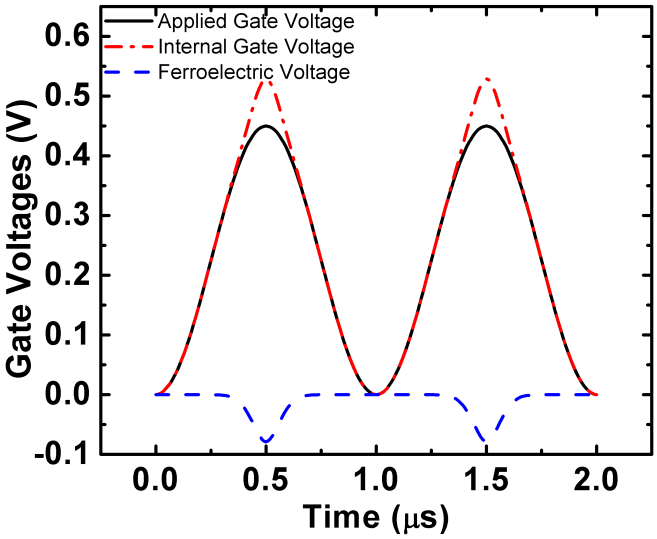

Figure 8.5. Applied gate voltage, internal gate voltage, and ferroelectric voltage for a nmos NC-FinFET without parasitic capacitance at $V_{DD} = 0.45V$.

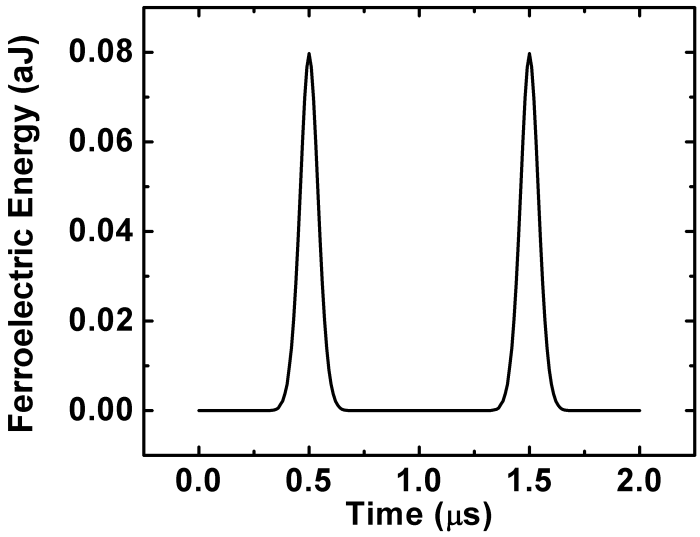

Figure 8.6. Energy delivered by the FE layer as a function of time.

When $V_{GS} \simeq$0V and V_{DD} =0.45V, there is still a large amount of charge at the drain side, charge that couples with the FE layer to produce a net gate voltage amplifi-

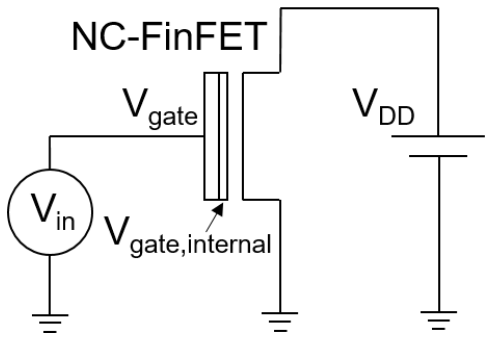

Figure 8.7. Single NC-FinFET set-up simulation.

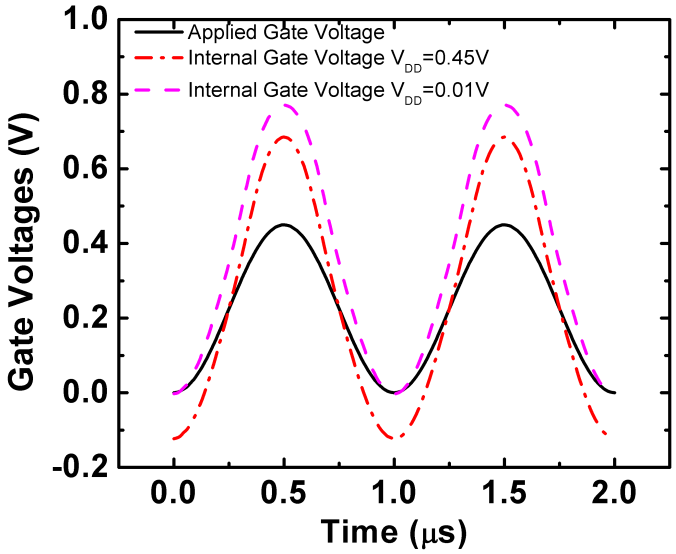

Figure 8.8. Applied gate voltage and internal gate voltage for nmos NC-FinFET with parasitic capacitance at $V_{DD} = 0.45V$ and $V_{DD} = 0.01V$.

cation effect. On the other hand, when $V_{GS} \simeq$0V and V_{DD} =0.01V, the charge at the drain side is small and voltage amplification ($\sim$0.8V) mainly occurs only at the on-state condition (Fig. 8.8). This contrast is also reflected in dependence of energy shape on V_{DD} (Fig. 8.9). When V_{DD} =0.45V, the FE layer delivers energy at the on and off state conditions, due the voltage amplification at both bias states. Energy that is recovered when transistor is switch between on/off states. However, when V_{DD} =0.01V, the FE requires energy only in the on state and then it recovers it while transistor is set back to off state. This basic mechanism produces a quasi-adiabatic system, where part of the energy needed to bias the transistor at a given voltage is later recovered while it goes to a lower energy bias state.

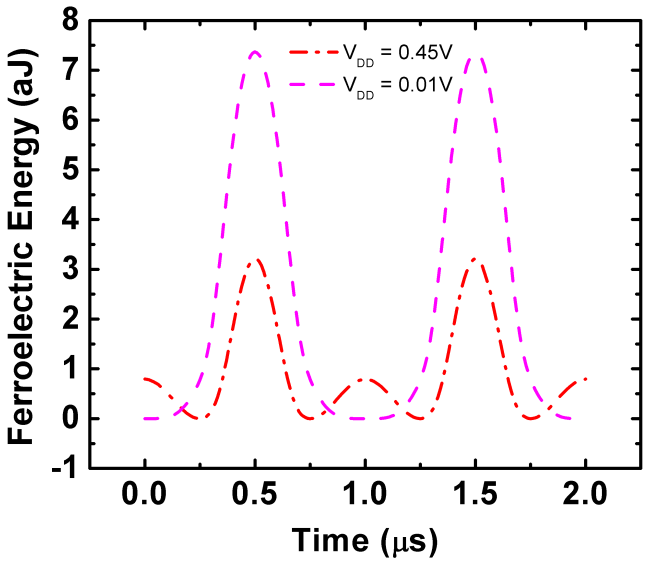

Figure 8.9. Energy used by the FE layer as a function of time for $V_{DD} = 0.45V$ and $V_{DD} = 0.01V$.

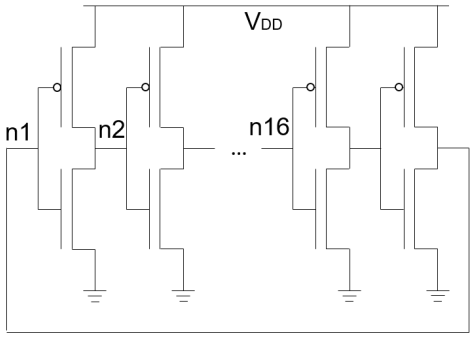

Figure 8.10. 17-stage Ring-Oscillator set-up. 11 and 10 Fins are used for pmos a nmos, respectively.

8.4 NC-FinFET Ring-Oscillator Analysis

Ring-Oscillators (ROs) are widely use to evaluate, validate, and monitor performance of a given technology. Indeed, the frequency of ROs provides indications of technology speed and can be measured in the early stages of production. A 17-stage RO is utilized in this work (Fig. 8.10). First, a RO without interconnection load capacitances is considered; i.e., only intrinsic switching characteristics are analysed. Fig. 8.11 shows a comparison of the voltages at the first node of the RO under study utilizing base-line ULP 14nm FinFETs versus NC-FinFETs. V_{DD} has been

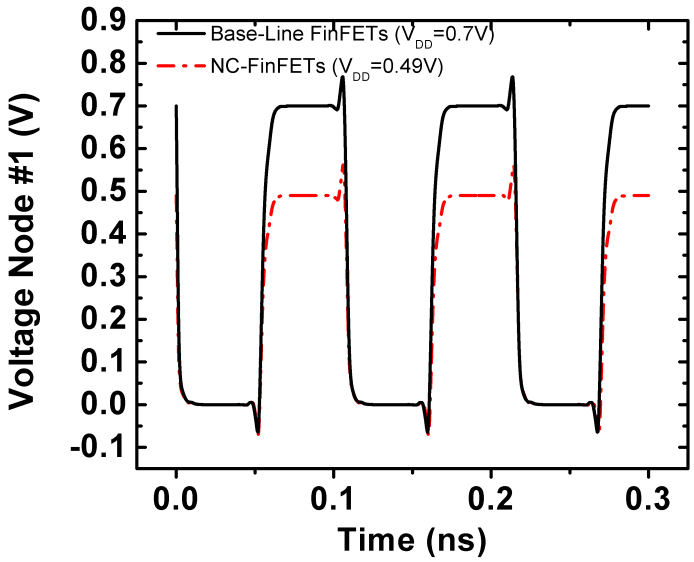

Figure 8.11. Voltages at the first node of a 17-stage ring oscillator utilizing base-line ULP 14nm FinFETs versus NC-FinFETs.

set to 0.7V and 0.49V, respectively. Although both technologies use different V_{DD}, they both match the technology speed, this is the result of the voltage amplification provided from the FE films in NC-FinFETs (Fig. 8.12) which translates to a larger effective gate to source voltage (V_{GS}) for each transistor (Fig. 8.13). In order to get the same speed for both ROs, V_{GS} effective for the NC-FinFET RO has to be larger than the base-line one (0.8V vs. 0.7V), because V_{DD} is lower for the NC-RO and also because the total capacitance is increased for the NC-RO. The energy needed for the voltage amplification at each cycle is provided by the FE layers (Fig. 8.14). In every cycle, pmos and nmos deliver approximately 0.1fJ that are later recovered by the FE layers and re-utilized at later cycles, in a similar manner as explained in section III. This is the key mechanism that allows voltage amplification and energy reduction, making possible the implementation of quasi-adiabatic ROs where not all of the charging/discharging energy is dissipated as heat but part of it is recycled by FE layers. For each inverter, 0.2fJ (19%) per cycle is saved by using NC-FinFETs (Fig. 8.15), which corresponds to the energy delivered by the FE in the NC-FinFET nmos and pmos together as shown in Fig. 8.14. This translates to a 19% total energy reduction for NC-FinFETs compared to the base-line FinFET based RO used in this study (Fig. 8.16).

The second RO configuration in this study is a 17-Stage RO which includes a load capacitance at each connection node between inverters. This load capacitance represent interconnection/wiring capacitances; therefore, it is a more realistic way

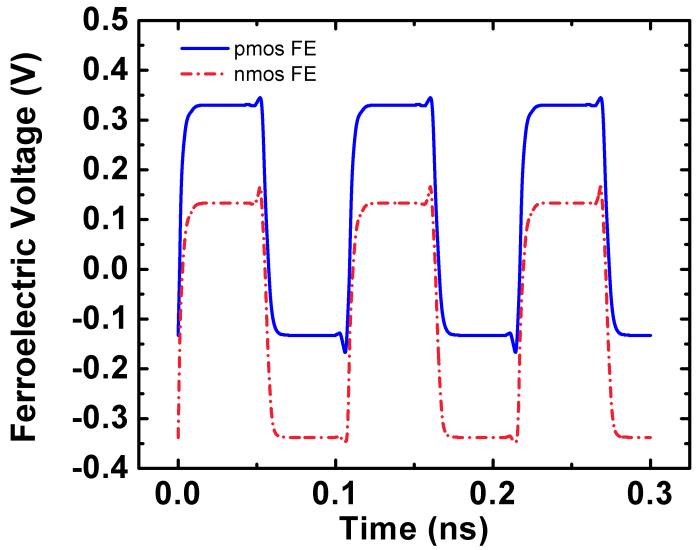

Figure 8.12. FE voltage as a function of time for nmos and pmos NC-FinFETs at the first stage of the RO under study.

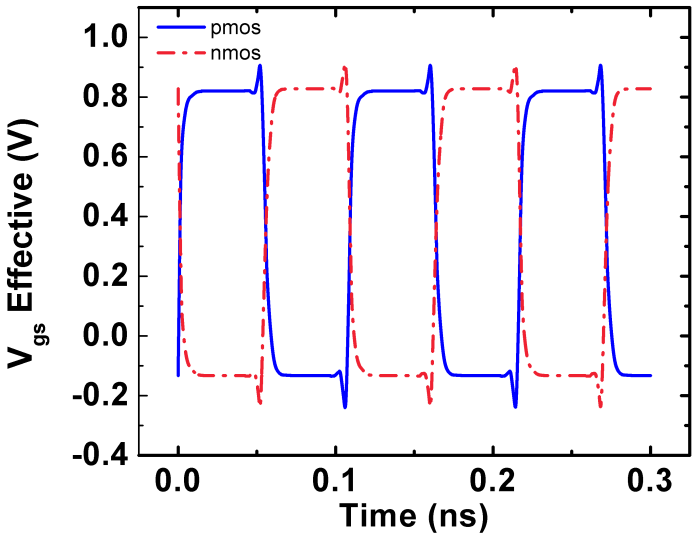

Figure 8.13. Effective gate to source voltage for nmos and pmos NC-FinFETs at the first stage of the RO under study.

of characterizing energy behaivor for NC-FinFET based circuits. Fig. 8.17 shows

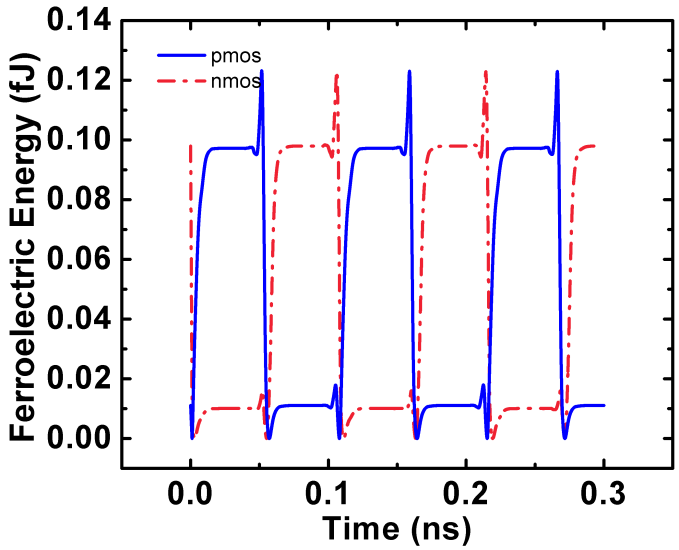

Figure 8.14. Energy deliver by each FE layer as a function of time. 0.1fJ is delivered by each nmos and pmos, energy that is later recover by the FE layers.

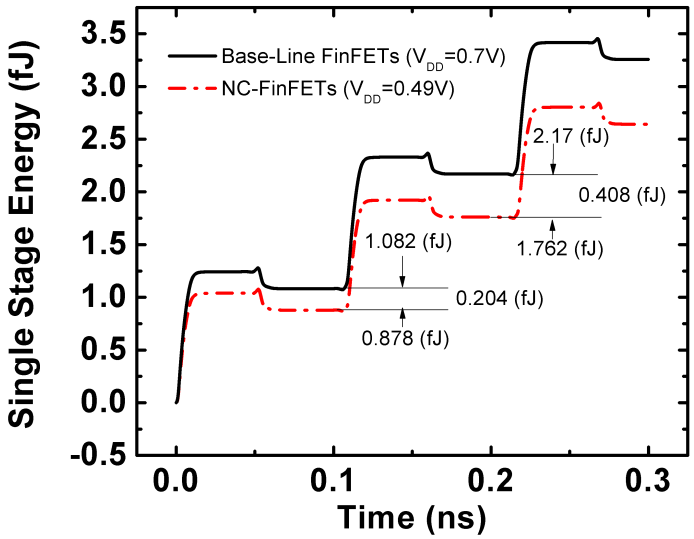

Figure 8.15. Energy as a function of time used by a single stage of the RO.

the RO period under different load capacitances. V_{DD} is constant for the base-line FinFETs and tuned for the NC-FinFET ROs; thus, speed is matched at each load

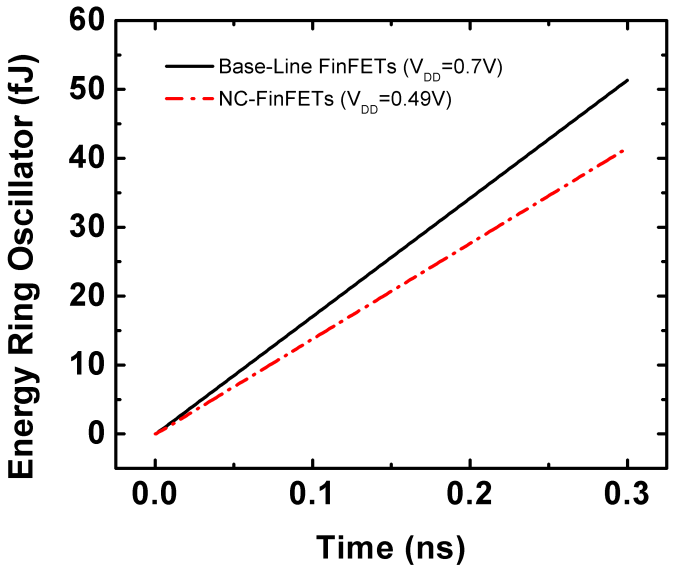

Figure 8.16. Total energy as a function of time used by the 17-stage ROs using base-line FinFETs and NC-FinFETs. The later saves 19% of energy at equal RO speed.

capacitance. As load capacitance become more dominant, V_{DD} can be further scaled for NC-FinFET technology. Indeed, energy reduction is increased as load capacitance become more significant (Fig. 8.18). These results can be understood using a simple equation for the inverter energy per cycle [77]:

$$E_{inv} = E_{dyn} + E_{dp} + E_{stat} \simeq C_L V_{DD}^2 + V_{DD} I_p t_s + V_{DD} I_l t_c \tag{8.4}$$

where E_{dyn}, E_{dp}, E_{stat} are the dynamic, direct-path, and leakage energy consumptions, respectively. C_L is the total loading capacitance for each inverter, I_p the peak current during direct path switching [77], t_s is the time during short circuit, I_l is the leakage current, and t_c is the cycle time. For NC-FinFET inverters, C_L is composed of three components: parasitic/intrinsic FinFET capacitances, interconnection capacitances, and FE capacitance. For the unloaded RO case, C_L is mainly composed by the transistor capacitances and the FE capacitance; therefore, energy reduction is not proportional to V_{DD}^2 due the extra FE capacitance (19% energy reduction). However, as C_L increases, FE capacitance becomes less significant and energy reduction is approximately proportional to V_{DD}^2, as shown in Fig. 8.18 (58% energy reduction for large capacitance load). Note that if FE does not recover the energy utilized in the quasi-adiabatic process, there is still a significant energy reduction as C_L increases.

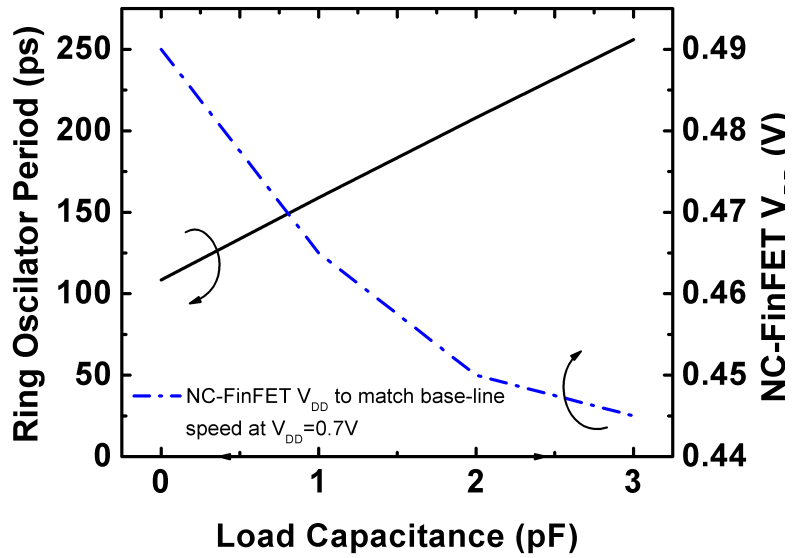

Figure 8.17. Ring oscillator period (left axis) and V_{DD} (right axis) versus load capacitance per node for base-line and NC-FinFETs.

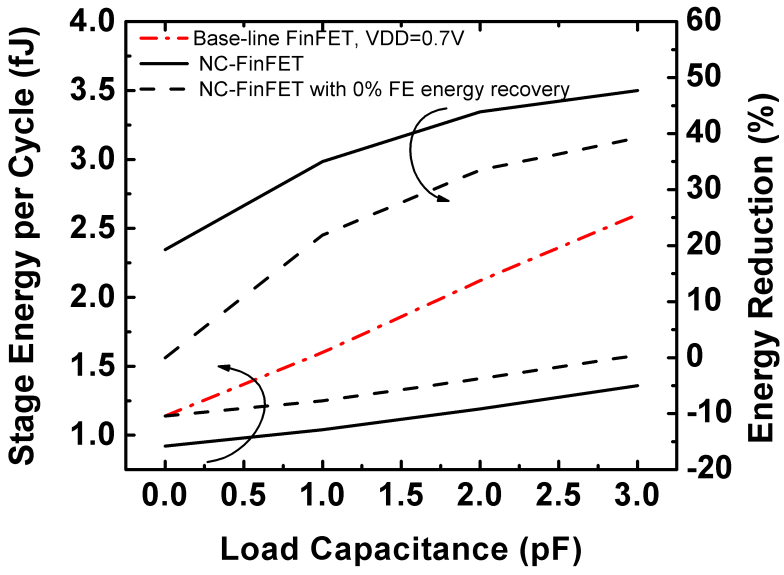

Figure 8.18. Stage energy per cycle (left axis) and energy reduction (right axis) versus load capacitance per node for base-line and NC-FinFETs.

8.5 Conclusion

This work uses an accurate spice compact model to simulate and analyse energy reduction of NC-FinFET based circuits. A quasi-adiabatic mechanism of the

ferroelectric layer in the NC-FinFET recovers part of the energy during the switching process of transistors, helping minimizing the energy losses of the wasteful energy dissipation nature of conventional transistor circuits. As load capacitances further increase, V_{DD} scaling becomes more dominant. This is the case of scaled transistor technologies where interconnect/wire capacitance become dominant. In the example provided in this work, a 58% energy reduction is achieved for the ring oscillator with largest load capacitance.

Chapter 9

Summary

9.1 Chapters Summary

Chapter 2 presented an explicit surface potential model for the industry standard compact model of FinFETs, BSIM-CMG. The compact model version where this model was implemented is BSIM-CMG108. The explicit model was derived by obtaining a continuous first approximate of the implicit surface potential model. The solution was then improved by two quartic modified iterations. The proposed model has been tested under a large range of device geometry, doping, gate oxide thickness, temperature, and bias conditions, and it exhibits excellent accuracy and robustness. The delatiled calculation of this model has been presented in Appendix B.

A new compact model introduced into the industry standard compact model BSIM-CMG was explained in Chapter 3. The core model of BSIM-CMG was updated with a new unified FinFET model, which calculates charges and currents of transistors with complex fin cross-sections. In addition, threshold voltage modulation from bulk-bias effects and bias dependent quantum mechanical confinement effects were incorporated into the new core model. Short channel effects, affecting threshold voltage and subhtreshold swing, were modeled with a new unified field penetration length, enabling accurate modeling of sub 14nm node FinFETs. The new proposed models further assure the BSIM-CMG model's capabilities for circuit design using FinFET transistors for advanced technology nodes such as Gate-All-Around FETs or FETs with III-V channel materials.

Using the model presented in Chapter 3, Chapter 4 established a methodology of modeling FinFET's variability. The new Unified Model was able to predict the effects of complex and subtle fin variations. TCAD simulation results of 14nm node FinFETs with seven sources of variability, such as gate and fin edge roughness and random dopant fluctuation, were accurately matched with the new unified compact

model using only shape variation parameters. Due to the physical foundation of the unified model, it can predictively model the performance variability of future FinFET technology nodes using expected shape variations.

Compact models for UTBSOIs are presented in Chapter 5. It developed a new analytical form of the core model for the industry standard compact model BSIM-IMG, a fully-featured turn-key compact model for independent multi-gate MOSFETs. An explicit model was derived by obtaining a continuous first approximate of the implicit surface potential model. This solution was then improved by three first order iterations, leading to a numerically robust, accurate, and fast core model. This new core model includes back-side inversion. To represent real device effects, several extra models were later incorporated such as drain-induced barrier lowering, velocity saturation, short-channel effects, self-heating effect, mobility-field dependence, substrate-depletion effect, etc.

Negative Capacitance FETs are studied from Chapter 6. Chapter 6 first presented insights into the device physics and behaviors of ferroelectric based negative capacitance FinFETs using lumped and distributed compact models for its simulation. For NC-FinFETs having a floating metal between ferroelectric (FE) and the dielectric layers, lumped charge model were used. For NC-FinFETs without a floating metal, a distributed charge model was used, where at each point in the channel the ferroelectric layer impacts the local channel charge. This distributed effect have shown important implications on device characteristics. The proposed compact models have been implemented in circuit simulators for exploring circuits based on NC-FinFET technology.

Numerical simulations of NC-FETs were developed in Chapter 7. A self-consistence framework of 2D simulation of transistors with a 1D ferroelectric formulation was proposed. Different effective polarization across the channel was captured by the numerical simulations. Simulation were used to compare base-line FinFET against NC-FinFETs. It results showed how NC-FinFETs can help scaling of transistors to under 5nm node. For the case of FE with small E_c, the FE layer help to reduce the effective EOT which also helps on device scaling.

The last part of this thesis, Chapter 8, presented a detailed analysis, from an energy perspective, of the gate voltage amplification of NC-FinFETs. The models presented in Chapter 6 were used for this study. Results explained how the ferroelectric layer in transistors use a quasi-adiabatic mechanism to recover the energy needed for gate voltage amplification. This voltage amplification leads to energy reduction by supply voltage scaling, which becomes the main energy reduction factor for circuits loaded with parasitic capacitances as those found in scaled technologies.

9.2 Future Work

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Appendix A

1D Numerical Simulation of Symmetric FinFET

A 1D Poisson's solution for cross sectional section of a FinFET [34] device is implemented using Matlab. The Poisson's equation is expressed as:

$$\frac{\partial^2 \psi\left(x\right)}{\partial x^2} = \frac{q}{\varepsilon_{\mathrm{ch}}}\left(\frac{n_i^2}{N_{\mathrm{ch}}} e^{\frac{\psi(x)}{V_{\mathrm{tm}}}} + N_{\mathrm{ch}}\right) \tag{A.1}$$

Using $x_j = j/(n+1)$ for $j = 0, 1, ..., n+1$ as a set of mesh points. One approximation of the second derivative of ψ at a point x_j in the channel can be obtained using finite difference method:

$$\frac{\partial^2 \psi\left(x\right)}{\partial x^2} \approx \frac{\psi(x_{j-1}) - 2\psi(x_j) + \psi(x_{j+1})}{h^2} \tag{A.2}$$

where $h = 1/(n+1)$ is the mesh distance between each point. Using this approximation the Poisson equation can be solve with the finite-difference technique. In the case of a symmetric FinFET, we have two boundaries conditions. The first one at the middle of the channel, where we know that the derivative of the potential is equal to zero (due device symmetry). This constitutes a Neumann boundary condition given by:

$$\frac{\partial \psi\left(x\right)}{\partial x} = 0 \tag{A.3}$$

Using finite difference method, this translates to:

$$\frac{\psi(x_1) - \psi(x_0)}{h} = 0 \tag{A.4}$$

The second boundary condition is at the semiconductor-insulator interface where Gauss's law must be fulfilled, i.e., displacement vector must be constant at the interface (Dirichlet's boundary condition):

$$\varepsilon_{\mathrm{ch}} E_{ch,interface} = \varepsilon_{\mathrm{ox}} E_{ox} \tag{A.5}$$

Assuming there is not charge at the insulator oxide, E_{ox} can be obtained as:

$$E_{ox} = \frac{V_G - V_{FB} - \psi(x_{n+1})}{t_{ox}} \tag{A.6}$$

Using the boundary conditions and the Poisson's equation approximated by finite difference method, the problem can be solved using a matrix equation given in the for of $T\psi = h^2 f$, where T and f are given by:

$$T = \begin{bmatrix} 2 & 1 & & & & \\ -1 & 2 & 1 & & & \\ & \ddots & \ddots & \ddots & & \\ & & -1 & 2 & -1 & \\ & & & & -1 & 2 \end{bmatrix} \tag{A.7}$$

$$f = \begin{bmatrix} \psi(x_1) \\ r(\psi(x_2)) \\ \vdots \\ r(\psi(x_n)) \\ BC(\psi(x_n), \psi(x_{n+1})) \end{bmatrix} \tag{A.8}$$

where $r(\psi)$ and $BC(\psi_1, \psi_2)$ are defined as:

$$r(\psi) = \frac{q n_i^2 h^2}{\varepsilon_{ch} N_{ch}} \exp(\psi / v_T) + \frac{q h^2}{\varepsilon_{ch}} N_{ch} \tag{A.9}$$

$$BC(\psi_1, \psi_2) = h\varepsilon_{\text{ox}} \frac{V_G - V_{FB} - \psi_2}{\varepsilon_{\text{ch}} t_{ox}} + \psi_1 \tag{A.10}$$

The system can be solved using Newton's method. In this case, since the system is multidimensional, the Jacobian of the vector f need to be calculated. In the below code, the Jacobian is obtained using an automatic differentiation technique [5]. The below code in octave shows the implementation, note that the code from automatic differentiation technique [5] must be downloaded and save it in the same folder that the code presented here.

Listing A.1. Octave code for 1D Symmetric FinFET Poisson's Equation

```
clear all; close all;
%%%%%%%%%%%%%%%parameters%%%%%%%%%%%%%%%
q    = 1.602190e-19; k    = 1.380650e-23; T    = 300;  eo   =
    8.854000e-14 ; eins   = 3.453060e-13 ; ech  = 1.035918e-12
    ; Eg   = 1.169640 ; Nc   = 2.540000e+19 ; Nv   = 3.140000e
    +19 ; vt   = 0.0259; ni  = 1e11; Nch   = 4e18; tins  = 1e
    -7; TFIN  = 20e-7; phi_substrate = 4.05;  phi_gate = 4.3;
Vfb     = phi_gate - phi_substrate -Eg/2-vt*log(Nch/ni);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
N    = 50;
xa   = 0;
xb   = TFIN/2;
h    = (xb-xa)/(N-1);
%%%%A definition%%%%%
e=ones(N,1);
A=spdiags([e,-2*e,e],(-1:1),N,N);
A(1,:)=zeros(1,N); A(1,1)=1;
A(N,:)=zeros(1,N); A(N,N)=1;
%%%%%%%%%%%%%%%%%%%%%
rho0     = (1./vt)*h^2*(q/ech)*(ni^2/Nch);
rhofix   = (1./vt)*(q/ech)*Nch;
r = (1./vt)*eins *h./(ech*tins);
f1       = @(u,Vg)(u(2));
fend   = @(u,Vg)(r*(Vg-Vfb-u(end).*vt)+u(end-1));%(rhofix*(TFIN
    /2)^2/2);
f    = @(u,Vg)([f1(u,Vg);mtimes(exp(u(2:end-1)),rho0)+h^2*
    rhofix;fend(u,Vg)]);
%%%%%%%%%%%%%%%%%%%%%
Vg   = 1;
u    = (0:(rhofix*(TFIN/2)^2/2)/(N-1):rhofix*(TFIN/2)^2/2)';
x    = xa:h:xb;
Vgi  = 0;
Vgf  = 1;
Vgpoints = 10;
for j = 1:Vgpoints
  Vg = (j-1)*(Vgf-Vgi)/(Vgpoints-1)+Vgi;
  uvec   = myAD(u);
  fvec   = f(uvec,Vg);
  fval = getvalue(fvec);
  fdval = getderivs(fvec);
  g = A*u-fval;
  i=1;
  while(abs(sum(g))>1e-8)
  dg = A-fdval;
  u = u- dg \ g;
  uvec   = myAD(u);
  fvec   = f(uvec,Vg);
  fval = getvalue(fvec);
  fdval = getderivs(fvec);
  g = A*u-fval;
  i=i+1;
  end
```

```
47    u_all(:,j) = u;
48 end
```

Appendix B

Explicit Surface Potential Model

The surface potential model use in BSIM-CMG was initially derived in an implicit form in chapter 2, which relies on numerical calculations to be solved, such as Newton-Raphson method [76, 81]. Newton-Raphson method is an iterative algorithm that start from an initial guess to then keep refining it until the method arrives to a final solution. This refinement is done by approximating the function to be solved at the given guess by a linear system which is then used to obtain the new guess for the solution [79]. Although Newton-Raphson method could potentially have a rapid convergence (e.g. quadratic [81, 79]), its convergence is no guarantee. Indeed, it could potentially fail by, for example, getting into an infinite loop. This is not practical for compact models, where convergence and speed are key requirements. However, by making sure that the initial guess is close enough to the final solution and that the solution is not singular, i.e. the derivative of the function is non zero at the solution, it could be assured that the Newton-Raphson method will converge [81]. Therefore, in order to implement the model proposed in section 2 in a circuit simulator, a good initial guess formula, so called continuous starting function (CSF) [90], for equation (2.11) is presented in this section. In addition, Newton-Raphson method could be replaced for a higher order method such as the quartic modified iteration [81]. The main difference between quartic modified and Newton-Raphson iterations is that the first refine the initial guess by approximating the function to be solved using a high order approximation, instead of the linear one used in Newton-Raphson iteration. Therefore, quartic modified iteration could give a faster convergence rate which would reduce the iterations needed to solve equation (2.11), making the proposed compact model fast.

B.1 Continuous Starting Function

A initial guess for equation (2.11) has been already proposed in [28]. It was derived by considering the asymptotic behaviour of β in equation (2.11) under the

two main regimes of operation: subthreshold regime and strong inversion regime. Although the initial guess proposed in [28] works well for most conditions, it has few important issues that must be solved. First, it is not a single continuous and smooth starting function because it was constructed by taken the minimum between two different functions. The lack of smoothness implies a higher number of iterations needed to arrive to a final solution. The second issue is that the initial guess does not work very well for devices with highly doped or wide channels, where β can get values as low as 1×10^{-15}. This makes the model unstable depending on device geometry and bias conditions. This a critical point, especially when a compact model is used for circuit-device optimization where the optimization algorithm could bring the evaluation of the model to extreme conditions. Due the mentioned issues, in this section a new CSF is proposed to solve equation (2.11). In a similar manner as the initial guess proposed in [28], the new CSF will be obtained by considering the asymptotic behaviour of equation (2.11); however, highly doped condition will be considered first to later update the derived CSF to lightly doped channels.

In the case of FinFET device with a highly doped channel, ψ_{pert} is large and β tends to 0, which makes $\cos(\beta)$ to tend to one and $\ln(\cos(\beta))$ to zero. Using these assumptions and neglecting $\ln\beta$ term which is close to be constant in the strong inversion condition, a β function for highly doped channel FinFETs can be obtained in the strong inversion by solving equation (2.11) for the β^2 term inside the square root:

$$\beta_{SI} = e^{\frac{-\psi_{pert}}{2V_{tm}}} \frac{A_{g0}}{r} \sqrt{\left(\frac{F - F_{th,SI}}{A_{g0}} + 1\right)^2 - 1} \tag{B.1}$$

where A_{g0}, r, F and $F_{th,SI}$ are defined as follows:

$$A_{g0} = \frac{r\psi_{pert}}{V_{tm}} \tag{B.2}$$

$$r = \frac{2\epsilon_{si} t_{ox}}{\epsilon_{ox} T_{FIN}} \tag{B.3}$$

$$F = \frac{V_G - V_{FB} - V_{CH} - \psi_{pert}}{2V_{tm}} + \ln\left(\frac{T_{FIN}}{2}\sqrt{\frac{qn_i^2}{2\epsilon_{si} N_{ch} V_{tm}}}\right) \tag{B.4}$$

$$F_{th,SI} = (2r - 1)\frac{\psi_{pert}}{2V_{tm}} \tag{B.5}$$

Equation (B.1) is only valid when $(F - F_{th,SI})/A_{g0} > -1$. In the subthreshold region β is even smaller than in the previous assumption, then β^2 can be neglected in equation (2.11). The $\ln\beta$ is not any more constant in the subthreshold region, from it, a β function for the subhtreshold can be obtained as follows [28]:

$$\beta_{ST} = e^{F-F_{th}} e^{\frac{-\psi_{pert}}{2V_{tm}}} \tag{B.6}$$

Note that equation (B.6)is a good approximation for the subthreshold region of lightly and heavily doped channels as well. Equations (B.1) and (B.6) are good approximations for β; however, a single CSF has not been constructed yet. In order to obtain a a single CSF, equation (B.1) can be modified to:

$$\beta_{doped} = e^{\frac{-\psi_{pert}}{2V_{tm}}} \frac{A_{g0}}{r} \sqrt{\left(\frac{\ln\left(1 + e^{2(F-F_{th,SI})}\right)}{2A_{g0}} + 1 \right)^2 - 1} \tag{B.7}$$

The above expression can be evaluated in all bias conditions and it tends to (B.1) when $F > F_{th}$. In the case of $F << F_{th,SI}$ equation (B.7) tends to a expression similar but not exactly equal to (B.6). In order to make (B.7) to reduce to (B.6) for $F << F_{th,SI}$, $F_{th,SI}$ can be updated by equating (B.6) and (B.6) at the subthreshold, given:

$$F_{th} = (2r-1)\frac{\psi_{pert}}{2V_{tm}} + \ln\left(\frac{\sqrt{A_{g0}}}{(2r-1)\frac{\psi_{pert}}{2V_{tm}}} \right) \tag{B.8}$$

Figures B.1 and B.2 show β obtained from equation (2.11) solved using Newton-Raphson iteration and from initial guess expressed by equation (B.7) using (B.8), as expected, the proposed guess is close to the final solution in all bias regimes for highly doped channels. In order to extend (B.7) to devices with lightly doped channels, only two majors changes are needed. First, it must be noticed that as channel doping decreases A_{g0} tends to zero, this would give invalid results. Therefore, analysing the asymptotic behaviour of equation (2.11) it can be noticed that, as doping decreases, a valid value for A_{g0} should be one, thus A_{g0} can be updated to following expression:

$$A_g = \frac{\frac{r\psi_{pert}}{V_{tm}}}{1 - e^{\frac{-r\psi_{pert}}{V_{tm}}}} \tag{B.9}$$

The second change that must be done is to limit the value of β obtained from (B.7) to $\pi/2$. This limit is obtained analysing the behaviour of (2.11) in strong inversion for lightly doped devices as also explained in [28]. Therefore, the final CSF proposed here is given as follows:

$$\beta_0 = \frac{1}{\frac{1}{\beta_{doped}} + \frac{2}{\pi}} \tag{B.10}$$

where β_0 is obtained from equation (B.7) using F_{th} and A_g from equations (B.8) and (B.9), respectively. Figures B.3 and B.4 show β obtained from equation (2.11) solved using Newton-Raphson iteration and from initial guess expressed by equation

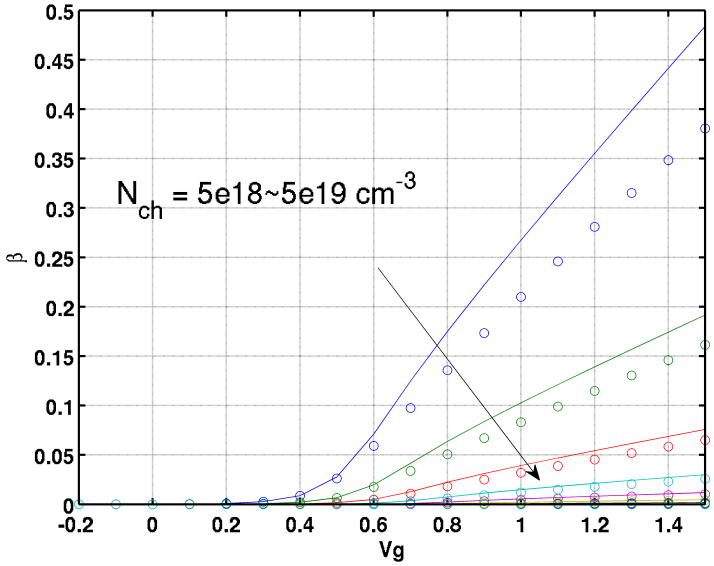

Figure B.1. β obtained from equation (2.11) solved using Newton-Raphson iteration (symbols) and from initial guess expressed by equation (B.7) (lines) using (B.8) in a linear scale, for different doping concentrations. Equation (B.7) should be extended to cover lightly doped devices. $T_{FIN} = 20nm$, $t_{ox} = 1nm$, and a gate work-function equal to $4.4eV$ have been used for simulations.

(B.10). As expected, equation (B.10) is valid for devices with lightly or heavily doped channels.

B.2 Quartic Modified Iteration: Implementation and Evaluation

In order to complete the explicit surface potential model, a quartic modified iteration have to be derived. Quartic modified iteration update the initial guess expressed by (B.10) using a high order correction:

$$\beta_1 = \beta_0 - \frac{f_0}{f_1}\left(1 + \frac{f_0 f_2}{2f_1^2} + \frac{f_0^2\left(3f_2^2 - f_1 f_3\right)}{6f_1^4}\right) \tag{B.11}$$

where f_n is the n derivative of equation (2.11) with respect to β, i.e. $f_n = \frac{\partial^n f}{\partial \beta^n}|_{\beta=\beta_0}$. Using this algorithm, a explicit surface potential model can be calculated using the following steps:

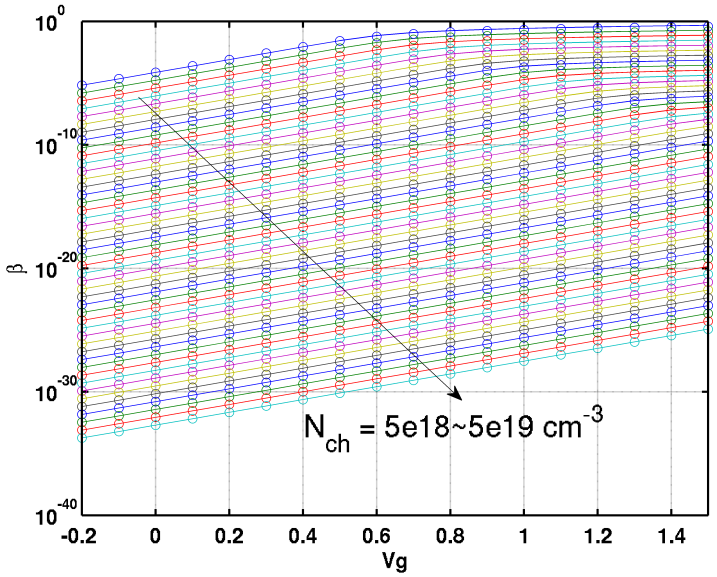

Figure B.2. β obtained from equation (2.11) solved using Newton-Raphson iteration (symbols) and from initial guess expressed by equation (B.7) (lines) using (B.8) in a logarithm scale, for different doping concentrations. Equation (B.7) should be extended to cover lightly doped devices. $T_{FIN} = 20nm$, $t_{ox} = 1nm$, and a gate work-function equal to $4.4eV$ have been used for simulations.

1. Calculate the continuous starting function in the following order:

$$T_a = \psi_{pert}/V_{tm}^2 \tag{B.12a}$$

$$T_b = e^{\psi_{pert}/V_{tm}} \tag{B.12b}$$

$$T_c = 2V_{tm} \tag{B.12c}$$

$$r = \frac{2\epsilon_{si}t_{ox}}{\epsilon_{ox}T_{FIN}} \tag{B.12d}$$

$$A_g = \frac{\frac{r\psi_{pert}}{V_{tm}}}{1 - e^{\frac{-r\psi_{pert}}{V_{tm}}}} \tag{B.12e}$$

$$F_{th} = (2r-1)\frac{\psi_{pert}}{2V_{tm}} + \ln\left(\frac{\sqrt{A_g}}{(2r-1)\frac{\psi_{pert}}{2V_{tm}}}\right) \tag{B.12f}$$

$$\beta_{doped} = e^{\frac{-\psi_{pert}}{2V_{tm}}}\frac{A_g}{r}\sqrt{\left(\frac{\ln\left(1+e^{2(F-F_{th})}\right)}{2A_g}+1\right)^2 - 1} \tag{B.12g}$$

$$\beta_0 = \frac{1}{\frac{1}{\beta_{doped}} + \frac{2}{\pi}} \tag{B.12h}$$

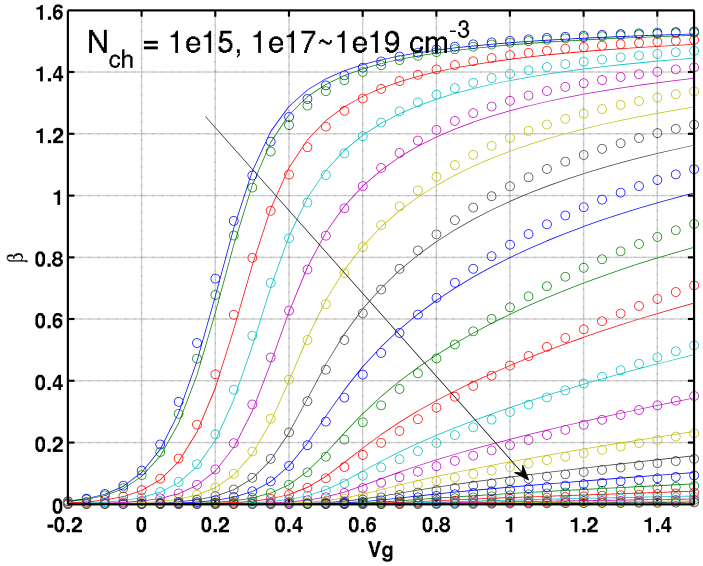

Figure B.3. β obtained from equation (2.11) solved using Newton-Raphson iteration (symbols) and from the proposed CSF expressed by equation (B.10) (lines) in a linear scale, for different doping concentrations. Equation (B.10) is valid for devices with lightly or heavily doped channels. Note that for lightly doped devices β has a similar behaviour, which changes as doping is increased. $T_{FIN} = 20nm$, $t_{ox} = 1nm$, and a gate work-function equal to $4.4eV$ have been used for simulations.

2. Compute:

$$tang0 = \tan(\beta_0) \tag{B.13a}$$
$$cosg0 = \cos(\beta_0) \tag{B.13b}$$
$$secg0 = cosg0^{-1} \tag{B.13c}$$
$$secg0sq = secg0^2 \tag{B.13d}$$
$$lng0 = \ln(\beta_0) \tag{B.13e}$$

3. Compute:

$$T_0 = 1 + \beta_0 tang0 \tag{B.14a}$$
$$T_1 = \beta_0^2(T_b secg0sq - 1) + T_{abb}(\psi_{pert} - T_c \ln(cosg0)) \tag{B.14b}$$
$$T_2 = \sqrt{T_1} \tag{B.14c}$$
$$T_3 = -2\beta + T_{abb}T_c tang0 + 2T_b\beta secg0sqT_0 \tag{B.14d}$$
$$T_4 = -2 + 2T_b\beta_0^2 secg0sq^2 + secg0sq(2T_b + T_aT_c + 8T_b\beta tang0 + 4T_b\beta_0^2 tang0^2) \tag{B.14e}$$
$$T_5 = 2tang0T_4 + 4(3T_b\beta secg0sq^2T_0 + tang0 + 2T_b secg0sqT_0 tang0) \tag{B.14f}$$

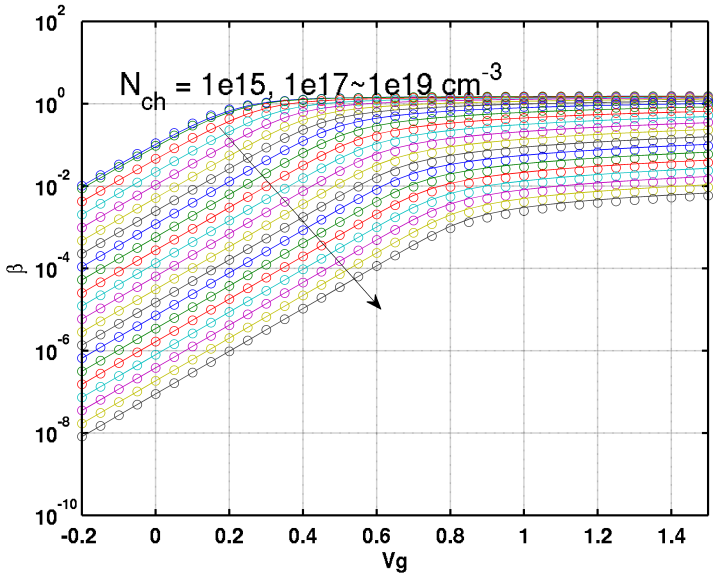

Figure B.4. β obtained from equation (2.11) solved using Newton-Raphson iteration (symbols) and from the proposed CSF expressed by equation (B.10) (lines) in a logarithm scale, for different doping concentrations. Equation (B.10) is valid for devices with lightly or heavily doped channels. Note that for lightly doped devices β has a similar behaviour, which changes as doping is increased. $T_{FIN} = 20nm$, $t_{ox} = 1nm$, and a gate work-function equal to $4.4eV$ have been used for simulations.

4. Compute derivatives:

$$f_0 = lng0 - lln(cosg0) + rT_2 - F \tag{B.15a}$$

$$f_1 = \beta^{-1} + tang0 + \frac{rT_3}{2T_2} \tag{B.15b}$$

$$f_2 = -\beta_0^{-2} + secg0sq - \frac{rT_3^2}{4T_2^3} + \frac{rT_4}{2T_2} \tag{B.15c}$$

$$f_0 = 2\beta_0^{-3} + 2secg0sqtang0 + \frac{3rT_3}{4T_2^3}\left(\frac{T_3^2}{2T_2^2} - T_4\right) + \frac{rT_5}{2T_2} \tag{B.15d}$$

5. Update β_0 to β_1 using a quartic modified iteration:

$$\beta_1 = \beta_0 - \frac{f_0}{f_1}\left(1 + \frac{f_0 f_2}{2f_1^2} + \frac{f_0^2\left(3f_2^2 - f_1 f_3\right)}{6f_1^4}\right) \tag{B.16a}$$

Steps 2 to 5 can be repeated more than once. The number of iterations can be obtained by doing an extensive analysis of the proposed model accuracy under difference device and bias conditions. Figure B.5 shows the error of β obtained from the proposed

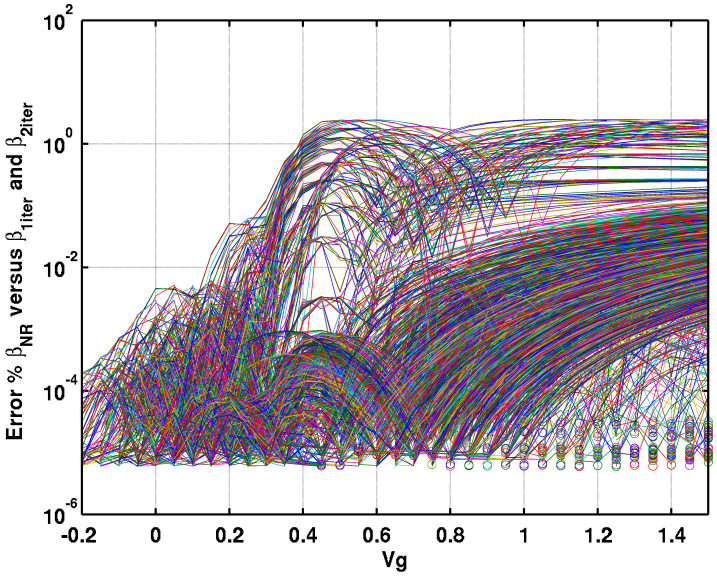

Figure B.5. Error of β obtained from the proposed explicit surface potential model with one (lines) and two (symbols) iterations with respect to β obtained using Netwon-Raphson method under all different combinations of doping concentration (1×10^{15} to $1 \times 10^{19} cm^{-3}$), channel width (1 to $30nm$), dielectric thickness (0.5 to $5nm$), gate voltage (-0.2 to $1.5V$), and temperature (-100 to 100°C).

explicit surface potential model with one and two iterations with respect to β obtained using Netwon-Raphson method under all different combinations (>52500 simulations) of doping concentration (1×10^{15} to $1 \times 10^{19} cm^{-3}$), channel width (1 to $30nm$), dielectric thickness (0.5 to $5nm$), gate voltage (-0.2 to $1.5V$), and temperature (-100 to 100°C). Using one Householder's iteration the RMS error is 0.28% with a peak error of 2.47%. Using two Householder's iterations the RMS error is 1.58×10^{-6}% with a peak error of 3.31×10^{-5}%. Therefore, only two iterations are needed to obtain an accurate solution of β as shown by figure B.6.

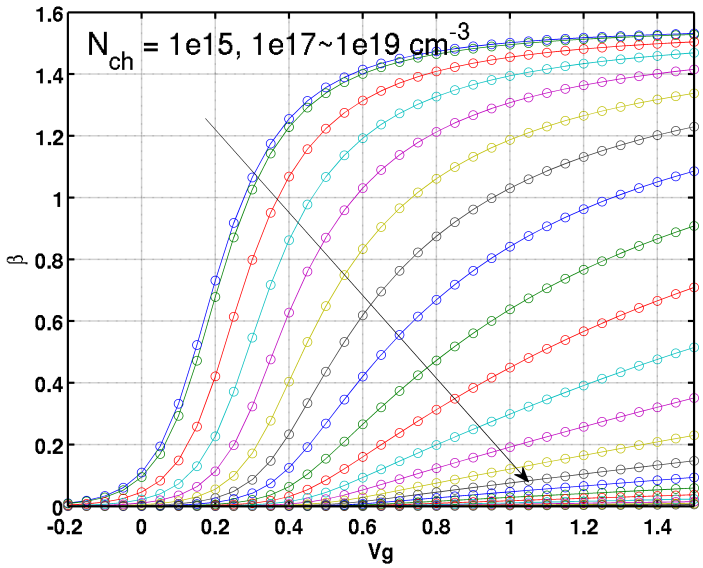

Figure B.6. β obtained from equation (2.11) solved using Newton-Raphson iteration (symbols) and from the proposed explicit surface potential model using two Householder's iterations (lines) in a linear scale, for different doping concentrations. $T_{FIN} = 20nm$, $t_{ox} = 1nm$, and a gate work-function equal to $4.4eV$ have been used for simulations.

Appendix C

Unified Model Implementation in Verilog-A

The complete code of BSIM-CMG can be found at [1]. Here, the core model implementation in Verilog-A is introduced. First, bulk bias threshold voltage shift is calculated (variable T0 and T1):

Listing C.1. Threshold voltage shift due bulk bias

```
vch = vs;
T4 = -qdep;
if (BULKMOD != 0) begin //bulk devices
  T1 = `hypsmooth((2.0 * phib + vch - ves), 0.1);
  T3 = -K1_t / (2.0 * Vt) * (sqrt(T1) - sqrt(2.0 * phib));
  T0 = -qdep - T3 + vth_fixed_factor_Sub + QMF * T4;
  T1 = -qdep - T3 + vth_fixed_factor_SI;
end else begin //SOI devices
  T0 = -qdep + vth_fixed_factor_Sub + QMF * T4;
  T1 = -qdep + vth_fixed_factor_SI;
end
```

The next step is to obtain a solution of the equation unified charge model (represented as e0 in the code):

$$\begin{aligned} e_0 = &-(v_G - v_o - \Delta q_{dep} - v_{ch}) - q_m + \ln(-q_m) \\ &+ \ln\left(\frac{q_t^2}{e^{q_t} - q_t - 1}\right) + \alpha_{QM}\left(q_m + q_{dep}\right)^{2/3} = 0 \end{aligned} \tag{C.1}$$

It is obtained by a initial guess, followed by two second order Newton's update (note e_1 is e_0' and e_2 is e_0'', both derivatives with respect to q_m). This model also incorporate quantum mechanical corrections. If the charge is very small ($qm > 1.0e-7$), the code does not calculate the iterations, and just initial guess is good enough for the calculations.

Listing C.2. UFCM core model implementation in Verilog-A

```
T2 = (vgs - vch) / Vt;
F0 = -T2 + T1;
T3 = 0.5 * (T2 - T0);
qm = exp(T3);
if (qm > 1.0e-7) begin  // inversion condition
  T7 = ln(1.0 + qm);
  qm = 2.0 * (1.0 - sqrt(1.0 + T7 * T7)); // Initial Guess
  T8 = (qm * ALPHA_UFCM + qdep) * rc;
  T4 = T8 / (exp(T8) - T8 - 1.0);
  T5 = T8 * T4;
  qm_ln = ln(-(qm + qdep));
  e0 = F0 - qm + ln(-qm) + ln(T5) + QMF * exp(2/3 * qm_ln);
  e1 = -1.0+1.0/qm+(2.0/T8-T4-1)*rc-2/3*QMF*exp(-1/3 * qm_ln);
  e2 = -1.0 / (qm * qm) - (2.0 / 9.0) * QMF * exp(-4/3 * qm_ln
   );
  //iteration update
  qm = qm - (e0 / e1) * (1.0 + (e0 * e2) / (2.0 * e1 * e1));

  T8 = (qm * ALPHA_UFCM + qdep) * rc;
  T4 = T8 / (exp(T8) - T8 - 1.0);
  T5 = T8 * T4;
  qm_ln = ln(-(qm + qdep));
  e0 = F0 - qm + ln(-qm) + ln(T5) + QMF * exp(2/3 * qm_ln);
  e1 = -1.0+1.0/qm+(2.0/T8-T4-1)*rc-2/3*QMF*exp(-1/3 * qm_ln);
  e2 = -1.0 / (qm * qm) - (2.0 / 9.0) * QMF * exp(-4/3 * qm_ln
   );
  //iteration update
  qm = qm - (e0 / e1) * (1.0 + (e0 * e2) / (2.0 * e1 * e1));
end else begin // Subthreshold condition
  qm = -qm * qm;
end
qis = -qm * Vt;
```

Appendix D

1D Numerical Simulation for UTBSOIs

The code presented in this appendix solves the Poisson's Equation of a independent double gate FinFET (UTBSOI) in 1-D, assuming Boltzman charge statistics. It solves Poisson's Equation using finite difference method in python 3 version (run the test code to see results). numpy, scipy and pylab libraries are needed. The code has the same form as that in Appendix A; however, since this is an asymmetric device, different boundaries conditions must be implemented. Front and back boundary conditions are related to the semiconductor-insulator interface where Gauss's law must be fulfilled, i.e., displacement vector must be constant at the interface (Dirichlet's boundary conditions):

$$\varepsilon_{\text{ch}} E_{ch,front} = \varepsilon_{\text{ox,front}} E_{ox,front} \tag{D.1}$$

$$\varepsilon_{\text{ch}} E_{ch,back} = \varepsilon_{\text{ox,back}} E_{ox,back} \tag{D.2}$$

Assuming there is not charge at the insulators, the oxide fields can be obtained as:

$$E_{ox,front} = \frac{V_{GF} - V_{FB,front} - \psi(x_1)}{t_{ox,front}} \tag{D.3}$$

$$E_{ox,back} = \frac{V_{GB} - V_{FB,front} - \psi(x_{n+1})}{t_{ox,back}} \tag{D.4}$$

Then only T matrix and f vector must be change accordenly to the new boundary conditions. The following code implements these changes.

Listing D.1. Python code for 1D UTBSOI

```
1 import numpy as np
2 from numpy.matlib import repmat
3 from scipy.misc import factorial
4 from scipy import sparse
```

```
5  from scipy.sparse import lil_matrix
6  from scipy.sparse.linalg import spsolve
7  from numpy.linalg import solve, norm
8
9  from scipy import integrate
10 from scipy.integrate import quad
11
12
13 def mkfdstencil(x,xbar,k):
14 #this funtion is sue to create finite diference method matrix
15   maxorder             = len(x)
16   h_matrix             = repmat(np.transpose(x)-xbar,maxorder
      ,1)
17   powerfactor_matrix   = np.transpose(repmat(np.arange(0,
      maxorder),maxorder,1))
18   factorialindex       = np.transpose(repmat(factorial(np.
      arange(0,maxorder)),maxorder,1))
19   taylormatrix         = h_matrix ** powerfactor_matrix /
      factorialindex
20   derivativeindex      = np.zeros(maxorder)
21   derivativeindex[k]   = 1
22   u = np.linalg.solve(taylormatrix,derivativeindex)
23   return u
24
25 def K_generator(x):
26 #this return matrix of Poisson Equation in Silicon Fin, with
      Neuman BC at both ends
27   N=len(x);
28   K = lil_matrix((N, N))
29   K[0,:5]=mkfdstencil(x[0:5],x[0],1)
30   i=1
31   for xbar in x[1:-1]:
32     K[i,i-1:i+2]=mkfdstencil(x[i-1:i+2],xbar,2)
33     i+=1
34   K[i,i-6:i+1]=mkfdstencil(x[i-6:i+1],x[i],1)
35   return K.tocsr()
36
37 def Efield_matrix(x):
38 #this return matrix of Poisson Equation in Silicon Fin, with
      Neuman BC at both ends
39   N=len(x);
40   K = lil_matrix((N, N))
41   K[0,:5]=mkfdstencil(x[0:5],x[0],1)
42   i=1
```

```
43    for xbar in x[1:-1]:
44      K[i,i-1:i+1]=mkfdstencil(x[i-1:i+1],xbar,1)
45      i+=1
46    K[i,i-6:i+1]=mkfdstencil(x[i-6:i+1],x[i],1)
47    return K.tocsr()
48
49  def rho_phi(phi,q,vt,ni,Nch,ech):
50    return -(-q*(ni**2/Nch)*np.exp(phi/vt)-q*Nch)/ech
51
52  def drho_dphi(phi,q,vt,ni,Nch,ech):
53    return q*(ni**2/Nch)*np.exp(phi/vt)/(vt*ech)
54
55  def charge_fb(phi,x,Vgf,Vgb,Tsi,q,vt,ni,Nch,ech,eins,tins,
      tinsbox,\
56  phi_gatef,phi_gateb,phi_substrate,Eg,N):
57      Vfbf      = phi_gatef - phi_substrate -Eg/2-vt*np.log(Nch/
      ni)
58      Vfbb      = phi_gateb - phi_substrate -Eg/2-vt*np.log(Nch/
      ni)
59      print (Vfbf)
60      print (Vfbb)
61      Qf =  eins/(tins)*(Vgf-Vfbf-phi[0])
62      Qb =  eins/(tinsbox)*(Vgb-Vfbb-phi[-1])
63      #print total_charge
64      return  Qf,Qb
65
66  def solvePoisson(Vgf,Vgb,Tsi,q,vt,ni,Nch,ech,eins,tins,tinsbox
      , \
67  phi_gatef,phi_gateb,phi_substrate,Eg,N,phi,x,K):
68      Vfbf      = phi_gatef - phi_substrate -Eg/2-vt*np.log(Nch/
      ni)
69      Vfbb      = phi_gateb - phi_substrate -Eg/2-vt*np.log(Nch/
      ni)
70      print (Vfbf)
71      print (Vfbb)
72      #x        = Tsi/2*np.linspace(-1, 1, N)
73      rhs      = np.zeros(N)
74      jrhs     = np.zeros(N)
75      J = lil_matrix((N, N))
76      ################################
77      #K = K_generator(x)
78      g    = 1000
79      iter=1
80      while True:
```

```
81          iter+=1
82          if (norm(g)/N**2) <1e-16 or iter> 50:
83              print ("Solve in iterations:" + str(iter))
84              print ("Solve with norm:" + str(norm(g)/N**2))
85              break
86          rhs[1:N]    = rho_phi(phi[1:N],q,vt,ni,Nch,ech)
87          rhs[0]      = -eins/(ech*tins)*(Vgf-Vfbf-phi[0])
88          rhs[-1]     = eins/(ech*tinsbox)*(Vgb-Vfbb-phi[-1])
89
90          jrhs[1:N]   = drho_dphi(phi[1:N],q,vt,ni,Nch,ech)
91          jrhs[0]     = -eins/(ech*tins)*(-1)
92          jrhs[-1]    = eins/(ech*tinsbox)*(-1)
93
94          J.setdiag(jrhs)
95
96          g   = K*phi-rhs
97          dg  = (K-J.tocsr())
98          phi = phi -  solve(dg.todense(),g)
99      return phi
```

The following code call and runs the 1D solver for UTBSOI devices.

Listing D.2. Python code to call and run 1D UTBSOI solver

```
1  import IMGDGPoisson1D
2  import numpy as np
3  import pylab
4  from scipy import integrate
5  import scipy
6
7  ############################PARAMETERS
       ##############################
8  #physical constants
9  q        = 1.6e-19
10 vt       = 0.0259
11 ni       = 2.6e10
12 k        = 1.380650e-23
13 T        = 300
14 eo       = 8.854000e-14
15 eins     = 3.453060e-13
16 ech      = 1.035918e-12
17 Eg       = 1.169640
18 Nc       = 2.540000e+19
19 Nv       = 3.140000e+19
20
21 #device dimensions and parameters
```

```
Tsi              = 12e-9
tins             = 2e-9
tinsbox          = 10e-9
Nch              = 1e15
phi_substrate    = 4.05
phi_gatef        = 4.5
phi_gateb        = 4.5

##############################SIMULATION
    ##############################
Vg_array = np.linspace(-1, 2, 10)
Vgb = 0.5 #front gate fixed in this case

N = 100
phiguess = np.zeros(N)
x        = Tsi/2*np.linspace(-1, 1, N)
K = IMGDGPoisson1D.K_generator(x)
Efield_mtx = IMGDGPoisson1D.Efield_matrix(x)
iter=1
for Vgf in Vg_array:
    print ("solving: " + str(iter))
    iter+=1
    print ("Solve for Vgf %5.3f and Vg %5.3f, using %d nodes"
    % (Vgf,Vgb,N))
    phiguess = IMGDGPoisson1D.solvePoisson(Vgf,Vgb,Tsi,q,vt,ni
    ,Nch,ech,eins,tins,tinsbox,phi_gatef,phi_gateb,
    phi_substrate,Eg,N,phiguess,x,K)
    pylab.figure(1)
    pylab.plot(x ,phiguess,'o')
    pylab.figure(2)
    pylab.plot(x ,q*ni**2/(Nch)*np.exp(phiguess/vt),'o')
    Efield = Efield_mtx*phiguess
    pylab.figure(3)
    pylab.plot(x ,Efield,'o')
    pylab.figure(4)
    pylab.plot(Vgf ,Efield[-1],'o')
    pylab.plot(Vgf ,Efield[0],'s')
    y=q*ni**2/(Nch)*np.exp(phiguess/vt)
    qchannel = scipy.integrate.simps(y, x)
    pylab.figure(5)
    pylab.plot(Vgf ,qchannel,'s')

pylab.show()
```

Appendix E

Energy Calculation with Hspice

This appendix explains how to accurately calculate energy using Hspice. Each circuit simulation solve self-consistently the voltages and currents for each element. Using these quantities, power can be obtained using $V * I$. Energy flow is then calculated by integrating the power using cumulatively numerical integration, by the composite trapezoidal rule. It is important to notice that simulations settings are very important for accurate energy calculations. Simulations in this work were obtained using Hspice simulation engine, with simulations options set to RUNLVL=6, METHOD=GEAR, and MAXORD=3. Fig. E.1 shows energy calculations of a simple RC circuit using default Hspice options and the accurate one used for this work; clearly, the chosen settings are needed for precise calculations.

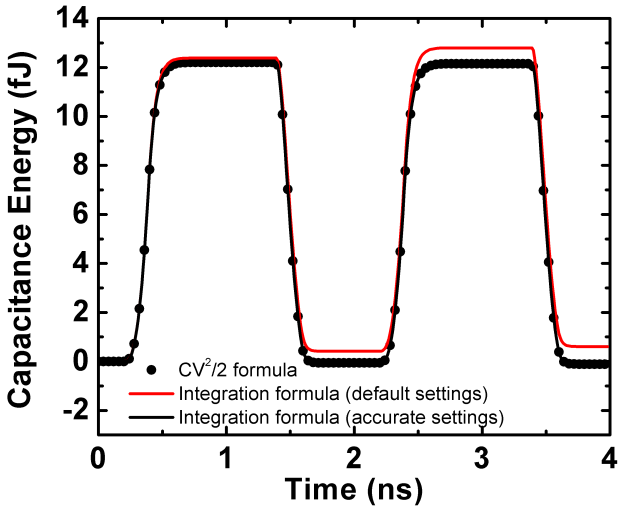

Figure E.1. Energy of a capacitance in a RC circuit as a function of time calculated using analytical formula, and numerical integration of $V * I$ using default and accurate simulation settings.