Transconductance Amplifier for SC Filter

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Technical Report No. UCB/EECS-2018-4
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2018/EECS-2018-4.html

February 8, 2018

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***Abstract*— This paper presents a fully differential transconductance amplifier. The proposed OTA is designed using 65nm CMOS process with nominal parameters and a voltage supply of 1.2V. The amplifier is designed to keep the power dissipation to a minimum while meeting design constraints.**

I. INTRODUCTION

The OTA is a fundamental piece in most analog designs. The OTA is widely used in instrumentation amplifiers, ADC and filter circuits. In this paper, we inspect and design a CMOS OTA. The OTA will be used in a low pass filter composed of switching capacitors. Our part in the design is to guarantee a successful operation of the filter while applying what we learn about amplifier design in the class.

In Section II, the different OTA topologies that were considered and established are presented as well as design equations and parameters related to the OTA architecture of choice. Section III introduces the simulations and results. Section IV covers discrepancies, issues with requirements and future work to improve the design to meet all requirements that were off.

II. OTA TOPOLOGIES

Three OTA topologies are discussed and presented:

(1) Two stage OTA.
(2) Telescopic cascode OTA.
(3) Folded cascode OTA.

The design requirements are key to choose a proper topology that could potentially meet specifications. Table 1 presents the specifications for the project.

Parameter	**Value**
Input amplitude (differential)	2V peak-to-peak
3-dB bandwidth	10 MHz
Sampling frequency f_s	150 MHz
Static settling error	<0.1%
Dynamic settling error	<0.05%
Dynamic range at output	80 dB
Temperature (all simulations)	100 ºC
Power dissipation	Minimum

Table 1. Design specifications.

Due to time constraint of the project deadline and several and also several attempts to get the design working I discarded the two stage topology although it was the topology that I needed to get the highest gain, highest output swing and medium power consumption. A couple of things I had problems with was setting up the CMFB properly for my two stage topology. From there I had to decide to whether go with telescopic cascode or folded cascode. The fully implemented differential folded cascode suppresses the even harmonics which are dominant, has a high common mode rejection ratio and an improve dynamic range. Due to the reasons mentioned above I decided to go with the folded cascode.

The first step during my initial analysis was to identify the gain needed for my amplifier. Since I started working with an ideal model and the previous project I was working on before getting the new requirements had a gain of two, I decided to keep it the same so that I wouldn't go back and change it(I should have done it). The gain selected was 2 and the first thing I did was to identify what kind of switched capacitor topology I was dealing with. The topology I was assigned to work on was two integrator loop biquad switched capacitor. My first assessment was to simplify the switched capacitor to a resistor equivalence, this equivalence is only correct at fc=infinity but it is approximately correct for fc>>f. the transfer function ended up showing that for low frequencies the gain depended on the two switching capacitances a1C1 and a2C1. By setting up a1 =2 and a2 =1 I was able to get my pretty good approximation to the closed loop gain. I arbitrarily picked 1pf for the feedback capacitor since my f3db is pretty much set by the ratio a1/a2. Moreover, I started my assumptions and iterations using matlab scripts where I store all the different formulas, required parameters and approximations. Knowing in advance that the only way to achieve the output swing requirement is through a second stage, I took an initial guess for the maximum output swing that I can obtain for my design by making sure I keep the devices in saturation. Figure 1 shows the designed folded cascode OTA with the summary for initial guess device parameters.

Assuming a 200mv voltage drop per transistor on the bottom branch I calculated my minimum output voltage to be 400mV. Similarly, my maximum output voltage can be solved by looking at the top branch which is around 800mV. After this, I made more assumptions that are somewhat reasonable from our lectures such as v* ~120-160m, beta, L, Cl.

From these assumptions, I was able to plug some values into the matlab script and get parameters such as gm_ID, v2ot, CLtot, and etc. Having the technology database lookup functions handy made the transition to finding widths according to GM_ID, and L. this also gave me the opportunity to play with the rest of the parameters such as CDD,CSS to add some parasitic into the design.

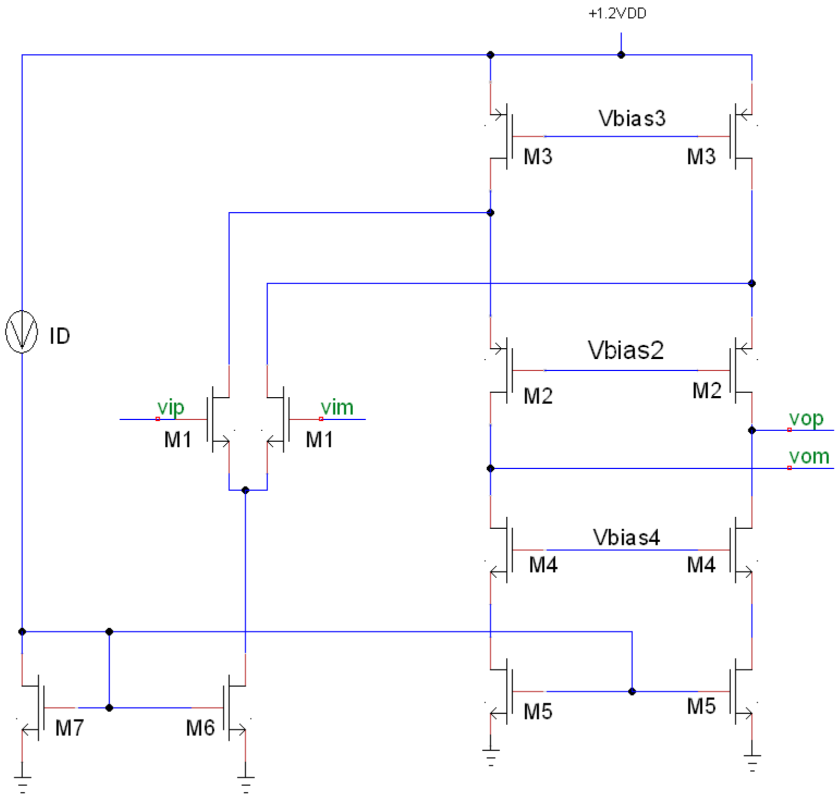


Figure 1. folded cascode OTA and device parameters.

After being able to test the open loop gain of the OTA, the next challenge approached. In order to establish or stabilize the operating points of the OTA we needed to design a common-mode feedback circuit. This common mode feedback is assumed to set the desired common mode DC output ~VDD/2. Figure 2 shows the OTA with CMFB.

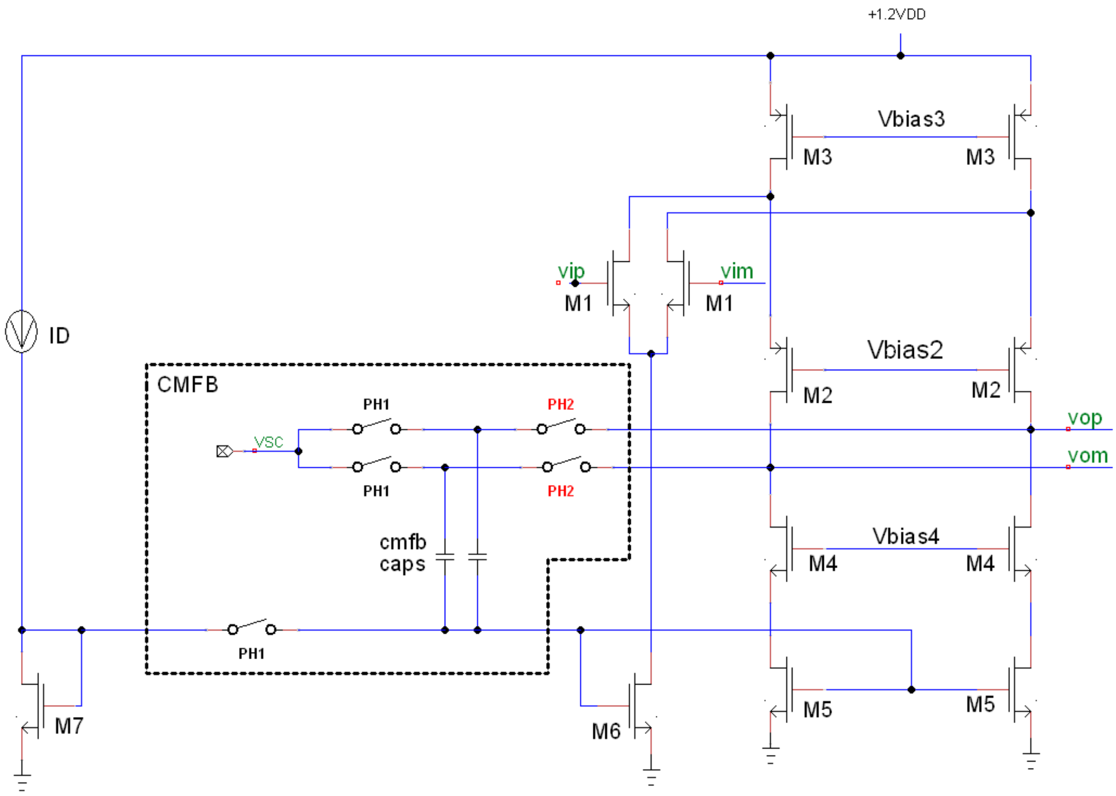


Figure 2. OTA with CMFB implementation

III. Simulations and Results

In this section I will be presenting both the simulations of the ideal model and the transistor made OTA. The full SC filter is shown in figure 3.

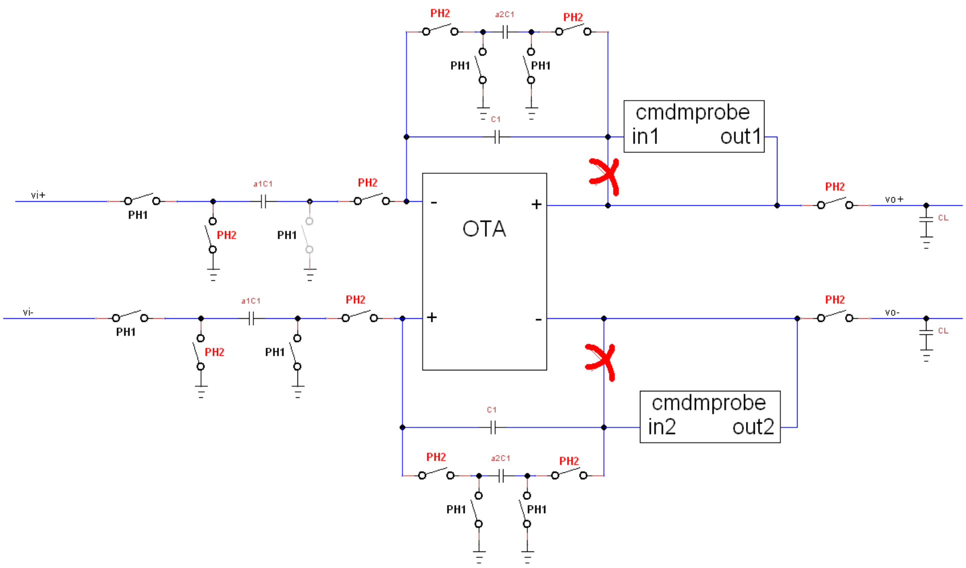


Figure 3. fully differential SC OTA

A. Open loop Gain

In this setup, the differential inputs and outputs are connected to ideal Baluns. The cmdmprobe is setup in such a way that it breaks the major feedback loops in the setup, except for the transistor made OTA. The way I designed my OTA it keeps the CMFB internal to the OTA and the CMFB loop should be also broken. Due to this, I only simulated the open loop gain with PSTB on the ideal OTA. Figure 4 shows the open loop gain of the OTA.

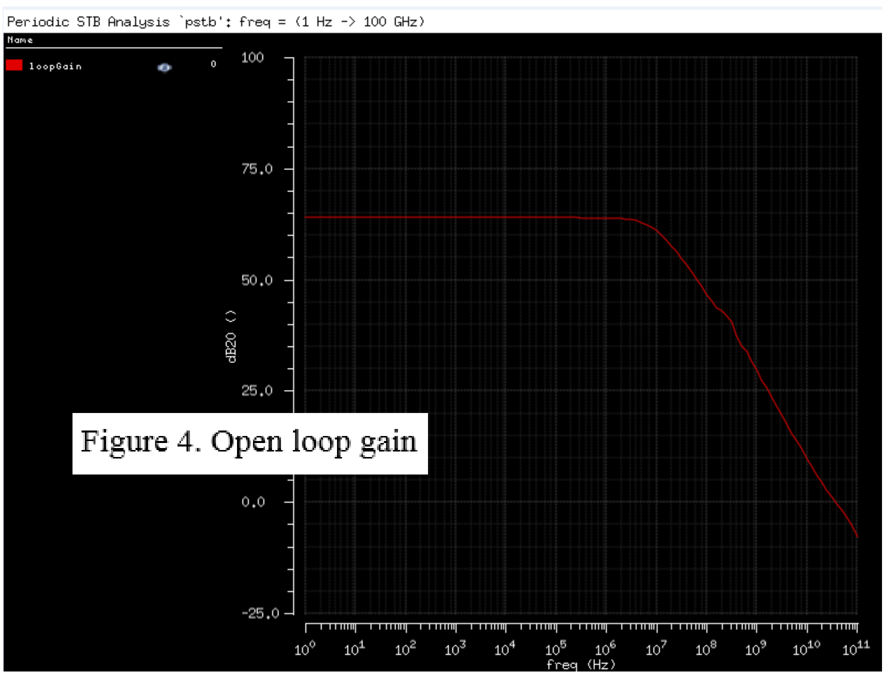
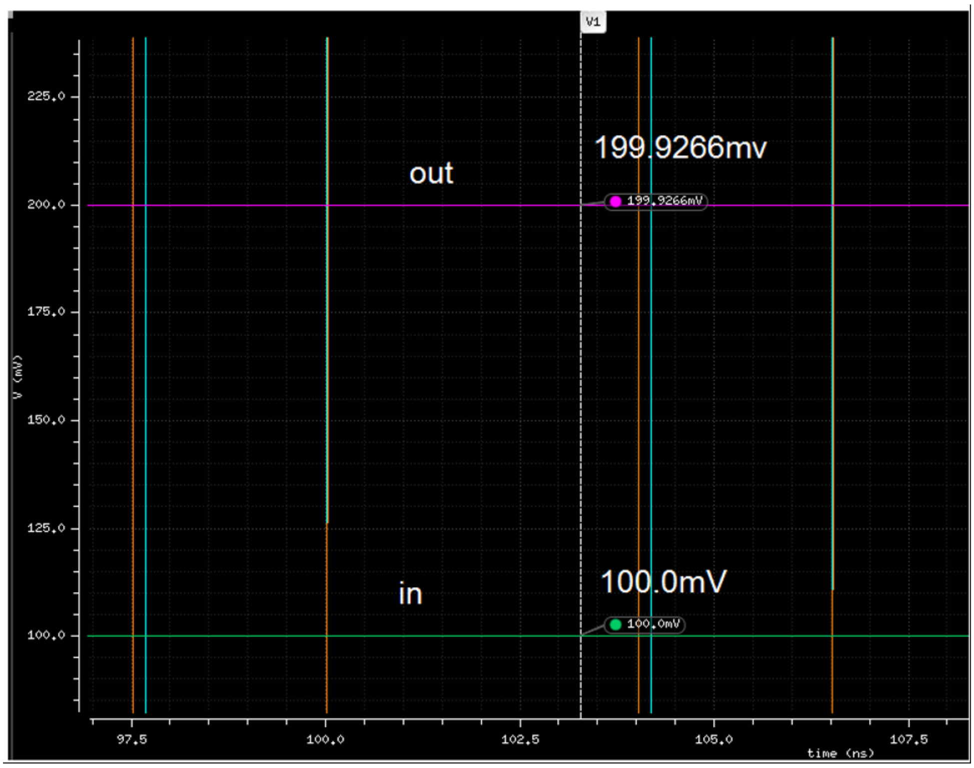


Figure 4. Open loop gain

B.   OTA static settling error

One of the project requirements was to keep the static settling error under 0.1%. which is indirectly proportional to To so by default in order to meet this requirement I needed a high open loop gain, this is achieved with the ideal OTA and barely meet the spec with my second OTA. Figure 5 shows both waveforms with Estatic = 0.04% for the first OTA and Estatic = 0.09% for the second one.



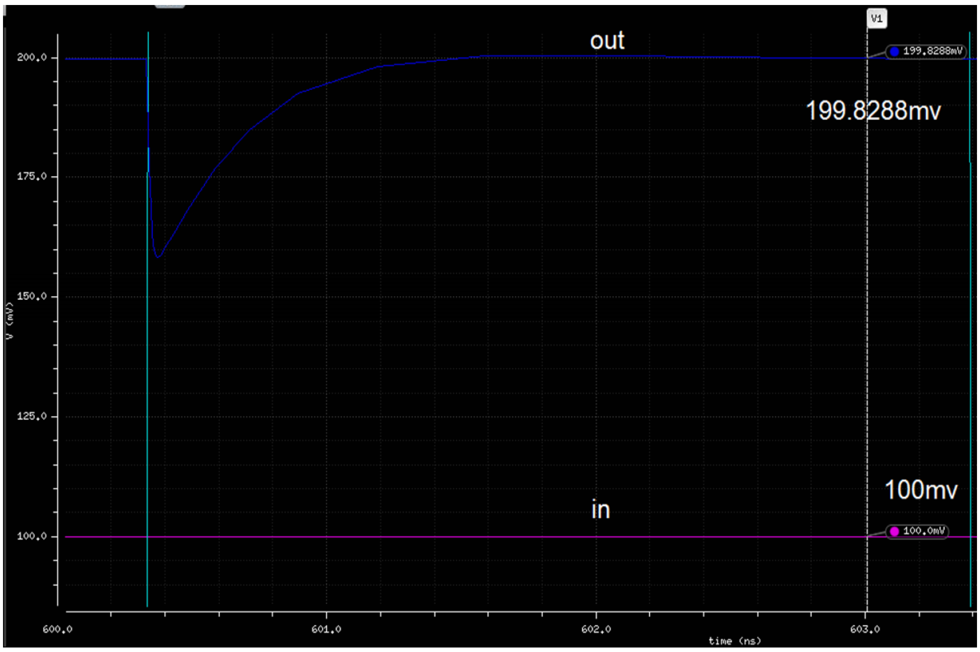
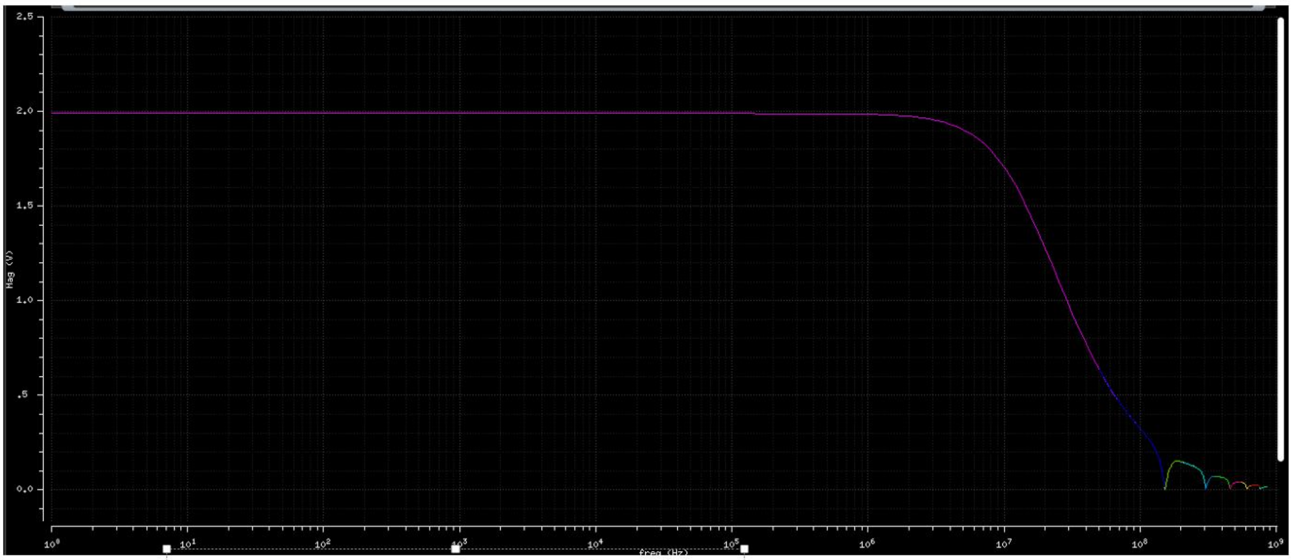


Figure 5. static settling error.

C. Frequency response

To verify the complete filter transfer function of the OTA, a periodic AC analysis is performed. The results are on spec according to the equation shown below. Figure 6 shows the transfer function of the second OTA with a gain magnitude of 2V and including up to 5 harmonics.



$$\text{Freq Response} = \frac{a2}{a1} \cdot \frac{1}{1 + Sc * R}$$

Freq@ 3b = 2/1.41 = 1/(1+ s/(Fclk * a2))

Fclk = 150Mhz
a2=1
10Mhz = F3db

Figure 6. Frequency response

D. *Pnoise*

After verifying the transfer function, the next step was to run a Pnoise simulation which is very similar to PAC but a sine wave is needed at the input. Figure 7 shows both the density and integrated noise versus frequency for the simulation for first OTA and second OTA.

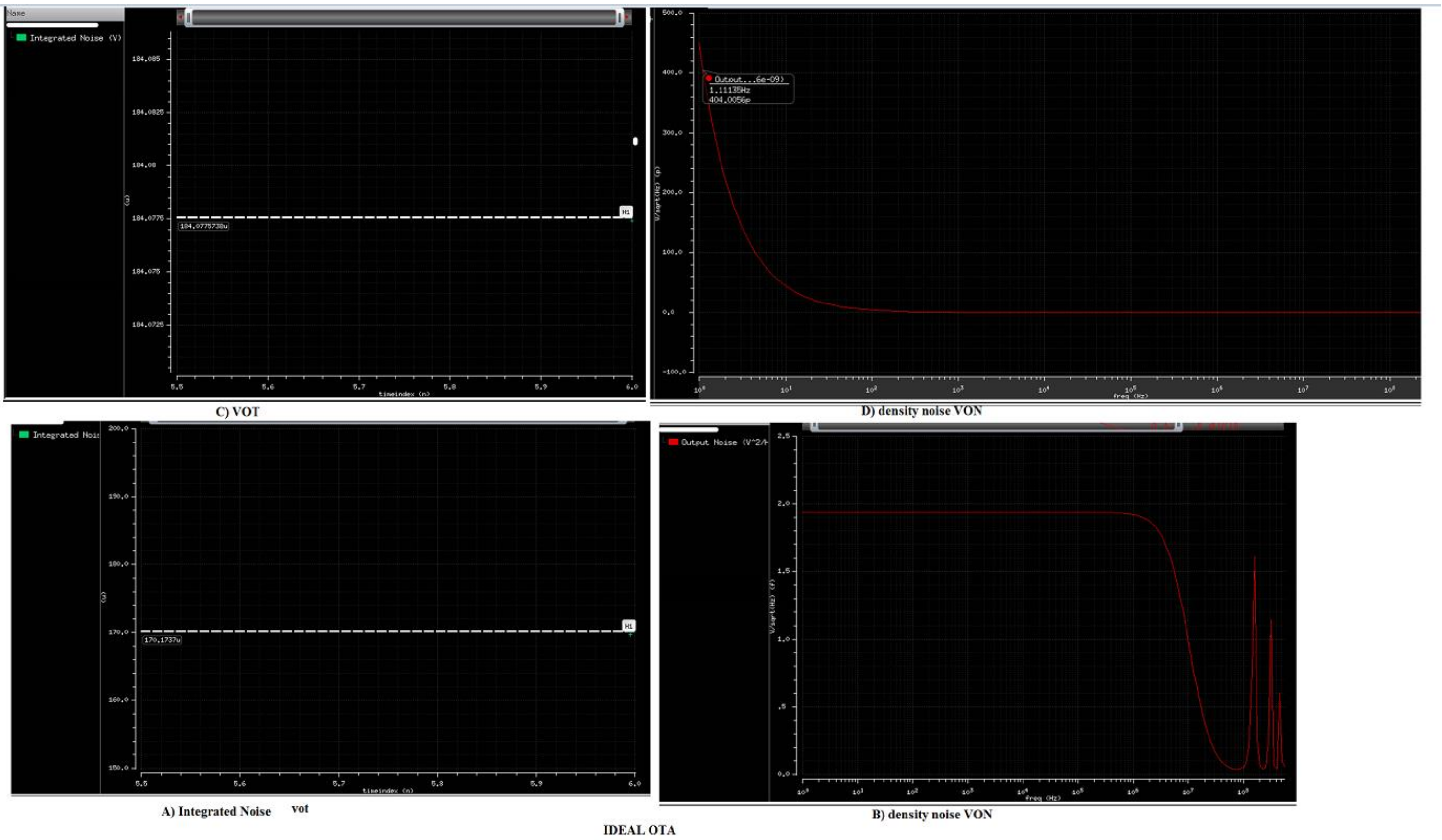


Figure 7. A) vot = 170.1737u B) density noise Von 1.95V/(sqrt(hz)) (First ideal OTA)

C) vot = 184.077573u D) density noise Von (Second OTA)

My calculated value for vot = 214.132 uV , vot can be calculated by the combination of vopp and the dynamic range as follows:

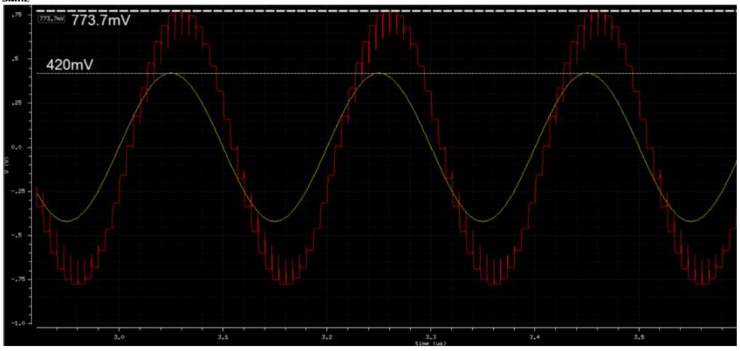
V^2ot = ((vopp/2)^2)/2/DR then take the sqr root of the result. The reason I belive my values were not close to the simulation values is because my DR got affected really bad when I found out I couldn't get the second stage working and same thing for vopp (plus I decided to make my gain 2 instead of one...) … I had to be more conservative with the values picking something close to what I thought was going to be getting from the simulations. I did not have enough time to go through the simulations and iterate my design one more time to improve my parameters.

E. Time domain simulation with sinusoidal full-scale inputs at 0.5f-3db, f-3b, and 2f-3db

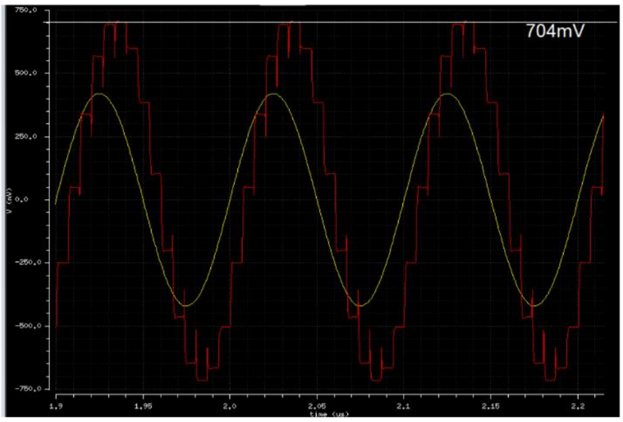
For this exercise we can see how limited is my full input swing due to the poor judgement on my first assumptions a gain of one would have improved my swing and even a simple second stage as well.

Both OTAs are simulated and we can see how my gain degrades as we get closer and closer to unity.

5MHZ



10MHz



20Mhz

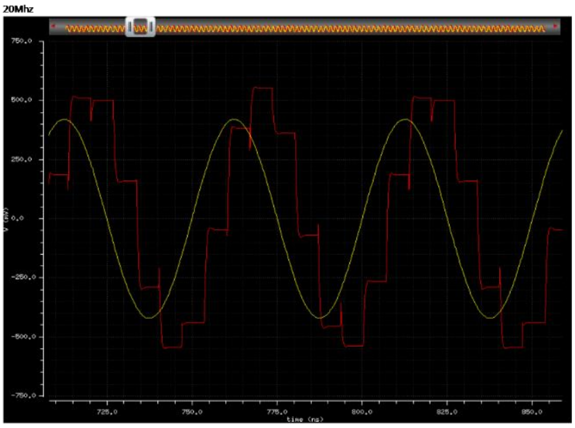
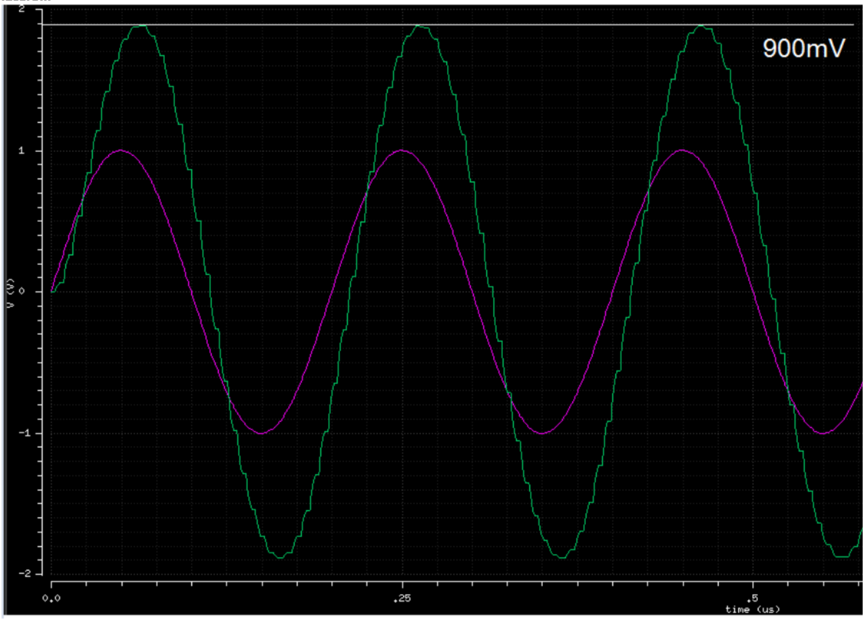
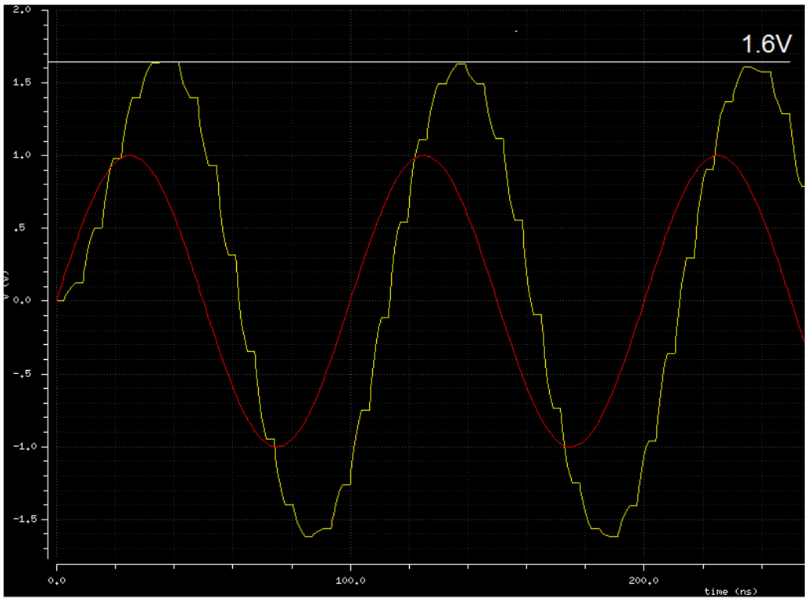


Figure 8. time domain simulation for second amplifier.

Ideal 5M



10MHzz ideal



20Mhz

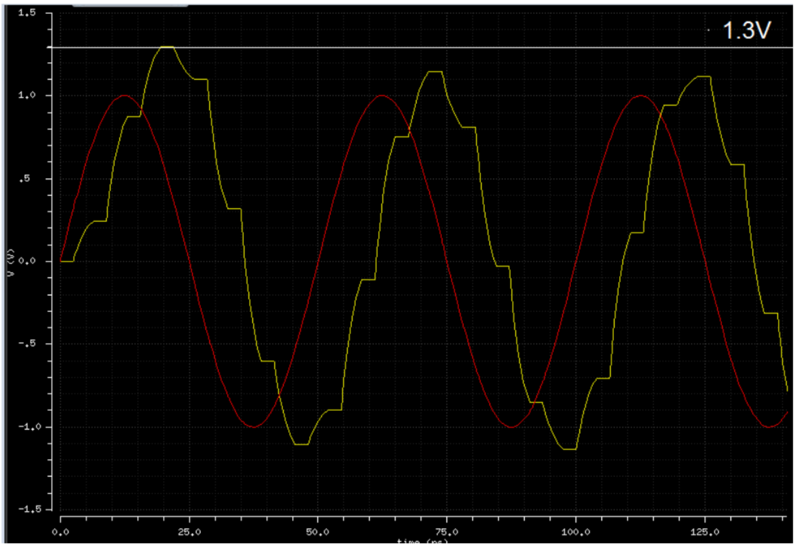


Figure 9. time domain simulations for ideal OTA.

F. Settling time and dynamic settling

The setting time was calculated by 1/2fs which is 3.33 ns and my simulation results shows 2.446 ns.

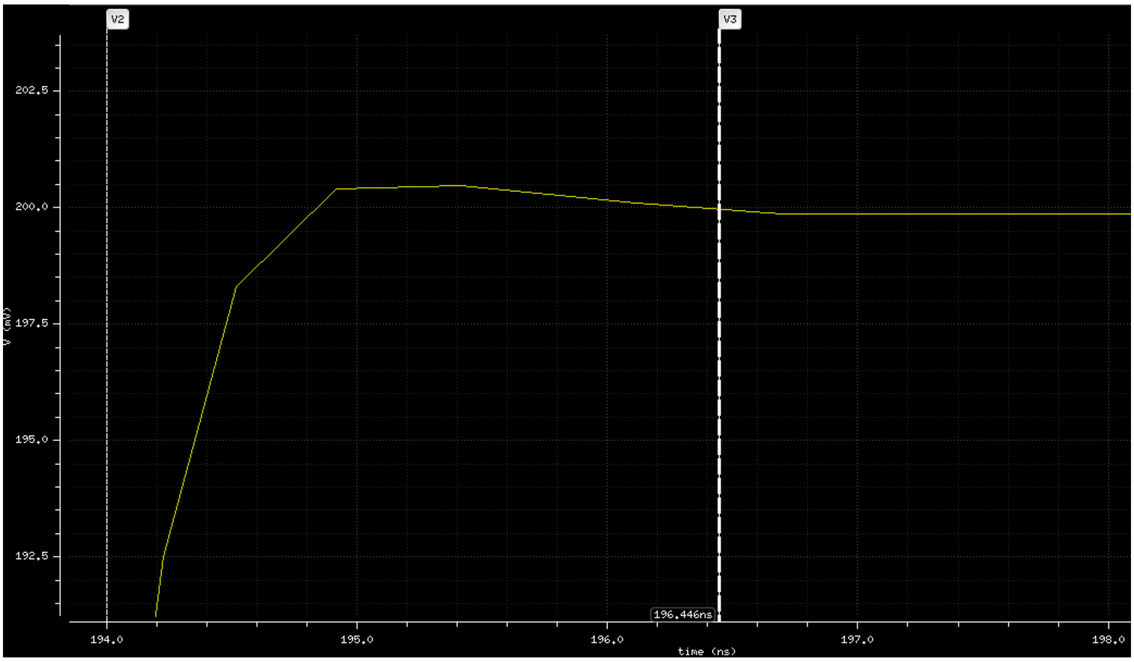


Figure 10. Settling time and dynamic settling error.

G. Dynamic range

The dynamic range was calculated by getting the vopp^2 divided by v2ot which equals to 73.2 db.

$$Dynamic\ Range = 10log_{10}\left(\frac{839.2983mV^2}{184.07757uV^2}\right)$$
$$= 73.2db$$

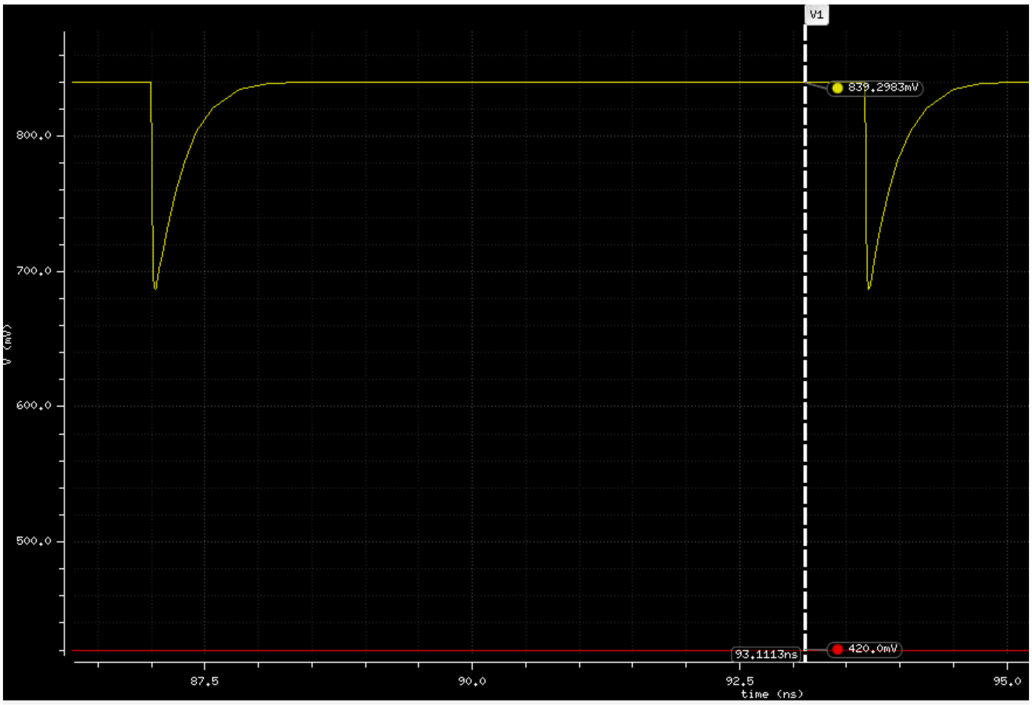


Figure 11. Dynamic range.

The current drawn from the design was 8.5mA which is considerably low against previous iterations of my design.

IV. DISCREPANCIES, ISSUES WITH REQUIREMENTS AND FUTURE WORK

Parameter	Value
Input amplitude (differential)	2V peak-to-peak
3-dB bandwidth	10 MHz
Sampling frequency f_s	150 MHz
Static settling error	<0.1%
Dynamic settling error	<0.05%
Dynamic range at output	80 dB
Temperature (all simulations)	100 °C
Power dissipation	Minimum

In this section I will compare each parameter that was a requirement for this project with my calculations/simulations.

Input amplitude (2V peak to peak):

I did not met this parameter because of two reasons:

1. my top and bottom branch of my folded cascode reduced my output swing to nearly 1.6v peak to peak thus directly proportional affecting my input swing since I can not longer achieve 2v peak to peak at the input without getting my output hit a max or min. I was aware of this issue but the plan was to have two stages. This decision was discarded due to time constraint and issues setting up the second stage with the extra CMFB.

2. I killed my input swing by increasing my gain to two… further decreasing my input swing to the point of making it 800mV peak to peak. This was a mistake that I was planning to fix at the end but I encounter issues with my OTA that forced me to deal with that later… which I never did. Nevertheless, it would have been an easy change that affects CLTOT, beta, and Id.

   I believe in order to meet this requirement and still not fall short on the rest of the requirements was to have a second stage which would have given me in return a high gain, the highest output swing out of the different topologies discussed in this paper, a reasonable power dissipation.

   3-db bandwidth = 10MHz
   was met in both my simulation and calculations.

Static setting error <0.1%

This part of the design was met by both OTA and calculations. My transistor made OTA was nearly out of spec because I was having issues reaching a good open loop gain with the folded cascode OTA.

Dynamic settling error < 0.05%

$$t_s = \frac{1}{2fs} = \sim 3ns$$

My simulation exceeded the expectations on the settling time.

For the switches part I decided to use ideal switches with added resistance in series due to time constraint I wanted to concentrate on figuring out why my OTA wasn't working and how to fix it. A typical switch could have been implemented by using a transmission gate with enough a good ratio approximation of 1:3 from nmos to pmos width.

Conclusion:

This project increased my understanding on how the performance parameters are affected. For example, I realized that increasing bias currents increases the transistor sizes which helps with device mismatch for real transistor application which proportionally affects the power consumption. Another thing I would have considered to be different was to use PMOS as input pair because from the research I did, PMOS is affected less than NMOS in regards to flicker noise. All design equations were gathered from the lectures.