Modeling and Control of Resonant Switched Capacitor DC-DC Converter

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by Yongjun Li

Research Project

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Abstract

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Present-day mobile platforms call for a compact power management solution due to the necessity of packing ever increasing functionality into a very constrained form factor. The conventional buck/boost converter suffers from bulky magnetics with its compromise between the size of passives and the performance. The emerging switched-capacitor (SC) converter shows great potential for a fully integrated solution with the on-die capacitor. However, the intrinsic charge sharing in a SC converter leads to an efficiency and power density trade-off which inhibits its application in the battery powered devices that demands more than a few watts. In addition, a SC converter is only efficient at a discrete conversion ratio determined by its topology. The voltage regulation over a wide range usually comes at the cost of efficiency degradation.

As a way to mitigate the limitation of the inductor-based and switched-capacitor based converter, we explore the resonant switched capacitor (ResSC) topology as a hybrid approach. The ResSC topology can utilize the favorable on-die capacitor for tight integration while leveraging a small inductor to eliminate the intrinsic charge sharing. This enables higher power density without efficiency compromise along with lossless regulation. The introduced inductance is much less than that needed in the common buck/boost converter.

In order to facilitate the design and control of a ResSC converter, the harmonic-balance method is adopted for developing its large signal and small signal models. A current-phase based compensation scheme based on the small signal model is developed to enable a fast transient response. The effectiveness of topology concept, modeling and control are verified by the switched-based simulation in a design example for on-chip power delivery.

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Chapter 1

Introduction

The platform limitation in most portable electronics drives the demand for a compact and efficient power conversion stage that delivers energy from the Lithium-ion (Li-ion) battery to multiple functional blocks. The commonly-used buck/boost converter rely on bulky inductors which take a large amount of board area. Though increasing switching frequency can help reduce the size of passives including the inductors, the benefits are limited due to performance degradation that comes from the increased switching losses.

On the other hand, switched-capacitor (SC) based power converters have shown great promise for enabling fully-integrated power management solution, due to the favorable high energy density of on-chip capacitors [1] [2] [3]. However, the power density in a standard switched capacitor converter is limited by the available capacitor density of a given technology, along with the trade-off with efficiency due to the intrinsic charge sharing loss.

Recently, resonant switched-capacitor (ResSC) based converters have been proposed as an approach that can mitigate the intrinsic charge-sharing loss in SC operation by introducing a small inductor in series with the flying capacitor [4] [5]. By avoiding charge sharing losses, substantially larger voltage swings can be sustained on the working capacitors, which enables increased power density while not compromising efficiency. Therefore, this approach enables converters with higher efficiency and power density for the fully or near-fully integrated designs.

In addition, by strategically designing the switch gating pattern, lossless voltage regulation of the ResSC converter can be enabled. To date, some regulation methods have been proposed for the ResSC converter [6] [7] [8] [9]. By decoupling the phase control of two stacked sections of the ResSC circuit, lossless voltage regulation is enabled [10]. With this modality, the circuit can best be viewed as a stacked series resonant converter. Thus, the well known control methodologies based on frequency tuning, phase-shifting, and/or phase-plane can be brought to bear on the problem. In order to effect nominally lossless zero-voltage switching, operation above resonance is maintained, in conjunction with properly adjusted deadtimes. Parasitic capacitances associated with devices, flying capacitor bottom and top plates, and inductor capacitances constitute the contributing components to potential dynamic switching losses.

In order to expand the application of integrated ResSC dc-dc converters to directly bridge the battery voltage or a high dc bus voltage in the mobile or PC platforms, a stacked topology that enables higher conversion ratios is also developed [11]. The topology can be extended to any N-to-1 conversion with reduced switch stress, which enables the use of standard CMOS technology, and only a single inductor. To further reduce voltage ripple or the required bypass capacitors, multi-phase interleaving can be employed.

In this thesis, the author develops the framework of designing an analog control based on the small signal model. The steady state operation of a ladder type 2-to-1 ResSC is first analyzed. Operation above resonance is presumed to effect zero voltage switching (ZVS). Based on the generalized averaging method [12], the state space small signal model of the converter is derived. According to the dynamics of the model, the author further develops a compensation method relying on a phase feedback loop. The switch-based simulations show the effectiveness of the developed model and proposed regulation scheme.

Chapter 2

Large Signal Model of Resonant Switched Capacitor Converter

In this chapter, we start with the basic operation of a 2-to-1 ResSC converter and apply the generalized averaging methods to obtain the large signal model. The large signal model can be illustrated with the phasor diagrams which facilitate the derivation of the zero voltage switching (ZVS) conditions for the topology.

2.1 Topology Overview and Principle Operation

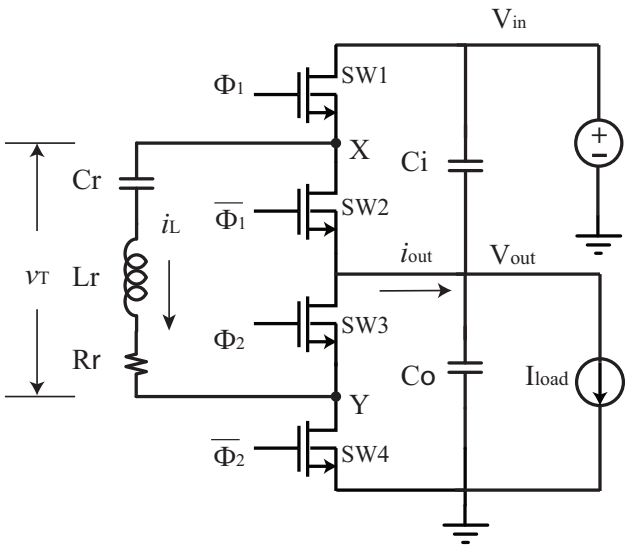

Figure 2.1: A Ladder Type 2-to-1 Resonant Switched-capacitor DC-DC Converter

A ladder type 2-to-1 resonant switched-capacitor converter is shown in Fig. 2.1. C_r and L_r form the resonant tank. C_i and C_o are decoupling capacitors. R_r represents all the series

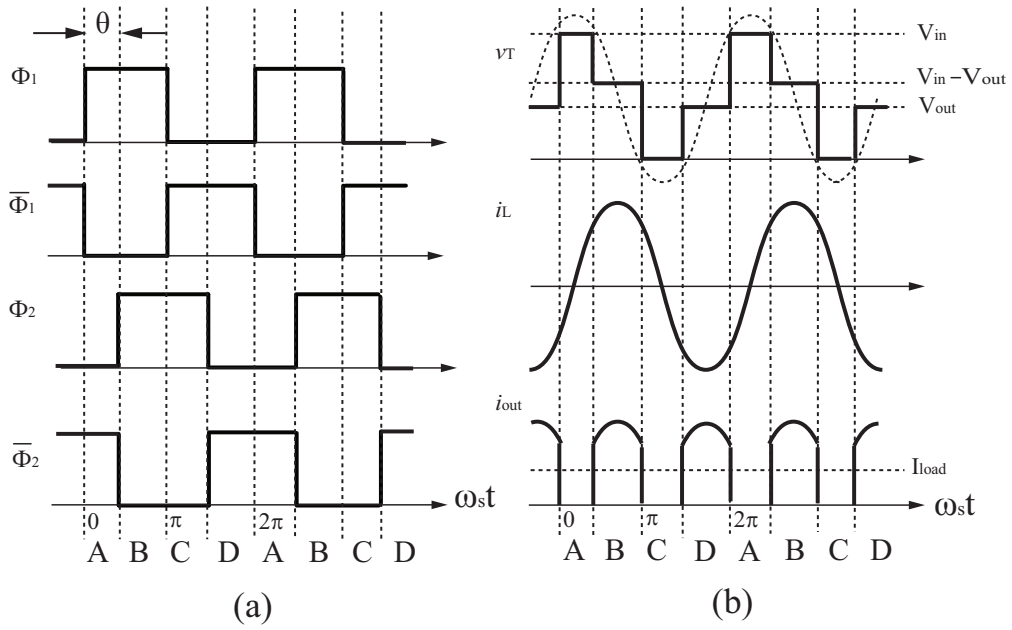

Figure 2.2: (a) Switch Gating Patterns of the ResSC (b) Waveforms of the Tank Voltage, Inductor Current and Output Current

resistance within the tank which includes the switch resistance, and the ESR of the inductor and capacitors. There are two complementary switch pairs SW_1/SW_2 and SW_3/SW_4. Each switch pair is driven by a square wave with 50% duty cycle. The switching of SW_1/SW_2 leads that of SW_3/SW_4 by a phase angle of θ. Fig. 2.2(a) shows the gating signals for each switch. With this switching pattern, the converter has four different switch states: A, B, C, and D, as shown in Fig. 2.3. Fig. 2.2(b) shows the representative waveforms of the tank voltage v_T, the inductor current i_L and the output current i_{out}, when the converter operates above the resonating frequency set by C_r and L_r.

One benefit of the proposed ResSC operation is that all switches can potentially realize zero voltage switching (ZVS), which helps to improve converter efficiency. To achieve that, the tank current i_L needs to flow into node X and out of node Y before turning SW_1 or SW_4 on, in which case I_L needs to be negative given reference direction defined in Fig. 2.1. Similarly, a positive tank current favors the soft turn-on of both SW_3 and SW_2. By operating the converter under the proposed switching sequence above resonance, all switches can meet the ZVS requirement.

However, this condition is not true for all possible operation points. In order to benefit from the ZVS, the zero crossing of the tank current should be constrained within the interval set by switching actions of the top switch pair and the bottom switch pair. This leads to an acceptable output range with ZVS for the proposed operation, which will be illustrated in Section 2.2 after the phasor model is introduced.

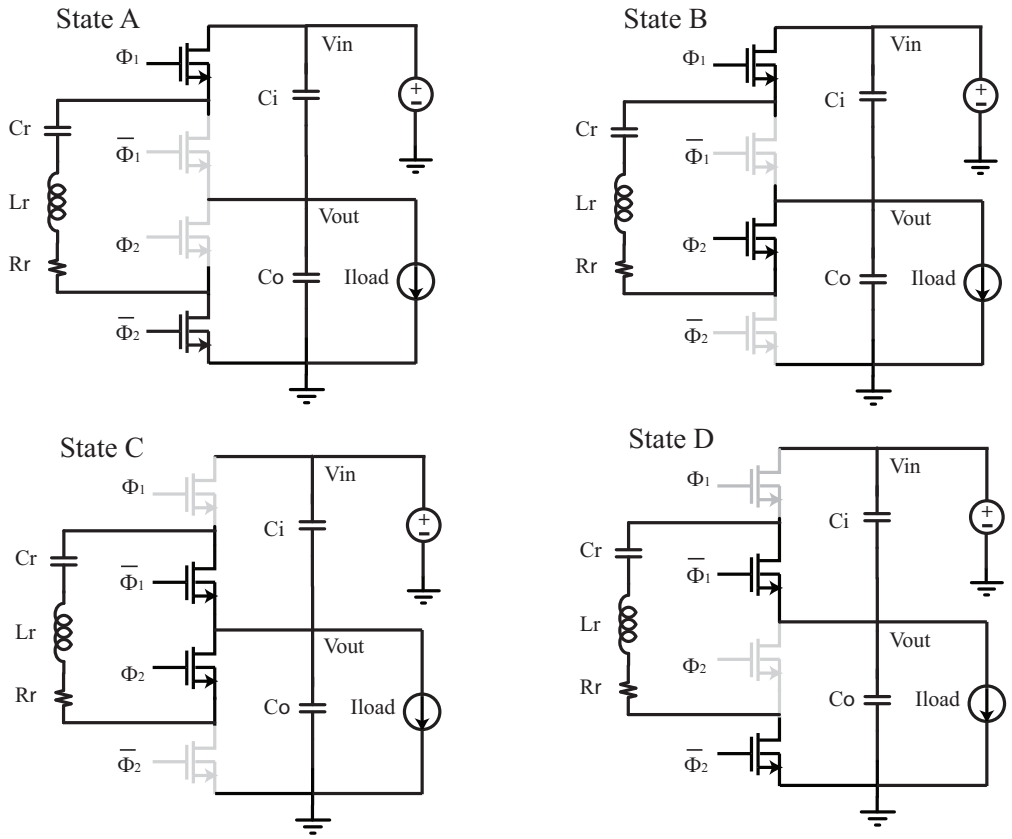

Figure 2.3: Different States of the ResSC

2.2 Large Signal Model

Fig. 2.4(a) shows a simplified circuit model of the resonant converter in Fig. 2.1. Equivalently we can view the system as an LCR tank driven by two square waves V_s and V_o at nodes X and Y. Assuming the Q of the tank is high, as enforced by design, we can further simplify the system by considering only the fundamental sinusoidal components of the square waves and use phasors to describe the system.

In Fig. 2.4(b)(c)(d), $\overrightarrow{V_X}$ and $\overrightarrow{V_Y}$ represent the fundamental phasors of the two driving signals v_s and v_o. The magnitudes of $\overrightarrow{V_X}$ and $\overrightarrow{V_Y}$ determined by:

$$\begin{aligned} \| \overrightarrow{V_X} \| &= \frac{2}{\pi}(V_{in} - V_{out}) \\ \| \overrightarrow{V_Y} \| &= \frac{2}{\pi}V_{out} \end{aligned} \tag{2.1}$$

$\overrightarrow{V_X}$ leads $\overrightarrow{V_Y}$ by a fixed phase angle of θ. $\overrightarrow{V_T}$ represents the phasor of the tank voltage which is the difference between $\overrightarrow{V_X}$ and $\overrightarrow{V_Y}$. $\overrightarrow{I_L}$ represents the phasor of inductor current

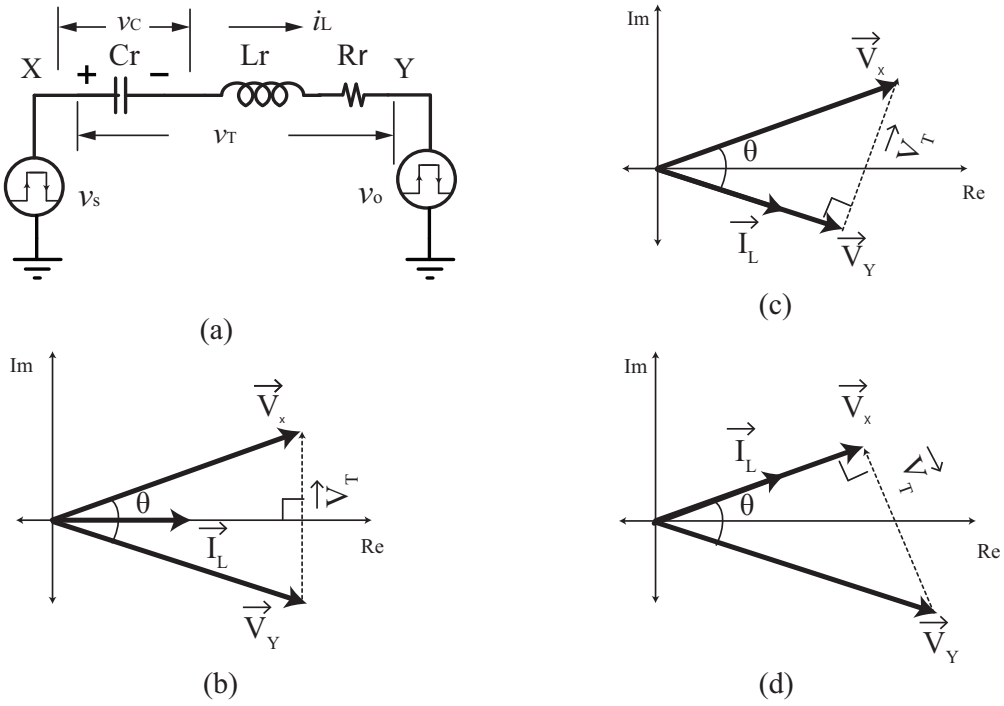

Figure 2.4: Large Signal Phasor Model of the ResSC

which should be perpendicular to the tank voltage phasor under high Q assumption and above-resonance operation. Phase angle θ is a design parameter, selected based on the desired voltage regulation range, and efficiency considerations.

As discussed above, in order to benefit from ZVS operation, the zero crossing of the current i_L should happen between the switching actions of SW_1 and SW_3. In the phasor domain, this means the tank current phasor $\overrightarrow{i_L}$ should be contained within the phase angle set by phasor $\overrightarrow{V_Y}$ and phasor $\overrightarrow{V_X}$.

Nominally for a 2-to-1 converter, V_{out} equals half of V_{in}. In this case, $\overrightarrow{V_X}$ and $\overrightarrow{V_Y}$ have the same magnitude such that the current phasor is aligned in the middle of the phase angle θ as shown in Fig. 2.4(b). However, as the output voltage is modulated, the magnitude of $\overrightarrow{V_X}$ and $\overrightarrow{V_Y}$ adjust. This leads to the movement of the position of the current phasor according to the geometrical property of the triangle. As the output voltage decreases, the current phasor $\overrightarrow{I_L}$ moves closer to $\overrightarrow{V_X}$. Therefore, the minimum output voltage with ZVS occurs when the tank current is aligned with $\overrightarrow{V_X}$, as shown in Fig. 2.4(c). Similarly, the case of maximum output voltage happens when the tank current is aligned with $\overrightarrow{V_Y}$, as shown in Fig. 2.4(d). From the geometry of the right triangle, the ideal output voltage range with ZVS is therefore given by:

$$\frac{V_{in}\cos\theta}{1+\cos\theta} < V_{out} < \frac{V_{in}}{1+\cos\theta} \tag{2.2}$$

We can see that the output range with ZVS can be adjusted by properly choosing θ. This offers the major benefit of the resonant switched-capacitor converter over conventional switched-capacitor converter, since the latter sacrifices efficiency to achieve the regulation of the output voltage. In the design example for V_{in}=2V and a 2-to-1 topology, with $\theta = \frac{\pi}{4}$, the output can be losslessly adjusted from 0.83 to 1.17. As can be seen, a larger angle θ result in a greater adjustment range, but at the cost of degraded power factor at sending and receiving nodes with attendant efficiency costs.

To obtain an analytic expression for the steady state operation, we apply the generalized averaging method [12] to the state-space equations of the converter which read:

$$\begin{aligned}
\frac{di_L}{dt} &= \frac{1}{L_r}[(V_{in} - v_{out})s_i - v_{out}s_o + v_{out} - i_L R_r - v_c] \\
\frac{dv_C}{dt} &= \frac{1}{C_r} i_L \\
\frac{dv_{out}}{dt} &= \frac{1}{C_o}[s_o s_i i_L - (1 - s_i)(1 - s_o) i_L - I_{load}]
\end{aligned} \tag{2.3}$$

where s_i and s_o represent the switching functions of $SW1$ and $SW3$, which take the form:

$$\begin{aligned}
s_i &= \frac{1}{2}\{sign[sin(\omega t)] + 1\} \\
s_o &= \frac{1}{2}\{sign[sin(\omega t - \theta)] + 1\}
\end{aligned} \tag{2.4}$$

Applying operator $\langle \bullet \rangle_1$ to the i_L and v_C state equations and operator $\langle \bullet \rangle_0$ to the v_{out} state equation, we obtain:

$$\begin{aligned}
\frac{d\langle i_L \rangle_1}{dt} &= -j\omega \langle i_L \rangle_1 + \frac{1}{L_r}[(V_{in} - \langle v_{out} \rangle_0)\langle s_i \rangle_1 - \langle v_{out} \rangle_0 \langle s_o \rangle_1 - \langle i_L \rangle_1 R_r - \langle v_C \rangle_1] \\
\frac{d\langle v_C \rangle_1}{dt} &= -j\omega \langle v_C \rangle_1 + \frac{1}{C_r}\langle i_L \rangle_1 \\
\frac{d\langle v_{out} \rangle_0}{dt} &= \frac{1}{C_o}(\langle s_o \rangle_{-1}\langle i_L \rangle_1 + \langle s_o \rangle_1 \langle i_L \rangle_{-1} + \langle s_i \rangle_{-1}\langle i_L \rangle_1 + \langle s_i \rangle_1 \langle i_L \rangle_1 - I_{load})
\end{aligned} \tag{2.5}$$

where $\langle \bullet \rangle_k$ represent the kth order complex Fourier coefficient, which is also equivalent to the phasor transformation in [13]. Using high Q assumption and neglecting the output voltage ripple, the first order Fourier coefficient $\langle i_L \rangle_1$ and $\langle v_C \rangle_1$ and the zero order Fourier coefficient $\langle v_{out} \rangle_0$, which is real, capture the most significant properties of the tank and the output. We then decompose the complex coefficients into their real and imaginary parts

$$\begin{aligned}
\langle i_L \rangle_1 &= \frac{1}{2} X_{i_L} + j\frac{1}{2} Y_{i_L} \\
\langle v_C \rangle_1 &= \frac{1}{2} X_{v_C} + j\frac{1}{2} Y_{v_C}
\end{aligned} \tag{2.6}$$

where X_{i_L} and Y_{i_L}, X_{v_C} and Y_{v_C} also represent the real and imaginary parts of the resonant inductor current and capacitor voltage in the complex phasor domain.

Applying operator $\langle\bullet\rangle_1$ to the switching functions, we have:

$$\begin{aligned}\langle s_i\rangle_1 &= -j\frac{1}{\pi}\\ \langle s_o\rangle_1 &= -j\frac{1}{\pi}e^{-j\theta}\end{aligned} \tag{2.7}$$

Then the real-valued fifth order state space equations are obtained:

$$\begin{aligned}\frac{dX_{i_L}}{dt} &= -\frac{R_r}{L_r}X_{i_L} + \omega Y_{i_L} - \frac{1}{L_r}X_{v_C} + \frac{1}{L_r}\frac{2}{\pi}sin\theta V_{out}\\ \frac{dY_{i_L}}{dt} &= -\omega X_{i_L} - \frac{R_r}{L_r}Y_{i_L} - \frac{1}{L_r}Y_{v_C} + \frac{1}{L_r}\frac{2}{\pi}(1+cos\theta)V_{out} - \frac{1}{L_r}\frac{2}{\pi}V_{in}\\ \frac{dX_{v_C}}{dt} &= \frac{1}{Cr}X_{i_L} + \omega Y_{v_C}\\ \frac{dY_{v_C}}{dt} &= -\omega X_{v_C} + \frac{1}{Cr}Y_{i_L}\\ \frac{dV_o}{dt} &= \frac{1}{C_o}[-\frac{1}{\pi}sin\theta X_{i_L} - \frac{1}{\pi}(1+cos\theta)Y_{i_L}) - I_{load}]\end{aligned} \tag{2.8}$$

To obtain the steady state, we have:

$$\begin{aligned}\frac{dX_{i_L}}{dt} &= 0\\ \frac{dY_{i_L}}{dt} &= 0\\ \frac{dX_{v_C}}{dt} &= 0\\ \frac{dY_{v_C}}{dt} &= 0\\ \frac{dV_o}{dt} &= 0\end{aligned} \tag{2.9}$$

so that we can solve:

$$I_{load} = -\frac{1}{\pi}\frac{\frac{2}{\pi}\omega C_r}{(1-\frac{\omega^2}{\omega_o^2})^2 + (\frac{\omega}{\omega_o Q})^2}[sin\theta(1-\frac{\omega^2}{\omega_o^2})V_{in} - (1+cos\theta)\frac{\omega}{\omega_o Q}(V_{in}-2V_o)] \tag{2.10}$$

with

$$\begin{aligned}\omega_o &= \frac{1}{\sqrt{LrC_r}}\\ Q &= \frac{\sqrt{\frac{L_r}{C_r}}}{R_r}\end{aligned} \tag{2.11}$$

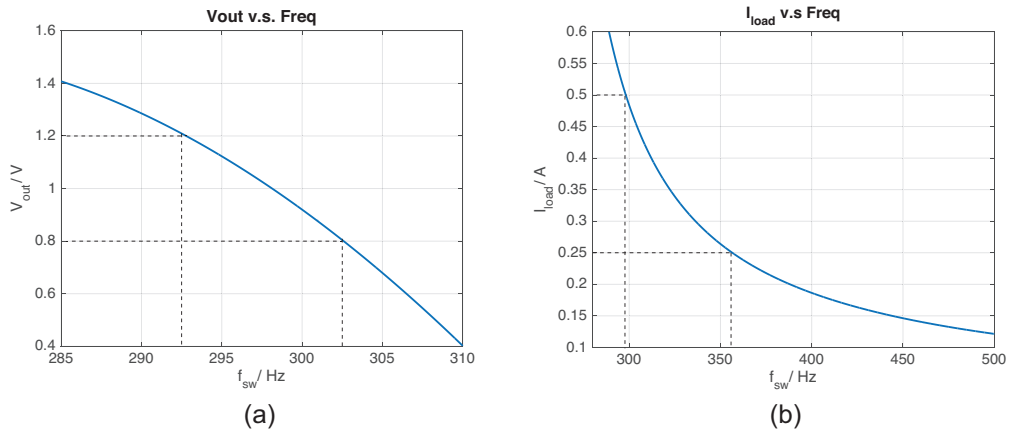

Figure 2.5: Steady state operation points with V_{in}=2V, $\theta = \pi/4$, $L_r = 1nH$, $C_r = 405pF$, $R_r = 25m\Omega$, $C_o = 10nF$ for (a) $I_{load} = 500mA$ and (b) $V_{out} = 1V$

From Eq. 2.10, the operating point of the converter can be uniquely determined given certain V_{in}, θ. The proposed method uses the switching frequency ω as the tuning parameter for the output voltage regulation under varying load and set-point commands. The phase angle is chosen for the expected output range and is not tuned dynamically.

Consider a reasonably achievable design example for the chip-level power delivery application with $L_r = 1nH, C_r = 405pF, R_r = 25m\Omega, C_o = 10nF$, a set of operating points according to Eq. 2.10 are plotted in Fig. 2.5. Given certain load condition, modulating frequency can regulate the output voltage. In the design example, a 3% frequency change can cover a voltage regulation range of 40%. In terms of load regulation, the frequency range has to be large enough to support the extreme light load condition. In this case, the efficiency will drop due to the increased switching loss. However, to alleviate this scenario, the burst operation can be introduced to improve the light load efficiency.

Chapter 3

Small Signal Model and Control Strategy of Resonant Switched Capacitor Converter

In this chapter, the small signal model is further developed following the large signal model. The system dynamics are revealed by the transfer functions derived from the small signal model. A fast compensation method assisted with the phase information of the current is proposed and validated through the simulation.

3.1 Small Signal Model

To obtain the small signal model, we apply the small signal perturbation to Eq. 2.8 with the state variables taken as:

$$\begin{aligned} x_{i_L} &= X_{i_L} + \hat{x}_{i_L} \\ y_{i_L} &= Y_{i_L} + \hat{y}_{i_L} \\ x_{v_C} &= X_{v_C} + \hat{x}_{v_C} \\ y_{v_C} &= Y_{v_C} + \hat{y}_{v_C} \\ v_o &= V_o + \hat{v}_o \end{aligned} \tag{3.1}$$

and the input variables taken as:

$$\begin{aligned} \omega &= \Omega + \hat{\omega} \\ i_{load} &= I_{load} + \hat{i}_{load} \end{aligned} \tag{3.2}$$

The output variables that we are interested in are $\hat{v}_o$, $\parallel \hat{i_L} \parallel$ and $\hat{\phi}_{i_L}$. With

$$\begin{aligned} \parallel \hat{i_L} \parallel &= \sqrt{(X_{i_L} + \hat{x}_{i_L})^2 + (Y_{i_L} + \hat{y}_{i_L})^2} - \sqrt{X_{i_L}^2 + Y_{i_L}^2} \\ \hat{\phi}_{i_L} \approx \hat{\phi}_{i_L} &= tan(\phi_{i_L + \hat{i}_L} - \phi_{i_L}) = \frac{tan\phi_{i_L + \hat{i}_L} - tan\phi_{i_L}}{1 + tan\phi_{i_L + \hat{i}_L} tan\phi_{i_L}} \end{aligned} \tag{3.3}$$

we can obtain:

$$\begin{aligned} \| \hat{i_L} \| &= \frac{X_{i_L}\hat{x}_{i_L} + Y_{i_L}\hat{y}_{i_L}}{\| i_L \|} \\ \hat{\phi}_{i_L} &= \frac{-Y_{i_L}\hat{x}_{i_L} + X_{i_L}\hat{y}_{i_L}}{\| i_L \|^2} \end{aligned} \tag{3.4}$$

Then the real-valued fifth-order small signal state space matrix is obtained as Eq. 3.5.

$$\begin{bmatrix} \frac{d\hat{x}_{i_L}}{dt} \\ \frac{d\hat{y}_{i_L}}{dt} \\ \frac{d\hat{x}_{v_C}}{dt} \\ \frac{d\hat{y}_{v_C}}{dt} \\ \frac{d\hat{v}_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_r}{L_r} & \Omega & -\frac{1}{L_r} & 0 & \frac{1}{L_r}\frac{2}{\pi}\sin\theta \\ -\Omega & -\frac{R_r}{L_r} & 0 & -\frac{1}{L_r} & \frac{1}{L_r}\frac{2}{\pi}(1+\cos\theta) \\ \frac{1}{C_r} & 0 & 0 & \Omega & 0 \\ 0 & \frac{1}{C_r} & -\Omega & 0 & 0 \\ -\frac{1}{C_o}\frac{1}{\pi}\sin\theta & -\frac{1}{C_o}\frac{1}{\pi}(1+\cos\theta) & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} Y_{i_L} & 0 \\ -X_{i_L} & 0 \\ Y_{v_C} & 0 \\ -X_{v_C} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \begin{bmatrix} \hat{\omega} \\ \hat{i}_{load} \end{bmatrix}$$

$$\begin{bmatrix} \hat{v}_o \\ \| \hat{i_L} \| \\ \hat{\phi}_{i_L} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ \frac{X_{i_L}}{\|i_L\|} & \frac{Y_{i_L}}{\|i_L\|} & 0 & 0 & 0 \\ -\frac{Y_{i_L}}{\|i_L\|^2} & \frac{X_{i_L}}{\|i_L\|^2} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} \tag{3.5}$$

For a convenient presentation, Eq.3.5 is rewritten as:

$$\begin{aligned} \begin{bmatrix} \frac{d\hat{x}_{i_L}}{dt} \\ \frac{d\hat{y}_{i_L}}{dt} \\ \frac{d\hat{x}_{v_C}}{dt} \\ \frac{d\hat{y}_{v_C}}{dt} \\ \frac{d\hat{v}_o}{dt} \end{bmatrix} &= \mathbf{A} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} \mathbf{B}_\omega & \mathbf{B}_{i_{load}} \end{bmatrix} \begin{bmatrix} \hat{\omega} \\ \hat{i}_{load} \end{bmatrix} \\ \begin{bmatrix} \hat{v}_o \\ \| \hat{i_L} \| \\ \hat{\phi}_{i_L} \end{bmatrix} &= \begin{bmatrix} \mathbf{C}_{v_o} \\ \mathbf{C}_{\|i_L\|} \\ \mathbf{C}_\phi \end{bmatrix} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} \end{aligned} \tag{3.6}$$

Based on Eq. 3.6, the small signal transfer functions from the switching frequency to the output voltage magnitude ($\| H \|_{\omega \to v_o}$) and frequency to the resonant current properties ($\| H \|_{\omega \to \|i_L\|}$ and $\| H \|_{\omega \to \phi}$) are evaluated based on:

$$\begin{aligned} \| H \|_{\omega \to v_o} &= \mathbf{C}_{v_o}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_\omega \\ \| H \|_{\omega \to \|i_L\|} &= \mathbf{C}_{\|i_L\|}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_\omega \\ \| H \|_{\omega \to \phi} &= \mathbf{C}_\phi(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_\omega \end{aligned} \tag{3.7}$$

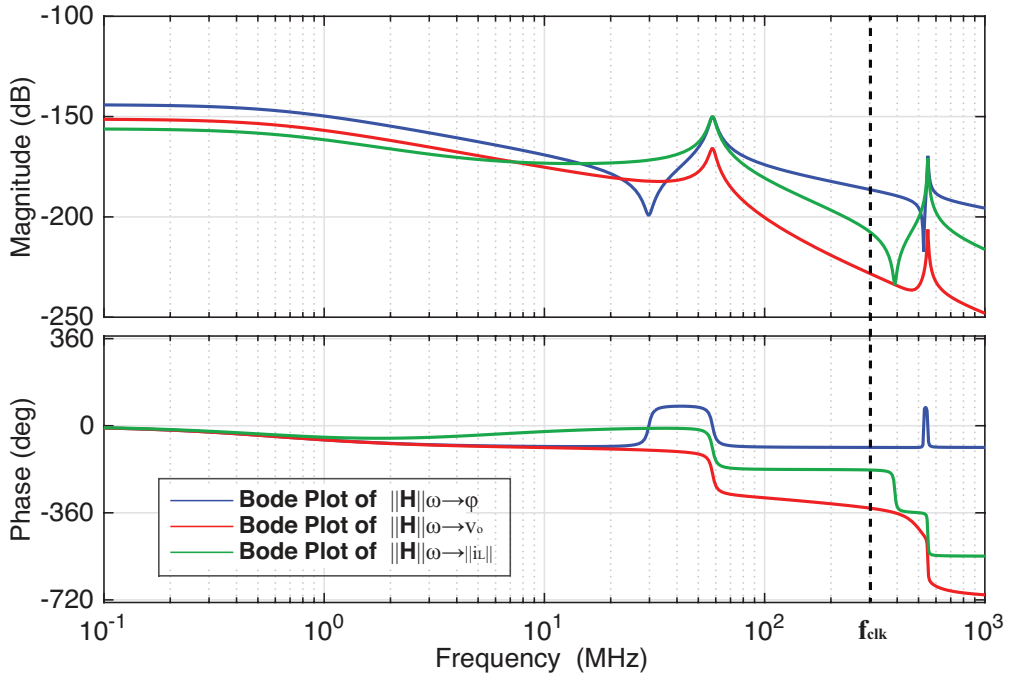

Figure 3.1: Bode Plot of $H_{\omega\to\phi}$, $H_{\omega\to v_o}$ and $H_{\omega\to\|i_L\|}$

Using the design example in Chapter 2 with $L_r = 1nH, C_r = 405pF, R_r = 25m\Omega, C_o = 10nF$ and according to Eq. 2.10, a set of operating point is given by $f_{clk} = 300MHz, V_{in} = 2V, V_{out} = 1V, I_{load} = 500mA, \theta = \pi/4$. With the design parameters and the operating point, the Bode plots of the transfer functions are plotted in Fig. 3.1. We can see from the Bode plot of $H_{\omega\to v_o}$ that there is a dominant pole introduced by the output capacitor, contributing a 90° phase lag and magnitude drop, followed by two complex conjugate poles, contributing another 180° phase lag and a large resonant peak in the magnitude response around 50MHz. This makes it challenging to do compensation with a pure voltage loop at a high crossover frequency. However, looking at the transfer function of $H_{\omega\to\phi}$, a 180° phase lead, thanks to the complex conjugate zeros at a lower frequency than the resonant poles, is present. Therefore, we take advantage of the phase lead in the current phase transfer function by adding in a phase loop to stabilize the system as shown in Fig. 3.2. The degree of compensation can be adjusted by properly choosing respective gains of the phase loop and voltage loop. Furthermore, a proportion-integral (PI) voltage loop can be used for reduction of the DC error.

3.2 Simulation Verification

To verify the small signal model and proposed control methodology. We implement the converter and control loop using the switch model based simulator PLECS. The small signal

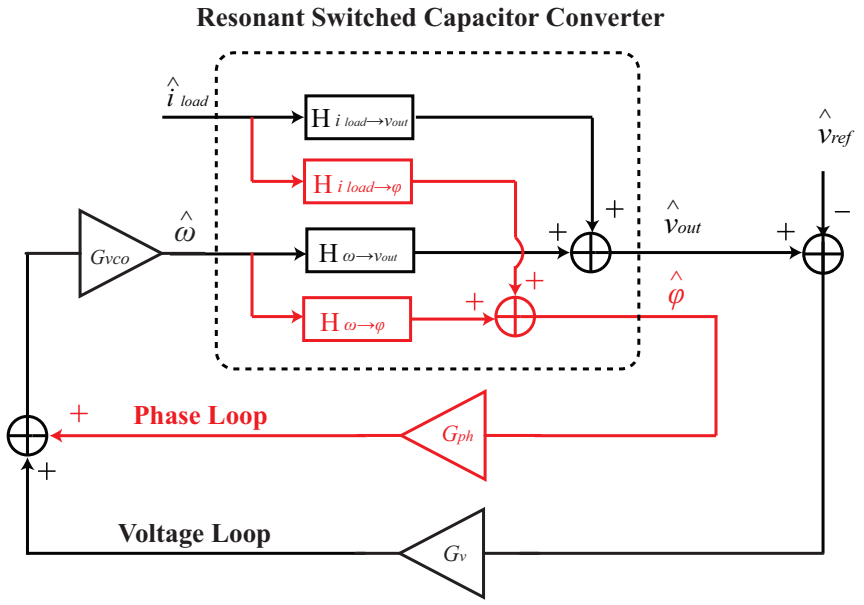

Figure 3.2: Small Signal Block Diagram of Close Loop System

signal dynamics of the converter are verified with the open loop simulation. Fig. 3.3 shows the dynamic response of the output voltage and current phase under a frequency step of $1MHz$, we see that circuit simulation match the developed small signal model very well.

In order to implement the phase loop, we use a passive phase sensing scheme as shown in Fig. 3.4. The R_s and C_s form a passive lossless current sensor. With the matched time constants of $R_s \cdot C_s$ and L_r/R_r, the voltage across C_s (V_s) replicates the voltage drop on the parasitic resistance of the inductor. Moreover, as the inductor frequency is much higher than the corner frequency set by L_r/R_r, a slight mismatch of the time constants would not result in any significant error in the phase information captured by V_s. V_s is then mixed with a reference clock through an H-bridge. Fig. 3.5 shows the waveform of the reference clock (Φ_3), V_s and V_{ph}. The reference clock (Φ_3) is shifted 90° ahead relative to the middle of the top (Φ_1) and bottom clock(Φ_2) for high sensitivity. The DC component of the output (V_{ph}) from the mixer approximates the phase error if the phase error is small:

$$\langle V_{ph}\rangle_0 = \parallel I_L R_r \parallel \frac{2}{\pi} sin\theta \approx \parallel I_L R_r \parallel \frac{2}{\pi}\theta \tag{3.8}$$

The scaling effect caused by the current magnitude is accounted for in the gain of G_{ph}. The design here can be extended as one phase leg of a multi-phase converter.

With the developed small signal mode, a control design with proposed dual loop is pre-

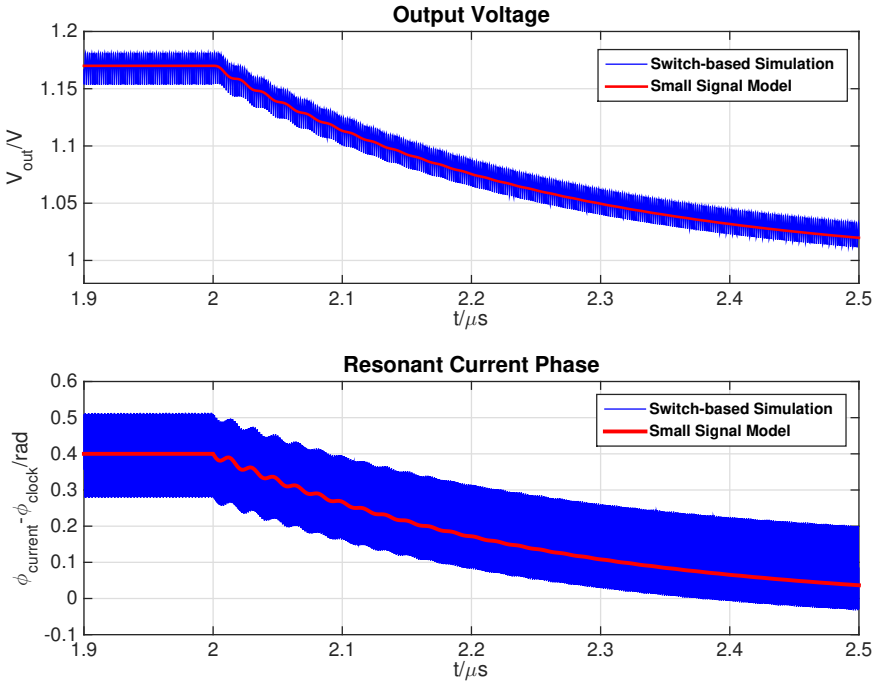

Figure 3.3: Open Loop Comparison of Small Signal Model and Switch Based Simulation

sented

$$G_{ph}(s) = G_1 \frac{1}{1+\frac{s}{p}}$$
$$G_v(s) = G_2 \frac{s+z}{s} \tag{3.9}$$

where, $G_1 = 4, G_2 = \frac{1}{10}, p = 1.01e8, z = 6.28e8$. The low pass filter in the phase loop is used for reducing the high frequency harmonics of the phase error. In a multi-phase system, the low pass filter can be eliminated due to the harmonics cancellation from interleaving. The voltage loop consists of a simple PI controller for the management of DC error. The gains of phase and voltage loops are selected so that closed-loop sytem is stable and well compensated. Fig. 3.6 shows the closed-loop transient response of the voltage output under a $50mA$ load step. The overshoot and response time from the switch based circuit simulation match well with the prediction from the developed small signal model.

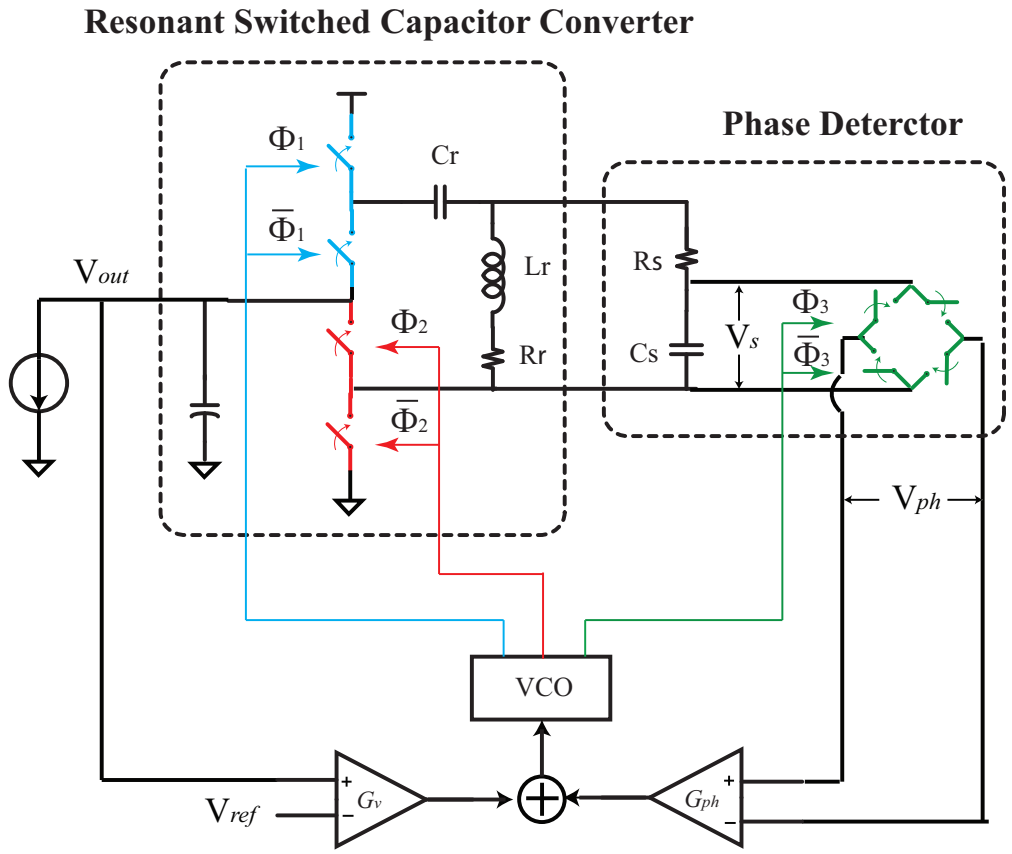

Figure 3.4: Circuit Implementation of the Close Loop Resonant Switch Capacitor Converter

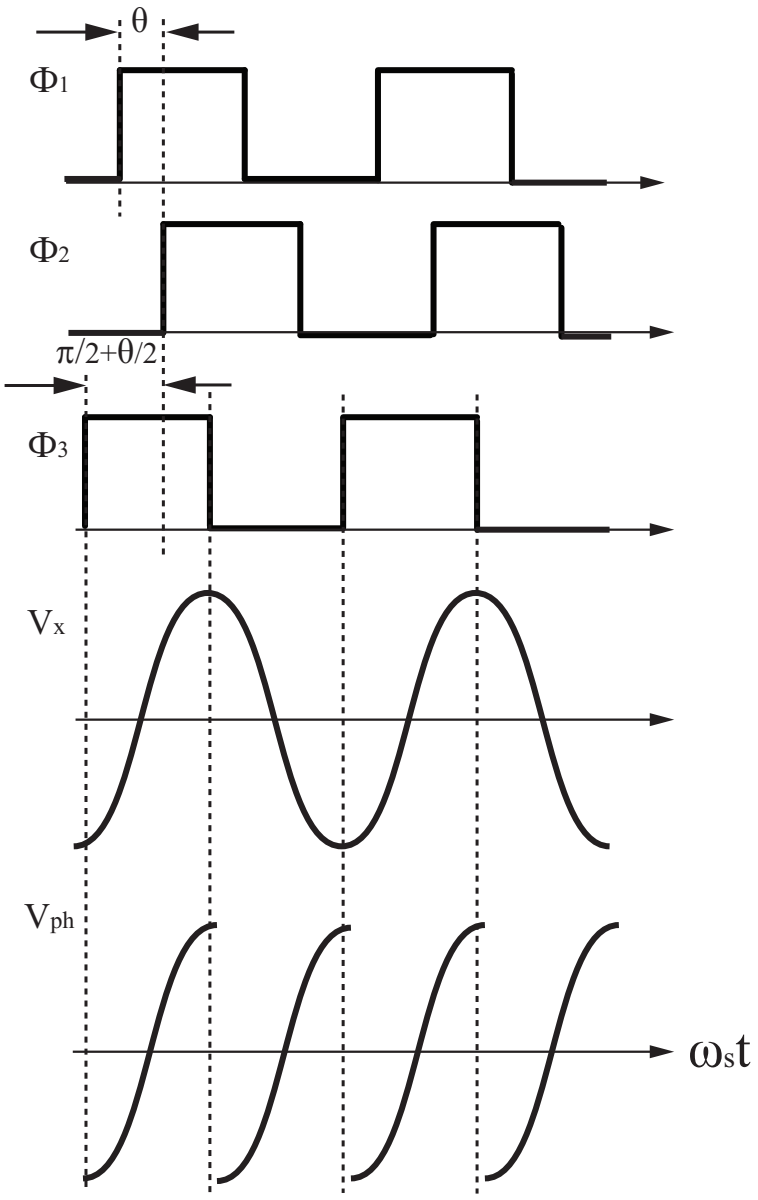

Figure 3.5: Waveform of Phase Detector

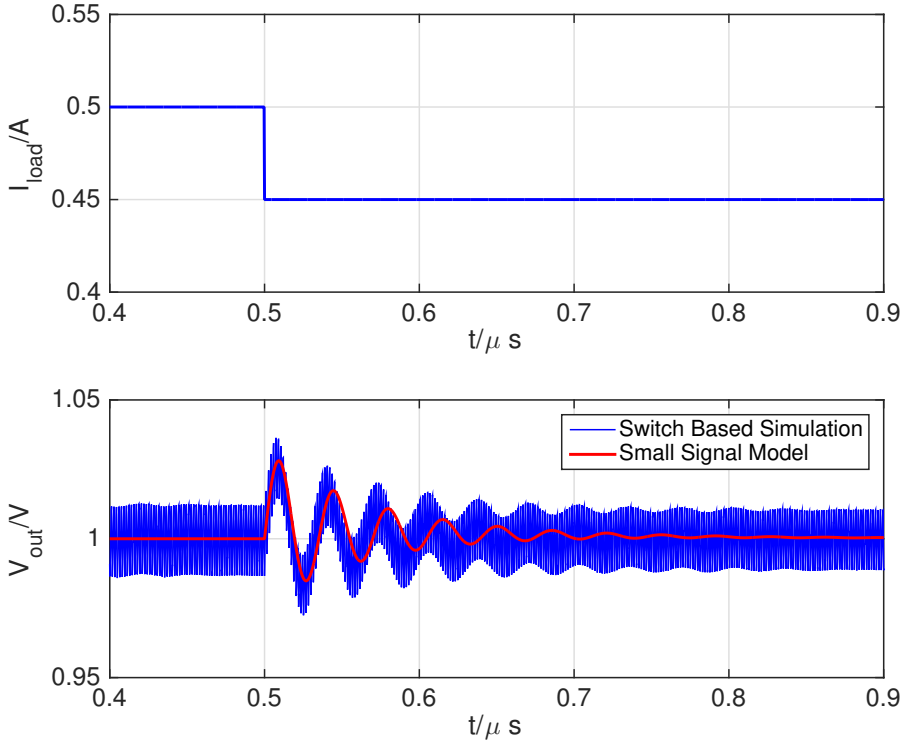

Figure 3.6: Load Transient Comparison of Small Signal Model and Switch Based Circuit Simulation

Chapter 4

Conclusion and Future work

4.1 Conclusion

The thesis introduces the phase shift operation and regulation design for the ResSC converter. After exploring the operating strategies and large signal characteristics of this promising circuit, a detailed development of the circuit dynamics has been undertaken using a harmonic averaging methodology. The method and models developed lead to simple strategies for the control design and implementation.

4.2 Future work

For future, an IC implementation will be taped-out to demonstrate benefits of ResSC converter with the proposed operation. Popular 65nm CMOS technology or more advanced nodes should be selected for the reasonable switching loss at a few hundreds MHz operating frequency. The inductance of a few nH can be realized with the bond-wire or a simple PCB trace which is promising for a tight integration.

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