Equalization of Backplane Channels Using Transmitter FFE and Receiver CTLE+DFE

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1. Introduction

1.1. Background

The constant demand for higher server data throughput in today's increasingly connected world has led to the need for robust chip to chip communication links on server backplanes to operate at very high data rates. However, at the high frequencies required to achieve these data rates, the communication channel is very lossy, due to the parasitics associated with the server line card and backplane traces, associated vias, connectors, and chip packages. This introduces significant distortion, causing intersymbol interference (ISI) that will lead to a high bit error rate (BER). Therefore, equalization must be performed in the transceiver to reduce the ISI and improve the BER in order to faithfully receive the information that is sent. In addition to equalization, the receiver must also extract the clock frequency and phase through clock and data recovery circuitry (CDR). Equalization at transmitter involves pre-emphasis of the transmitter signal to negate the channel effects. Equalization at the receiver generally aims for signal correction by way of amplification, digital correction or both.

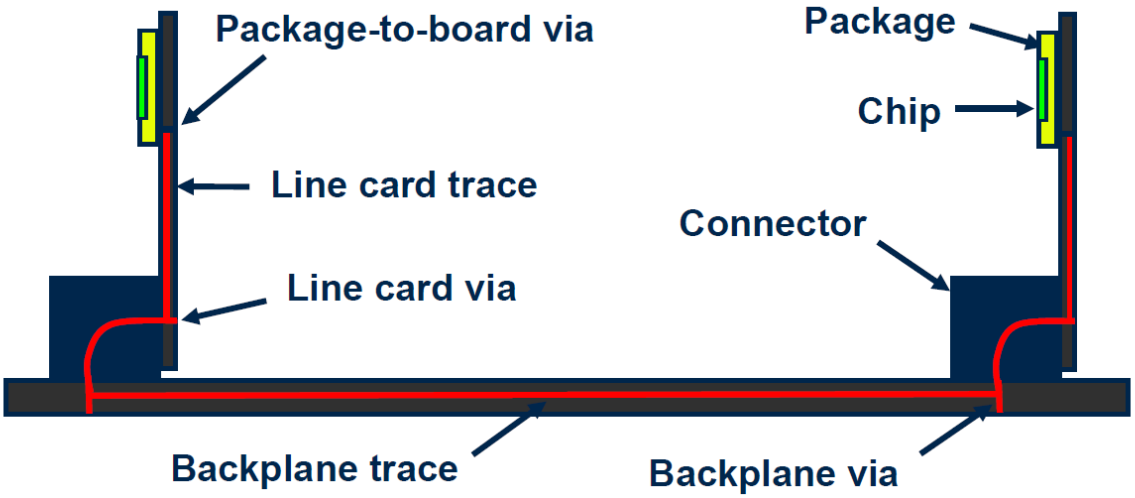

Figure 1. Diagram of the typical backplane environment.

1.2. Objective

The goal of this project is to design a 12.5 Gbps high-speed transceiver able to achieve a BER of 10^{-15} or lower on five backplane channels in a 32 nm CMOS process while minimizing power consumption.

2. Channel Characterization

Before proposing an equalization scheme to achieve the desired BER, it was first necessary to characterize the five channels. AC and transient simulations at different frequencies were performed on each of the five backplane channels.

2.1. Channel 1: 30-inch Top

2.1.1. Frequency Response

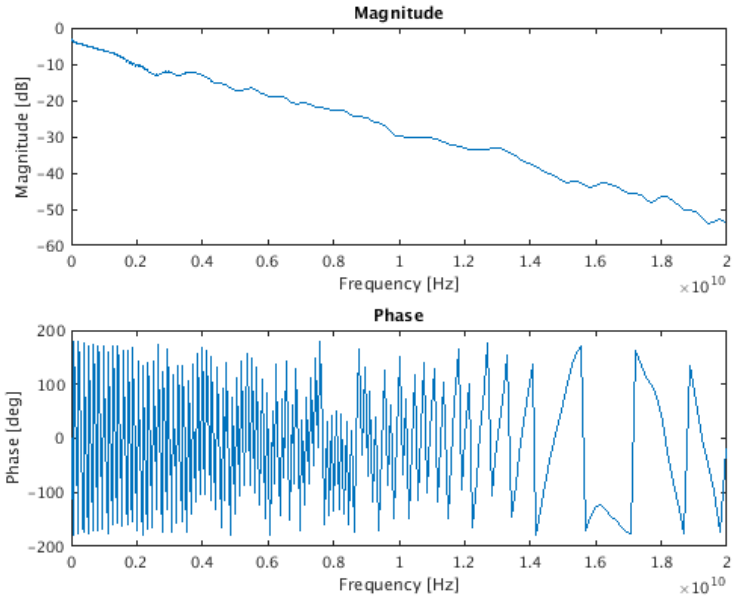

Figure 2. 30-inch top frequency response from 0 to 20 GHz.

2.1.2. Impulse Response

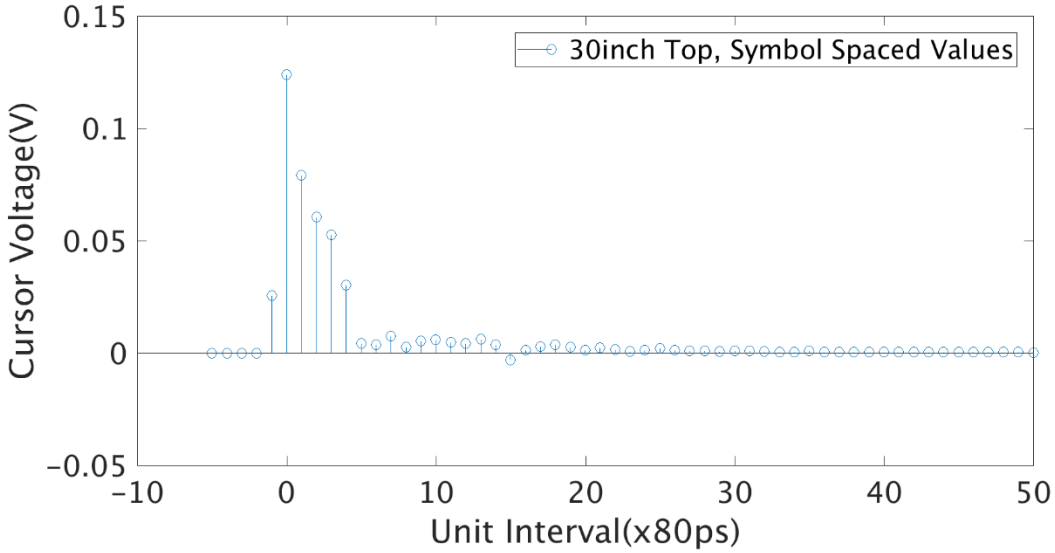

Figure 3. 30-inch top Impulse Response at 12.5 GHz (UI = 80 ps).

2.2. Channel 2: 30-inch Bottom

2.2.1. Frequency Response

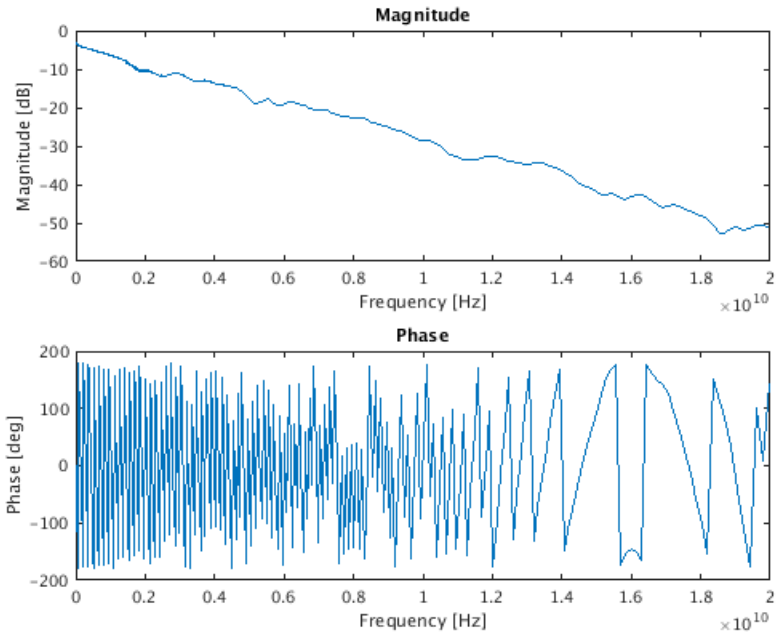

Figure 4. 30-inch bottom channel frequency response from 0 to 20 GHz.

2.2.2. Impulse Response

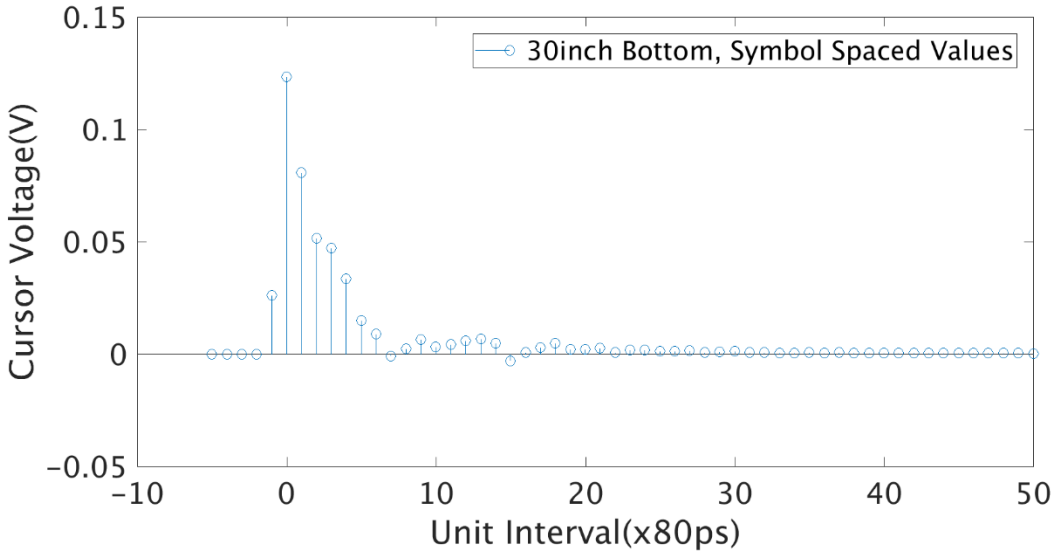

Figure 5. 30-inch bottom channel impulse response at 12.5 GHz (UI = 80 ps).

2.3. Channel 3: 20-inch Mid

2.3.1. Frequency Response

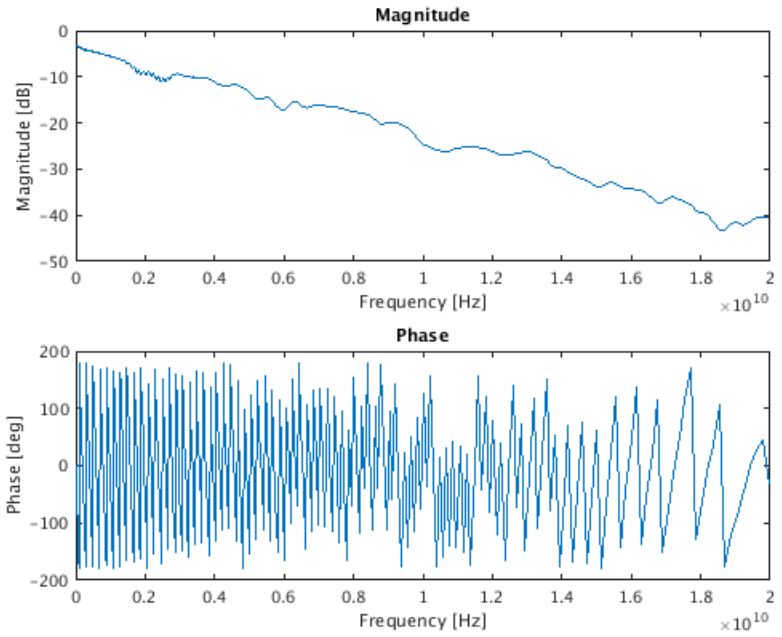

Figure 6. 20-inch mid channel frequency response from 0 to 20 GHz.

2.3.2. Impulse Response

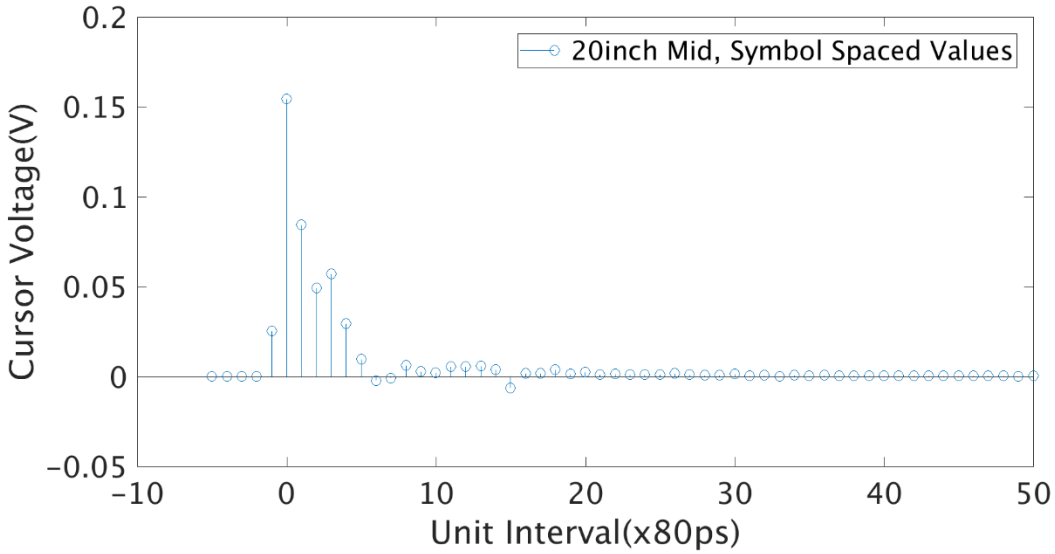

Figure 7. 20-inch mid channel impulse response at 12.5 GHz (UI = 80 ps).

2.4. Channel 4: 10-inch Mid

2.4.1. Frequency Response

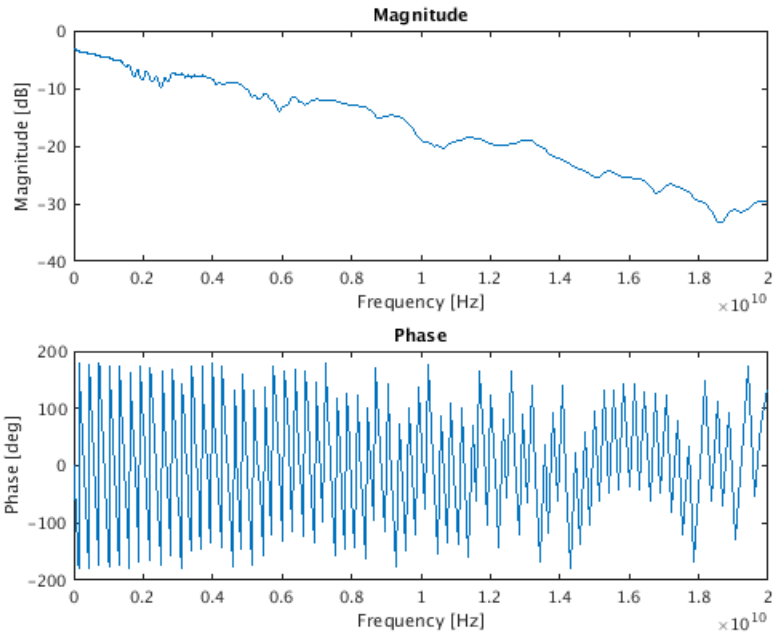

Figure 8. 10-inch mid channel frequency response from 0 to 20 GHz.

2.4.2. Impulse Response

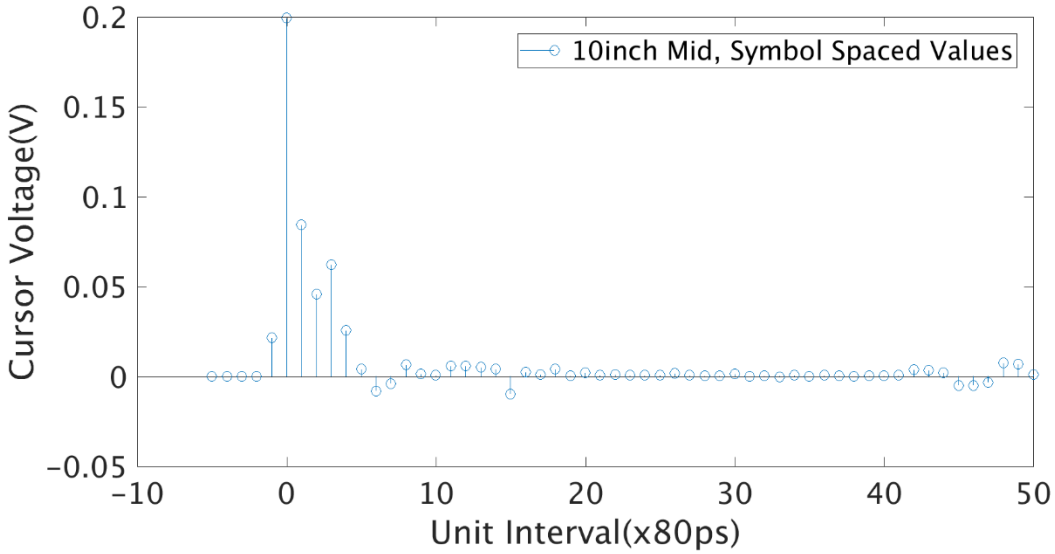

Figure 9. 10-inch mid channel impulse response at 12.5 GHz (UI = 80 ps).

2.5. Channel 5: 1.5-inch Top

2.5.1. Frequency Response

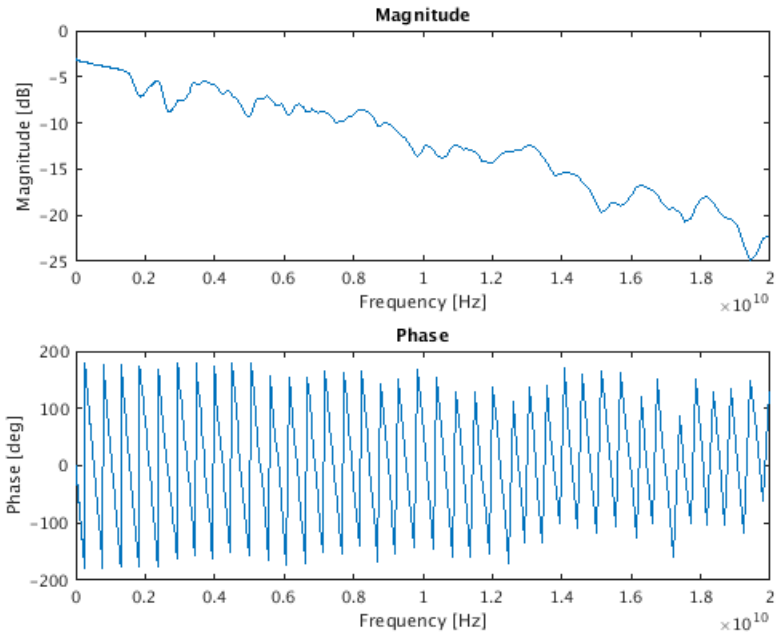

Figure 10. 1.5-inch top channel frequency response from 0 to 20 GHz.

2.5.2. Impulse Response

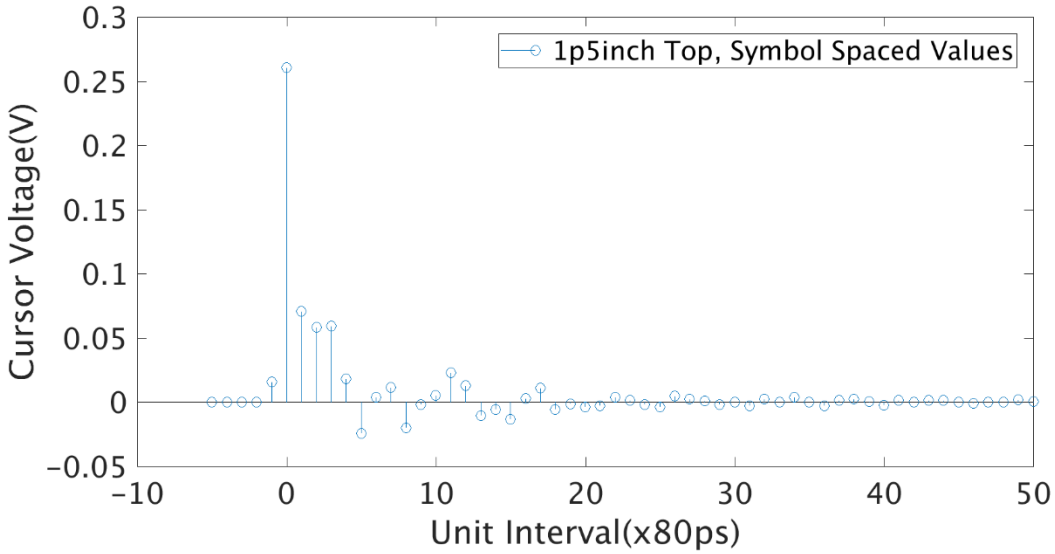

Figure 11. 1.5-inch top channel impulse response at 12.5 GHz (UI = 80 ps).

3. Equalization Architecture

It was observed in the channel characterization results that all channels had significant precursors as well as long-tail ISI. In order to accommodate the precursors and reduce the long-tail ISI, a 1 stage CTLE is proposed at the receiver. The CTLE will also act as amplifier before the digital equalization. In order to cancel the precursor, a 2 tap Feed Forward Equalizer(FFE) is proposed at the transmitter. The FFE is implemented as a Finite Impulse Reponses(FIR) filter. For the post cursor ISI removal, we propose Decision Feedback Equalizer(DFE). Our initial analysis revealed that a 10 tap DFE is desirable for achieving a 10^{-15} BER. A block diagram of the proposed architecture is shown in Figure 12. The target data rate is 12.5Gbps.

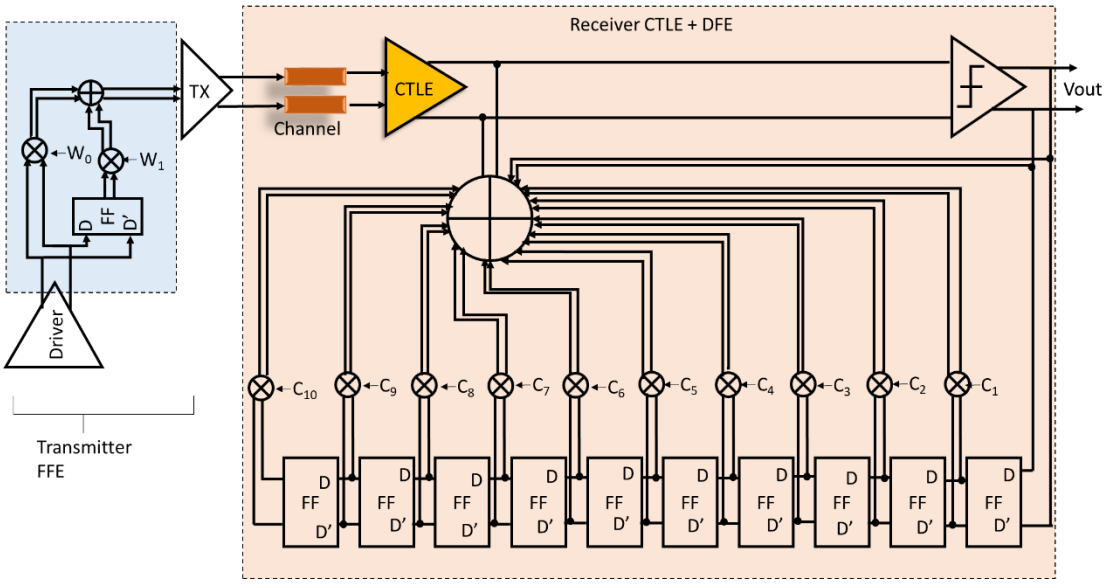

Figure 12. Block diagram of the proposed transceiver showing 1 stage CTLE and 10 tap DFE at the receiver and a 2 tap FFE equalizer at the transmitter. The target data rate is 12.5 Gbps.

4. Equalization / Signal Chain Implementation

4.1. Transmit FIR

4.1.1. Design

As shown in Figure 13 below, all of the five channels contain one precursor besides post cursor ISI. The worst-case channel being Channel 1 (30-inch top) and Channel 2 (30-inch bottom). The equalization architecture is mostly focused on receiver equalization to eliminate post cursors. However, a feed-forward equalizer is still required for eliminating the first precursor. This is more prominent for channels 1 and 2 with precursor ISI close to 22% of the main cursor.

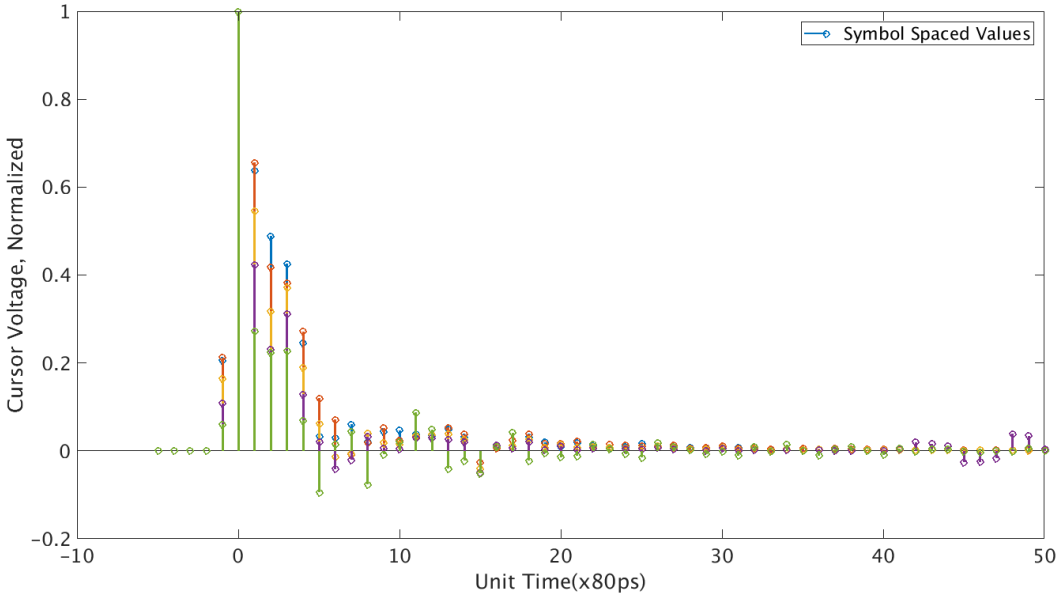

Figure 13. Impulse response of all channels overlaid.

A 1-tap FIR was designed for the worst-case channel, Channel 1. A ZFE algorithm was used to determine the tap coefficients. Using the channel impulse response as the channel matrix and with the goal of all other cursors are zeroed, a MATLAB script was utilized to calculate the tap coefficients for the FIR. They were determined to be [0.8, -0.1984].

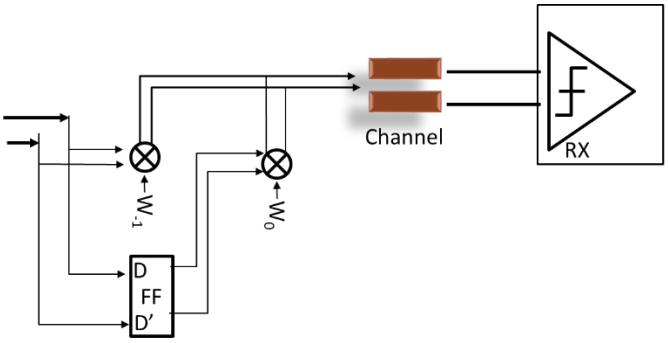

Figure 14. Diagram of the 1-top FIR.

Table 1. Tap coefficients for 1-tap FFE for Channel 1

W_0(normalized)	0.8
W_{-1}(normalized)	-0.1984

A current summing FIR filter was designed. As shown in Figure 15 below, the circuit comprises of a differential pair that steers current to a 50Ω termination. The current proportional to W_{-1} is subtracted from the current proportional to cursor current W_0.

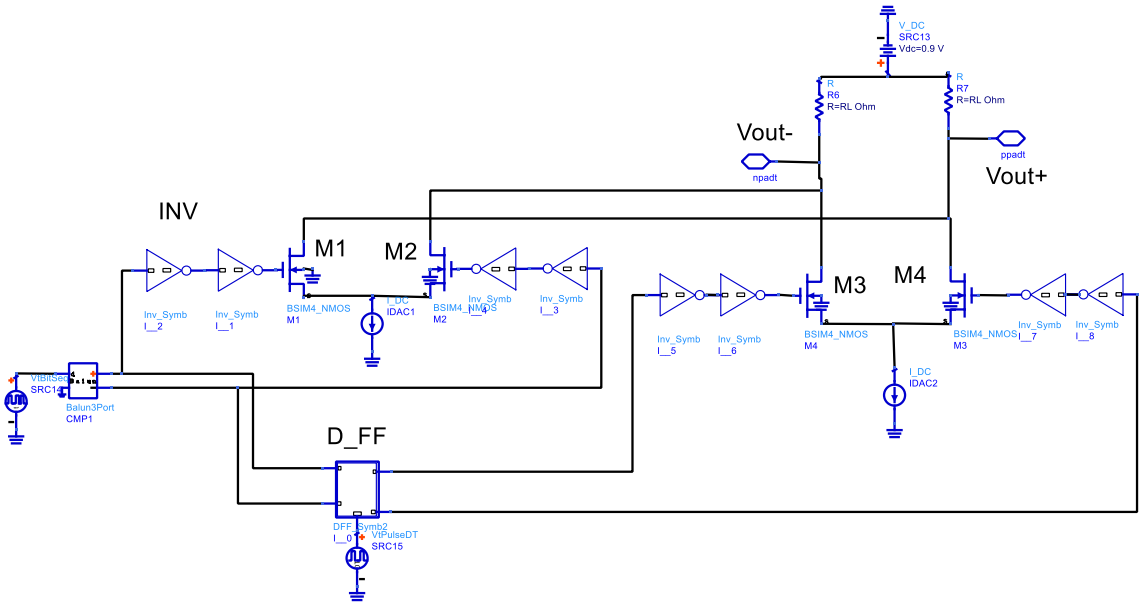

Figure 15. TX FIR circuit implementation

The design involves a trade between device size, current and bias. The differential pair is large in order to handle the large current. Besides, it also helps maintain the current DAC devices in saturation. This however limits the flip flop's drive capability. Therefore, buffers (comprised of inverters) were added to be able to dive the differential pair.

The differential pair M1-M2 is the pre cursor current steering pair. M_3-M_4 form the main cursor steering pair. A flip flop is used as delay element. The schematic of this flip flop is shown in Figure 18 below. The flip has been realized using NAND-2 and NAND-3 gates. The actual current IDAC1 and IDAC2 were realized using NMOS current DAC shown in Figure 16 below.

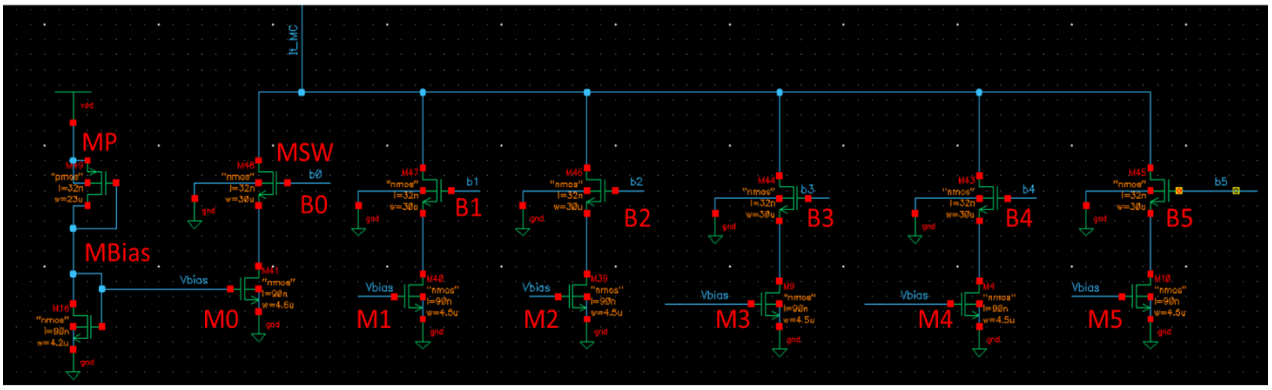

Figure 16. IDAC

Table 2: IDAC Design Specification

Device	**Width**	**DC Current(uA)**
MP	23um, 32nm	150uA
MBIAS	4.2um, 90nm	150uA
M0	4.5um	150uA
M1	9um	300uA
M2	18um	600uA
M3	36um	1.2mA
M4	72um	2.4mA
M5	144um	4.8mA
MSW	30um	

The devices MP and MBIAS form the current generators. The devices M0-M5 are scaled progressively to generate the required DC current. As shown in the table above, the currents increase as $150uA*2^N$. A voltage swing of 450mV was selected for the FIR filter. For a V_{DD} of 900mV and termination resistance R_L of 50Ω, this corresponds to a total current of 9mA. The channels lengths of the devices were increased to 90nm to ensure that they are in saturation. The switch device MSW was sized for minimum on resistance. The current is selected by setting the bit pattern B0[5:0] and B1[5:0].

The maximum output swing of the TX FIR is limited by the overhead of the NMOS devices. To maintain the IDAC and differential pair devices in saturation, the maximum swing is limited to ~400mV assuming a V* of 200mv for each of the devices.

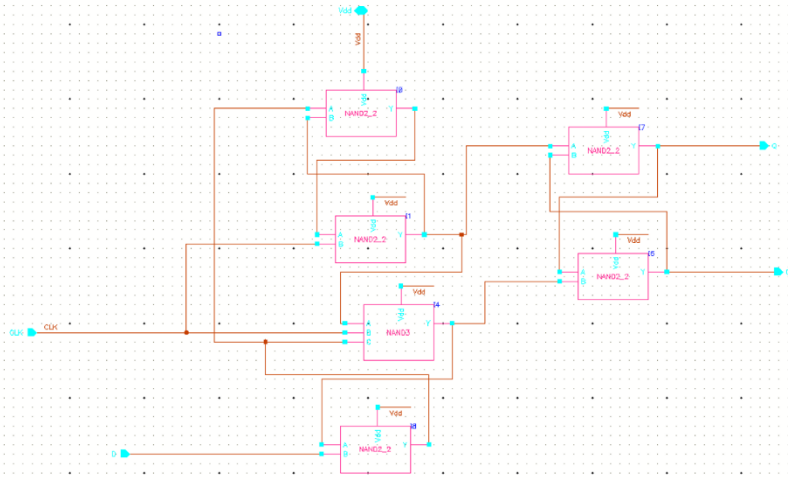

Figure 17:D Flip Flop Using NAND2 and NAND3

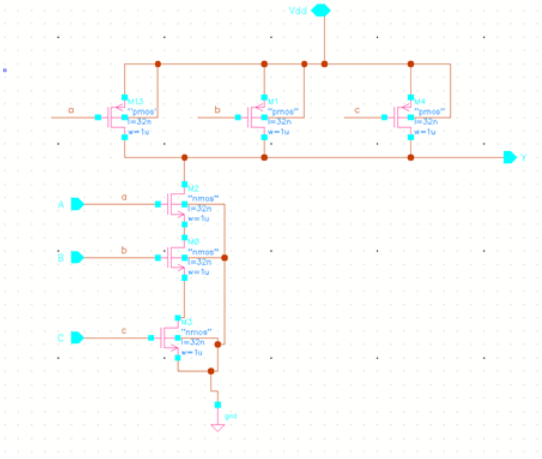

Figure 18:NAND3

The NAND3 and NAND2 were sized for minimum delay.

Table 3:IDAC settings for each channel

Channel	**Cursor IDAC Setting**	**Pre-Cursor IDAC Setting**
1	011111	001011
2	011111	001011
3	011111	000100
4	011111	000111
5	011111	000011

4.1.2. Simulation Results

A transient simulation was performed with different channels. Table 3 above lists the IDAC settings to achieve precursor cancellation. Figure 19 below shows the test bench.

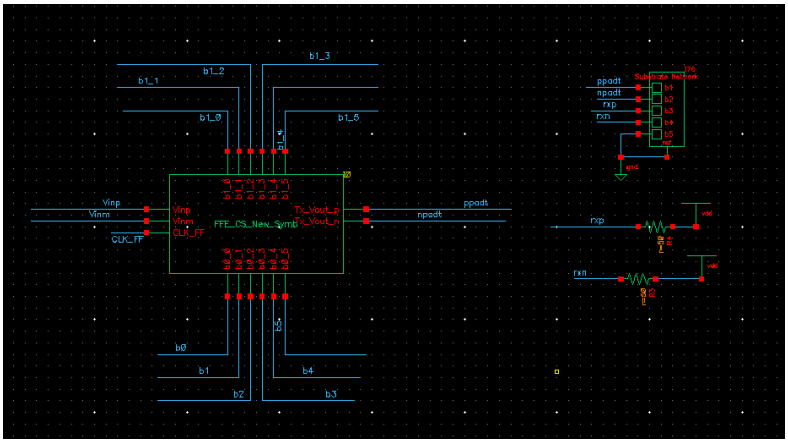

Figure 19:Tx FIR Test Bench

Figure 20 below is a plot showing the output of the transmitter showing pre-emphasis. A 900mV input pulse (80ps) was input to the FIR. As shown in figure below, it is shifted by 1 unit interval and pre-emphasized one unit interval (80ps) preceding the main cursor. Figure 21 below shows the signal received at the output of channe1 which is the worst-case channel. It can be clearly observed that the first precursor is negated.

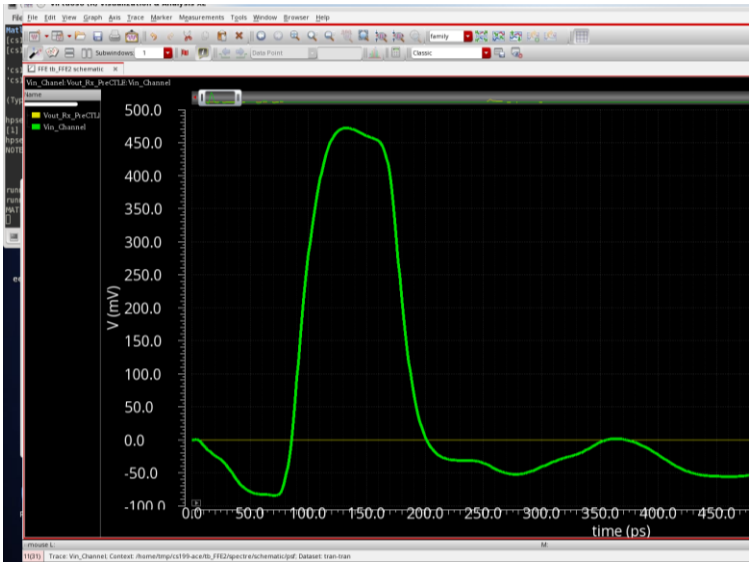

Figure 20:Premphasised pulse at the output of the FFE

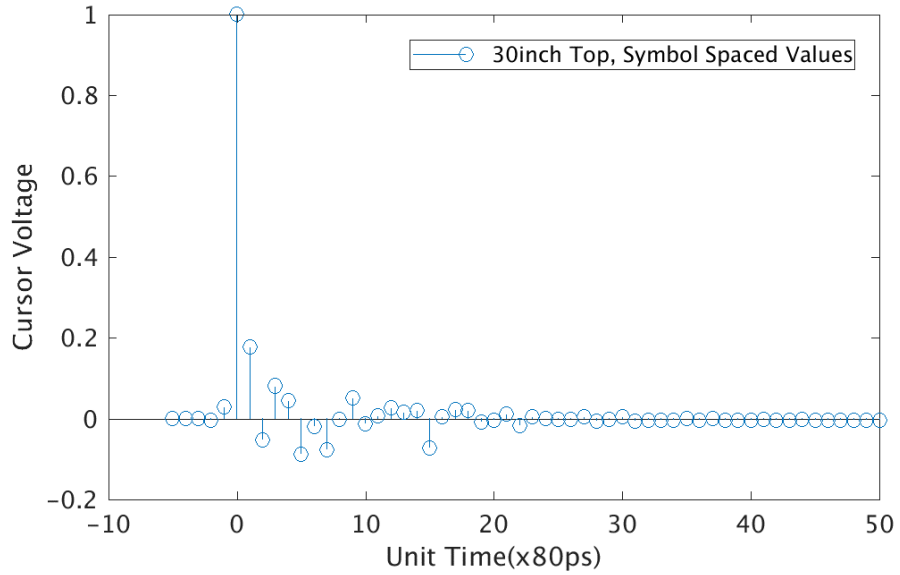

Figure 21:Channel output (30-inch top) after transmit FFE Output normalized w.r.t main cursor. The main cursor value is 121mV.

4.2. CTLE

4.2.1. CTLE Design

A high frequency peaking amplifier can be used for compensating for the severe attenuation in the channel. A Continuous Time Linear Equalizer (CTLE) was designed as the first stage of the receiver. The initial design was a CTLE amplifier using shunt peaking to boost the gain at the data rate. However, since an inductor-less design is desirable, the CTLE was redesigned. To improve the bandwidth, a cascode design was used which provides gain at high frequencies. To account for the loading at the CTLE output, the CTLE was loaded with 10fF capacitors. Figure 22 below is the schematic of the CTLE.

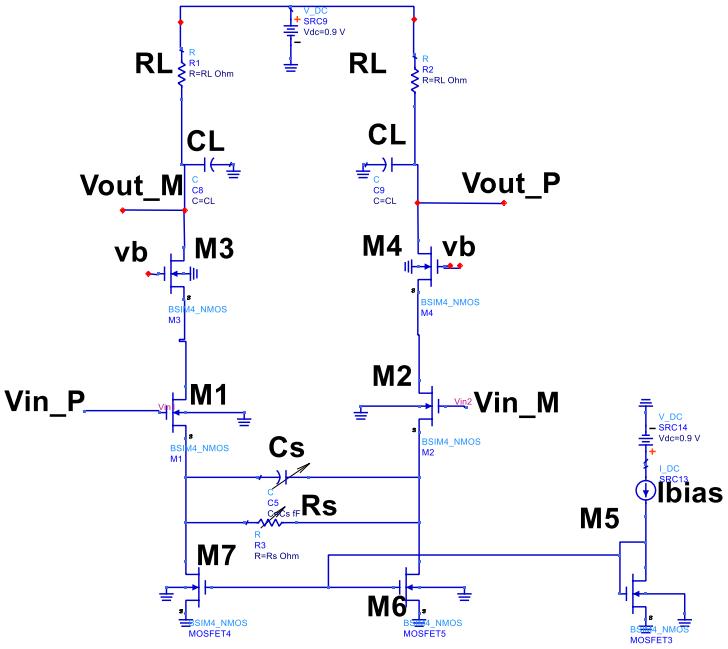

Figure 22. Cascode CTLE schematic

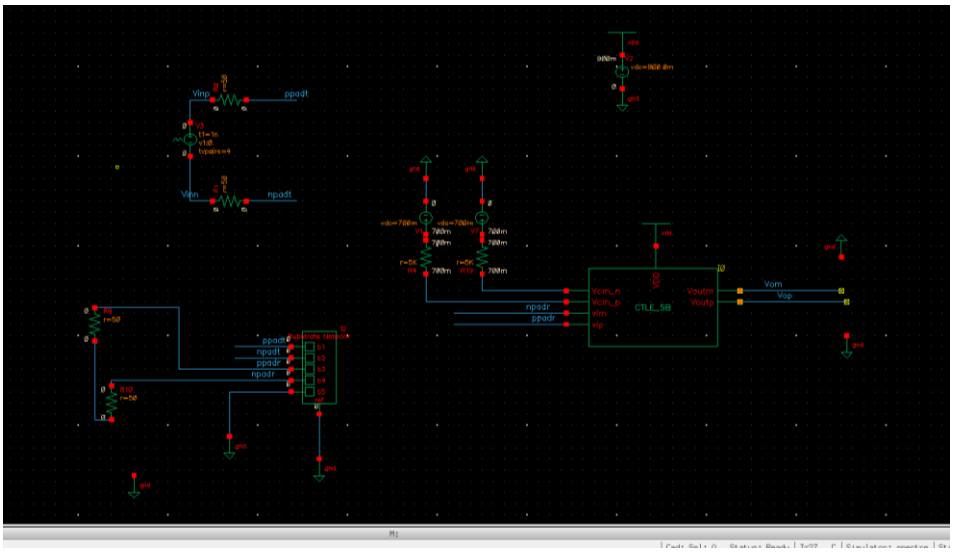

Figure 23: Test Bench for CTLE

Figure 24 below is the AC behavior of the CTLE amplifier with input fed through channel 1 (30-inch top).

The design parameters are a peak gain of 2 at the bit rate (12.5GHz) and a zero frequency of ~300MHz which is the 3dB pole frequency of the worst-case channel(channel1). While it is common to center the peak gain at -2/3 of bit rate(8.33GHz), a peaking gain at 12.5GHz is more desirable and it also improves the transient behavior by reducing both precursor and long tail ISI. The CTLE's second pole frequency is ~ 14GHz. Table 4 summarizes the CTLE design parameters.

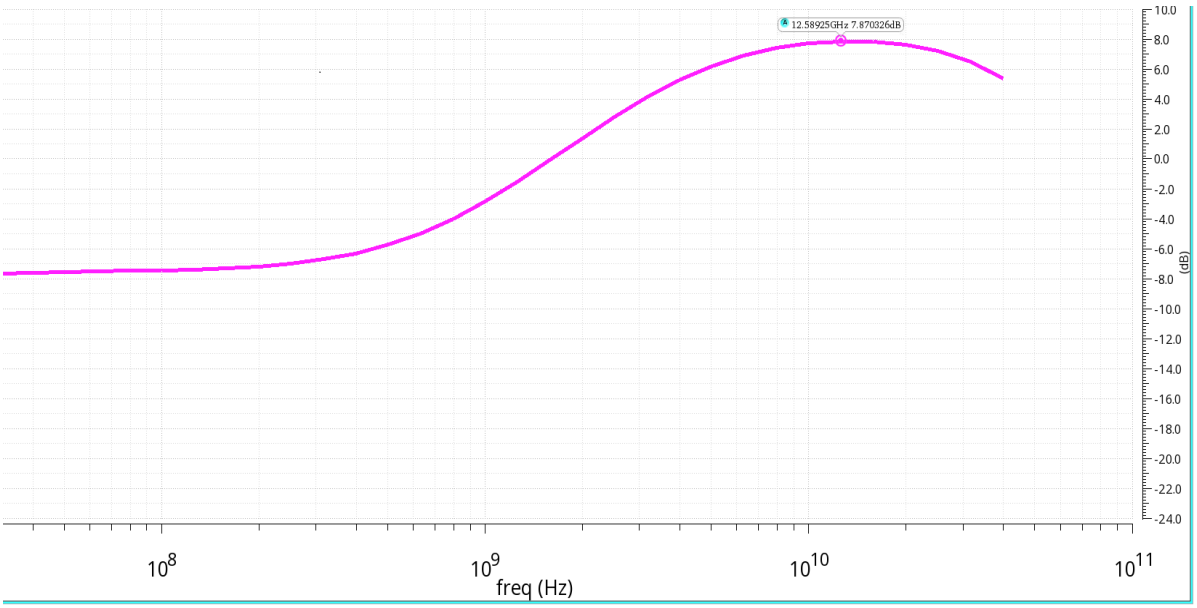

Figure 24: AC response of CTLE loaded with 30inch top channel and 25fF load.

The degeneration resistance Rs and Capacitance Cs are based on a zero frequency of 300MHz. The resistance RL sets the peak gain (gm*RL) but also sets the output common mode voltage to 650mV.

Table 4:CTLE Design Specification

Specification	
Peak Gain	7dB
g_m	15ms
Ibias	700uA
CL	25fF
Rs	1350Ω
RL	170Ω
Cs	400fF
M1, M2	19.6 um / 50 nm
M3, M4	14 um / 60 nm

A second amplifier stage was also added to further boost the gain. The second amplifier stage used a common source amplifier without the degeneration employed in the CTLE. This is shown in Figure 25.

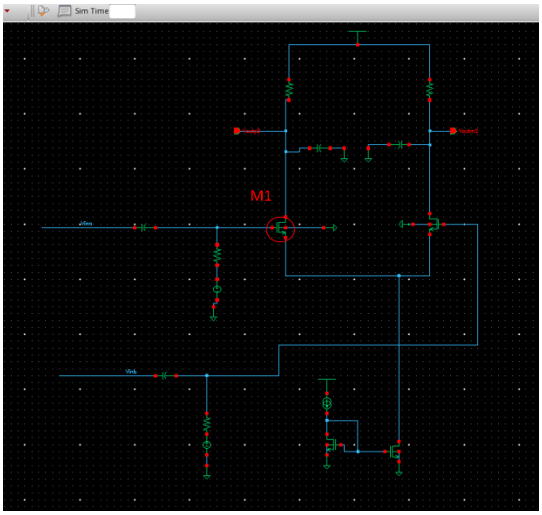

Figure 25: Second amplifier stage after the CTLE

Figure 26 is a plot showing the gain of this two-stage design. The second stage also has an output common mode voltage of 650mV which is compatible with the comparator (described later in this report). Figure 27 below is the transient response of the CTLE-amplifier combination. It can be clearly seen that not only is the signal amplitude boosted (at 12.5GHz), but the precursor is also reduced.

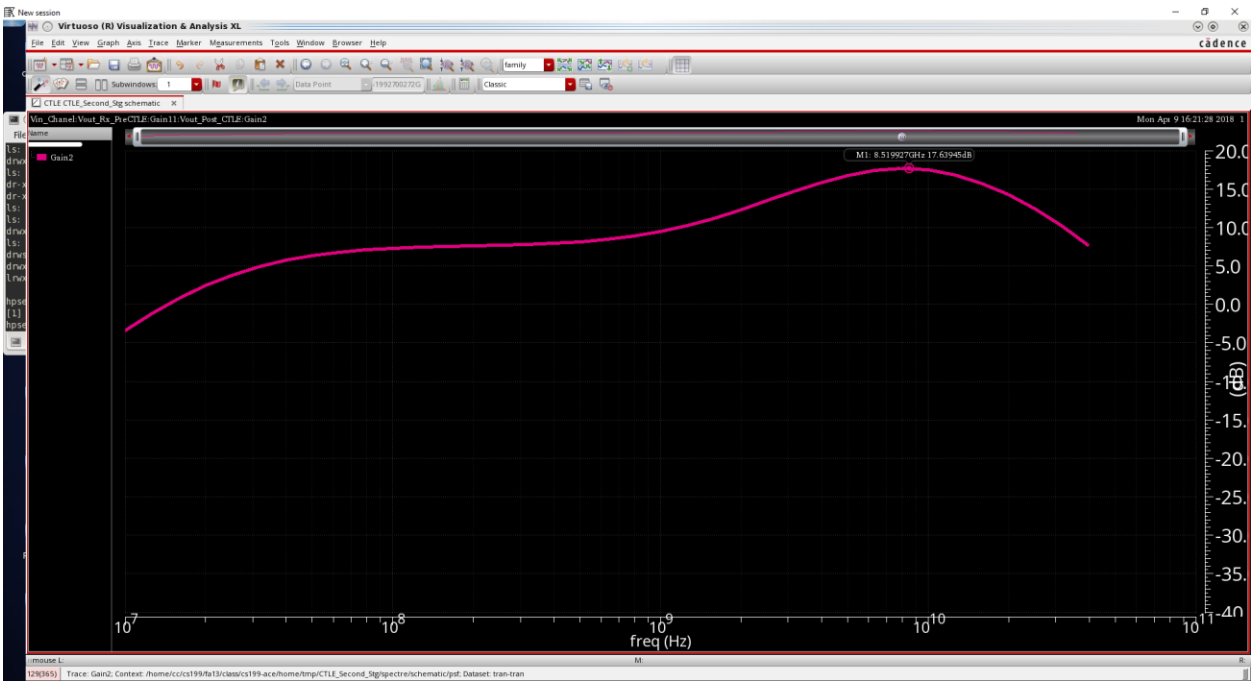

Figure 26. Combined gain of CTLE and second amplifier stage

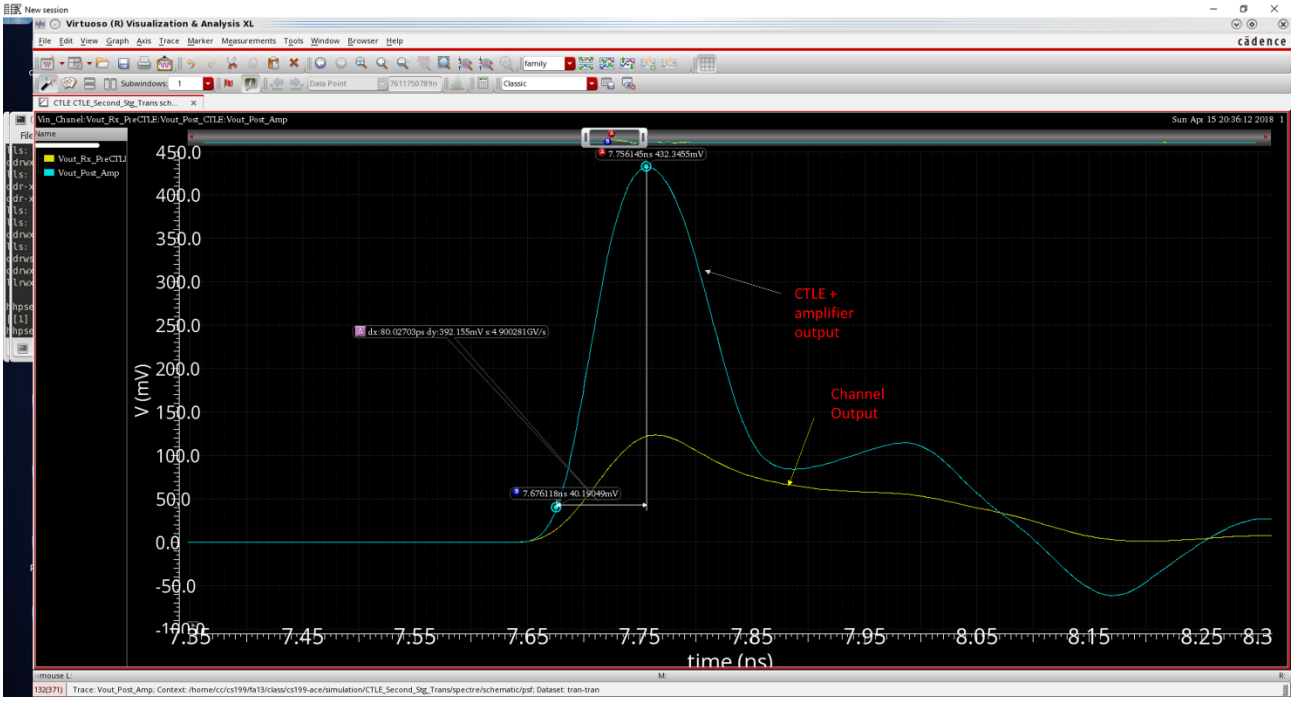

Figure 27. Transient response of CTLE and amplifier loaded with 30inch top channel and 25fF load

Eventually, the second amplifier stage was eliminated in order to save power consumption. Besides, the second amplifier stage reduces the overall bandwidth and increased noise contribution. Moreover, the input and output common mode voltage was ~650mV which is the requirement for the subsequent stages such as the DFE summer and StrongARM comparator

(described later). Since the original single stage CTLE amplifier was already producing an output common mode voltage of 650mV, the second stage was removed.

The output of the channel was connected to the CTLE and a transient simulation was performed with a single pulse. Figure 28 below is the impulse response at the output of the CTLE when Channel 1 is connected to the input. It can be clearly seen that long tail ISI is reduced. Some of the post and precursors are also reduced. The sharp rising edge of the pulse at the output of the CTLE is attributed to the peaking gain at the operating frequency of 12.5GHz.

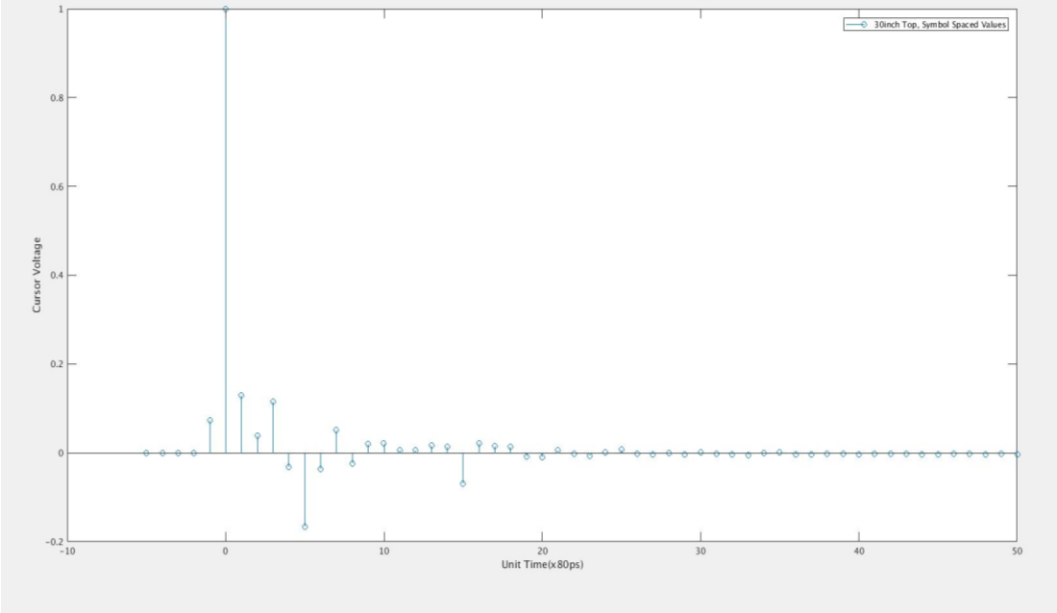

Figure 28:Impulse response at the output of the CTLE. Channel input is 900 mV pulse, channel output is connected to CTLE.

4.2.2. CTLE Adaptation

A transistor level pole-zero adaption circuit was designed to optimize the zero frequency of the CTLE. As shown in Figure 29, in addition to the nominal degeneration resistance and capacitance, an NMOS device (in triode) is added which functions as a voltage-controlled resistor.

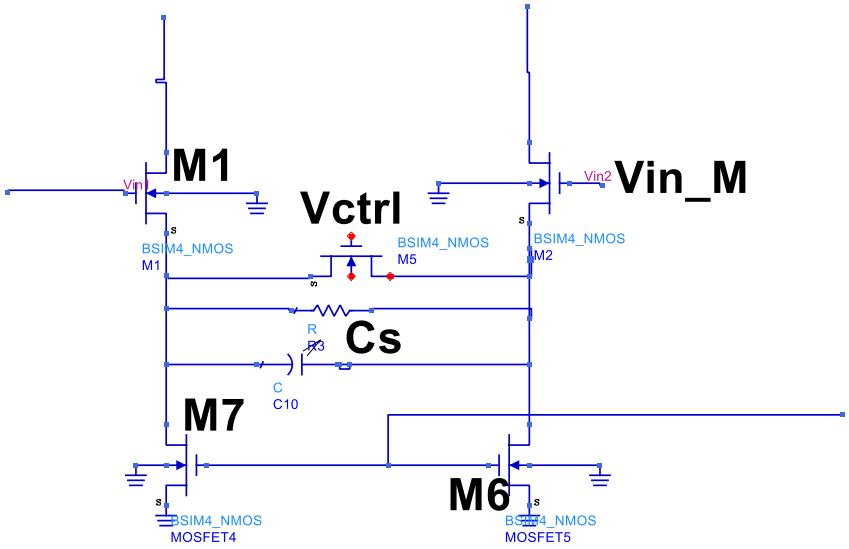

Figure 29: Implementing variable resistor

To generate Vctrl, the CTLE bandwidth is segmented into lower and upper half and the energy in the bands is compared. Figure 30 below is the block diagram.

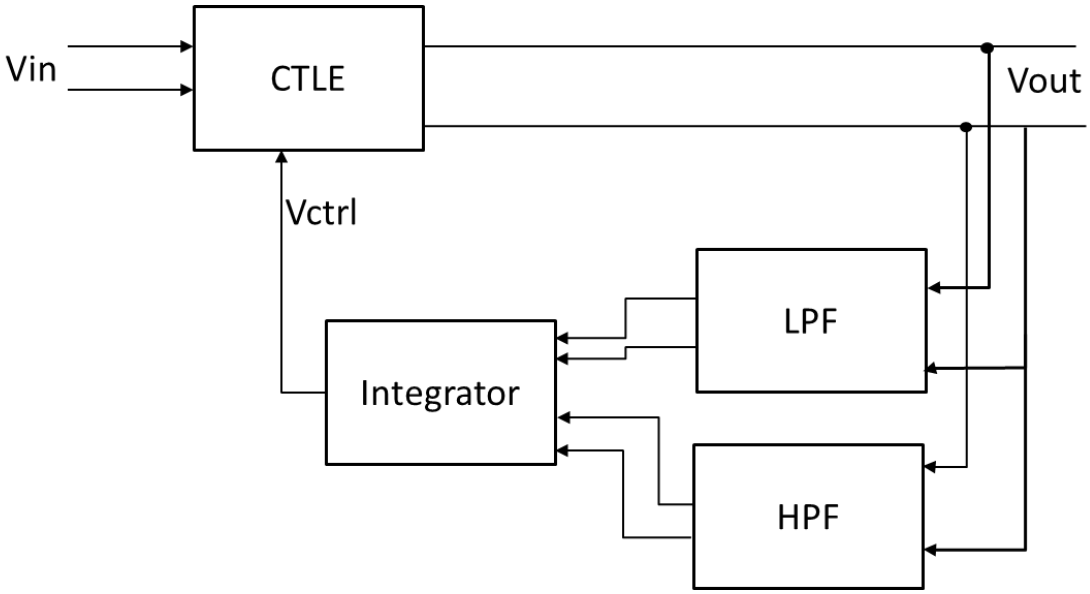

Figure 30. CTLE adaptation block diagram

The actual implementation was based on the circuitry in [1]. Figure 31 below shows the variation of the CTLE zero frequency with Vctrl. The tunable range for the NMOS resistor is 600mv-700mV. The adaptation circuit was designed to generate this range of control voltage. The nominal voltage of 650mV corresponds to the zero-frequency resistance of ~1.35KΩ.

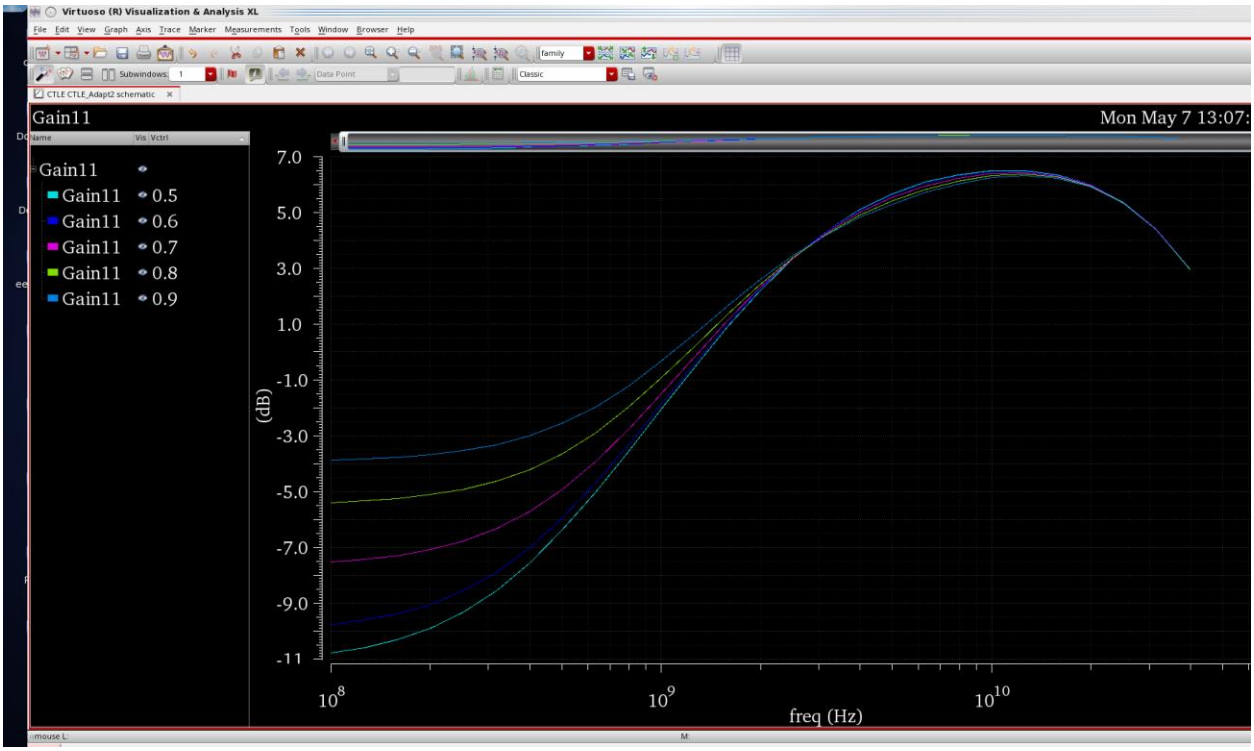

Figure 31. Vctrl Vs CTLE gain

In the actual implementation, the LPF-HPF network was designed using current steering as shown in Figure 32. C1-R1 pair set the filter cutoff frequency. For a frequency of 6.25GHz, which is roughly at the center of the CTLE bandwidth, C1~12fF and R1~2KΩ. The transistor quad M_1-M_4 will steer the current and add the high and low frequency components. C2 is used for filtering.

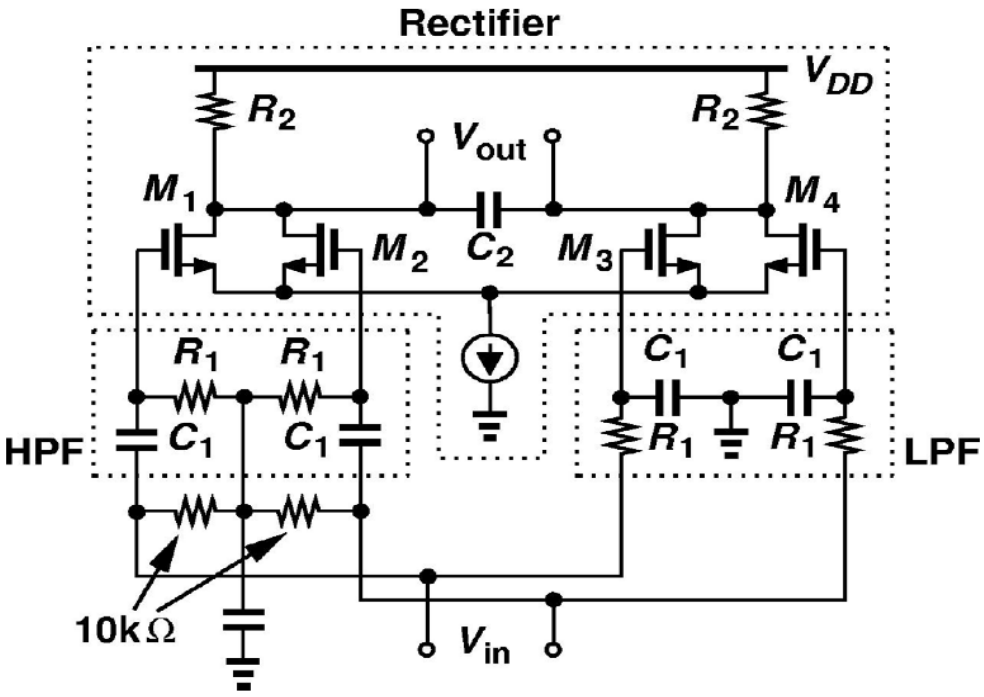

Figure 32. LPF-HPF filter and combiner [1]

A V/I converter [1] generates the control voltage.

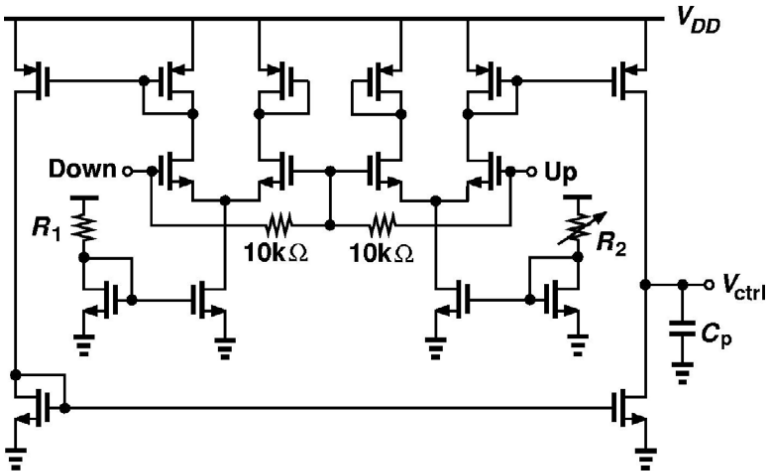

Figure 33. V-I Converter[1]

Figure 34 below shows the control voltage settling behavior for various channels.

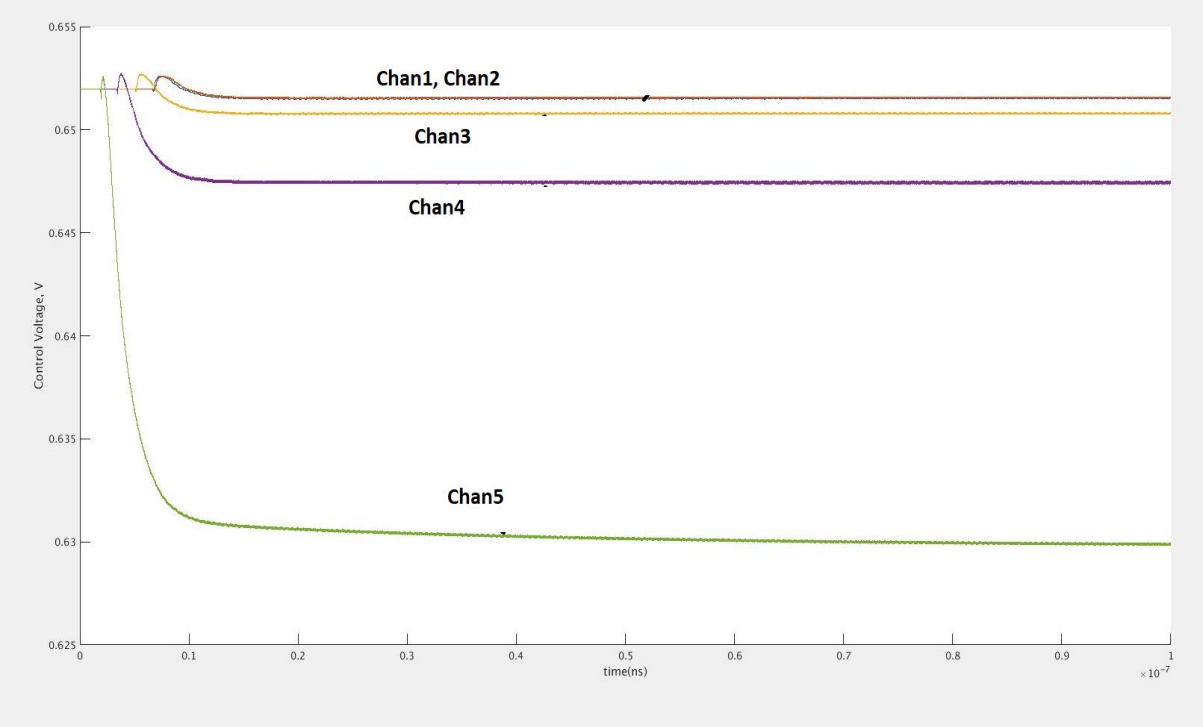

Figure 34. Vctrl settling for different channels

4.2.3. CTLE and FFE with Channel

The CTLE and the 1-tap FFE equalizer were integrated with the channel and the impulse response was simulated. Figure 35 and Figure 36 show the impulse response at the output of the CTLE after equalization with CTLE and 1-tap FFE for channels 2 and 3 respectively. It can be clearly noticed that the precursor is cancelled, first post cursor is reduced, and long tail ISI is reduced.

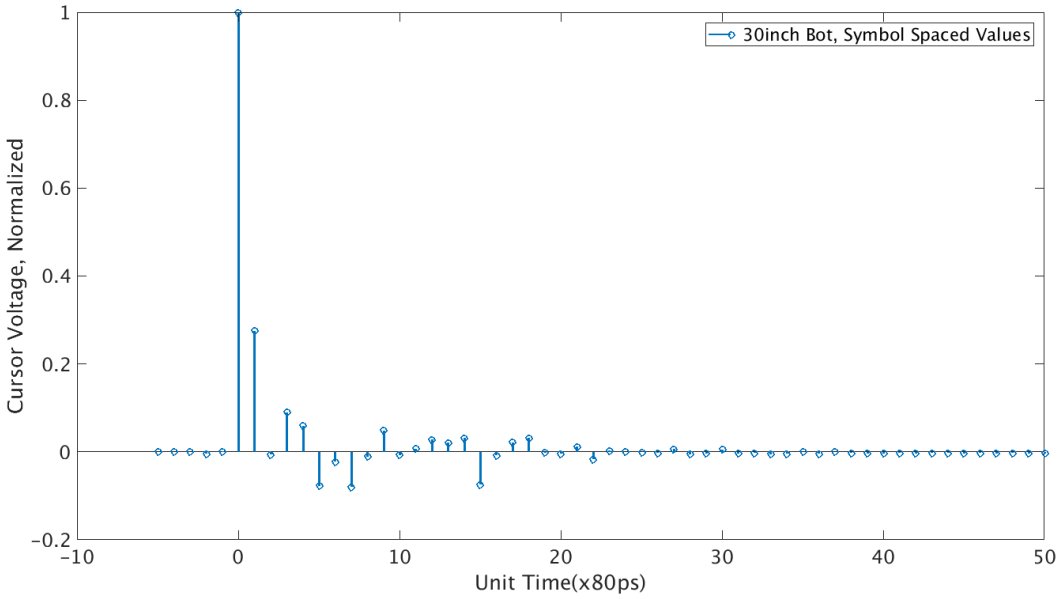

Figure 35. Channel 2 impulse response at the output of the CTLE after equalization with CTLE and 1-tap FFE

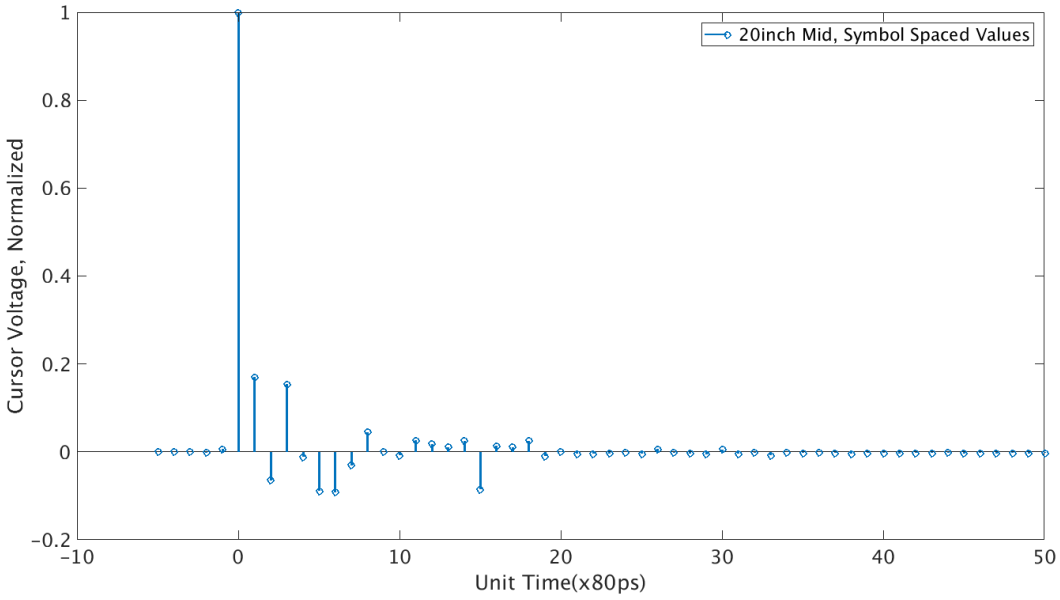

Figure 36. Channel 3 impulse response at the output of the CTLE after equalization with CTLE and 1-tap FFE

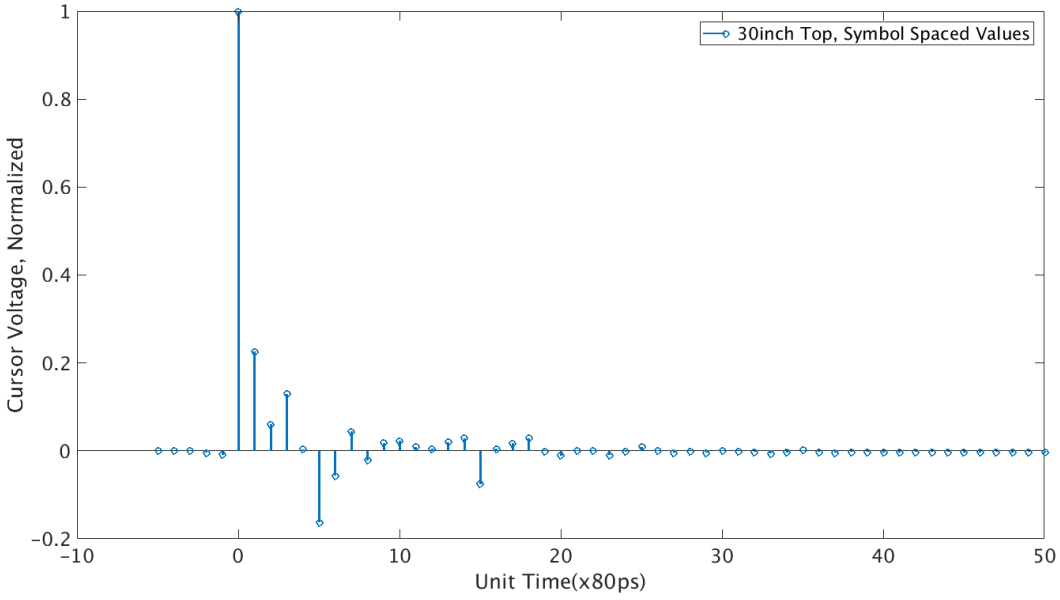

Figure 37. Channel 1 impulse response at the output of the CTLE after equalization with CTLE and 1-tap FFE

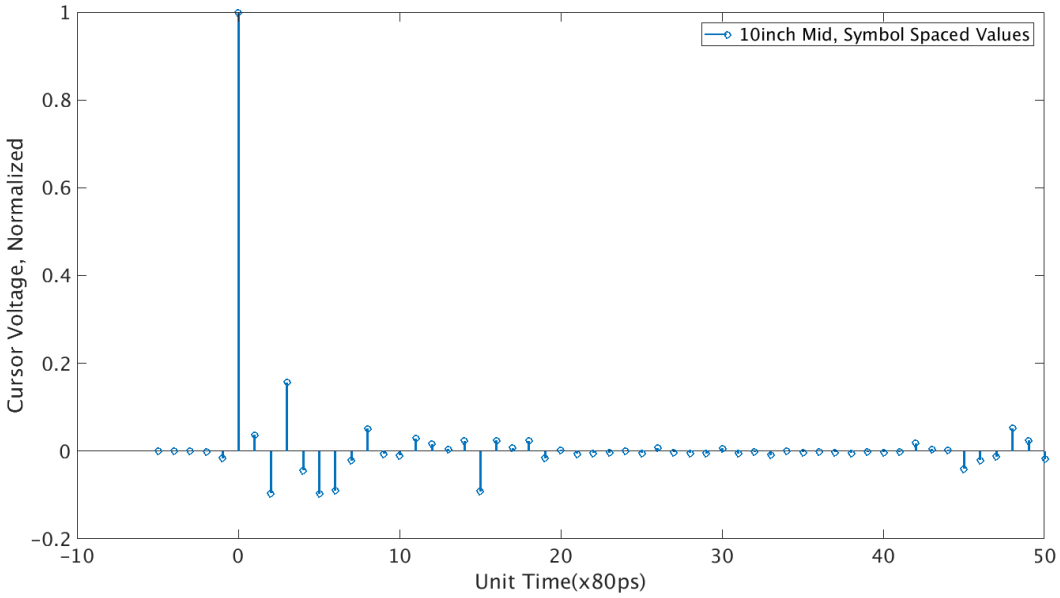

Figure 38. Channel 4 impulse response at the output of the CTLE after equalization with CTLE and 1-tap FFE

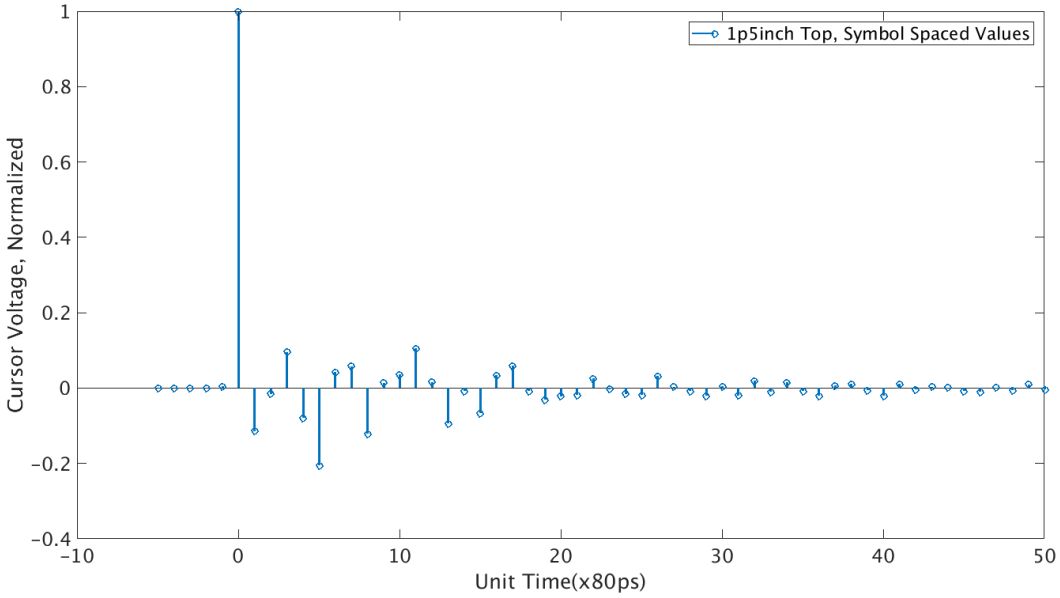

Figure 39. Channel 5 impulse response at the output of the CTLE after equalization with CTLE and 1-tap FFE

4.3. DFE

4.3.1. High Speed Comparator

The first loop of the DFE is the most critical path comprising of a comparator/slicer, unit delay element(D-FF) and DFE summer. Both CML and StrongARM Latch designs were investigated for implementing the comparator. While CML latch is faster, the StrongARM latch was preferred because of its ability to rail. This is critical because the compotator is followed by a flip flop which requires rail to rail inputs. While a CML latch can have higher output swing with the addition of more CML stages, through simulation, it was realized that the CML devices must be large causing large capacitances, which ultimately increases the settling time. Figure 40 below is a schematic of the StrongARM comparator. A preamplifier comprising of M1-M2 pair was added in order to reduce kickback. Table 5 lists the device dimensions. The devices sizing was based on a tradeoff between transconductance and self-loading capacitance with the goal being speed.

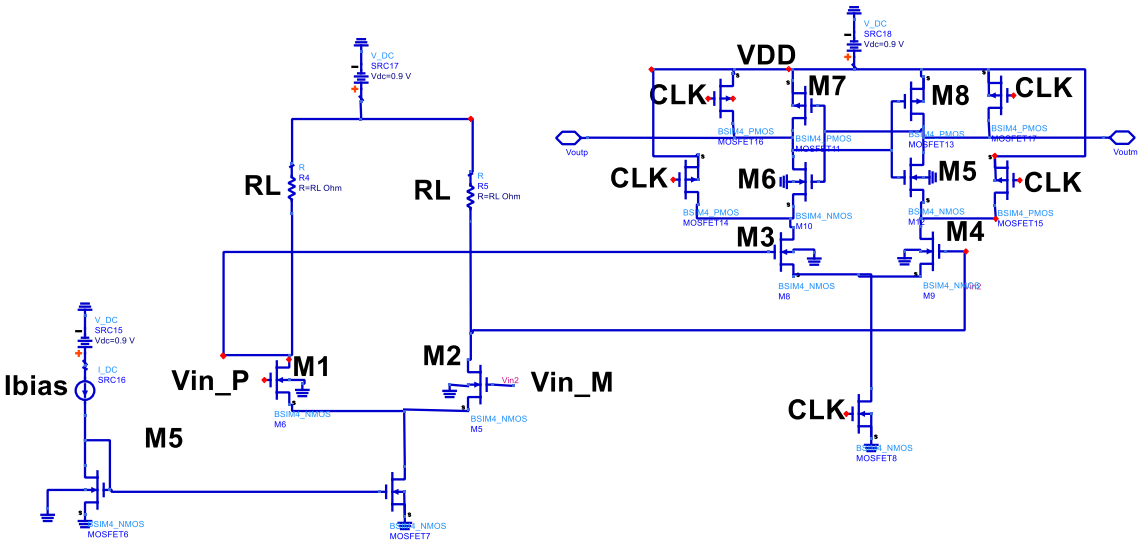

Figure 40: StrongARM Latch Comparator

Table 5: Device dimensions

Device	Width
M1, M2	14um, 50nm
M3, M4	5um,32nm
M7, M8	1um, 32nm
M5, M6	1um, 32nm

An RS latch was also added to the StrongARM latch to hold its output value. Figure 41 below shows the schematic of the latch. The comparator was simulated with a random signal generator with 80ps bit period. The comparator was closed at 12.5GHz. Figure 42 is the output of the comparator. It can be seen that the output follows the input with a data-Q delay of ~28ps.

The comparator was also inserted into the DFE circuit (using ideal IDAC). The DFE was simulated with ISI added manually to simulate the channel behavior. We artificially added ISI to a to a random bit stream generator in Cadence. This was done by time shifting and adding voltages to emulate the ISI. It can be seen in Figure 43 that the output of the comparator follows the original input bit sequence.

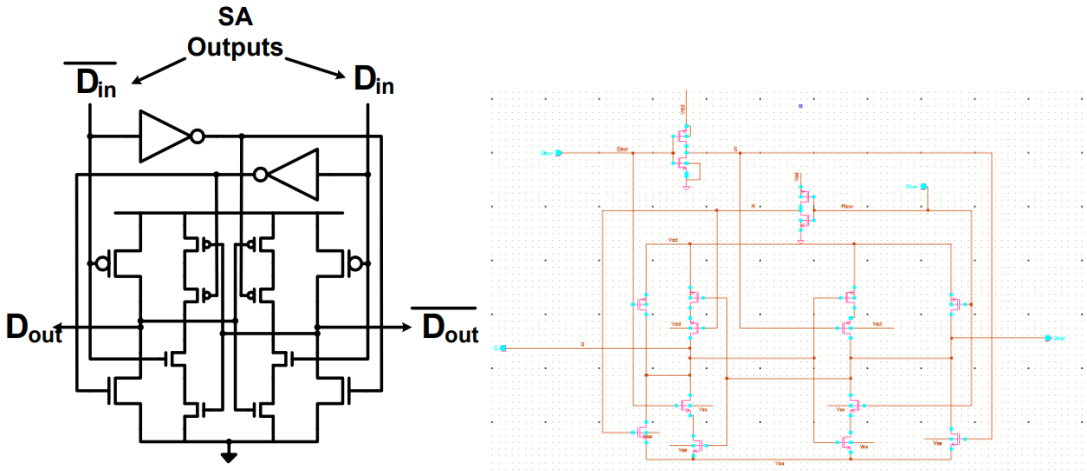

Figure 41(left) high speed SR latch and (right) transistor level implementation

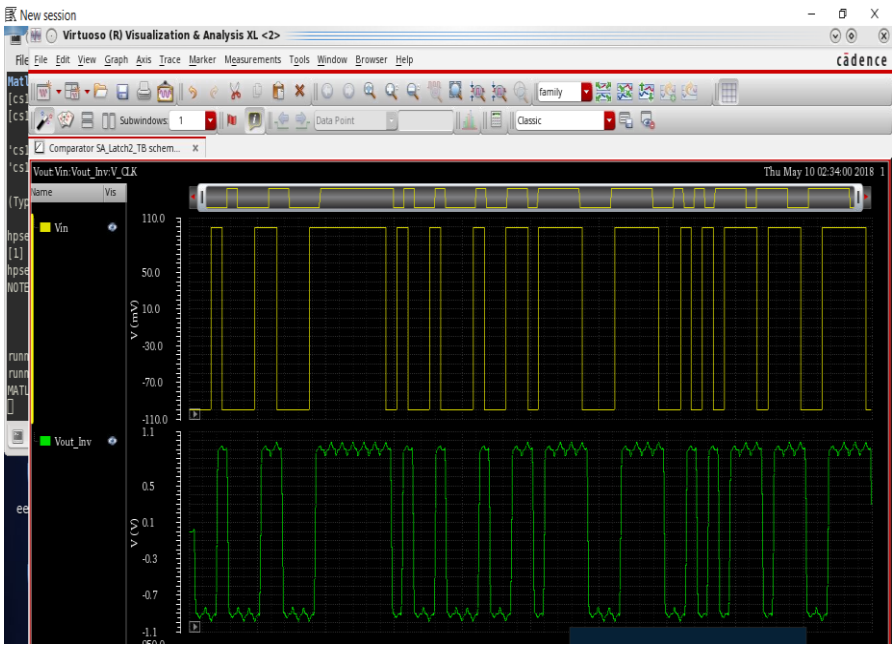

Figure 42. Output of the comparator with random input

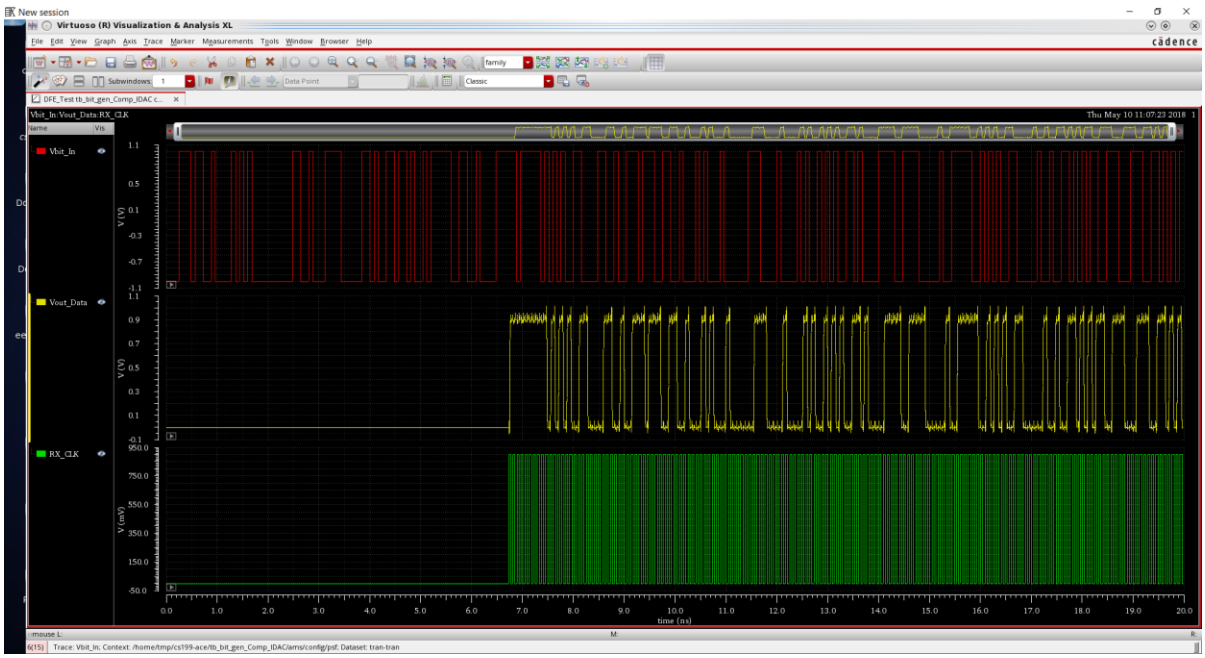

Figure 43: Output of ideal 10 tap DFE (w/ISI added manually)

4.3.2. DFE Summer

The DFE summer design is constrained primarily by settling time. The summer output must settle within 30ps given the logic delay (comparator and D-flip-flop). Table 6 below lists the post cursor values at the DFE input for the 30-inch top channel (Channel1) after passing through the Transmit FIR and CTLE.

Table 6:Post Cursors at the input of the DFE

T1	**T2**	**T3**	**T4**	**T5**	**T6**	**T7**	**T8**	**T9**	**T10**
0.2678	-.04061	0.05861	0.03481	-.0912	-.03809	-.09196	-.01671	0.04713	-0.009488

For the summer, $M_{DFE} = 0.78$, which corresponds to a g_m of 37 mS for the summer input device. The DFE summer was designed using a cascode topology. Figure 44 below is a schematic of the DFE summer. Figure 45 is a transient simulation showing the output of the DFE with the comparator, summer and flip flop inserted. ISI was artificially added to a to a random bit stream generator in Cadence. This was done by time shifting and adding voltages to emulate the ISI.

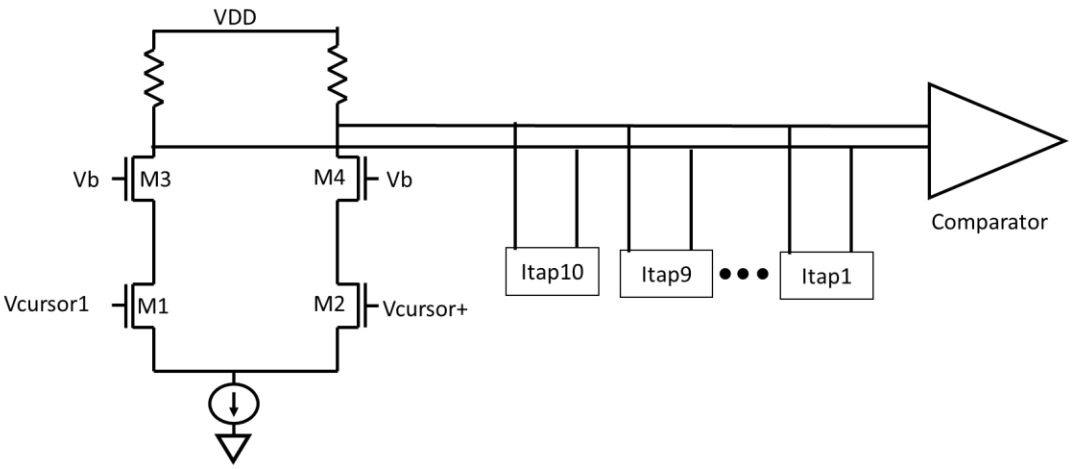

Figure 44:DFE Summer stage

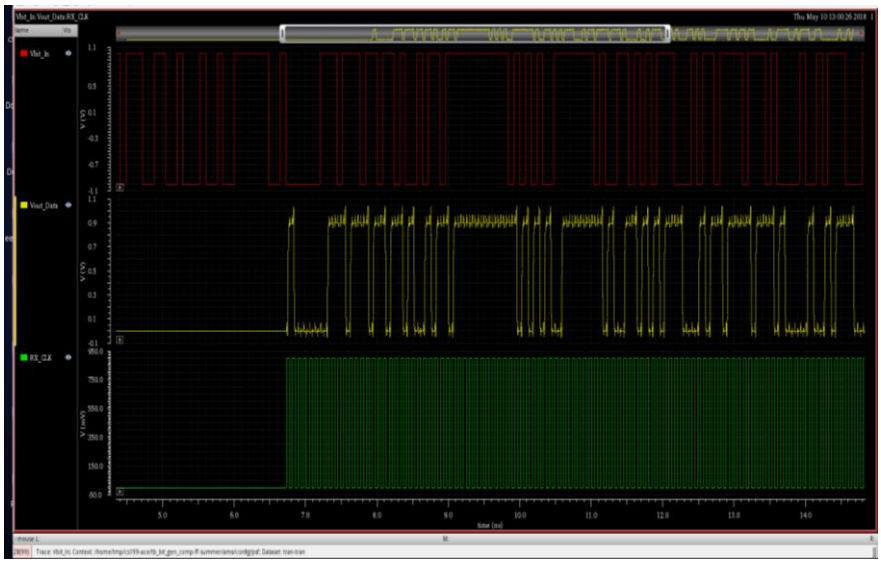

Figure 45:Output of the DFE with the Summer, Comparator and flip flop inserted

As shown in Figure 46, the summer output node settles within 26ps. We simulated the summer after loading with the comparator and also added 50fF loading capacitance to emulate external parasitic capacitances.

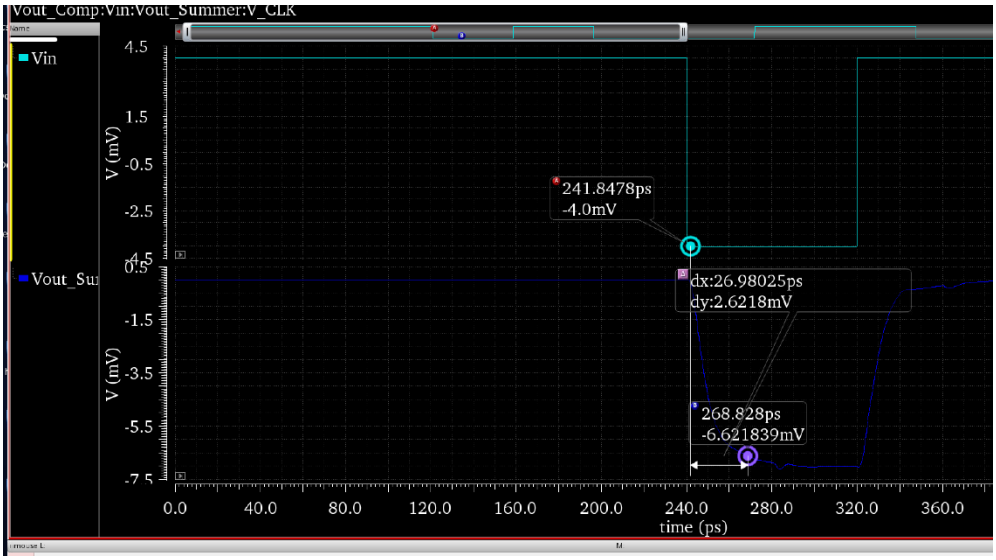

Figure 46. Output of DFE summer when loaded with the comparator and 50fF capacitive load

4.3.3. DFE Adaptation

For the DFE to correctly cancel ISI for different channels, the DFE tap currents needed to be adapted. An adaptation loop was implemented using the Sign-Sign Least Mean Squares (SS-LMS) algorithm. In this adaptation scheme, one loop generates a reference voltage, dlev, that is used to compare with the data level. The dlev voltage is output by an 8-bit DAC controlled by an up/down counter. The counter value increases when the error signal (current data level compared to dlev) is high and decreases when dlev is lower than the current data level. To simplify the circuit and reduce the need for another comparator, the dlev loop only updates when the current bit is a '1'. Only updating on '1's slows down the adaptation convergence, since it is updating less frequently. However, this is generally not an issue for backplane channels, where changes in the channel characteristics happen very slowly (due to temperature/humidity changes, etc.).

The tap coefficients are then adapted using the same error signal (current data level compared to dlev) using the following equation, where w_n is the n^{th} tap coefficient, e is the dlev error signal, and d is the data bit:

$$w_n[k+1] = w_n[k] + e[k] * d[k-n]$$

The 6-bit tap coefficients are then used to control current DACs that set the tap tail currents for the DFE summer.

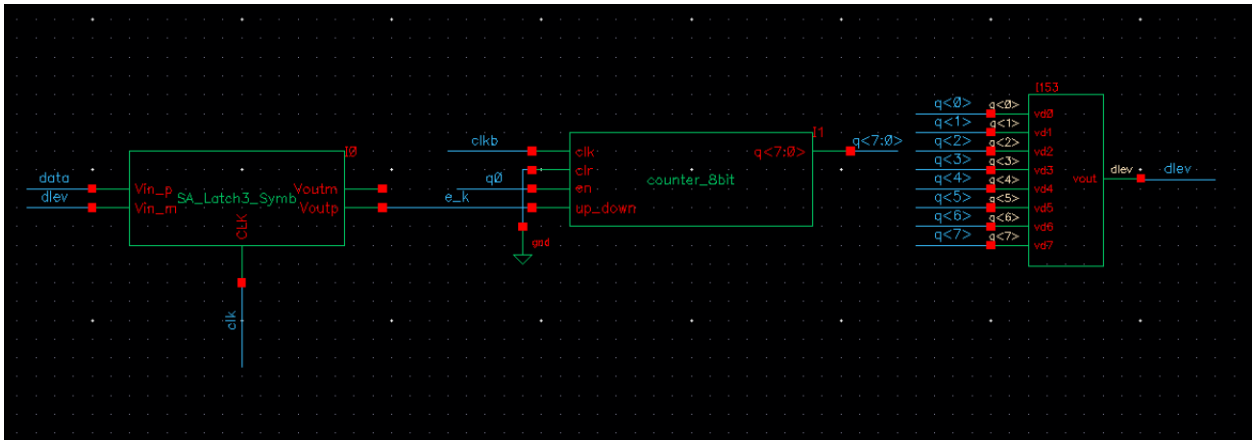

Figure 47. dlev loop schematic.

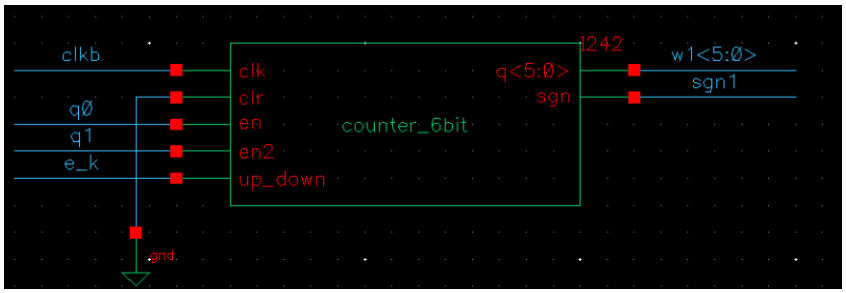

Figure 48. 1st tap adaptation schematic, representative of other 9 tap schematics.

We ran initially ran full system simulations. However, an alternate faster technique is to use impulse responses and convolve them with random data streams. Therefore, the DFE adaptation was simulated for each channel by generating the ISI by summing time delayed values of a random data stream weighted with coefficients corresponding to the channel impulse response. The results are shown in Figures 49 through 53.

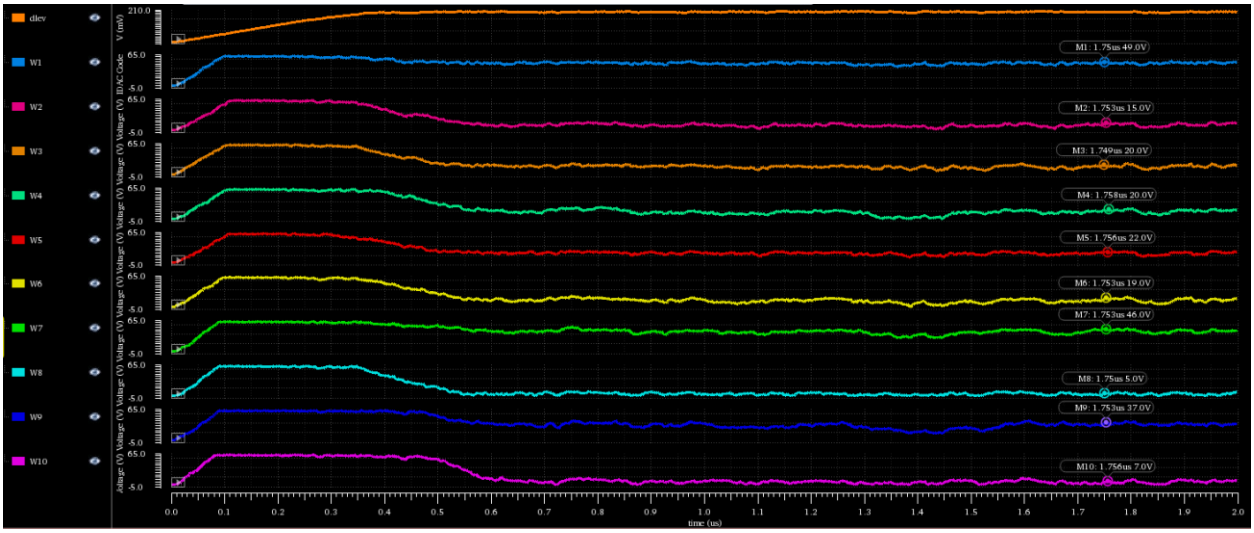

Figure 49. Adapted tap coefficients for the first channel.

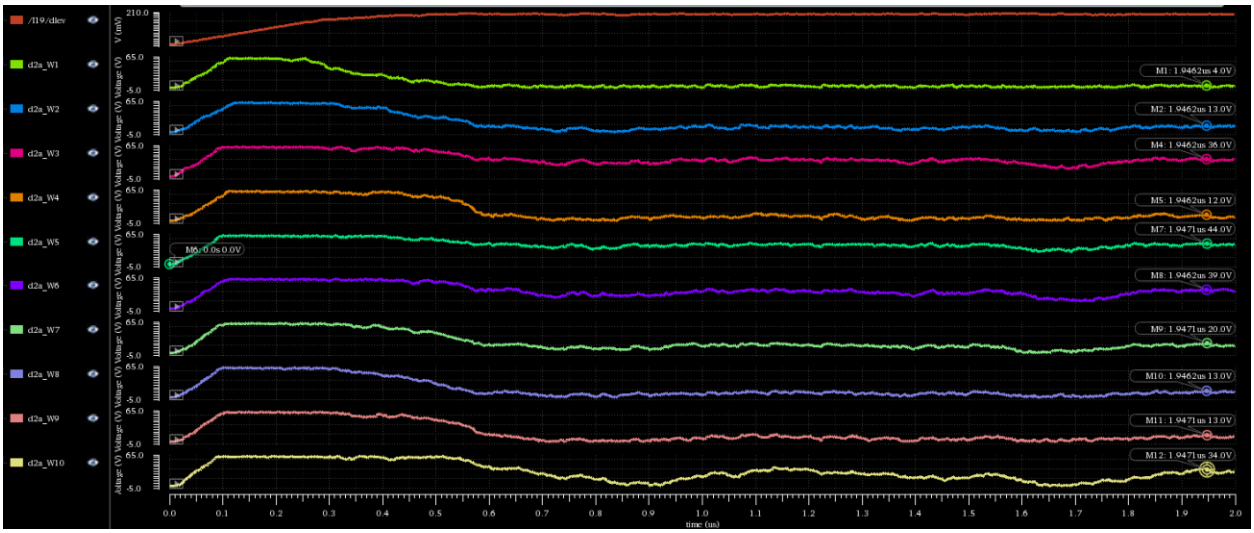

Figure 50. Adapted tap coefficients for the second channel.

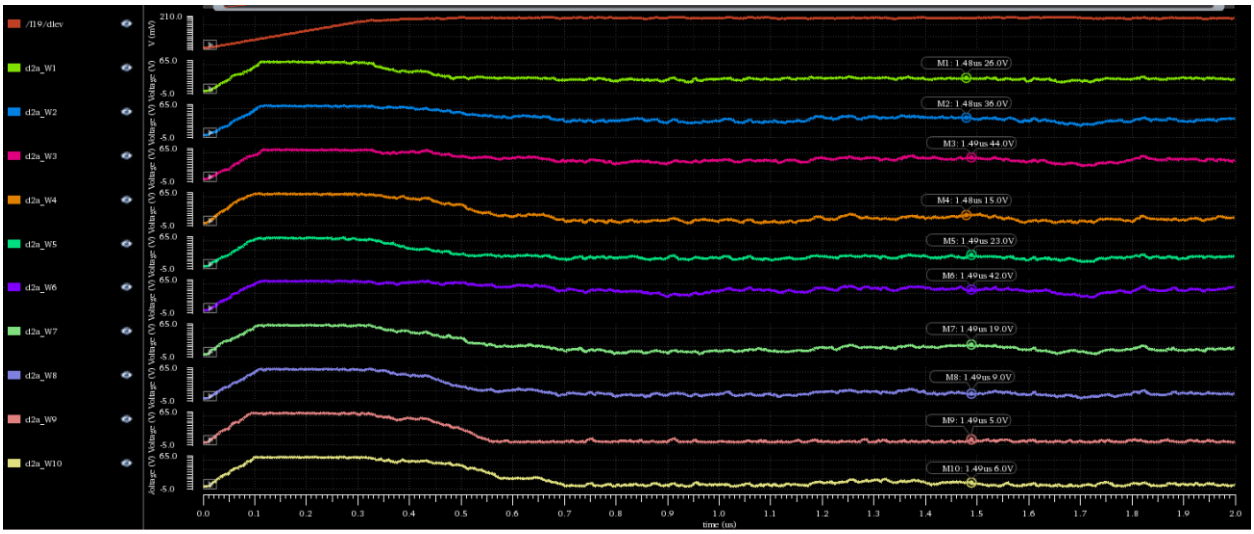

Figure 51. Adapted tap coefficients for the third channel.

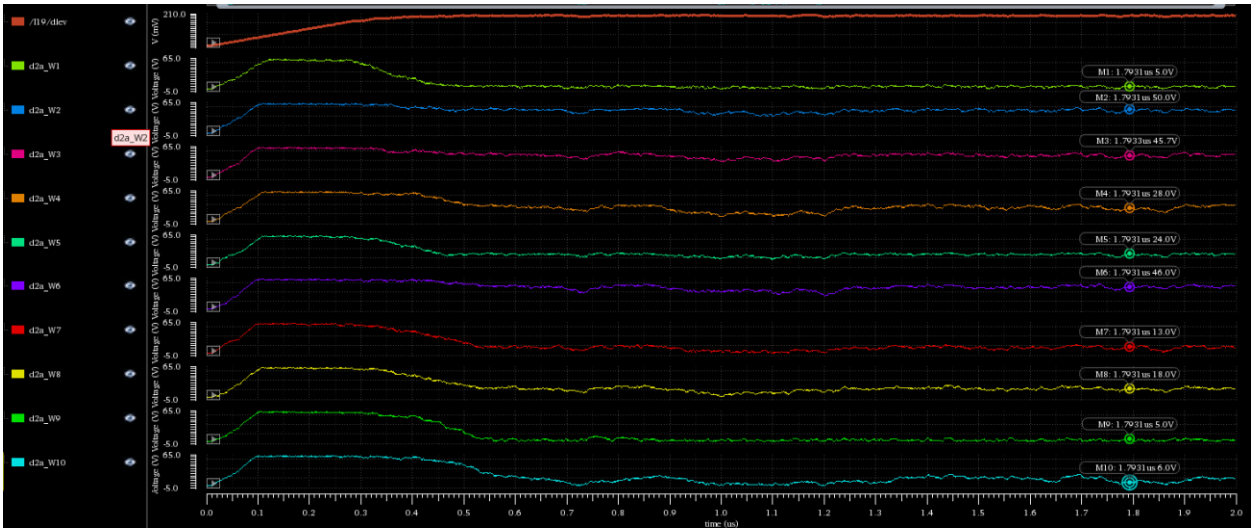

Figure 52. Adapted tap coefficients for the fourth channel.

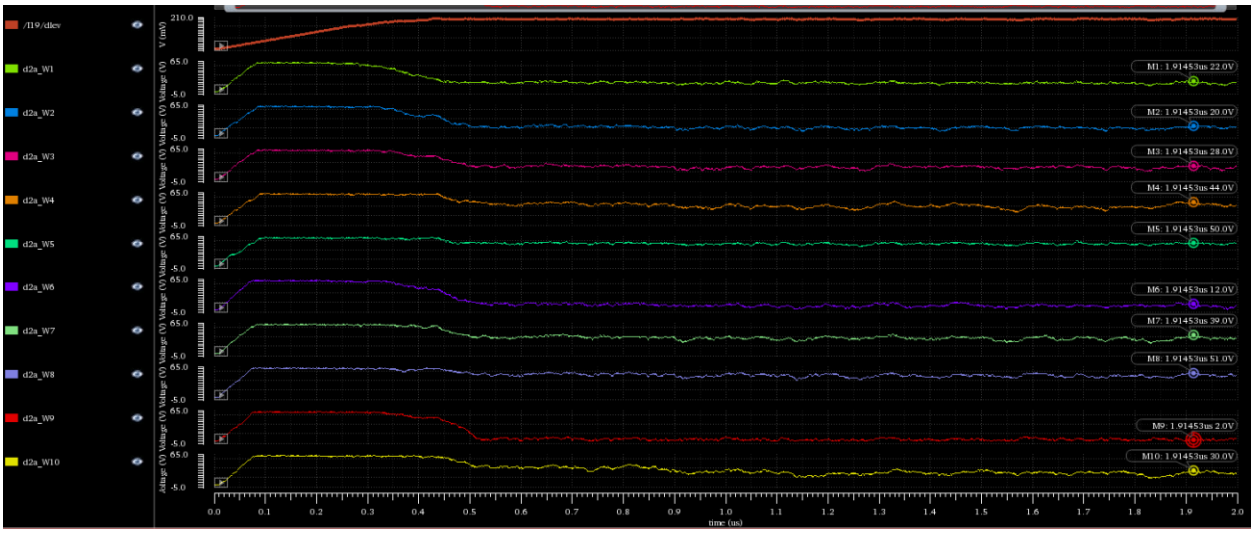

Figure 53. Adapted tap coefficients for the fifth channel.

Table 7. Expected vs. adapted tap coefficients for the five channels. The adapted values closely matched the expected values.

	Channel 1		Channel 2		Channel 3		Channel 4		Channel 5	
	Expected IDAC Code	Adapted Value	Expected IDAC Code	Adapted Value	Expected IDAC Code	Adapted Value	Expected IDAC Code	Adapted Value	Expected IDAC Code	Adapted Value
w1	49	49	4	4	29	26	6	5	21	22
w2	15	15	13	13	40	36	51	50	21	20
w3	21	20	37	36	47	44	50	46	30	28
w4	22	20	11	12	19	15	34	28	43	44
w5	21	22	44	44	24	23	25	24	51	50
w6	20	19	39	39	53	42	50	46	13	12
w7	47	46	18	20	20	19	15	13	37	39
w8	7	5	12	13	18	9	22	18	51	51
w9	40	37	13	13	0	5	4	5	5	2
w10	16	7	37	34	18	6	21	6	40	30

5. PLL and Clock and Data Recovery

5.1. PLL

5.1.1. Topology

The PLL for the transmitter clock was implemented using the typical charge pump topology with a current-starved ring oscillator for the VCO.

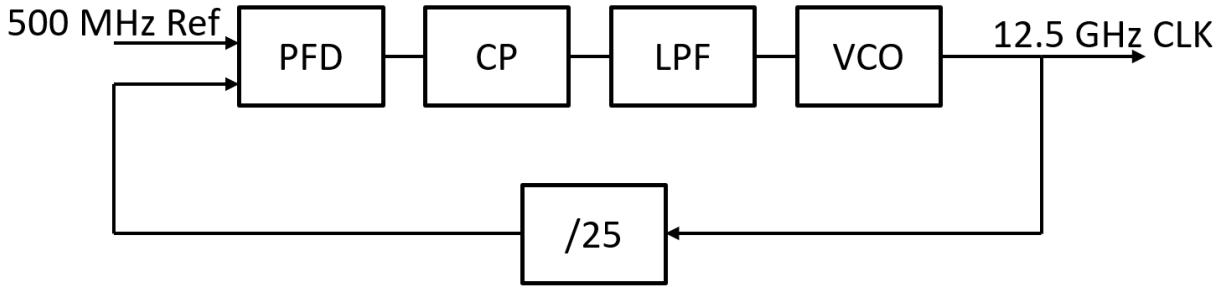

Figure 54. PLL block diagram

Table 8. PLL Specifications

Charge Pump Current, I_{CP}	1 mA
Divider Ratio, M	25
Filter Bandwidth	17.5 MHz
K_{VCO}	42.6 GHz / V

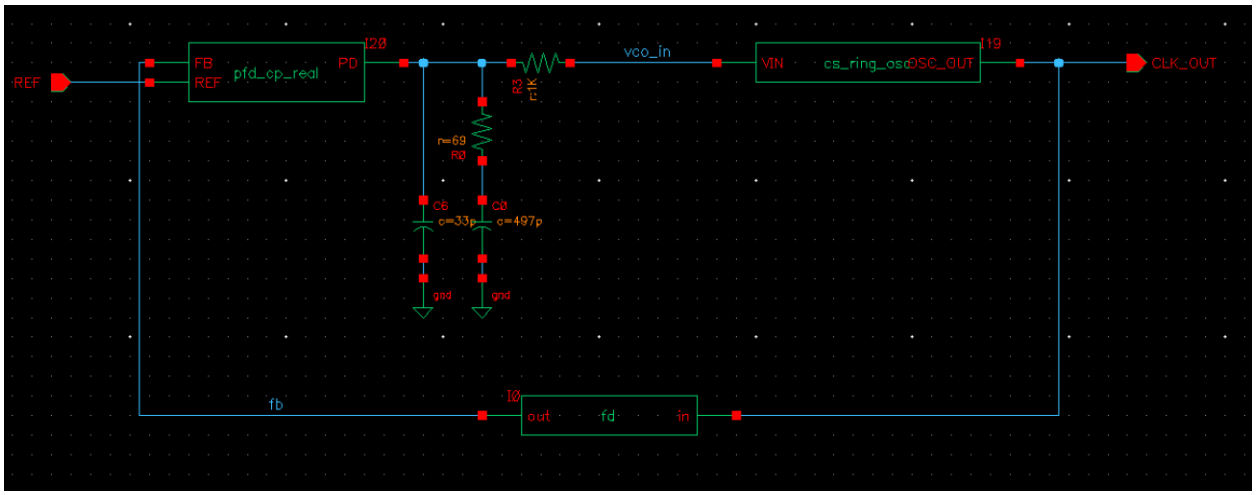

Figure 55. PLL schematic

5.1.2. Phase Frequency Detector

The PFD was implemented using the conventional topology [2] shown in Figure 56, which generates UP pulses when the PLL output clock (divided by 25) is slower than the reference clock, and DN pulses when the PLL output clock is fast compared to the reference. The width of the UP and DN pulses is proportional to the phase difference between the inputs.

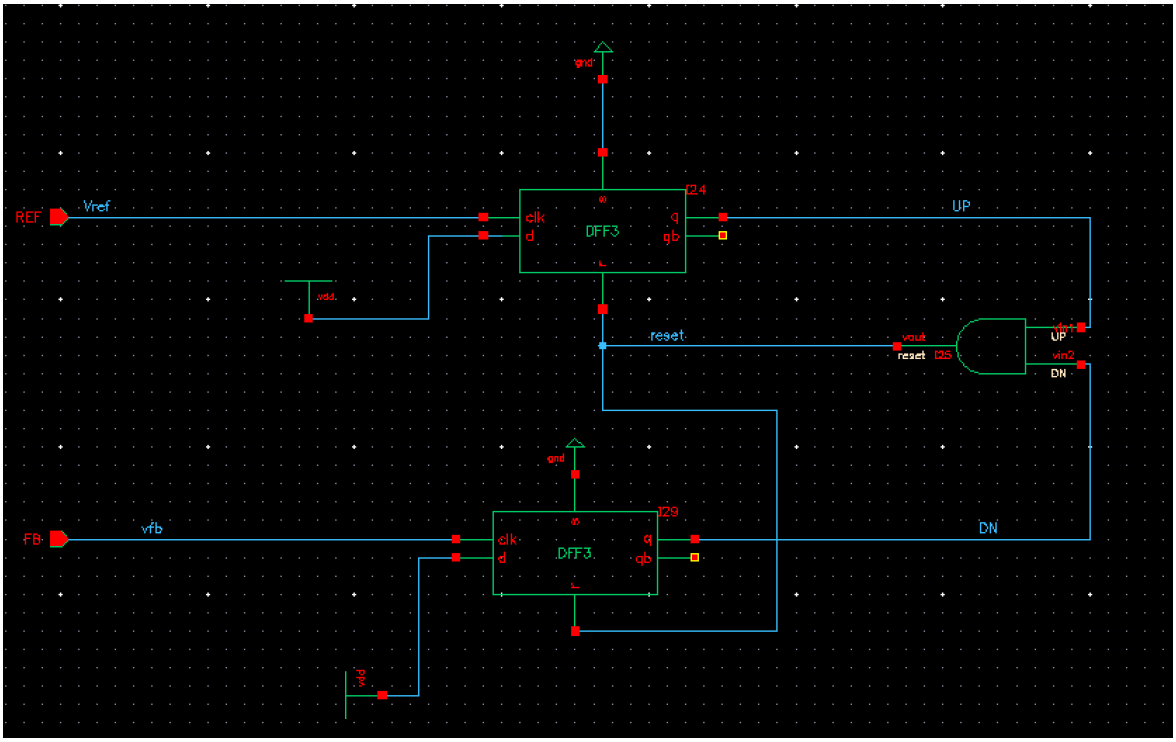

Figure 56. PLL PFD schematic

5.1.3. Charge Pump (CP)

The purpose of the charge pump is to convert the UP and DN pulses from the PFD into currents that either push or pull current from the loop filter. It is critical that the magnitude of the up and down currents match to avoid a steady-state offset in the PLL output frequency. The original topology used was from [3] with an error amplifier to improve current matching, but it was noticed that the currents matched closely without the amplifier so it was removed.

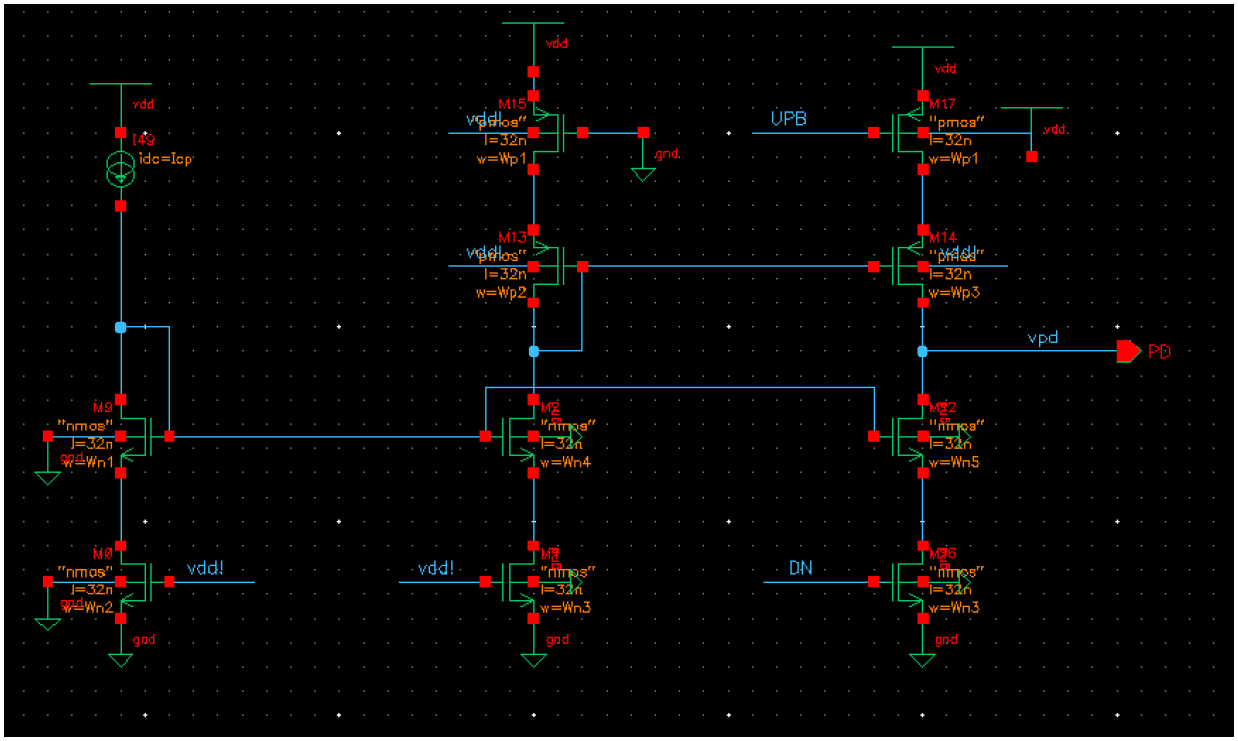

Figure 57. PLL CP schematic. Icp = 1 mA

5.1.4. Voltage Controlled Oscillator (VCO)

A current-starved ring oscillator was used for the PLL VCO. The control voltage is used to change the current available for the inverters. Increasing the control voltage increases the current which allows the inverters to switch faster, and likewise decreasing the control voltage decreases the current and slows down the inverters. The current-starved topology keeps the supply voltage constant, so level shifting is not required at the output and the main supply can be used. However, a separate regulator might be needed to reduce the impact of supply noise on the oscillator frequency.

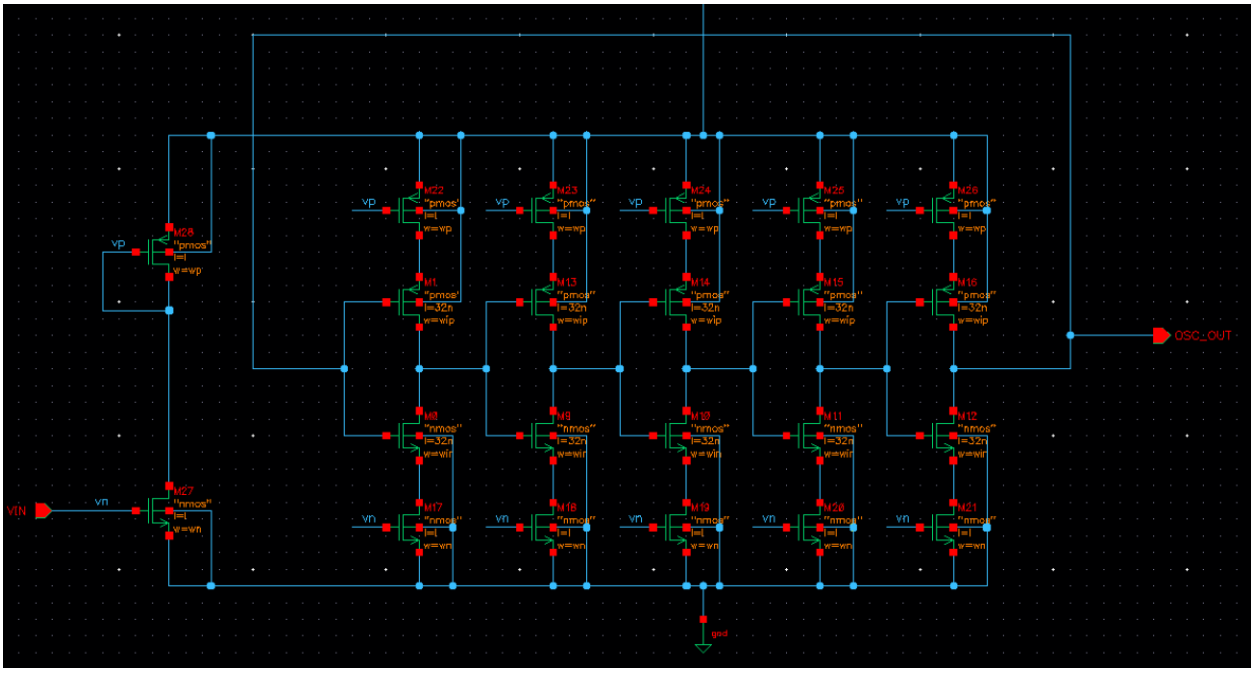

Figure 58. PLL VCO (current starved ring oscillator) schematic

Table 9. VCO device sizes

Wip	96 nm
Win	64 nm
Wp	1.536 um
Wn	1.024 um
L	32 nm

5.1.5. Simulation

Simulations showed that the PLL locks to the correct frequency of 12.5 GHz with a start-up time of ~ 450 ns.

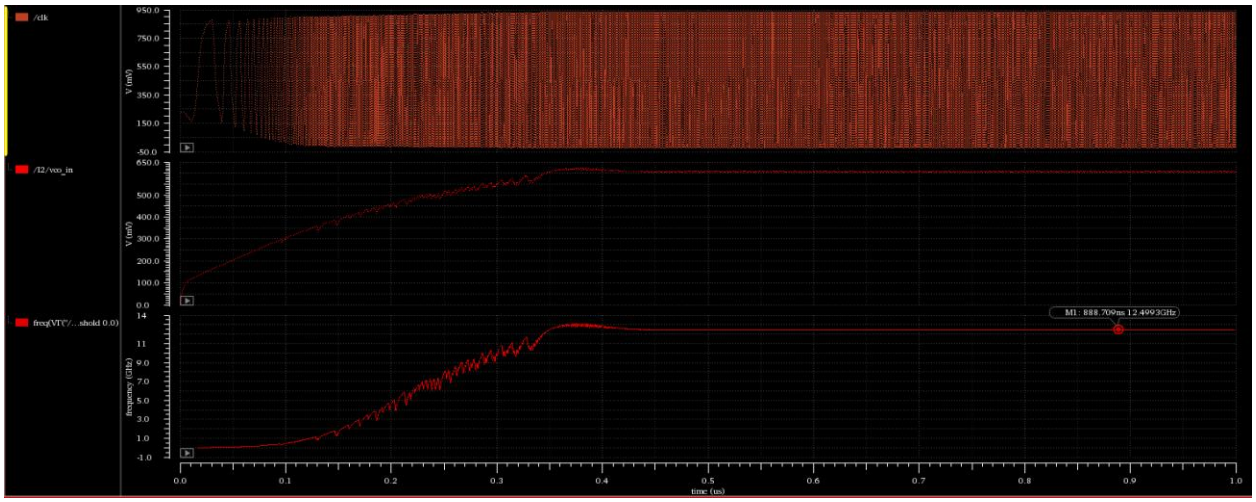

Figure 59. PLL simulation showing correct lock frequency of 12.5 GHz

5.2. Receiver Clock and Data Recovery (CDR)

5.2.1. Overview

A dual-loop CDR topology was implemented for the receiver to be able to recover the clock from the input data stream. The circuit uses a PLL similar to the transmitter PLL, except the VCO is a multi-phase cross-coupled current-starved ring oscillator. This VCO generates the multiple clock phases needed for the CDR phase interpolator. The CDR loop uses a bang-bang phase detector to generate up and down signals for the digital control logic. This digital logic sends control signals to the phase interpolator, indicating which two clock phases to interpolate as well as the tail current ratio to set the phase weighting.

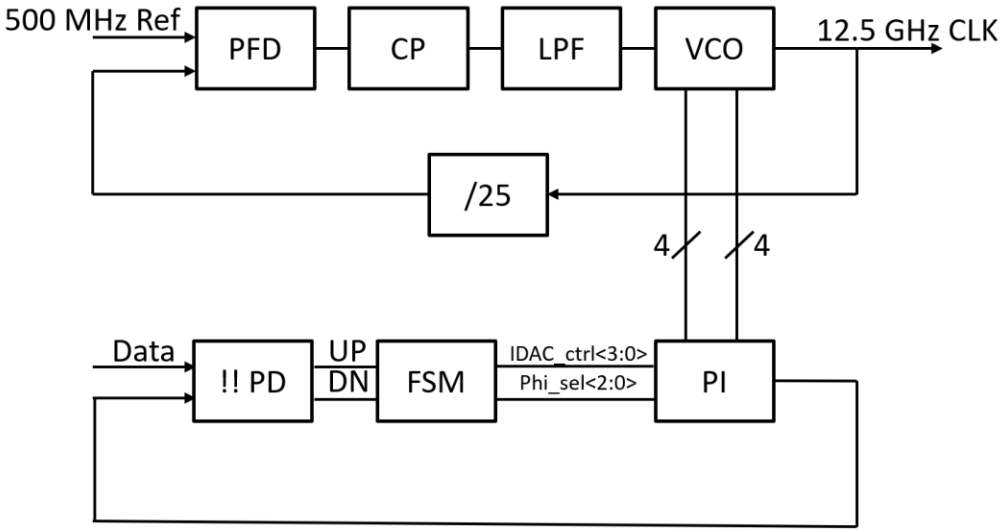

Figure 60. Block diagram for the receiver dual-loop CDR.

5.2.2. Cross-coupled VCO

The VCO from the TX PLL could not be used for the CDR, since an even number of clock phases were needed. A four-stage cross-coupled current-starved ring oscillator was used to generate the eight clock phases, with the frequency tuning still provided by current starving.

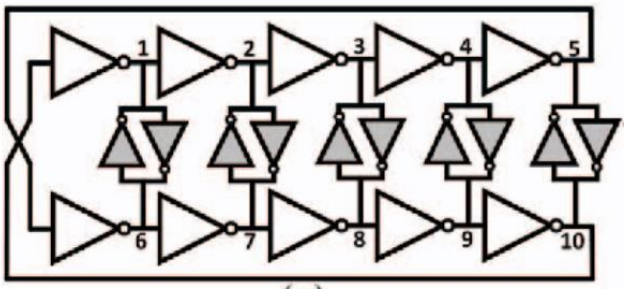

Figure 61. Block diagram of a cross-coupled ring oscillator [3]. The VCO implemented in this project uses four stages instead of the five shown here.

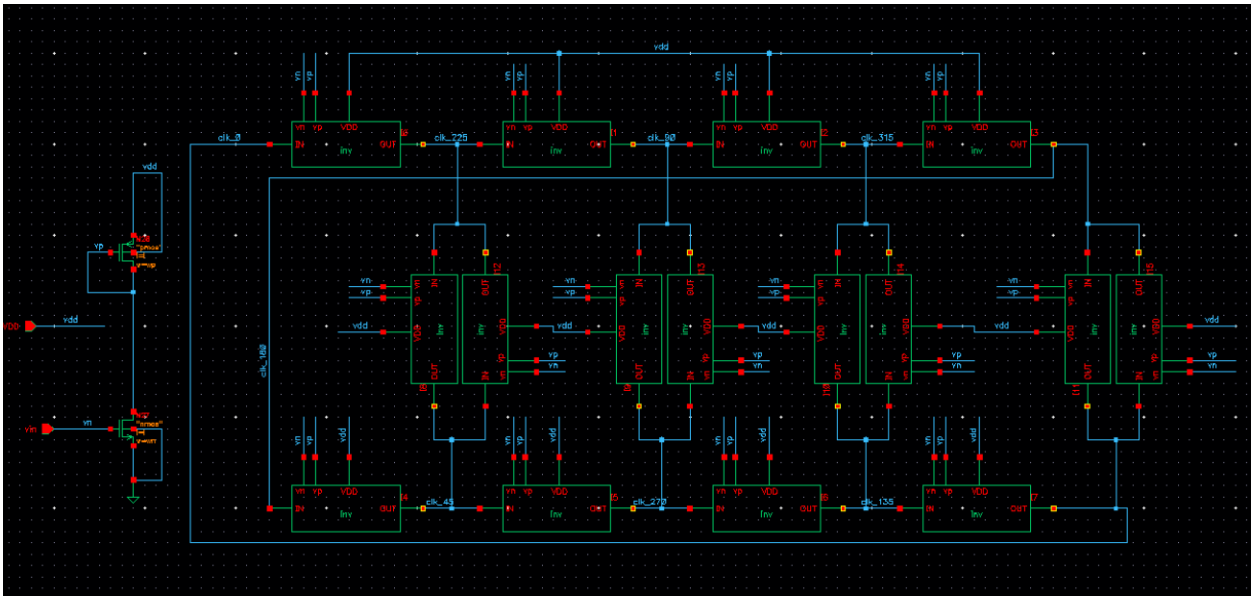

Figure 62. Cross-coupled current-starved ring oscillator schematic for the PLL in the receiver CDR.

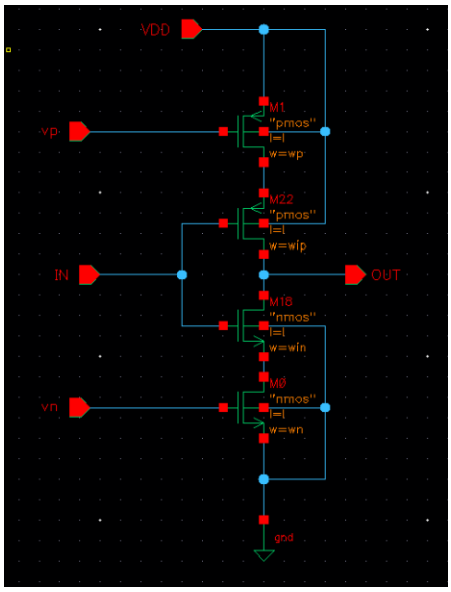

Figure 63. Current-starved inverter schematic used in the VCO of Figure 57. Wn = 1.28 um, Wp = 1.92 um, Win = 64 nm, Wip = 96 nm, L = 32 nm

5.2.3. Phase Detector (PD)

The CDR phase detector was implemented using a bang-bang phase detector as shown in Figure 64.

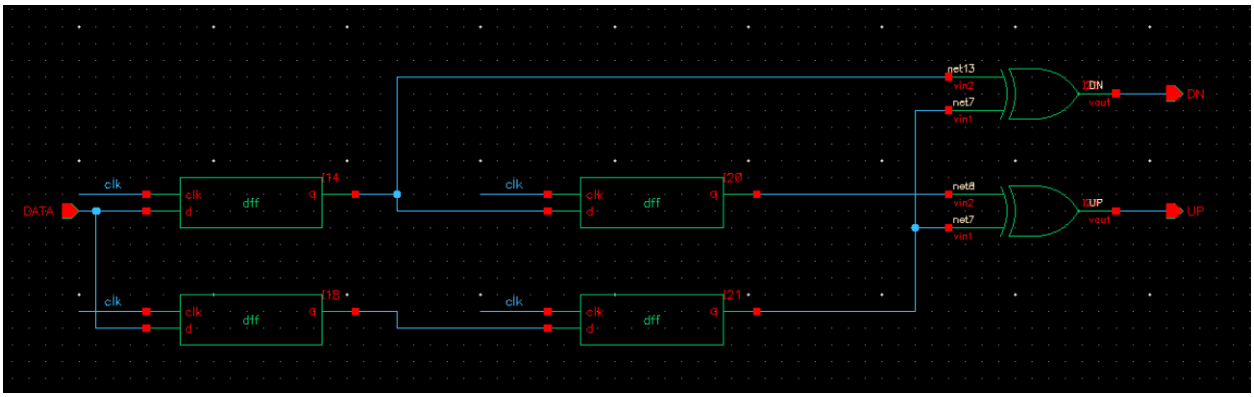

Figure 64. Bang-Bang phase detector schematic

5.2.4. Phase Interpolator

The digital control logic selects two clock phases based on the current phase error, which are passed to the phase interpolator with 8 to 1 multiplexers. A CML phase interpolator was used to interpolate between the two selected clock phases. The ratio of the bias currents between the two differential pairs selects how to weight the two phases. The settling time of the PI output had to be made slow enough to create a smooth output.

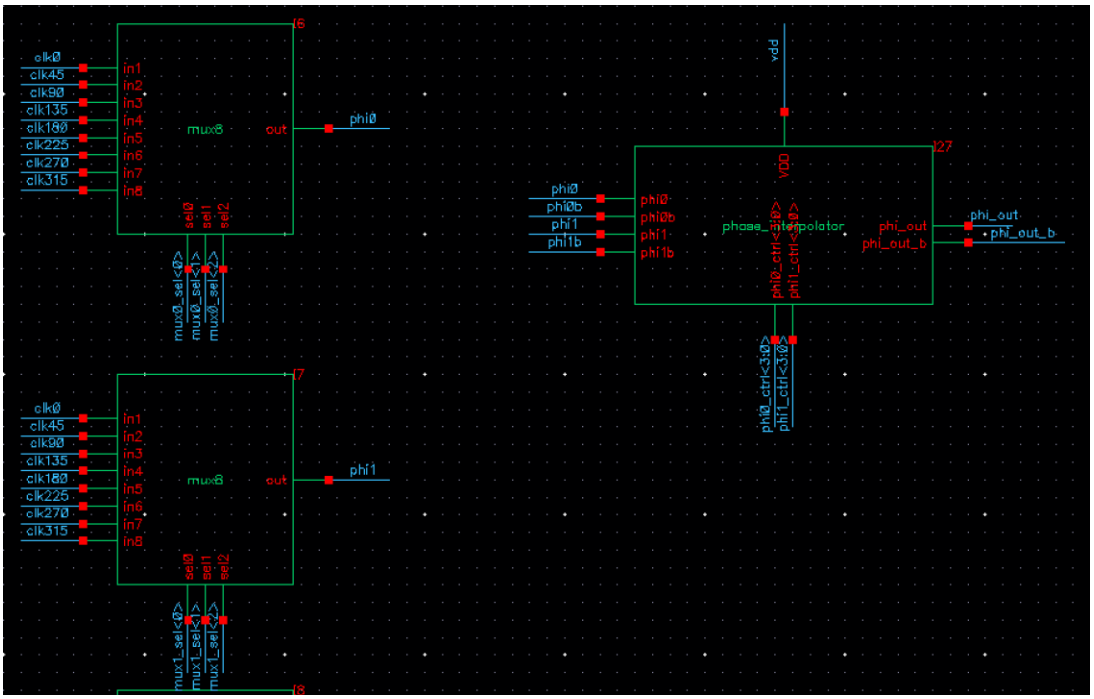

Figure 65. Schematic showing the 8 to 1 multiplexers and the phase interpolator.

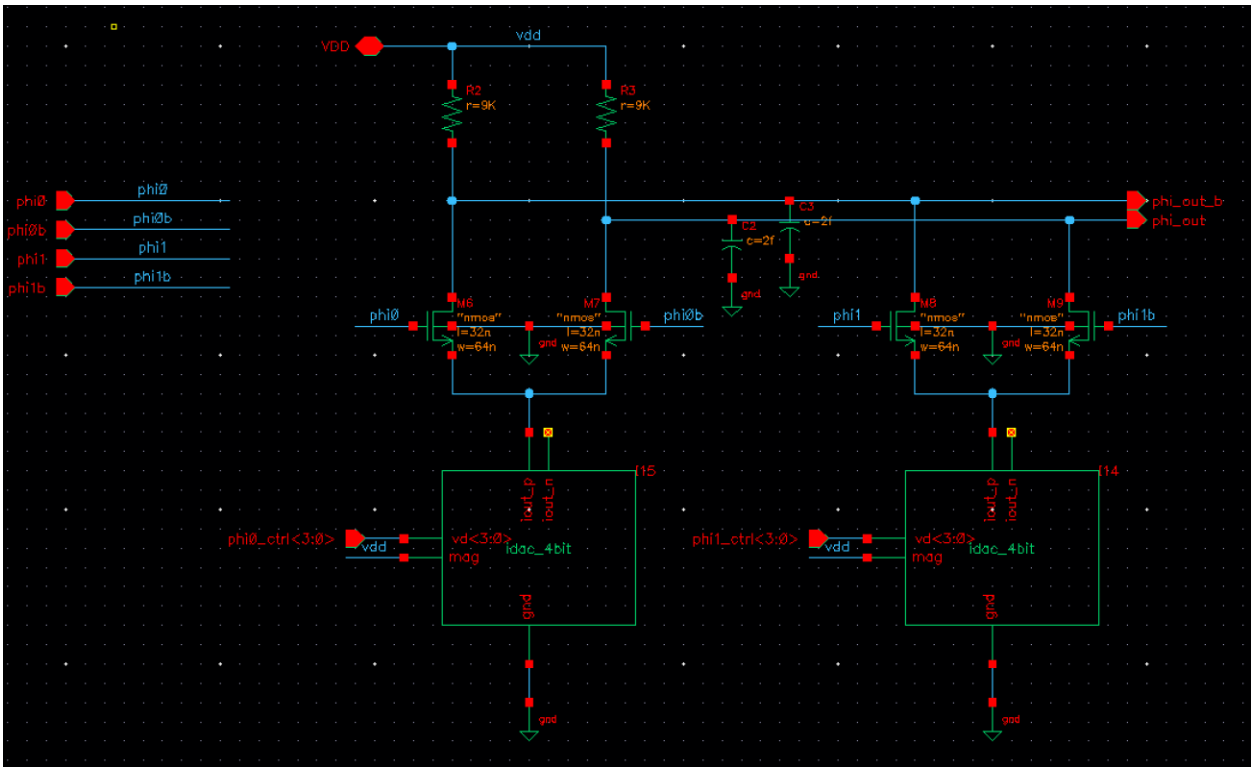

Figure 66. Phase interpolator schematic. Wn = 64nm, L = 32 nm. The IDAC current range is 100 uA.

5.2.5. Multiplexer

8 to 1 multiplexers were implemented using transmission gates to pass the selected clock phases to the phase interpolator.

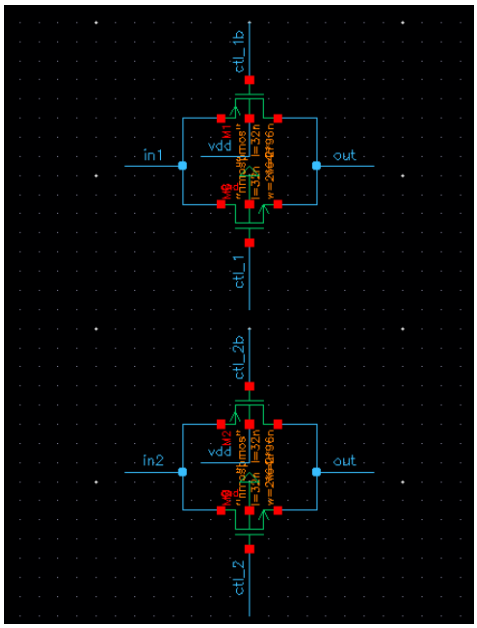

Figure 67. Partial schematic of the 8 to 1 multiplexer showing two of the eight transmission gates. Wn = 128 nm, Wp = 192 nm, L = 32 nm.

5.2.6. Simulation

The dual loop CDR was simulated using an alternating bit pattern as the input data. For this simulation, the multiplexers were implemented in VerilogA. Figures 68 and 69 show that the CDR output clock successfully locked onto the data. The output clock jitter was determined to be ~3.8 ps.

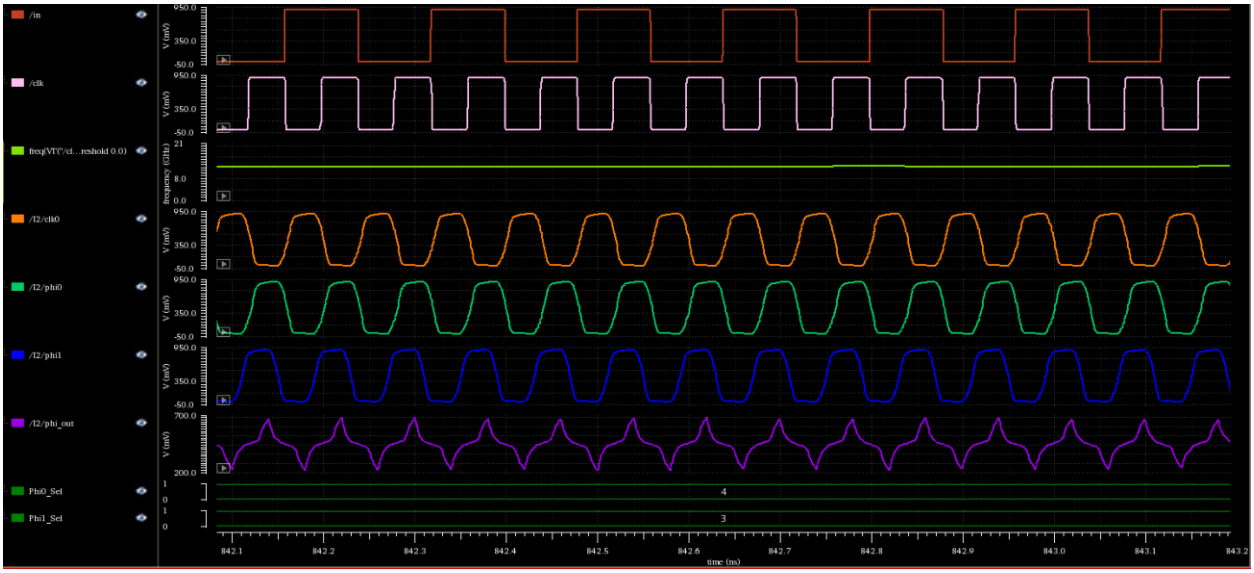

Figure 68. CDR simulation waveforms showing the recovered clock (pink) tracking the input data stream (red). The two input clocks to the PI, phi0 and phi1, are shown in green and blue, respectively. The CML PI output is shown in purple. This simulation

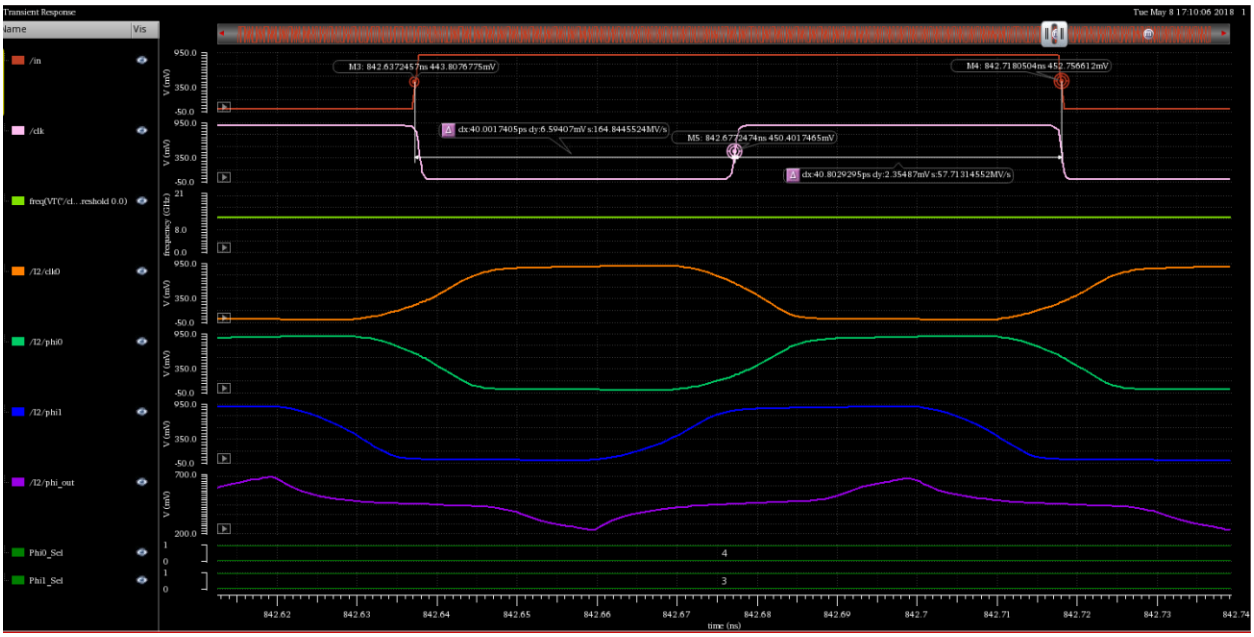

Figure 69. Zoomed in view of the CDR simulation waveforms showing the recovered clock (pink) tracking the input data stream (red).

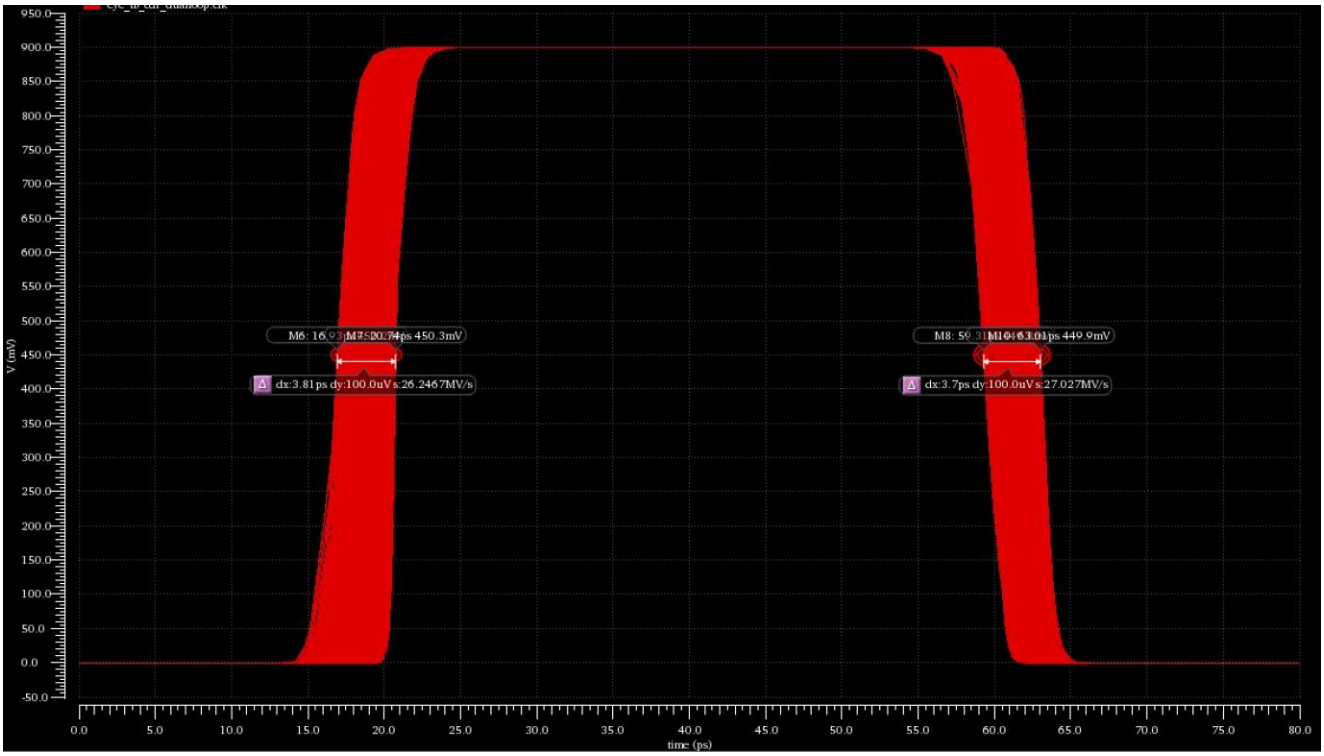

Figure 70. CDR simulation showing a jitter of ~3.8 ps.

6. Results

6.1. BER Estimation

A worst-case BER analysis was performed to determine if the system would meet the BER requirements for all channels. When using an offset voltage of 30 mV to account for timing errors and a noise measurement of 3 mV, the following BERs are achieved for the five channels. The BER for the 5th channel is when manually setting the CTLE adaptation control voltage, as there was an issue with getting it to properly adapt due to the channel characteristics being significantly different than the others. BER was calculated using the following equation:

$$BER = \frac{1}{2} erfc\left(\frac{V_{cursor} - \Sigma ISI_{total} - V_{offset}}{\sqrt{2}\, V_{noise}}\right)$$

Table 10. Estimated BER for the system on the five channels.

	BER
Channel 1 (30-inch Top)	$7.5*10^{-68}$
Channel 2 (30-inch Bottom)	$1.8*10^{-87}$
Channel 3 (20-inch Mid)	$4*10^{-129}$
Channel 4 (10-inch Mid)	$1.4*10^{-54}$
Channel 5 (1.5-inch Top)	$9.1*10^{-17}$

An alternate approach to analyze the channel performance is to use statistical BER analysis. We did investigate the Stateye® program for this. However, given our time and manpower constraint, we did a worst case BER analysis.

6.2. Power Consumption

The system power consumption was estimated based on the simulated bias currents for the different blocks along with estimates for the switching power consumption based on the device capacitances. The system power consumption was estimated to be ~17.5 mW.

Table 11. Estimated power consumption by circuit

	Power Consumption
DFE (Slicer + Summer + Logic)	9 mW
CTLE + Adaptation	3 mW
CDR	1.6 mW
TX	2.7 mW
TX PLL	1.2 mW
Total	**17.5 mW**

7. Conclusion

We designed and simulated an equalizer for 12.5Gbps backplane channels. The equalizer comprised of a 2 Tap Feed Forward Equalization (FFE) at the transmitter and a Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE) at the receiver. The main sub-circuits were designed using 32nm CMOS technology. Adaption was implemented and the channel coefficients converged to the desired values. Besides equalization, we also designed and simulated clock and phase recovery circuits including transmit Phase Locked Loop (PLLs) and receiver dual loop Clock and Data Recovery (CDR). Simulations showed convergence to the desired frequency and phase.

8. References

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