Design, Modeling and Control of the Integrated Stacked Resonant Switched Capacitor DC-DC Converter

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by

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University of California, Berkeley

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Abstract

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Mobile, wearable, and internet of things (IOT) electronic systems are typically powered by a single cell Lithium-Ion (Li-ion) battery. Increasing demand for battery life and the constraint of the overall platform size impose an emerging desire for an efficient and compact power conversion stage that can directly deliver power from the battery, which ranges from 3.2V to 4.2V, to the supplies of application/communication processors in the range of 1V. The conventional buck converter, dimensioned for the 3.2-4.2 V input range, requires switches that are not typically available in standard sub-micron CMOS technology. Efficient implementation of the conventional buck converter has required a rather bulky off-chip inductor. The switched capacitor (SC) converter, though promising for a fully integrated solution, is inefficient at voltage regulation and is limited in capacitor energy utilization. In addition, with the SC converter, to cover the input range of a Li-ion battery to the processor supply voltage, topology reconfiguration has to be adopted. This additional functionality requires some additional design and implementation complexity.

Given the limitations of either pure inductive or pure capacitive converter topologies, various hybridized power conversion architectures have been proposed recently. The hybrid approaches leverage minimum magnetic components to mitigate the intrinsic charge sharing loss in the standard SC operation while still maintaining a better switch utilization inherent in some SC topologies. This thesis introduces a hybrid dc-dc converter topology named stacked resonant switched capacitor (Stack-ResSC) that eliminates charge sharing losses with a small inductor. Consequently, capacitor energy utilization is improved and lossless voltage regulation is enabled. Since the necessary inductance is small, the magnetic component can still be tightly integrated within the package with a PCB trace or a bondwire. The proposed topology can also adapt to any N-to-1 conversion ratio, which extends the topology for wider applications. Harmonic averaging is used in this thesis to develop the large and small signal model of the converter. A tight load line regulation can be effected with the designed controller according to the developed small signal model.

In addition to the Stack-ResSC, this thesis also introduces the stacked dual active bridge (Stack-DAB) as a derivative of the Stack-ResSC. An integrated circuit example is demonstrated with a nominal 3:1 conversion ratio. It supports a 3.2V-4.2V input voltage with a continuous output regulation of 0.8V-1.5V. The circuit delivers 83.4% efficiency at a power density of 0.46 W/mm^2. The converter also shows superior transient response compared to state-of-art integrated implementation. This work demonstrates the advantage of the proposed hybrid approach in terms of tight integration and voltage regulation. The scope of the resonant switched capacitor based DC-DC converter is thus further extended.

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Acknowledgments

Dedicated to my wife, my parents, my advisor and friends, who have been unwavering in their love and support during my PhD.

Chapter 1

Introduction

1.1 Power Management for Mobile Application

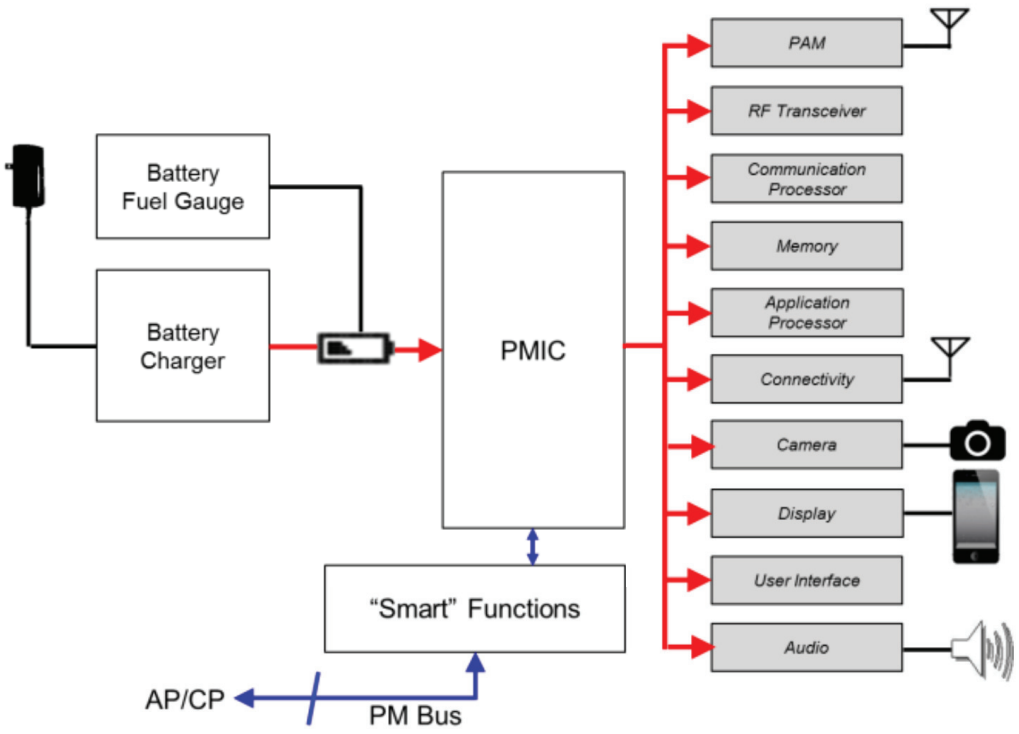


Figure 1.1: The standard power management architecture in a mobile platform [1]

Fig. 1.1 shows the standard system architecture of a mobile device. The power management integrated circuit (PMIC) is the central piece that bridges the battery with the application/communication processors and various other functional blocks. The processor cores

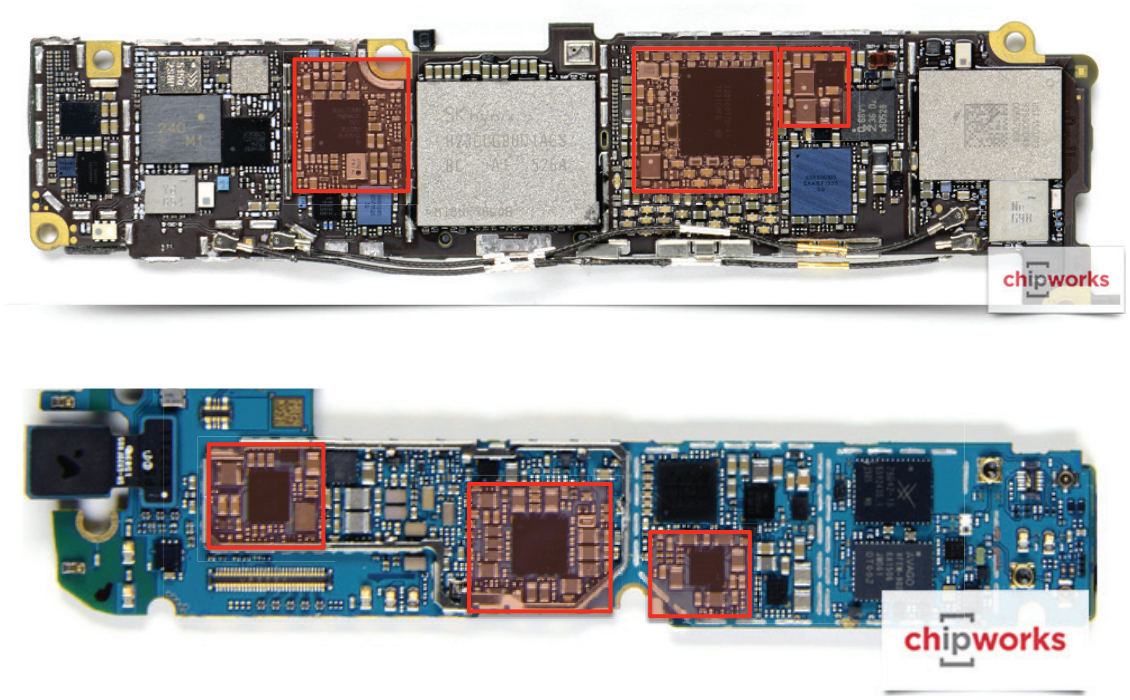


Figure 1.2: The mother boards of iPhone 6s and Samsung Galaxy S5

and other hardware components require a range of supply voltages with distinct load/line regulation and power sequences. A PMIC consists of a set of DC-DC converters to support these needs and is an essential part for ensuring the proper operation of a mobile device.

Fig. 1.2 shows the mother boards of a iPhone 6s and Samsung Galxy S5. The red zones highlight the areas taken by the PMICs and their peripheral passives components, which comprise more than 30 percent of the mother board's total area. This scenario imposes an emerging desire for a more compact power management platform to reduce or eliminate discrete components. In this way, the overall footprint can be reduced and BOM cost can be saved.

A fully integrated dc-dc converter is the way towards a more efficient and compact power management architecture. With the removal of off-chip passive components, the voltage regulator can be placed in close proximity to the processor core or other IP blocks on the same chip. A finer-grained voltage regulation can be realized. This can enable a much faster dynamic voltage scaling (DVS) in the modern multi-core processors. Moreover, each core can operate under its individual optimal supply voltage to save more energy [2].

1.2 Reviews of Approaches to the Fully Integrated DC-DC Power Converter

The DC-DC converter can be divided into two main categories: the linear regulator and the switch mode regulator. A low-dropout regulator (LDO) is an example of a linear regulator. The efficiency of a linear regulator is determined by its voltage conversion ratio. Thus, a linear regulator is inefficient in an application with a high voltage conversion ratio. The buck converter is the dominant switch mode voltage regulator. A buck converter can operate efficiently across a wide range of input and output voltages. The major drawback of a buck converter is the requirement of a large inductor. Though increasing switching frequency can shrink the size of magnetics, the compromise of efficiency degradation with the increased switching loss limits the reduction of passive components.

In recent years, the switched capacitor (SC) converter has emerged as a promising candidate for fully integrated chip level power delivery [3, 4, 5, 6, 7, 8, 9, 10]. In contrast to the buck converter [11, 12, 13, 14, 15], the switched capacitor solutions are compatible with advanced CMOS processes, since circuits can be readily arranged using on-die capacitors, and integrated switch devices without overstress. As is known, the intrinsic charge sharing loss of the SC conversion process limits the performance of the SC converter. There is a fundamental compromise between efficiency and power density given an available capacitor technology in a standard CMOS process [16, 17].

Fig. 1.3 shows the recent state of art integrated switched capacitor DC-DC converters. The converter examples [8, 9, 10] using 65nm or 90nm bulk CMOS technology achieves medium performance. The works [6, 7] adopt more advanced CMOS process pushing the performance toward the corner around $1W/mm^2$ power density and 80% efficiency. As shown in the chart, given a certain CMOS process, there is a performance trade-off between efficiency and power density. Using advanced technology nodes can move the performance contour towards the right-top corner in the chart. Adoption of more advanced CMOS technology can offer switch devices with a better figure-of-merit and capacitors with a higher density. Moreover, with the availability of deep trench capacitor, the performance limit can be further improved. The deep trench capacitor technology can provide more than 200 $fF/\mu m^2$ capacitor density. That is much higher than what is achievable in a standard CMOS process. The examples [3, 4, 5] represent the bench-marking SC works leveraging both advanced CMOS processes and deep trench capacitors.

As is known, the SC converter is inefficient in voltage regulation, due to its discrete conversion ratio nature. In order to support a wide input (or output) voltage range, topology reconfiguration has been adopted [18, 19, 20, 21, 22, 23, 24]. The few battery connected examples reported to date suffer from low efficiency and/or low power density [25] [26]. The added re-configurable functionality requires some additional design and implementation complexity. Fig. 1.4 plots a few representative works with re-configurable SC topologies. From the figure, the performance contour that illustrates the efficiency and power density compromise still exists. And the performance is especially worse with large conversion ra-

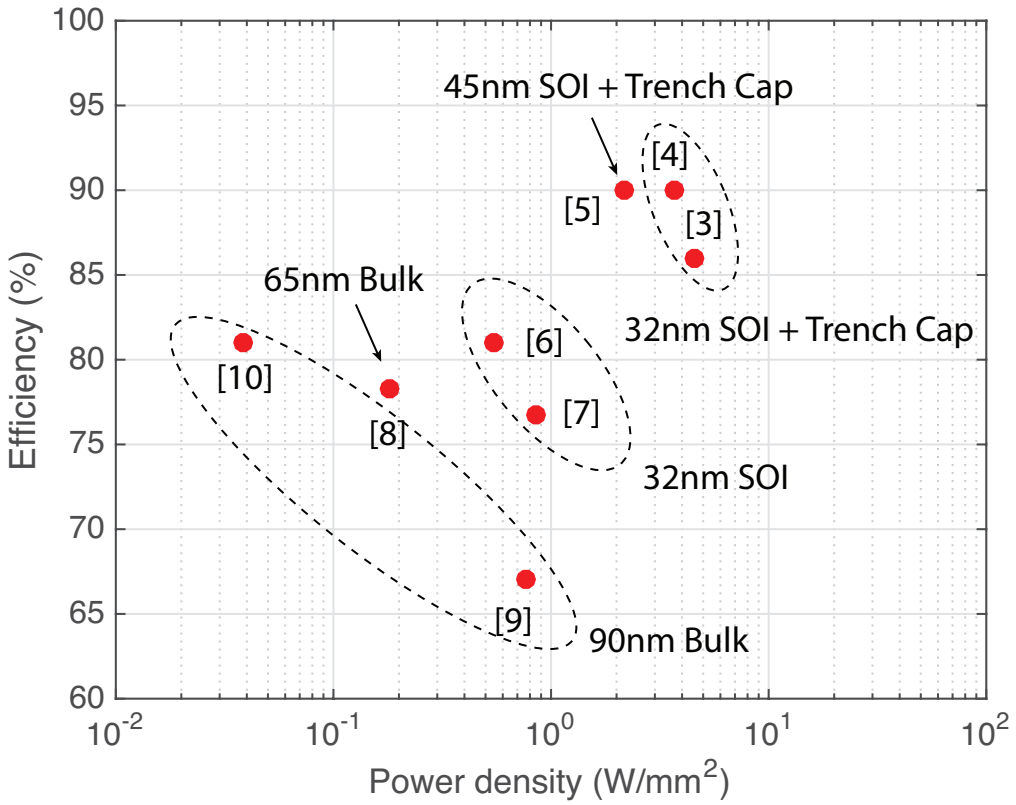


Figure 1.3: State-of-art integrated switched capacitor based dc-dc converters: efficiency vs power density

tios. In addition, the auxiliary switches and additional parasitic capacitors that come from different configurations complicate the system design and optimization.

In all, all key limitations of SC or re-configurable SC converters are attributed to the fundamental charge sharing loss. There are works showing that the charge sharing loss can be alleviated through the charge recycling of parasitic capacitor [27] or successive small step charge transfer with sophisticated phasing control [28]. Recently, hybrid approaches including multi-level buck, soft-charging switched capacitor (SC with an inductive stage) and resonant switched capacitor (ResSC) have been proposed to alleviate the drawback of SC based converters by introducing inductors into the SC topologies [29, 30, 31].

The hybrid approaches take advantage of better switch utilization that is inherent in some SC topologies while leveraging magnetics for mitigating instrinsic charge sharing loss and enabling efficient voltage regulation [32] [33]. Adding an inductive stage following a conventional SC converter can enable soft-charging of working capacitors. Depending on the topology of the SC stage, all or only part of the working capacitors can be soft charged with a single inductor [34]. Among various SC topologies, the serials-parallel SC is the one that

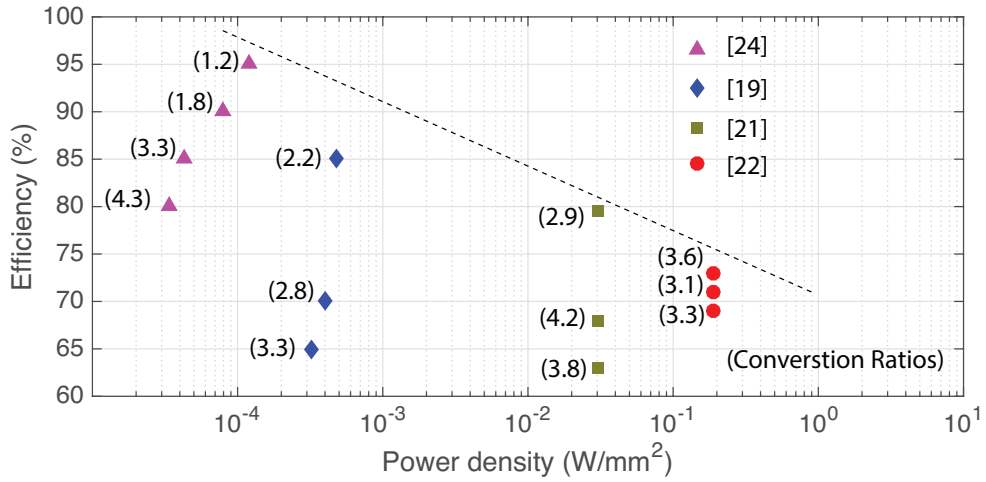


Figure 1.4: State-of-art reconfigurable switched capacitor dc-dc converter. The number in the parenthesis represents the normalized convertion ratio (V_{in}/V_{out})

can readily enable soft-charging for all working capacitors with a single inductor. During the normal operation, the inserted inductor is always on the charging or discharging path of each capacitor, maintaining lossless charge transfer. A few serials-parallel based soft-charging SC examples were successfully demonstrated [35, 36]. The Dickson SC converter features superior switch utilization compared with other SC topologies. However, to eliminate the charge sharing loss in a Dickson SC converter with a single inductor is challenging. Special timing and phase arrangement is needed to avoid charge transfer between the capacitors without an inductor in between [37, 38]. An integrated circuit example based on 4:1 soft-charging Dickson was recently demonstrated for the application of Li-ion battery power delivery with a discrete inductor and capacitors [30].

Multi-level converters has been proposed and widely used in the DC-AC application for reduced device rating and increased pulse frequency [39, 40]. Recently flying capacitor based multi-level converter has received attention in the application of DC-DC converter. Compared to a conventional buck, a N-level converter can effectively increase the switching frequency of the inductor by (N-1). Thus, the size of the inductor can be reduced. A few discrete examples has shown superior performance with reduced platform size in the communication/industrial applications [41, 42, 43, 44, 45]. Although pursing a higher level N can benefit the reduction of magnetic components, the increased number of flying capacitors with high voltage rating and the floating switching domain bring in challenges towards the chip-level integration. In addition, the voltage balance of the flying capacitors in a multi-level DC-DC converter also needs special attention [46, 47, 48]. Most of the reported integrated circuit examples are based on 3-level [49, 31, 50, 51]. A 4-level integrated example was reported recently with added auxiliary switches to maintain low capacitor rating for all flying capacitors, such that the limited on-die capacitor resource can effectively utilized [52].

Resonant switched capacitor (ResSC) is another hybrid SC approach for eliminating the charging sharing loss [53, 32, 54]. By having an inductor to resonate with the working capacitor, the energy is transferred through the formed tank losslessly. At the same time, the voltage swing across the working capacitor is maximized such that the capacitor energy utilization gets improved. In addition, ResSC operation can conveniently enable lossless voltage regulation with the phase-shift or frequency modulation [55, 56]. Examples of a ladder based ResSC were demonstrated for the stacked voltage balancing [57, 58, 59]. However, with ladder stages larger than 2, more than one inductor are needed. The scenario is similar for other topologies like Dickson [60]. The series-parallel based ResSC can enable resonant operation for all flying capacitors with a single inductor [61]. A few Dickson based ResSC examples using a single inductor were also demonstrated with sophisticated phasing control [62, 63]. Depending on the placement of the resonant inductor and timing, different resonant mode can also be effected [64, 65]. Since the inductance required in the ResSC can be much smaller compared to a buck converter, this minimum inductor can be tightly integrated with a CMOS chip for on-die power delivery [66, 29, 67, 68]. However, most of chip-level ResSC implementation is limited to 2:1 conversion ratio. The work reported in [68] merges a re-configurable SC stage with a single resonant inductor achieves a wide operation range but suffers from lower efficiency and low power density.

In this thesis, stacked resonant switched capacitor (Stack-ResSC) has been proposed to further extend the resonant switched capacitor topology for wide conversion ratios. Depending on the passive and CMOS technologies, the Stack-ResSC can operate in two scenarios according to inductor waveforms. In one case, the inductor current is a sinusoidal waveform; in the other case, the current waveform behaves more like a trapezoid as in the dual active bridge converter. Given this analogy, the converter operated in this scenario is named as stacked dual active bridge (Stack-DAB) and treated as a derivative of Stack-ResSC. The switching pattern is the same for both cases. The control details are different due to different system dynamics. The harmonic averaging method [69] is used in both cases to capture the operating condition with good accuracy, and also facilitate the small signal analysis for the control loop design.

1.3 Thesis Organization

The remainder of the thesis is organized as follows: Chapter 2 introduces the proposed Stack-ResSC topology and its principle operation. The large and small signal models are developed with fundamental frequency approximation. A PCB prototype is presented to prove the topology concept and demonstrate the effectiveness of the controller. Chapter 3 presents the topology of stack-DAB as another derivation of Stack-ResSC. A silicon level realization using off-chip ceramic capacitor with PCB traces is presented in this chapter. The design optimization and harmonic averaging based modeling techniques are also presented. Chapter 4 concludes the thesis and discusses potential future works.

Chapter 2

Stacked Resonant Switched Capacitor DC-DC Converter Topology

As discussed in Chapter 1, the resonant switched capacitor (ResSC) converter is emerging out of various hybrid approaches as minimum inductance is needed. To extend the application of ResSC, this chapter introduces the stacked resonant switched capacitor (Stack-ResSC) DC-DC converter topology. Section 2.1 presents the general N-to-1 Stack-ResSC topology and the principle of operation. Harmonic averaging method is adopted to develop the large and small signal model in Section 2.2 and 2.3. To prove the topology concept and methodology of the controller design, a PCB prototype is built and discussed in Section 2.4. Section 2.5 presents the experimental results and highlights the effectiveness of the topology and its controller. In order to mitigate efficiency drop at extreme light load condition, a burst operation mode is introduced and experimentally verified in Section 2.6.

2.1 Topology overview and principle of operation

Fig. 2.1 shows the general single phase N-to-1 stacked resonant switched capacitor (Stacked-ResSC) topology. It consists of N-1 top stages, series stacked on top of one another, with the output voltage coming from the bottom stage. The capacitors C_{i1} to $C_{i(N-1)}$ and C_o are DC bypass capacitors that divide the input voltage into N stacked DC domains. A pair of complementary switches sits within each DC domain. The capacitors C_{r1} to $C_{r(N-1)}$ are resonant capacitors handling the major power flow. Since all resonant capacitors are in series with a single inductor L_r, there is no charge sharing losses during the power transfer. Thanks to the stacking structure, all switches are only rated for their local domain voltage, which is nominally 1/N of the input voltage. Futher, the upper N-1 resonant stages share the resonant current, and thus each stage is only rated for its fraction of the resonant current. As such, the topology can be also thought of as a series-parallel arrangement. The gate drivers are decoupled from high resonant voltage swing across the AC capacitors. The number of stacking stages N can be adjusted accordingly, which enables the use of advanced CMOS

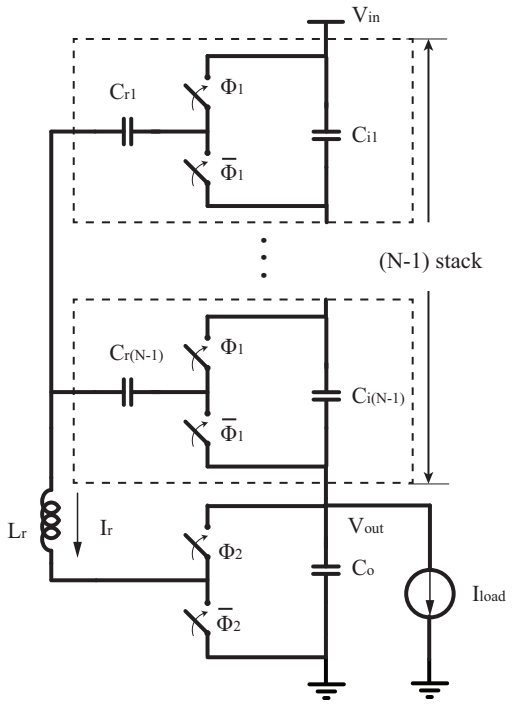


Figure 2.1: A single phase N-to-1 Stacked Resonant Switched Capacitor (ResSC)

process in the design of high voltage, high conversion ratio applications.

A single phase 4-to-1 stacked-ResSC is shown in Fig. 2.2 (a) as an example. The stacked stages divide the input rail into four DC voltage domains sustained by the local bypass capacitors C_{i1}, C_{i2}, C_{i3} and C_o. In steady state, the top three DC domains are balanced to be $\frac{1}{3}(V_{in} - V_{out})$. Three resonant capacitor C_{r1}, C_{r2} and C_{r3} work in parallel in the AC sense and resonate together with a single inductor L_r. The resonant frequency of the converter is determined by $\frac{1}{\sqrt{3C_rL_r}}$.

A phase shift operation is adopted for the topology to enable efficient voltage regulation. As illustrated in Fig. 2.2 (b), the top three switch pairs are driven by the same complementary gating signals $\Phi_1/\overline{\Phi}_1$. The bottom switch pair is driven by $\Phi_2/\overline{\Phi}_2$ and phase shifted by a angle of θ with respect to the top switch pairs. In this way, the operation of the converter can be divided into four switch states as shown in Fig. 2.3. In states B and D, the inductor current flows to the output. In states A and C, the inductor current commutes to favor the power delivery in the coming state. With a high quality tank and switching above resonance, the representative voltage and current waveforms are illustrated in Fig. 2.2 (b). Assuming identical capacitance, C_{r1}, C_{r2} and C_{r3} bear the same AC swings but block different DC voltages. The DC stress across each resonant capacitor is determined by the input voltage and output voltage. The current flowing through each top stacked stage equals one third of the inductor current I_r. Under the nominal 4-to-1 conversion ($V_{out} = \frac{1}{4}V_{in}$), the zero crossings of the inductor current are aligned in the middle of the phase angle θ. This feature

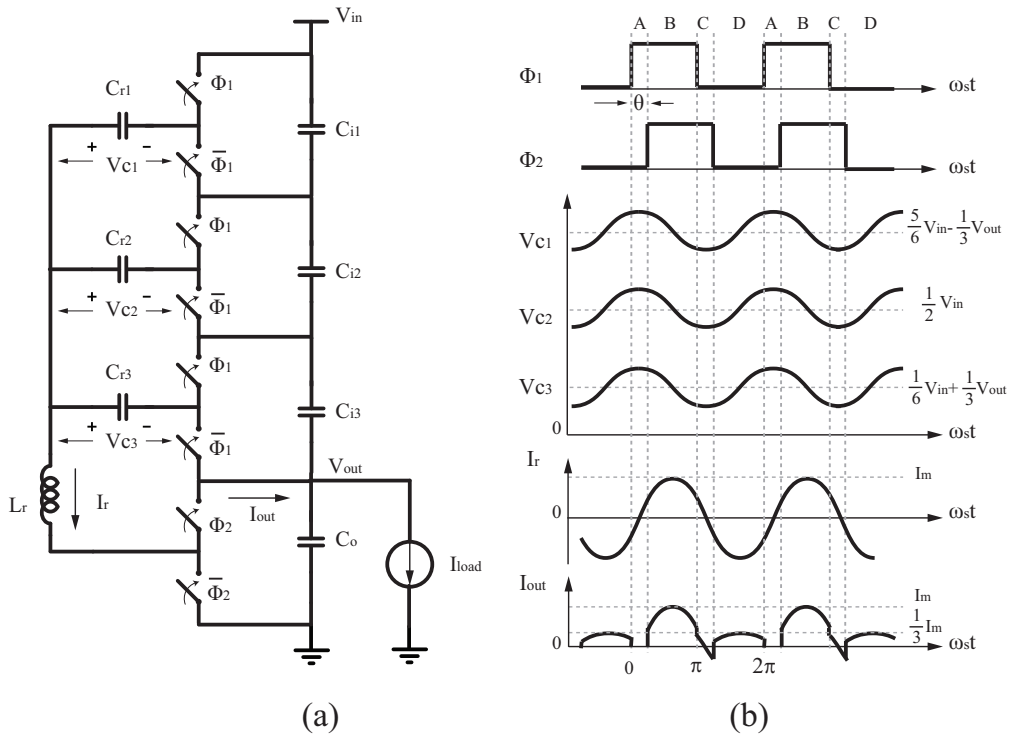


Figure 2.2: A single phase 4-to-1 Stacked ResSC (a) and representative current and voltage waveforms (b)

can potentially enable zero voltage switching (ZVS) for all switches given proper deadtime. The output current I_{out} is a function of the tank current I_r determined by the switching actions. Though the output current in a single phase will lead to large output voltage ripples without significant bypass capacitance, the scenario can be alleviated by having a multi-phase implementation. Multi-phase interleaving can also help reduce the voltage ripple on intermediate DC nodes. In addition, the synchronous top stages form a ladder type switched capacitor structure such that the intermediate nodes are always self balanced with the embedded switched capacitor operation.

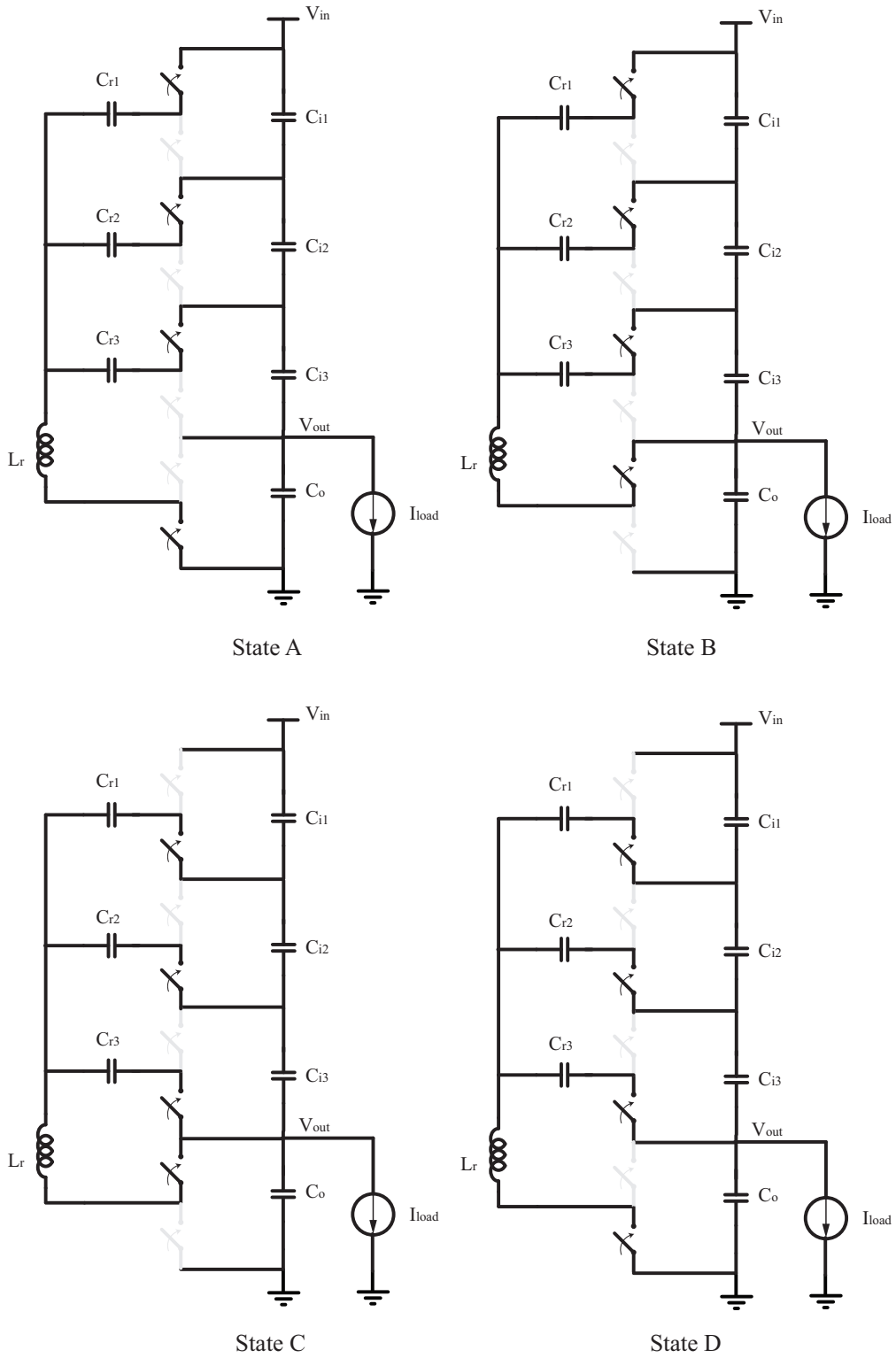


Figure 2.3: Different switching states of a single phase 4-to-1 Stacked ResSC

2.2 Large Signal Model

To provide a more intuitive way for understanding the operation of the converter, a phasor model is introduced to capture the steady state operation of the converter. Either by having enough bypass capacitance in a single phase or having a balanced number of interleaving phases, it can be assumed that a DC source with low impedance exist between intermediate nodes. With the perspective of folding the top three stages into a single stage, the 4-to-1 topology can be degenerated into a simple 2-to-1 topology as shown in Fig. 2.4 (a). The voltage across the top stage becomes $\frac{1}{3}(V_{in} - V_{out})$. Three identical resonant capacitors lump together to be $3C_r$ since they carry the same AC swing although they sustain the different DC voltages.

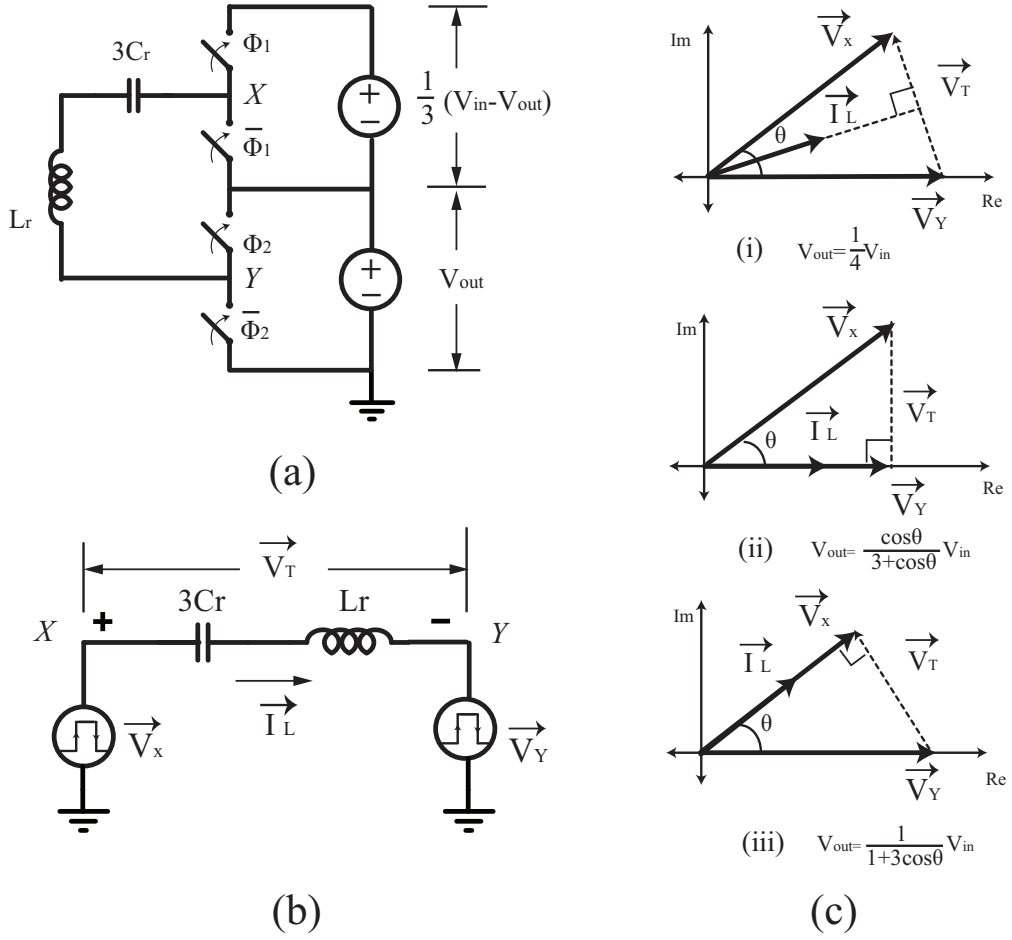


Figure 2.4: Degenerated 4-to-1 Stacked ResSC (a), simplified AC circuit (b) and phasor models under different input and output voltages (c)

Furthermore, the degenerated 2-to-1 ResSC circuit can be simplified into an AC circuit as shown in Fig. 2.4 (b). With a high Q tank, a phasor model can be used to represent

the fundamental frequency components of the driving signals at node X and Y, and all circuit variables: $\overrightarrow{V_X}$, $\overrightarrow{V_Y}$, $\overrightarrow{I_L}$ and $\overrightarrow{V_T}$. Under the phase-shift switching pattern, $\overrightarrow{V_X}$ leads $\overrightarrow{V_Y}$ by a angle θ. When $V_{in} = \frac{1}{4}V_{out}$, $\overrightarrow{V_X}$ has the same magnitude as $\overrightarrow{V_Y}$. With operation above resonance, the tank current phasor $\overrightarrow{I_L}$ should lag the tank voltage phasor $\overrightarrow{V_T}$ by 90 degrees. According to the geometry constraint of an isosceles triangle formed by the phasors, $\overrightarrow{I_L}$ should bisect the angle θ as shown in Fig. 2.4 (c)-(i). The phasor model also correlates the zero crossing of the tank current with the phase-shifted gating signals, as illustrated in Fig. 2.2 (b). In order to benefit from zero volatage switching (ZVS), the current phasor should be constrained within the phase angle set by $\overrightarrow{V_X}$ and $\overrightarrow{V_Y}$ [56].The cases for the minimum and maximum output voltage in a lossless model is shown in Fig. 2.4 (c)-(ii) and (iii). Based on the geometrical property of right triangle, the output range with potential ZVS for a 4-to-1 ResSC is obtained as:

$$\frac{V_{in}cos\theta}{3+cos\theta} < V_{out} < \frac{V_{in}}{1+3cos\theta} \tag{2.1}$$

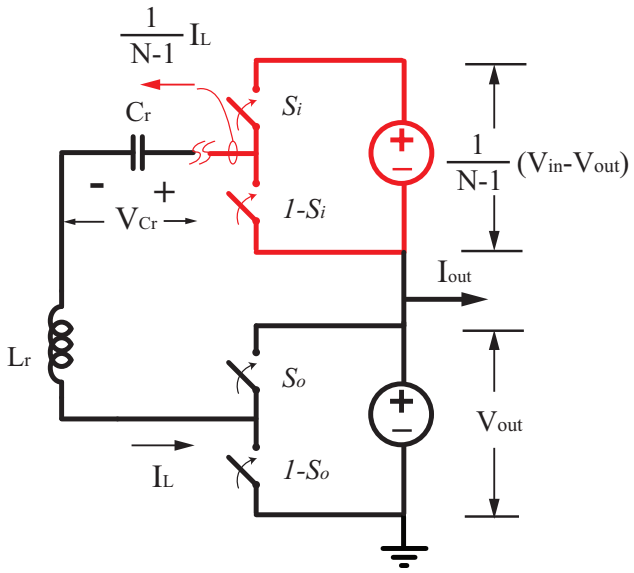


Figure 2.5: Degenerated N-to-1 Stacked ResSC

To obtain an analytic expression for the steady state operation, the generalized averaging method [69] is applied to the state space equation of the converter. The derivation below is based on the general N-to-1 Stack-ResSC topology. Similarly, a N-to-1 stack-ResSC can be degenrated into a simple 2-to-1 circuit as shown in Fig. 2.5. In the figure, all resonant capacitors are lumped together as one capacitor C_r and in series with L_r. The current I_r is continuous through C_r and L_r, however, the current flowing in the top stage is 1/(N-1) of the inductor current due to the degeneration concept. The symbols s_i, s_o represent the switching function of the top and bottom stages, which take the form:

$$\begin{aligned} s_i &= \frac{1}{2}\{sign[sin(\omega t)] + 1\} \\ s_o &= \frac{1}{2}\{sign[sin(\omega t - \theta)] + 1\} \end{aligned} \tag{2.2}$$

Given that, the state space equations that consider L_r, C_r and C_o read:

$$\begin{aligned} \frac{di_{L_r}}{dt} &= \frac{1}{L_r}[s_i(v_{out} + \frac{V_{in} - v_{out}}{N-1}) + (1 - s_i)v_{out} - s_o v_{out} - i_{L_r}R_r - v_{C_r}] \\ \frac{dv_{C_r}}{dt} &= \frac{1}{C_r} i_{L_r} \\ \frac{dv_{out}}{dt} &= \frac{1}{C_o}[s_o s_i i_{L_r} - (1 - s_i)(1 - s_o)\frac{i_{L_r}}{N-1} + \frac{N-2}{N-1} i_{Lr} s_o (1 - s_i) - I_{load}] \end{aligned} \tag{2.3}$$

In this example, the resonant states are modeled with their fundamental frequency component, while the output is modeled with its conventional DC average component. The generalized averaging method [69] provides a framework for developing a dynamic model for key DC and harmonic components of circuit state variables. Applying the averaging method to Eq. 2.3, one obtains:

$$\begin{aligned} \langle\frac{di_{L_r}}{dt}\rangle_1 &= \frac{1}{L_r}[\frac{1}{N-1}(\langle s_i\rangle_1 V_{in} - \langle s_i v_{out}\rangle_1) - \langle v_{out} s_o\rangle_1 - \langle i_{Lr}\rangle_1 R_L - \langle v_{C_r}\rangle_1] \\ \langle\frac{dv_{C_r}}{dt}\rangle_1 &= \frac{1}{C_r}\langle i_{L_r}\rangle_1 \\ \langle\frac{dv_{out}}{dt}\rangle_0 &= \frac{1}{C_o}[\frac{1}{N-1}\langle s_i i_{L_r}\rangle_0 + \langle s_o i_{L_r}\rangle_0 - I_{load}] \end{aligned} \tag{2.4}$$

According to the generalized averaging method [69], The operator $\langle\bullet\rangle_k$ represents the kth order complex Fourier coefficient. The time derivative of the kth coefficient and transformation of variable product are computed to be:

$$\begin{aligned} \frac{d}{dt}\langle x\rangle_k &= \langle\frac{d}{dt}x\rangle_k - jk\omega\langle x\rangle_k \\ \langle xy\rangle_k &= \sum_i \langle x\rangle_{k-i}\langle y\rangle_i \end{aligned} \tag{2.5}$$

where x and y are variables and ω is the switching frequency. Eq. 2.4 can be further transformed as:

$$\begin{aligned}
\frac{d\langle i_{L_r}\rangle_1}{dt} &= -j\omega\langle i_{L_r}\rangle_1 + \frac{1}{L_r}[\frac{1}{N-1}(\langle s_i\rangle_1 V_{in} - \langle s_i\rangle_1\langle v_{out}\rangle_o) - \langle v_{out}\rangle_0\langle s_o\rangle_1 - \langle i_{L_r}\rangle_1 R_r - \langle v_{C_r}\rangle_1] \\
\frac{d\langle v_{C_r}\rangle_1}{dt} &= \frac{1}{C_r}\langle i_{L_r}\rangle_1 - j\omega\langle v_{C_r}\rangle_1 \\
\frac{d\langle v_{out}\rangle_0}{dt} &= \frac{1}{C_o}[\frac{1}{N-1}(\langle s_i\rangle_{-1}\langle i_{L_r}\rangle_1 + \langle s_i\rangle_1\langle i_{L_r}\rangle_1) + \langle s_o\rangle_{-1}\langle i_{L_r}\rangle_1 + \langle s_o\rangle_1\langle i_{L_r}\rangle_{-1} - I_{load}]
\end{aligned} \tag{2.6}$$

The variable $\langle v_{out}\rangle_0$ represents the output voltage which is real. The complex coefficients $\langle i_{Lr}\rangle_1$ and $\langle v_{Cr}\rangle_1$ are related to the magnitude and phase of the fundamental frequency components in i_{Lr} and v_{Cr}. The complex coefficients can be decomposed into the real and imaginary parts as:

$$\begin{aligned}
\langle i_{L_r}\rangle_1 &= \frac{1}{2}X_{i_{L_r}} + j\frac{1}{2}Y_{i_{L_r}} \\
\langle v_{C_r}\rangle_1 &= \frac{1}{2}X_{v_{C_r}} + j\frac{1}{2}Y_{v_{C_r}} \\
\langle s_i\rangle_1 &= -j\frac{1}{\pi} \\
\langle s_o\rangle_1 &= -j\frac{1}{\pi}e^{-j\theta} \\
\langle v_{out}\rangle_0 &= V_o
\end{aligned} \tag{2.7}$$

where $X_{i_{L_r}}$, $Y_{i_{L_r}}$ and $X_{v_{C_r}}$, $Y_{v_{C_r}}$ represent the real and imaginary parts of the fundamental phasor of the inductor current and capacitor voltage:

$$\begin{aligned}
\overrightarrow{I}_{L_r} &= X_{i_{L_r}} + jY_{i_{L_r}} \\
\overrightarrow{V}_{C_r} &= X_{v_{C_r}} + jY_{v_{C_r}} \\
\parallel \langle i_{L_r}\rangle_1 \parallel &= \frac{1}{2} \parallel \overrightarrow{I}_{L_r} \parallel \\
\parallel \langle v_{C_r}\rangle_1 \parallel &= \frac{1}{2} \parallel \overrightarrow{V}_{C_r} \parallel
\end{aligned} \tag{2.8}$$

With Eq. 2.6 and Eq. 2.7, the real-valued fifth order state space equations are obtained:

$$\begin{aligned}
\frac{dX_{i_L}}{dt} &= -\frac{R_r}{L_r}X_{i_L} + \omega Y_{i_L} - \frac{1}{L_r}X_{v_C} + \frac{1}{L_r}\frac{2}{\pi}sin\theta V_{out} \\
\frac{dY_{i_L}}{dt} &= -\omega X_{i_L} - \frac{R_r}{L_r}Y_{i_L} - \frac{1}{L_r}Y_{v_C} + \frac{1}{L_r}\frac{2}{\pi}(\frac{1}{N-1} + cos\theta)V_{out} - \frac{1}{L_r}\frac{1}{N-1}\frac{2}{\pi}V_{in} \\
\frac{dX_{v_C}}{dt} &= \frac{1}{Cr}X_{i_L} + \omega Y_{v_C} \\
\frac{dY_{v_C}}{dt} &= -\omega X_{v_C} + \frac{1}{Cr}Y_{i_L} \\
\frac{dV_o}{dt} &= \frac{1}{C_o}[-\frac{1}{\pi}sin\theta X_{i_{L_r}} - \frac{1}{\pi}(\frac{1}{N-1} + cos\theta)Y_{i_{L_r}} - I_{load}]
\end{aligned} \tag{2.9}$$

Under steady state:

$$\begin{aligned}
\frac{dX_{i_L}}{dt} &= 0 \\
\frac{dY_{i_L}}{dt} &= 0 \\
\frac{dX_{v_C}}{dt} &= 0 \\
\frac{dY_{v_C}}{dt} &= 0 \\
\frac{dV_o}{dt} &= 0
\end{aligned} \tag{2.10}$$

which leads to:

$$\begin{aligned}
I_{load} = -\frac{K}{\pi}\{A\frac{V_{in}}{N-1}sin\theta + BV_{out}[1 + \frac{1}{(N-1)^2} + \frac{2cos\theta}{N-1}] \\
- BV_{in}[\frac{1}{(N-1)^2} + \frac{cos\theta}{N-1}]\}
\end{aligned} \tag{2.11}$$

with

$$K = \frac{\frac{2}{\pi}\omega C_r}{A^2 + B^2} \quad A = 1 - \frac{\omega^2}{{\omega_o}^2} \quad B = \frac{\omega}{\omega_o Q} \quad \omega_o = \frac{1}{\sqrt{C_r L_r}} \quad Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_r} \tag{2.12}$$

From Eq. 2.11- 2.12, it can be seen that with properly selected L_r, C_r and R_r, the switching frequency ω can be uniquely determined given V_{in}, V_{out}, I_{load} and θ. Therefore, the switching frequency is selected as the tuning knob for regulating the output voltage under varying load and set-point commands. The phase angle is pre-selected for the expected output range and not tuned dynamically in the controller design. Alternatively, if the switching frequency is fixed, the phase angle can also be chosen as the control parameter.

2.3 Small Signal Model and Control Strategies

To obtain the small signal model to facilitate a analog controller design, the small signal perturbation is applied to Eq. 2.9 with the state variables taken as:

$$\begin{aligned} x_{i_L} &= X_{i_L} + \hat{x}_{i_L} \\ y_{i_L} &= Y_{i_L} + \hat{y}_{i_L} \\ x_{v_C} &= X_{v_C} + \hat{x}_{v_C} \\ y_{v_C} &= Y_{v_C} + \hat{y}_{v_C} \\ v_o &= V_o + \hat{v}_o \end{aligned} \tag{2.13}$$

The input variables are taken as:

$$\begin{aligned} \omega &= \Omega + \hat{\omega} \\ i_{load} &= I_{load} + \hat{i}_{load} \end{aligned} \tag{2.14}$$

and output variables are taken as:

$$\begin{aligned} v_o &= V_o + \hat{v}_o \\ \parallel i_L \parallel &= \parallel I_L \parallel + \parallel \hat{i}_L \parallel \\ \phi_{i_L} &= \Phi_{i_L} + \hat{\phi}_{i_L} \end{aligned} \tag{2.15}$$

With

$$\begin{aligned} \parallel \hat{i_L} \parallel &= \sqrt{(X_{i_L} + \hat{x}_{i_L})^2 + (Y_{i_L} + \hat{y}_{i_L})^2} - \sqrt{X_{i_L}^2 + Y_{i_L}^2} \\ \hat{\phi}_{i_L} \approx tan\hat{\phi}_{i_L} &= tan(\phi_{i_L + \hat{i}_L} - \phi_{i_L}) = \frac{tan\phi_{i_L + \hat{i}_L} - tan\phi_{i_L}}{1 + tan\phi_{i_L + \hat{i}_L} tan\phi_{i_L}} \end{aligned} \tag{2.16}$$

one obtains:

$$\begin{aligned} \parallel \hat{i_L} \parallel &= \frac{X_{i_L}\hat{x}_{i_L} + Y_{i_L}\hat{y}_{i_L}}{\parallel i_L \parallel} \\ \hat{\phi}_{i_L} &= \frac{-Y_{i_L}\hat{x}_{i_L} + X_{i_L}\hat{y}_{i_L}}{\parallel i_L \parallel^2} \end{aligned} \tag{2.17}$$

The real-valued fifth-order small signal state space matrix is obtained as Eq. 2.18.

$$
\begin{bmatrix} \frac{d\hat{x}_{i_L}}{dt} \\ \frac{d\hat{y}_{i_L}}{dt} \\ \frac{d\hat{x}_{v_C}}{dt} \\ \frac{d\hat{y}_{v_C}}{dt} \\ \frac{d\hat{v}_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_r}{L_r} & \Omega & -\frac{1}{L_r} & 0 & \frac{1}{L_r}\frac{2}{\pi}\sin\theta \\ -\Omega & -\frac{R_r}{L_r} & 0 & -\frac{1}{L_r} & \frac{1}{L_r}\frac{2}{\pi}(\frac{1}{N-1}+\cos\theta) \\ \frac{1}{C_r} & 0 & 0 & \Omega & 0 \\ 0 & \frac{1}{C_r} & -\Omega & 0 & 0 \\ -\frac{1}{C_o}\frac{1}{\pi}\sin\theta & -\frac{1}{C_o}\frac{1}{\pi}(\frac{1}{N-1}+\cos\theta) & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} Y_{i_L} & 0 \\ -X_{i_L} & 0 \\ Y_{v_C} & 0 \\ -X_{v_C} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \begin{bmatrix} \hat{\omega} \\ \hat{i}_{load} \end{bmatrix}
$$

$$
\begin{bmatrix} \hat{v}_o \\ \| \hat{i}_L \| \\ \hat{\phi}_{i_L} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ \frac{X_{i_L}}{\|i_L\|} & \frac{Y_{i_L}}{\|i_L\|} & 0 & 0 & 0 \\ -\frac{Y_{i_L}}{\|i_L\|^2} & \frac{X_{i_L}}{\|i_L\|^2} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} \tag{2.18}
$$

For a convenient presentation, Eq. 2.18 can be rewritten as:

$$
\begin{bmatrix} \frac{d\hat{x}_{i_L}}{dt} \\ \frac{d\hat{y}_{i_L}}{dt} \\ \frac{d\hat{x}_{v_C}}{dt} \\ \frac{d\hat{y}_{v_C}}{dt} \\ \frac{d\hat{v}_o}{dt} \end{bmatrix} = \mathbf{A} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} \mathbf{B}_\omega & \mathbf{B}_{i_{load}} \end{bmatrix} \begin{bmatrix} \hat{\omega} \\ \hat{i}_{load} \end{bmatrix}
$$

$$
\begin{bmatrix} \hat{v}_o \\ \| \hat{i}_L \| \\ \hat{\phi}_{i_L} \end{bmatrix} = \begin{bmatrix} \mathbf{C}_{v_o} \\ \mathbf{C}_{\|i_L\|} \\ \mathbf{C}_\phi \end{bmatrix} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{x}_{v_C} \\ \hat{y}_{v_C} \\ \hat{v}_o \end{bmatrix} \tag{2.19}
$$

Based on Eq. 2.19, the small signal transfer functions from the switching frequency to the output voltage magnitude ($\| H \|_{\omega \to v_o}$) and switching frequency to the resonant current properties ($\| H \|_{\omega \to \|i_L\|}$ and $\| H \|_{\omega \to \phi}$) are evaluated based on:

$$
\begin{aligned} \| H \|_{\omega \to v_o} &= \mathbf{C}_{v_o}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_\omega \\ \| H \|_{\omega \to \|i_L\|} &= \mathbf{C}_{\|i_L\|}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_\omega \\ \| H \|_{\omega \to \phi} &= \mathbf{C}_\phi(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_\omega \end{aligned} \tag{2.20}
$$

Given a set of design parameters as $L_r = 4.7\mu H$, $C_r = 100nF$, $C_o = 40\mu F$, $\theta = \pi/4$ and $R_r = 500m\Omega$, the small signal transfer functions are plotted in Fig 2.6. From the Bode plot

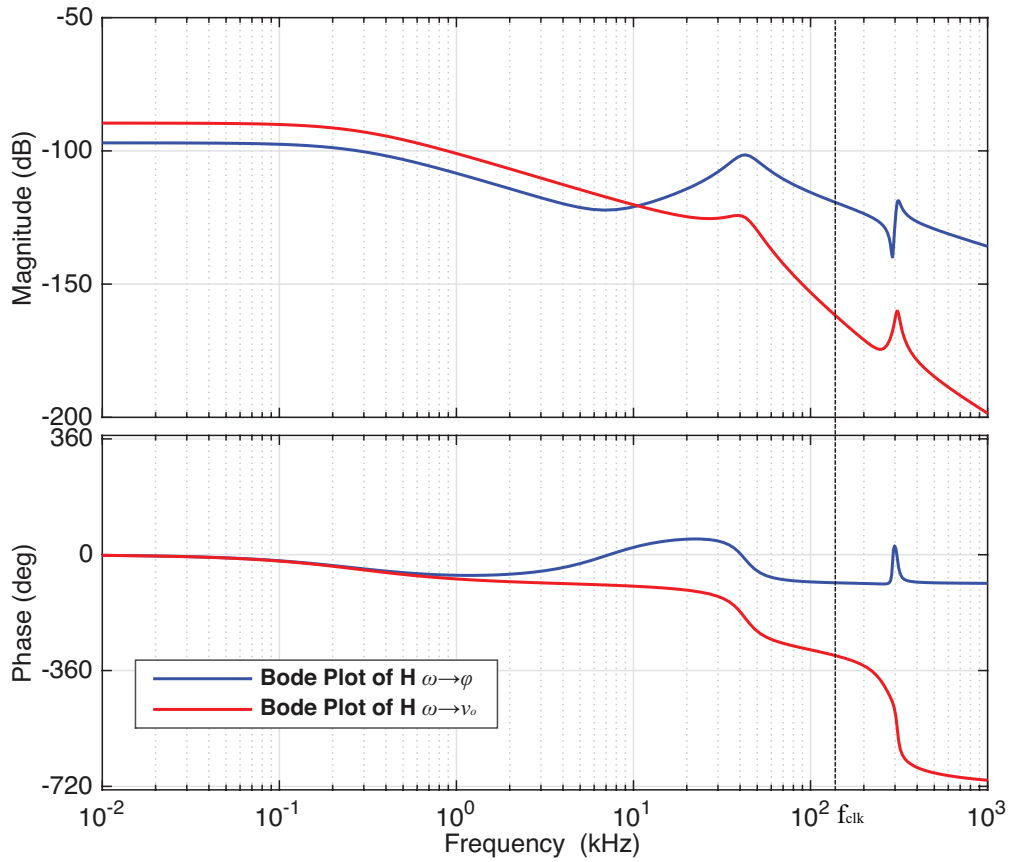


Figure 2.6: Small signal transfer function of $H_{\omega\to\phi}$ (blue) and $H_{\omega\to v_o}$ (red) with $N = 3$, $L_r = 4.7\mu H$, $C_r = 100nF$, $C_o = 40\mu F$, $\theta = \pi/4$ and $R_r = 500m\Omega$ under the operating points of $V_{in} = 24$, $V_{out} = 6$ and $\omega = 2\pi \times 175kHz$

of $H_{\omega\to v_o}$, it can be seen that there is a dominant pole introduced by the output capacitor followed by a pair of complex conjugate poles, contributing an additional 180° phase lag and a resonant peak in the magnitude response. This makes it challenging to realize compensation with a pure voltage loop at a high crossover frequency. However, by inspecting $H_{\omega\to\phi}$, one sees a significant amount of phase lead present at high frequency, due to the resonant zeros appearing ahead of the resonant poles.

Therefore, this work takes advantage of the phase lead from the dynamics of current phase to stabilize the system by adding a phase loop. Fig. 2.7 shows the small signal block diagram of the control system. Both voltage loop and phase loop are realized with simple proportional gains. The degree of compensation can be adjusted by properly choosing respective gains of the two loops. Fig. 2.8 illustrates the effect of compensation from the transfer function of frequency control input v_c to the output voltage v_o with and without the phase loop. By adding the phase loop, a 20kHz crossover frequency with a 35 degrees phase margin can be achieved with the same design parameters noted in Fig. 2.6. A tight load line regulation can

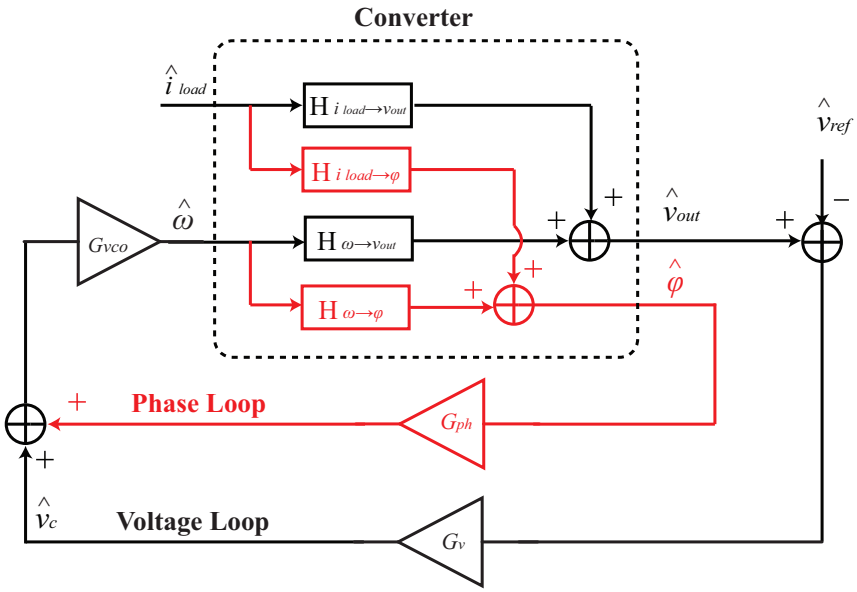


Figure 2.7: Small signal blocks of close loop control system

be maintained with a sufficient DC gain, as illustrated in the next subsection.

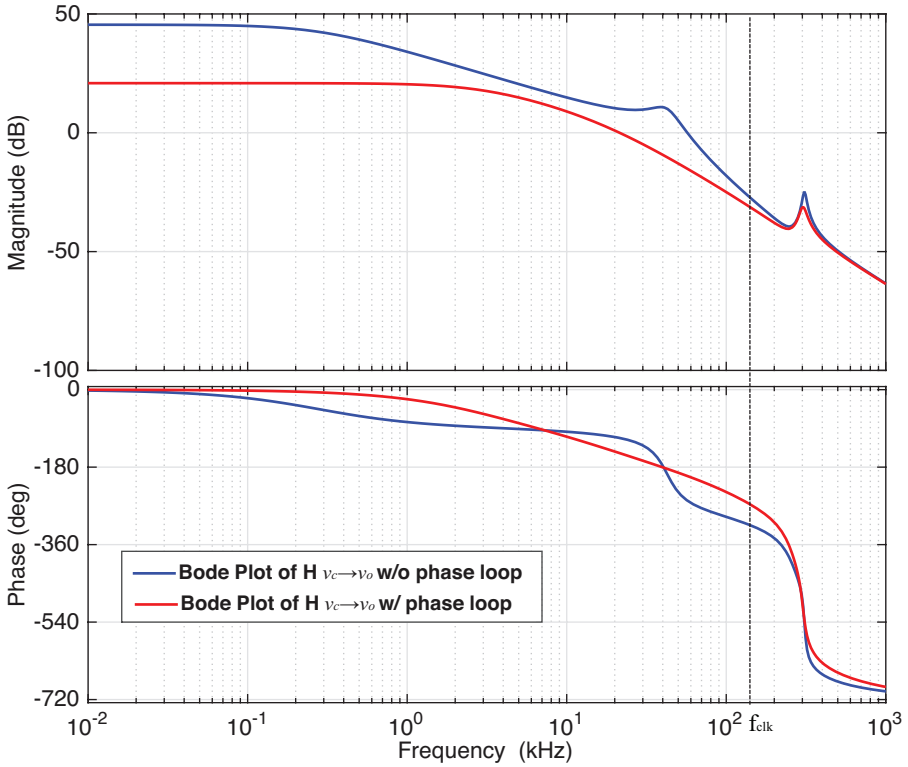


Figure 2.8: Small signal transfer function of $H_{v_c \to v_o}$ with the phase loop closed and a gain of 0.2 ($G_{ph} = 0.2$) (red) and without phase loop ($G_{ph} = 0$) (blue) and $G_{vco} = 0.9MHz/V$

2.4 A PCB prototype of 6W 4-to-1 Stack-ResSC

Table 2.1: The selection of components

Component	Part Number	Parameters
Tank Inductor (L_r)	VER2923-472	4.7μH
Tank Capacitors (C_{r1-r6})	HMK316B7104KL-T	100V, 100nF
Bypass Capacitors (C_{i1-i3})	CC1210KKX7R9BB105	50V, 4×1μF
Output Capacitor (C_o)	CC1210KKX7R9BB106	50V, 4×10μF
Power Switches (SW_{1-16})	STS10P3LLH6(H-Brigde)	30V, 25$m\Omega$, 6A (NMOS)
		-30V, 50$m\Omega$, -4.2A (PMOS)
Analog Switches (SW_{17-24})	MC14016BDR2G(Quad)	18V, 310Ω, ±25mA
Gate Driver	UCC27424	
Op-amp (Op_{1-3})	LMV721	
VCO	SN74LS628D	

To verify the concept of the topology and the effectiveness of the modeling techniques, a PCB prototype of a two-phase interleaved 4-to-1 ResSC was built for a 6W nominal output power. The main power train schematic is shown in Fig. 2.9. The PCB circuit

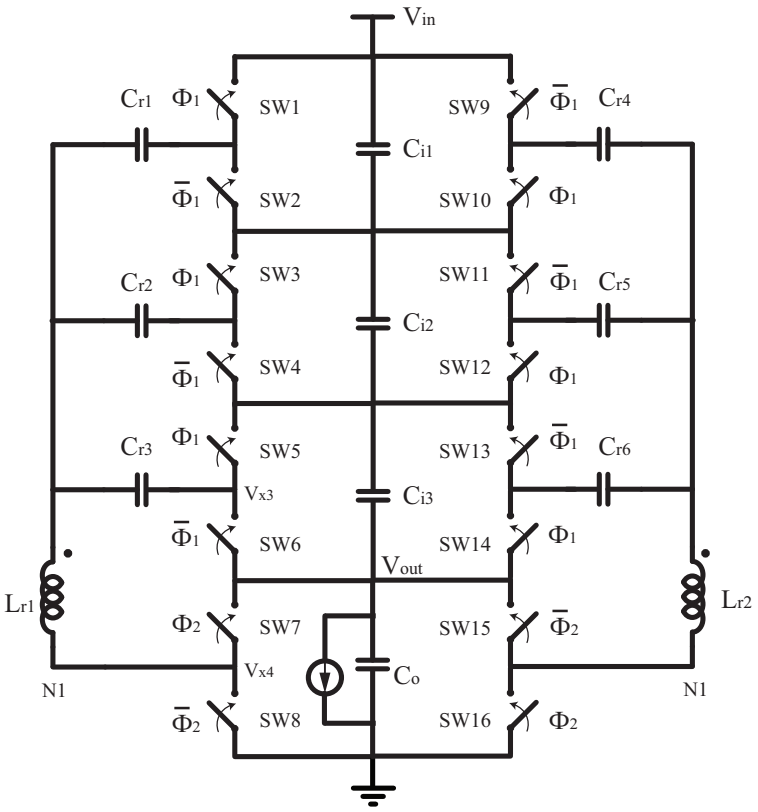


Figure 2.9: A 2 phase interleaved 4-to-1 Stack-ResSC converter

board is illustrated in Fig. 2.10 with components listed in Table 2.1. Fig. 2.11 (a) shows the implementation of controller. The resonant currents are sensed by using a voltage sense transformer formed with the resonant inductor as the primary side. The turn ratio of the transformer is 4:3. A passive integrator formed by R_{int} and C_{int} follows the voltage sensing transformer to generate a replica of the resonant current. The scaling factor of sensing current is determined by:

$$\frac{V_{sens}}{I_L} \approx \frac{N_2}{N_1}\frac{L_r}{R_{int}C_{int}} \tag{2.21}$$

The phase error is extracted by using a passive mixer which compares the replicated current waveform V_x with a reference clock Φ_3. The clock Φ_3 is generated as the middle reference of Φ_1 and Φ_2 shifted backward by $\pi/2$. The representative waveforms are illustrated in Fig. 2.11 (b). In this way the phase error can be approximated as the DC average of the mixer output V_{ph} with a high sensitivity.

$$V_{ph} \approx \| V_{sens} \| \frac{2}{\pi}\widehat{\psi} \tag{2.22}$$

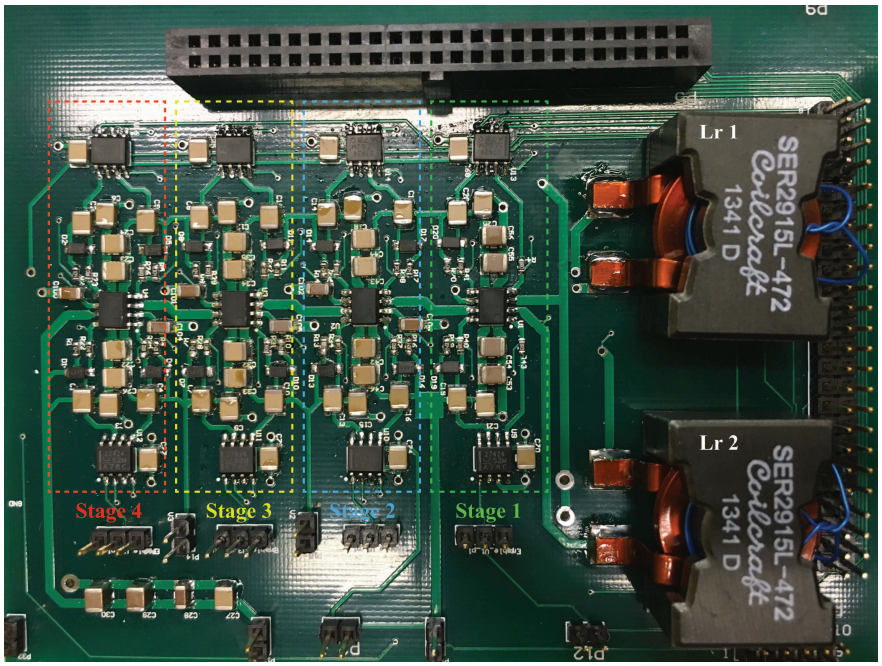


Figure 2.10: The prototype of a two-phase interleaved 4-to-1 Stack-ResSC converter

A gain stage follows the phase error detector and combines the error signals from two phase legs. The amplified phase error signal combines with the voltage error to control the frequency of the voltage controlled oscillator. The ratio of R_2/R_1 sets the phase loop gain. The ratio of $R_5/(R_3 \parallel R_4)$ sets the voltage loop gain. The overall loop gain can be adjusted by tuning the ratio of R_7/R_6. An FPGA is used to generate all gating signals for the power train switches and switches in the phase error detector from the oscillator output. A phase shift of 45^o between the top and bot switch driving signals is chosen to cover a wide output voltage range. The deadtime of 100 ns is selected to enable ZVS around nominal operation.

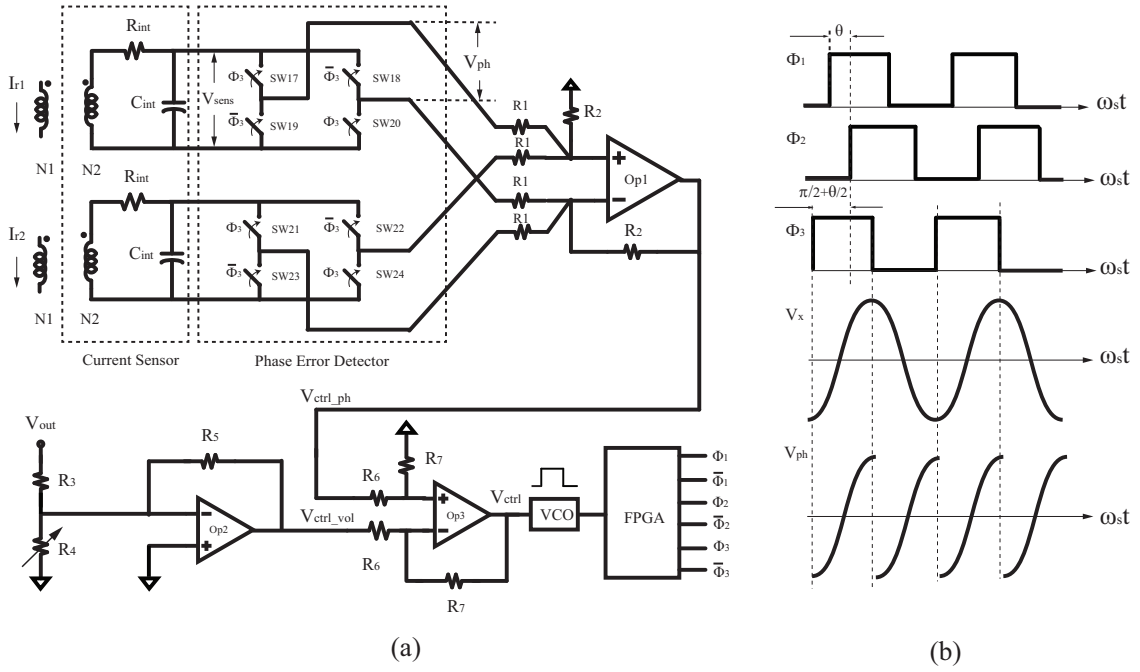


Figure 2.11: The control circuit of the 4-to-1 Stack-ResSC converter (a), and key waveforms of the phase loop with $N1 : N2 = 4 : 3$, $R_{int} = 4.7k\Omega$, $C_{int} = 10nF$, $R_1 = 13k\Omega$, $R_2 = 100k\Omega$, $R_3 = 82k\Omega$, $R_4 = 0 - 200k\Omega$, $R5 = 470k\Omega$, $R_6 = 100k\Omega$ and $R_7 = 100k\Omega$

2.5 Experimental Results

Fig. 2.12 shows the experimental waveforms of switching voltages at node V_{x4} and V_{x3} in the power train as well as the sensed current signal V_{sens} under the nominal 24V input to 6V output voltage conversion. It can be seen that the zero crossing of the current is roughly aligned in the middle of the interval set by the top and bottom switching actions as predicted also by Fig. 2.2.

The measured efficiency over a range of operating points is shown in Fig. 2.13 and Fig. 2.14. Fig. 2.13 plots the efficiency and operating frequency over a 4V-8V output range. As it can be seen, the converter can maintain efficiency above 88% with a peak efficiency of 91.7% when $V_{out} = 6.2V$. This highlights the major benefit of the ResSC topology versus SC converter topology. In a standard SC converter, efficiency has to be significantly compromised to achieve voltage regulation over a wide range. It is also challenging to achieve voltage higher than the nominal conversion ratio with a fixed topology. However, in this work, a high efficiency can be maintained across a wide range of output voltages. Fig. 2.13 also shows the effectiveness of using frequency to modulate the output voltage. A 5% frequency change can achieve a range of 67% output voltage modulation given a fixed load condition. Fig. 2.14 shows the efficiency and operating frequency over a 0.3A-1.8A load range with fixed input voltage and output voltage. As the load decreases, the operating frequency has to increase

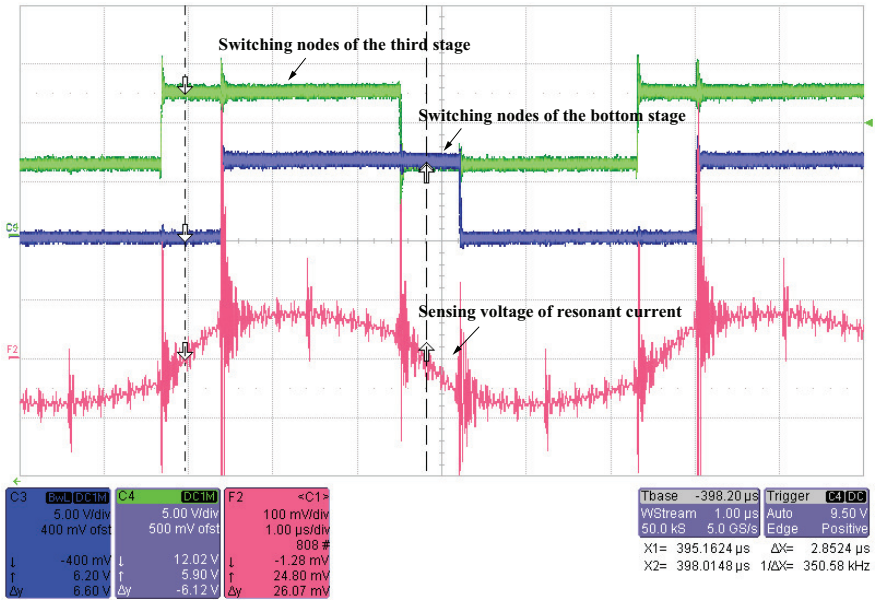


Figure 2.12: The steady state waveforms of voltages at the switching node V_{x4} (purple) and V_{x3} (green) and the sensing voltage of the resonant current V_{sens} (pink) with $V_{in} = 24V$, $V_{out} = 6V$, $I_{load} = 1.0A$ and switching frequency of 173kHz

to maintain the output voltage regulation. Thus at the light load condition, the gate drive loss dominates the total loss. At the extreme light load, the efficiency is compromised. In Section 2.6, burst mode operation is introduced to improve the efficiency at extreme light load condition.

Fig. 2.15 shows the transient performance of the output voltage under a load step of 1A. In order to minimize the overall voltage overshoot or undershoot, load line regulation is adopted in the control loop design. With the compensation scheme discussed in Section 2.3, and 40μF output capacitance, the small signal control bandwidth is designed to be 20kHz. In the experiment, an overall 295mV overshoot and undershoot are achieved with 40μs response time. Fig. 2.15 also highlights the voltage control output V_{ctrl_vol} and phase error signal V_{ph} during the transient. It can be noticed that it is the voltage control signal that determines the operating frequency. The phase control signal helps in stabilizing the system during transients and has minor impact in determining operating frequency in the steady state.

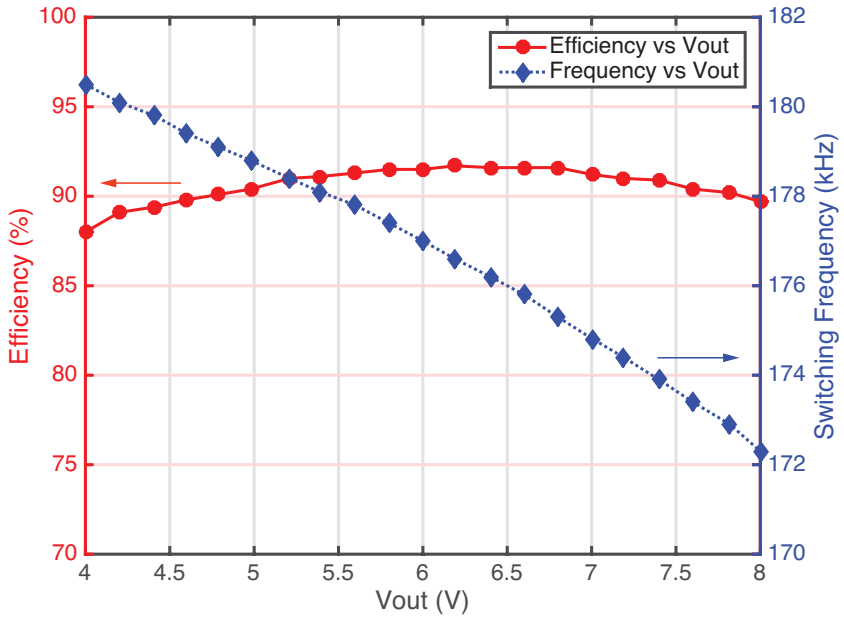


Figure 2.13: Operating frequency and corresponding efficiency (gating loss included) vs the output voltage at $I_{load} = 1A$ and $V_{in} = 24V$

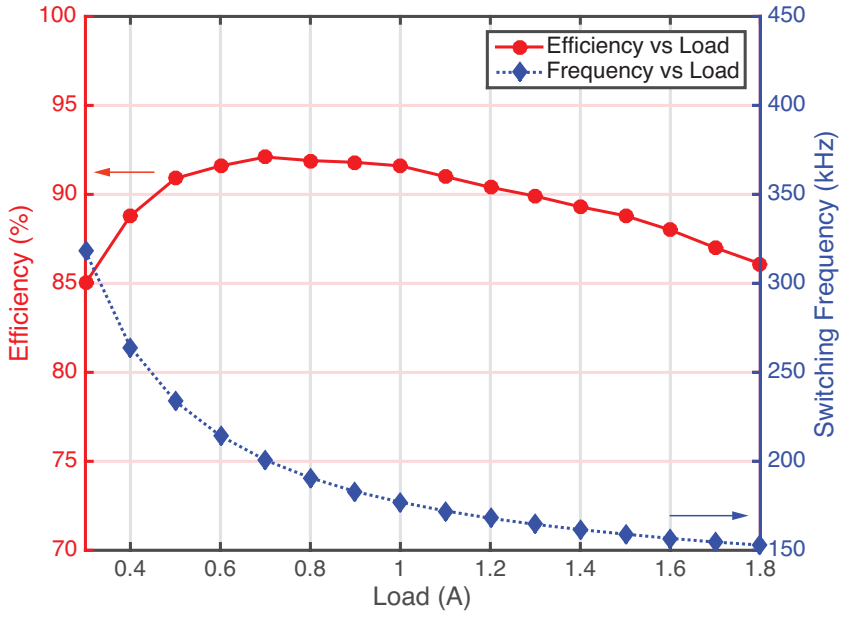


Figure 2.14: Operating frequency and corresponding efficiency (gating loss included) vs the load current at $V_{out} = 6V$ and $V_{in} = 24V$

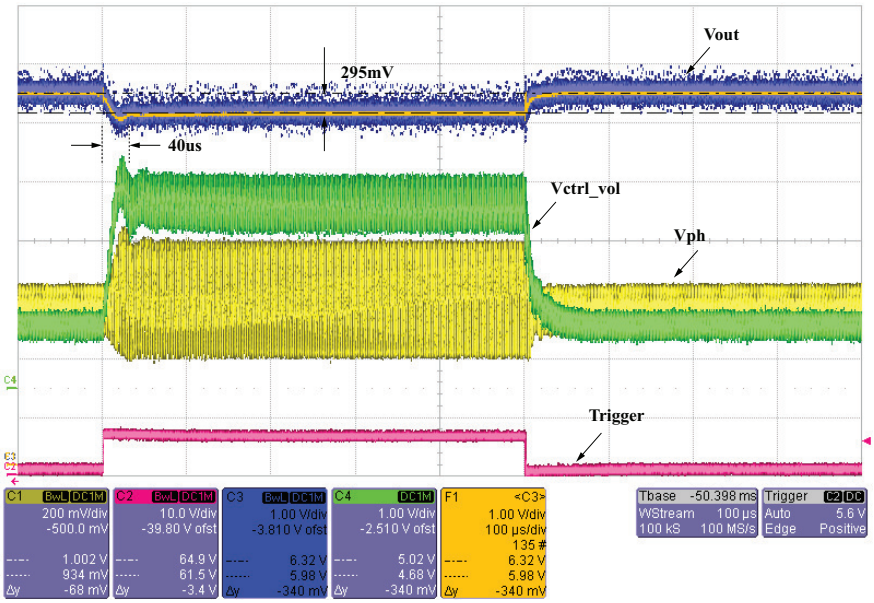


Figure 2.15: The transient waveforms of the output voltage (purple), phase error output (yellow), voltage control output (green) under the load steps of 0.5A to 1.5A and 1.5A to 0.5A triggered by the external pulse (pink)

2.6 Burst Mode Operation

Based on the control scheme discussed above, the switching frequency would need to be held at a rather high value to support light load condition. At very light load condition, this is not power efficient since the switch gating loss will become dominant. In order to improve the efficiency at light load condition, burst operation is introduced and added to the controller presented earlier. The idea of combined burst mode control is illustrated in Fig. 2.16.

In previous discussion, switching frequency is set by voltage error feedback signal while the phase error feedback signal does not affect the operating frequency during steady state. Therefore, a hysteresis window for voltage error feedback signal is used as the arbitrator for burst operation. As shown in Fig. 2.16, V_{fb2} is the lower level of the hysteresis window which sets the upper limit of the switching frequency for normal operation. During normal operation, if the output voltage continues to increase under the light load, the controller will increase the switching frequency continuously by driving V_{ctrl_vol} down until it hits the lower boundary of hysteresis window. The signal $Burst\_EN$ is then triggered on and enables the Power ON/OFF control from the hysteresis comparator. During burst operation, the on/off time depends on the load condition and hysteresis window for the output voltage. When the load recovers to mid-range level or higher, the under shoot will draw the voltage error signal higher hitting the upper limit of the feedback hysteresis window, which disables the burst operation. Then the operation reverts to the normal operation.

Fig. 2.18 shows experimental signals during the burst operation. The converter is period-

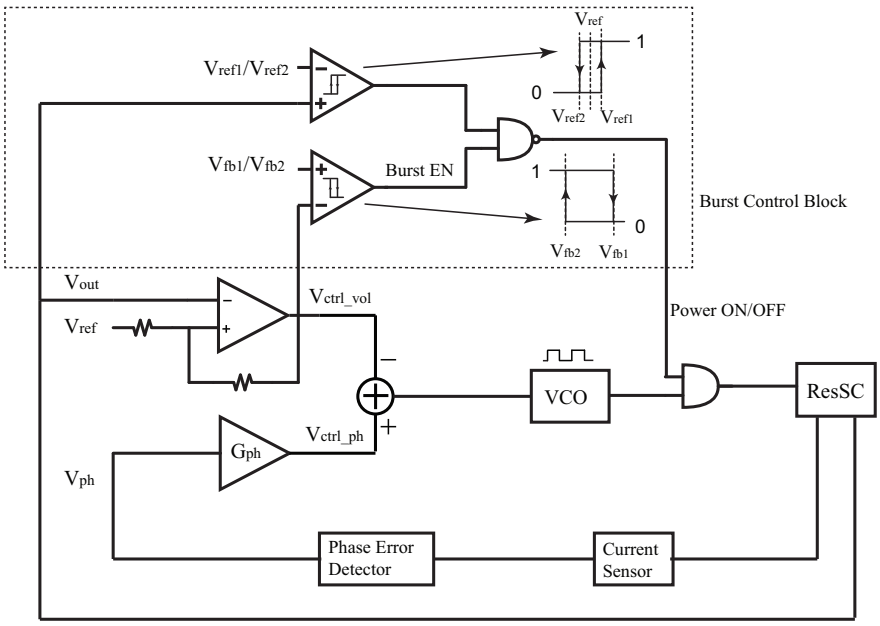


Figure 2.16: Control diagram with added burst mode function

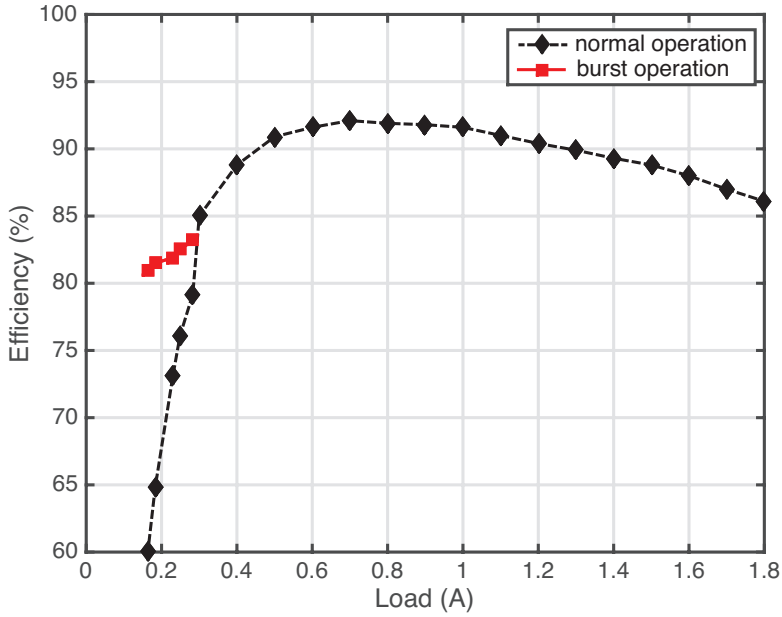


Figure 2.17: Efficiency comparison with and without burst mode operation when $V_{out} = 6V$ and $V_{in} = 24V$

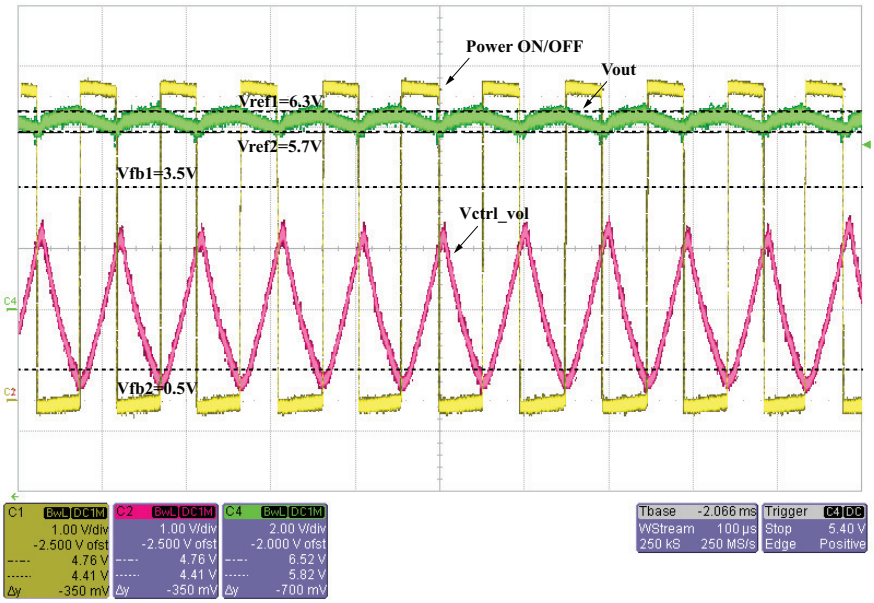


Figure 2.18: The waveforms of output voltage (green), voltage error feedback signal (pink) and Power ON/OFF signal (yellow) during steady state operation of burst mode

ically turned on and off after the burst operation is triggered. Fig. 2.17 shows the comparison of the efficiency with and without burst mode. The plot verifies the effectiveness of burst operation for efficiency improvement when the load drop below 20% of the full load. Therefore, with the combination of the burst mode, one can maintain the overall high efficiency over a wide load range.

Chapter 3

A Direct Battery-Connected Integrated Circuit Prototype

As a derivation of Stack-ResSC, the AC-coupled stacked dual active bridge (Stack-DAB) is introduced in this chapter. This topology shares the same architecture as the Stack-ResSC with the key difference in the inductor current waveform. In Section 3.1, an overview of the topology and the basic operation are presented. Section 3.2 introduces modeling methodology for a general N:1 Stack-DAB analogous to that for Stack-ResSC. The large signal operating points and small signal dynamics are evaluated with this method. Section 3.3 discusses the design considerations along with the selection of the passives. Section 3.4 presents the overall system architecture and the circuit implementations of the whole system. A load line based controller facilitated by the developed small signal model is designed and implemented in the same chip. Experimental results are given in Section 3.5.

3.1 Architecture Overview

Fig. 3.1 (a) shows the converter topology of a single-phase 3:1 example. The top two ladder stages are driven by the same complementary gate signal pair $\Phi_{top}/\bar{\Phi}_{top}$, which leads the bottom complementary gate signal pair $\Phi_{bot}/\bar{\Phi}_{bot}$ by a certain phase angle θ. Capacitors C_{r1} and C_{r2} are AC coupling capacitors which block the DC voltages between the top two switching nodes and the bottom switching node, so that AC square waves generated by the top and bottom half bridges are applied across the inductor L_r. The inductor current is determined by its imposed AC voltage swing, as detailed in Fig. 3.1 (b).

The 3:1 topology can be degenerated into a simple 2:1 model as shown in Fig. 3.2(b) with the awareness that the current flowing in each of top ladders is half of the current in the inductor. In turn, the degenerated 2:1 circuit can evolve into an N:1 circuit just by splitting the top stage into (N-1) slices and series stacking one on the top of another. All (N-1) top stages work in parallel in the AC sense. The conversion ratio N can be chosen according to the input range and available integrated circuit devices. For an integrated solution, splitting

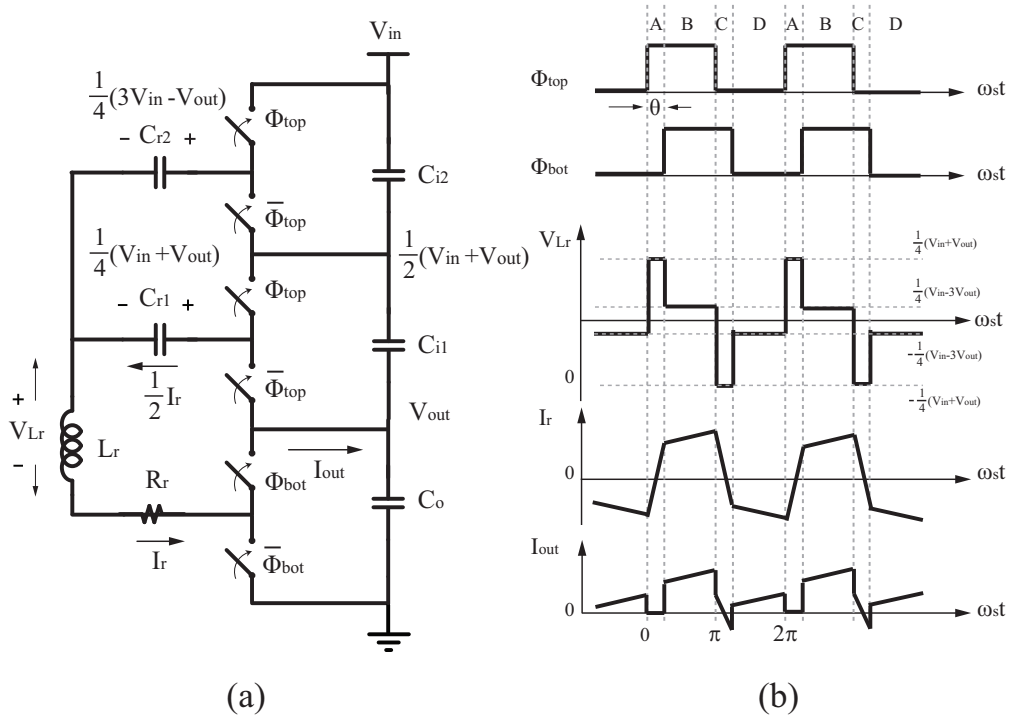


Figure 3.1: Steady state waveforms of 3-to-1 AC-coupled stacked dual active bridge (Stack-DAB)

the top stage does not add additional switch area, which provides convenient scaling with process technology.

In the present work, available off-chip AC coupling capacitors have rather large capacitance values. These devices are selected mainly for their AC resistive impedance given a physical size constraint. Optimal selection resulted in AC coupling capacitors large enough such that their working ripple voltage turned out to be negligible. This is the major distinction between this topology and the Stack-ResSC in which the flying capacitors carry significant resonant voltage swings and form a moderately high Q tank with the inductor [70]. The DC voltages blocked by the coupling capacitors are annotated in Fig. 3.1 (a). The resulting inductor waveform takes a trapezoidal shape in this topology, while in the Stack-ResSC circuit, a more sinusoidal current waveform is present.

Similar to Stack-ResSC, the zero crossing of the inductor current falls within the interval set by Φ_{top} and Φ_{bot}, zero voltage switching (ZVS) can be effected for all the switching nodes with properly adjusted dead time. Parasitics capacitance associtated with switching nodes can then be soft charged. More discussion about this is given in Section 3.2. In a low voltage IC implementation, the majority of the dynamic switching loss comes from gate charge. Thus, the benefit of ZVS is limited to certain extent.

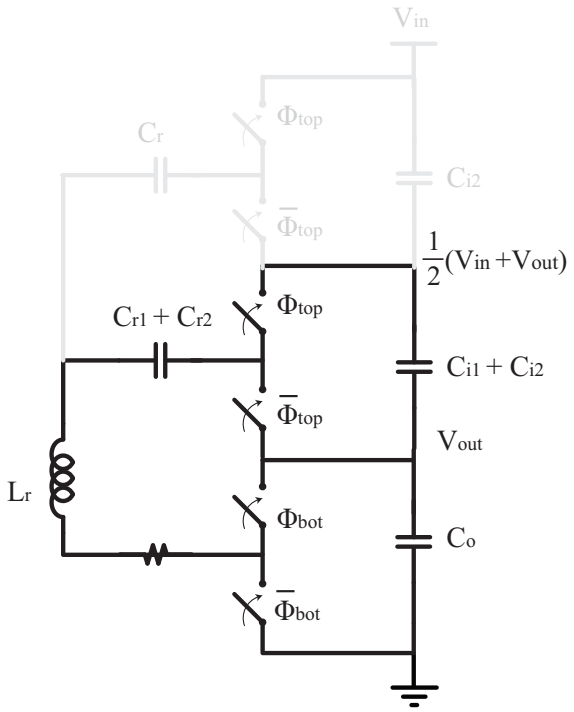


Figure 3.2: Degenerated 2-to-1 circuit for 3-to-1 Stack-DAB

3.2 Modeling Methodology

The current delivered to the output is determined by the inductor current and the switch state. The steady state inductor current waveform can be solved by integrating the first order differential equation of the inductor waveform. However, by comparing the inductor waveform with its fundamental component, as shown in Fig. 3.3 and Fig. 3.4, it is seen that the actual current waveform is well approximated with its fundamental component. Thus, a fundamental approximation can still be used to capture the large signal operating points and small signal dynamics with reasonable accuracy. This is in consistent with the modeling methods used for ResSC [56], where the fundamental component is even more dominant with a high Q tank.

3.2.1 Large Signal Model and Operating Points

To obtain the operating points in the steady state operation, the generalized averaging method [69] is applied to the state-space equations of the converter. For the sake of more

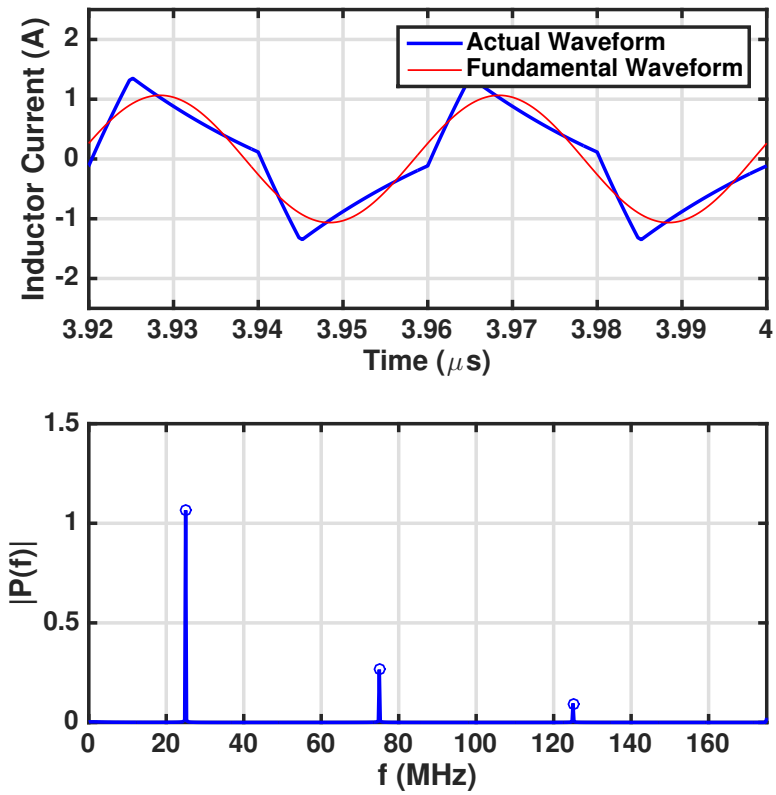


Figure 3.3: Simulated inductor current waveform with fundamental component overlaid (top) and magnitude spectrum of inductor current (bottom) for V_{in}=3.6V, V_{out}=1.5V, θ=$\pi/4$, $f_{sw} = 25MHz$, $L_r = 4nH$

general application, equations below are derived for any N-to-1 Stack-DAB topology:

$$\begin{aligned}
\frac{di_{L_r}}{dt} &= \frac{1}{L_r}[s_i(v_{out} + \frac{V_{in} - v_{out}}{N-1}) + (1-s_i)v_{out} - ... \\
&\quad - s_o v_{out} - i_{L_r}R_r - v_{C_r}] \\
\frac{dv_{C_r}}{dt} &= \frac{1}{C_r} i_{L_r} \\
\frac{dv_{out}}{dt} &= \frac{1}{C_o}[s_o s_i i_{L_r} - (1-s_i)(1-s_o)\frac{i_{L_r}}{N-1} + ... \\
&\quad + \frac{N-2}{N-1} i_{Lr} s_o (1-s_i) - I_{load}]
\end{aligned} \tag{3.1}$$

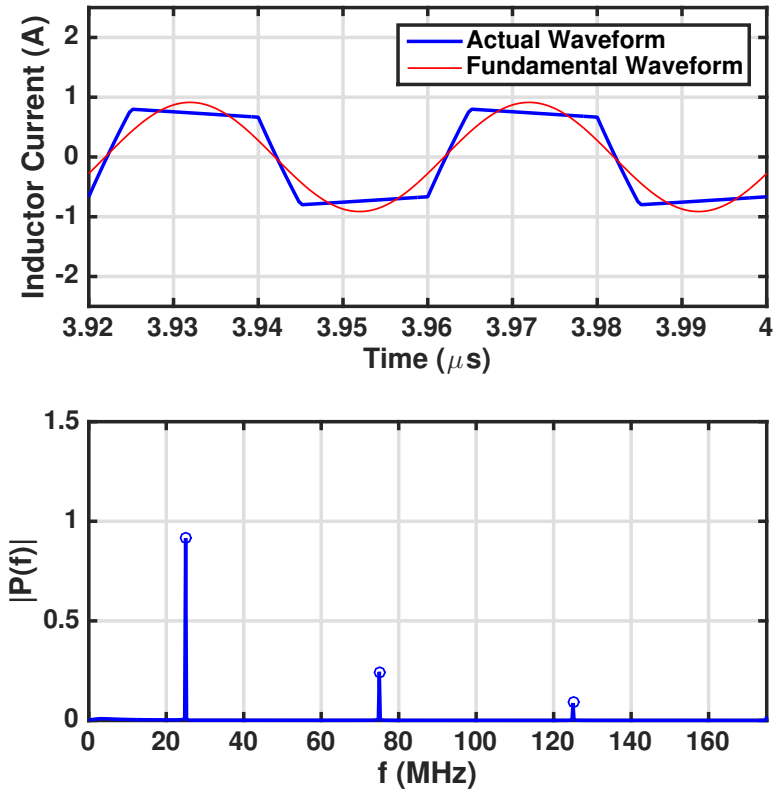


Figure 3.4: Simulated inductor current waveform with fundamental component overlaid (top) and magnitude spectrum of inductor current (bottom) for V_{in}=3.6V, V_{out}=1.1V and θ=$\pi/4$,$f_{sw} = 25MHz$, $L_r = 4nH$

where s_i and s_o represent the switching function of top stages and bottom stages, which take the form:

$$\begin{aligned} s_i &= \frac{1}{2}\{sign[sin(\omega t)] + 1\} \\ s_o &= \frac{1}{2}\{sign[sin(\omega t - \theta)] + 1\} \end{aligned} \tag{3.2}$$

Applying the averaging operator $\langle\bullet\rangle_1$ to the i_{L_r} state equations and operator $\langle\bullet\rangle_0$ to the v_{C_r} and v_{out} state equation where $\langle\bullet\rangle_k$ represents the kth order complex Fourier coefficient, which is also equivalent to the phasor transformation in [71]. Noticing that $\langle v_{C_r}\rangle_1 = 0$ if the ripple of the coupling capacitance are neglected and since $\langle i_{L_r}\rangle_0 = 0$, it follows that:

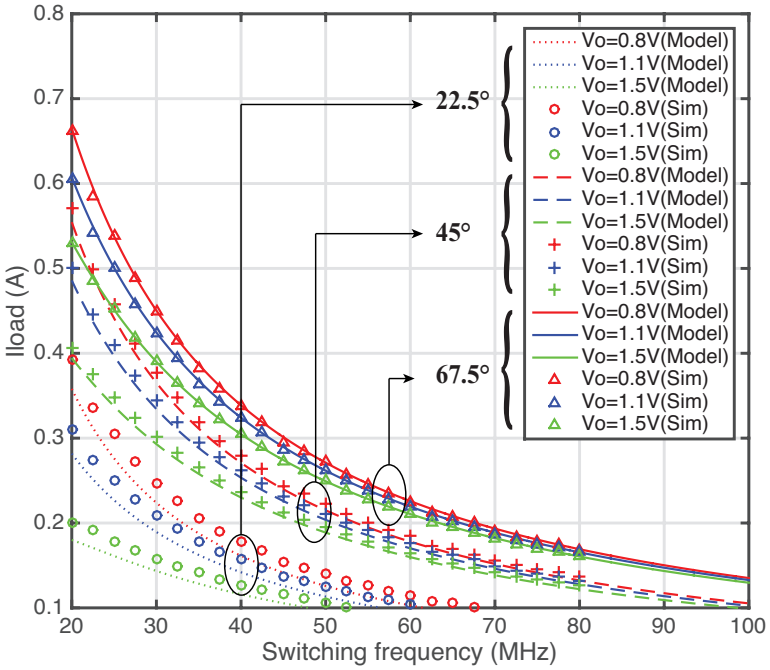


Figure 3.5: Comparison of the operating points for supported load current versus operating frequency. The discrete data correspond to time domain simulations. The curves are predictions from Eq. 3.7 for V_{in}=3.6V, L_r=4nH, R_r=150mΩ with different phase angles

$$\begin{aligned}\frac{d\langle i_{L_r}\rangle_1}{dt} &= -j\omega\langle i_{L_r}\rangle_1 + \frac{1}{L_r}[\frac{1}{N-1}(\langle s_i\rangle_1 V_{in} - ... \\ &\quad - \langle s_i\rangle_1\langle v_{out}\rangle_o) - \langle v_{out}\rangle_0\langle s_o\rangle_1 - \langle i_{L_r}\rangle_1 R_r] \\ \frac{d\langle v_{out}\rangle_0}{dt} &= \frac{1}{C_o}[\frac{1}{N-1}(\langle s_i\rangle_{-1}\langle i_{L_r}\rangle_1 + \langle s_i\rangle_1\langle i_{L_r}\rangle_1) + ... \\ &\quad + \langle s_o\rangle_{-1}\langle i_{L_r}\rangle_1 + \langle s_o\rangle_1\langle i_{L_r}\rangle_{-1} - I_{load}]\end{aligned} \tag{3.3}$$

The variable $\langle v_{out}\rangle_0$ represents the output voltage which is real, while $\langle i_{Lr}\rangle_1$ relates to the fundamental current component. The complex variable $\langle i_{Lr}\rangle_1$ can be decomposed into its real and imaginary parts:

$$\langle i_L\rangle_1 = \frac{1}{2}X_{i_{L_r}} + j\frac{1}{2}Y_{i_{L_r}} \tag{3.4}$$

Here, $X_{i_{L_r}}$ and $Y_{i_{L_r}}$ are the real and imaginary coordinates of the phasor representation of the inductor current, and with:

$$\begin{aligned} \langle s_i \rangle_1 &= -j\frac{1}{\pi} \\ \langle s_o \rangle_1 &= -j\frac{1}{\pi}e^{-j\theta} \end{aligned} \tag{3.5}$$

The real-valued state space equations are obtained:

$$\begin{aligned} \frac{dX_{i_L}}{dt} &= -\frac{R_r}{L_r}X_{i_{L_r}} + \omega Y_{i_{L_r}} + \frac{1}{L_r}\frac{2}{\pi}sin\theta V_{out} \\ \frac{dY_{i_L}}{dt} &= -\omega X_{i_{L_r}} - \frac{R_r}{L_r}Y_{i_{L_r}} + \frac{1}{L_r}\frac{2}{\pi}(\frac{1}{N-1} + ... \\ &\quad + cos\theta)V_{out} - \frac{1}{L_r}\frac{1}{N-1}\frac{2}{\pi}V_{in} \\ \frac{dV_o}{dt} &= \frac{1}{C_o}[-\frac{1}{\pi}sin\theta X_{i_{L_r}} - \frac{1}{\pi}(\frac{1}{N-1} + ... \\ &\quad + cos\theta)Y_{i_{L_r}} - I_{load}] \end{aligned} \tag{3.6}$$

In the steady state, with all the derivatives go to zero in Eq. 3.6, the steady state equation can be obtained that yields the operating point as:

$$\begin{aligned} I_{load} = -\frac{2}{\pi^2}\frac{R_r}{{R_r}^2 + (\omega L_r)^2}(V_{out} - \frac{V_{in} - V_{out}}{(N-1)^2} - ... \\ - \frac{V_{in}}{N-1}\frac{\omega L_r}{R_r}sin\theta - \frac{V_{in} - 2V_{out}}{N-1}cos\theta) \end{aligned} \tag{3.7}$$

From Eq. 3.7, the operating points of the converter can be uniquely determined by phase shift θ and switching frequency ω given specified input voltage, output voltage and output load current. To verify the effectiveness of the large signal model, Fig. 3.5 shows a comparison between the time domain simulation and prediction from Eq. 3.7. Under larger phase angle, it can be seen that the model matches the time domain simulation very well. As the phase angle reduces, the mismatch increases. This is due to the fact that when the converter is operating with smaller phase angle, the relative magnitudes of high order harmonics become more significant, but the general trends are still consistent with adequate accuracy in modeling. Overall, the fundamental approximation gives a reasonably good estimate of the operating points. Also as seen in Fig. 3.5, smaller phase angle offers lower load current at fixed frequency given input and output voltages. For the same load condition, operation under smaller phase angle, if possible, can result in smaller operating frequency and smaller circulating current. Both of these effects improve the efficiency. This can be understood intuitively if the degenerated 2:1 circuit is further simplified into an AC circuit model as shown in Fig. 3.6 (a) and (b). The AC coupling capacitor is treated as a DC block

and neglected in the AC circuit, in which the inductor is driven by two AC square waves V_x and V_y with a phase shift θ. Using the fundamental approximation, one only needs to consider the fundamental frequency component. The fundamental voltage phasor $\overrightarrow{V}_x$ and $\overrightarrow{V}_y$ and resulting current phasor $\overrightarrow{I}_L$ take the forms of:

$$\begin{aligned}\overrightarrow{V}_x &= \frac{2}{\pi}\frac{1}{N-1}(V_{in}-V_{out})e^{j\theta}\\ \overrightarrow{V}_y &= \frac{2}{\pi}V_{out}\\ \overrightarrow{I}_L &= \frac{\overrightarrow{V}_T}{Z_L} = \frac{\overrightarrow{V}_x-\overrightarrow{V}_y}{j\omega L_r+R_r}\end{aligned} \tag{3.8}$$

The output current is directly related to inductor current and phase shift θ. Under a large phase angle, a large AC voltage $\overrightarrow{V}_T$ is applied across the inductor such that inductor current becomes larger. As shown in Fig. 3.6 (c), when the converter operates around the nominal N:1 conversion ratio, the current phasor lies within the interior angle set by $\overrightarrow{V}_x$ and $\overrightarrow{V}_y$. In this case, ZVS can be effected along with a proper dead-time to soft charge the parasitic capacitors at the switching nodes.

Given the operating points as shown in Fig. 3.5, there exist two obvious single-input control methodologies for output voltage regulation: modulating the switching frequency ω given θ or modulating θ given the switching frequency ω. In this work, the first methodology is chosen due to the design simplicity. Controlling the phase needs additional loop for locking the phase. A fixed phase angle is selected for a required range of input and output combinations and is not tuned dynamically.

Generally, the large signal model derived from the fundamental approximation provides guidance to the operation of the proposed converter and at the same time offers a simplified and intuitive way for understanding the overall behavior.

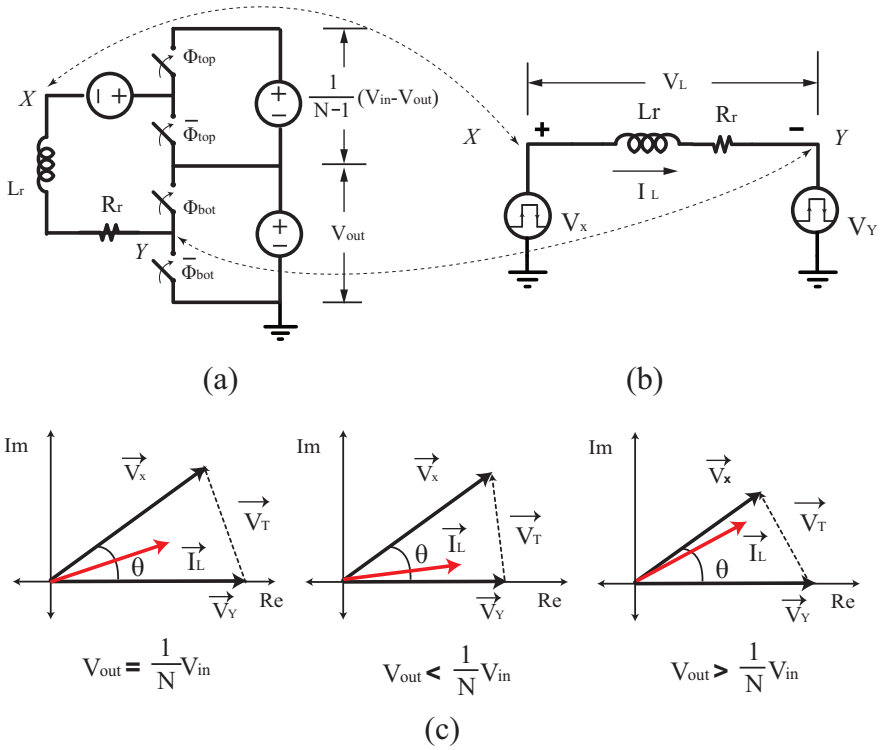


Figure 3.6: (a) Degenerated circuit for 3-to-1 AC-coupled DAB, (b) simplified AC circuit of degenerated circuit, (c) phasor model for varying phase angle given input and output voltage, (d) phasor model for varying output voltage given phase angle and input voltage

3.2.2 Small Signal Model

$$\begin{bmatrix} \frac{d\hat{x}_{i_{Lr}}}{dt} \\ \frac{d\hat{y}_{i_{Lr}}}{dt} \\ \frac{d\hat{v}_{out}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_r}{L_r} & \Omega & \frac{1}{L_r}\frac{2}{\pi}\sin\theta \\ -\Omega & -\frac{R_r}{L_r} & \frac{1}{L_r}\frac{2}{\pi}(\frac{1}{N-1}+\cos\theta) \\ -\frac{1}{C_o}\frac{1}{\pi}\sin\theta & -\frac{1}{C_o}\frac{1}{\pi}(\frac{1}{N-1}+\cos\theta) & 0 \end{bmatrix} \begin{bmatrix} \hat{x}_{i_{Lr}} \\ \hat{y}_{i_{Lr}} \\ \hat{v}_{out} \end{bmatrix} + \begin{bmatrix} Y_{i_{Lr}} & 0 \\ -X_{i_{Lr}} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \begin{bmatrix} \hat{\omega} \\ \hat{i}_{load} \end{bmatrix} \tag{3.9}$$

$$\hat{v}_{out} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{x}_{i_L} \\ \hat{y}_{i_L} \\ \hat{v}_{out} \end{bmatrix}$$

In order to facilitate the controller design, one has to understand the small signal dynamics of the proposed converter. To obtain the small signal model, we apply the small

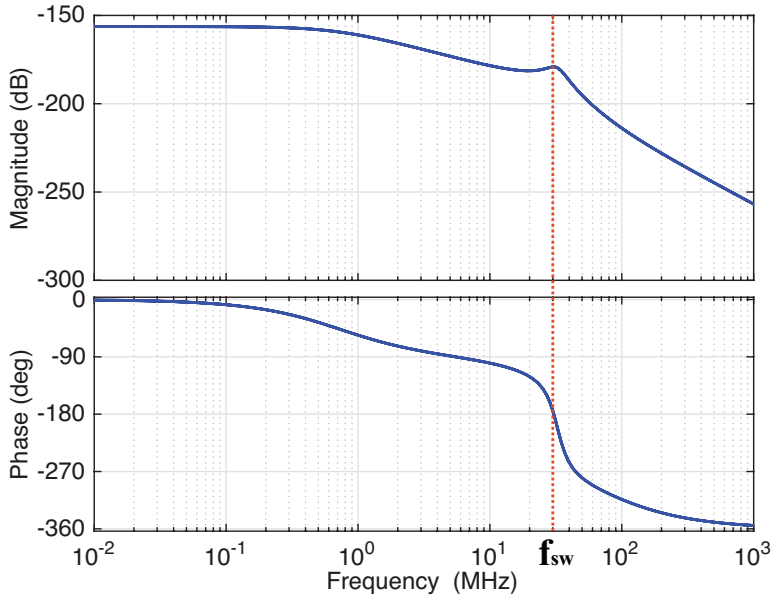


Figure 3.7: Magnitude and phase response of small signal dynamics of $\| H \|_{\omega \to v_{out}}$ with design parameters of $L_r = 4nH, C_r = 516nF, R_r = 150m\Omega, C_o = 20nF$ and at operating condition of $f_{sw} = 30MHz, Vin = 3.6V, Vout = 1.2V, I_{load} = 300mA, \theta = \pi/4$.

signal perturbation to Eq. 3.6. As the phase angle is not tuned dynamically, the switching frequency and load current are treated as inputs to the converter model. Then the real small signal state space model is obtained as Eq. 3.9.

With the model of Eq. 3.9, the small signal transfer functions from the switching frequency to the output voltage ($\| H \|_{\omega \to v_{out}}$) are evaluated based on the law of state space representation to transfer functions. The magnitude and phase response of the transfer function are shown in Fig. 3.7. As illustrated in Fig. 3.7, the dynamics of switching frequency to output voltage consists of one dominant pole from the output capacitance at low frequency followed by a pair of damped resonant pole around the switching frequency. A right plane zero exists at very high frequency and it is not within the design consideration. Fig. 3.8 compares the step reponse predicted by derived transfer function with the simulated waveforms under 5% input pertubations, which verifies the effectiveness of the developed small signal model. Since the dominant pole is located at a frequency that is much lower than the resonant poles, the compensation is trivial. Therefore, a simple lag compensator can complete a tight control and a proper finite DC gain can be selected to realize a load line regulation. By contrast, in ResSC/Stack-ResSC the resonant poles are close to the dominant pole which requires a more dedicated compensation strategy for high loop bandwidth as discussed in Chapter 2.

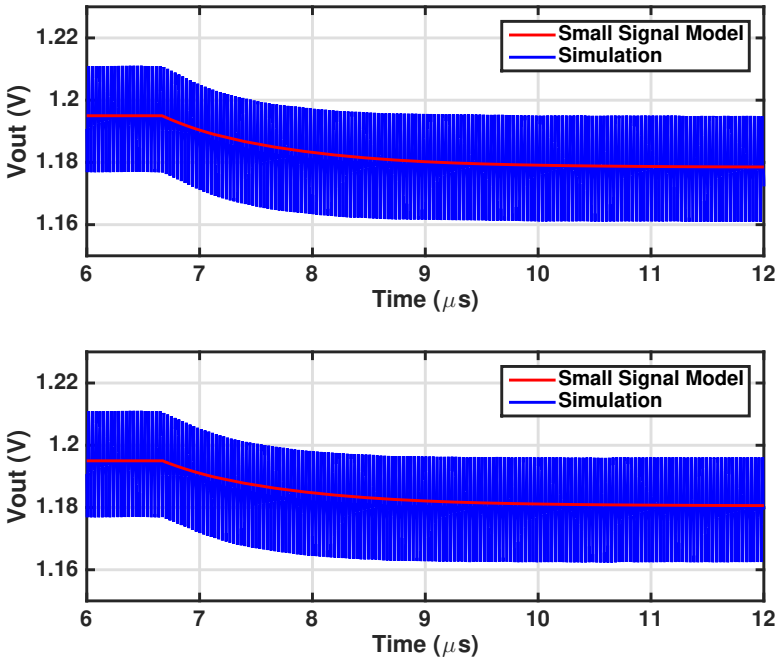


Figure 3.8: Comparison of step response from small signal model and simulation with 5% load (top) and frequency (bottom) pertubation

3.3 Design Consideration

The AC-coupled Stack-DAB can be viewed as the Stack-ResSC operating at a frequency that is much higher that the resonant frequency set by the coupling capacitor (C_r) and working inductor (L_r). Since the fundamental frequency approximation is valid in the Stack-DAB with reasonable accuracy, it is used for efficiency analysis as discussed below.

3.3.1 Efficiency Evaluation

The load current is related to fundamental component of the inductor current by:

$$K_i = \frac{I_{rms}}{I_{load}} = \frac{\sqrt{X_{i_{Lr}}^2 + Y_{i_{Lr}}^2}}{\sqrt{2} I_{load}} \tag{3.10}$$

where I_{load} and $X_{i_{Lr}}$ and $Y_{i_{Lr}}$ can be obtained from Eq. 3.7 and Eq. 3.6. Parameter K_i can be thought of as a measure of the reciprocal of power factor at the rectifying output stage. Given a certain load condition, the higher K_i, the more circulation current loss.

Fig. 3.9 and Fig. 3.10 plot K_i versus various operating conditions. It can be seen that K_i is generally within the range of 1.5 to 3. Operating with a smaller phase angle or under lower

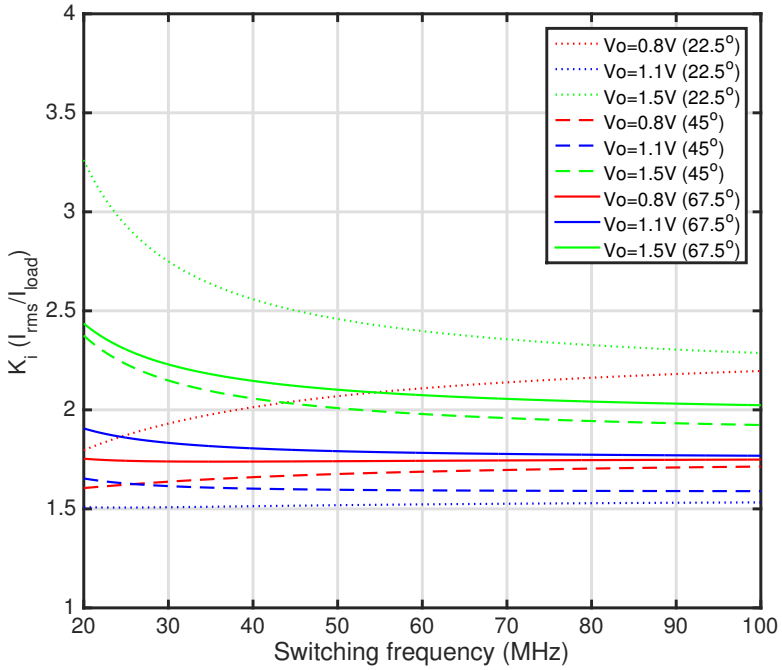


Figure 3.9: K_i versus operating conditions across different output voltage at $V_{in} = 3.6V$ for different phase angles of 22.5^o, 45^o and 67.5^o

input voltage causes large K_i variation across the output range. This can be interpreted from the geometry constraint of the phasor model shown in Fig. 3.6. The dependence of K_i over operating frequency is related to the finite time constant of inductor. In the simulation an inductor of 4nH with 150mΩ equivalent series resistance is used. As the frequency reduces, the current phase deviates from the ideal position as shown in the phasor diagram when the period approaches the time constant of the inductor (26.7ns), and causes additional degradation of the power factor. To start with, a K_i of 1.75 is used for the optimization in the typical case when the converter is operated at a frequency that is much higher than resonant frequency set by C_r and L_r.

Since there is no intrinsic charge sharing loss and the bottom plate losses can be potentially eliminated with ZVS, the losses of the converter stem from the power switches and conduction losses of the inductor and capacitor equivalent series resistance (R_{esr}) as given by:

$$P_{loss} = I_{rms}^2 R_{esr} + I_{rms}^2 \frac{R_{on}}{W_{sw}} + C_{sw} V_{sw}^2 W_{sw} f_{sw} \tag{3.11}$$

where R_{on} is the switch resistance density measured in $\Omega \cdot m$, W_{sw} (m) is the total width of switches; and V_{sw} is the gate voltage swing, C_{sw} is gate capacitance density (F/m) of the

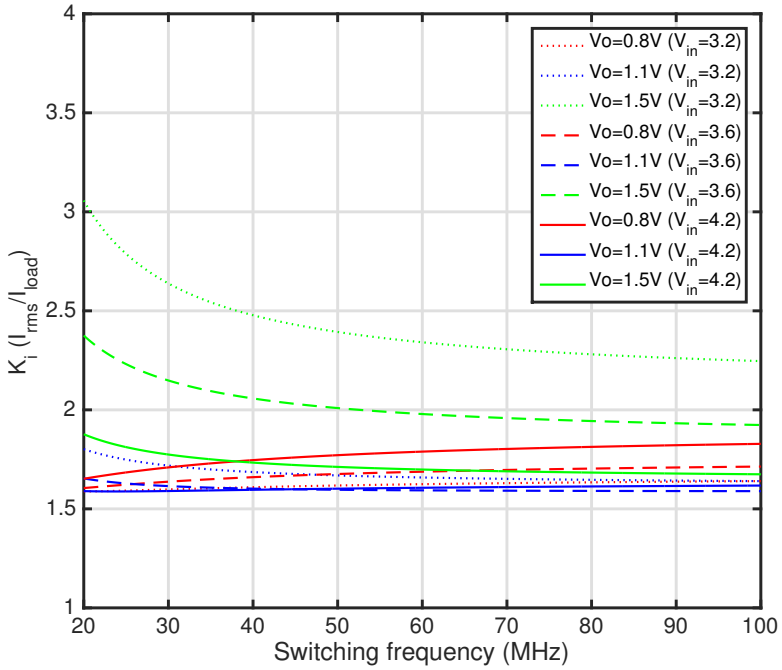


Figure 3.10: K_i versus operating conditions across different output voltage at the phase angles of 45^o for different input voltages of 3.2V, 3.6V and 4.2V

switches. Since I_{rms} and f_{sw} are determined by the operating condition, the only design variable that can be optimized is the W_{sw}. The minimal loss with optimized switch widths is given by:

$$\begin{aligned} P_{loss\_opt} &= K_i^2 I_{load}^2 R_{esr} + 2K_i I_{load} V_{sw} \sqrt{R_{sw} C_{sw} f_{sw}} \\ W_{sw\_opt} &= \frac{I_{rms}}{V_{sw}} \sqrt{\frac{R_{sw}}{C_{sw} f_{sw}}} \end{aligned} \tag{3.12}$$

Fractional loss can be expressed as :

$$\frac{P_{loss\_opt}}{P_{out}} = K_i^2 \frac{I_{load} R_{esr}}{V_{out}} + 2K_i \sqrt{R_{sw} C_{sw} f_{sw}} \frac{V_{sw}}{V_{out}} \tag{3.13}$$

Given operating conditions and optimized switch size, the only way to improve efficiency is to improve the quality factor of passive components by lowering R_{esr}. As noted, the parameter R_{esr} is a combination of ESR of the inductor and capacitors.

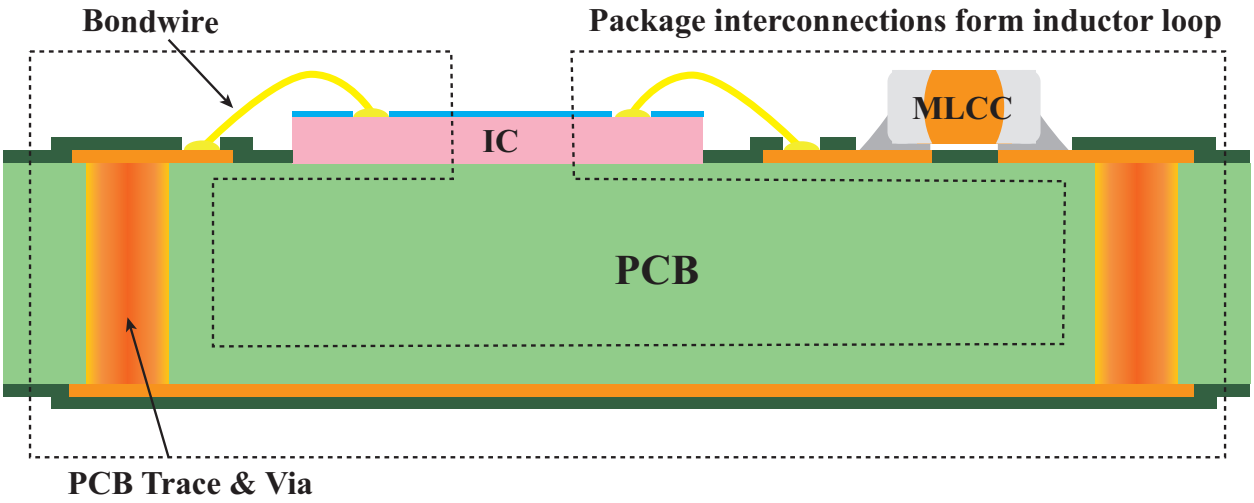


Figure 3.11: Concept view of physical implementation of the system using PCB trace inductor and off-chip capacitors

3.3.2 Passive Options and Implementation

Achieving a high quality inductor on die is challenging [72]. The performance of on-die spiral inductors is not attractive [73] [74] [31]. SMD chip inductors are bulky and area consuming. Inductors built from bondwires or PCB traces are practical for achieving a small amount of inductance, and promising for integration within the package. Prior works have adopted the package inductors in the range of a few nH [29] [75] [12]. In this work, inductors built from PCB traces are selected over bondwires due to better matching, controllability and lower ESR.

In order to take advantage of the parasitics within the package, the passives and the active circuits are assembled as shown in Fig. 3.11. The AC coupling capacitors are attached as separate chips (silicon caps) or discrete components (MLCC). The traces and vias that bridge the active chip and capacitor chips are constructed to realize the required inductance. In this way the LC loop is formed within the package, and it absorbs the parasitics of interconnection along with the bondwires and the ESL of the coupling capacitors. The selection of discrete capacitors is based on the minimum ESR given the allowed package footprint. Another possible assembly can arrange the capacitor chips on the back of the active chip for further reducing the footprint. The bypass capacitors for the input, output and intermediate nodes are still tightly integrated within the active chip to enforce low impedance paths for all switching nodes.

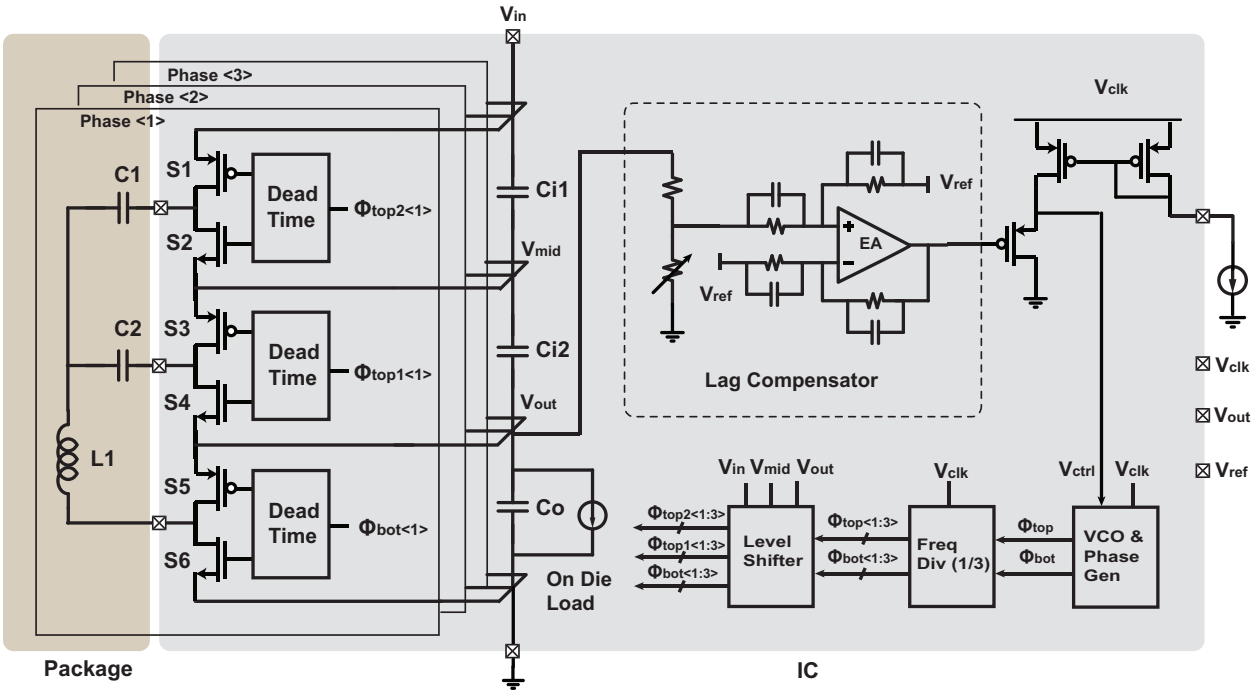


Figure 3.12: Overall system implementation with power train and controller

3.4 Circuit Techniques

The overall circuit implementation of the system is shown in Fig. 3.12. The power switches and bypass capacitors of the power train along with the controller and clock generation blocks are implemented on die. The AC coupling capacitors and the inductor are implemented off chip and organized as shown in Fig. 3.11. In order to relax the on-die bypass capacitor requirement, three phase have been adopted. The odd number of phases has been reported to be more effective for sinusoidal ripple cancellation than an even number of phases [29]. According to the small signal dynamics discussed in Section. 3.2, a simple lag compensator with one pole and one zero is adopted to achieve a tight load line regulation with a finite DC gain of 40. The compensator is followed by a buffer that drives a voltage controlled ring oscillator that controls the switching frequency of the converter. When the output is higher than the reference voltage, the error signal amplified by the compensator raises the supply of the VCO, increasing the operating frequency so that output current gets reduced and output voltage drops until it falls closer to the reference voltage.

The phase shift between the top and bottom switches is generated by selecting proper taps from the chain of the ring oscillator. In this way, as frequency changes, phase shift is kept constant without requiring an additional phase locked loop. The schematic of the ring oscillator is shown in Fig. 3.15. It consists of 8 differential stages so that the minimum phase shift that can be generated between each tap is 22.5^o. Therefore, the phase angles that can

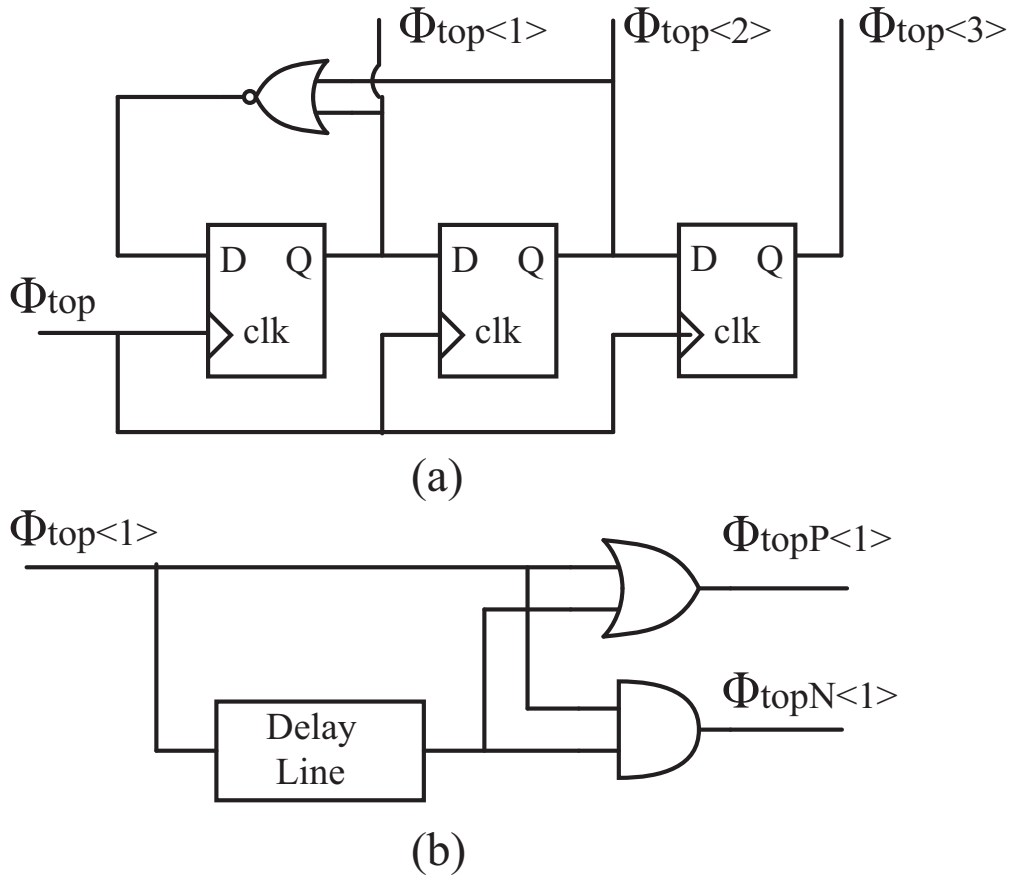


Figure 3.13: Circuit implementation of (a) one third frequency division block and (b) deadtime generation block

be enabled are integral multiples of 22.5^o. A 4-to-1 MUX is used to select the proper phase angle according to the input and output voltages.

The VCO is followed by a one-third frequency division block as shown in Fig. 3.13 (a) for generating synchronized phase-shift signals for three interleaved phases. Considering this arrangement, the taps selected from the ring oscillator require delays that equal three times the desired phase shift. A deadtime block shown in Fig. 3.13 (b) generates a proper dead time for gating the complementary switch pair within each half bridge to facilitate ZVS. Finally, a dynamic level shifter shifts gating signals from the V_{clk} domain to voltage domains in the top stages. The schematic of the dynamic level shifter is shown in Fig. 3.14. The AC coupling scheme in the dynamic level shifter ensures level-shifted gating signals that have better matching for each top stage. The gate drivers within each stage are driven directly from the local bypass capacitors, powered by V_{in}, V_{mid} and V_{out}.

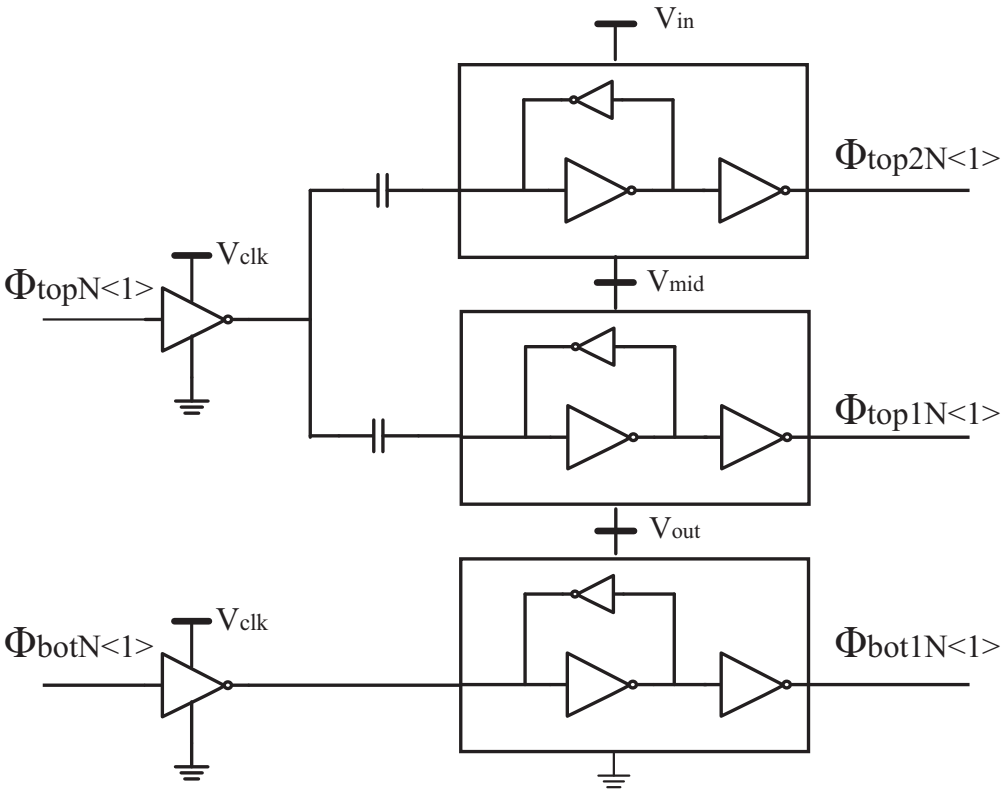


Figure 3.14: Circuit implementation of dynamic level shifter

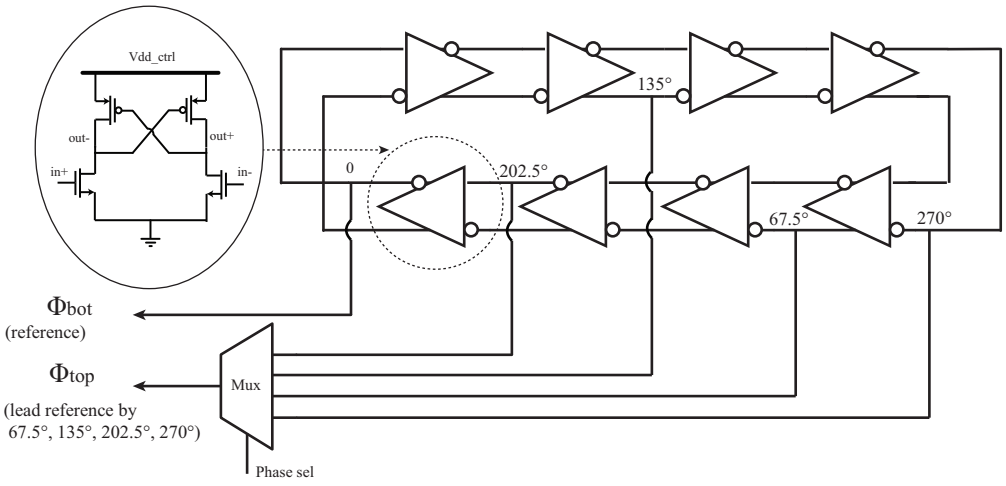


Figure 3.15: Voltage controlled ring oscillator with phase angle selection

3.5 Experimental Results and Discussion

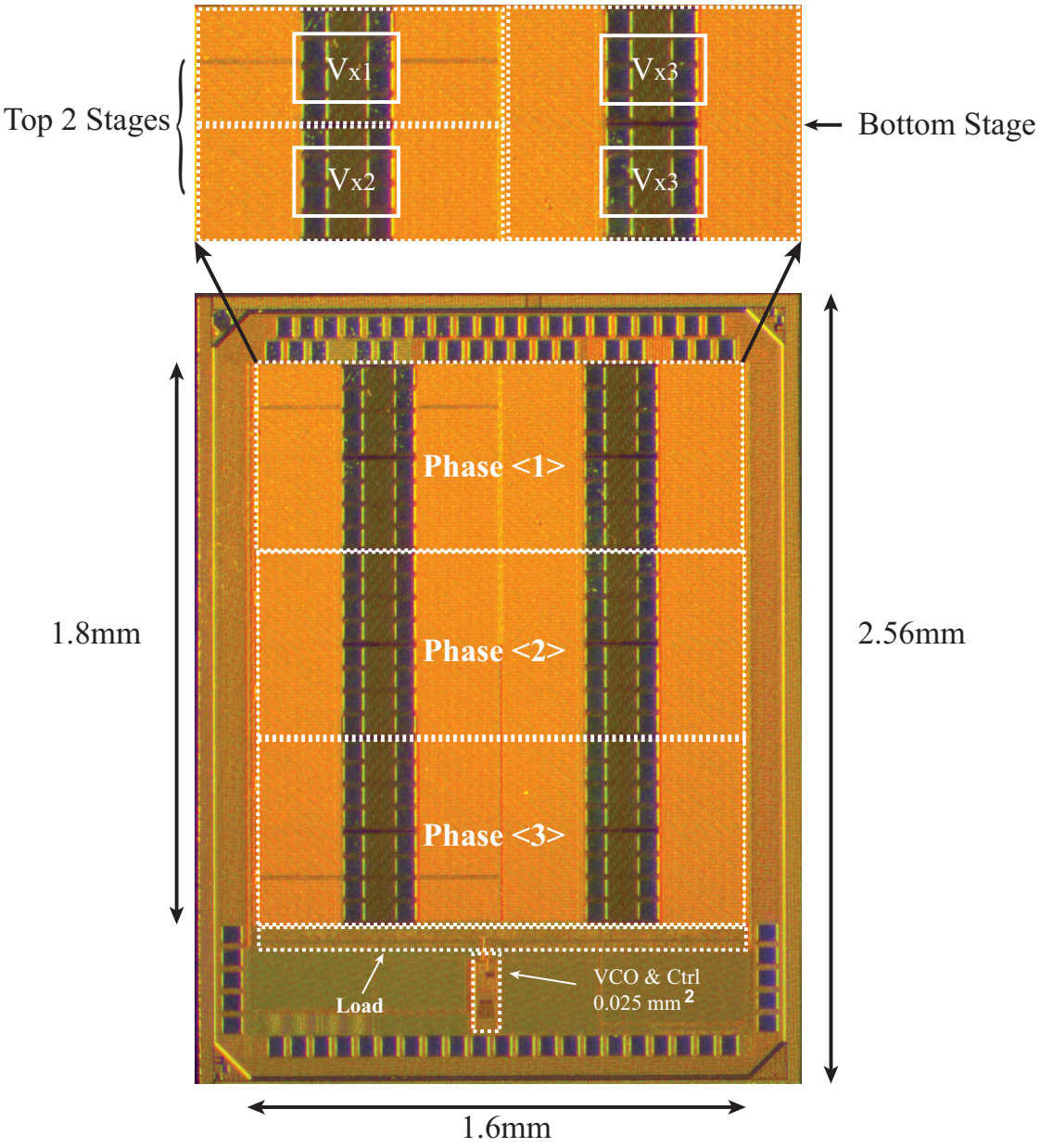


Figure 3.16: Die photo of the three-phase converter along with control and clock generation blocks

The design is implemented in TI's 0.15-μm CMOS process with Ferro-electric capacitor option. A die photo of the three phase converter along with the control and clock networks is shown in Fig. 3.16. The switches are all standard CMOS switches while the bypass capacitors

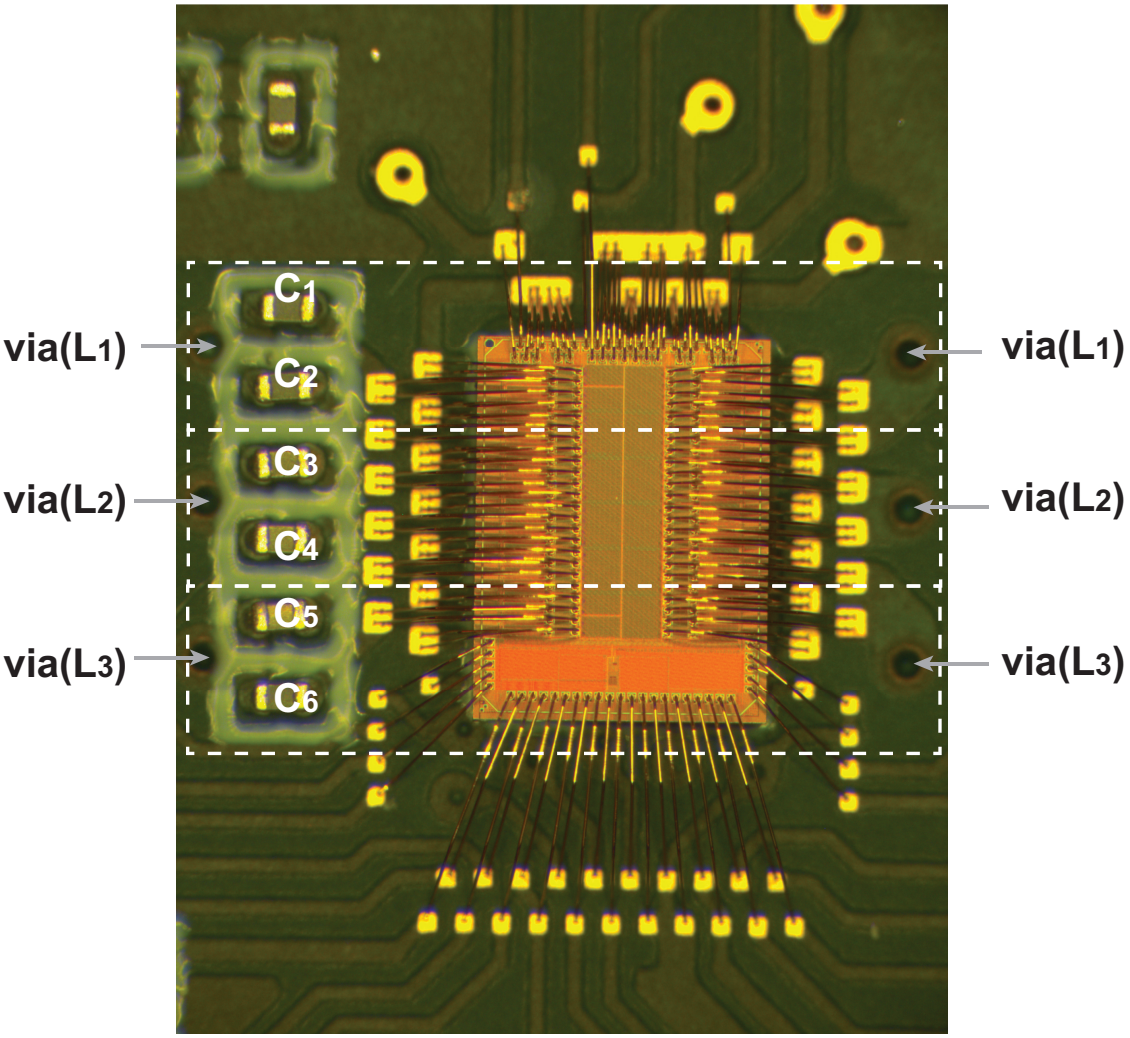


Figure 3.17: Chip on board photograph of the three-phase converter with passive implementation

are implemented with Ferro-electric capacitors. The effective die area is 2.9 mm^2 including the power train and control blocks. The converter consists of three phases. Thus, six AC coupling capacitors are needed with two for each phase. The AC coupling capacitors are implemented by using 01005 ceramic capacitors as show in Fig. 3.17. With these capacitors, a lumped area of 3.38 mm^2 is used to calculate the power density including the area of the off-chip components and active die area. The layout of a single phase is annotated on the die shot in Fig. 3.16. In each phase, 4 pads are dedicated to each of the top switching nodes V_{x1}, V_{x2} and 8 pads to the bottom switching node V_{x3}. The current flow through the bottom switching node is twice as much as the current flow through each top stage. The voltage rails V_{in}, V_{mid} and V_{out} are shared across all three phases. The total bypass capacitance

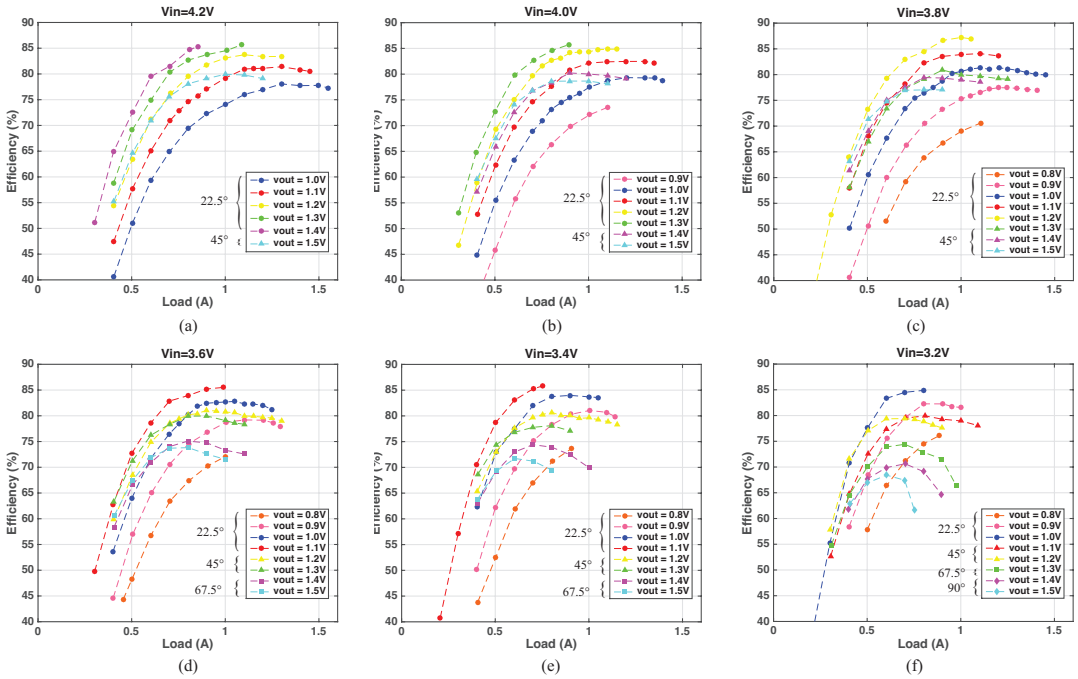


Figure 3.18: Measured efficiency versus load current under different output voltage for (a) $V_{in} = 4.2$, (b) $V_{in} = 4.0$, (c) $V_{in} = 3.8$, (d) $V_{in} = 3.6$, (e) $V_{in} = 3.4$, (f) $V_{in} = 3.2$. Phase angle is adjusted for different input and output combination to support sufficient load range

Table 3.1: The summary of the design specs, parameters and performance

Process	0.15μm
NO. of phases	3
Inductor per phase	4.2nH
AC coupling caps (per phase)	2 x 470nF MLCC(01005)
Total bypass caps	20nH
Input Range	3.2V - 4.2V
Output Range	0.8V - 1.5V
Operating Frequency	20 - 50MHz
Peak Efficiency	87.2%
Load Transient	50mV/400mA

dedicated to each top stage is 5nF (C_{i1} and C_{i2}), with 10nF for the bottom stage (C_o). The total on die bypass capacitor is 20nF. The overall design parameters and key performance are summarized in Table. 3.1.

Fig. 3.18 shows the measured efficiency vs load current for a range of output voltages and for an input voltage range from 3.2 to 4.2V. As discussed in Section 3.3, a small phase angle is preferred for better efficiency given the input and output voltages. However, larger phase angles have to be used in the case of a low input and a high output voltage to provide

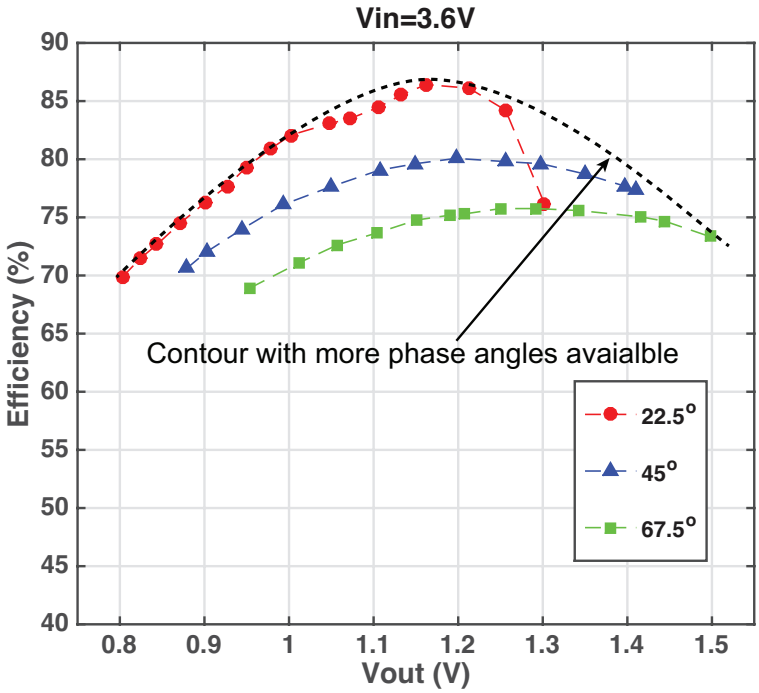


Figure 3.19: Measured efficiency versus output voltage with 3.6V input voltage and 0.9A load current under different phase angles

Table 3.2: The estimated loss breakdown

Input	3.6V	
Output	1.2V	
Load	1A	
Efficiency	85.8%	80.7%
Phase Angle	22.5^o	45^o
Operating Frequency	16MHz	28MHz
Total Loss (mW)	198.6	287
Dynamic Loss (mW)	96.9	163.3
Switch Conduction Loss (mW)	31.9	36.0
Interconnect/Tank ESR Loss (mW)	69.7	87.5
Control and VCO (mW)	0.1	0.2

sufficient load capability. It can be noticed that for for a 4.2V-3.8V input range, using a 22.5^o phase angle can cover most of the output range. A peak efficiency of 87.2% is achieved at 3.8V to 1.2V under 1A load current.

In Fig. 3.19, efficiency versus output voltage at the 3.6V input voltage and 0.9A load current is plotted. From Fig. 3.19, it can be noticed that operation with 22.5^o can cover output voltage up to 1.25 V. From the the trend of the available data in Fig. 3.19, an

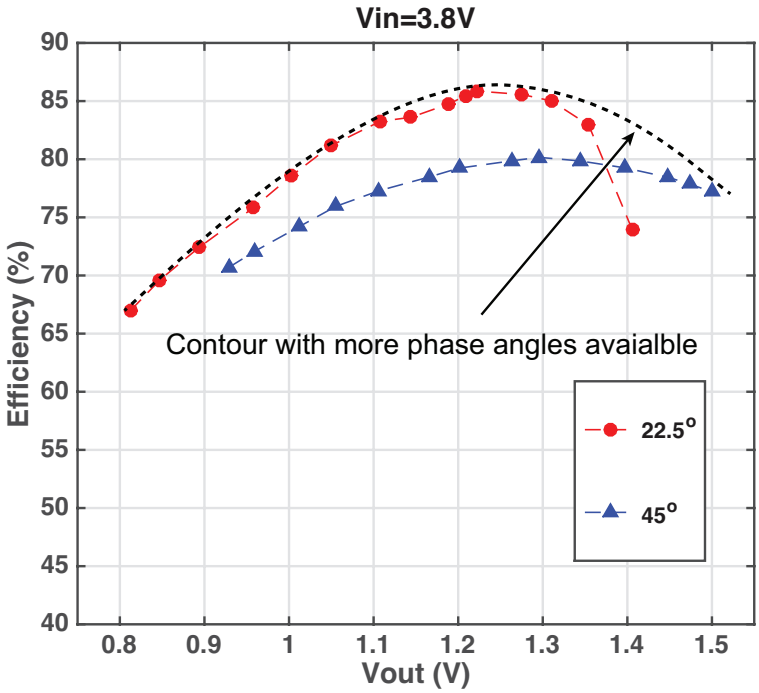


Figure 3.20: Measured efficiency versus output voltage with 3.8V input voltage and 0.9A load current under different phase angles

efficiency contour drawn in the dashed line can be predicted if more phase angles in the timing and drive circuitry are available. Fig. 3.20 plots efficiency versus output voltage at the 3.8V input voltage and 0.9A load current. Compared with Fig. 3.19, the transition point where a larger phase angle needs to come into effect happens at a larger output voltage. That means the range of necessary phase shift under a higher input voltage is less in relation to that with a smaller input voltage.

As seen in Fig. 3.19, the converter demonstrates the capability of efficiently covering a wide output range without the necessity of topology reconfiguration. This is in contrast to the SC based converters. The operating frequency versus the corresponding regulated output voltages is plotted in Fig. 3.21. As can be seen, the operating frequency under a small phase angle is lower given the same load and input/output voltage. This lowers the dynamic losses and circulating current losses in the converter and contributes to higher efficiency. To highlight this impact, Table. 3.2 shows the estimated loss breakdown for the same input/output and load condition under two different phase angles.

To verify the effectiveness of the control loop, a load step is applied to the converter. Fig. 3.22 shows the output waveforms with 400mA on-die load step. Due to adopted load line regulation, a finite 50mV DC error is present with 400mA load step. The transient waveforms show the converter is nicely compensated with a phase margin of 90 degrees. The

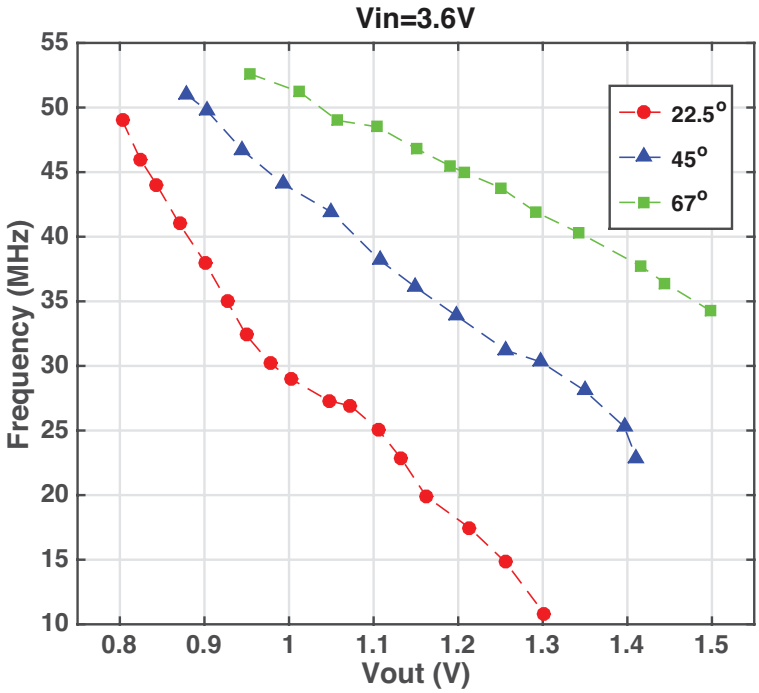
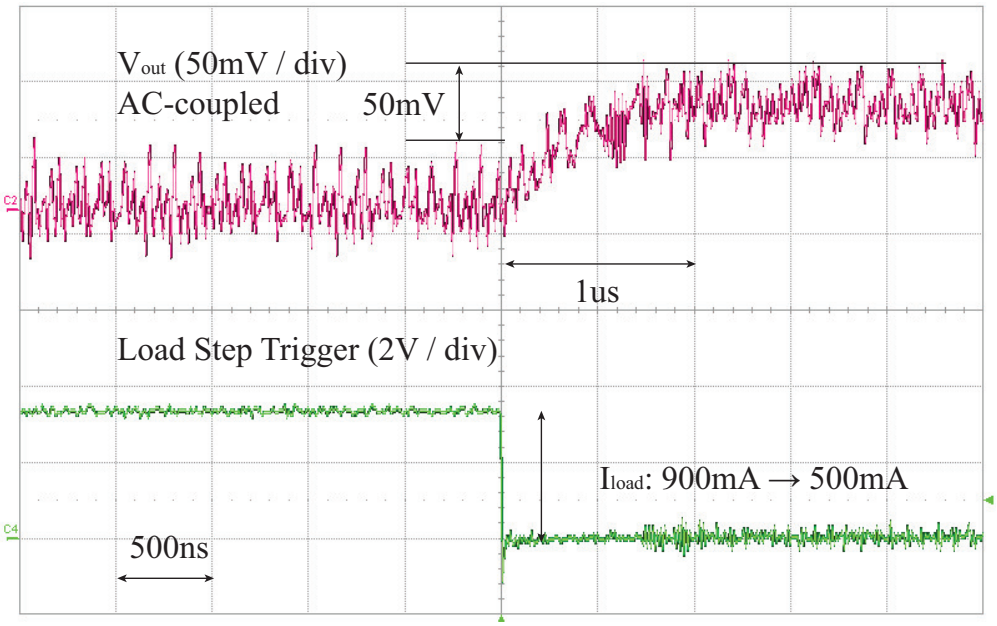


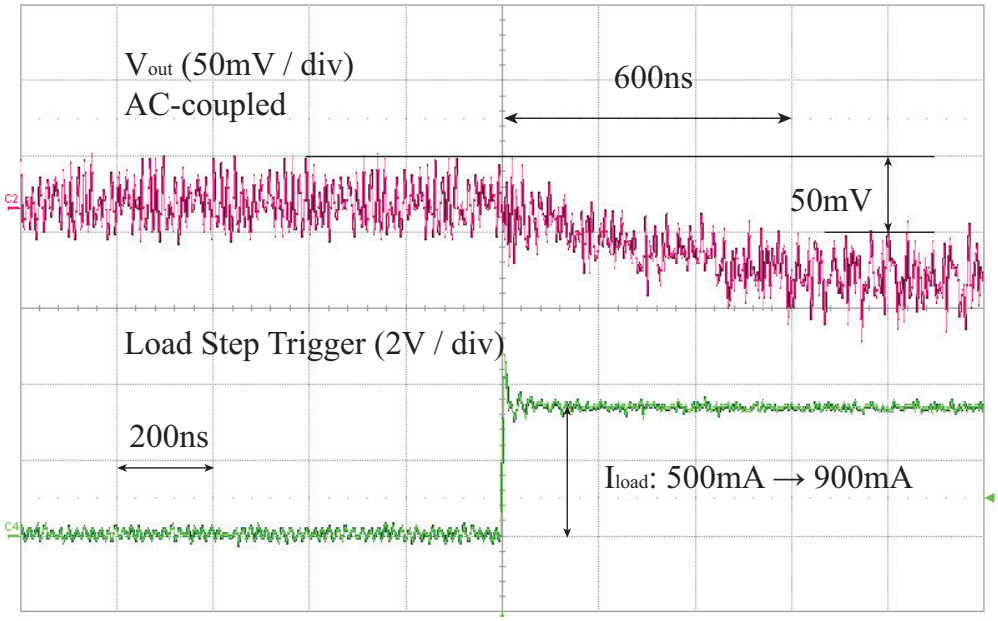
Figure 3.21: Measured frequency versus output voltage with 3.6V input voltage and 0.9A load current under different phase angles

response time for the step down and step up is 1μs and 600ns in each respective case. In this test, no external bypass capacitor is used at any terminal.

Finally, Table. 3.3 compares this work with similar works. The present work provides direct power conversion from battery compatible voltage range down to 1 V output voltage. The designed converter achieves continuous voltage regulation with competitively high power density and efficiency. Tight regulation is achieved with a simple control method.



(a)



(b)

Figure 3.22: Measured V_{out} waveform with the on-die load steps: (a) I_{load} step down from 900mA to 500mA (b) I_{load} step up from 500mA to 900mA

Table 3.3: Performance Comparison with Prior Works

Work	[28]	[22]	[31]	[30]	[29]		This work
Process	28nm	65nm	0.13um	65nm	0.18um		0.15um
Topology	3:1 SC	3:1, 5:2 SC	3-level Buck	4:1 SC w/ inductive load	2:1 ResSC		3:1 Stacked DAB
Input Range	3.2	3.0-4.0	2.4	3.0-4.5	5-3.7	6	3.2-4.2
Output Range	0.95	1.0	0.4-1.4	0.3-1.0	1.2-2.5	3	0.8-1.5
Flying Capacitor	1.5nF (On-die)	3.88nF (On-die)	18nF (On-die)	3 x 22uF(0402) (Ceramic)	24.6nF (On-die)		6 x 470nF (01005) (Ceramic)
Bypass Capcitor	145pF (On-die)	0	10nF (On-die)	22uF(0402) (Cermiac)	12nF (On-die)		20nF (On-die)
Inductor (per phase)	0	0	1n (On Die)	180nH (Discrete)	5.5nH (Discrete)	1.1nH (PCB Trace)	4.2nH (PCB Trace)
NO. of Phases	6	18	4	1	3		3
Efficiency (Peak)	82%	74.3%	77%	94.2%	85%*	85.6%*	87.2%
PD (W/mm^2)	1.1	0.19	0.2	0.096**	0.22*	0.91	0.46**
Output (@ PD)	0.95V	1.0V	1.25V	0.95V	1.2V	3V	1.2V
Power (@ PD)	0.13W	0.12W	1W	0.96W	1.8W*	7.7W	1.56W
Efficiency (@ PD)	82%	73%	63%	88.3%	72%*	85.1%	83.4%
Load Transient?	Yes	Yes	Yes	NO	NO	NO	Yes
ΔV_{out} /ΔI_{load}	55mV/135mA*	170mV/253mA	120mV/150mA*	N/A	N/A	N/A	50mV/400mA

* Extracted from measurement
** Power density with area of off-chip components included

Chapter 4

Conclusion and Future work

As the modern mobile and portable electronic product calls for a more tightly integrated system, the power management units still remain area-consuming with a large amount of off-chip passive components. The conventional buck converter dominates the commercial market due to its convenient regulation capability. Though the SC converter can enable a fully integrated voltage regulator, the fundamental efficiency and power density trade-off along with lossy regulation limit its application. Various emerging hybrid approaches try to leverage inductive components for maximizing the energy utilization of integrated capacitors and enable lossless voltage regulation. In order to fulfill the demand of tight system integration, the introduced magnetic components should be kept minimal.

The Stack-ResSC topology proposed in this thesis enjoys the benefit of soft charging for all working capacitors with minimum inductance. The stacking feature extends the adaptability of the topology to bridge a high input voltage. A simple gate driver design can be easily derived from the stacked DC domains. Based on the phase-shift operation, lossless regulation can be enabled. An intuitive phasor model can provide a guidance for capturing the large signal behavior. A small signal model based on harmonic averaging method further facilitates the design of a tight analog controller.

As a derivation of Stack-ResSC, Stack-DAB is also introduced in this thesis. They share the similar circuit architecture with the distinction in the inductor current waveform. A Stack-DAB converter can be viewed as a Stack-ResSC converter operating at a much higher frequency than the resonant frequency of the LC tank. The resonant capacitors behave as DC blocking capacitors with negligible voltage ripples. In the presented IC implementation, the Stack-DAB topology is chosen, based on the minimum achievable resistance given the constraint of allowable capacitor footprint. An IC prototype is implemented in TI's 0.15-μm CMOS technology. The AC coupling capacitors are implemented using 01005 ceramic capacitors. The inductors are built from the PCB traces and vias (4.2nH) together with the package bondwires that bridge the coupling capacitors and active die. All power switches and bypass capacitors are integrated on die along with the control blocks and the clock networks.

The converter can operate under an input voltage of 3.2V-4.2V which covers the com-

mon voltage range of a Lithium-Ion battery, and achieves continuous output regulation of 0.8V-1.5V. The operating frequency is used for the output regulation given prescribed load condition. The converter can achieve a peak efficiency of 87.2%, and a power density of 0.46 W/mm^2 with efficiency of 83.4%. A tight loadline regulation is demonstrated with a 50 mV overshoot/undershoot in the presence of 400 mA load step. Compared with the SC based approach, this converter can achieve efficient voltage regulation without topology reconfiguration. Compared with other hybrid topologies, this converter can achieve high conversion ratios while still maintaining high efficiency over a wide operation range.

Further improvement can be applied to the present work. One improvement is to optimize the passive component. Though charge sharing loss is mitigated, the introduced inductors bring in additional conduction loss. This loss is significant especially when the operating frequency is high due to inductor's high AC resistance. Under two-phase interleaved operation, a coupled inductor is a better option for magnetic arrangement.

Another limitation of the developed topology is the bypass capacitor requirement. In a SC converter, there is no physical limitation of the number of interleaved phases. However, the presence of inductor in the Stack-ResSC, though small, still limits the number of phases that can be implemented. This is due to the discrete nature of inductor though it can be realized with a in-package bondwire or PCB trace. Advanced 3D packaging options can potentially alleviate the inductor integration difficulty, such that more phases can be arranged. With the relaxation of bypass capacitance from the increasing number of interleaved phases, the power density can be further improved with reduced die area for bypass capacitance.

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