Expanding the Scalability and Applications of III-V Optoelectronic Devices by Evolution of Thin-Film Vapor-Liquid-Solid Growth

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By

Mark James Hettick

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Committee in charge:

Professor Ali Javey, Chair

Professor Ming C. Wu

Professor Daryl C. Chrzan

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Abstract

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Two significant drivers to innovation in electronics and electronic materials in recent history have been electronic device scaling and the pursuit of high efficiency photovoltaic cells at low costs. The motivations of these two fields have been interestingly parallel, as "density" has been a key metric for both – areal energy density in the case of photovoltaics, and component density in the case of electronic devices. So strong is this motivation to lower device costs by packing more performance into a smaller area that "laws" have been devised to inspire innovation in each field, with Moore's law to describe the periodic doubling of transistor density and Swanson's law to outline the steady drop in solar cell module costs over time. As each law approaches a wall erected by fundamental physical limitations, science must identify roadblocks and solutions that can allow innovation to continue.

Semiconductor materials are a key limiting factor for each application, as their physical properties determine ultimate functionality of a device and the challenges involved in device design. In both electronic and optoelectronic applications, scalable manufacturing of III-V materials has been a promising avenue to improvement, as while they are traditionally expensive to produce, they use a larger portion of the solar spectrum for photovoltaic devices, and are easily utilized in the fabrication of high performance optical and electronic devices. In recent years, a more scalable method for the growth of III-V materials without costly epitaxial substrates has been developed, by utilizing the vapor-liquid-solid growth (VLS) process to grow structures confined by a metal catalyst. Structures such has nanowires have been fabricated with this technique and studied extensively, but a recent expansion of the approach has also allowed for growth of high-quality thin films using planar templates for nucleation control. In this dissertation, I discuss the use of this approach in a number of applications, including the development of large-area photovoltaic devices and an evolution of the technique to greatly expand its application space through lower process temperatures.

First, I will discuss an ideal preliminary application of this technique, with the development of p-body InP photoelectrochemical cells for the direct production of chemical fuel using sunlight. This application shows the utility of large-scale polycrystalline growth with larger than normal grain sizes enabled by the technique, and the fundamentals of the growth process and usable doping methods are explored in tandem. This study also demonstrates the successful application of an efficient selective electron contact to the poly-InP system, enabling promising device performance and enhancing device stability under harsh photocathode operation conditions. Hydrogen fuel production from simulated sunlight is also directly and quantifiably observed from the device as a capstone to this experiment.

Following the investigation of larger area thin-film growth, the microscale templated-liquid-phase (TLP) crystal growth method is explored and expanded to target a wider range of applications. This method, a modification to the thin-film vapor-liquid solid (TF-VLS) process initially studied, has previously enabled growth of defined patterns of single crystal domains on amorphous substrates. While this is an impressive result with great promise for integration of III-Vs into highly scaled electronics, growth temperatures previously explored would need to be lowered significantly for facile integration to be a reality. Using a simple modification to the existing TLP process, I demonstrate growth temperatures well within the silicon CMOS thermal budget, with proof-of-concept devices fabricated at temperatures as low as 270°C with the InP system. With applicability to a variety of substrates, this study has neatly expanded the application space of III-Vs, with complex methods and material requirements replaced with simple direct growth.

To Ashley

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First, I would like to thank Prof. Ali Javey, for his mentorship, training, and support during my studies over the many years I have been part of this group. Since starting as an undergraduate in this lab, I have been able to learn so much about not only the typical experimental skills required of a researcher but also many skills in management and mentorship, which would not have been possible without his trust and guidance.

I would also like to thank my qualifying exam and dissertation committees, including Prof. Ming Wu, Prof. Daryl Chrzan, and Prof. Joel Ager. Their feedback and contributions during and after the exam were very helpful for the shaping of my project, and in particular Prof. Chrzan has provided great insight on the growth process theory and fundamentals integral to my work. Prof. Ager also played a critical role in my studies of photoelectrochemical systems, and was a great mentor as well during my initial years as an undergraduate and junior grad student. Prof. Wu also facilitated a great teaching experience while I served as his head graduate student instructor, and I really appreciate his advice, feedback, and help during the course of that class.

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TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Material limitations in near-future electronics and photovoltaics

Many of the devices we rely on today were based on the innovative driving force of a straightforward observation made more than 50 years ago. Gordon Moore's observation, that integrated circuit component density was continuously doubling every year (Figure 1-1), has encouraged the semiconductor industry to match and exceed this prediction as far as physically possible.[1] While silicon-based devices have been directly scaled to metal half pitches less than 14nm,[2] limitations such as direct source-drain tunneling and metal line breakdown could lead to a stall in planar scaling as early as 2021. To avoid this barrier, there are a number of different strategies for expanding transistor density and performance into the future, including 3D integration[3] methods that seek to increase density by stacking and III-V on silicon processes[4] that seek to increase performance directly by improving the channel material's carrier transport properties. In particular,

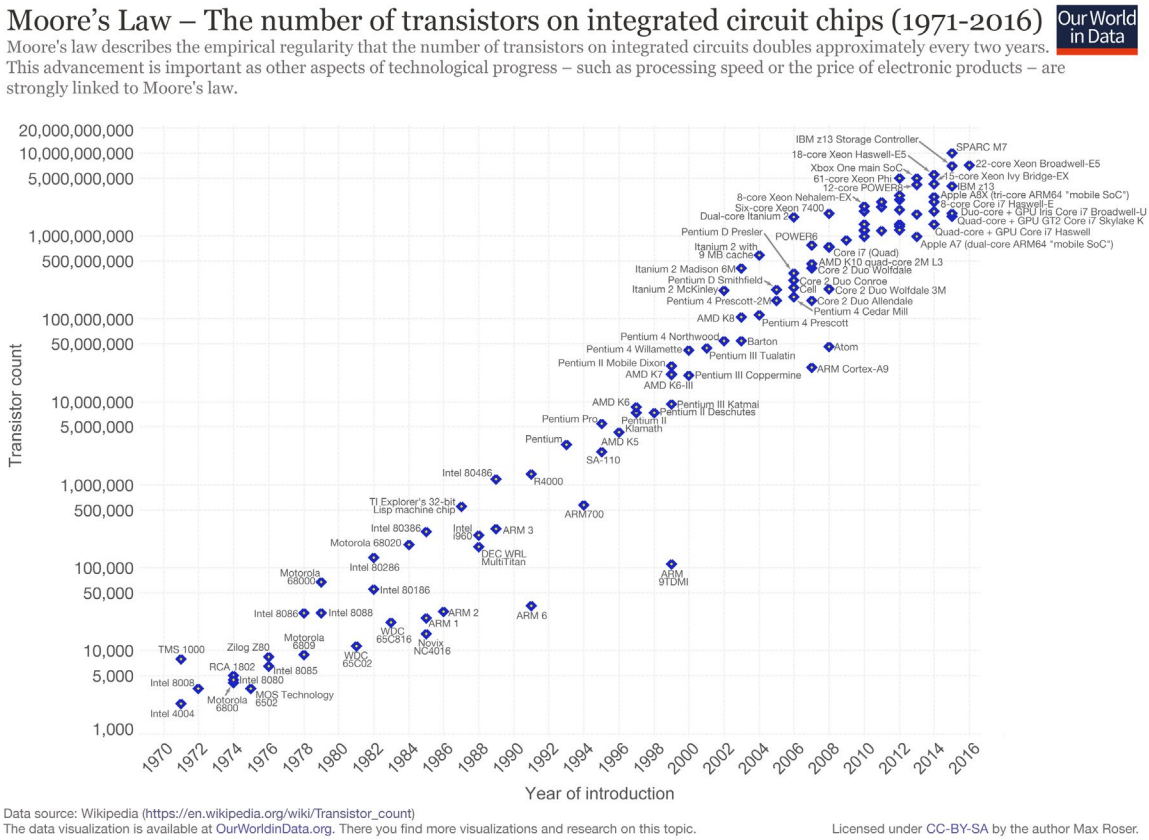

Figure 1-1. Transistor count on integrated circuits from 1970 to 2016.
(Reproduced from plot and data in https://ourworldindata.org/technological-progress)[5]

III-V on silicon processes have additional advantages due to the increasing prevalence of photonic circuit applications.[6] However, the critical roadblock is the co-integration of silicon and III-V materials, which traditionally require complex graded heteroepitaxy or an additional transfer step to realize a III-V active layer.

With inspiration from Moore's law, other industries have targeted similar motivational trends to define a "learning curve" for their respective technological trends. One such trend which has broad impact on the world we live in is the learning curve of photovoltaic (PV) adoption, which emulated Moore's law both in form and in nomenclature. "Swanson's law," which tracks the average module price as more panels are shipped, follows a somewhat more modest 20% per year price decline.[7] This curve (Figure 1-2) illustrates the maturation of photovoltaics, both in terms of business volume and the implicit improvement of cell efficiency, which has also been increasing steadily over time as a result of such competitive trends. However, similarly to Moore's law, cost pressures and increasing module efficiencies have pushed manufacturers to more complex designs and manufacturing methods,[8] and silicon solar cells are rapidly approaching the Schockley-Quiesser limit in practical device configurations.[9] Because of this, many researchers and some companies have been looking to alternative materials systems for photovoltaics, including the ideally positioned III-V materials as alternatives and tandem candidates. However, similar impediments to progress exist for broad adoption due to strict cost constraints in PV markets that have made epitaxial strategies undesirable.

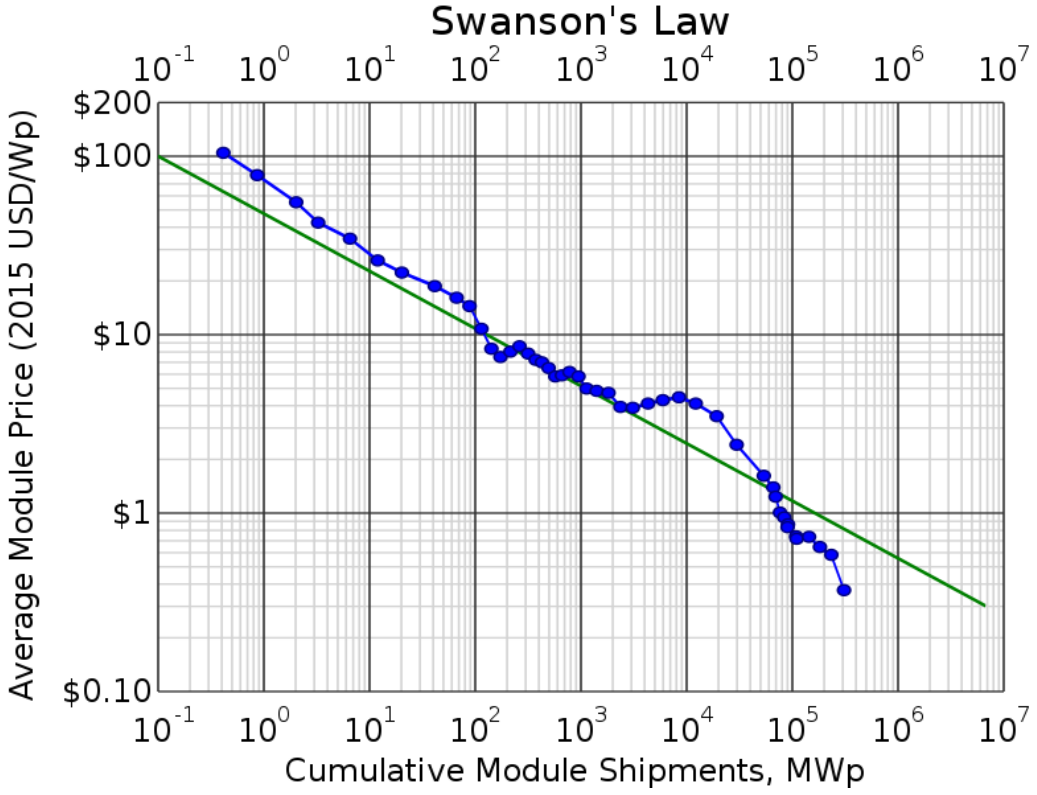

Figure 1-2. Illustration of Swanson's law as module prices have dropped to near grid parity, to ~2015. (Reproduced from https://en.wikipedia.org/wiki/Swanson%27s_law, Data from ITRPV Edition 2017 Presentation.)[8]

1.2 III-V materials: Optical and electronic applications

With integration issues in mind, we can look to a few additional properties and applications of III-V materials to motivate a solution and explain some of the specific physical challenges we face. Figure 1-3 displays a map of material gap vs. lattice constant for a variety of compound semiconductors, with tie lines to indicate bandgap modification with ternary compositions. This plot neatly explains both the advantages and disadvantages of III-Vs, as their ternary compounds have a wide tunable range of emission and absorption energies but require epitaxial substrates and processes to accommodate lattice differences. An example of this conundrum is the case of tandem solar cells, by which efficiencies above the single junction limit can be achieved using multiple absorbers to target the various parts of the solar spectrum. For silicon solar cells, an evolution of the limiting efficiency could be achieved with an ideally matched gap such as the 1.8 eV InGaP composition shown, but the lack of a scalable integration method between these materials has allowed only mechanical stacking methods to realize this combination.[10]

On-chip silicon photonics are another area of great interest in the pursuit of III-V on silicon integration. Near-IR semiconductors are prevalent in the III-V family as shown, but the silicon lattice constant of 5.43Å is difficult to match to these materials. Structures have been demonstrated with hybrid Si/III-V designs allowing wavelength tuning of on-chip lasers in the InP system,[5] but a multi-step process involving traditional epitaxial growth followed by wafer bonding is needed due to the lack of a direct integration method.

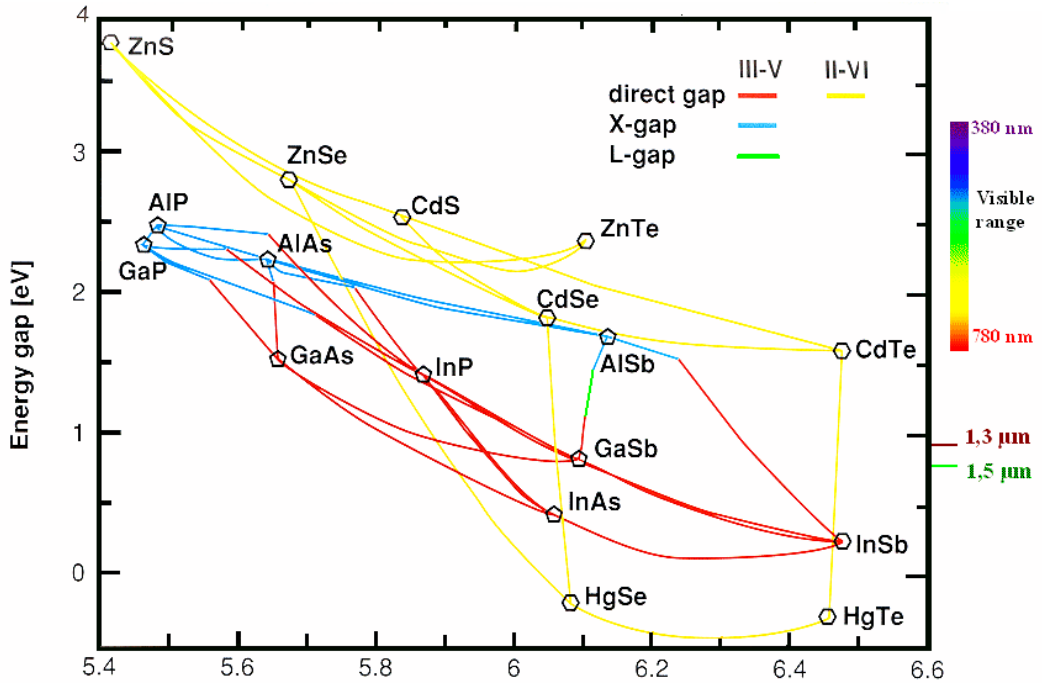

Figure 1-3. Energy gap of various III-V and II-VI semiconductors vs. lattice constant, with tie lines for bandgap of ternary compositions. (Reproduced from https://www.tf.uni-kiel.de/matwis/amat/semitech_en/kap_2/backbone/r2_3_1.html, Data from Tien 1988, Bell Laboratories.)

Finally, in the silicon complementary metal-oxide-semiconductor (CMOS) applications space, III-V materials have significant advantages in both planar and 3D cointegration. Due to their high mobilities[4] and the advent of photonic circuit applications[11] that would directly utilize on-chip optoelectronic devices, this is yet another area where simplified integration methods would be a key for future progress. One example is the integration of InAs transistors on silicon by layer transfer,[12] where field-effect mobilities in excess of 4000 cm^2/V-s were realized. Direct growth of GaAs on Si has also been explored in the past,[13] but initial naïve approaches of direct metal-organic chemical-vapor-deposition (MOCVD) were limited by high pre-treatment and deposition process temperatures.

1.3 State of the art in III-V growth for heterogeneous integration

Significant effort has been placed on bonded devices for III-V on silicon photonics due to ease of stacking and component mating,[11] but many direct growth techniques have also been explored for accommodating the lattice mismatch between silicon and III-V materials to achieve metamorphic epitaxy. In metamorphic epitaxy, dislocations generated as lattice mismatches are accommodated and gradually graded away, and the initial dislocations are left behind well outside of the active device area.[14] In Figure 1-4, a graded buffer layer for a solar cell application is demonstrated, showing the possible path of dislocations in the schematic and in the transmission electron micrograph (TEM) of the real structure.

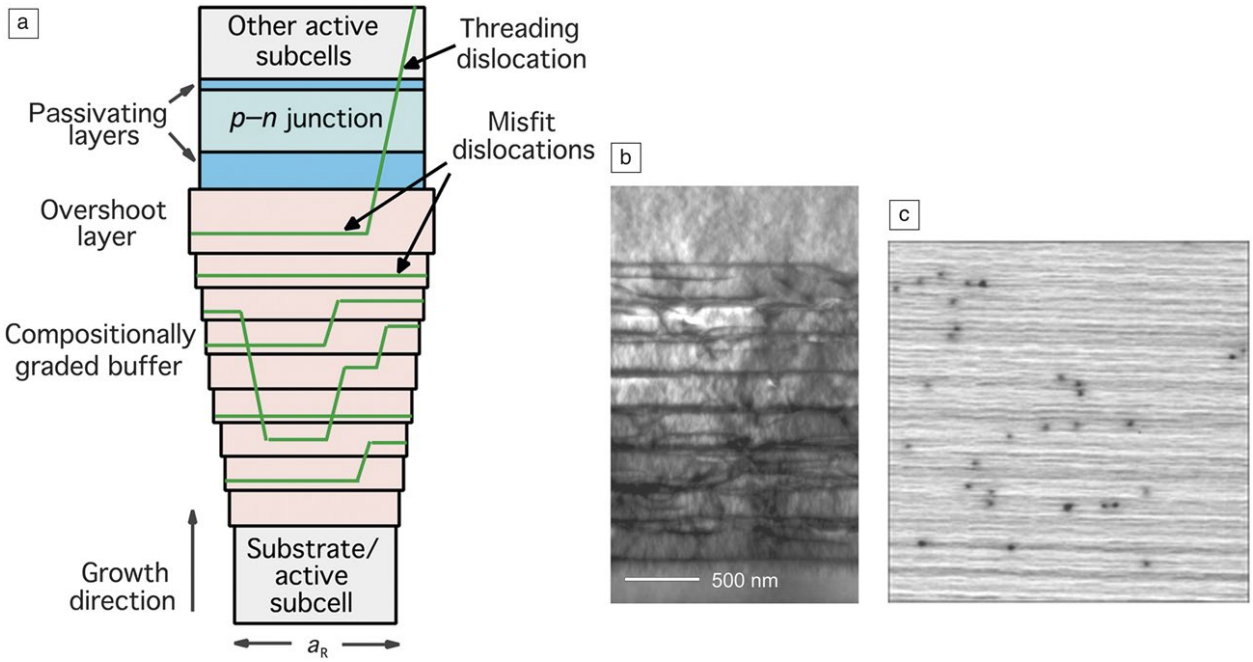

Figure 1-4. A graded buffer layer in schematic and TEM form displaying the accommodation of a $Ga_{0.7}In_{0.3}As$ cell onto a nonepitaxial subcell substrate. (Reproduced from France et al. 2016,[14] Figure 3)

While graded buffers are an adequate strategy, they are necessarily wasteful, as many microns of growth can be necessary due to the relative ease of defect propagation.

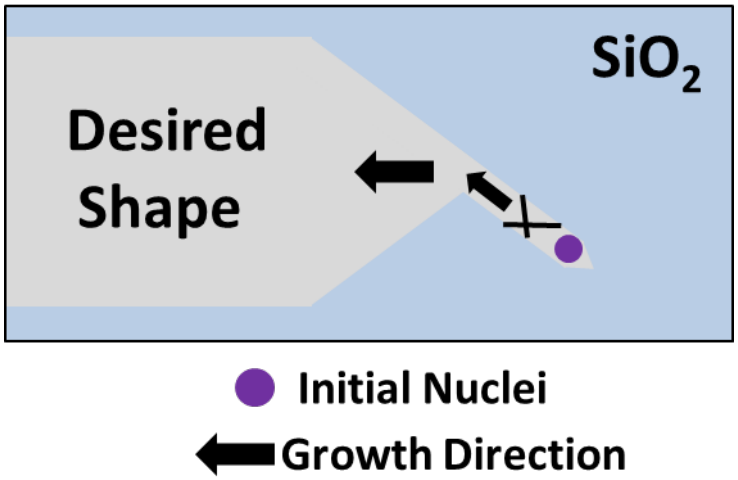

Figure 1-5. Schematic of aspect ratio trapping with a typical unseeded Bridgman ampoule-like design. Defect lines within the tip are cut off at the tip edges before leaving to affect the desired shape.

Aspect ratio trapping, similar to classical applications of unseeded Bridgman growth,[15] allows for circuitous dislocation lines to terminate at an edge within a defined pattern (Figure 1-5), greatly decreasing the distance over which a defect can propagate and cause problems in an active structure.[16] Through characterization of defect spacing and careful trapping structure design, traditional methods such as MOCVD can generate high quality structures within these templates, but due to high dislocation densities at typical process temperatures lateral dimensions can still be limited, and access to the base substrate is still needed. Epitaxial layer overgrowth[17] and rapid melt growth[18,19] have shown some success in high quality thin films with a similar base template idea, though neither are universally applicable, and the latter method results in some material degradation due to a decline in stoichiometry over the course of the process.

1.4 Thin-Film Vapor-Liquid-Solid (TF-VLS) Growth Techniques: Our approach

Due to the significant void in viable thin-film processes for direct III-V growth for integration into promising applications, the advent of a scalable method with reduced complexity would open up a new space for rapid innovation. In recent years, one such technique has emerged, with inspiration from the popular vapor-liquid-solid nanowire growth method. Vapor-liquid-solid nanowire growth processes utilize precipitation of precursors dissolved from the vapor phase into a liquid catalyst to grow wires in a nanoscale template defined by the catalyst area, and can be used to grow a wide variety of group IV and III-V semiconductors.[20] By modification to the template portion of this technique, the thin-film vapor-liquid solid method allows both large scale and locally defined thin-film growth by using liquid metals confined by oxide “capping” layers, with a patternable nucleation promoter to encourage preferential growth in specific substrate areas.[21,22] Importantly, the control of precursor flux through the same confinement layer also allows for fine control of nucleation density, leading to large grain sizes in thin films compared to the target film thickness (Figure 1-6).

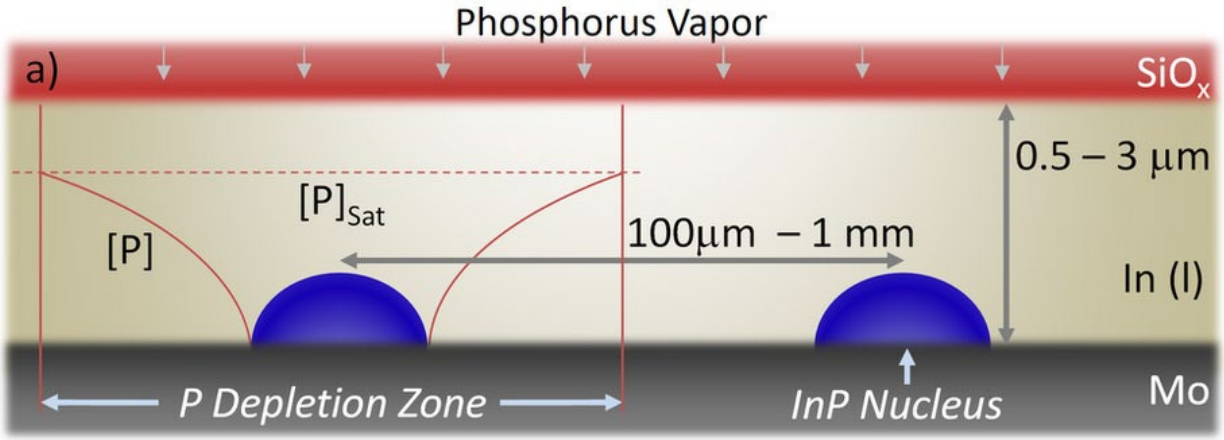

Figure 1-6. Schematic representation of the TF-VLS growth mode, displaying control of nucleation density by phosphorus depletion zones that form around each nucleus. (Reproduced from Kapadia et al. 2013[21])

The mechanism for nucleation control offered by this method is visualized in Figure 1-6 for the InP system. As it forms, each nucleus reduces the local phosphorus concentration as it accumulates more for growth, and in some area around the nucleus the diffusion gradient reduces the phosphorus concentration below the supersaturation concentration that is required for another nucleus to form.

This mechanism was carried even further in the development of templated liquid phase (TLP) growth, where only one nucleus is allowed to form in a feature by virtue of its defined nucleation and precursor area.[23] In this method, single crystal domains of III-V materials have been grown on amorphous substrates by simple nucleation layer and metal precursor patterning. In this way, the III-V process void for both large area and microscale electronic and optoelectronic applications can be filled, but further development and adaptation of the technique to specific applications is needed to pinpoint its utility in each space.

With this motivation in mind, in the rest of this report I seek to carry the reader through two unique applications and evolutions of the TF-VLS process. Chapter 2 will first show the direct application of TF-VLS growth to efficient non-epitaxial photocathode cells fabricated by scalable methods. Chapter 3 will then present a development of the technique that widely expands its application space, allowing us to conclude with a bright vision of the future of III-V applications without epitaxial substrates.

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CHAPTER 2

SCALABLE INP PHOTOCATHODES BY TF-VLS GROWTH

2.1 III-V photovoltaics and photocathodes: Introduction

In the realm of clean energy, photovoltaic devices are king, due to the large amount of mostly unharnessed energy density[1] in sunlight that could easily provide abundant free energy reserves to the world. In particular among photovoltaic devices, though silicon dominates the filed due to continuously dropping cell and module costs, III-V compound semiconductors are among the most promising candidates for future solar cells because of their primarily direct band gaps with a wide range of tunable energies. The high quality and tunability of this materials system has allowed III-V cells to consistently hold both the single- and multi-junction efficiency records (Figure 2i), in both thin-film and bulk crystal forms. However, the aforementioned difficulties with III-V process and material integration have inhibited widespread adoption of these technologies, as the highest efficiency devices displayed all rely on complex multijunction growth and strategies to lower costs of epitaxial substrates. As a result, the TF-VLS process is uniquely suited to address this problem, as in the large area format any suitable material from the chart could be chosen to design a more scalable thin-film III-V PV structure, enabling higher limiting efficiencies in future cells and a continued downward trend in PV energy costs.

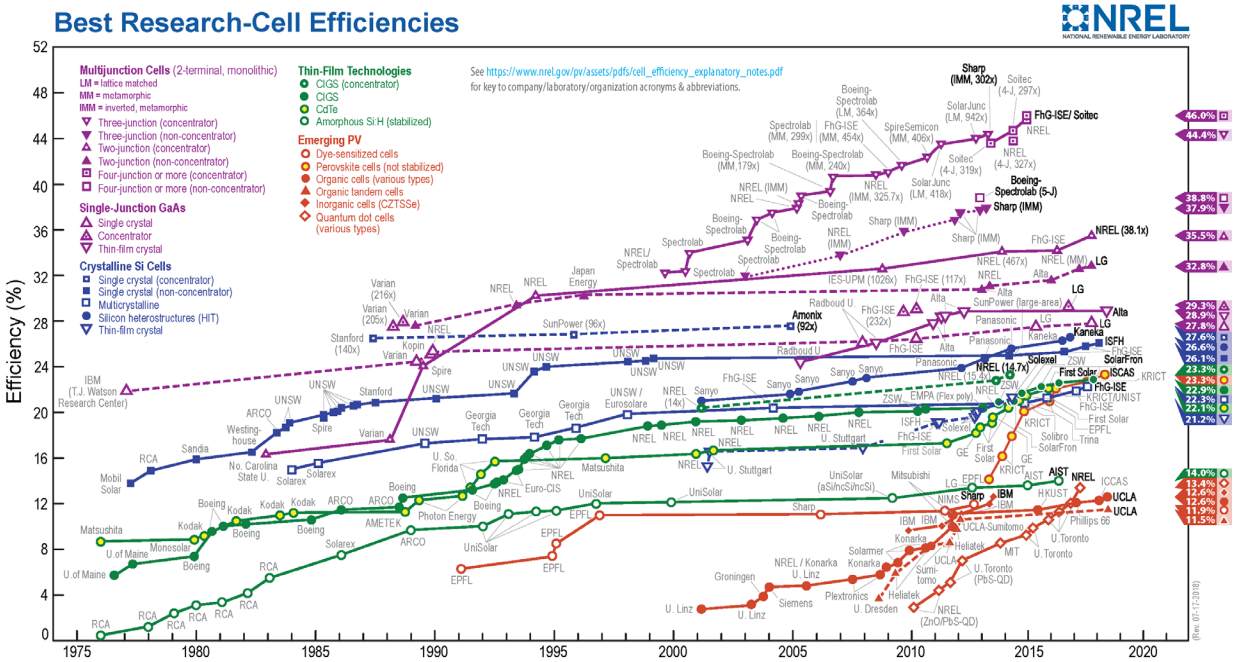

Figure 2i. Research cell efficiency chart from the National Renewable Energy Laboratory (NREL), additional explanatory notes at https://www.nrel.gov/pv/assets/pdfs/cell_efficiency_explanatory_notes.pdf.

Among PV applications, the generation of storable fuel from sunlight in the manner of photosynthesis is a particularly promising solution to the clean energy problem, and the prospect of highly efficient photoelectrochemical (PEC) cells is an attractive route to generation of solar fuels[1,2,3]. Due to the 1.23 eV free energy required for the water splitting process, in addition to the overpotentials generated at each electrode under operation, work on the tandem cell architecture with a particular focus on producing high voltage half cells is desirable to meet this requirement while maintaining adequate absorption across the solar spectrum.[4] For the H_2 producing photocathode half-cell, a variety of semiconductors have been explored, including planar,[5,6,7] micro-[8], and nano-structured[9] crystalline Si, amorphous Si,[10] InP,[11-17] WSe_2[18], TiO_2 coated Cu_2O,[19,20] and CdS-modified *p*-$CuGaSe_2$.[21]

In particular, *p*-type InP stands out for its direct bandgap of ~1.35 eV, suitable conduction band position in relation to the proton reduction potential, and associated high efficiency for the hydrogen evolution reaction.[12-16] In fact, nanostructured crystalline InP wafers have achieved a half-cell solar-to-hydrogen (STH) efficiency of approximately 14%,[12] which is the highest reported to date. In addition, other work on TiO_2 passivated crystalline InP wafers resulted in half-cells with an onset potential greater than 800 mV, providing some of the high voltage necessary for unassisted water splitting in the ideal tandem cell configuration.[13] Still, despite its high efficiency, prior work on InP as a PEC photocathode material has primarily focused on single crystal wafers, which limits large-scale application due to the high cost of the bulk substrates. In this work we explore a more practical approach, utilizing a new high quality thin-film InP growth method[22] on low-cost Mo substrates along with previously explored protection schemes[7,10,12,13] to establish a low-cost and high efficiency PEC system. The system, the first solar device structure implemented using the TF-VLS growth method, exhibits decreased overall material usage, high performance, and potential expansion to device structures requiring fine nucleation and growth control.[22,23] Material and device quality is evaluated using imaging, photoluminescence (PL), and Mott-Schottky capacitance-voltage measurements, and performance of our photocathodes is evaluated through current voltage (J-V) measurements, to be compared with previous photocathode reports.

2.2 Growth, p-doping, and device structure of TF-VLS InP photocathodes

A full process scheme for our photocathodes is visualized in Figure 2-1. The TF-VLS growth method is chosen as it produces films with high optical and crystal quality with theoretical performance approaching that of the bulk crystal in terms of the luminescence efficiency and optically implied open-circuit voltage.[22] Briefly, the TF-VLS growth method begins with an indium film approximately 2 micron in thickness deposited on a molybdenum substrate, capped by a thin silicon oxide (SiO_x) layer (details in Methods). This stack is heated in hydrogen past the film's melting point, followed by the introduction of PH_3 gas for phosphorization of the liquid indium by a vapor-liquid-solid growth mode. Importantly, the SiO_x layer confines the indium during growth to a planar thin-film geometry, allowing growth to proceed only in the lateral direction and reducing loss of the metal source to evaporation. The resulting InP is poly-crystalline with a thickness of 2 to 3 μm (determined by the evaporated indium thin film thickness) and a lateral grain size of up to 1 mm.[22,23] This ultra-large grain size produces high optoelectronic performance as demonstrated previously.[22]

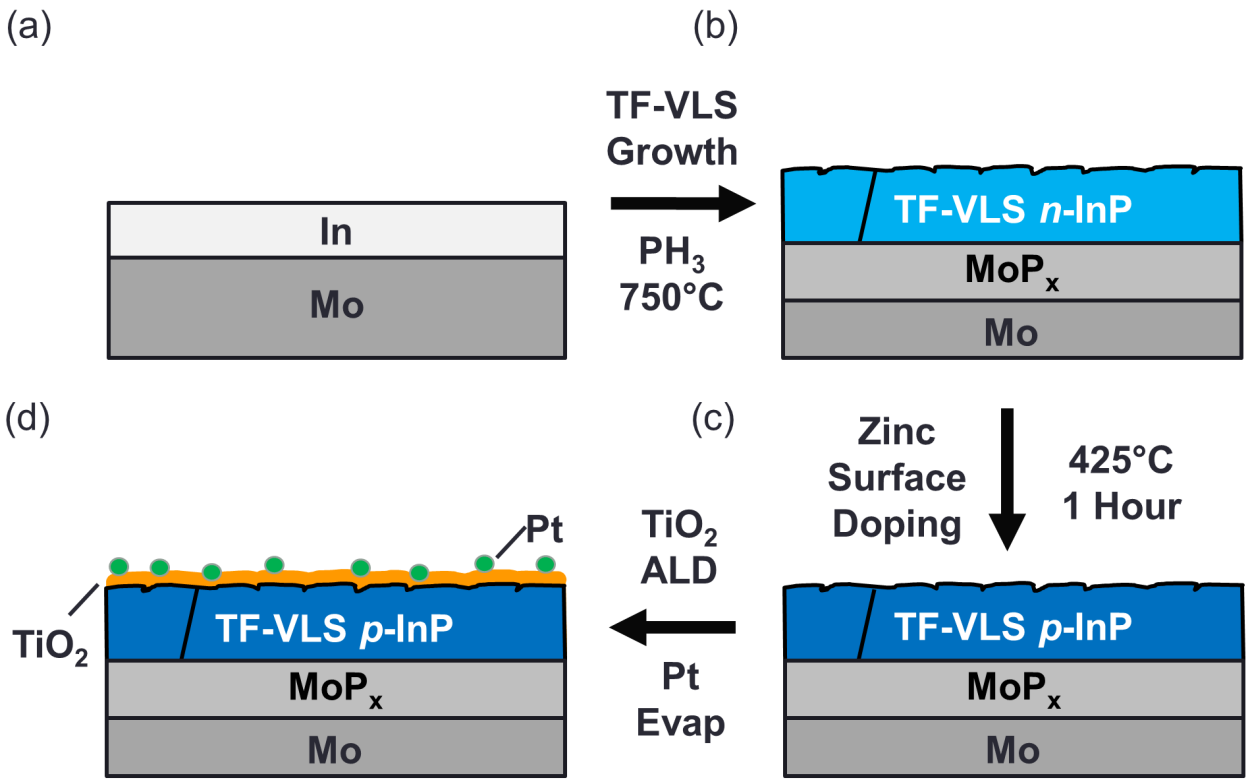

Figure 2-1. The fabrication process for TF-VLS InP PEC devices. (a) Indium metal is evaporated on the substrate using an electron beam evaporator. (b) An *n*-type (unintentionally doped) polycrystalline InP film is grown on the Mo substrate through a TF-VLS process. (c) The *n*-type film is *p*-doped by surface diffusion using a Zn_3P_2 solid source. (d) A TiO_2 protection layer is grown by ALD on the top surface of the InP and a Pt co-catalyst is evaporated onto the surface of the TiO_2 to finish the device fabrication.

To produce *p*-type InP for use as a photocathode, an *ex-situ* surface diffusion doping process was carried out at a sample temperature of 425°C using zinc phosphide (Zn_3P_2) as the precursor (see Methods for details). Zn was chosen as the dopant since it is a commonly used acceptor in InP with a low activation energy.[24] Notably, the Zn_3P_2 source was chosen to prevent InP decomposition by providing a phosphorus ambient present during the doping period. A 30 nm thick *n*-TiO_2 protection layer was then deposited by ALD at 120 °C to protect the surface from corrosion during PEC measurements.[12] Our previous studies[13,25] have shown that this *n*-TiO_2 layer on InP also provides a favorable surface energy band bending, allowing for transport of electrons while reflecting the holes due to the large barrier height at the InP/TiO_2 interface. Thus, higher V_{OC} was observed previously for TiO_2 coated InP PV and PEC devices.[13,25] The temperature of TiO_2 deposition was optimized for device performance, as pictured in the J-V comparison shown in Figure 2-S1. Finally, Pt was used as an efficient catalyst material for water reduction. Throughout, growth and processing choices were influenced not only by the goal of cost reduction but also by stability and efficiency.

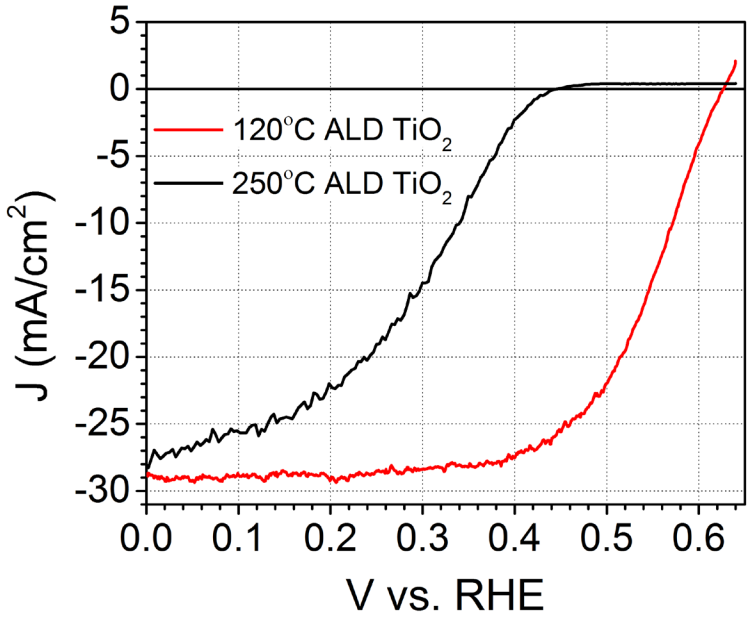

Figure 2-S1. J-V performance of TF-VLS InP PEC devices, comparing the performance for TiO_2 ALD deposition temperatures of 120°C and 250°C under AM1.5 illumination. J-V test performed in 1M $HClO_4$.

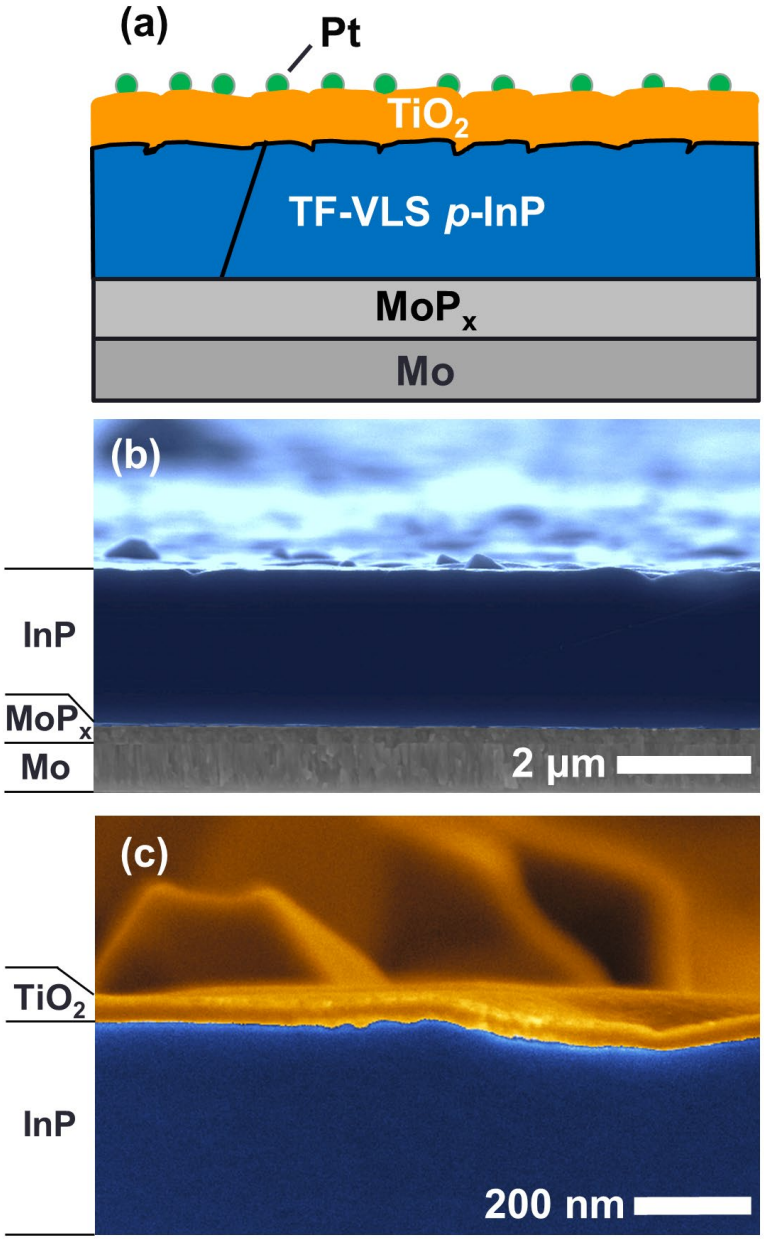

Figure 2-2. (a) Schematic of the typical device stack. (b) False-colored cross-section SEM image of the as-grown InP film. (c) High magnification SEM image (false-colored) of the TiO_2-InP interface after TiO_2 deposition by ALD.

Morphological characterization of completed photocathodes is given by SEM images of a representative cross section in Figures 2-2b-c. Note that as reported in our previous studies, each grain extends vertically from the Mo substrate to the top-surface with a surface roughness defined primarily by the confinement of indium metal under the SiO_2 cap, as demonstrated by the limited protrusions extending above large, high quality grains shown in Figure 2-2b.[22] The 30 nm thick, highly uniform and conformal TiO_2 layer depicted is designed to not only improve the protective qualities over the TF-VLS InP, but also to act as an anti-reflective coating, improving the solar-weighted reflectance of the stack as compared to thinner coatings (Figure 2-S2). This structural and electrically

functional anti-reflection coating is particularly important in a PEC cell since conventional multilayer anti-reflective coatings may not be possible due to the intimate semiconductor-solution contact necessary for charge transfer. It has also been shown previously that TiO_2 thickness does not significantly impact charge transfer through the film, so this design choice does not impact the electrical performance of our devices.[10,25] Further optimization of the reflectance properties is possible with thicker TiO_2 films, and sputtering of TiO_2 as a protection layer and electron contact has been explored and implemented at much greater thicknesses in other photocathode systems.[10] In the future, the electronic benefits and chemical stability shown in ALD TiO_2 films could be combined with the increased throughput and lower cost of sputtering processes to yield optimal electronic, chemical passivation, and optical properties for photocathode cells.

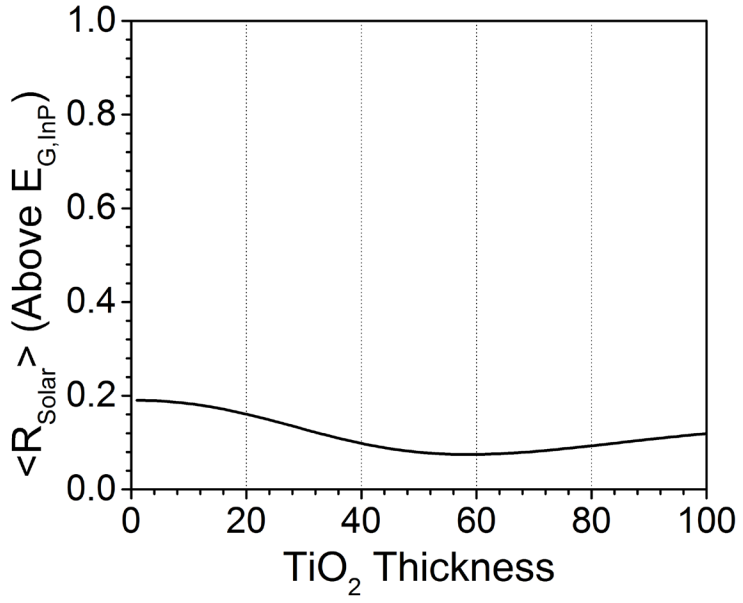

Figure 2-S2. Calculated average solar reflectance above the InP bandgap as a function of TiO_2 thickness, defined as the weighted average of reflectance with the normalized AM1.5 solar spectrum as a weighting parameter.

2.3 Structural and optoelectronic characterization of TF-VLS InP films

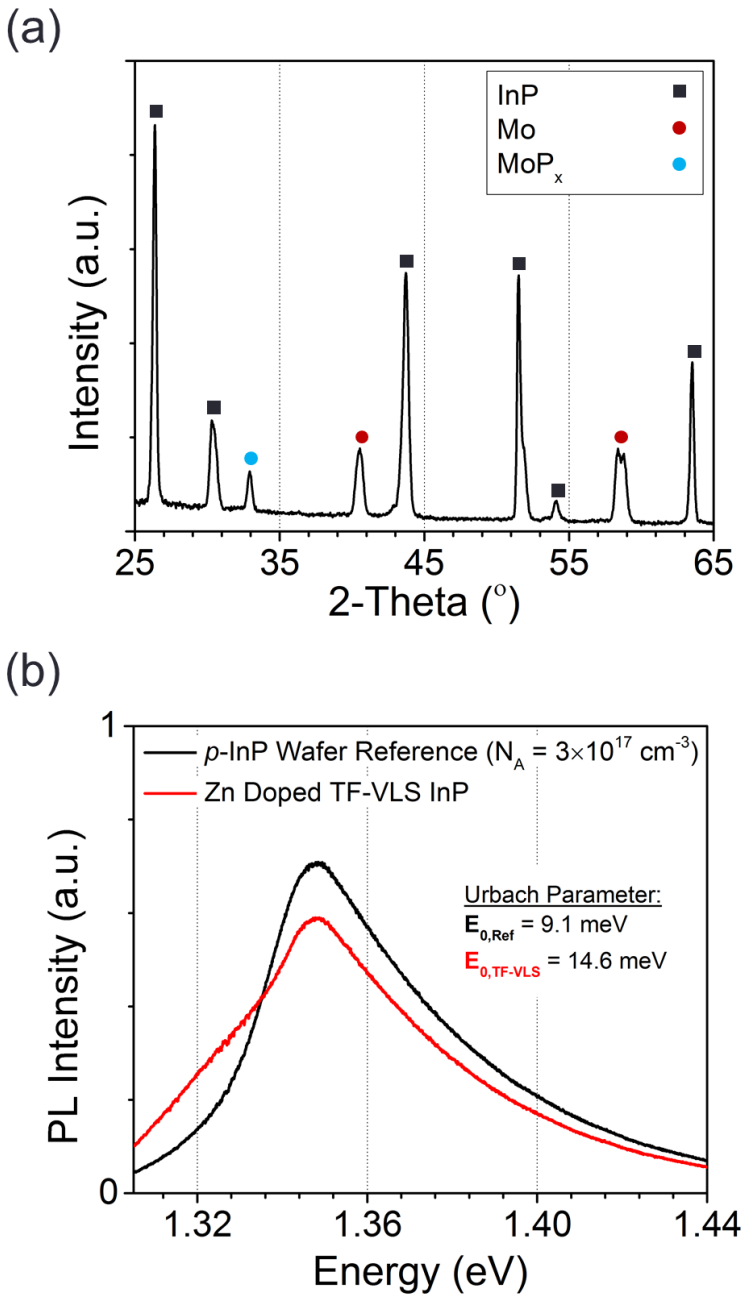

Figure 2-3. Physical and optical characterization of as-grown TF-VLS InP material and processed devices. (a) X-ray diffraction data of as-grown material, indicating high crystallinity with narrow peaks closely matching a zinc blende powder reference. Peaks attributed to the growth substrate are also visible, here denoted as Mo and $Mo_{1-x}P_x$ ($0.5 < x < 0.8$) according to a powder reference. (b) Steady-state micro-PL measurements, indicating similarity of intensity and shape to a *p*-type crystalline reference. Extracted Urbach tail parameter E_0 fitted from extracted absorbance (Experimental and T, Figure 2-S3) is also reported for both the single crystalline wafer reference and our *p*-type TF-VLS film.

The intrinsic optoelectronic and structural qualities of the material used in these PEC cells are also quite important, and these parameters were explored by steady state micro-photoluminescence (PL) and X-ray diffraction (XRD) measurements (Figure 2-3). XRD measurements (Figure 2-3a) indicate a high level of crystallinity of as-grown films, with peak positions closely matching a zincblende powder reference,[29] and with other peaks attributed to the MoP_x/Mo substrate.[30,31] As in our previous reports, a preferred (111) texture is observed for growth on Mo. In addition, while Mo is the most prominent feature of the substrate, MoP_x peaks are also visible in XRD (with $0.5 < x < 0.8$), demonstrating that there is some phosphorization of the Mo substrate during the growth process as shown in previous explorations of InP growth.[22,26,27] While not directly explored in this work, this modification of the Mo contact layer could have some impact on the device performance.

Steady state, room temperature PL data for Zn-doped TF-VLS InP show peak positions, intensity, and full-width half maxima close to those of a crystalline *p*-InP reference with similar doping concentration (Figure 2-3b), with only a low energy shoulder distinguishing the TF-VLS InP in this PL comparison. Particularly notable is the similarity in PL intensity and integrated counts, as this indicates our material approaches a similar luminescence yield and optically implied open circuit voltage (V_{OC}) to the crystalline reference.[22] The difference in peak shape can be attributed to the non-epitaxial growth and effects from the zinc doping process, a feature previously observed in impurity studies for InP and attributed to both the Zn impurity level and LO phonon coupling with the Zn impurity.[28]

To further characterize our material, we perform a fit of the Urbach tail using the Roosbroeck-Shockley[32] equation to extract a relative absorption parameter from our steady-state PL data. From a logarithm fit to the Urbach formula for band tail absorption (1) we can extract the Urbach parameter E_o, which is a measure of band edge sharpness that can be correlated to disorder in a semiconductor. Details of this extraction can be found in the Experimental and Theoretical Methods and in Figure 2-S3. Comparing the single-crystal *p*-type wafer reference and our *p*-type TF-VLS film with a similar doping concentration, we see similar E_o values of 9.1 meV and 14.6 meV respectively, indicating band edge sharpness in our TF-VLS material in line with the single crystal wafer. In summary, the PL data show that our TF-VLS material is of high optical quality for implementation in a device, and that the growth and doping methods used here represent a promising route to poly-crystalline thin-film material approaching equal performance to previously explored bulk single-crystals.

$$\left(\alpha(E) = \alpha_0 e^{\left(\frac{E-E_{ref}}{E_0}\right)}\right) \qquad (1)$$

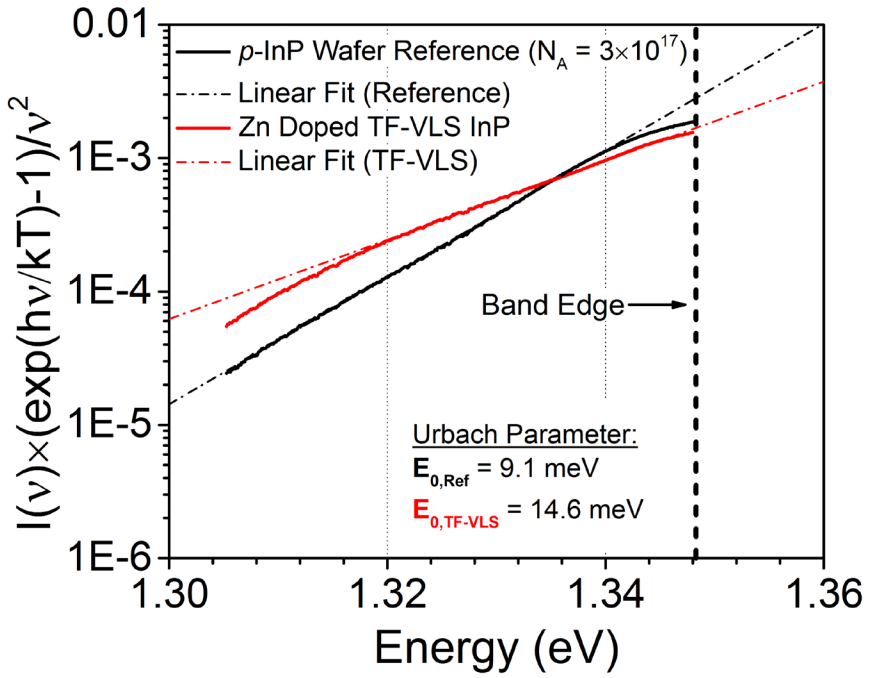

Figure 2-S3. Extracted absorption tails near the InP band edge, extracted using the Roosbroeck-Schockley equation for the Zn doped *p*-type TF-VLS InP and a *p*-type wafer reference of similar doping concentration. Urbach parameter, representing the sharpness of the band edge according to the exponential decay constant of the band tail, is extracted from the linear fits to the log plot.

2.4 Electronic characterization of poly-InP photocathode devices

Given the high optical and crystalline quality of our thin-film InP on Mo, we then sought characterization of the electronic properties and photoelectrochemical performance of the complete photocathode cell. Before measuring our device in the final configuration, we first aimed to understand the doping and solution-semiconductor electronic interface properties by performing Mott-Schottky capacitance-voltage measurements both without and with the protective TiO_2 window layer (Figure 2-4a,b). Without the TiO_2 layer, we can first measure the bare InP surface in order to extract doping concentration and flatband potential (V_{FB}) of the InP-solution interface. The measured doping concentration of our material following the aforementioned doping process is $1.9 \times 10^{17} cm^{-3}$, a concentration in line with single crystal wafers used in record photocathode cells.[12] The V_{FB} extracted in this measurement is 0.81 V vs. RHE, a value ~0.55 eV less than the InP band gap. As the

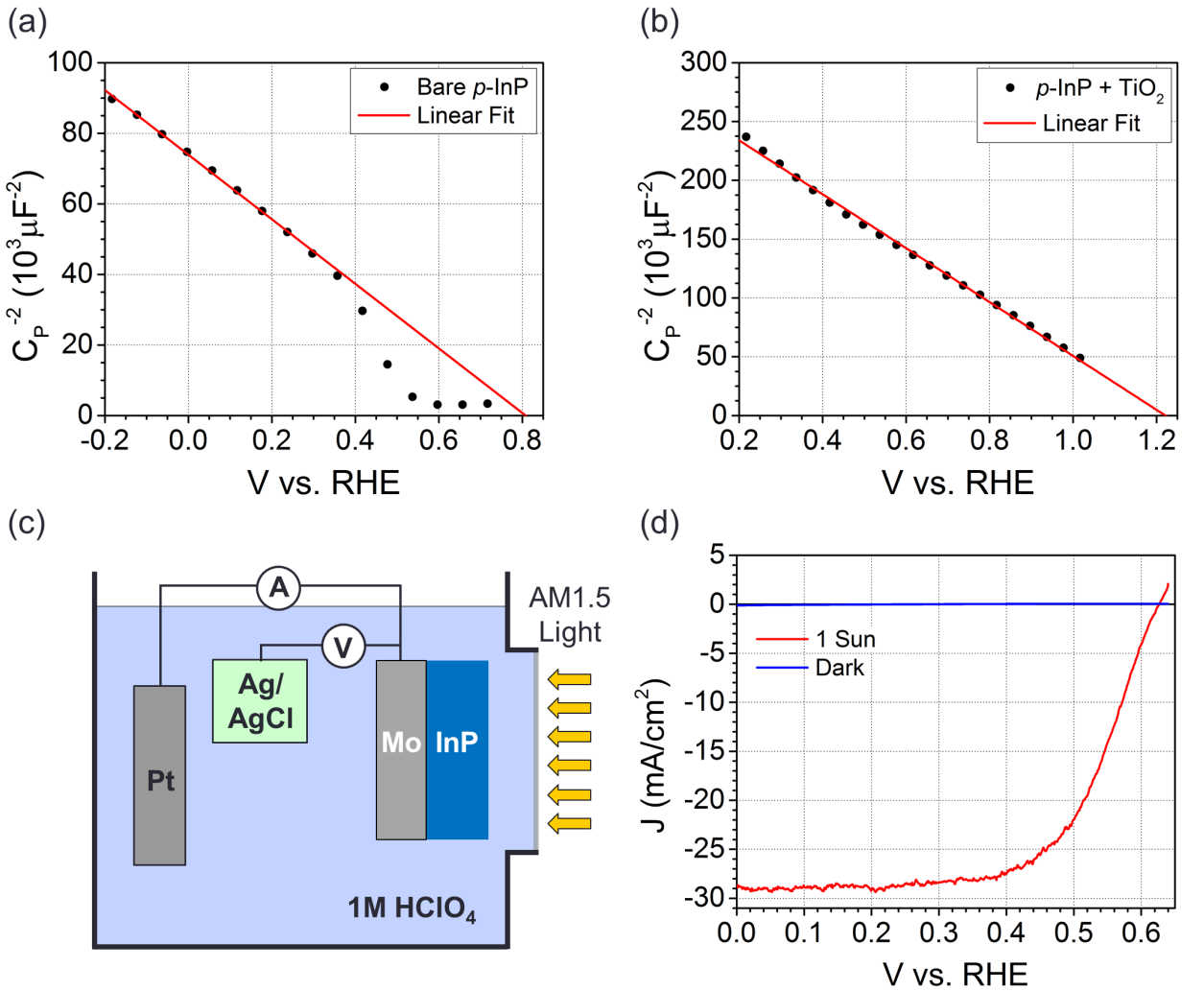

Figure 2-4. Mott-Schottky analysis and PEC performance of TF-VLS InP photocathodes with a 30 nm TiO_2 protection layer and Pt co-catalyst. (a,b) Mott-Schottky plot for *p*-doped TF-VLS, before (a) and after (b) TiO_2 deposition in a pH 7 buffer. Linear fits are included for extraction of flatband potential and doping concentration. (d) J-V performance of a TF-VLS InP PEC device under AM1.5 illumination. J-V test performed in 1M $HClO_4$ with the cell depicted in (c).

InP conduction band is close to the H_2O/H_2 redox potential at pH 0 according to previous reports,[12,13] we would expect *n*-type surface inversion of the *p*-InP material at the liquid junction, a condition that would require a value of V_{FB} near the band gap to flatten the InP bands. The value of V_{FB} is thus a reflection of the surface band position prior to applying a potential, as the built-in potential is applied to return the surface to the bulk band position. The lower value of V_{FB} despite an effective metal work function (Φ_m) position near the InP conduction band edge suggests reduced sensitivity of the built-in potential to Φ_m, a condition reflective of Fermi level pinning at the direct solution-InP interface. A similar result has been observed in previous explorations of the *p*-InP liquid junction (Figure 2-4a).[33,34] Ideally, while the deposition of a TiO_2 protective layer should primarily serve to allow electrode operation in strong acid solutions, the semiconductor heterojunction quality should also be maintained or improved following this process if it is a practical solution for high efficiency cells, since any degradation of the interface would lead to a direct reduction of obtainable V_{OC}.[34] Measuring the flatband potential by the same method (Figure 2-4b), a measurement enabled due to rapid depletion of the thin TiO_2 layer under reverse bias, we see that the V_{FB} of the InP/TiO_2-solution interface shifts positively to 1.22 V. This positive shift implies that indeed the TiO_2 deposition improves the InP junction, as the proximity of V_{FB}, and thus built-in potential, to the band gap energy places the redox potential far from the valence band, a condition that maximizes possible photovoltage in a solar device.[34] As discussed in prior work on InP-TiO_2 p-n heterojunctions, we have created a thin-film cell with a high built-in potential, as well as a large barrier to minority holes that prevents interface recombination and supports charge separation.[13,25] Therefore, the application of our TiO_2 heterojunction contact provides both a chemically inert surface and an ideal structure for a high efficiency cathode cell.

Finally, TF-VLS InP photocathode device performance was evaluated directly on the basis of J-V measurements in 1M $HClO_4$ (Figure 2-4d). Light and dark J-V sweeps were measured with a three-electrode configuration depicted in Figure 2-4c, under a simulated AM1.5 spectrum at 100 mW/cm^2, showing a short-circuit current density (J_{SC}) of 29.4 mA/cm^2 and a photocurrent onset of approximately 630 mV vs. RHE, with no significant features in the dark J-V curve that would suggest unwanted electrochemical side-reactions. Moreover, this performance level is consistent across multiple devices fabricated under these conditions, with a mean V_{OC} of 609 mV and mean J_{SC} of 27.4 mA/cm^2. More detailed device statistics are available in Figure 2-S4. Comparing device performance, single crystalline bulk wafers have a J_{SC} of 25.5 mA/cm^2 and a photocurrent onset potential of approximately 810 mV vs. RHE.[12] The lower V_{OC} for the TF-VLS InP compared to single crystal wafers, despite the comparable high photoluminescence yields both as-grown[22] and after doping (Figure 2-3) is attributed to a non-ideal back contact and remaining observable crystal defects such as twin boundaries and grain boundaries. For the back contact, the effects of the MoP_x present below the InP are not known, and previous reports suggest that a Zn-based metal alloy is necessary for ohmic contact to *p*-type InP. Therefore, further optimization in the doping process or growth substrate may improve photocathode performance.[35,36] To this end, contact improvement strategies such as film transfer and alternate nucleation and contact layers for film growth are being pursued,[22,23] so significant improvement in overall photocathode performance using TF-VLS InP is certainly possible.

Number of Devices: 12	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)
Mean	0.609	27.4	49.3	8.330
Standard Deviation	0.0237	2.510	9.07	2.001
Max	0.639	30.0	63.0	11.595
Champion	0.626	29.4	63.0	11.595

Figure 2-S4. Device statistics for the final set of conditions presented in the text, including mean, max, and standard deviation for each major performance parameter. 12 devices were successfully fabricated and tested in this set.

2.5 Poly-InP Solar Fuel Production: Conclusions and Outlook

Nevertheless, the performance obtained here is still quite remarkable, with comparable voltage and improved efficiency compared to most non-III-V cathode technologies (Table 2-1). As the water-splitting PEC system requires large overpotentials beyond a minimum of 1.23 V for normal operation, the ultimate achievable voltage of a material is of utmost importance to its viability. When compared to single crystal systems, the TF-VLS InP photocathode is favorable over silicon and WSe_2 in voltage, and possesses one of the highest short-circuit current densities of all reported photocathodes with a competitive fill factor of 63%. In addition, we have measured sustained photocurrent and 100% Faradaic efficiency for H_2 over more than two hours, suggesting that our device structure is stable against corrosion during testing (Figure 2-S5, S6). Along with efficiency closely approaching that of crystalline InP wafer devices, the TF-VLS InP photocathode is poised as a promising future choice in high efficiency PEC systems.

In this work, we have demonstrated a stable, efficient photocathode device utilizing a low-cost, scalable fabrication technique that avoids expensive epitaxial growth processes and maintains high voltages and efficiencies necessary for viable operation of the water splitting PEC system. The devices presented in this work are the first demonstrated using this growth method, a technique that decreases usage of precious feedstock materials in high efficiency III-V systems. While the existing performance is promising, the implied potential from this growth method, on the basis of measurements of the material's intrinsic quality, suggests that much more can be done to bring the system and structures explored in this work up to and beyond the crystalline wafers. To this end, the TF-VLS growth method will be a valuable tool for production of higher efficiency photocathodes, with precisely controlled nucleation and mm-scale grain sizes as the ultimate limit in highly scalable thin-film PEC technology.

System: absorber/catalyst	E_G (eV)	V_{OC} (V vs. RHE)	$\|J_{SC}\|$ (mA/cm^2)	η (%)
Si Microwire[a]	1.1	0.54	15	5.8
Planar Si[a]	1.1	0.56	28	9.6
Microtextured Si[c]	1.1	574	31.8	10.6
Amorphous Si[b]	1.7	0.93	11.6	6
WSe_2 Crystal[d]	1.2	0.63	24.5	7.2
Cu_2O/MoS_{2+x}[e]	2.2	0.45	5.7	0.85
CuGaSe/CdS[f]	1.68	0.65	8.7	0.83
InP Wafer Nanopillars[g]	1.35	0.73	37	14
InP Wafer/(Rh, H sat.)[h]	1.35	0.64	28.6	13.3
InP Wafer/TiO_2[i]	1.35	0.81	25.5	12.2
This Work (TF-VLS InP/TiO_2)	1.35	0.63	29.4	11.6

Table 2-1. Tabulated half-cell STH efficiencies, V_{OC}, and J_{SC} of reported photocathode devices.

[a]Ref. 8; [b]Ref 10; [c]Ref 38; [d]Ref 18; [e]Ref 37; [f]Ref 21; [g]Ref 12; [h]Ref 39, 81.7 mW/cm^2 illumination; [i]Ref 13

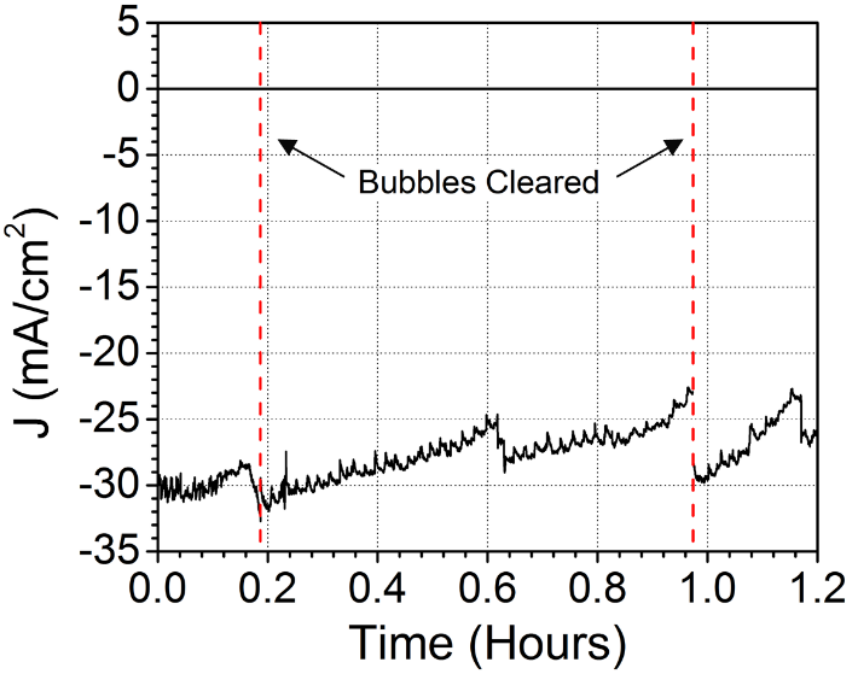

Figure 2-S5. Stability demonstration of TF-VLS InP photocathodes in 1M HClO4. Bubble clearing events, where measurements are paused to remove bubbles from electrode, are marked by dotted lines.

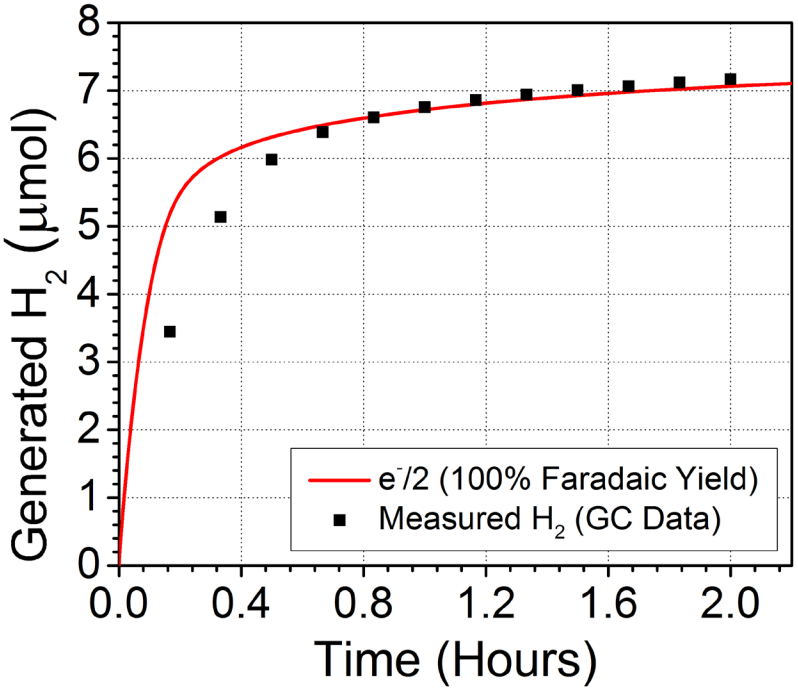

Figure 2-S6. Stability demonstration of TF-VLS InP photocathode in 0.1M H2SO4, with H_2 gas production measured by a gas chromatograph. H_2 generation calculated by 1-to-1 conversion of passed current is shown as a solid line. Data for this measurement is collected following the measurement in Figure 2-S5, but from the same device.

2.6 Experimental and Theoretical Methods

A. Fabrication Process.

InP materials used in this work were grown using a recently developed Thin-Film Vapor-Liquid-Solid (TF-VLS) growth method.[22] Molybdenum foil substrates were degreased in acetone and isopropanol, followed by a hydrochloric acid etch and a deionized (DI) water rinse and nitrogen blow dry. The cleaned substrates were then loaded immediately into an electron beam evaporator, and 2 μm of 99.9999% pure indium metal was deposited on the foils, followed by a 40 nm SiO_2 capping layer. After this, the coated substrates were placed in a tube furnace, where they were phosphorized according to a previously described method utilizing 10% PH_3 in H_2 as the phosphorus source.[22] The typical growth process involves heating the substrates to 750 °C in H_2 ambient, followed by a 20 minute phosphorization step in 10 sccm of 10% PH_3. This process yields an *n*-type InP layer approximately 3 μm in thickness, after etching of the SiO_2 capping layer in 49% HF. As we wish to extract minority electrons for the reduction of protons in solution, this *n*-type as-grown material must then be doped *p*-type. For this process, a closed-space sublimation system was used, with the TF-VLS InP placed on a 2 mm quartz spacer above Zn_3P_2 (99.999%) powder used as the Zn acceptor source. The powder and substrate, held in thermal contact to graphite blocks, are heated separately by quartz lamps at 520 °C and 425 °C respectively, for a total doping time of one hour. The acceptor doping concentration in the InP layer using this method is approximately 10^{17} cm^{-3} as extracted by Mott-Schottky analysis. The doped samples were cleaned in five cycles of an acid treatment, utilizing 1% HCl, 1% HNO_3, and DI water in succession to remove surface layers that may have been damaged during the doping step. The InP films were then coated with a 30 nm thick layer of titanium oxide (TiO_2) by an atomic layer deposition (ALD) process using titanium tetraisopropoxide and water, and a deposition temperature of 120 °C. Finally, to enhance catalytic activity at the solution interface, a thin layer of platinum (thickness of approximately 1 nm) co-catalyst was deposited by electron beam evaporation.

B. Physical Characterization.

Scanning electron microscope (SEM) images were taken using a Zeiss Gemini Ultra-55. X-ray diffraction (XRD) data were taken using a Bruker AXS D8 Discover GADDS XRD Diffractometer system. Steady state micro photoluminescence (PL) data were taken using a 633 nm HeNe laser and the detector was a silicon CCD.

C. Photoelectrochemical (PEC) Characterization.

PEC devices were characterized using a BioLogic SP-300 bipotentiostat in a three-electrode, quartz-windowed cell with a BASi RE5B Ag/AgCl Reference electrode, platinum wire counter electrode, and TF-VLS InP as the working electrode. 1M $HClO_4$ was used as the electrolyte for J-V experiments, and a pH 7 buffer solution was used for Mott-Schottky measurements. The illumination source for J-V characterization, stability, and H_2 generation measurements was a Solar Light 16S-300-005 solar simulator with

AM1.5 filter. The light intensity of 100 mW/cm^2 was adjusted and calibrated using a Solar Light PMA-2100 radiometer and a PMA-2144 pyranometer, verified using a crystalline InP electrode IPCE calibrated against a NIST traceable photodiode (71648) from Newport. H_2 generation data were measured using an Agilent 490 Micro Gas Chromatograph (GC), with N_2 carrier gas and a 0.1M H_2SO_4 electrolyte to avoid corrosion of internal GC components.

D. Average Solar Reflectance Calculation.

Average solar reflectance above $E_{G,InP}$ is defined by a weighted average of the spectral reflectance $R_S(\lambda)$ weighted by the AM1.5G solar spectrum $E(\lambda)$.

$$< R_{Solar} \geq = \frac{\sum_\lambda R_S(\lambda) \times E(\lambda) \times \Delta\lambda}{\sum_\lambda E(\lambda) \times \Delta\lambda}$$

The spectral reflectance R_S in this calculation was determined by the following equations for a one layer anti-reflection coating of varying thickness t_{AR}, with the three interface refractive indices for water, TiO_2, and InP taken at the InP band edge of 1.35 eV. These values are 1.3280, 2.496, and 3.395 respectively.

$$r1 = \frac{n_0 - n_1}{n_0 + n_1}$$

$$r2 = \frac{n_1 - n_2}{n_1 + n_2}$$

$$\theta = \frac{2\pi n_1 t_{AR}}{\lambda}$$

$$R = |r^2| \frac{r_1^2 + r_2^2 + 2r_1 r_2 cos2\theta}{1 + r_1^2 r_2^2 + 2r_1 r_2 cos2\theta}$$

E. Extraction of absorption and Urbach Tail Parameter by the Roosbroeck - Shockley Relation

By the Roosbroeck-Schockley equation, emission rate can be directly related to absorption by an exponential relationship. The inverse of this relationship has been used[32] to extract the absorption coefficient from the photoluminescence emission of III-V materials. Here we utilize the same method to extract a relative absorption parameter:

$$\alpha(h\nu) \sim I(h\nu) \times (e^{\frac{h\nu}{kT}} - 1)/(h\nu^2)$$

As the Urbach energy parameter, defined as the exponential decay factor E_0 in the Urbach tail equation below can be extracted as the inverse *slope* of the log of this absorption parameter, the absolute emission intensity is not required in this process. Therefore, in this case we extract the Urbach parameter directly from the slope of our relative PL intensity near the band edge as in figure 2-S3, converting the $\log_{10}$ slope to the exponential factor.

$$\alpha(h\nu) = \alpha_0 e^{(\frac{E-E_{ref}}{E_0})}$$

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CHAPTER 3

DIRECT TEMPLATED LIQUID PHASE GROWTH OF HIGH QUALITY INP BELOW 300°C

3.1 Heterogeneous III-V integration: Introduction

While photovoltaic devices have broad applicability to environmentally motivated applications, another thrust of scientific innovation with significant impact to our lives has been the continuous increase in the power and efficiency of electronic and optoelectronic devices. Computers work every day to make our lives simpler and solve important problems for the world, and their power has been continuously rising over the years thanks to constant innovation in silicon device structures and processing. However, to sustain the meteoric rise in computing power that has been the result of continuous size scaling of silicon-based circuit elements over the past five decades, 3D integration must be pursued as nanometer-scale devices approach both electronic and atomic limits. In addition, significant advances in optoelectronics have not only expanded the scope of electronic circuit paradigms but also the power and efficiency of light emitting devices (LEDs) such as the III-V based white LEDs used in a variety of industries today. All of this has the additional benefit of enabling new low-power devices with high energy efficiency while maintaining high device performance.

Still, while certain applications have been able to leverage III-V materials such as GaN (LEDs) and InP (on-chip lasers)[1] to great benefit, most techniques still require clever but complex process modifications such as advanced bonding techniques for silicon and III-Vs to coexist. In this chapter, we take the TF-VLS process explored thus far and use the templated liquid phase (TLP) process modification to target microscale device structures with the goal of expanding process integration opportunities on a variety of substrates. With this, we hope to again demonstrate the scalability of this approach, indicating the possibility of future growth in III-V optoelectronics utilizing the TF-VLS method.

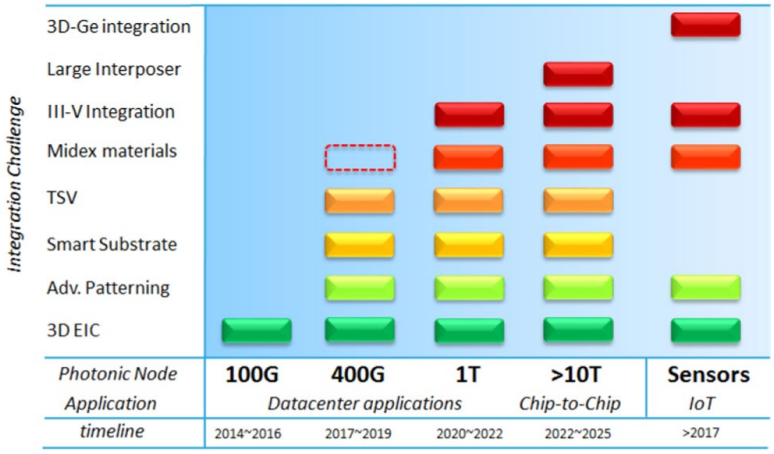

Figure 3i. Process integration roadmap for silicon photonic systems on a chip. (Fig. 11 top panel, Thomson et al. 2016)[1]

3.2 Low-T Templated Liquid Phase Crystal Growth of InP below 300°C

Three-dimensional integration of microelectronic circuits, where additional devices are placed above prior layers in the overall structure, is a promising method for increasing device density in electronics as size scaling approaches physical limits.[2] Particularly, Monolithic 3D integration, by which subsequent layers and interconnects are directly fabricated on the same chip, offers the best path to improvement due to reduction in complexity and similarity to existing "bottom up" fabrication schemes.[3,4,5,6] However, while III-V nanowire and 2D material transfer processes[3,5] have been demonstrated in monolithic structures, direct growth of high-performance electronic materials such as III-Vs has been limited primarily by high typical process temperatures[7,8] given the low temperature tolerance of materials such as interlayer metals and metal nitrides.[9] Recently, a new method has been developed that allows for direct growth of III-V thin films on amorphous substrates, using the vapor-liquid-solid (VLS) process with thin-film templates (TF-VLS) to grow single crystal domains in defined patterns.[10, 11, 12] In this work, we extend this templated liquid phase (TLP) crystal growth method by utilizing a thermal gradient to lower sample process temperatures, enabling InP growth at temperatures below 300 °C while maintaining material quality at the micron scale due to single crystal domain size thresholds identified for each temperature range. Importantly, with process temperatures below the silicon complementary metal-oxide-semiconductor (CMOS) integration threshold of 400 °C, promising electronic performance is demonstrated, with measured Hall mobilities μ_H > 800 cm²/V-s and with transistor effective mobility μ_{Eff} over 600 cm²/V-s. With light emitting devices also demonstrated at temperatures below 300 °C and proof-of-concept growths on plastic and indium-tin-oxide (ITO) glass substrates, this evolution of the TLP process has greatly expanded the application space of III-V materials.

The first benefit of this method is its simplicity, as indicated in the growth process schematic in Figure 3-1a. A standard tube furnace is used for the reaction, with PH_3 diluted by H_2 at a controlled pressure. In this case, as with some MBE systems, a key step is the separation of source cracking from substrate heating, so the gaseous PH_3 source can be converted into useful P_2 and P_4 reactants.[13] As phosphine cracking is inefficient below 500 °C,[14] and as phosphorus condensation can also be a concern, both a cracking zone and a temperature gradient to the substrate are needed to enable low temperature TLP (LT-TLP) growth. In this case, a calibrated gradient in a typical tube furnace was used with a center temperature of 550 °C to ensure adequate PH_3 cracking and accurate substrate temperature (Details in Experimental Methods, Supplementary Data Figure S1). Otherwise, the process is similar to previous descriptions of TF-VLS and TLP growth, where patterned nucleation layers and confining SiO_x caps lead to localized VLS growth of crystalline thin films. Optical images of sample patterns in Figure 3-1b demonstrate Si/SiO_2, ITO glass, and polyimide substrates in sequential panels, grown at temperatures of 370 °C, 270 °C, and 270 °C respectively. Critically, at these growth temperatures there is no strong impact to the properties of each substrate, such as the ITO resistivity and transparency and polyimide flexibility. While 270 °C is the lowest temperature explored for devices in this paper, nucleation and growth also occurs at temperatures as low as 180 °C (Figure S2), demonstrating the enabling power of this method for many applications.

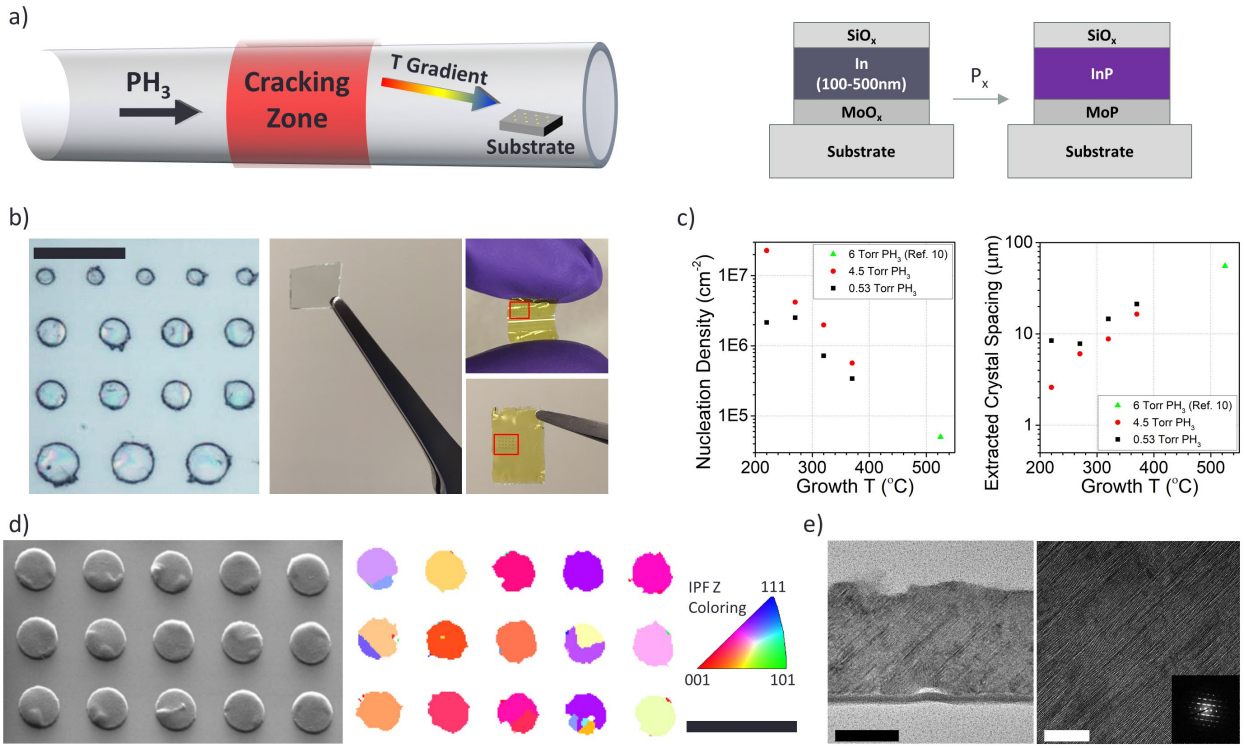

Figure 3-1. (a) General low temperature TLP process, with thermal gradient for T reduction, and typical substrate schematic. (b) Images of grown patterns on Si/SiO_2, ITO, and peeled polyimide from left to right, with contacts defined on the polyimide. Scale bar 15 μm for optical microscope image of Si/SiO_2 substrate. (c) Nucleation density vs. growth temperature for varied PH_3 concentration. (d) SEM image with EBSD map for 3 μm circles grown at 270°C, scale bar 8 μm. (e) TEM/HRTEM characterization at 270°C growth temperature, with SAED inset in the HRTEM image. TEM and HRTEM scale bars 50 nm and 10nm respectively.

3.3 Nucleation and growth behavior of Low-T TLP InP

As growth temperatures are lowered, it is critical to identify the nucleation behavior at these lower substrate temperatures to define a useful target condition for a given process or application. To this end, partial growths on indium strips with full area MoO_x layers are completed at a range of temperatures from 180 to 370 °C, and a plot of extracted nucleation density as a function of growth temperature for different PH_3 partial pressures is shown in Figure 3-1c. Assuming a hexagonal packing geometry, an estimate of domain spacing can also be extracted from the nucleation density data, with a range of approximately 8 to 21 μm spacing for 220 to 370 °C at the lowest PH_3 partial pressure presented. This projected feature spacing compares favorably to the reference point of 55 μm at a 550 °C, and the clear exponential relationship between projected feature size and growth temperature over the entire range can be easily explained by the previously developed model of nucleation density for TF-VLS growth (Details in Ref. 11, Supplementary Note 1):

$$N_{Total} = \frac{A}{h^2}\left(\frac{Fh^4}{D}\right)^{\alpha} \qquad (1)$$

In this case, the parameters of interest are the flux of phosphorus (F) and the diffusivity of phosphorus in indium (D). The exponential increase in nucleation density with decreasing T, as well as the weak dependence of nucleation density on cap thickness (Figure S3), suggests that the decreasing diffusivity of phosphorus due to an Arrhenius relationship is the dominant factor in nucleation behavior.

The projected domain spacing data in Figure 3-1c also show that despite increasing nucleation density, process conditions can be controlled to enable variation in the single-domain threshold temperature. Assuming nucleation behavior extends from MoO_x films to MoO_x patterns, nucleation density data predicts an approximately 8 μm threshold size for single crystal domains at 270 °C. In Figure 3-1d, a set of crystals is shown in a representative scanning electron microscope (SEM) image for a 270 °C growth condition, with a corresponding twin-corrected electron back scatter diffraction (EBSD) map (Details and additional images in Supplementary Data Figure S4). The majority of the 3 μm features in this image contain a single crystal domain, and while single domain features quickly become less common for ≥5 μm features at this growth temperature, the EBSD data largely agrees with the nucleation density extraction when accounting for the purely geometrical estimation. Transmission electron microscope (TEM) characterization further confirms the crystalline nature of films grown using this condition, with HRTEM and selected area electron diffraction (SAED) images displaying uniform twin orientation across the exposed crystal face (Figure 3-1e). Similar twin behavior is also observed as expected for higher growth temperatures, with similar manifestation of stacking faults and only minor rotational differences likely from sample variation. (Supplementary Data Figure S5, S6)

3.4 Optoelectronic Characterization of Low-T TLP InP

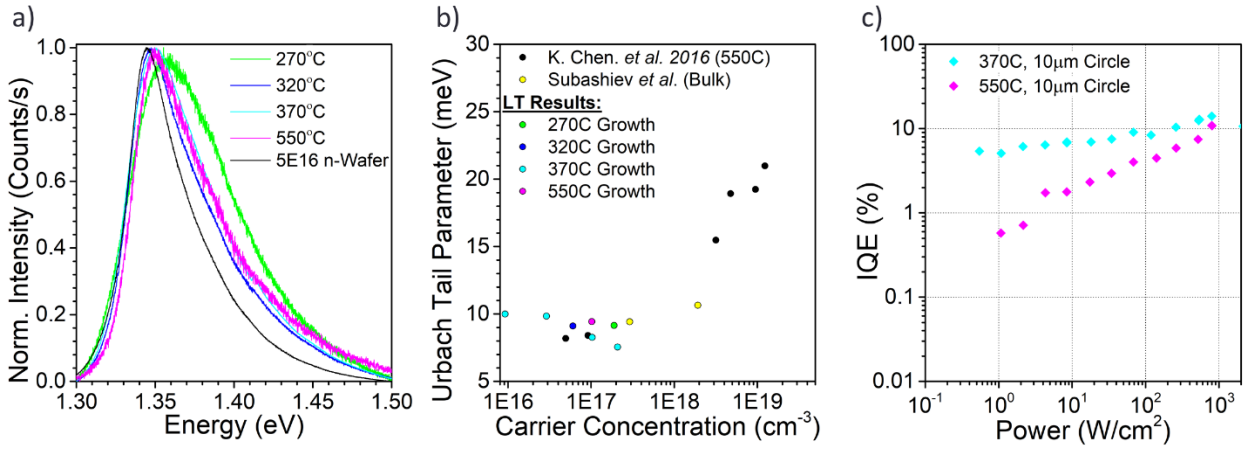

Figure 3-2. Photoluminescence characterization of LT-TLP material at various temperatures. (a) Normalized steady state PL spectra at different growth temperatures, compared to an n-type wafer reference. (b) Extracted Urbach tail parameter vs. extracted carrier concentration at different growth temperatures. (c) A comparison of internal quantum efficiency between 550 and 370°C growth temperatures.

Given the apparent extendibility of crystal domain control to lower temperatures, the material's overall optical and electronic quality should also be assessed to prove viability for real applications. In Figure 3-2, the basic optoelectronic quality of locally defined crystals grown at various temperatures below 400 °C is first explored.
In Figure 3-2a, normalized photoluminescence (PL) spectra from TLP crystals are plotted for growth temperatures from 270 °C to 370 °C. Though all are broader than the bulk wafer reference, the shape and peak positions of the PL spectra are largely unchanged until below 300 °C. At the 270 °C growth temperature, the full-width half-max (FWHM) of the spectrum increases from ~58 meV to ~74 meV and the peak position shifts from ~1.35 eV to ~1.359 eV, indicating some defect influence when compared to growths above 300 °C. The Urbach tail parameter, a common optical measure of band-edge sharpness and disorder in crystalline materials,[15,16] can also be extracted from absorbance converted from the steady state PL spectra (Figure 3-2b, Details in Methods). It should be noted that the carrier concentration for each measurement in this plot is estimated from the Burstein-Moss peak shift above a reference gap energy, in this case taken from the moderately doped wafer plotted in Figure 3-2a. For all lower growth temperatures, despite any changes in spectrum broadness or intensity, the Urbach tail parameter remains very similar to values extracted from 550 °C and bulk references.[10,17] A comparison of PL internal quantum efficiency (IQE) extracted from measured external quantum efficiency (Figure 3-2c, Supplementary Data Figure S8) shows similar emission performance between 550 °C and 370 °C growth temperatures, indicating limited impact to radiative efficiency. As in previous work,[11] extracted quasi-Fermi level splitting is still above 900 meV for the 370 °C growth temperature at approximately 1 sun illumination, including a slight decrease in ideality factor from the "optical I-V" measurement (Supplementary Data Figure S7). Overall, optoelectronic measurements show that material grown across all temperatures 270 °C and upwards should be appropriate for light emitting devices and other optoelectronic applications.

3.5 Transient electroluminescence from InP grown below 300°C

As a proof-of-concept optoelectronic application, we have utilized the LT-TLP growth method to fabricate light emitting devices, using the transient electroluminescent (t-EL) device structure recently demonstrated for a number of 2D materials[18] and an InP growth temperature of 270 °C. A schematic representation of the structure is given in Figure 3-3a, for a Si/SiO_2 substrate with an insulating Al_2O_3 nucleation layer and a Ti/Au contact which is typically grounded under normal operation. To operate a t-EL device, a high frequency square wave is applied across the capacitor structure shown, with carriers injected by a large voltage drop and subsequent tunneling current at the contact during each voltage transition (More detailed discussion in the Supplementary Materials). This transient carrier injection can be visualized by the time-resolved electroluminescence (TREL) spectrum in Figure 3-3c, with emission transients closely following the rising and falling edges of the 20V V_{pp}, 2MHz gate bias square wave plotted above for reference. The emission transients display similar asymmetry to previous t-EL devices, with larger intensity on the rising edges of each pulse indicating a somewhat larger Schottky barrier to holes in this case. However, as the peak half widths are also asymmetrical (at

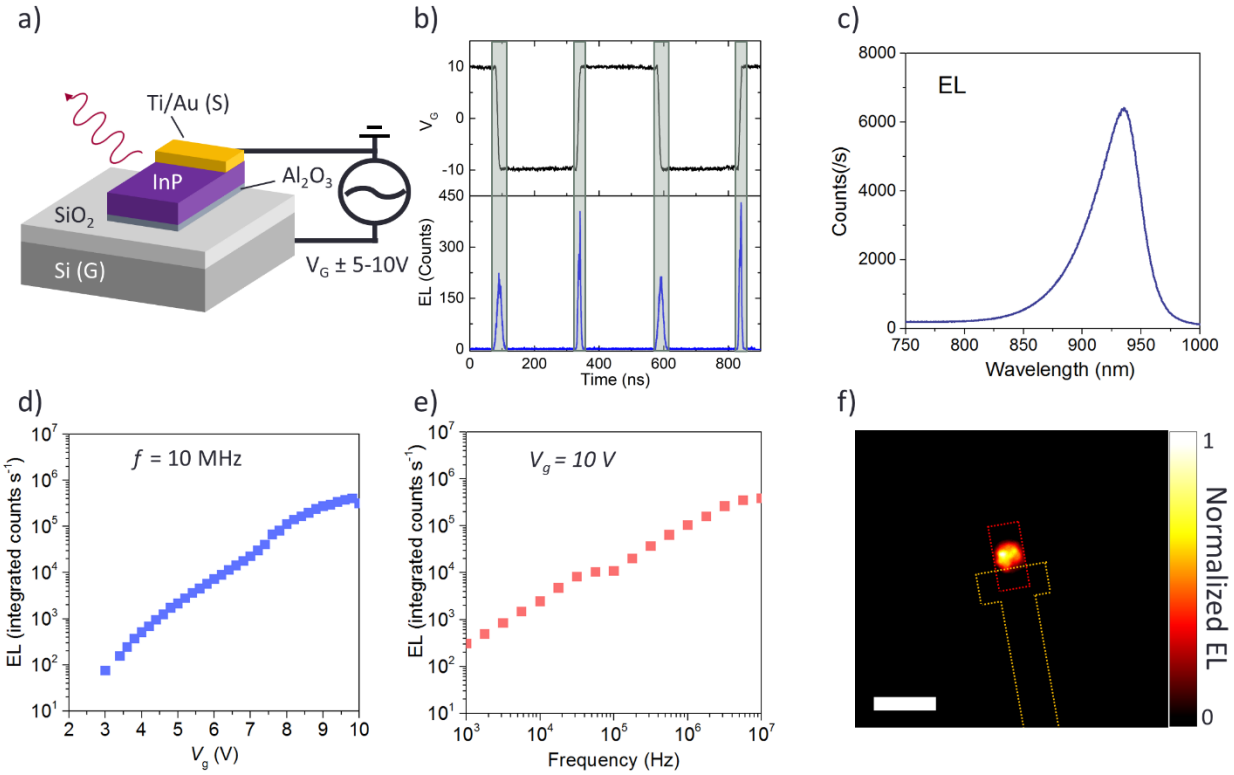

Figure 3-3. Transient EL devices on silicon and ITO substrates. (a) Schematic structure for Si/SiO_2 substrates. (c) Time-resolved EL spectrum for one full cycle of a t-EL device in operation. (c-e) Quasi-steady state EL spectrum, and integrated counts/s vs. V_g for a representative device. (f) EL image of device modulated with a V_g = 10V, f = 20 MHz square wave on Si/SiO_2 substrate, indicating emission near the contact edge.

approximately 8 ns for the rising edge and 15 ns for the falling edge), the number of emitted photons per transition is similar regardless of the dominant carrier to be injected.

The quasi-steady state (QSS) behavior of the t-EL device is demonstrated in Figure 3-3c-e. A QSS-EL spectrum for a typical device (10V 10MHz V_G) is plotted in Figure 3-3c, and the relative dependence of EL intensity with respect to gate bias and frequency are presented in Figure 3-3e and 3f respectively. The EL peak position at 935nm corresponds to a slightly lower emission energy than the typical InP bandgap and PL peak position, but the emission behavior is otherwise similar to t-EL results in the 2D material systems. Emission intensity increases linearly with frequency in the range of study, an expected result given the transient peak half-widths observed in TREL. The V_G dependence is relatively shallow in comparison to the 2D material case, however, and the weak "turn-on" transition at approximately 9 V is higher for our InP devices in spite of a smaller bandgap. This could be explained by the bulk nature of our devices, as the InP layers are more than 100 times thicker than the 2D materials previously studied, leading to some voltage drop across the semiconductor bulk rather than at the contact edge.

The practical operation of the t-EL device is then exhibited by EL imaging of devices on Si/SiO_2 and ITO substrates in Figure 3-3f. In the EL image of the typical Si/SiO_2/InP device, a relatively uniform emission profile is indicated away from the contact edge, though the intensity does appear to decay at distances more than ~8-9 μm. Hole and

electron diffusion lengths were previously measured to be ~1.4 to ~3 μm in bulk and thin-film InP respectively,[19,20] similar in value to the decay range. Edge effects due to growth morphology could also lend explanation to this effect, so further study of the emission decay and careful device design to consider decay behavior is necessary to maximize device efficiency. Still, the relatively long emission distance and reasonable uniformity of the InP t-EL structure indicates a promising path to pixel-level implementations.

3.6 Hall Mobility of Low-T TLP InP

In addition to a proof of concept device to show applicability of our process over a wide temperature range, an ultimate judgement of the material's electronic quality is necessary to determine viability for strict performance requirements in circuit structures. With this in mind, Hall measurements are performed using patterned layers to elucidate the true electronic quality of our material as a function of temperature, and single wire transistors are fabricated and tested directly on Si/SiO_2 substrates using material grown within a 400 °C thermal budget (Figure 3-4). Hall measurements for growth temperatures across the working range are displayed in Figure 3-4a, along with error bars following a geometrical estimation of hall voltage error (Supplementary Note 3) for each set of measurements. To avoid grain boundary and corner defect influence on measurements, a square geometry was chosen, with a size of 7x7 μm² and triangular contacts utilized to minimize error given the device shape (Details in Methods and Supplementary Materials). At least three devices across different growths are included in the statistics for each temperature to confirm consistency of the values and measurement. The doping concentration reported by Hall measurements is lower than expected at ~1-10× $10^{14} cm^{-3}$ for typical growths. However, the Hall mobility μ_H is quite promising for all temperatures measured, with mean values above 200 cm²/V-s for all temperatures and particularly impressive averages of ~770 cm²/V-s and ~518 cm²/V-s for 370 °C and 340 °C temperatures respectively. The highest μ_H measured for the 370 °C case is 965.9 cm²/V-s at a doping concentration of ~1.8× $10^{14} cm^{-3}$, a value approaching 20 to 30% of mobilities reported for theoretical calculations and similarly doped bulk InP respectively.[21, 22] This is of particular interest if some phosphorus-based compensation is responsible for our low measured doping concentration, as in Ref. 22, because of the lower theoretical mobility for compensated material. While our films are not grown or annealed in the significant phosphorus overpressure used for the referenced undoped wafers, at our low growth temperatures loss of phosphorus by decomposition (and diffusion through caps) could be lower in comparison to the delivered flux.

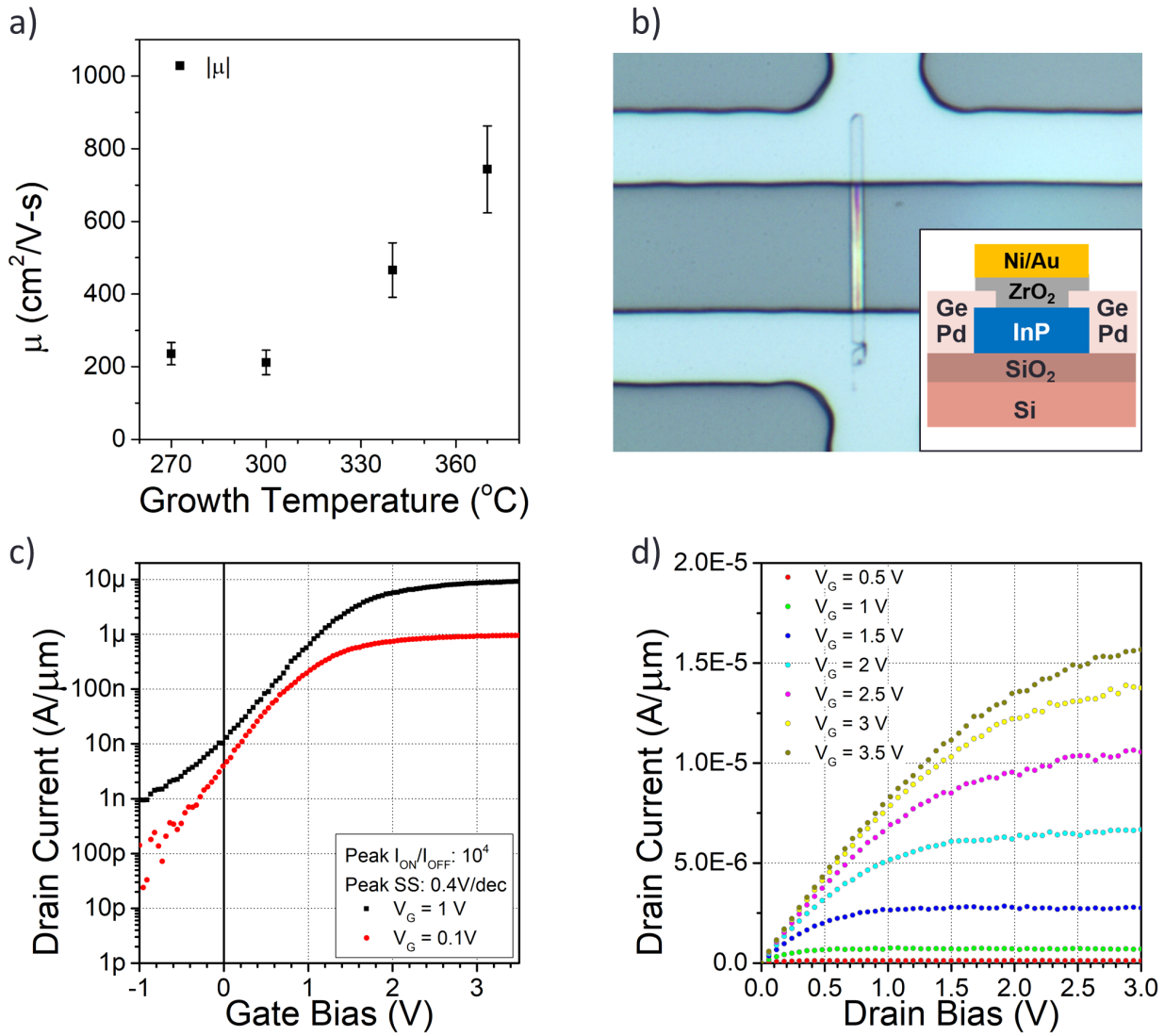

Figure 3-4. Electronic Characterization of LT-TLP material. (a) Mean Hall mobility vs. T, with error estimated by measurement geometry indicated by whiskers. (b) Schematic and optical image (before gate deposition) of a typical single-microwire transistor with InP grown at 370°C, W = 1 μm. (c) Transfer (I_D-V_G) and (d) output (I_D-V_D) characteristics of a single microwire transistor with W/L 1 μm/20 μm.

3.7 Low-T TLP InP Transistors

With promising Hall mobility data at temperatures well within the standard CMOS thermal budget, the natural next step is to utilize LT-TLP growth to produce and characterize transistors on Si/SiO_2 substrates as a proof-of-concept for integrated structures. A schematic structure and optical image of a typical device prior to gate deposition is displayed in Figure 3-4b. The fabrication process is a typical ALD top-gate scheme, with ZrO_2 gate dielectric, Ni/Au top gate, and a Pd/Ge based alloyed source/drain used to reduce contact resistance (details in Methods and Supplementary Materials). The Pd/Ge metallization is particularly important to the function of this device, as good contact resistance can be achieved at relatively low doping concentrations

while avoiding spiking and other common morphology issues with typical alternatives.[23] The transfer characteristics (I_D-V_G) for a device fabricated at a growth temperature of 370 °C and contact anneal temperature of 340 °C are presented in Figure 3-4c, and the output characteristics (I_D-V_D) are presented in Figure 3-4d. The device (with W/L 1/21 and thickness approximately 80 nm) exhibits key metrics of a 400 mV/decade subthreshold slope (SS), I_{ON}/I_{OFF} ratio of approximately 1.5×10^4, and I_{ON} of nearly 14 μA/μm at $V_G = V_D = 3V$. It should be noted that in this case contact resistance is a severe limiting factor for performance of these devices, as indicated by the significant roll-off of the I_D-V_G curve at high V_G. The contact resistance can be extracted from this structure by assuming the resistance at high V_G is dominated by the contacts, giving $R_{tot} \approx 2R_C$ at high V_G-V_T.[24,25] Extracting the contact resistance for this transistor (Extraction details in Supplementary Materials), we find that a relatively large R_C of approximately 44 kOhm-μm is present in our device, possibly due to the small contact area overlap present. Utilizing the standard MOSFET equation and including contact resistance, the expression for I_D becomes:

$$I_D = \mu C_{ox} \frac{W}{L} (V_G - V_T - I_D R_C)(V_D - 2I_D R_C) \quad (2)$$

Using this expression and the I_D-V_G curve presented above yields a peak contact-resistance corrected mobility of 663 $cm^2/V\text{-}s$. This mobility is comparable with average mobilities extracted from Hall measurements for this temperature, and very close to the mobility previously reported[10] for wires fabricated at 550 °C, indicating that the electronic quality does not drop significantly as growth temperature is lowered. While other device parameters could be improved with engineering of gate interface defects and contacts, this result implies great promise for III-V active materials grown at low temperatures on application-specific substrates.

3.8 Conclusion

In this paper, we have extended the already useful TLP growth technique into a new realm of possibilities, by demonstrating high quality III-V material growth at temperatures applicable to a large number of substrates. With promising proof-of-concept devices already explored for optoelectronic and circuit applications, future endeavors with this method can immediately target monolithic 3D integration of III-Vs in silicon CMOS and beyond. Additionally, other III-V materials can be studied to add to the LT-TLP material toolbox, including materials such as InSb and GaP previously explored in TLP growth.[10] In all, this is a versatile method that, when combined with the wide application space of myriad III-V materials, could enable significant progress in a number of areas.

3.9 Experimental Methods

Temperature Gradient Calibration

Prior to growth, the temperature gradient from furnace center to furnace end was calibrated using a thermocouple in-situ in order to closely approximate the substrate temperature for our typical center set point of 550°C. The thermocouple was inserted inside the tube via feedthrough, and temperatures were measured under gas flow at different positions. Substrate placement for each growth temperature was dictated by the highest temperature reading for all calibration conditions, to give a rough upper bound on growth temperature.

Substrate Preparation and Growth Method

Growth patterns and devices in this study were fabricated on 50nm SiO_2/Si n+ substrates with phosphorus doping. Commercial ITO glass (12Ω-cm ITO coating on square float glass, Sigma-Aldrich) was used for test patterns shown, with transparency and sheet resistance confirmed unchanged after the 270°C process condition. Polyimide substrates shown were prepared using SiO_2/n+ Si handle wafers and a spun polyimide film (HD MicroSystems, polyimide-2525) cured at 300°C. After growth, polyimide films were cut at the substrate edges and liberated via mechanical peeling. The growth process is similar to the method in Ref. 10 (theoretical details in Supplementary Note 1): Briefly, a starting substrate with a thin nucleation layer such as MoO_x, indium of desired thickness, and confining caps of SiO_x evaporated on all indium surfaces is prepared. The substrate is then heated in a tube furnace in hydrogen to the desired substrate temperature and exposed to PH_3 gas diluted in H_2 to a desired partial pressure. The resulting phosphorized films are then etched in HF to remove the SiO_x caps before further processing. Insulating Al_2O_3 nucleation layers were used for the ACEL devices and MoO_x nucleation layers were used for all other structures shown. Typical film thicknesses, measured by quartz crystal monitor, were ~5-10 nm for e-beam evaporated Al_2O_3, 0.3-1.3 nm for thermally evaporated MoO_x, ~40-150 nm for e-beam evaporated indium, and 10-50nm for e-beam evaporated SiO_x side caps. Further fabrication and measurement details for the device structures presented in this work can be found in Supplementary Note 2.

Optical Characterization

For SSPL measurement, a 532nm Nd:YAG laser was used to excite each sample at the same power (approximately 80μW), with light collected by a 50x objective lens, passed through a long pass filter, and analyzed by a Horiba LabRAM spectrometer and charge-coupled-device (CCD) camera. Photoluminescence quantum yield and electroluminescence data for this study were collected using a homebuilt optical system with components, wavelength calibration, and system response calibration details described in detail in Ref.18. Briefly, quantum yield measurements were calibrated using a ThorLabs SLS201 calibration lamp reflected off a Lambertian surface under the objective, followed with the measurement of system response by collection of the diffusely reflected excitation beam by the system spectrometer and cross-calibration with the lamp.

The PL response was then corrected to the system response, and Ar^+ ion laser excitation power used in the EQE calculation and referenced in each plot were measured by laser power meter simultaneously. Single pass absorption was assumed for all cases in the IQE calculation, due to the lack of back reflector in all configurations.

EBSD Measurement

EBSD measurements were performed using an FEI Quanta FEG SEM and an Oxford EBSD detector with a fluorescent screen. Oxford Aztec and Tango software were used to analyze the EBSD patterns and maps, and to generate inverse pole figure color schemes for the data shown. Twin boundary correction was performed in the same software by removing <111> 60° rotational boundaries and replotting grain surface orientation. Twins are a common feature in InP due to low stacking fault energy,[10] so while twin correction is needed to adequately display nucleation behavior by EBSD, other extracted optoelectronic and electronic parameters display our material's fundamental quality.

Electron Concentration Estimation for Comparison of Urbach Tail Parameter

Doping concentrations referenced for extraction of the Urbach tail parameter in Figure 3-2 were extracted assuming a Burstein-Moss shift due to band filling in the InP.[26] Using a parabolic band model, the doping estimated from band edge shift is given to be:

$$n = 10^{19} cm^{-3} \left(\frac{\Delta E_g}{16.9} \frac{m}{m_0} \right)^{\frac{3}{2}}$$

Here, m/m_0 is the ratio of the InP electron effective mass to the free electron mass, and ΔE_g is taken with reference to a wafer with a low nominal doping concentration, in our case a reference wafer (plotted in Figure 3-2) with doping concentration $5 \times 10^{16} cm^{-3}$. It should be noted that this relationship may differ from electronically extracted doping concentrations, as the method is not as accurate[27] for values of n less than $\sim 1 \times 10^{16} cm^{-3}$.

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CHAPTER 4

CONCLUSIONS AND FUTURE PROSPECTS

As we look to the future, significant challenges lie ahead as our world becomes more populated and polluted, and as climate change threatens to upend the ways and places we live. It is in times like these that innovation must accelerate, especially in areas that can address some of these environmental and resource-driven challenges. In my work for this dissertation I sought to contribute to some of these solutions, by offering a way to enhance the scalability of solar fuels generation, and by attacking some of the fundamental problems with device integration through development of new material processing methods.

In Chapter 2, an exploration of scalable thin-film growth of the high efficiency photovoltaic material InP is presented, with direct application in a photovoltaic cell configuration that generates storable hydrogen fuel from sunlight. An ex-situ doping method is discussed to enable efficient device structures for this application, and an efficient electron selective contact is utilized, characterized, and demonstrated to improve both device operation and stability. The doped material and devices are found to have high optoelectronic and structural quality, and the devices are found to function well in the harsh environment of the photoelectrochemical cell, producing hydrogen fuel for a number of hours without degradation. Finally, a promising cell efficiency is demonstrated, with a value of 11.6% closely approaching that of bulk wafer analogues.

In the future, expansion of TF-VLS growth for photovoltaic applications can focus on the future of PV, with tandem architectures a natural path for the utilization of a direct, scalable III-V growth technique. To realize this end goal, ternary explorations would be needed to include both group III and group V components in the process, or heteroepitaxy would need to be realized with a TF-VLS virtual substrate. The first system to target could be the gallium-based compounds, for which the method discussed in chapter 3 may be utilized to surpass some practical barriers experienced thus far.

In Chapter 3, the templated liquid phase crystal growth process is explored over a much wider temperature range than before, with the goal of lowered processing temperatures for integration on a wider set of possible substrates. The nucleation behavior is studied in detail as growth temperatures are lowered, with linkage to the descriptive nucleation model of TF-VLS growth. Single crystal domains are still demonstrated at growth temperatures below 300°C, and optoelectronic quality is again found to be promising regardless of growth temperature. A direct application of this material for light emitting devices is explored with a transient electroluminescent device fabricated at 270°C, an application that could have broad impact to on-chip photonics. Finally, the ultimate electronic quality of the material was demonstrated with Hall measurements across a large temperature span, with mobilities greater than 200 $cm^2/V\text{-}s$ in the entire window

and a mean value near 800 $cm^2/V\text{-}s$ demonstrated at 370°C. This holds great promise in 3D integration applications for III-V transistors fabricated through direct growth, with a preliminary transistor effective mobility greater than 600 $cm^2/V\text{-}s$ demonstrated directly in this work.

Looking to the future, this significant expansion of the growth temperature range for III-V electronic materials could open a new and exciting path to integration of efficient optoelectronic materials on a large set of application-specific substrates, including glass and plastic based systems. Future work in the technique should focus simply on the realization of these "killer apps," with direct demonstration of multilayer 3D integration on silicon CMOS a clear first goal. With further structural innovation and device design, III-V on silicon photonic structures could also be explored, such as InP lasers that have already shown promise for photonic circuit applications.

In short, as both promising applications and highly scalable and versatile methods were demonstrated in this work, future prospects are bright for TF-VLS growth of III-V materials, as a host of optical and electronic applications is now available for rapid pursuit.

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APPENDIX A: SUPPLEMENTARY DATA & NOTES FOR CHAPTER 3

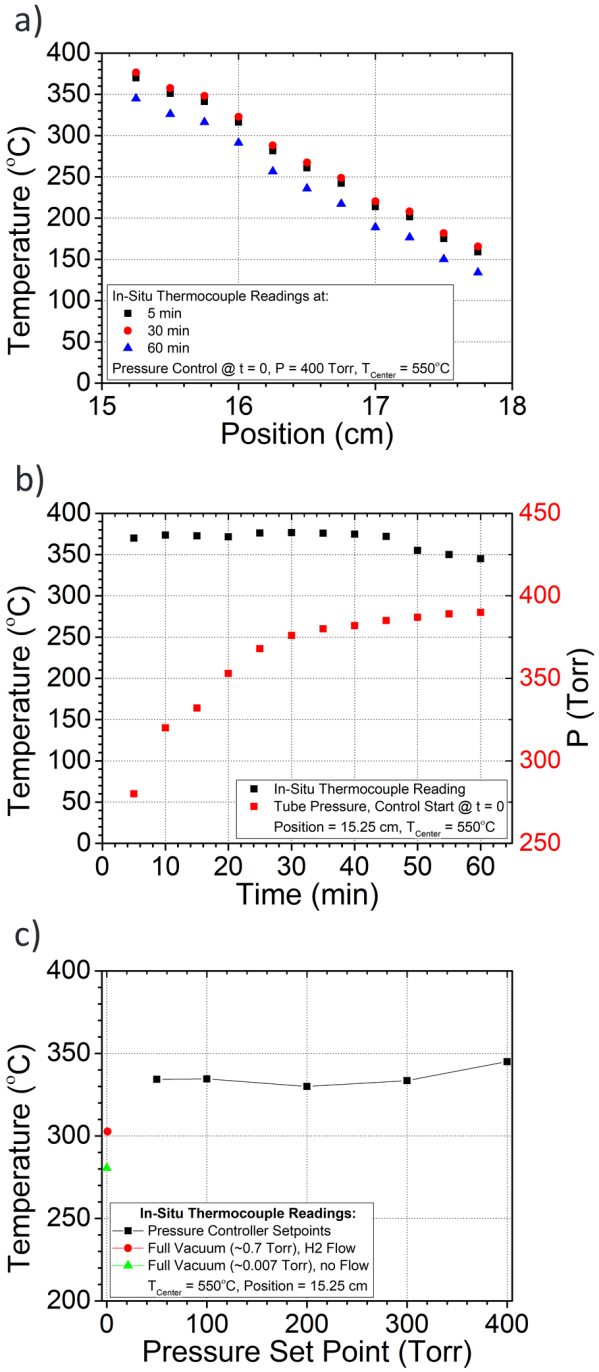

Figure S1. Calibration data for the tube furnace gradient near typical sample positions, with position referenced to the furnace center and time referenced to the butterfly isolation valve transition (pressure control start). Readings were taken with a bare thermocouple fed into the quartz tube to provide accurate readings under gas flow. (a) Temperature vs. position over the course of a normal growth process time. (b) Variation in the temperature at a given sample position vs. time, with pressure controller reading included as a reference. (c) Variation in the temperature reading as a function of gas pressure after long-time stabilization, at the same position as in (b).

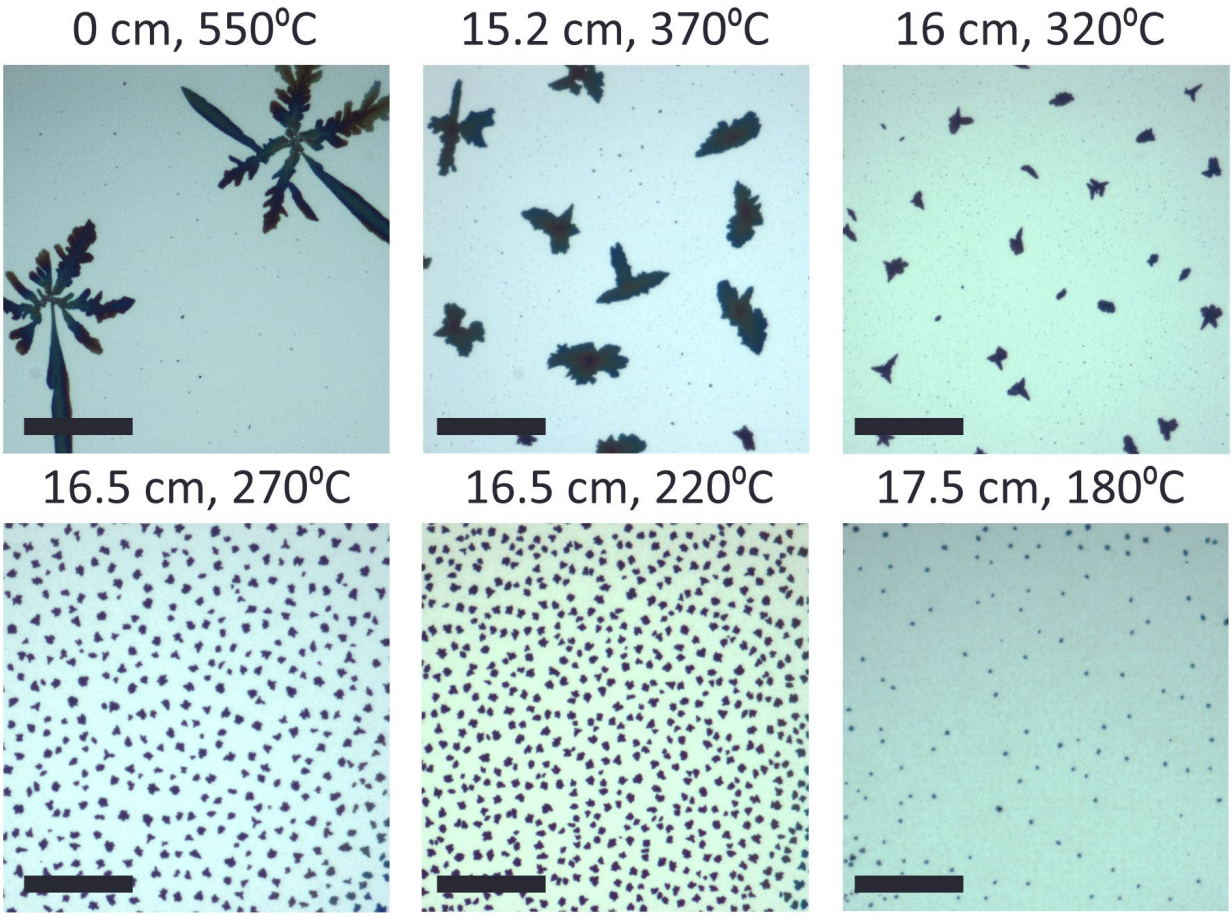

Figure S2. Nucleation density and growth images for thick (~100nm) large area indium/MoO_x/SiO_2/Si substrates, and demonstration of lowest growth temperature observed. 3 minute growths are used with typical PH_3 partial pressure, demonstrating relative growth rate and nucleation density as temperature is lowered. Scale bars 30 micron.

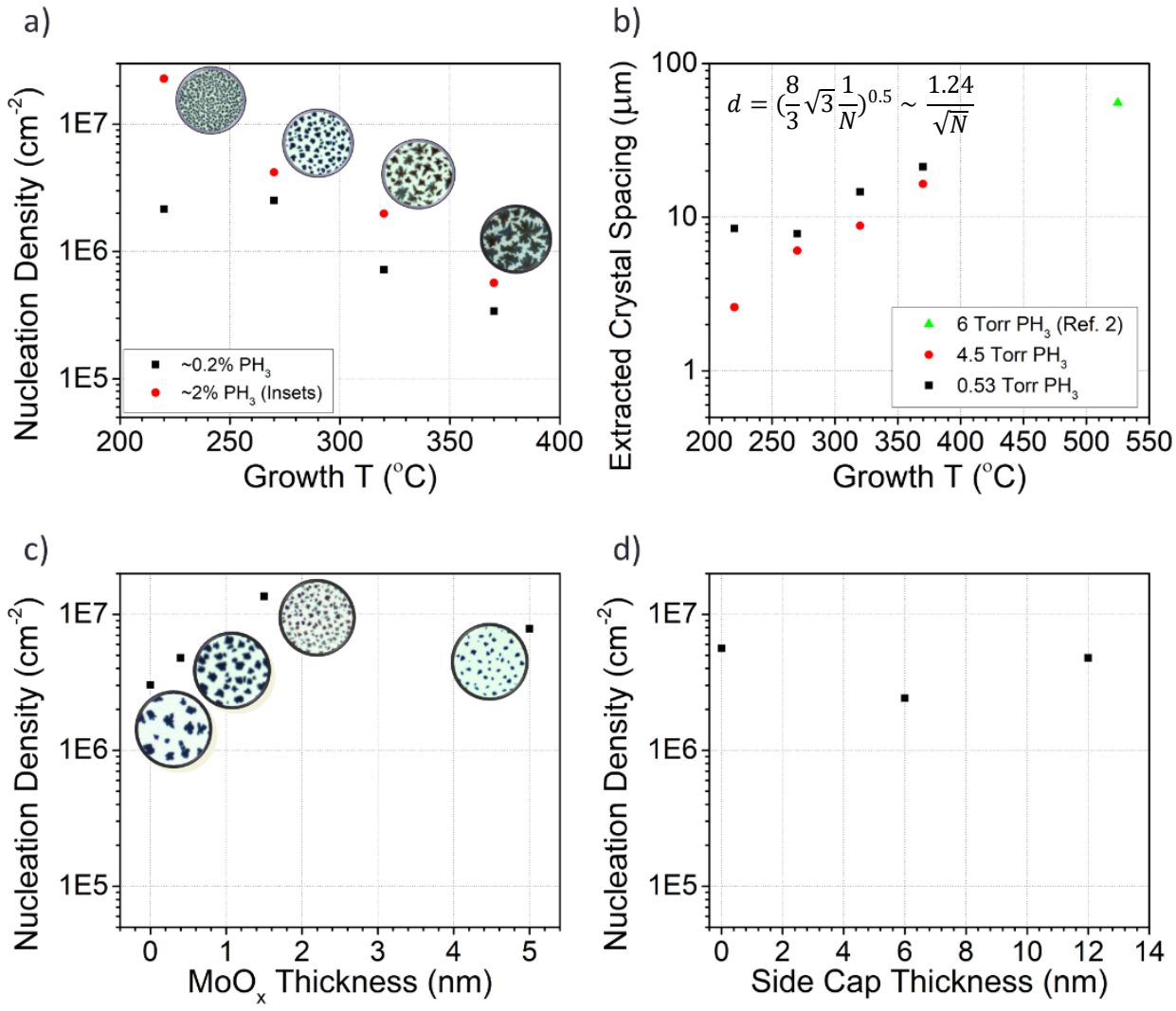

Figure S3. Nucleation density vs. temperature and substrate structure with representative images for nucleation counts in insets. Cropped areas are 30 micron in diameter. (a) Nucleation density vs. Growth T for 2 different PH_3 concentrations, (b) extracted crystal spacing extracted from nucleation density N assuming hexagonal packing (equation in inset, Ref. 10) with reference spacing included from prior work, (c) nucleation density vs. MoO_x nucleation layer thickness including a no-nucleation layer case, and (d) relative insensitivity of nucleation density for different thicknesses of SiO_x side caps in a 3-cap configuration.

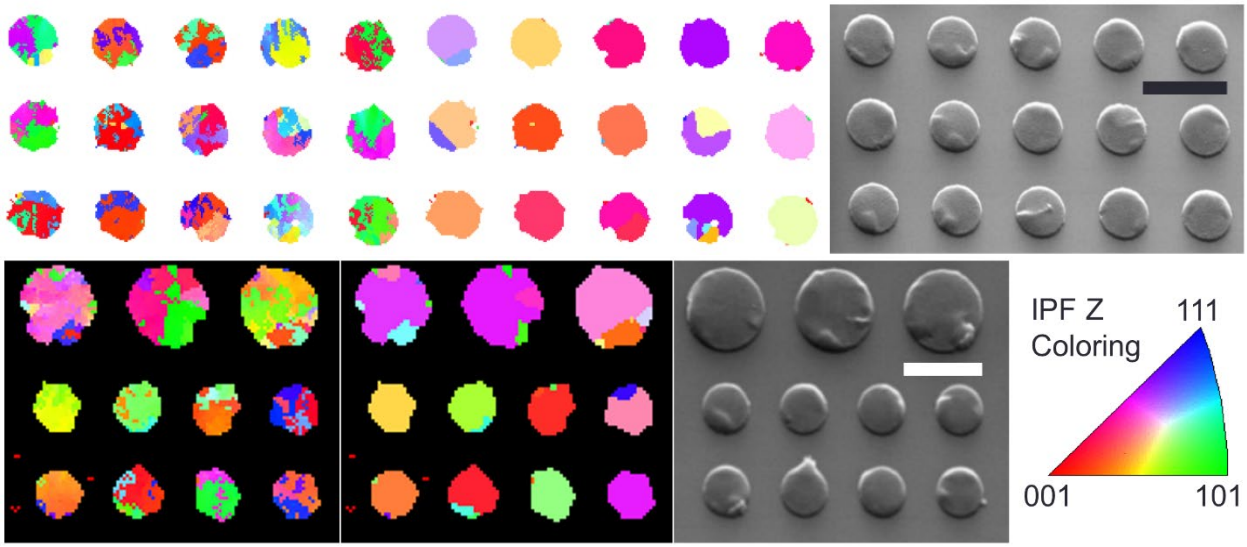

Figure S4. Additional EBSD maps and corresponding SEM images for patterns grown at 270 °C, (a) before and (b) after twin correction (ignoring <111> 60° rotational boundaries, details in Supplementary Note 2). The IPF color map is provided with orientations marked, and scale bars are 8 and 10 micron respectively.

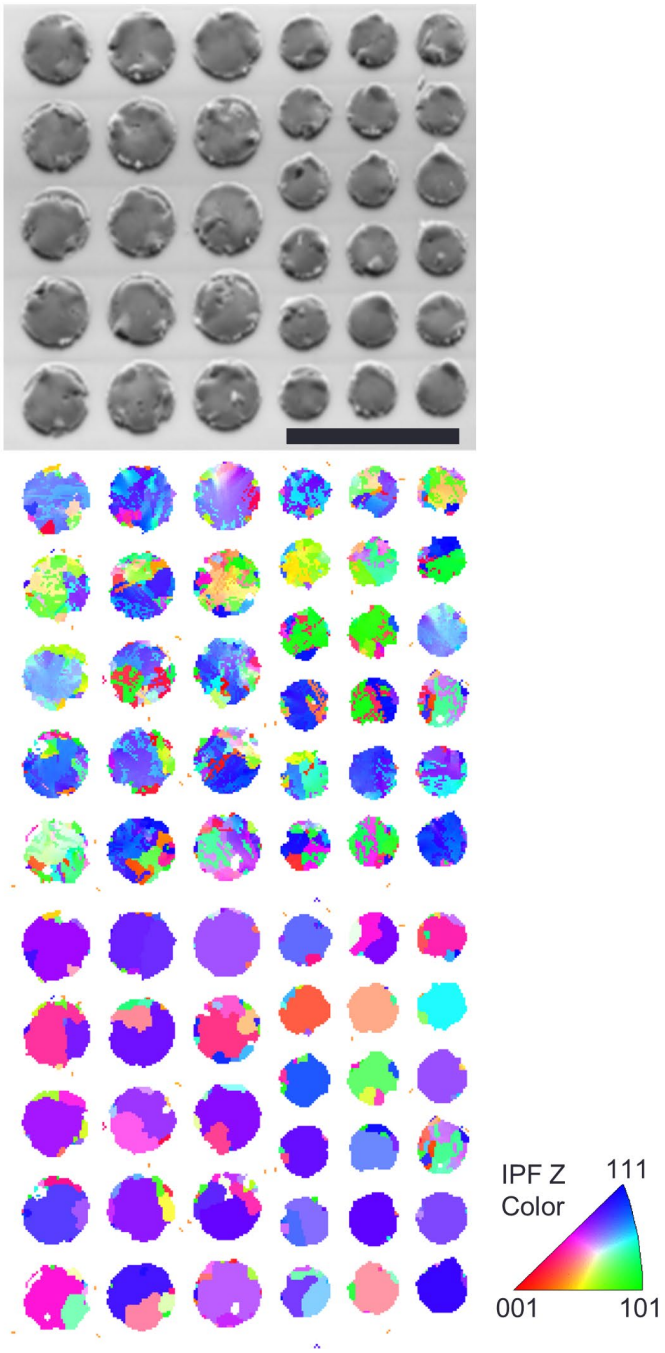

Figure S5. Additional EBSD map of material grown at 370 °C, (a) before and (b) after twin correction. Scale bar is 50 micron, indicating that some features at the 15 micron size and very few at the 20 micron size are single domain after twin removal.

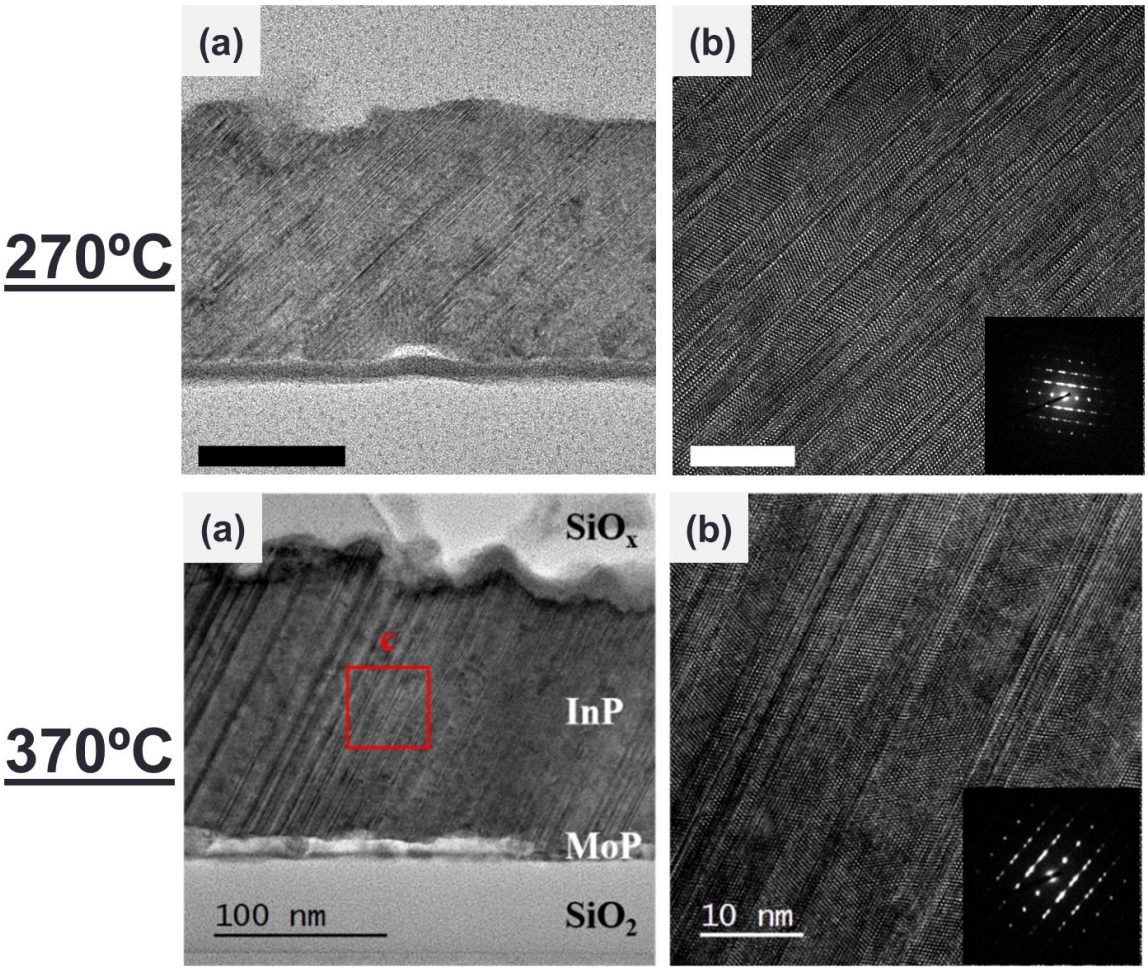

Figure S6. Comparison between TEM and HRTEM images of crystals grown at 270 and 370 °C. (a) TEM image of a FIB cut crystal edge for each temperature, and (b) HRTEM zoom with SAED inset to observe twinning behavior. Double diffraction in the SAED patterns indicates twinning in both crystals. Scale bars 50nm and 10nm for the TEM and HRTEM at 270ºC.

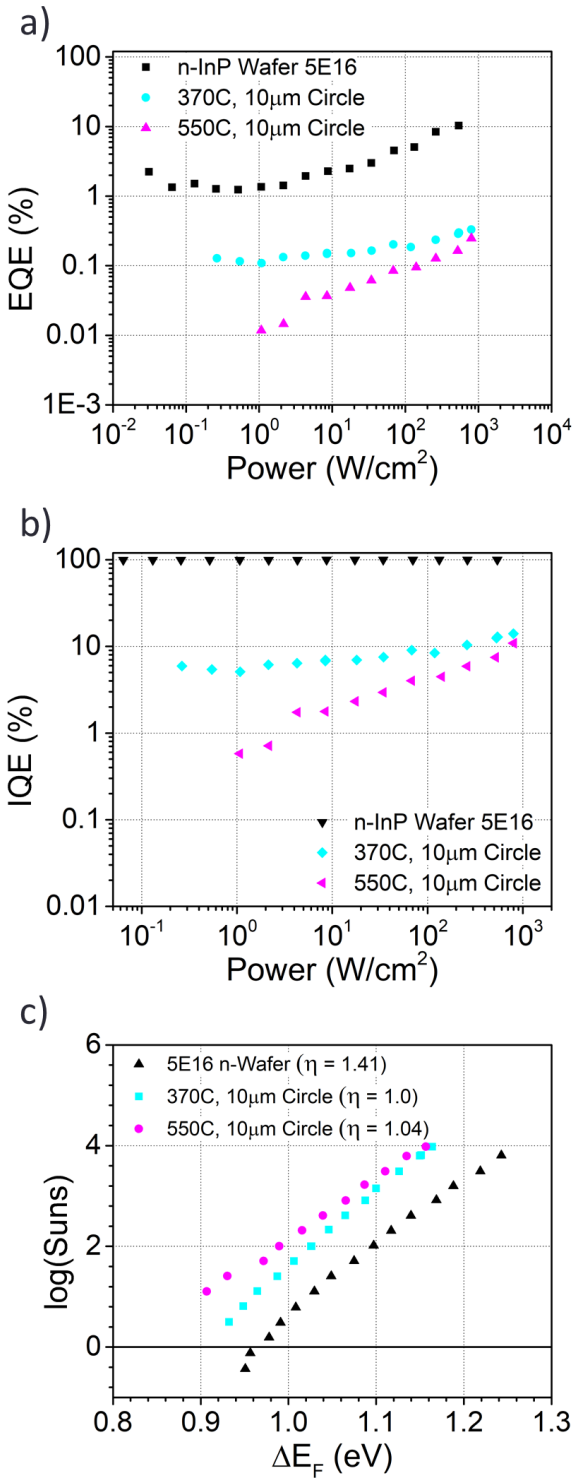

Figure S7. Photoluminescence EQE, IQE, and optical I-V measurements on a crystal grown at 370 °C by our method, with reference to a crystal grown at 550 °C by a typical TLP method. A bulk reference wafer doped at 5E16 cm^{-3} is included for comparison.

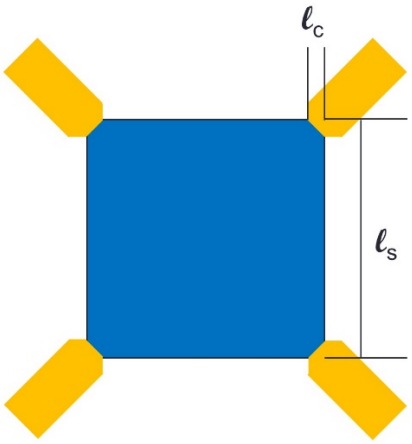

Figure S8. Representation of our Hall device measurement pattern. L_c/L_s was ~0.16-0.17 in a typical configuration.

Supplementary Notes for Chapter 3

Supplementary Note 1: Growth Process Nucleation Density vs. Temperature

In the TF-VLS growth process, the nucleation and growth of InP from a supersaturated solution of P in In follows directly from the In-P phase diagram. Control of nucleation density is given due to the limited amount of phosphorus that is able to make it through the SiO_x cap, as when a nucleus is formed the growth of that crystal starves available phosphorus from the surrounding area by a diffusion-based "depletion zone." As PH_3 is cracked separately in our process, the nucleation density at a given temperature therefore depends on how much phosphorus can still get through the cap and on the width of this depletion zone. In prior work,[11] it was determined that the density of InP nuclei in a large area film can be expressed as the following equation:

$$N_{Total} = \frac{A}{h^2}\left(\frac{Fh^4}{D}\right)^{\alpha}$$

In this equation, D is the diffusivity of phosphorus in indium, F is the flux of indium through the cap, h is the height of the indium, α (~0.6 for our system) is related to the number of atoms in a critical nucleus η, and A is a fitting parameter related to the capture cross section of phosphorus atoms for both nucleation on existing islands and as new domains. In the experiment shown in Figure 3-1 and Figures S2 and S3, this expression holds true due to the film configuration of the nucleation promoter, so the result we observed is essentially as expected. As temperature is lowered, the most sensitive parameters will be the F and D coefficients, as both depend on an exponentially varying diffusivity (through the "barrier" cap for F and the indium for D) factor if phosphorus delivery to the substrate is equal. Therefore, it appears that D drops faster than F here, perhaps due to minimal blocking in the thin cap layers used in this study. Further study at each temperature point of nucleation density with respect to flux could identify η and A parameters and identify correlation between bulk phosphorus diffusivity and our case, though care would have to be taken at some lower temperatures due to very high nucleation densities at low fluxes.

Supplementary Note 2: Fabrication Methods and Device Measurement Details

t-EL Device Fabrication and Measurement

All transient EL devices were fabricated using material grown at 270°C ± 10°C, with PH_3 partial pressures approximately 1-5 Torr. To lower the effects of surface recombination, thicker than typical layers were used for the devices, at approximately 400-500 nm as grown. Following growth and cap etching, a light wet mechanical polish was performed, followed by a second surface clean in hydrofluoric acid. Ti/Au contacts patterned by G-line photolithography were used for a typical device, with a forming gas anneal at 270 °C for approximately 10 minutes to improve the contact-InP interface. For

all devices, a lower than normal contact anneal temperature was chosen to fit the maximum growth temperature, maintaining the low-T process window. Measurements were performed in a similar manner to Chapter 3 Ref. 18, with the Ti/Au source grounded and a square wave excitation applied to the silicon back gate. Importantly, the Al_2O_3 used as an insulating nucleation layer contributes to the effective oxide thickness, and the non-insulating MoOx also trialed decreased device function likely due to screening. The square wave was generated by a bipolar-based Agilent 33522A waveform generator, and EL images presented were collected using a microscope system and an Andor Luca camera with excitation in ambient environment.

Hall Device Fabrication and Measurement Details

Hall measurement devices were fabricated in a square configuration using MoO_x nucleation layers less than 1.4 nm and as-grown thicknesses of approximately 85-90 nm as estimated by AFM and cross-sectional TEM measurements. A square Van der Pauw[28] configuration with devices in the 7-10 micron size range was chosen to limit fabrication and growth complexity, and electron beam lithography was used to pattern contacts to avoid alignment offset error. A Pd/Ge metallization was used to give linear contact behavior for all devices, with rapid thermal annealing in a 5% H_2 / 95% N_2 ambient to improve contact resistance. The temperature for this step was maintained at a maximum of 10°C above the growth temperature to avoid annealing effects on the electrical parameters. An Ecopia HMS 300 Hall measurement tool was used with a ~0.55T permanent magnet for the presented measurements, with currents in the 10-100nA range. Further details on the measurements and cross-checking procedures, along with geometrical error estimation, can be found in Supplementary Note 3.

Transistor Fabrication and Measurement Details

Transistor devices were fabricated using InP grown at 370°C ± 10°C, given the higher measured Hall mobility at this growth temperature. First, microwires were patterned using e-beam lithography with widths between 250 nm and 1000 nm. Indium substrates were prepared as previously described, with MoO_x nucleation layer thickness less than 1.2 nm and indium thickness approximately 30-40nm. Source and drain contacts of Pd/Ge were then patterned by photolithography on the ~75-85 nm as-grown films, with channel lengths between 4 and 20 μm. To minimize contact resistance, an optimized Pd/Ge rapid thermal alloy process was used in a forming gas ambient,[23] in order to dope a thin surface layer under the contact and provide a spike-free alloyed contact interface with the PdGe alloy metal. The optimum contact annealing conditions were a 225°C/3m initial alloy step followed by a 390°C/3m anneal step, though contact resistance could still be improved beyond the ~10kOhm+ range presented in this work by more targeted doping and activation procedures such as ion implantation in future devices.

Following contact annealing, a 15 nm ZrO_2 gate oxide a was thermally deposited at 200°C using a Cambridge Nanotech ALD system and tetrakis(ethylmethylamido) zirconium (TEMAZ) Zr precursor with water as the oxidizer. The gate metal was then patterned by photolithography, with a Ni/Au gate used to compare to prior InP devices.

Supplementary Note 3: Electronic Measurement and Extraction Details

Hall Measurement Cross-Checking and Geometrical Error Estimation

For Hall measurements in the typical 4-point Van der Pauw geometry (Figure S8), a Hall voltage error is introduced due to influence of the forced current on the voltage measurement probes when contacts are larger than the idealized "point" configuration.[28] With a square Hall pattern and triangular contacts, it is estimated that a value of l_c/l_s = 1/6 gives an error of approximately 15% in the final Hall voltage, leading to systematic error in the measurement of Hall mobility. In particular, the values of the resistivity correction factor and Hall resistance (and therefore mobility) correction values follow these expressions for a square geometry:

$$\frac{\Delta\rho}{\rho} \propto \frac{{l_c}^2}{{l_s}^2} \qquad \frac{\Delta R_H}{R_H} \propto \frac{l_c}{l_s} \qquad (per\ contact)$$

While other structures can be used to measure Hall mobility, such as clover leaves and Greek Crosses, these structures introduce additional fabrication complexity due to either etching or growth of their required patterns, and could affect the quality of our material without careful optimization. Thus, a more simplistic approach was taken here, and errors from the original finite difference calculation referenced here were included in our mobility plots. With our device geometries designed to a ratio of ~0.16-0.17 as-patterned, our final error is ~15%. A 16% error was assumed for the plotted data based on an overestimate of contact overlap, though statistics on multiple measured devices (N = 10) also give a Std. error of 15.1%. In addition to geometrical error, cross-checking was performed to compare measurements from different tools and rule out internal systematic error – while an Ecopia HMS-3000 Hall Effect tool was used for the presented data, resistivities extracted from Van der Pauw 4 point measurements were cross-checked and confirmed with an Agilent B1500 parameter analyzer, and reference mobility samples were confirmed on each tool prior to measurement. For all measurements, contact linearity was confirmed in the measurement range by the parameter analyzer, and the ratio of vertical to horizontal conductivity was minimized for accepted data to avoid misalignment error.

Transistor Contact Resistance Extraction and Effective Mobility Correction

For contact resistance extraction, a polynomial model was used in the high gate overdrive region of the $I_D V_G$ curve at low V_D (0.1V) for a given transistor device:[25]

$$b_1 + \frac{b_2}{x} + \frac{b_3}{x^2} \qquad b_1 = 2R_C$$

As V_G goes to infinity, R_{Total} in the transistor approaches $2R_C$ as the channel resistance becomes negligible. However, in many cases the device oxide will break down before the curve becomes sufficiently flat, so a fit of the decay above can be used. For the device presented in Figure 3-4, the following values were extracted:

	Value	**Standard Error**
$\boldsymbol{b_1 = 2R_C}$	87666.32025	1097.52441
$\boldsymbol{b_2}$	20739.40394	3221.6751
$\boldsymbol{b_3}$	42435.74789	2104.6578

APPENDIX B: TF-VLS SUBSTRATE AND GROWTH REQUIREMENTS

For the TF-VLS growth process, there are a number of critical requirements for substrate preparation and growth that must be considered depending on the template in question. In this appendix, I will discuss a number of these, with particular emphasis on the thin-film and templated variants of the TF-VLS growth method.

First, we must consider each portion of the structure carefully. In a typical configuration for III-V growth, the structure is composed of a substrate, nucleation layer, metal precursor layer, and capping layer. The substrate is considered arbitrary for all further discussion, but typically has much lower nucleation density than the patterned or unpatterned nucleation layer. For this process, the nucleation layer and capping layers are idealized in structures and discussions as continuous thin films, but in reality this is not likely to be the case depending on preparation conditions. Likewise, the metal precursor layer is idealized as a flat thin film, but surface roughness and deposition conditions can strongly affect the growth process due to secondary effects on other layers, and defects in the film can contribute to the final quality of films.

The large area thin-film case is the easiest to visualize due to the simplified structure, and the full area nucleation layer is first discussed. For all large area structures discussed in this report, a molybdenum nucleation layer was used as it provided a convenient back contact for the devices implemented using these films. In many cases foils were used, but the roughness of the foils has a strong impact on the final morphology of the growth. Polishing can be used to avoid this effect, but this is a critical consideration if smooth foil substrates are needed. Thin-films deposited by sputtering or other methods were also trialed, but deposition parameters for these are also critical. In particular, roughness can be controlled depending on rate and substrate sputtering (with higher rates and pressures giving higher roughness), and substrate adhesion can be improved by pre-sputtering in many cases. All parameters such as power and partial pressure (for sputtering) must also be controlled carefully to avoid film stress, which is found to strongly affect film stability after growth due to the partial conversion of the metal nucleation layer. In summary, all parameters of nucleation layer deposition must be carefully controlled and characterized for each deposition method, to avoid further damage during the growth reaction.

For the large area case, the metal precursor layer process is deceptively simple, but has a strong influence on the success of growth as well. In a simplified description, e-beam evaporation is performed on a water-cooled substrate at high rates due to relatively large thicknesses in most applications. However, all of these parameters are important for final morphology, as both cooling and rate have a strong influence on the final surface roughness of the precursor layer. First, the substrate must be in intimate contact with the stage, to ensure uniform cooling across the substrate area, as most group III metals have low melting points that can cause dewetting or excessive surface mobility during deposition. Cryogenic cooling can also be used for some thickness ranges to ensure very smooth surfaces, which will be further discussed in the TLP substrate requirements. The rate of the metal deposition is also critical, and in many cases a two-stage process must

be used to tune surface roughness. With high surface mobility, some precursor metals agglomerate differently depending on deposition rate. It was found in our studies with indium that high deposition rates induce moderate roughness with water cooling, and that low deposition rates increase surface roughness of the film. This can be envisioned with impingement rate as a context, as with high surface mobility agglomeration depends on the rate of arrival due to kinetic limitations. With very thick films, the surface roughness has a large influence on the growth rate and morphology, as flux can be very limited through a thick cap and as very smooth films have limited area for volume expansion that can lead to stress-based cracking. Therefore, in thick full-area configurations presented here, we use a fast rate (~5nm/s) to induce moderate roughness to approximately 90% of the film thickness, followed by a slow rate step (~0.2nm/s) to increase surface roughness to a desired level. Roughness values were not thoroughly quantified in these studies, but in the future a particular process can be easily tuned due to the relatively monotonic increase in roughness using this method. In addition, high purity precursor metals should be used, and crucible choice and cleaning is critical to avoid any adverse contamination during this process.

Finally, the capping layer is a critical parameter of this method in particular, as with a full-area film it can very easily block phosphorization completely if deposited incorrectly. In most useful configurations, SiO_x deposited by e-beam evaporation is used, as it provides a semi-permeable layer due to vacancies even in an idealized context. However, the process can also provide voids at some thicknesses, which can be tuned to some degree (or perhaps patterned in a more controlled process) to enable larger group V precursor fluxes. The rate of the deposition can again be tuned to control these parameters, but care must be taken to avoid over-decomposition of the cap layer that can cause interactions with the precursor metal. Another consideration is cap "blockage," which can be caused by premature conversion of the cap to the effective SiO_xP_y diffusion barrier. This can of course depend strongly on the SiO_x stoichiometry and growth conditions, so these must be carefully controlled.

As the TLP process utilizes patterned nucleation layers, precursor metal, and top caps, the effects of nucleation layer and top cap thickness are much stronger in this context. Thin nucleation layers such as MoO_x are typically used here to avoid issues with device structures, so the surface coverage of these films can again strongly influence the nucleation density. The dependence of nucleation density on MoO_x thickness in Figure S3 is clear evidence of this. This is straightforward to consider, as a substrate with much lower nucleation density is effectively interspersed with a higher nucleation density layer. However, in some low temperature cases nucleation can still occur without a nucleation layer, so the nucleation contrast between substrate and nucleation layer should be studied carefully as a function of temperature as well. In this case, precursor metals should usually be quite smooth to enhance the quality of the final film, so cryogenic cooling is used (by way of cooled gas flowed to the chuck) to greatly decrease metal surface mobility and control surface roughness. The top cap is therefore especially important in this context, as depending on feature size and growth temperature side-only diffusion may be unrealistic for complete growth. The stoichiometry and coverage considerations previously discussed should again be carefully controlled to this end, and each additional

nucleation layer utilized (such as the Al_2O_3 used in this report) needs to be characterized to identify these issues.

The use of side caps in the TLP process adds another level of complexity to substrate preparation. In the idealized case, most flux enters through these caps, so again the stoichiometry and void formation should be carefully considered. In most cases, side cap deposition rate is approximately 0.1-0.2nm/s, about half the rate of top cap deposition. Side caps are also deposited at high angles to access the side walls, so angle is carefully chosen (here approximately 60-70 degrees) to ensure top caps are not excessively thickened during this process. For reasonable growth rates, all cap thicknesses need to be reduced as temperature is reduced due to decreased diffusivity, with an approximately 5x reduction from 550 to 270°C.

Following proper substrate preparation, the growth parameters must also be carefully considered. First, we consider the heating phase of the growth, where a reducing gas is typically used (hydrogen in our case). Due to the substoichiometric caps and nucleation layers, as well as the possibility of precursor metal oxidation, this could have a strong effect on their parameters. Therefore, any changes to the background gas and its interactions should be considered if the process is to be modified. During the growth itself, the precursor gas is always introduced at the target temperature to avoid spurious nucleation. In all cases presented, the precursor gas is diluted in hydrogen. This can also have an affect on the catalytic properties of the growth process, as some complexes could be forming at different rates depending on hydrogen concentration. Further study could utilize mass spectrometry to tune this effect if needed, and dopant introduction would make this knowledge especially important. Growth rate can also have an effect on sample morphology, so in high-stress conditions (such as large thicknesses) this needs to be carefully controlled to avoid film cracking and other such issues. Finally, previously discussed, the cap and nucleation layer also change during growth, so it is not straightforward that all lower precursor concentrations lead to lower growth rates. Therefore, depending on the intended material system, all of these parameters must be co-optimized with substrate conditions to achieve the perfect TF-VLS growth.

APPENDIX C: PATHWAYS TO IMPROVEMENT OF TF-VLS AND TLP GROWTH

In this report, we presented promising proofs-of-concept for both TF-VLS and low-temperature TLP processes, with promising devices in both cases that indicate future applicability of each technique. However, as these were lab-scale productions, it should be noted that there is significant possibility for improvement. In this section, I identify process modifications that can provide such pathways, with particular emphasis on improvement of process control and final film electronic quality.

First, the thin-film deposition process and general substrate preparation should be discussed. In this case, all substrates were prepared using shared tools, with background contamination of other metals an unfortunate reality. For nucleation layers and caps, vapor pressure contrast ensures that contamination is limited, but in an ideal process flow this effect should be eliminated. However, for the precursor metal, low-temperature alloys are possible with a variety of metals, contributing to the possibility of substrate contamination. Therefore, the first process modification should be the use of dedicated UHV deposition tools for all substrate preparation, with typical process control similar to CMOS systems to avoid cross-contamination in all processes. Liftoff processes were used for all demonstrations here, but etch processes could also eliminate additional contamination such as polymer and carbon residue and enable advanced substrate structures. Additionally, as discussed in the substrate preparation methods, rate control and substrate cooling are very important parameters, so with dedicated tools these should be controlled more precisely to allow statistical process control and modification in an industrial context. With additional resources, local patterning or control of nucleation and cap layers should also be explored. It is clear that void formation is one avenue for precursor flux, so again a process utilizing careful patterning of these layers (such as with a milling or imprint process) could offer a path to improved process control.

For the growth process, definite improvements in process uniformity and scale are clear with only minor modifications to the overall apparatus. As the large area thin-film process is primarily done in a standard CVD configuration, only minor improvements to the precursor flow pattern (such as with a showerhead) are necessary, so we should focus on the LT-TLP process here. For the LT-TLP process, the key components are the cracking and gradient zones of the apparatus. For cracking, a thermal method can be used, but more complete cracking and access to other species can be gained with a plasma cracker. This would allow the T gradient start and end points to be controlled over a wider range as well. For increased process uniformity and substrate size, a UHV vertical furnace with increased flow uniformity could also be used, as in this case only a thermal gradient is needed to enable correct precursor delivery to the substrate. Finally, exploration of additional precursors can improve the process, such as the inclusion of high purity doping sources during the growth process and mass-spectrometry characterization of products.

For all of this, an amazing aspect of this process is its room for improvement, as preliminary lab-scale explorations are already promising. Significant areas for additional study are certainly possible, with pathways to technology transfer especially clear.