Characterization and Modeling of Ceramic Capacitor Losses in High Density Power Converters

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Characterization and Modeling of Ceramic Capacitor Losses in High Density Power Converters

by

Samantha Nicole Coday

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in

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Committee in charge:

Prof. Robert Pilawa-Podgurski, Chair
Prof. Seth Sanders
Prof. Scott Moura

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Abstract

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Ceramic capacitors offer reliable and dense energy storage in power conversion applications. However, to effectively incorporate these devices in a design, it is important to have an accurate model of losses for the conditions under which the devices will be used. Small signal loss parameters at low bias voltage are frequently provided by the manufacturer, but the correlation between these data and losses exhibited under realistic large signal excitation has not been explored in detail. This work aims to provide a method for measuring capacitor losses under realistic operating conditions, using a calorimetric approach to provide an accurate measurement of losses under large signal excitation. Specifically this work will investigate the effect of high voltage bias and varying AC excitation on losses. This work concludes with a proposed loss model which encompasses operation of large signal excitation over varying frequencies and DC biases.

For Nana

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Acknowledgments

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Chapter 1

Introduction

NASA's More Electric Aircraft (MEA) project was developed to prioritize electrification in our growing age of transportation access. Objectives of this aircraft design can lead to a 80% reduction in NOx emissions, 60% reduction in fuel consumption as well as 71 dB reduction in noise [1]. Fig. 1.1 shows a concept for the X-plane, a hybrid electric solution.

High power specific density of the electric drive train is a limiting factor for enabling MEA, therefore it is necessary to develop lightweight motors with high specific power. One such motor [9, 10] uses a 20 pole outer rotor permanent magnet synchronous machine to achieve high specific power while remaining lightweight. As opposed to typical motor designs, this motor has low inductance due to its outer rotor configuration. Low inductance requires additional filtering on the inverter to reach low total harmonic distortion (THD) on the motor. Additional filtering can increase the size and weight of the system, so instead a nine-level flying capacitor multilevel (FCML) inverter was developed utilizing its inherently low THD output and small filter size requirement [6, 11, 12]. Details of this work can be found in [6], where a peak power of 9.7 kW at 98.6% efficiency was demonstrated. The desired

Figure 1.1: NASA's More Electric Aircraft X-Plane Concept [1].

Table 1.1: Inverter performance requirements [8].

	Specific Power (kW/kg)	Efficiency (%)
Minimum	12	98
Target	19	99
Stretch	25	99.5

requirements of this inverter, set by NASA in [8], can be seen in Table 1.1.

While [6] demonstrated an inverter reaching the minimum efficiency, original models of this inverter design anticipated efficiency within the target region, shown in Table 1.1. To reach the target efficiency it is necessary to systematically evaluate the losses of every component within the inverter. The FCML in [6] uses GaN switches and extensive work was done in [13] to better characterize the dynamic losses of these switches. However, little previous work has been done to understand the losses of the capacitors, which are the main energy storage element of this converter [14].

Most conventional power converters (i.e. buck, boost, two-level inverters, etc.) primarily use capacitors as filtering elements. Filter capacitors are large with low equivalent series resistance (ESR) and low losses. Typically, these capacitors contribute negligible amount of losses to the overall power loss of the converter. In the FCML converters recently proposed, [6, 11, 12, 15–17], to achieve high power density, the capacitors experience high currents and high voltage bias, which can yield increased power loss that comprise a non-negligible portion of the total losses. Therefore, this work will investigate how to model and better understand these losses.

The rest of this thesis will be organized as follows. Chapter 2 provides background information on multilayer ceramic capacitors, detailing their operation and losses. Chapter 3 explains different characterization techniques, explaining why an oil-based calorimetric approach was taken. Chapter 4 provides detail of the calorimetric setup used in this study, including careful techniques to reduce the error. Chapter 5 provides a summary of the calorimetric experimental results, explaining the trends discovered. Chapter 6 provides an electrical method and results for investigating losses at lower frequencies. Chapter 7 derives and explains a new model for Class II MLCCs which allows for understanding of losses at any operating condition. Chapter 7 also returns to the nine-level FCML MEA in [6] to understand how the introduced model effects the expected losses. Finally, Chapter 8 concludes the thesis and explains future work.

Chapter 2

Background on Multilayer Ceramic Capacitors

Multilayer ceramic capacitors (MLCCs) are a key enabling component for high density power converters due to their high energy storage capabilities. Commercially available MLCCs have energy storage densities which are up to three orders of magnitude higher than commercially available inductors [18]. Fig. 2.1 shows a comparison of an MLCC and an inductor, both of which have the same energy storage, determined by Eqn. 2.1 and Eqn. 2.2 respectively.

$$E_{capacitor} = \frac{1}{2}CV^2 \tag{2.1}$$

$$E_{inductor} = \frac{1}{2}LI^2 \tag{2.2}$$

This comparison illustrates that utilizing capacitors as the primary energy storage device in power converters can enable increased converter power density [12, 16, 19, 20]. Recent advances in hybrid [21] and resonant [22–24] switched capacitor power converters, as well as various multilevel topologies [15,25,26] have led to increased focus on capacitor-based power

Figure 2.1: Size comparison of inductor and MLCC with the same energy density storage. Components are not to scale, but are to relative scale for comparison purposes.

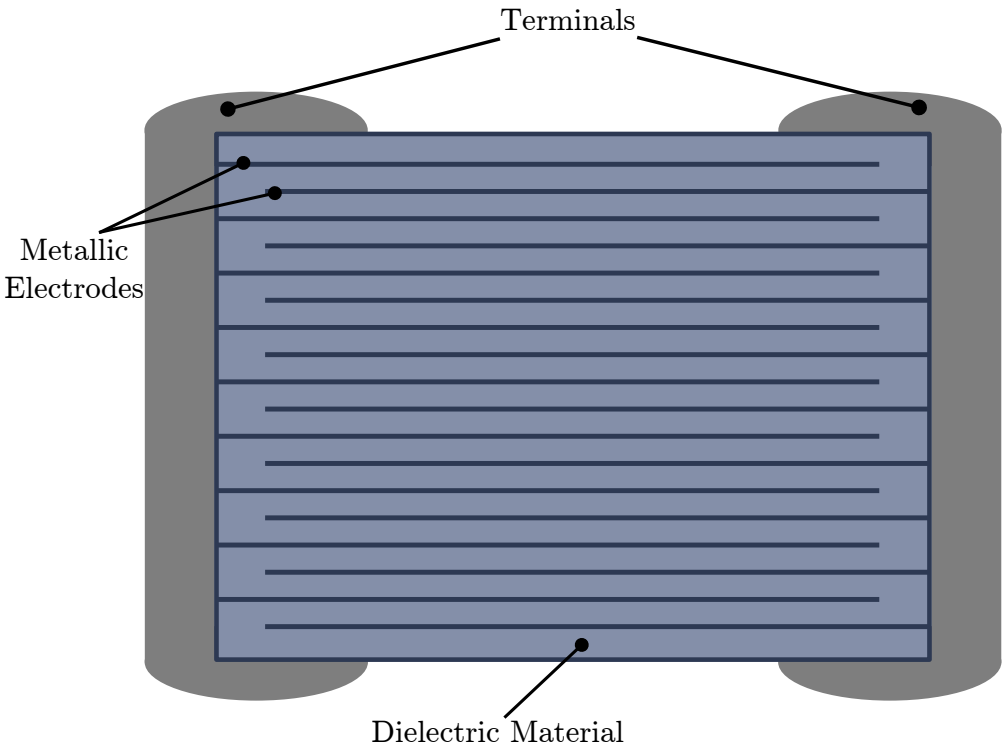

Figure 2.2: Composition of a basic multilayer ceramic capacitor.

converter architectures, often with MLCCs as the primary energy storage/transfer elements. To fully capitalize on the potential benefits of MLCCs, it is important to understand and model their energy storage and loss characteristics.

Capacitor Introduction

MLCCs are composed of several interwoven parallel plates, with a dielectric spaced throughout, which is shown in Fig. 2.2. Capacitance is defined in Eqn. 2.3 where parameter ϵ is the electrical permittivity of the dielectric, A is the area of the electrodes and d is the distance between the electrodes [2]. MLCCs offer high capacitance because the interwoven electrodes decrease the distance between electrodes as well as increasing the area of the electrodes. Since energy is defined by Eqn. 2.1, the increased capacitance leads to an increased energy density.

$$C = \frac{\epsilon A}{d} \tag{2.3}$$

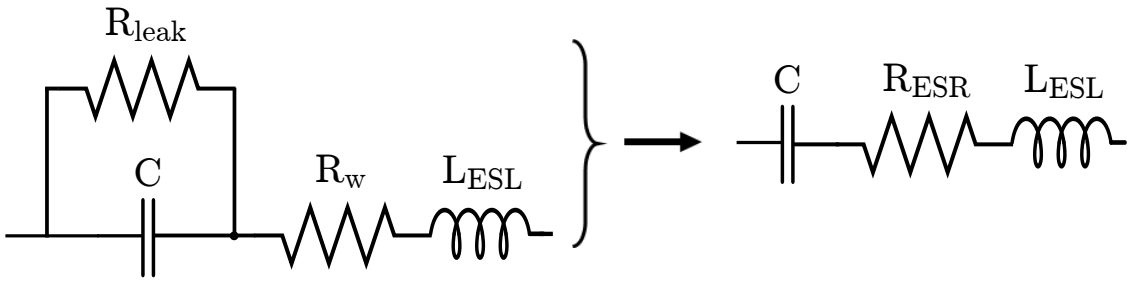

Figure 2.3: Standard capacitor model simplified [2].

MLCC Model

A commonly used capacitor model can be seen in Fig. 2.3. The electrical losses in termination resistance and series resistance of the dielectric are represented by R_w. The leakage losses are modeled as R_{leak}. These two resistances can be effectively combined to equal one equivalent series resistance (ESR) [2]. The real losses of the capacitor can be approximated by Eqn. 2.4.

$$P_{loss} = I_{rms}^2 R_{ESR} \tag{2.4}$$

The ESR of a MLCC depends on termination resistance, resistance within the dielectric and hysteresis losses. The resistance of the dielectric varies with large voltage swing as well as DC bias and temperature [27]. Note the model also includes a series inductance, L_{ESL} which is due to the inductance of the termination and composition of the MLCC.

Based on the simplified model shown in Fig. 2.3, the series impedance of an MLCC can be described as the sum of the impedance of the capacitor, equivalent inductance and resistance, shown in Eqn. 2.5.

$$Z_{MLCC} = j\omega L_{ESL} + \frac{1}{j\omega C} + R_{ESR} \tag{2.5}$$

The relationship between frequency and magnitude of the impedance is displayed in Fig. 2.4. The impedance reaches a minimum at self-resonance. At this point the impedance is equal to the ESR of the MLCC. The self-resonance frequency is defined in Eqn. 2.6.

$$f_{reson} = \frac{1}{2\pi\sqrt{L_{ESL}C}} \tag{2.6}$$

MLCC Comparison

Most MLCCs used in power electronics fall into the category of Class I or Class II capacitors. Class I MLCC's dielectrics are composed of paraelectric materials which are stable over temperature and bias. However, Class I MLCCs have lower energy density than Class II MLCCs [19]. Class II MLCC's dielectrics are composed of ferroelectric materials, mainly barium titanate, which allow for extremely dense energy storage, due to their high

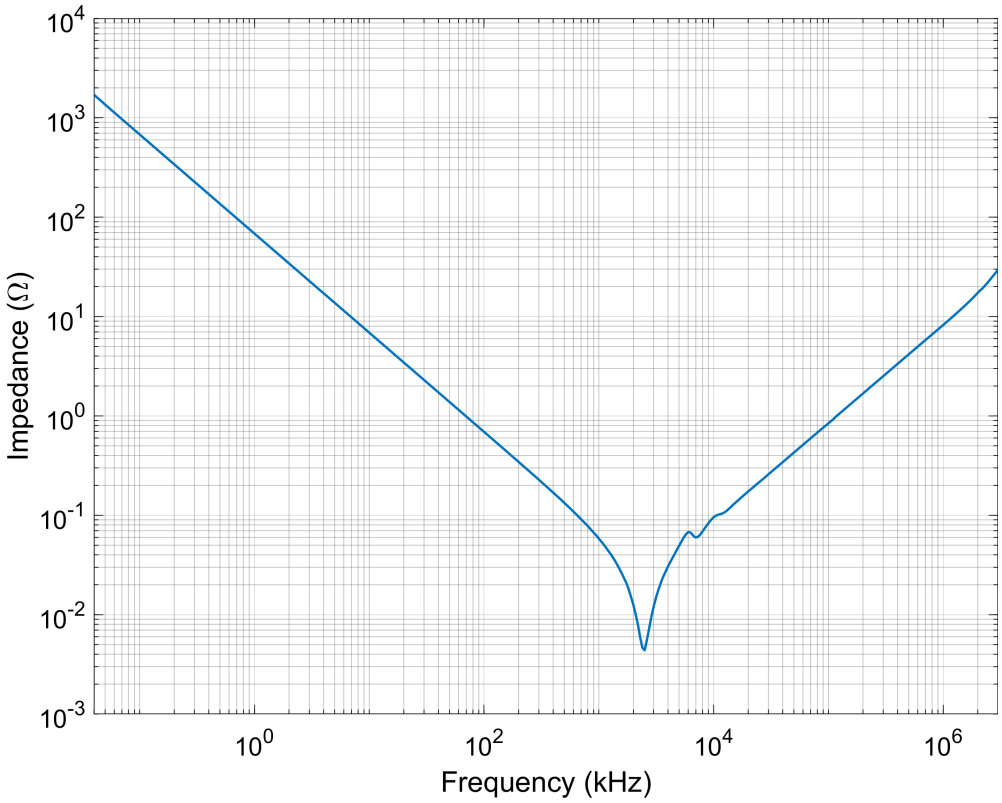

Figure 2.4: Impedance and frequency relationship of a Class II MLCC [3].

permittivity. However, these ferroelectric materials exhibit changes in permittivity due to realignment of electric dipoles within the material. The change in permittivity results in changes in the capacitance and ESR of the capacitors [28]. The decrease of capacitance by up to eighty percent at full DC voltage bias, an example of which is shown in Fig. 2.5, is due to the dipole realignment. The dipole realignment in Class II dielectrics is affected by four main operating conditions: Frequency, temperature, DC bias and AC amplitude.

Recently released Ceralink MLCCs are composed of a PLZT, lead-lanthanum-zirconate-titanate, dielectric which operates differently than Class I and Class II MLCCs. This dielectric is anti-ferroelectric, implying that as the DC voltage increases the capacitance also increases. This anti-ferroelectric behavior is attractive in hybrid switched capacitor topologies where high capacitance is often desired under high DC bias. Prior work characterized the losses of Ceralink capacitors at low frequencies and found that while the DC bias capacitance characteristics were favorable, the losses were greater than anticipated [27].

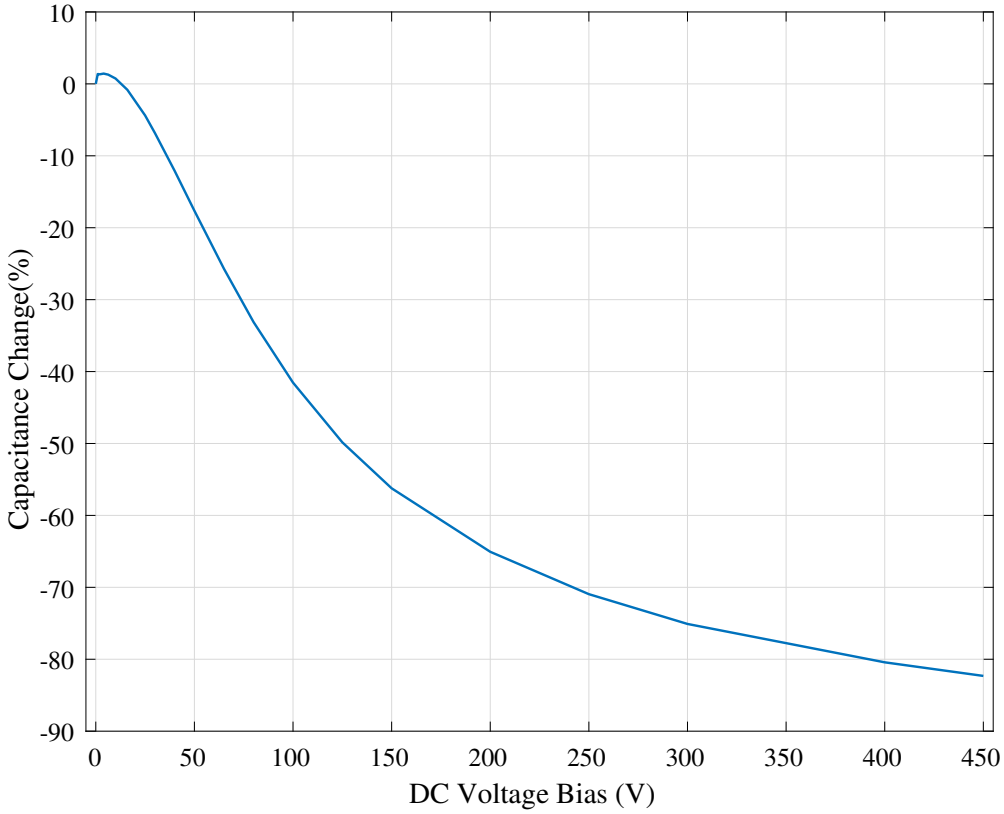

Figure 2.5: Change in capacitance with increased DC voltage bias [3].

2.1 Operating Conditions of Multilayer Ceramic Capacitors

Typical device data sheets only provide ESR values for small signal sinusoidal excitation at zero or near-zero voltage bias as a function of frequency. Fig. 2.6 shows an example of frequency versus ESR relationship for the chosen Class II MLCCs which will be studied in this work. These losses are dependent on a number of factors in addition to frequency; including DC bias, AC excitation and temperature. For switched capacitor power converter topologies, the capacitors within the circuit are typically operating near their DC bias rating, and excited with a quasi-square wave AC current instead of the sinusoidal waveform usually used to characterize devices. These quasi-square wave excitations have harmonics at higher frequencies than the fundamental, and therefore exhibit different loss characteristics than pure sinusoidal excitations. It is important to characterize the MLCCs with a realistic excitation to properly evaluate their loss characteristics. This work aims to provide a characterization of ceramic capacitor losses under large signal, square-wave current excitation over a range of DC bias levels, AC amplitudes, and at switching frequencies into the hundreds of kHz.

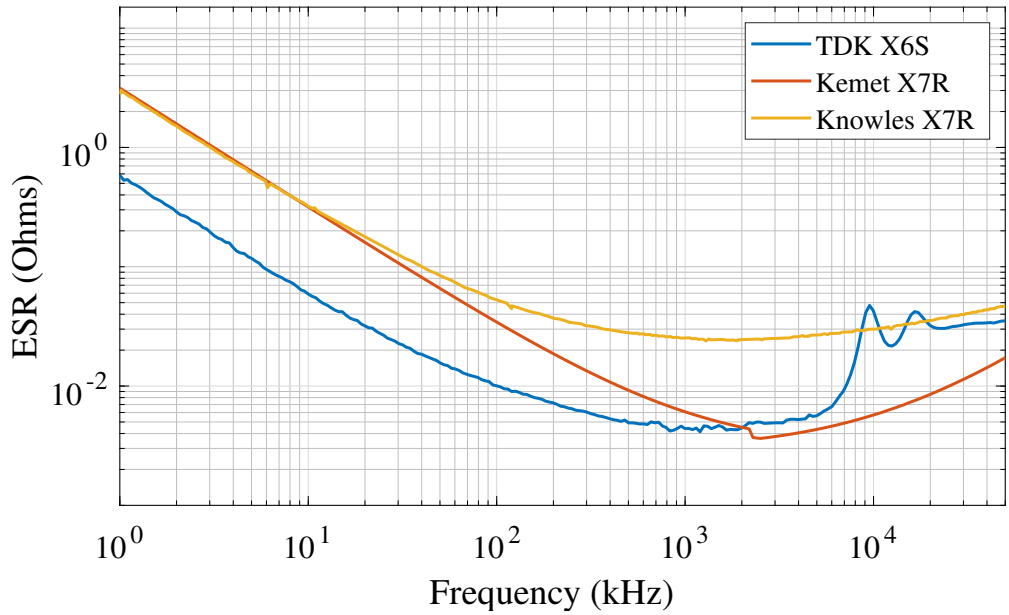

Figure 2.6: ESR of three Class II MLCCs over a range of frequencies, at 0 V bias small signal excitation (0.1 V_{RMS}) provided by the manufacturer [3] [4] [5].

2.2 Case Study: Flying Capacitor Multilevel Inverter

To understand the operating conditions described above it is helpful to consider an example converter. The nine-level FCML developed for NASA's MEA project, [6], is a useful tool to understand the MLCC operating conditions. The schematic of this converter is shown in Fig. 2.7. Two nine-level FCMLs are interleaved (i.e. operated with a 180 degree phase shift) to decrease output ripple and increase peak power capabilities. Fig. 2.7 also shows the operating conditions of a flying capacitor within the topology. This capacitor is referred to as flying because each capacitor (i.e. C_1, C_2, C_3, etc. marked in Fig. 2.7) is temporarily connected to different point in the circuit through the action of the switches. Moreover, each capacitor experiences a different DC voltage bias and ripple as discussed in the next section.

Flying Capacitor Operating Voltage

In the buck FCML inverter, each capacitor is nominally biased to a different voltage. The DC voltage on each capacitor is given by Eqn. 2.7, where N is the number of levels in the FCML (nine for this example). The parameter m is the specific level for the capacitor in question, ranging from 1 to N-2. Each set of high-side and low-side switches is referred to as a switching cell. There are a total of N-1 switching cells within the FCML. The switching cells are incremented starting at 1 on the output side of the converter, shown in Fig. 2.7.

$$V_{C_{FLY}} = \frac{mV_{DC}}{N-1} \tag{2.7}$$

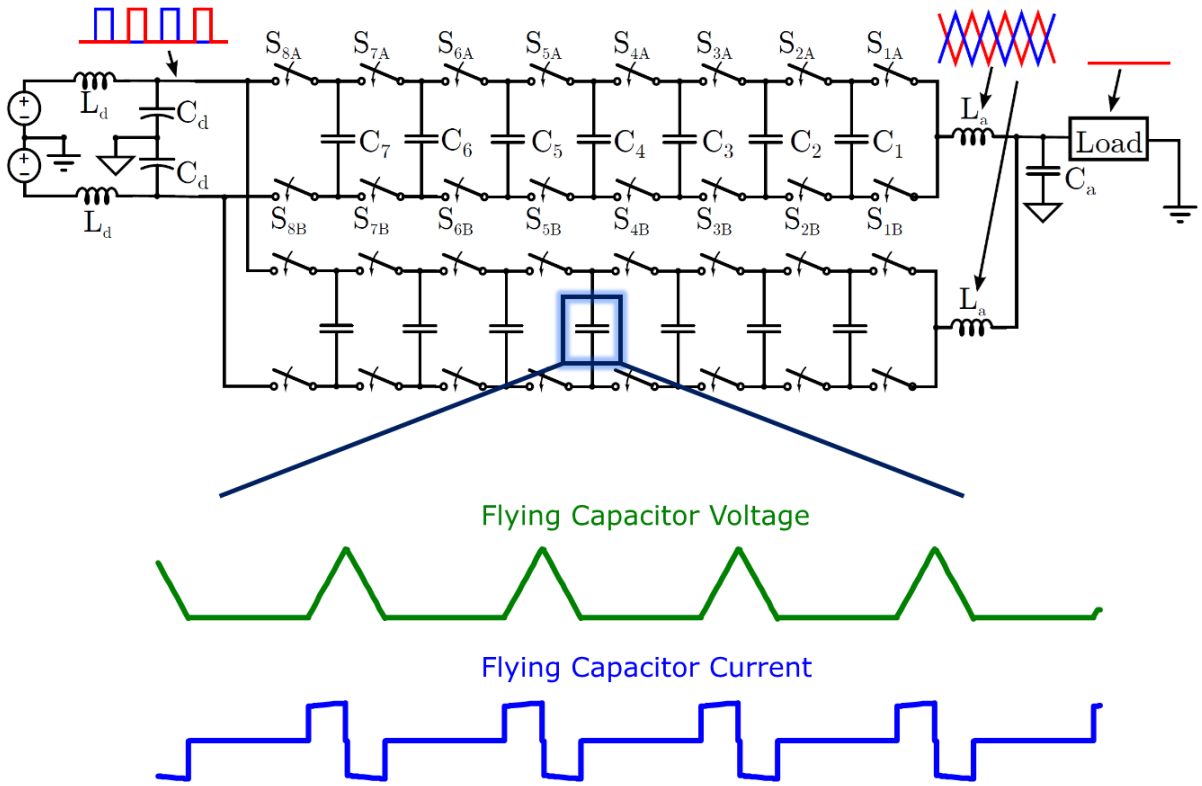

Figure 2.7: Schematic of nine-level FCML from [6]. Voltage and current waveforms of MLCC in FCML.

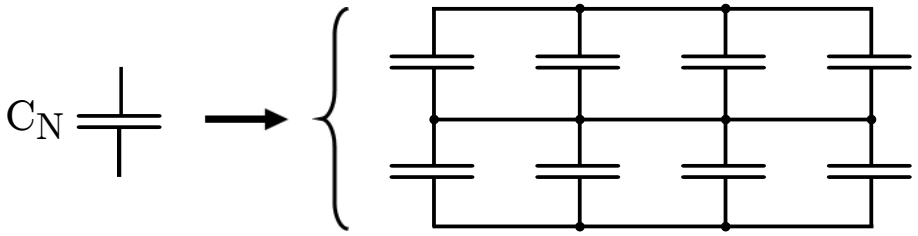

Figure 2.8: Actual implementation of capacitors in each switching cell.

For this example, the peak operating input voltage, V_{DC} is 1 kV, therefore the DC voltage bias of each level can be calculated using Eqn. 2.7 and is shown in Table 2.1.

Due to limited voltage ratings of commercially available capacitors, each level has two capacitors in series to reach the high DC voltage requirements. Therefore, the voltage of each capacitor is $\frac{1}{2}$ the voltage for each level stated in Table 2.1.

Level	DC Voltage Bias
1	125 V
2	250 V
3	375 V
4	500 V
5	625 V
6	750 V
7	875 V

Table 2.1: DC voltage bias on flying capacitors in 1 kV input 9-level FCML buck inverter.

Since the capacitor chosen for this converter is a Class II MLCC, the capacitance decreases with applied bias. In the highest biased switching cell, C_7 on Fig. 2.7, the voltage bias is 437 V DC. The capacitance is then approximately 20% of the 0 V bias capacitance, as shown in Fig. 2.5. To account for the reduced effective capacitance, it is necessary to increase the capacitance by placing four capacitors in parallel.

Due to these operating conditions, for each capacitor shown in Fig. 2.7, C_N, the actual implementation can be seen in Fig. 2.8, where there are a total of eight capacitors for each capacitor (i.e. C_1, C_2, C_3 etc.) shown in the schematic.

In addition to bias, each capacitor has a voltage ripple which has a triangular shape. This ripple can be calculated using Eqn. 2.8, where the voltage ripple of each capacitor is $V_{C_{FLY}}$. The current through the capacitor is $I_{C_{FLY}}$, and the switching frequency is f_{SW}. Since the capacitance changes with bias, this ripple value also changes for each level of the FCML.

$$\Delta V_{C_{FLY}} = \frac{I_{C_{FLY}}}{f_{SW} C_{FLY}} \tag{2.8}$$

Flying Capacitor Operating Current

Using phase shifted pulse width modulation (PSPWM) to control each switch allows for an output effective frequency of (N-1)*f_{sw}. This increase in effective frequency at the output allows for smaller output inductance. Each switch is operated with ϕ degrees of phase shift, defined in Eqn. 2.9 [17].

$$\phi = \frac{360}{N-1} \tag{2.9}$$

There are nine levels in this example FCML, thus the converter is operated with each switch set shifted 40 degrees from each other. This means each capacitor has current flowing for a total of 80 degrees per cycle, or $\frac{2}{9}$ of each switching period. Therefore, the RMS current through each flying capacitor can be found using Eqn. 2.10 [11].

$$I_{C_{FLY,RMS}} = I_{load}\sqrt{\frac{2}{9}} \tag{2.10}$$

Level Number	V_{Level}	V_{Cap}	C_{eff}	$\Delta V_{C_{FLY}}$	$\%Ripple$
1	125 V	62.5 V	3.27 μF	6.01 V	4.81 %
2	250 V	125 V	2.21 μF	8.89 V	3.56 %
3	375 V	187.5 V	1.65 μF	11.90 V	3.17 %
4	500 V	250 V	1.28 μF	15.34 V	3.07 %
5	625 V	312.5 V	1.10 μF	17.86 V	2.86 %
6	750 V	375 V	1.01 μF	19.41 V	2.59 %
7	875 V	437.5 V	0.75 μF	26.26 V	3.00 %

Table 2.2: Operating conditions of flying capacitors in nine-level FCML [6].

For peak operating conditions, the load current for each interleaved leg is approximately 20 A, therefore the $I_{C_{FLY,RMS}}$ is 9.42 A. For simplicity, a constant inductor current, I_{load} is assumed.

As stated above, to account for change in capacitance with voltage bias, each switching cell has four capacitors in parallel, which means the actual RMS current per capacitor is $\frac{1}{4}$ the total RMS current per leg. For this example, the RMS current for each MLCC is 2.35 A.

Summary of Flying Capacitor Operating Conditions

Table 2.2 shows a summary of the operating conditions of the flying capacitors in this converter. V_{cap} is the voltage across the capacitors in each level, which is $\frac{1}{2}$ the voltage bias of each level, since there are two capacitors in series. C_{eff} is calculated as the effective capacitance of each level taking into consideration the capacitance change due to voltage bias, described by Fig. 2.5, as well as the number of capacitors in series and parallel. The voltage ripple, V_{ripple} is found from Eqn. 2.8.

This example shows that the operating conditions from which the data sheets of MLCC losses are described, 0.1 V_{RMS} sinusoidal excitation, are not close to the operating conditions that these MLCCs are actually being used. In fact, the MLCC in this example has large voltage and current ripple, at high DC bias and high frequency. The rest of this thesis will aim to provide a procedure and results for characterizing the MLCC losses closer to the operating conditions under which the MLCCs are being operated. Chapter 7 will return to these operating conditions to explain the effective losses due to MLCCs in this FCML example.

Chapter 3

Comparison of Measurement Techniques

Illustrated in Chapter 2, the operating conditions of the MLCCs are not the ones shown on the data sheets. Therefore, a new technique to understand the losses of MLCCs under wide operating conditions is necessary. This chapter aims to evaluate different characterization techniques, on a bases of accuracy, to determine the best technique for this study.

3.1 Electrical Characterization Methods

Passive power electronic components are typically characterized using electrical measurement tools, such as impedance analyzers, because they are fast and accurate for small signal measurements. As the focus of this work is the evaluation of MLCC losses under large signal excitation (i.e. several amperes of current, and tens of volts of ripple) at high frequencies (i.e. hundreds of kHz), electrical measurements are more difficult, owing to the need for very high resolution over a wide amplitude range. To illustrate these constraints, it is helpful to consider the measurement resolution which can be achieved using a high resolution instrument, such as the WT3000 Yokogawa power analyzer [29]. Considering the conditions described previously for [6], where the MLCC has a voltage bias of 437 V DC and the current excitation of 2.35 A RMS, the range of measured instantaneous power *transferred* would be about one kilowatt. However, the expected measurement of power *loss* for typical values of capacitor ESR would be about 1 W. Given the accuracy of the power analyzer at frequencies in the hundreds of kHz, an uncertainty on the order of ± 10.2 W can be expected, even using a state-of-the-art power analyzer [29]. While AC coupled voltage measurements can help reduce the absolute accuracy requirements, electrical measurements remain challenging, owing to the wide frequency range and need for high precision.

3.2 Calorimetric Characterization Comparison

Since electrical characterization was deemed insufficiently accurate under these operating conditions, it is necessary to investigate a thermal method. Thermal loss characterizations observe the heat dissipated by the device under test (DUT) and then calculate losses from the temperature rise over a period of time. Several types of thermal characterization methods were considered for this study.

Heat Flux Sensor Characterization

A possible characterization method is to monitor the heat dissipated by the MLCC during excitation using a heat flux sensor. Assuming a flux sensor such as [30] is chosen, the assumed temperature accuracy is about ± 2 °C therefore the overall estimated accuracy for the MLCC ESR measurement would be ±0.645 mΩ, using the accuracy equations detailed in Chapter 4. Moreover, added setup complexity arises with the implementation of a heat flux sensor. Heat is dissipated from the MLCC in all directions, which means that mounting a heat flux sensor directly to the MLCC does not capture all of the losses. Another option is to create a setup where air flows across the MLCC then the air temperature rise is measured with the heat flux sensor. This would require an advanced setup where the air is precisely forced and measured. Lastly, an option is to implement heat flux sensors in the oil-based calorimetric study explained below. This would allow the heat flux sensor to capture heat dissipated through convection in all directions. This is a simpler setup than the forced air method. The overall accuracy is less than the accuracy of the resistive temperature devices (RTDs) detailed in Chapter 4. Therefore, this method will not be implemented in this study.

Thermal Camera Characterization

Similar to the heat flux sensor method, thermal cameras have been implemented to measure loss of passive components [27]. This method yields the same accuracy as the heat flux sensor since the methods have the same estimated temperature accuracy [31]. This method adds high cost. A thermal camera of this high accuracy is usually ten thousand dollars or more. In addition to cost, using a thermal camera requires careful attention to the emissivity of the materials being tested. The emissivity of a material is a measurement of the material's ability to emit electromagnetic waves [32]. Emissivity is defined as a ratio from zero to one, where one is a black body which emits maximum intensity at a given temperature. The emissivity of a material must be known to accurately determine the temperature of the DUT to determine device losses. In the case of an MLCC, the body and terminals will have different emissivity from the printed circuit board (PCB). In typical studies, the PCB is coated to replicate a black body which becomes a reference point for emissivity. Without precisely knowing the emissivity of the DUT, the accuracy of this method further decreases. Therefore, this method will not be employed in this study.

Oil-based Calorimetric Characterization

Lastly, the oil-based calorimetric characterization requires placing the DUT in a bath of oil and observing the temperature rise of the oil over time. This method is proven to be accurate to approximately ± 0.088 mΩ, derived in Chapter 4. Since this method has the least amount of error, it was implemented in this study.

3.3 Calorimetric Theory

The principle of a calorimetric measurement is to calculate power loss through the observed thermal energy dissipated over a period of time. It has been shown that an oil-based calorimetric study is both cost effective and accurate for measuring losses up to 30 W in magnitude [33]. For this study, the DUT was placed in an oil bath and the temperature rise of the oil was measured. During testing, both a DC voltage bias and a large signal square wave current was applied, this electrical excitation is further described in Chapter 4.

Heat Transfer Theory

In an oil-based calorimetric characterization, the primary mode of heat transfer is convection. Convection heat transfer occurs as conduction between a surface and a moving fluid, in this case oil [32]. Eqn. 3.1 defines the relationship between the power dissipated and the change in the temperature of the oil, derived from convection heat loss calculations.

$$\mathrm{P_{diss}} = \frac{1}{\tau}(k_{oil}\Delta \mathrm{t} + \int_0^{\tau} \frac{\mathrm{t}_{oil} - \mathrm{t}_{amb}}{R_{TH}} d\tau) \tag{3.1}$$

Where τ is the time for which the temperature was observed and t is the temperature measured. The oil bath is characterized by k_{oil} which is the product of the specific heat ($\frac{J}{gK}$), density ($\frac{g}{cm^3}$) and volume of oil used (mL). The parameter k_{oil} determines how quickly the temperature of the oil rises as convection occurs between the oil and DUT. Parameter R_{TH} ($\frac{K}{W}$) is the thermal impedance between the oil and the ambient. This parameter is important as it relates the amount of power dissipated but not captured by the temperature measurement. An accurate characterization of this impedance is a critical step in ensuring the accuracy of the calorimetric measurement, the method for accurately determining the setup's thermal impedance will be detailed in Chapter 4.

Constraints of an Oil-based Calorimetric Study

While the oil-based study was chosen, it also has several drawbacks. First, it is necessary to strictly constrain the ambient temperature. As shown in Eqn. 3.1, if the temperature of the ambient, t_{amb}, changes over the course of a test, the calculated power dissipated will also change. To mitigate this constraint, a temperature chamber was utilized to keep a constant ambient temperature, listed in Table 4.2. Since this adds cost to the overall setup,

an approximate measurement alternative would be to implement a thermally insulated box as the ambient, i.e. a cooler, which is also resistant to changes in the ambient temperature.

Another constraint of this setup is the increased time each test takes when compared to the previously listed methods. Each calibration test, described in Chapter 4 takes up to ten hours since the oil must come to thermal equilibrium. After performing the calibration tests, each test takes an hour, and then time is allowed between each test to allow the oil to come to equilibrium with the ambient, which can take anywhere from one to seven hours depending on the heat dissipated during testing. Since the majority of the testing time is inactive, i.e. no person is having to take measurements, it is easy to run the tests in the background, provided safety is prioritized and the setup is not left unattended when operating at high power.

Chapter 4

Calorimetric Study

A calorimetric, oil-based, study was chosen due to high accuracy. However, the results are only determined to be accurate if the calorimetric setup is designed carefully. The following chapter details the construction of the calorimetric test setup and the details of the expected accuracy.

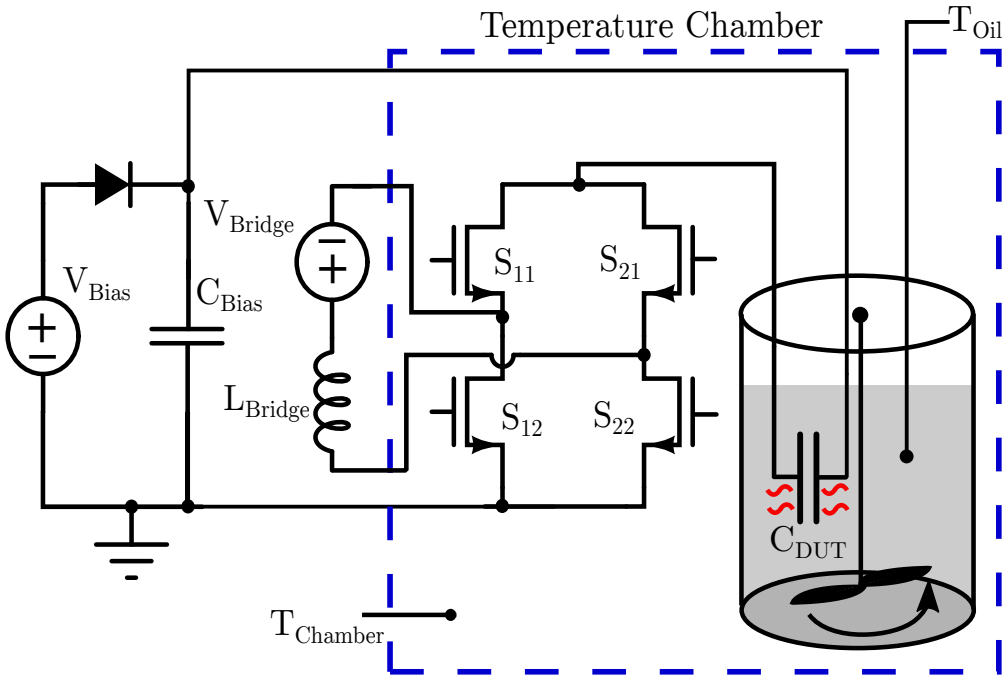

Figure 4.1: Electrical excitation circuit and thermal setup for calorimetric testing.

Label	Instrument
Switches	GaN Systems GS61008T
Gate Driver/Isolator	SI8275GB-IS1
V_{Bias}	Magna-Power DC Supply
Microcontroller	TI C2000

Table 4.1: Components used in electrical excitation circuit.

4.1 Theory and Design of Electrical Excitation

To test the MLCCs under realistic operating conditions, like those described in Chapter 2, a test circuit was created which could provide an adjustable DC voltage bias, excitation frequency and AC amplitude. The square wave replicates the operating conditions of the capacitor in a realistic hybrid non-resonant switched capacitor power converter more accurately than a sinusoid which is typically used for testing. This is consistent with the operating conditions discussed in Chapter 2, shown in Fig. 2.7. Special consideration was taken to design an electrical excitation which would not require large amounts of power to test, this solution recycles the energy of the DUT between each switching cycle allowing for reduced total electrical power required for testing.

As shown in Fig. 4.1, the capacitor voltage bias can be adjusted independently of the current excitation by varying the supply labeled V_{bias}. The frequency of the excitation can be controlled by adjusting the gate drive signals of the H-bridge; which are controlled with a microcontroller. The AC current amplitude can be adjusted by controlling the current limited power supply labeled V_{bridge}. Fig. 4.1 also shows a schematic diagram of the implemented electrical circuit along with its physical relationship to the DUT, oil reservoir and temperature chamber.

It is worth noting that although the switches are capable of handling large current, the voltage stress across the switches is relatively small. GaN systems top side cooled devices were used due to their low R_{ds}. Since the GaNs are top side cooled, more of the heat was dissipated into the temperature chamber instead of the beaker which contains the DUT.

Sections of the excitation circuit are placed outside the temperature chamber to isolate any extra sources of heat. However, the H-bridge circuit is placed directly on top of the beaker and close to the DUT, to reduce stray inductance in series with the capacitor. Careful layout was completed to ensure small inductive loops within the H-bridge. The layout is detailed in Appendix B. Shown in Fig. 4.2 is an annotated photograph of the H-bridge PCB and power components. Fig. 4.3 shows the resulting voltage and current waveforms of the DUT created from the excitation circuitry.

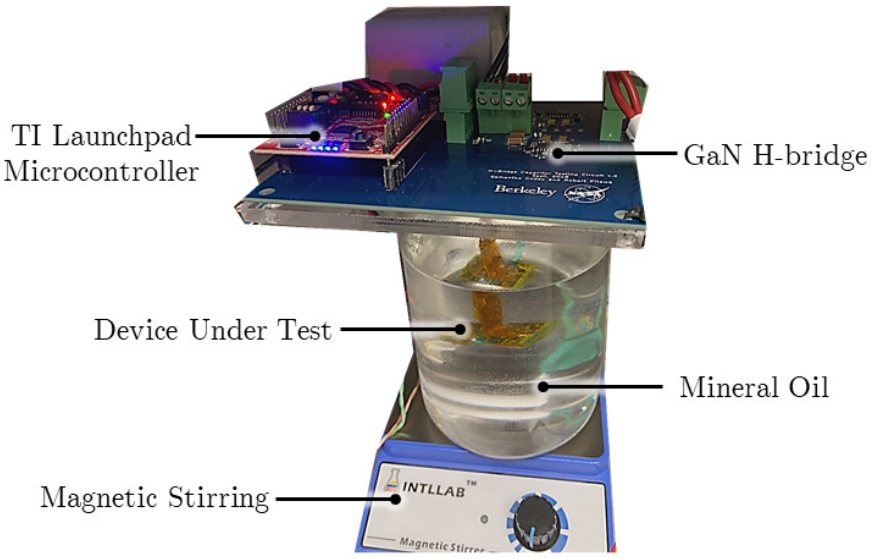

Figure 4.2: Picture of electrical excitation PCB mounted on top of beaker with DUT and stirring setup.

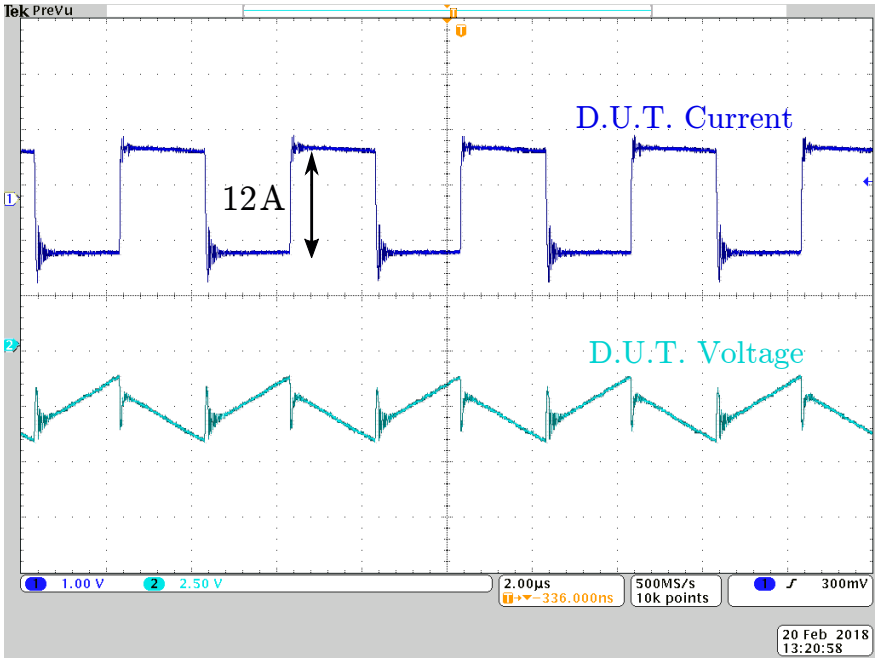

Figure 4.3: MLCC DUT voltage and current measured at 250 kHz (5A/V).

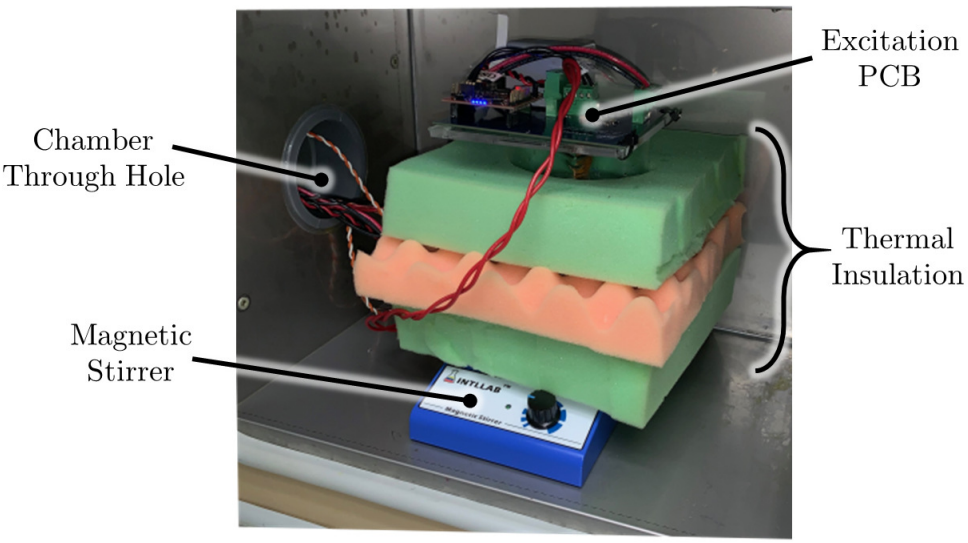

Figure 4.4: Calorimetric setup where the beaker is placed in insulation. The entire system is placed in the temperature chamber and the power is fed through the side of the chamber.

4.2 Calorimetric Setup

Structural design

Creating high thermal impedance between the oil reservoir and the ambient environment is necessary for high measurement accuracy. A higher thermal impedance allows for a more accurate measurement of dissipated loss since less thermal energy is lost from the system during the measurement. A high thermal impedance was created by surrounding the oil reservoir with three layers of thermal isolation. The isolated beaker was placed in a thermal chamber which was set at a constant twenty-three degrees Celsius, shown in Fig. 4.4. The thermal chamber and other necessary components of the calorimetric setup are listed in Table 4.2.

Temperature Measurements

The accuracy of the overall loss measurement is dependent on the accuracy of the temperature measurements. Resistive temperature devices (RTDs) were chosen for this study due to their improved accuracy for temperature measurements over a small temperature range as opposed to thermo-couples. Details of the accuracy can be found below. The temperature of the oil and chamber were all measured every five seconds using a Fluke Hydra DAC controlled through custom LabVIEW and MATLAB software. To provide even heat distribution within the oil bath, the beaker was stirred using a magnetic stirring apparatus, shown in Table 4.2.

Table 4.2: Devices used in calorimetric setup.

Label	Instrument
Temperature Chamber	TPS Tenney TJR-A-WF4
Data Recording Device	Fluke Hydra DAC
Magnetic Stirrer	INTLLAB MS-500
RTDs	TE Connectivity NB-PTCO-152 [34]

4.3 Calibration Methods

In this investigation, the thermal impedance was determined over a series of calibration tests. During calibration, the DUT was replaced with a precise resistor, 3.1 $m\Omega$, whose value was chosen to dissipate approximately the same amount of power as expected by the MLCCs tested. The calibration runs were done at DC operating conditions to increase the accuracy of the electrically measured power dissipation. The current and voltage of the DUT was measured through Kelvin sensing to accurately determine the power dissipation. The calibration was run in the calorimetric test chamber multiple times, with power levels comparable to those used during capacitor testing. In each test, the temperature of the oil was allowed to reach steady-state. An example calibration run can be seen in Fig. 4.5, where thermal equilibrium is reached around 250 minutes. The thermal impedance was then calculated to be the ratio of the temperature difference between the beaker of oil and the controlled external temperature divided by the continuous power dissipation of the resistor, seen in Eqn. 4.1.

$$R_{TH} = \left.\frac{t_{oil} - t_{amb}}{P_{diss}}\right|_{steady-state} \tag{4.1}$$

4.4 Calorimetric Testing Procedure

For each calorimetric test, the excitation circuit was assembled and placed inside the temperature chamber. Two RTDs were placed inside the temperature chamber and two inside the beaker of oil. The temperature chamber was then sealed and set to a constant twenty-three degrees Celsius, this temperature was chosen to match the ambient temperature of the lab. The temperature chamber was used to eliminate variations in ambient temperature which occur over the course of the day due to HVAC management.

At the beginning of each test the chamber was turned on and allowed to reach thermal equilibrium. Once the inside temperature of the chamber was stable, the DC bias and AC excitation were applied to the DUT. The temperature reading from each RTD was then collected every five seconds over the course of the test. Each calorimetric test was performed for approximately one hour to ensure even mixing and to increase the overall accuracy.

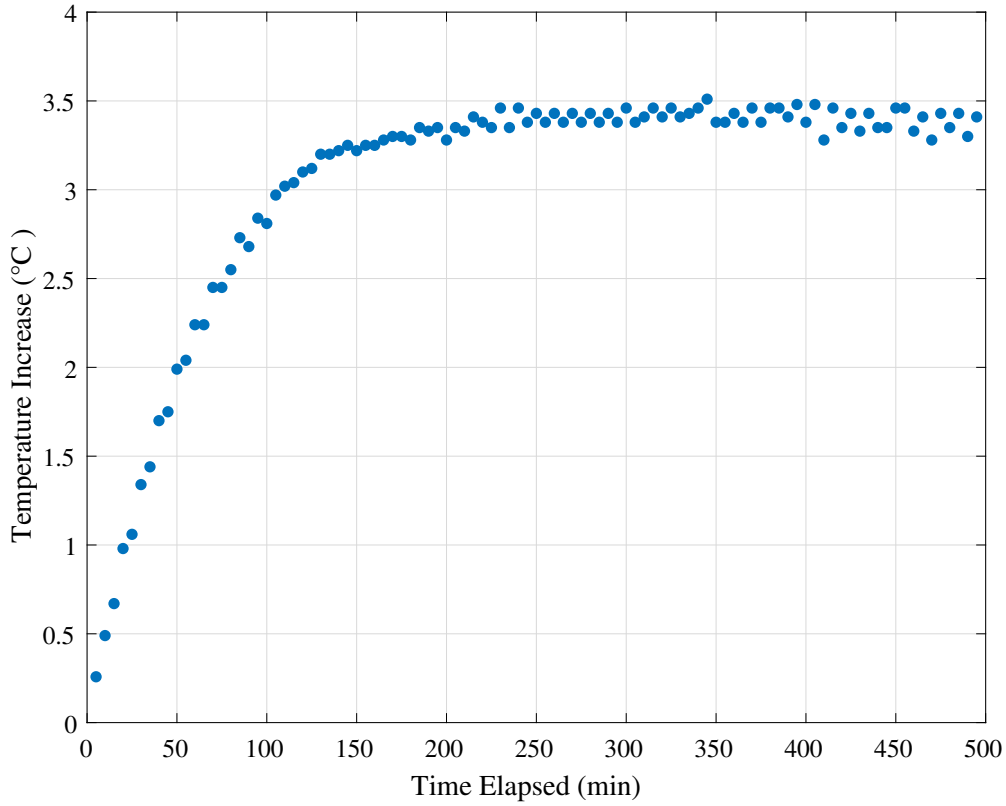

Figure 4.5: Calibration of calorimetric setup utilizing precise resistor in place of DUT to calculate thermal impedance of setup.

Additional time was allowed between each test to allow the system to reach equilibrium with the ambient temperature.

After the test was completed, the temperature data was used to calculate the power dissipated by the DUT, using Eqn. 3.1. Then the ESR was calculated by dividing the power by the squared RMS current.

4.5 Measurement Error Analysis

Temperature Measurement

The RTDs used in this study, shown in Table 4.2, are accurate to ±0.1% of the resistive measurement [34]. The nominal resistance for the RTDs is 100 Ω at 0 $°C$. The maximum resistance measured in this study was 114 Ω. Therefore, the maximum absolute error is ±0.114Ω. To relate temperature with measured resistance, the Steinhart method [35] was investigated. This method uses three known values, freezing, boiling and room temperature to create the relationship between resistance and temperature. However, it was determined

that the Steinhart method is only as accurate as the ability to measure the temperature accurately at the three calibration measurements. Specifically, it was extremely difficult to measure the temperature at room temperature accurately, thus using the data sheet calibration was proved to be more precise. Given in [34] the relationship between temperature and resistance yields an absolute error of $\pm 0.1425^{\circ}C$ for each temperature measurement. Since each temperature measurement is duplicated, the absolute error for the ambient and oil temperature is $\frac{\pm 0.1425^{\circ}C}{\sqrt{2}}$ or $\pm 0.1^{\circ}C$ [36].

Calibration Measurement

The calibration determined the thermal resistance R_{TH}, of the set-up. This was found as the ratio of the temperature rise and the continuous power generated shown in Eqn. 4.1. The power was measured with a Yokogawa WT310, a high precision power analyzer, and was determined to be accurate to 0.1% of the measured power [37]. The absolute accuracy of each calibration run is determined by Eqn. 4.2. Here Δ represents the absolute accuracy of the applied term [36].

$$\Delta R_{TH} = R_{TH}\sqrt{(\frac{\Delta t}{t})^2 + (\frac{\Delta P}{P})^2} \tag{4.2}$$

For an example calibration run, the temperature raise measured was approximately $3^{\circ}C$, and the power dissipated was 1 W. Applying these values to Eqn. 4.2, yields an accuracy of $\pm 0.336\ \frac{K}{W}$. The calibration was completed three times, which means the accuracy is divided by $\sqrt{3}$ [36]. Therefore, the final estimated absolute accuracy of R_{TH} is $\pm 0.194\ \frac{K}{W}$.

Power Dissipation Measurement

The power dissipated was determined by Eqn. 3.1. The integral term in Eqn. 3.1 can be rewritten as a summation of discrete points as shown in Eqn. 4.3. Parameter n is the total number of data points taken during a test, typically forty.

$$\mathrm{P_{diss}} = \frac{1}{\tau}(k_{oil}\Delta \mathrm{t} + \sum_{i=1}^{n} \frac{\tau}{n} \frac{\mathrm{t}_{oil} - \mathrm{t}_{amb}}{R_{TH}}\Big|_{\frac{\tau}{i}}) \tag{4.3}$$

As each measurement was performed for a long period of time to reach steady-state, any error in the time measurement was found to be negligible to the overall measurement error. In addition, the accuracy of the k_{oil} measurement is difficult to approximate since values were given on data sheets. Taking these simplifications into account the absolute accuracy of the dissipated power can be found with Eqn. 4.4.

$$\Delta P_{diss} = \frac{P_{diss}}{\sqrt{n}}\sqrt{(\frac{\Delta t}{t})^2 + (\frac{\Delta R_{TH}}{R_{TH}})^2} \tag{4.4}$$

ESR Measurement

The ESR was calculated by dividing the power dissipated by the squared RMS current. The RMS current was accurate to ±0.015 A, for frequencies between 100 kHz and 500 kHz as described in [37]. The absolute accuracy of the ESR is then defined by Eqn. 4.5 [36].

$$\Delta ESR = ESR\sqrt{(\frac{\Delta P_{diss}}{P_{diss}})^2 + (2\frac{\Delta I_{RMS}}{I_{RMS}})^2} \tag{4.5}$$

The accuracy of the power dissipated is dependent on the temperature measurement as well as the current measurement for each data point. The accuracy was determined for each data point and is shown as error bars for each result in Chapter 5.

Chapter 5

Experimental Results

Shown in Table 5.1, five different MLCCs were chosen to evaluate calorimetrically. Three Class II MLCCs were chosen due to their high energy density: One X6S type and two X7R type MLCCs. X6S and X7R are descriptors given to characterize the dielectric used in the MLCC. The difference between a X6S and X7R MLCC is the temperature rating of the device. X6S devices are rated for $-55°$ C to $105°C$ with 22% tolerance. The X7R MLCCs are rated for $-55°$ C to $125°C$ with 15% tolerance.

A Ceralink MLCC was similarly tested due to high energy density, and curiosity of the performance of the anti-ferroelectric dieletric compared to the Class II MLCCs. Lastly, a Class I capacitor was tested, type C0G. This MLCC was chosen to serve as a control since it is known that the paraelectric dielectric is more stable across operating conditions. It was hypothesized that the Class I MLCC would not exhibit loss changes with differing operating conditions, due to the stability of the dielectric.

It is important to note that the results of this study are not intended to show a comparison of performance between capacitors. As can be seen in Table 5.1, the MLCCs tested have varying temperature characterization, voltage rating and capacitance, and therefore would be suitable for differing applications. Instead, the goal of this study was to better understand the impact of operating conditions on ESR by testing varying MLCCs.

Table 5.1: Experimentally evaluated capacitors.

No.	Type	Manufacturer	Voltage	Cap	Part Number
I	X6S	TDK	450 V	2.2 μF	C5750X6S2W225K [38]
II	X7R	Knowles	630 V	1 μF	2220Y6300105KETWS2 [4]
III	X7R	Kemet	500 V	1 μF	C2220C105MCR2L [7]
IV	Ceralink	EPCOS	500 V	1μF	B58031U5105M062 [39]
V	C0G	TDK	630 V	0.1 uF	C5750C0G2J104J280KC [38]

5.1 DC Bias Calorimetric Results

The impact of DC bias on the MLCC losses was investigated first. For these tests, the current amplitude was kept constant and the bias voltage was adjusted, by changing V_{Bias} in Fig. 4.1. For each capacitor, three different frequencies were evaluated at five different voltage biases, to understand the relationship between the frequency and bias effect on losses.

The first MLCC tested was TDK's X6S, Cap I from Table 5.1. The results of DC bias on ESR can be seen in Fig. 5.1. The black star is shown as reference for small signal data provided on the data sheet, which is measured at 0 V bias and 0.1 V_{RMS} sinusoidal excitation. The small signal data point is comparable with the calorimetrically tested value at 0 V bias, which serves as a validation of the measurement technique. The data was tested at 6 A RMS, and the frequency was varied from 125 kHz to 500 kHz, to mimic realistic switching frequencies in hybrid switched capacitor converters. The error bar on each data point was calculated from Eqn. 4.5.

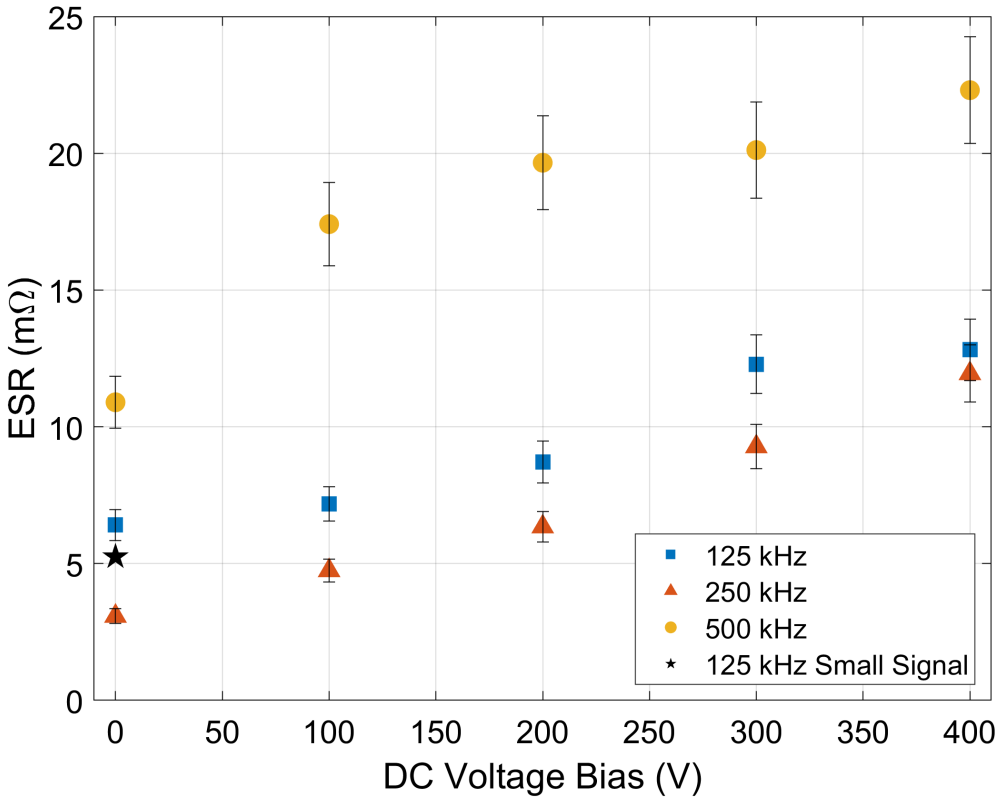

Figure 5.1: TDK X6S, Cap I from Table 5.1, effect of DC bias on ESR. The black star represents the small signal ESR from the data sheet [3].

Fig. 5.1 shows that with increased DC bias the ESR also increases. The relationship is approximately linear, displaying the same trend at each measured frequency. It should be noted that the ESR for 250 kHz is lower than 125 kHz and 500 kHz across all tested

DC biases. If this trend is compared to the ESR and frequency relationship presented in Fig. 2.6 it follows that the 250 kHz ESR should be lower than the 125 kHz measured ESR, because 250 kHz is closer to self-resonance. However, the 500 kHz ESR is greater than both of the other measured frequencies, which does not follow trends seen in Fig. 2.6. This is most likely due to the impact of the third harmonic of the 500 kHz excitation. Since the excitation is a square waveform, there are odd harmonics present, and the third harmonic of 500 kHz, which would fall at 1.5 MHz, is after the capacitors self-resonance point. After self-resonance, the ESR of the capacitor increases, which would account for the increased ESR at these data points.

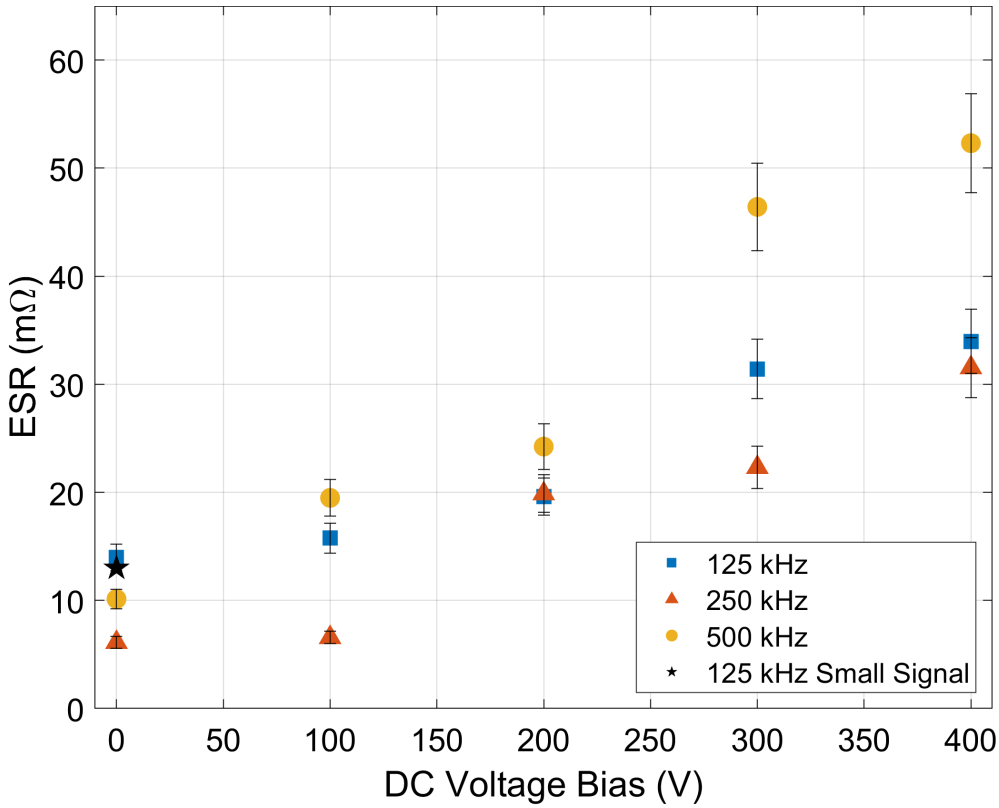

Figure 5.2: Knowles X7R, Cap II from Table 5.1, effect of DC bias on ESR. The black star represents the small signal ESR from the data sheet [4].

The Knowles' X7R, Cap. II from Table 5.1, was tested under the same conditions as discussed for Cap. I. The results can be seen in Fig. 5.2. The small signal ESR attained from the data sheet is also plotted in Fig. 5.2, as the black star, and is within the margin of error of the calorimetrically measured ESR under large signal operating conditions. Similar to Fig. 5.1, the ESR increases with increased DC bias. However, there are a few differences in trend between the two MLCCs. At low bias the 125 kHz test had higher loss than the 500 kHz tested data. At all biases except 0 V, the frequency relationship follows the same

as Cap. I. This is again assumed to be due to third harmonic falling after the point of self-resonance. As can be seen in Fig. 2.6, the self-resonance point for Cap. I and II are similar. In general, the ESR of Cap. II is higher than that of Cap. I. This is also true for the small signal data provided by the manufacturer, shown in Fig. 2.6. While there are some differences between these two capacitors, the overall trend of increased ESR with increased bias holds for both MLCCs.

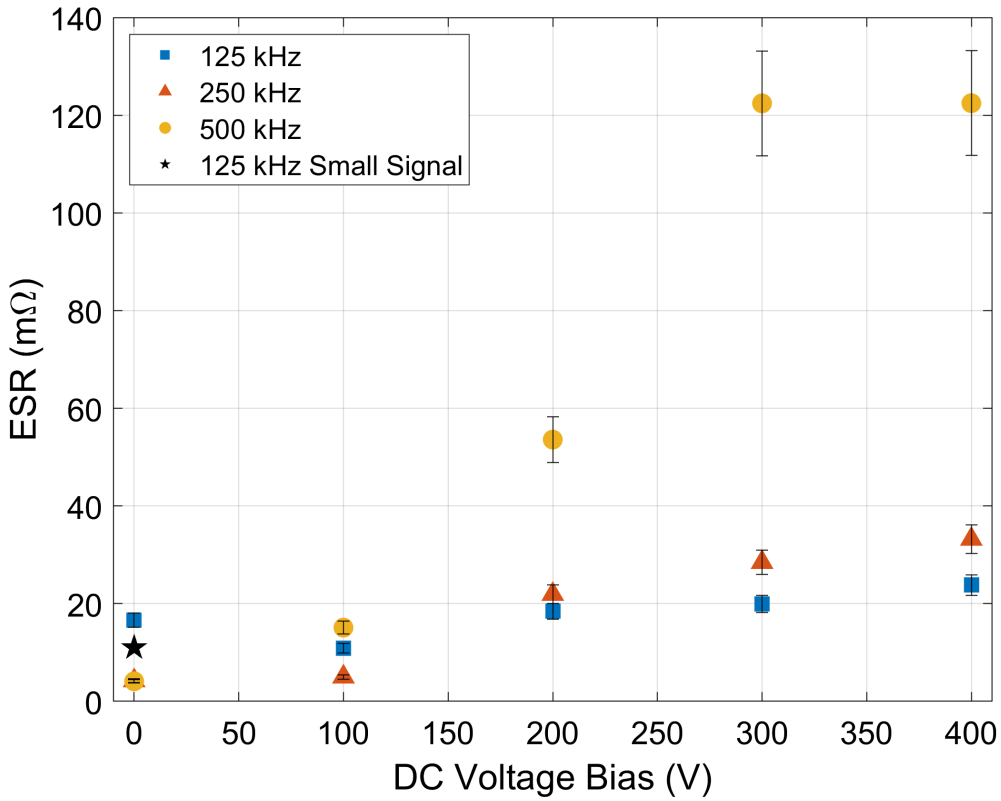

Figure 5.3: Kemet X7R, Cap III from Table 5.1, effect of DC bias on ESR. The black star represents the small signal ESR from the data sheet [7].

The Kemet X7R, Cap. III from Table 5.1, was tested under the same conditions as Cap. I and II. The results for these tests can be seen in Fig. 5.3. Similar to above, the small signal measured ESR is plotted as a black star. In general, Cap. III shows the same trends as the other two: With increased DC bias voltage the ESR also increases.

The 500 kHz data shows higher losses than the other two frequencies above 0 V bias. However, unlike the other Class II MLCCs, the losses increase at 250 kHz compared to 125 kHz. This is most likely due to the the self resonance point of the MLCC, shown in Fig. 2.6. It can be seen in Fig. 5.3 that for 500 kHz; as the bias increases the ESR increases exponentially instead of linearly. The cause of this phenomena is unknown, but was verified through three separate trial tests.

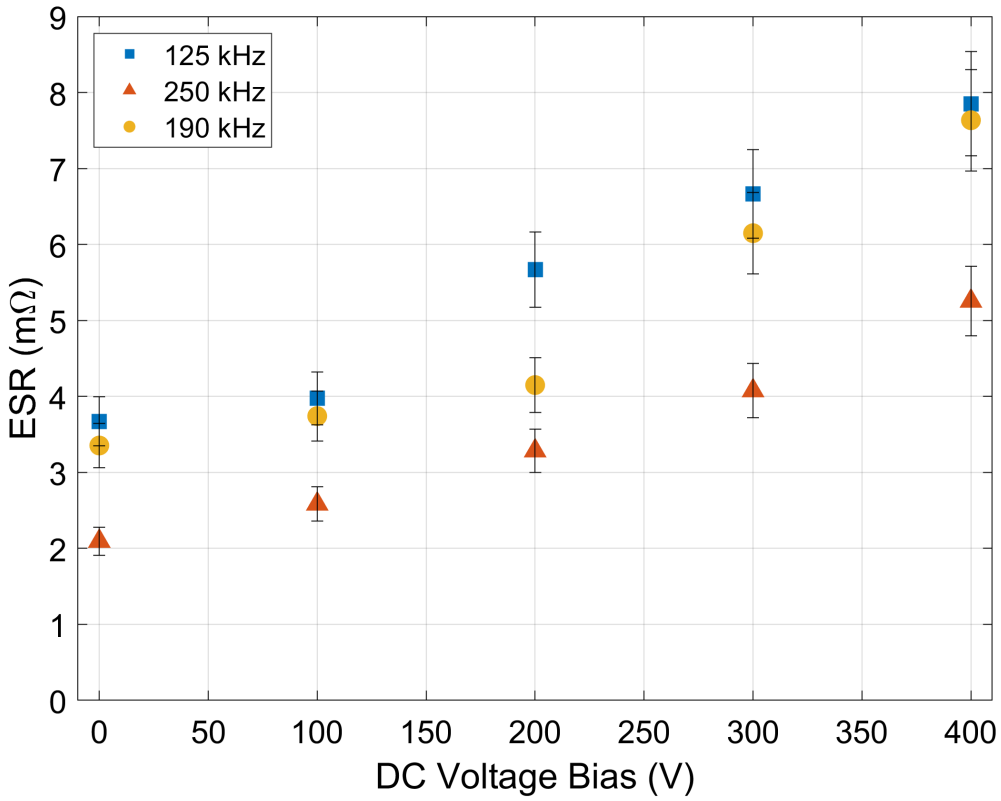

Figure 5.4: Ceralink, Cap IV from Table 5.1, effect of DC bias on ESR.

The Ceralink capacitors, Cap IV in Table 5.1, were tested at 125 kHz, 250 kHz and 190 kHz. The frequency was adjusted for these tests to avoid the self-resonance of the capacitor. The results of these tests can be seen in Fig. 5.4. With the adjusted test frequencies the trend follows expectation more closely, and shows that as frequency increases the ESR decreases, which is anticipated up to the point of self-resonance. Even though the Ceralink capacitors are not Class II MLCCs they still show the same increase in ESR with bias as the other tested capacitors. This follows results shown in [27].

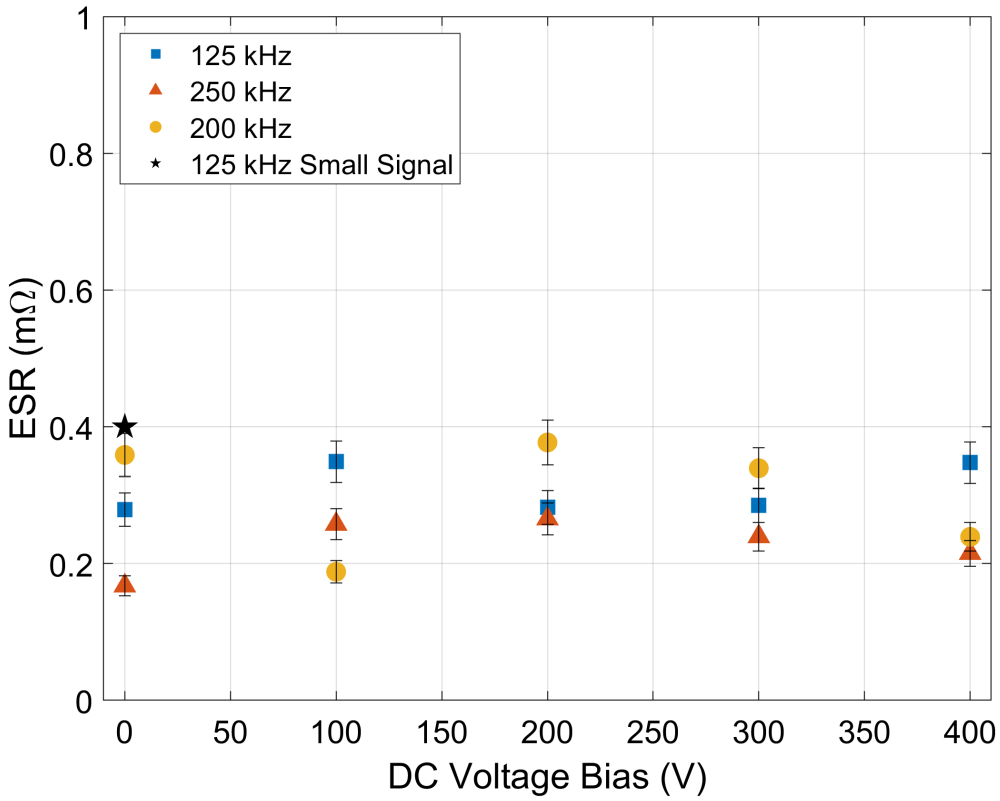

Figure 5.5: TDK C0G, Cap V from Table 5.1, effect of DC bias on ESR. The black star represents the small signal ESR from the data sheet [3].

The last MLCC tested was the Class I capacitor, Cap. V in Table 5.1. This capacitor is C0G which means the temperature rating is $-55°$ C to $125°$ C. As explained in Chapter 2, the Class I dielectrics do not suffer from reduced capacitance with applied DC voltage. Therefore, it was hypothesized that the losses would have less dependence on bias than the Class II dielectrics. Fig. 5.5 shows the results tested at 125 kHz, 200 kHz and 250 kHz, these frequencies were chosen to avoid self-resonance. The black star shows the small signal data provided by the data sheet [38]. It can be noted that at all operating conditions tested, the ESR is smaller for this capacitor than the previously tested Class II capacitors which is supported by data sheet values, and is displayed by black stars on each figure. It can also be seen in Fig. 5.5 that the DC bias does not have the same effect on ESR as the other tested MLCCs. In general, the relationship is flat, which shows that as predicted, the losses are less dependent on operating conditions compared to Class II and Ceralink MLCCs.

5.2 AC Amplitude Experimental Results

Next, the impact of AC excitation magnitude on MLCC losses was investigated. To test the effect of AC amplitude, the DC bias was kept constant and the AC amplitude was

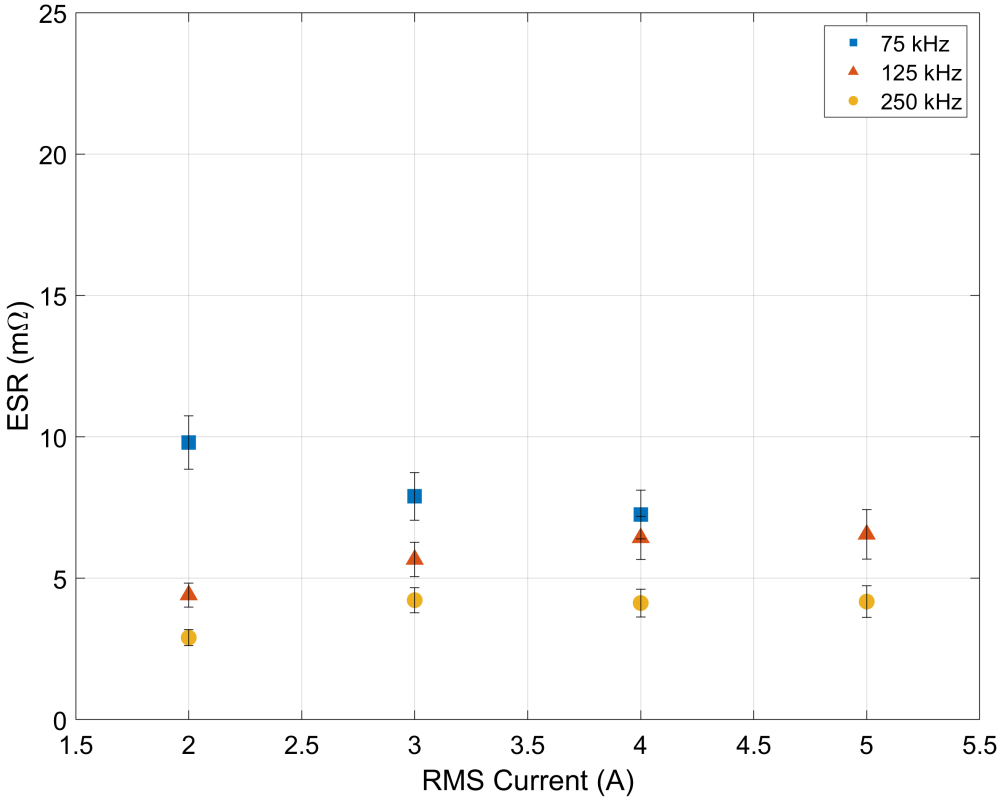

Figure 5.6: TDK X6S, Cap I from Table 5.1, effect of AC amplitude on ESR.

adjusted by tuning V_{Bridge} shown in Fig. 4.1. TDK X6S, Cap. I in Table 5.1, was tested at three frequencies over a wide range of current values at 0 V bias. The results from these tests can be seen in Fig. 5.6. The y-axis scale for Fig. 5.6 was purposefully left to be the same as the results shown in Fig. 5.1, to show the relative impact of AC amplitude and DC bias. Comparing Fig. 5.6 and Fig. 5.1 shows DC bias has a significantly higher effect on losses than AC amplitude.

Above 3 A RMS, the ESR is relatively constant over the range of tested values. At lower current values the ESR relationship is undefined, it appears to be lower at higher frequencies and higher at lower frequencies. A possible explanation of these results is the larger error seen at lower current measurements, supported by Eqn. 4.5. The results in Fig. 5.6 also show that with increasing frequency the ESR decreases, which agrees with Fig. 2.6.

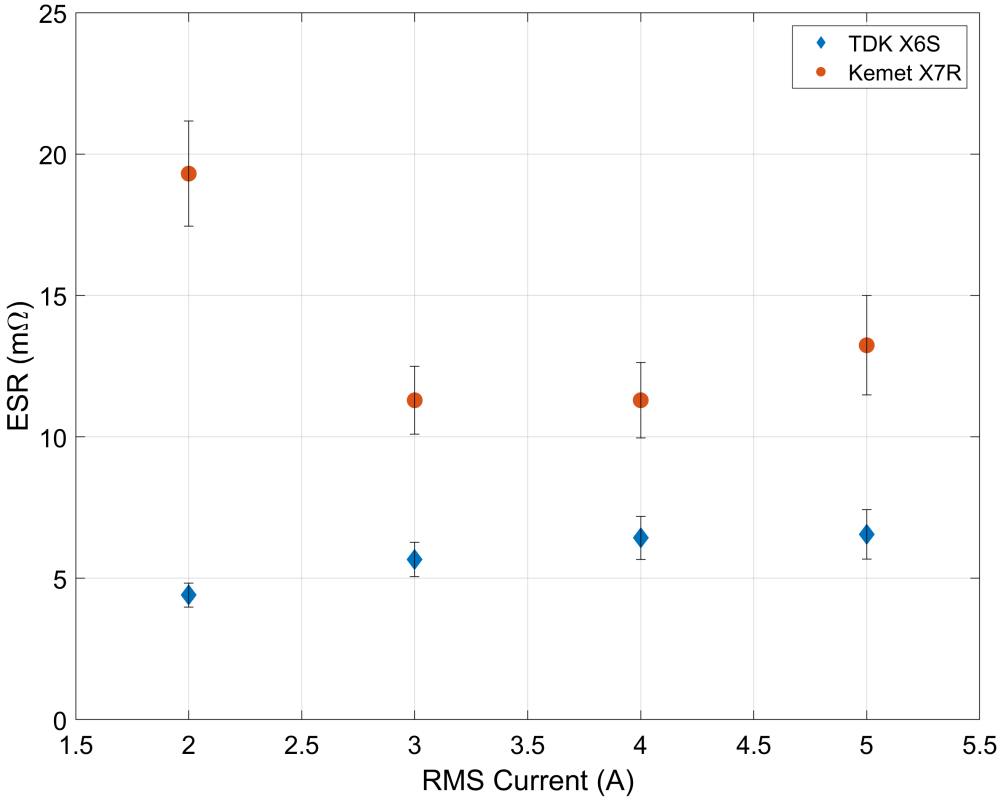

Figure 5.7: Kemet X6R, Cap III from Table 5.1 and TDK X6S, Cap I from Table 5.1 effect of AC amplitude on ESR.

This trend was verified with Kemet X7R, Cap. III in Table 5.1. Fig. 5.7 shows data tested at 0 V bias and 125 kHz switching frequency for both Cap. I and Cap. III. Again, there is an irregularity in the results at low current amplitudes. It is assumed that the accuracy of the measurement is lower at this low current point and therefore the irregularity can be neglected. At higher current values, the effect of current on ESR is small and the ESR seems stable over a wide operating region. In general, it can be seen that Cap. III exhibits higher losses than Cap. I, which is supported by Fig. 2.6.

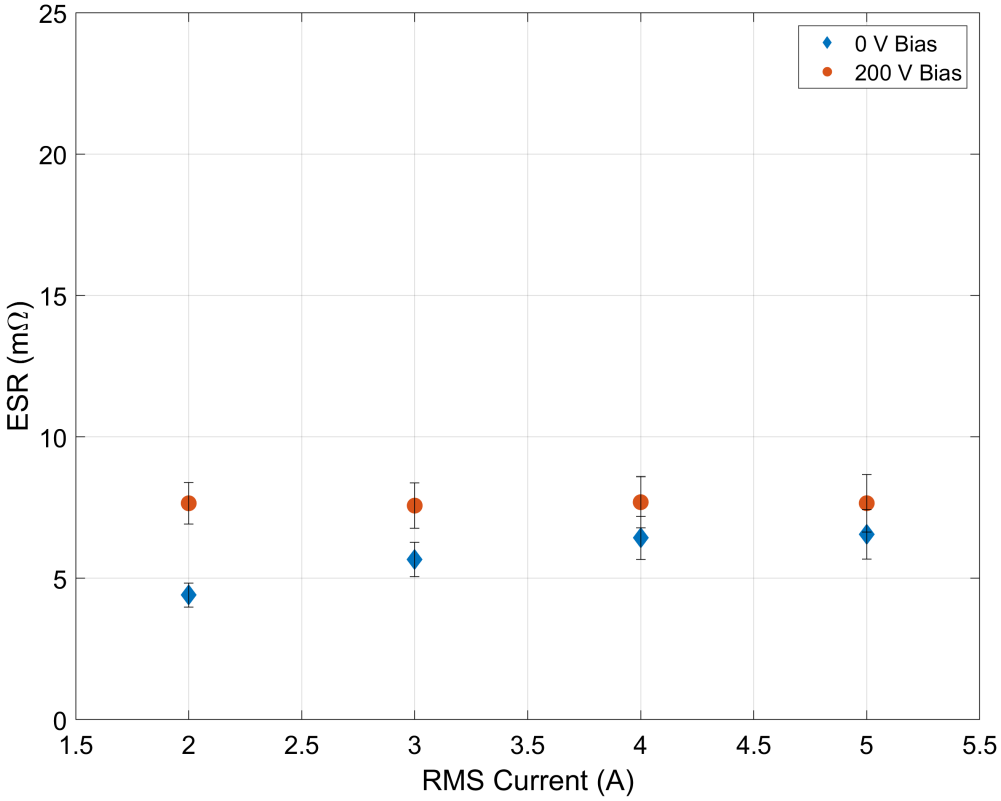

Figure 5.8: TDK X6S, Cap I from Table 5.1 effect of AC amplitude on ESR at multiple bias points.

The results show that AC amplitude effects ESR less than DC bias, this was further confirmed by testing TDK X6S, Cap. I, over a range of current amplitudes for two different bias points, shown in Fig. 5.8. This data was collected at 125 kHz. The y-axis scaling was set to show comparison to Fig. 5.1. Fig. 5.8 shows that at each operating condition the higher DC bias voltage resulted in higher ESR, which supports the data shown in Section 5.1. This figure shows that the ESR is relatively constant over the range of tested RMS currents.

5.3 ESR Dependence on Temperature

Published data shows that the ESR of ceramic capacitors changes over temperature [27, 38]. Thus, over wide temperature swings the capacitor loss model suggested by the simple resistor in Eqn. 2.4 is not linear since the resistance and losses vary as the device warms. To minimize the impact of temperature variation, the temperature swing of the oil in this work was restricted to less than five degrees Celsius. Fig. 5.9 shows the expected change in ESR with varying temperature for Cap. I, provided by [3].

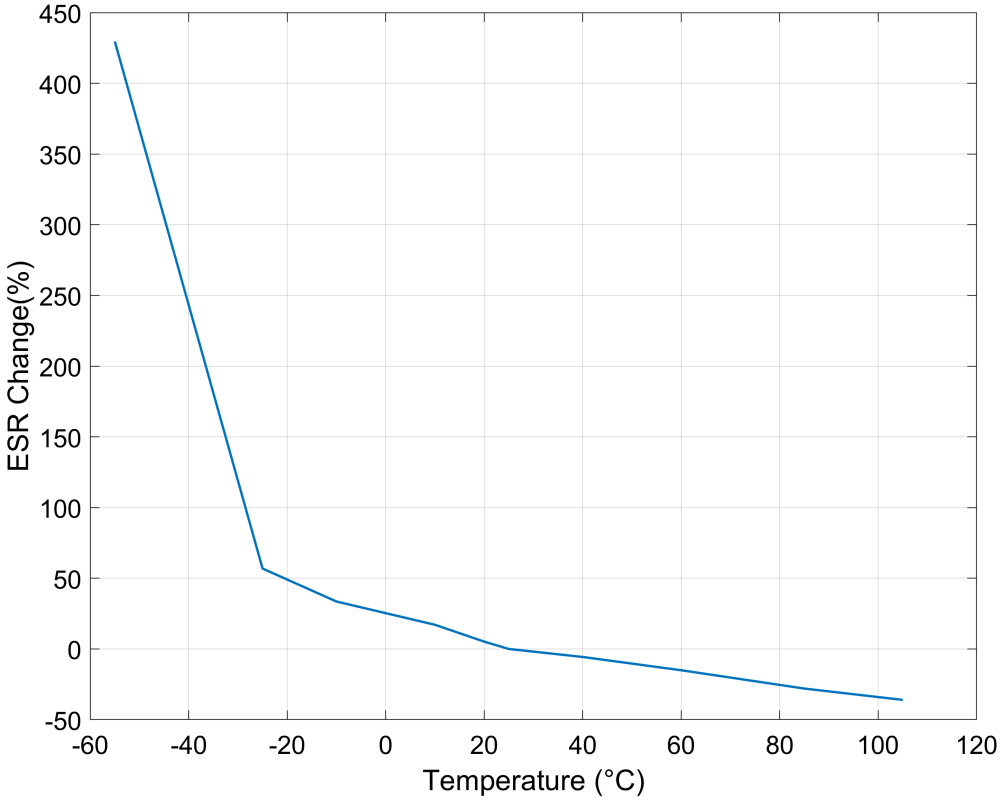

Figure 5.9: Dependence of ESR on operating temperature, shown for Cap I from Table 5.1 [3].

Looking more closely at the region of testing, from approximately 23 °C to 30 °C, the change in ESR due to temperature is limited to ±2% of the ESR, shown in Fig. 5.10.

To further investigate the effect of temperature on the ESR, the ESR was normalized to 25 °C using the data from Fig. 5.10. The results of this normalization can be seen in Fig. 5.11. This figure shows the losses of Cap. I over varying current amplitude, tested at 125 kHz and 0 V bias.

Fig. 5.11 shows that the effect of temperature is small and does not impact the overall trend of the data. The change due to temperature falls within the margin of error shown by the error bars. Therefore, it was determined that the temperature has no substantial impact on the collected data.

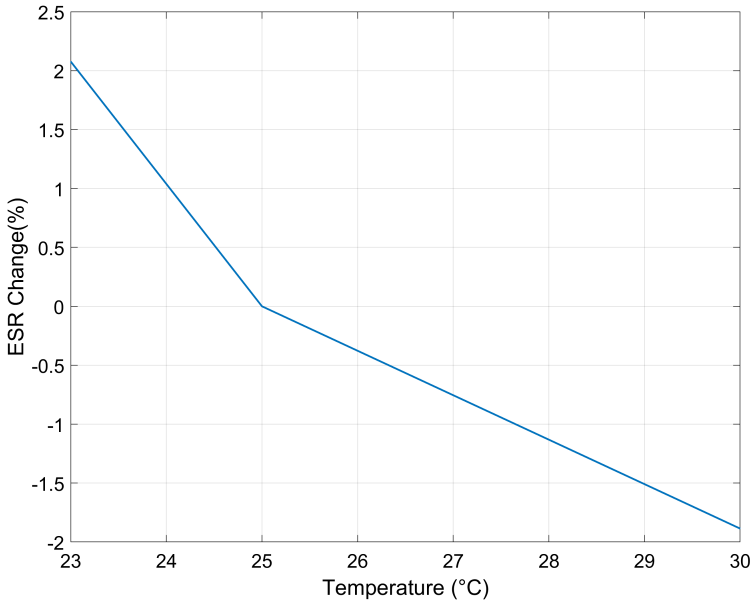

Figure 5.10: ESR dependence on temperature for the operating temperatures of this study [3].

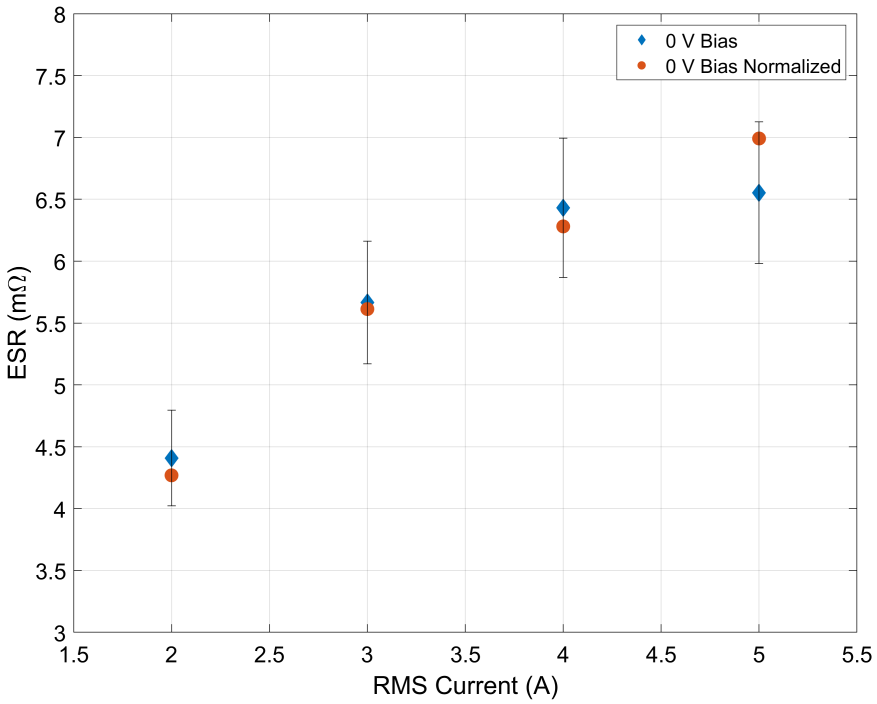

Figure 5.11: TDK X6S, Cap I in Table 5.1, 0 V bias at 125 kHz AC current amplitude effect on ESR. Shows the normalized data, adjusted for changes in temperature.

Chapter 6

Comparison to Low Frequency Electrical Measurements

To further validate the calorimetrically calculated losses and ESR, the results were compared to capacitor losses measured at low frequency using electrical measurements. As discussed in Chapter 3, an electrical evaluation was not employed for the high frequency loss measurements in this work due to the measurement accuracy requirements. However, at a lower frequency the simpler electrical characterizations have sufficient accuracy for comparison and validation. Assuming the Yokogawa WT3000 was used for low frequency measurement, i.e. 66 Hz to 1 kHz, then the expected error is approximately $\pm$ 0.5 W. This is much lower than the expected error for high frequency measurement discussed in Chapter 3.

While these low frequency measurements are not the desired operating conditions described in Chapter 2, they still serve as a check on the trends found from the calorimetric results, described in Chapter 5.

6.1 Electrical Setup

In [19] a methodology for testing capacitors in buffering applications was introduced. This same setup, shown in Fig. 6.1, was implemented to test the capacitors over a range of frequencies, 120 Hz to 500 Hz. The necessary equipment for this setup can be seen in

Table 6.1: Devices used in low frequency electrical setup.

Label	Instrument
V_{DC}	Magna-Power Electronics DC Supply
I_{DUT} and V_{DUT}	Yokogawa WT3000 Power Analyzer
V_{AC}	Pacific Smart Source 112-AMX
Transformer	Schneider Electric Cat. No: 151F

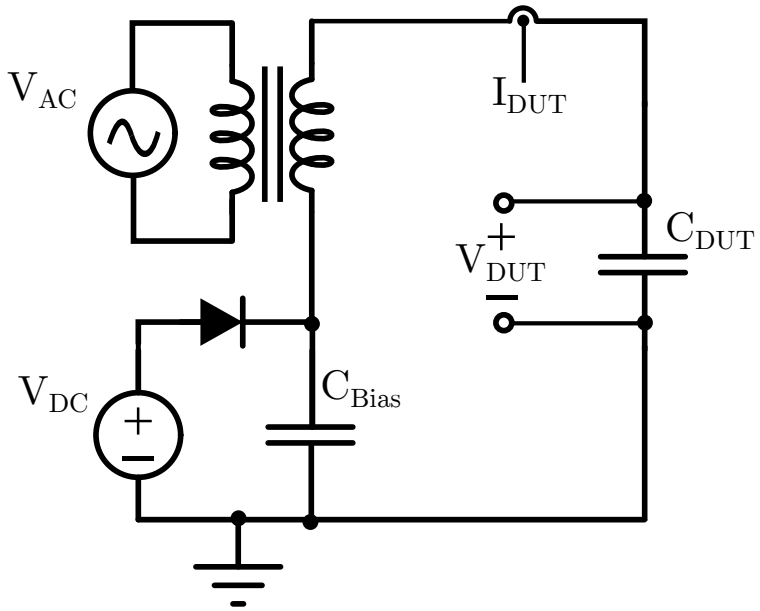

Figure 6.1: Low frequency electrical measurement capacitor testing circuit.

Table 6.1. The power dissipated by the DUT was found using an advanced power analyzer, the Yokogawa WT3000. The ESR was determined by dividing by the square of the RMS current. For this low frequency setup, the DC bias is adjusted by changing V_{DC}.

6.2 DC Bias Results

The results for low frequency measurements for TDK's X6S MLCC are summarized in Fig. 6.2. Note that as the frequency is doubled, from 250 Hz to 500 Hz, the ESR is approximately halved. This trend follows from the ESR and frequency results in Fig. 6.3, where at low frequencies the ESR decreases approximately linearly with frequency. These results verify that even at a low frequency, the ESR increases with applied DC bias. It must be noted that the ESR at the low frequencies measured is significantly higher than the results of the high frequency calorimetric measurements. The ESR is fundamentally higher at lower frequencies as is seen in the manufacturer supplied data shown in Fig. 6.3.

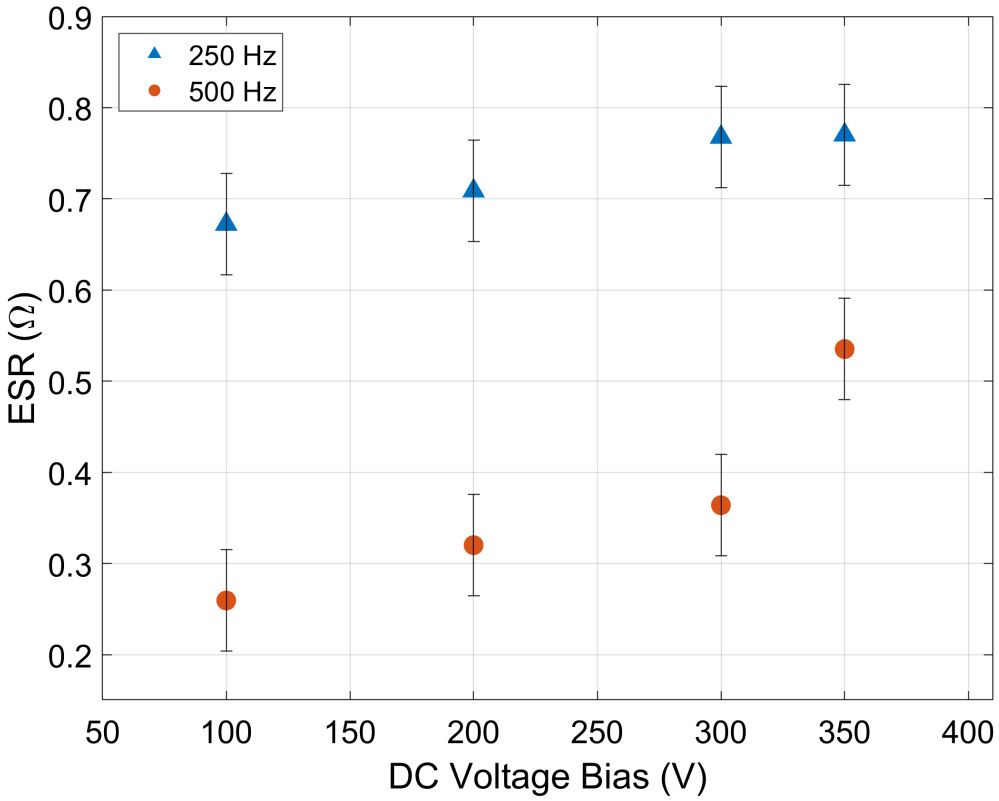

Figure 6.2: Low frequency bias dependent ESR results, for TDK X6S MLCC (Cap I in Table 5.1), attained through electrical experimental setup.

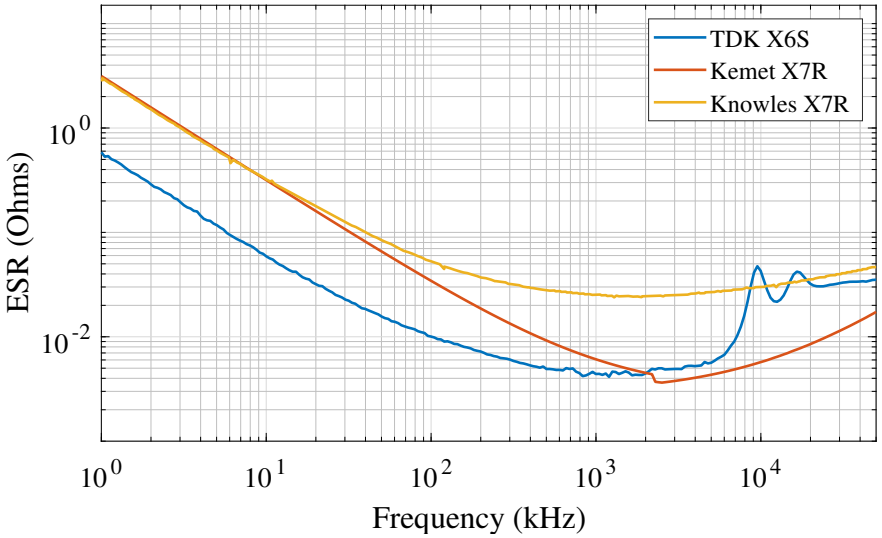

Figure 6.3: ESR of three Class II MLCCs over a range of frequencies, which highlights the increased ESR at lower operating frequencies [3] [4] [5].

Chapter 7

Loss Model

After experimental evaluation of the MLCCs, it was desired to create a model which would allow simple loss calculations based off parameters already provided on the data sheet, and new parameters which would be simple for the manufacturers to test and provide. This model will take into account the dominant influences on loss; DC bias and frequency. This chapter proposes a model to evaluate ESR at a given operating condition for Class II MLCCs.

7.1 Model Theory

Most manufacturers provide capacitance derating, an example seen in Fig. 2.5, on MLCC data sheets. Leveraging this relationship, an equation was derived relating the ESR and capacitance at any given voltage bias.

As described in Chapter 5, the relationship between ESR and voltage bias is relatively linear and therefore can be written as an expression, seen in Eqn. 7.1. Where a and b are constants determined by the frequency and MLCC in operation. Fig. 7.1 shows an example linear fit of the ESR and DC bias relationship. The coefficient of determination, R^2, value for this linear fit is 0.98.

$$R_{ESR} = a + bv_{bias} \tag{7.1}$$

The relationship between capacitance derating and voltage bias is exponential, and therefore the relationship can be described by Eqn. 7.2. Both ζ and λ are dependent on the MLCCs dielectric and package, but can be found from datasheet values. Fig. 7.2 shows an example capacitor derating fit with an exponential curve. The coefficient of determination, R^2, value for this fit is 0.96.

$$C = \zeta e^{-\lambda v_{bias}} \tag{7.2}$$

Solving equation 7.2 for v_{bias} as a function of C yields Eqn. 7.3.

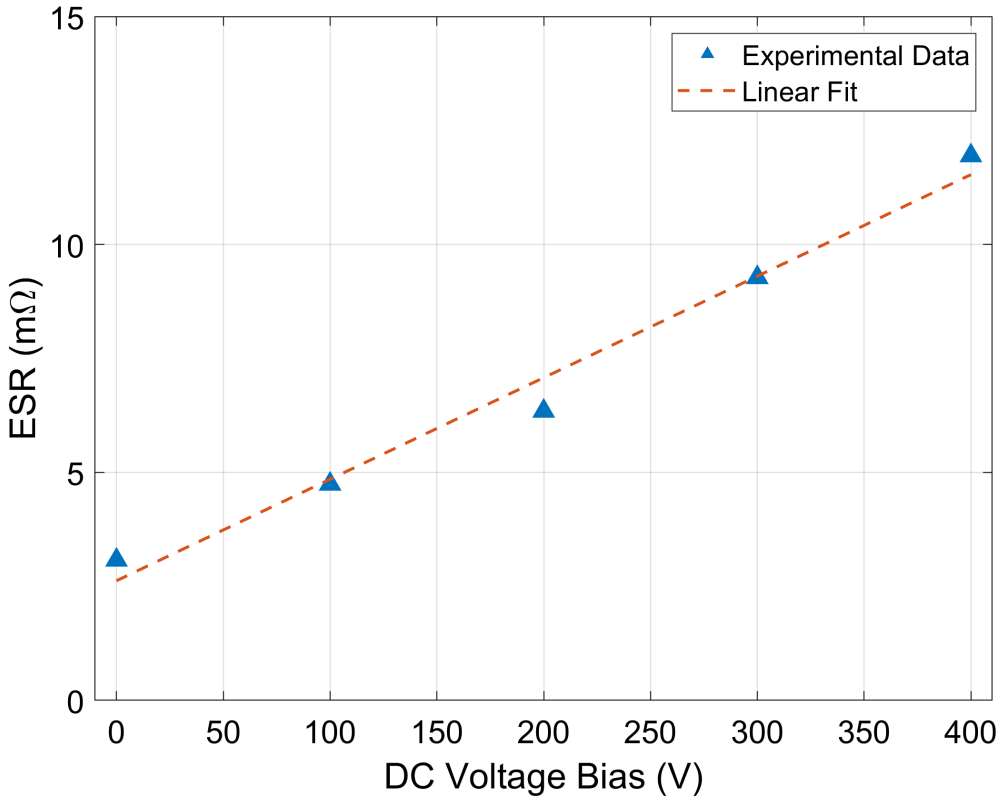

Figure 7.1: ESR and DC bias relationship for TDK X6S, Cap. I from Table 5.1 measured at 250 kHz, shown with a linear fit.

$$v_{bias} = \frac{ln(\zeta) - ln(C)}{\lambda} \tag{7.3}$$

Combining Eqn. 7.1 and Eqn. 7.3, results in Eqn. 7.4 which can be expanded to Eqn. 7.5.

$$R_{ESR} = a + \frac{b}{\lambda}(ln(\zeta) - ln(C)) \tag{7.4}$$

$$R_{ESR} = a + \frac{b}{\lambda}ln(\zeta) - \frac{b}{\lambda}ln(C) \tag{7.5}$$

Next two new constants are introduced; α and γ, which are defined in Eqn. 7.6 and Eqn. 7.7. This simplifies Eqn. 7.5 to Eqn. 7.8.

$$\alpha = a + \frac{b}{\lambda}ln(\zeta) \tag{7.6}$$

$$\gamma = \frac{b}{\lambda} \tag{7.7}$$

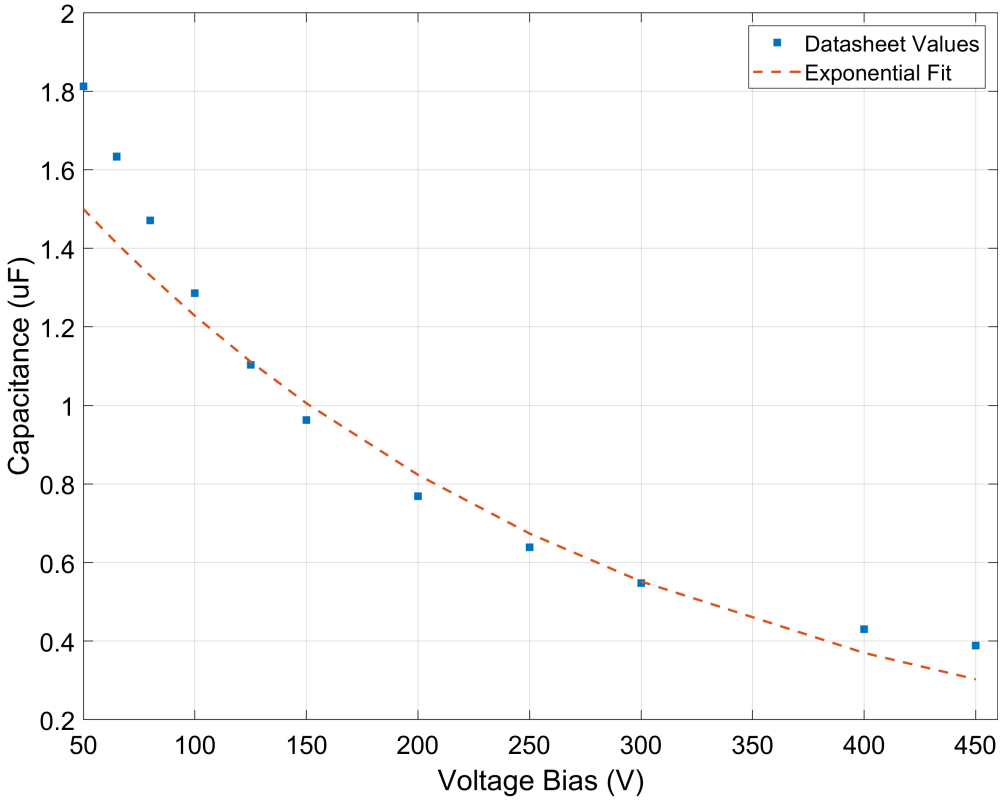

Figure 7.2: Capacitance and DC bias relationship for TDK X6S, Cap. I from Table 5.1, with an exponential fit [3].

$$R_{ESR} = \alpha - \gamma ln(C) \tag{7.8}$$

The α and γ introduced are dependent on frequency and MLCC, but are not dependent on the voltage bias.

The final model can be seen in Eqn. 7.9.

$$R_{ESR} = \alpha - \gamma ln(\beta C) \tag{7.9}$$

C represents the capacitance at the voltage bias desired. In Eqn. 7.9 the β parameter is fixed to a value that restricts βC to be greater than one, so that the natural log is a positive quantity. For the capacitors evaluated in this study a β of 10^7 was sufficient and used for every operating condition.

Parameters α and γ are both dependent on frequency, and vary in magnitude between different MLCCs. Therefore, they must be derived at each frequency tested. An explanation of the derivation of these parameters follows.

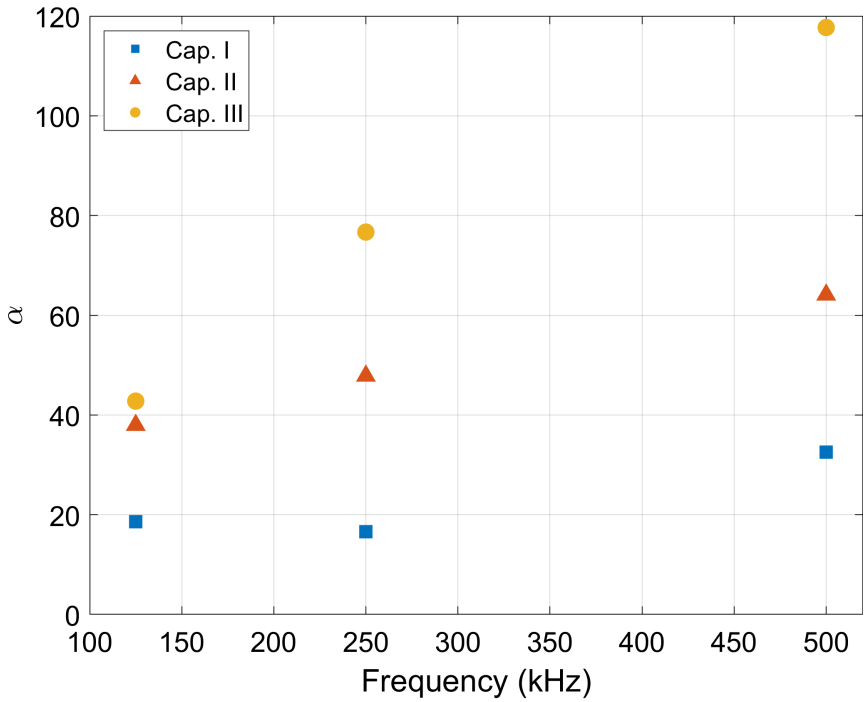

Figure 7.3: Calculated α values from optimization, for tested capacitors, listed in Table 5.1.

Alpha and Gamma Calculations

Using the calorimetrically evaluated data, parameters α and γ were determined for each frequency evaluated for each capacitor. To best fit the model to the experimental data the Excel Solver was used. Excel Solver, a built-in Excel add-in, works to minimize an error function described by the user. The solver was set-up to vary α and γ, and then recalculate the ESR from Eqn. 7.9. The solver was set to use a non-linear method to minimize the error over the range of biases tested. The error at a given frequency, e_f, was calculated in Eqn. 7.10.

$$e_f = \sum_{bias=0V}^{400V} \frac{|R_{exp} - R_{model}|}{R_{exp}}\Bigg|_{bias} \tag{7.10}$$

For the three Class II capacitors tested in this study, the α and γ for each frequency tested was evaluated and can be seen in Fig. 7.3 and Fig. 7.4, respectively.

It is difficult to extract the relationship between α and γ and frequency since only three frequencies were evaluated. However, it should be noted that this relationship is expected to be non-linear since it is known that ESR does not vary linearly with frequency, as shown in Fig. 2.6.

An example of the applied model data can be seen in Fig. 7.5, where both the experimental and modeled data are plotted together. This model was created using the capacitor

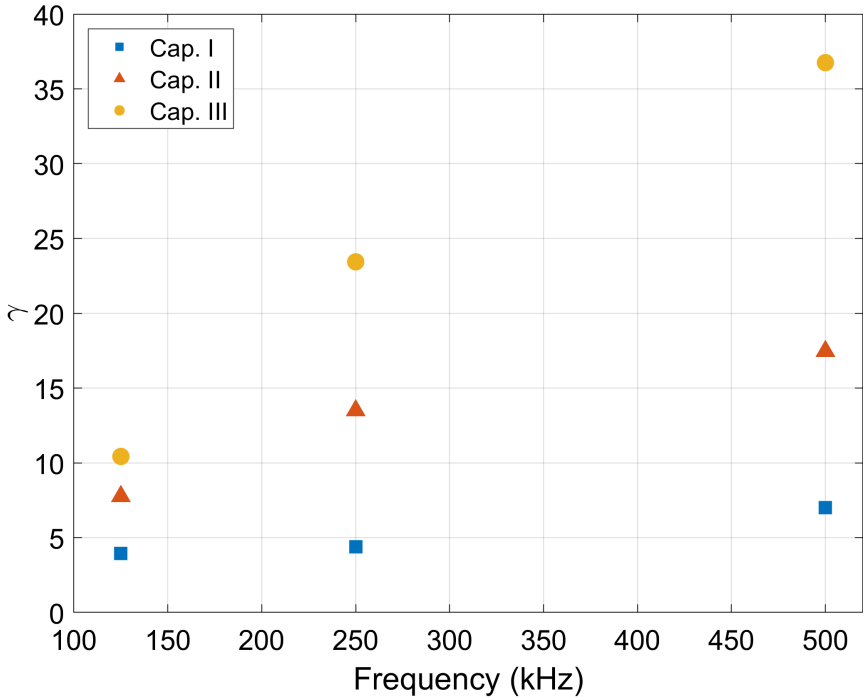

Figure 7.4: Calculated γ values from optimization, for tested capacitors, listed in Table 5.1.

derating seen in Fig. 7.2. Using the suggested model the average error between the measured and calculated ESR at any voltage bias was 7.9%.

Proposed Method for Manufacturer Provided Alpha and Gamma

To estimate losses of an MLCC at given operating conditions, it is desired that no additional testing by the designer is necessary, instead values can be extracted from the data sheet to determine the expected loss. One possible method for manufacturers would be to provide the α and γ relationships versus frequency. This combined with the derating relationship could be used to determine the ESR for any given operating condition.

However, it is expected that finding α and γ through calorimetric testing is too time consuming for a typical manufacturer with a wide portfolio of parts. Since the model provided does not require characterization at high voltage, a simpler method could be employed. Since there are two unknowns, α and γ, only two points with a known ESR and capacitance are required to derive the unknowns; however, more data points would likely increase accuracy. Therefore, an impedance analyzer could be implemented to gather the ESR and frequency relationship at 0 V bias and other small voltage biases, i.e. 10 V to 40 V. This would allow for high accuracy measurements using the impedance analyzer, since at higher voltage the measurement is difficult and inaccurate.

It is anticipated that this process would take much less time than calorimetric testing

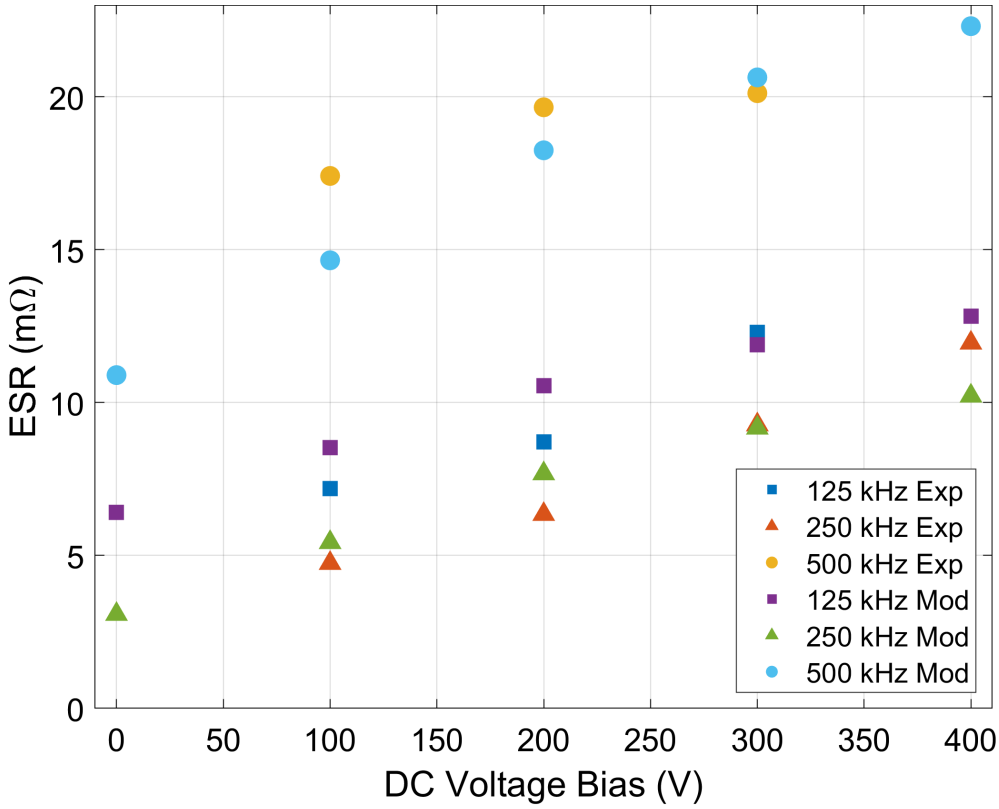

Figure 7.5: Modeled and experimental data compared for TDK X6S, Cap. I in Table 5.1.

and still provide the information necessary to apply the model described over a wide range of operating conditions.

7.2 Application of Model to Case Study

To understand the effect of the model and new understanding of losses in MLCCs, it is helpful to return to the case study presented in Chapter 2. Originally when estimating the losses due to capacitor ESR in this converter, it was assumed that each capacitor exhibits the loss attained from the frequency and ESR relationship from the data sheet. In this converter, the TDK X6S was used, Cap. I in Table 5.1. Therefore, the losses of the MLCC was assumed to be 5 mΩ, found from Fig. 2.6 where the switching frequency was approximately 125 kHz.

As explained in Chapter 2, the converter has seven sets of capacitors. In each level, the actual number of capacitors is eight, four in parallel and two in series. Since resistance divides in parallel and adds in series, for each capacitor leg the ESR is one half the ESR of one capacitor.

Therefore, originally the total capacitor loss for the converter could be calculated with Eqn. 7.11.

$$P_{loss} = I^2_{C_{FLY,RMS}} \frac{R_{ESR}}{2} \tag{7.11}$$

The estimated P_{loss} for this converter was determined to be 1.5 W for each interleaved leg, so approximately 3 W for the entire converter.

Using the new modeled losses, the ESR for each level can be calculated using Eqn. 7.9 where α and γ were calculated for 125 kHz, shown in Section 7.1. The ESR for each level is shown in Table 7.1.

Table 7.1: Adjusted power loss calculations for case study based on modeled ESR.

Level Number	V_{Level} (V)	V_{Cap} (V)	C_{eff} (μF)	R_{ESR} ($m\Omega$)	P_{loss} (W)
1	125	62.5	3.27	4.85	0.21
2	250	125	2.21	6.39	0.28
3	375	187.5	1.65	7.54	0.33
4	500	250	1.28	8.54	0.38
5	625	312.5	1.10	9.14	0.41
6	750	375	1.01	9.47	0.42
7	875	437.5	0.75	10.66	0.47

Table 7.1 shows the expected loss for each level based on the model. The sum of this loss shows the total loss to be 2.51 W per interleaved leg or 5.02 W for the entire converter.

The proposed model estimates the capacitor losses to be increased by approximately 67%. This substantial increase shows the importance of understanding the actual losses at the operating condition of MLCCs.

Chapter 8

Conclusions

As explained in Chapter 1, the move towards more electric transportation requires extremely efficient power electronics. This work has provided a method for accurately characterizing the losses of MLCCs used in these dense and efficient power converters. Through the method described in Chapter 4, results were attained that show the impact of large signal operating conditions on the loss of MLCCs. These results, shown in Chapter 5 helped to create a model explained in Chapter 7. This model can be applied in the future when designing power converters to better understand capacitor losses, and eventually can be used to find strategies to mitigate these losses.

8.1 Future Work

Further Model Verification

The model described in Chapter 7 aims to simplify the amount of work necessary to determine losses across many operating conditions. The next step is to validate this model over a wide range of frequencies. Since the α and γ parameters introduced are both dependent on frequency, and frequency is known to have a non-linear effect on losses, it is anticipated that the α and γ parameters will have a non-linear relationship with frequency. Therefore, it is necessary to characterize these parameters at a wide range of frequencies and for several different MLCCs to understand the effectiveness of the model.

Harmonic Content Characterization

As described in Chapter 2, the dynamics of the Class II MLCCs are dependent on temperature, DC bias, AC amplitude, frequency and harmonic content. Previous work has shown the loss dependence on temperature and frequency, and this work has demonstrated the effect of DC bias and AC amplitude. The next step will be to investigate the effect of harmonic content on losses. This effect will be more difficult to analyze, because the electrical excitation will need to be modified so that the MLCC excitation can be changed from

a sinusoidal waveform to a square waveform. Understanding the effect of harmonic content would allow understanding of the losses over all operating conditions.

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Appendix A

Experimental Data

Table A.1: DC bias characteristic data of TDK X6S, Cap I from Table 5.1.

Capacitor	Freq (kHz)	DC Bias (V)	AC Amp (A)	ESR ($m\Omega$)
TDK X6S (Cap. I)	125	0	6	6.41
TDK X6S (Cap. I)	125	100	6	7.18
TDK X6S (Cap. I)	125	200	6	8.72
TDK X6S (Cap. I)	125	300	6	12.29
TDK X6S (Cap. I)	125	400	6	12.82
TDK X6S (Cap. I)	250	0	6	3.08
TDK X6S (Cap. I)	250	100	6	4.74
TDK X6S (Cap. I)	250	200	6	6.35
TDK X6S (Cap. I)	250	300	6	9.27
TDK X6S (Cap. I)	250	400	6	11.95
TDK X6S (Cap. I)	500	0	6	10.90
TDK X6S (Cap. I)	500	100	6	17.41
TDK X6S (Cap. I)	500	200	6	19.66
TDK X6S (Cap. I)	500	300	6	20.12
TDK X6S (Cap. I)	500	400	6	22.31

Table A.2: DC bias characteristic data of Knowles X7R, Cap II from Table 5.1.

Capacitor	Freq (kHz)	DC Bias (V)	AC Amp (A)	ESR ($m\Omega$)
Knowles X7R (Cap. II)	125	0	6	13.97
Knowles X7R (Cap. II)	125	100	6	15.77
Knowles X7R (Cap. II)	125	200	6	19.62
Knowles X7R (Cap. II)	125	300	6	31.41
Knowles X7R (Cap. II)	125	400	6	33.97
Knowles X7R (Cap. II)	250	0	6	6.12
Knowles X7R (Cap. II)	250	100	6	6.56
Knowles X7R (Cap. II)	250	200	6	19.87
Knowles X7R (Cap. II)	250	300	6	22.31
Knowles X7R (Cap. II)	250	400	6	31.54
Knowles X7R (Cap. II)	500	0	6	10.13
Knowles X7R (Cap. II)	500	100	6	19.49
Knowles X7R (Cap. II)	500	200	6	24.23
Knowles X7R (Cap. II)	500	300	6	46.41
Knowles X7R (Cap. II)	500	400	6	52.31

Table A.3: DC bias characteristic data of Kemet X7R, Cap III from Table 5.1.

Capacitor	Freq (kHz)	DC Bias (V)	AC Amp (A)	ESR ($m\Omega$)
Kemet X7R (Cap. III)	125	0	6	16.67
Kemet X7R (Cap. III)	125	100	6	10.89
Kemet X7R (Cap. III)	125	200	6	18.46
Kemet X7R (Cap. III)	125	300	6	19.97
Kemet X7R (Cap. III)	125	400	6	23.82
Kemet X7R (Cap. III)	250	0	6	4.23
Kemet X7R (Cap. III)	250	100	6	5.00
Kemet X7R (Cap. III)	250	200	6	21.92
Kemet X7R (Cap. III)	250	300	6	28.46
Kemet X7R (Cap. III)	250	400	6	33.21
Kemet X7R (Cap. III)	500	0	6	4.10
Kemet X7R (Cap. III)	500	100	6	15.09
Kemet X7R (Cap. III)	500	200	6	53.59
Kemet X7R (Cap. III)	500	300	6	122.44
Kemet X7R (Cap. III)	500	400	6	122.46

Table A.4: DC bias characteristic data of Ceralink MLCC, Cap IV from Table 5.1.

Capacitor	Freq (kHz)	DC Bias (V)	AC Amp (A)	ESR ($m\Omega$)
Ceralink (Cap. IV)	125	0	6	3.67
Ceralink (Cap. IV)	125	100	6	3.98
Ceralink (Cap. IV)	125	200	6	5.67
Ceralink (Cap. IV)	125	300	6	6.67
Ceralink (Cap. IV)	125	400	6	7.85
Ceralink (Cap. IV)	250	0	6	2.09
Ceralink (Cap. IV)	250	100	6	2.58
Ceralink (Cap. IV)	250	200	6	3.28
Ceralink (Cap. IV)	250	300	6	4.08
Ceralink (Cap. IV)	250	400	6	5.25
Ceralink (Cap. IV)	190	0	6	3.35
Ceralink (Cap. IV)	190	100	6	3.74
Ceralink (Cap. IV)	190	200	6	4.15
Ceralink (Cap. IV)	190	300	6	6.15
Ceralink (Cap. IV)	190	400	6	7.64

Table A.5: DC bias characteristic data of TDK C0G, Cap V from Table 5.1.

Capacitor	Freq (kHz)	DC Bias (V)	AC Amp (A)	ESR ($m\Omega$)
TDK C0G (Cap. V)	125	0	4	0.28
TDK C0G (Cap. V)	125	100	4	0.35
TDK C0G (Cap. V)	125	200	4	0.28
TDK C0G (Cap. V)	125	300	4	0.29
TDK C0G (Cap. V)	125	400	4	0.35
TDK C0G (Cap. V)	250	0	4	0.17
TDK C0G (Cap. V)	250	100	4	0.26
TDK C0G (Cap. V)	250	200	4	0.27
TDK C0G (Cap. V)	250	300	4	0.24
TDK C0G (Cap. V)	250	400	4	0.22
TDK C0G (Cap. V)	200	0	4	0.36
TDK C0G (Cap. V)	200	100	4	0.21
TDK C0G (Cap. V)	200	200	4	0.38
TDK C0G (Cap. V)	200	300	4	0.34
TDK C0G (Cap. V)	200	400	4	0.24

Table A.6: AC amplitude characteristic data of TDK X6S, Cap I from Table 5.1.

Capacitor	Freq (kHz)	DC Bias (V)	AC Amp (A)	ESR ($m\Omega$)
TDK X6S (Cap. I)	125	0	1	7.79
TDK X6S (Cap. I)	125	0	2	4.27
TDK X6S (Cap. I)	125	0	3	5.61
TDK X6S (Cap. I)	125	0	4	6.28
TDK X6S (Cap. I)	125	0	5	6.99
TDK X6S (Cap. I)	250	0	1	7.09
TDK X6S (Cap. I)	250	0	2	2.90
TDK X6S (Cap. I)	250	0	3	4.22
TDK X6S (Cap. I)	250	0	4	4.12
TDK X6S (Cap. I)	250	0	5	4.17
TDK X6S (Cap. I)	125	200	1	7.97
TDK X6S (Cap. I)	125	200	2	7.65
TDK X6S (Cap. I)	125	200	3	7.57
TDK X6S (Cap. I)	125	200	4	7.69
TDK X6S (Cap. I)	125	200	5	7.65
TDK X6S (Cap. I)	250	200	1	9.35
TDK X6S (Cap. I)	250	200	2	9.33
TDK X6S (Cap. I)	250	200	3	7.55
TDK X6S (Cap. I)	250	200	4	6.84
TDK X6S (Cap. I)	250	200	5	7.38
TDK X6S (Cap. I)	75	0	1	4.35
TDK X6S (Cap. I)	75	0	2	9.80
TDK X6S (Cap. I)	75	0	3	7.90
TDK X6S (Cap. I)	75	0	4	7.26
TDK X6S (Cap. I)	75	0	5	4.84

Table A.7: AC amplitude characteristic data of Kemet X7R, Cap III from Table 5.1.

Capacitor	Freq (kHz)	DC Bias (V)	AC Amp (A)	ESR ($m\Omega$)
Kemet X7R (Cap. III)	125	0	1	21.99
Kemet X7R (Cap. III)	125	0	2	18.95
Kemet X7R (Cap. III)	125	0	3	11.40
Kemet X7R (Cap. III)	125	0	4	11.56
Kemet X7R (Cap. III)	125	0	5	12.41

Appendix B

Electrical Excitation Printed Circuit Board

For reference, the electrical excitation PCB designed to create a DC bias, and square wave current excitation across the DUT is detailed below.

Schematic

The schematic for the H-bridge excitation circuit is included in Fig. B.1.

Layout

The PCB layout for the H-bridge circuit is detailed, separated into four layers shown in Figures B.2, B.3, B.4 and B.5.

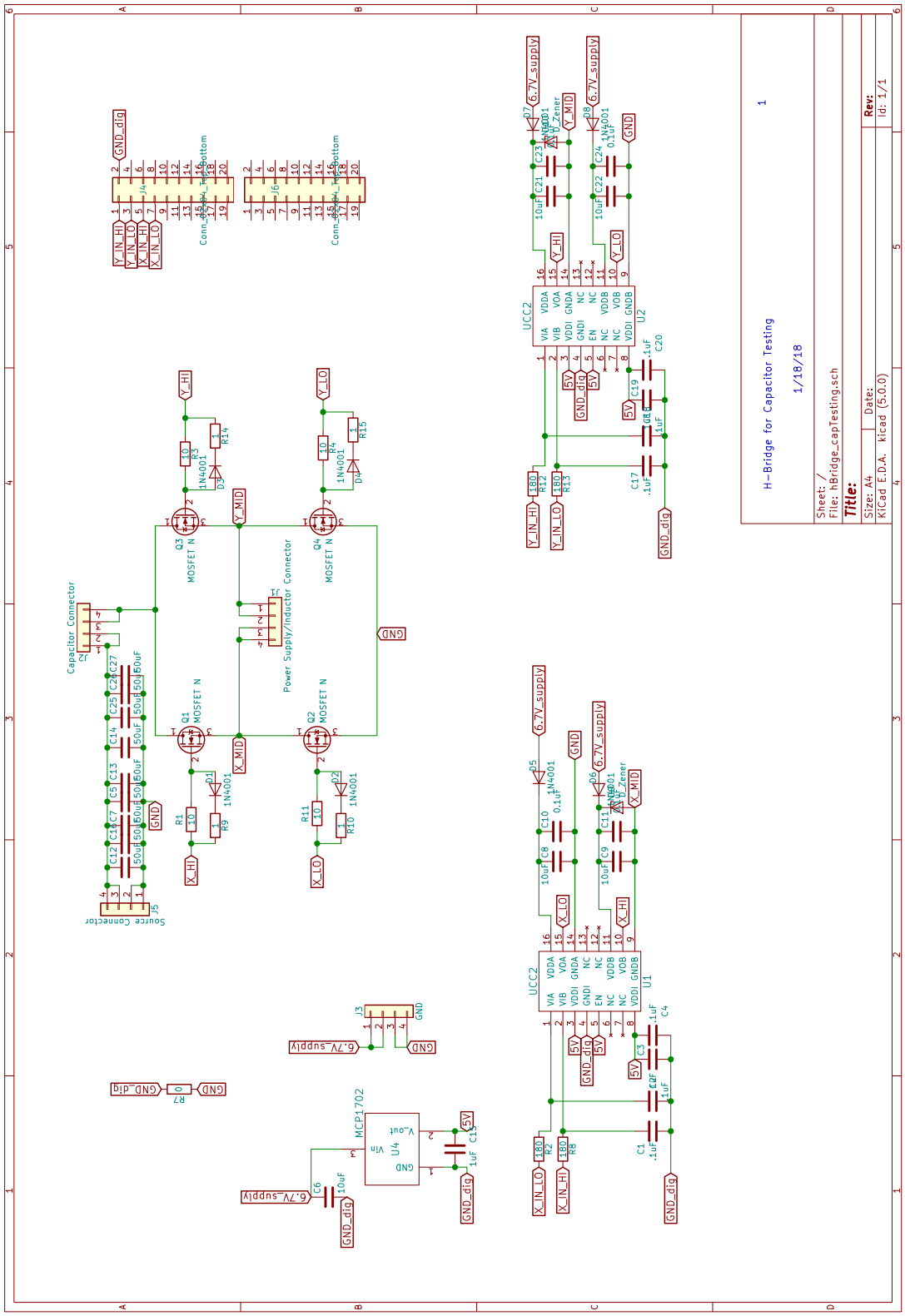

Figure B.1: H-bridge schematic for applying electrical excitation across the DUT.

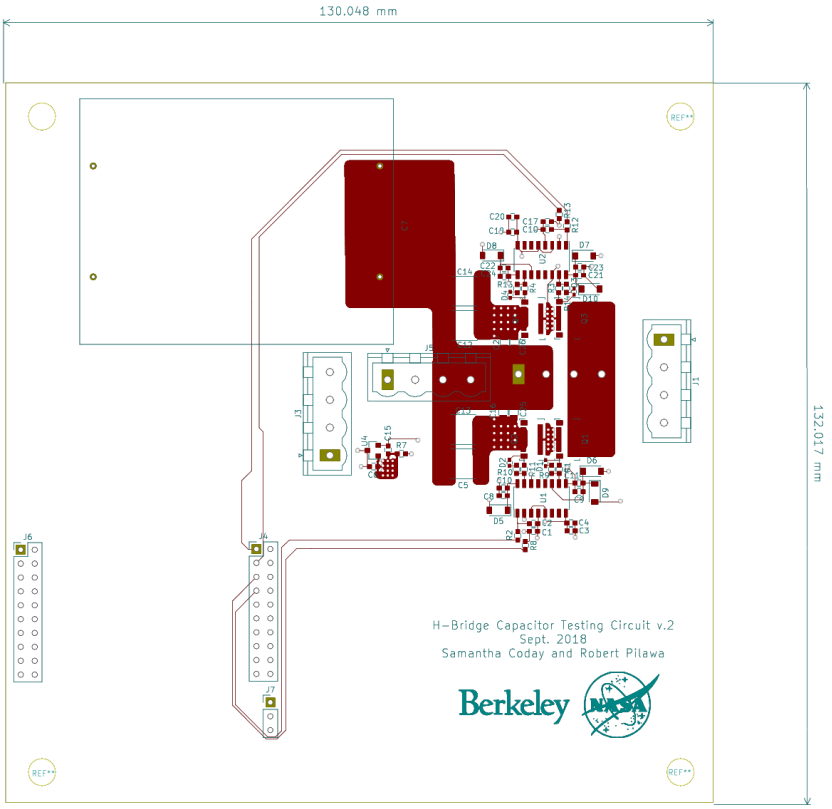

Figure B.2: Top layer of PCB.

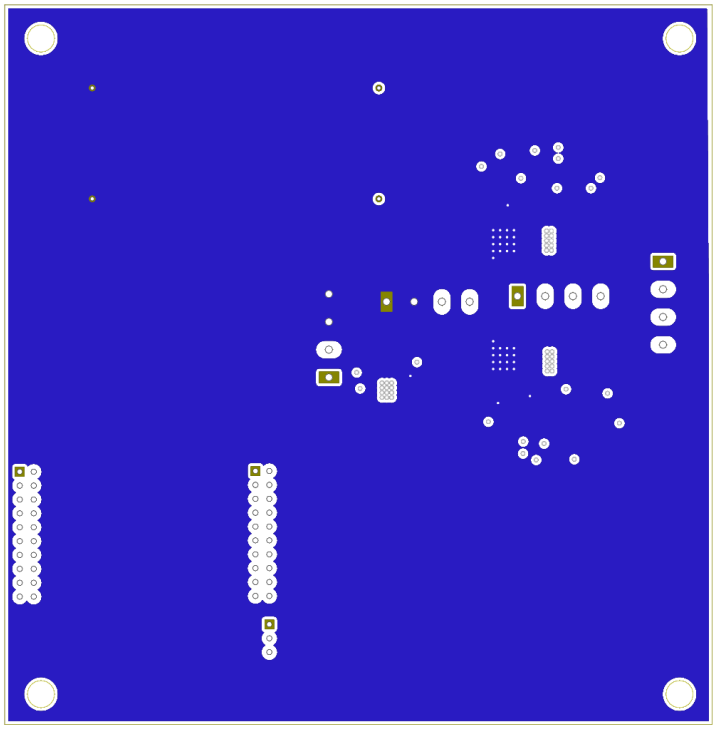

Figure B.3: Inner layer one of the PCB.

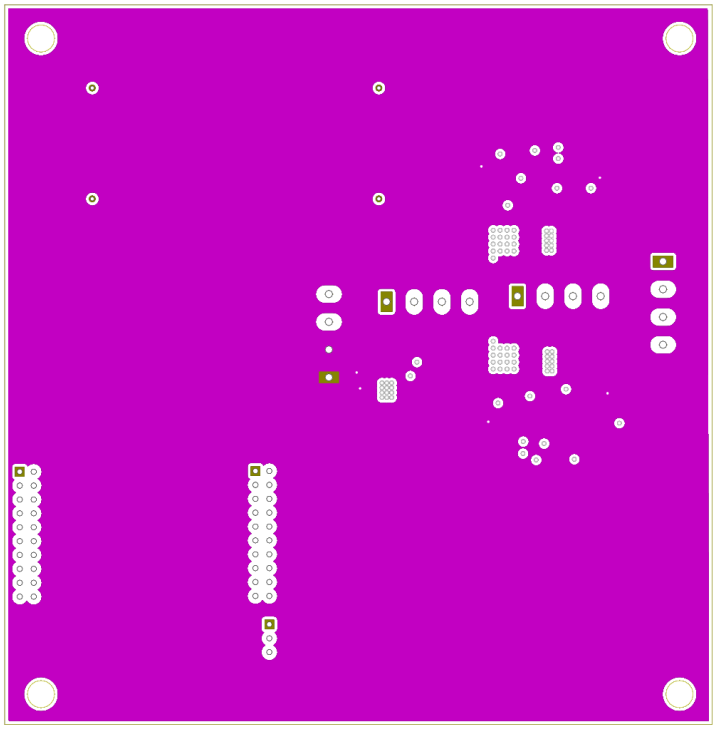

Figure B.4: Inner layer two of the PCB.

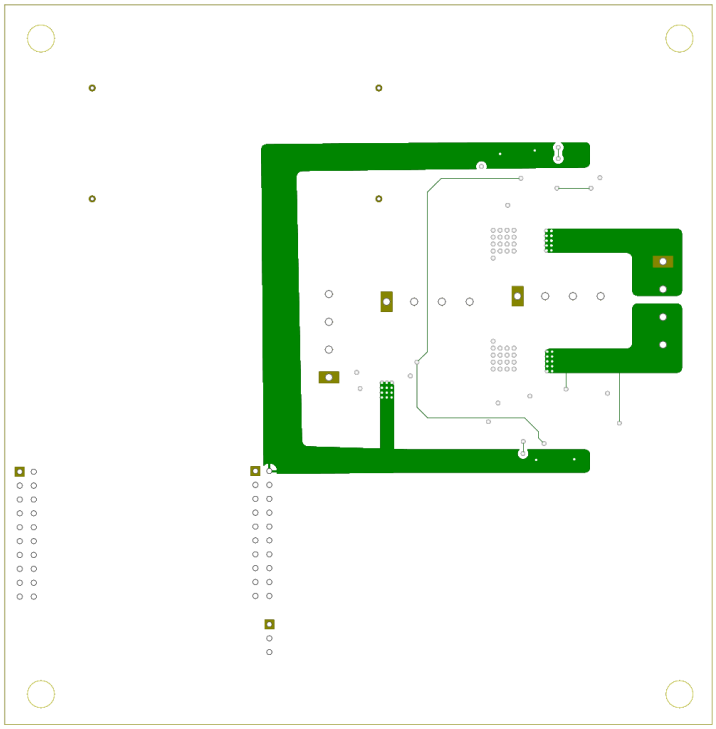

Figure B.5: Bottom layer of the PCB.