A Low Power Mutual Noise-Canceling Receiver Front-End with Blocker Tolerance for IoT Applications

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Technical Report No. UCB/EECS-2019-86
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2019/EECS-2019-86.html

May 18, 2019

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by

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A thesis submitted in partial satisfaction of the

requirements for the degree of

Master of Science

in

Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Ali M. Niknejad, Chair
Professor Osama Shana'a

Spring 2019

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Abstract

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An essential focus of developing Internet of Things (IoT) devices is designing ultra-low power radio receivers with low noise figure and high blocker rejection. This work will analyze the trade-offs associated with these important metrics in an ultra-low power blocker tolerant receiver and several noise-canceling LNA architectures. The design of a low power front-end is presented that utilizes mutual noise-cancellation and N-path filtering to reduce the noise figure and dramatically improve blocker tolerance in a 2.4 GHz direct-conversion Wi-Fi/Bluetooth receiver. From the two architectures that are developed, a minimum noise figure of 6.5 dB is achieved along with an out-of-band IIP3 of +0.36 dBm and power consumption of 0.83 mW in a 28 nm CMOS process.

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Acknowledgments

I would like to acknowledge Professor Ali M. Niknejad and Sashank Krishnamurthy for sharing their incredible technical advice with me throughout this entire process. I also want to thank Dr. Osama Shana'a from MediaTek who has graciously taken the time to provide me with some very valuable insights. I dedicate this thesis to my loving mother and father.

Chapter 1

Introduction

1.1 Motivation

With the next generation of wireless communications for consumer electronics, there will be an increase in demand for Internet of Things (IoT) devices that operate under Wi-Fi/Bluetooth standards and sub-6 GHz commercial bands. Therefore, current research is aimed at reducing the power consumption of the radio-frequency integrated circuits (RFICs) used by these devices. However, as the number of devices grows, receiver front-ends on these integrated radios will be required to operate with exceptional RF filtering for attenuating in-band and out-of-band blockers as well as low noise figure and low power consumption.

Previous work from the Berkeley Wireless Research Center (BWRC) [1, 2] has sought to bring the power consumption of these receivers into the sub-mW range while maintaining high tolerance for blocker signals, with an out-of-band IIP3 of +3.3 dBm. However, this

comes at the cost of a moderate noise figure (NF) of 11.9 dB. Meanwhile, [3] has utilized mutual noise-cancellation in a sub-mW low-noise amplifier (LNA) to reduce the NF to 2.8 dB. Incorporating this technique in a full receiver, [4] was able to achieve an NF value of 6.55 dB, but does not provide adequate RF filtering at the input and rejection of out-of-band blocker signals remains relatively low. [5] implements this filtering effect by integrating a noise-canceling LNA with a passive mixer at the antenna interface to attenuate out-of-band signals. Though this work reaches good out-of-band IIP3 of + 13.5 dBm and is able to achieve a NF of 1.9 dB, the power consumption (35.1 - 78 mW) is not feasible for low power IoT applications.

1.2 Outline

The objective of this work is to present a receiver front-end that breaks the trade-off between RF filtering and noise figure for a low power radio receiver. The proposed architecture combines the idea of using N-path filters at the antenna interface from [1, 2] with the mutual noise-cancellation LNA demonstrated in [3] to achieve low noise figure, high out-of-band rejection, and low power consumption. The N-path filter and LNA are designed for a 2.4 GHz Wi-Fi/Bluetooth direct-conversion receiver in a 28 nm CMOS process. All final results are produced using the spectreRF simulation tool in Cadence Virtuoso.

First, the ultra-low power blocker tolerant receiver in [1, 2] is analyzed in terms of out-of-band filtering and noise figure followed by a discussion of its drawbacks. Then, multiple

LNAs incorporating noise-cancellation are introduced that significantly reduce noise figure while maintaining low power [3, 6, 7]. Finally, the design of two novel receiver front-end architectures are presented, combing the use of N-path filtering for impedance matching and blocker tolerance with mutual noise-cancellation for low noise figure. The advantages and disadvantages of their inherent structures are weighed before a final comparison with current state-of-the-art receiver architectures is conducted.

Chapter 2

Ultra-Low Power Blocker Tolerant Receiver

2.1 N-Path Filter Passive Mixer

Before the ultra-low power blocker tolerant (ULP-BT) receiver architecture in [1, 2] is fully introduced, the 4-phase N-path filter from [8] and [9] will be discussed. Because of the inherent frequency mixing nature of the N-path filter, [1, 2] implements the passive mixers as 4-phase N-path filters in order to perform input impedance matching and provide high out-of-band rejection.

The basis of this architecture connects a quadrature passive mixer directly to the antenna, which is modeled as an input voltage V_{RF} and antenna impedance R_a shown in figure 2.1 below. The switches are driven by four non-overlapping LO pulses with 25% duty cycle, and

the outputs correspond with differential I and Q signals at baseband.

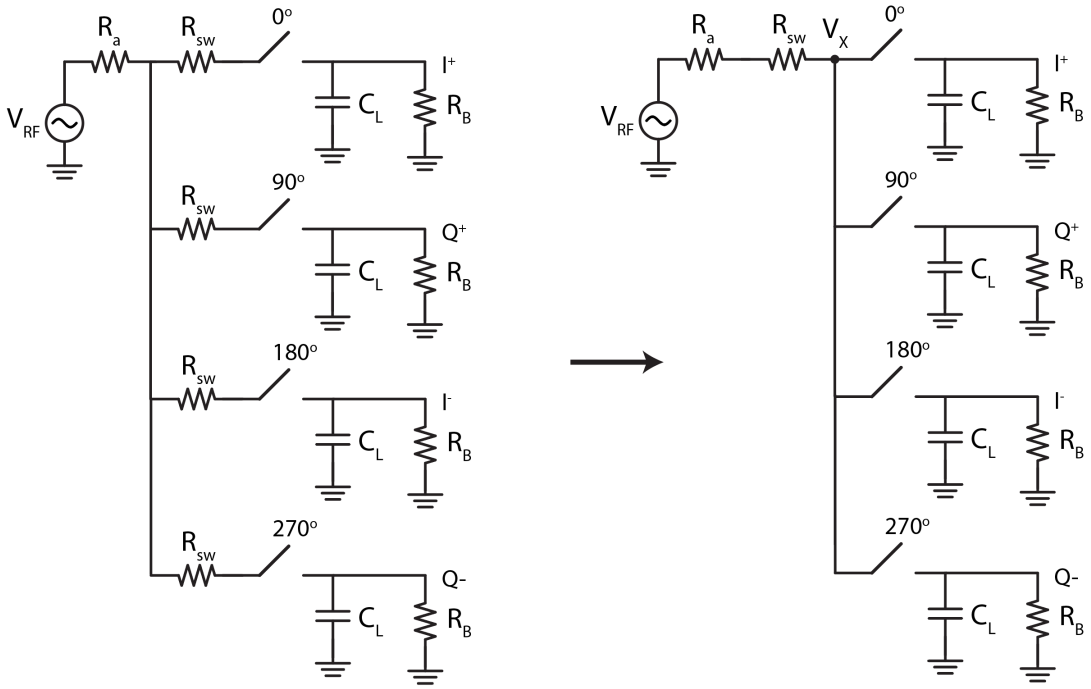


Figure 2.1: N-Path Filter and Equivalent Model

The switching transistors are modeled as ideal switches with switch resistance R_{sw}. Because the switches are driven by non-overlapping LO pulses, the antenna will only see one path at a time. As a result, the switches are modeled as four ideal switches with a single resistor of value R_{sw} in series with R_a, as shown in figure 2.1. A net antenna impedance is then defined as

$$R'_a = R_{sw} + R_a \tag{2.1}$$

Each switch is also loaded with a sampling capacitor C_L and resistor R_B. During each duty cycle of the LO when a switch is closed, the V_{RF} signal will be sampled on the respective C_L and appear on the virtual node V_x between R'_a and the ideal switches. If it is assumed

that the time constants $R_B C_L$ and $R'_a C_L$ are significantly greater than the LO period, then the voltage on these capacitors are approximated as constant during the on-period. For a given input waveform, the voltage at node V_x is plotted in figure 2.2 with the corresponding LO pulses.

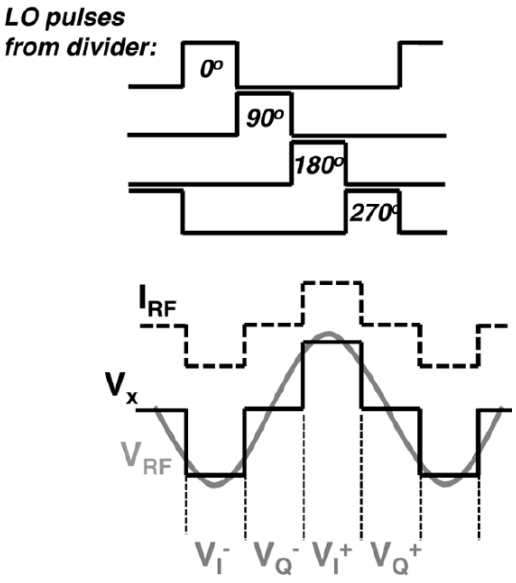


Figure 2.2: Voltages in the N-path Filter [9]

A derivation of the input impedance and equivalent LTI model is found in [8]. The result is reproduced below. The equivalent model is depicted in figure 2.3 and the input impedance seen by the antenna is

$$Z_{in} = R_{sw} + \gamma R_B || R_{sh} \tag{2.2}$$

where

$$\gamma = \frac{2}{\pi^2} \approx 0.203 \tag{2.3}$$

$$R_{sh} = R'_a \frac{4\gamma}{1 - 4\gamma} \approx 4.3 R'_a \tag{2.4}$$

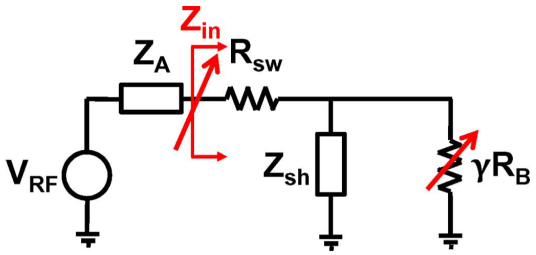


Figure 2.3: LTI Equivalent Circuit for the N-path Filter [9]

Based on the analysis in [8], it is determined that because of the higher order harmonics of LO on V_x, R_{sh} is dependent on the antenna impedance at each of these harmonics. Thus, R_{sh} represents the re-radiation power loss as a result of the baseband signal upconversion by these higher order harmonics. A spectrum showcasing this loss is depicted in figure 2.4.

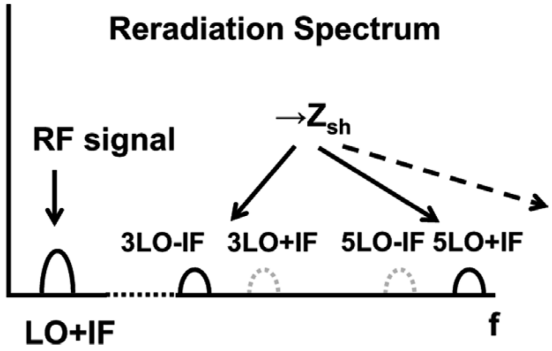


Figure 2.4: Spectrum of the Re-Radiation Losses at the Antenna Interface [9]

The dependence of the input impedance on R_B suggests that the baseband impedance is frequency translated to an RF impedance. Thus, in theory, an impedance with a low-pass effect and high roll-off can be designed at baseband, frequency translated to RF, and provide high out-of-band attenuation and impedance matching. Typically, this is more achievable

and area efficient than designing a high-Q band-pass filter at RF, hence the desirability of this architecture.

Taking $R_B \to 0$ and $R_B \to \infty$, the tuning capabilities of Z_{in} are limited by

$$R_{sw} < Z_{in} < R_{sw} + R_{sh} \tag{2.5}$$

This implies that the switch resistance must be sized properly to accommodate this inequality. Specifically, if $Z_{in} = R_a$ for matching, then $R_{sw} < R_a$ and $R_{sw} > R_a - R_{sh}$. The size of R_{sw} also affects out-of-band attenuation. This is seen if C_L is approximated as a short-circuit for high frequencies. The model in figure 2.1 then converges to a voltage divider with $V_x = \frac{R_{sw}}{R'_a + R_{sw}}$. Thus, smaller R_{sw} achieves higher out-of-band attenuation. It will also be shown later that $R_{sw} << R_a$ is desirable for low noise figure. Assuming the matched condition $Z_{in} = R_a$ and rearranging equation 2.2, the required R_B value is as follows

$$R_B = \frac{1}{\gamma} \frac{R_{sh}R_a - R_{sw}R_{sh}}{R_{sw} + R_{sh} - R_a} \tag{2.6}$$

Thus, designing the input impedance to match to an antenna impedance of R_a requires tweaking R_{sw} and R_B.

The LTI model is also used to simplify noise analysis. From figure 2.1, it is evident that the primary sources of noise originate from the antenna, switch resistance, and baseband resistor. Similar to previous analysis, the antenna and switch resistance noise are combined in R'_a by superposition. Thus, the current noise from R_B and R'_a are modeled through the equations shown below.

$$i^2_{n,b} = \frac{4kT}{\gamma R_B} \tag{2.7}$$

$$i_{n,a'}^2 = \frac{4kT}{R_a'} \tag{2.8}$$

The downconverted noise by the higher order harmonics of LO must also not be neglected. However, since R_{sh} represents the total loss from the higher order harmonics of LO, it is also used to model this noise contribution, as shown in figure 2.5.

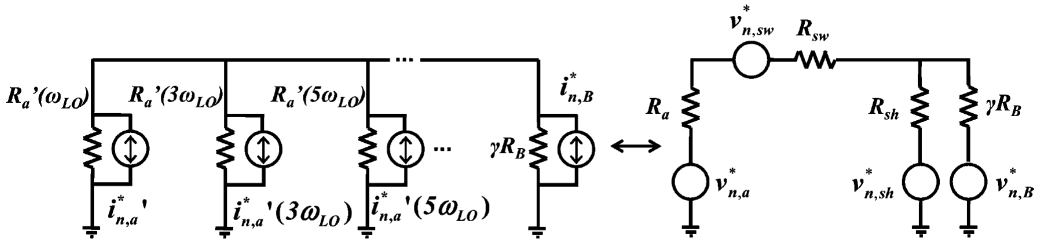


Figure 2.5: Equivalent Noise Model of the N-Path Filter [8]

The final noise figure is then calculated as

$$NF = 1 + \frac{v_{n,sw}^2}{v_{n,a}^2} + \frac{v_{n,sh}^2}{v_{n,a}^2}\left(\frac{R_a + R_{sw}}{R_{sh}}\right)^2 + \frac{v_{n,B}^2}{v_{n,a}^2}\left(\frac{R_a + R_{sw}}{\gamma R_B}\right)^2 \tag{2.9}$$

From this equation, it is evident that the condition $R_{sw} << R_a$ will achieve lower noise figure. A higher value of R_B also decreases the noise figure, though in practice, R_B is limited by the input impedance matching requirement. Thus, a trade-off is made between noise figure and input impedance matching if low noise figure is particularly desirable.

2.2 Receiver Architecture

Traditional receiver architectures typically exhibit a mixer-first or LNA-first configuration in the front-end. The former provides better out-of-band rejection, as passive mixers perform frequency conversion of a low-pass baseband impedance to a matched band-pass RF input impedance at the antenna interface. However, this comes at the cost of power consumption in the baseband amplifiers for a given noise figure. Meanwhile, an LNA-first topology achieves lower power consumption for the same noise figure, but its rejection is limited by the wideband input impedance matching. [1, 2] has presented an ULP-BT receiver architecture to break this trade-off that will be discussed in this chapter.

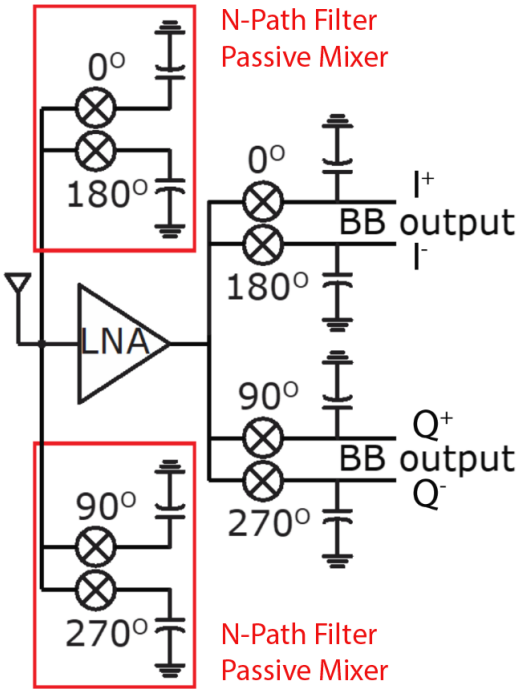


Figure 2.6: N-Path Filter Passive Mixer in Shunt [2]

Figure 2.6 demonstrates the modification that [1, 2] has made to the standard LNA-first configuration. A passive mixer implemented as a 4-phase N-path filter is placed in shunt with the input of the LNA to reintroduce the frequency conversion effect. For consistency, the downconversion mixers at the output of the LNA are also 4-phase N-path filters.

However, as discussed earlier, because of the $R_{sw} << R_a$ condition for impedance matching and low noise figure as well as the re-radiation losses modeled through R_{sh}, perfect in-band matching cannot be achieved with the configuration shown in figure 2.6. Figures 2.7 and 2.8 compare the input impedance performance of the parallel mixer configuration with the traditional LNA-first architecture and showcase the inability to achieve perfect in-band matching.

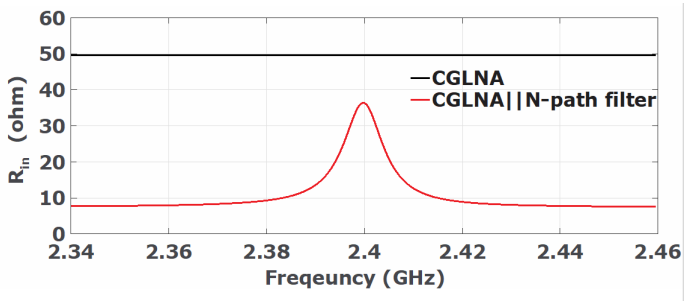


Figure 2.7: LNA-first vs. LNA-first + N-Path Filter Input Impedance [2]

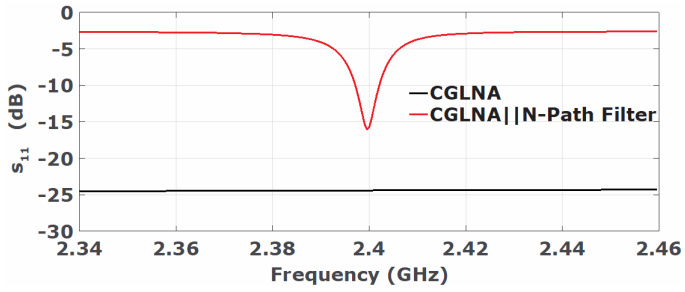


Figure 2.8: LNA-first vs. LNA-first + N-Path Filter S_{11} [2]

To compensate for this loss and boost the net R_{in} seen by the antenna, a negative baseband resistance is introduced at the output of the filters, as shown in figure 2.9. Based on the LTI model in figure 2.3, this is equivalent to adding a negative resistance in parallel with R_{sh}, increasing the effective R_{in} seen by the antenna. In an effort to conserve power and reuse the existing baseband signal path, the negative R_{BB} is realized as a positive feedback g_m generated from the original signal path.

As shown in figure 2.9, an input transformer with a transform ratio of 1:3 is used to increase the antenna's impedance as seen by the LNA and lower its g_m requirement for input impedance matching. The capacitively-cross-coupled common-gate (CCC-CG) LNA that is used in this architecture will be introduced later in this chapter.

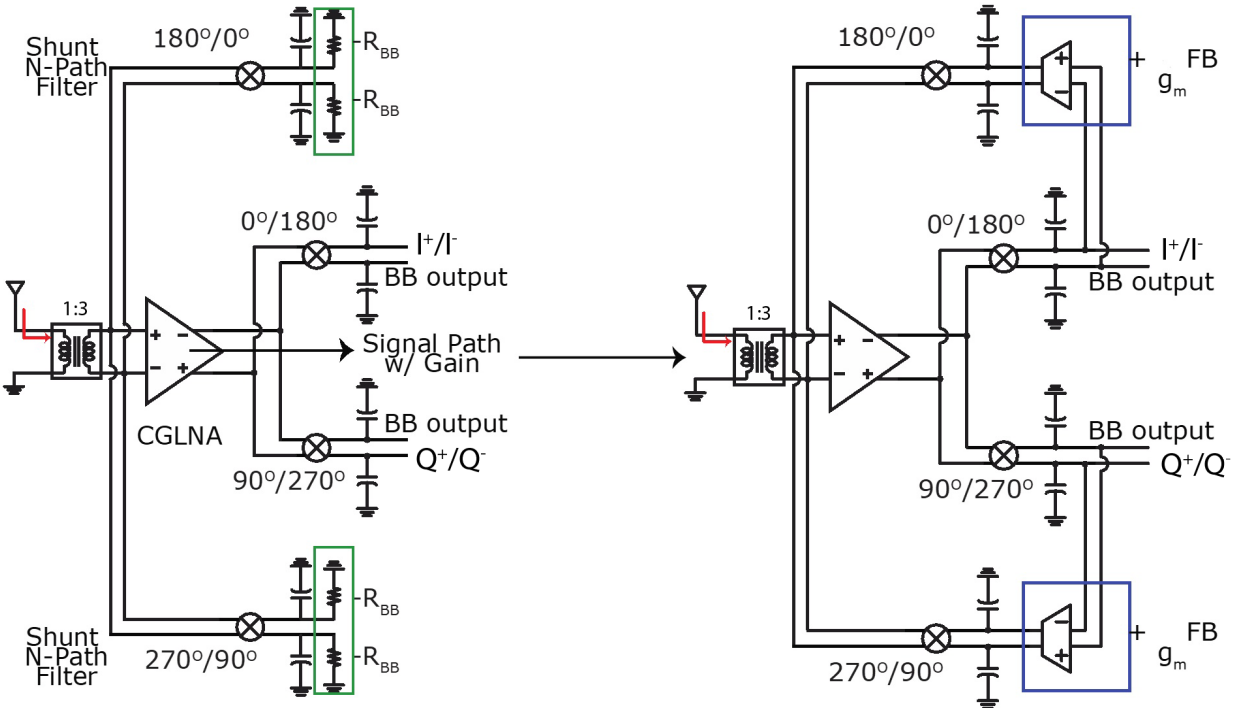


Figure 2.9: Frequency Translation of the Baseband Impedance with Positive Feedback [2]

A derivation to design the baseband g_m for matching is presented in [1]. The result to that approach follows equation 2.6 and also considers the parallel input impedance of the LNA. After finding this value of g_m, the in-band input impedance is matched perfectly to the antenna impedance while maintaining high out-of-band rejection, as depicted in figures 2.10 and 2.11 below. With this implementation, an out-of-band rejection of +3.3 dBm was achieved [1].

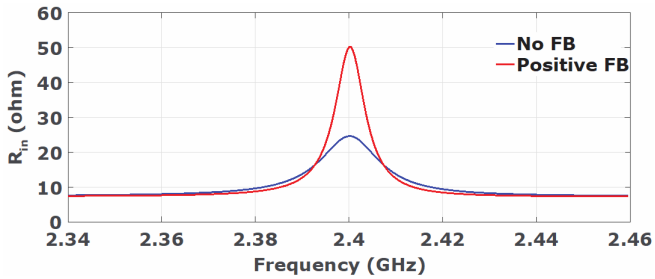


Figure 2.10: Input Impedance With and Without Positive Feedback [2]

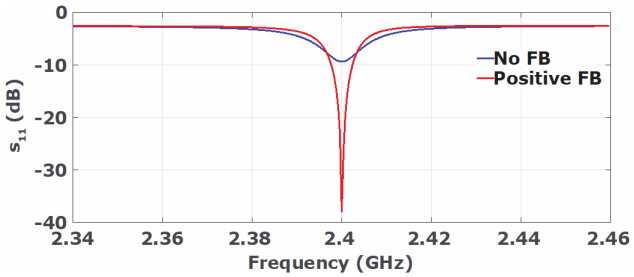


Figure 2.11: S_{11} With and Without Positive Feedback [2]

2.3 Capacitive Cross-Coupled Common-Gate (CCC-CG) LNA

The LNA for the ULP-BT receiver architecture from [1, 2] was implemented using a fully-differential capacitive cross-coupled common-gate (CCC-CG) LNA [10]. This was chosen primarily because of its g_m-boosting effect that is able to decrease the power consumption for a given noise figure and matching requirement. A model for this technique is shown below in figure 2.12.

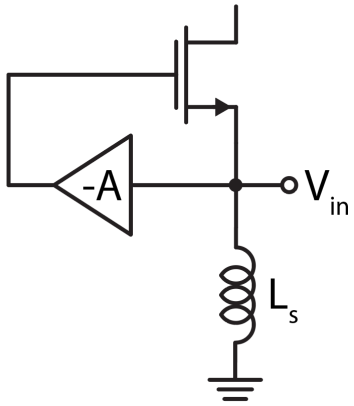


Figure 2.12: Common-Gate LNA g_m-Boosting Model

By inspection, the effective transconductance of this amplifier is given by $G_{m,eff} = (1+A)g_m$ from the negative feedback configuration. To achieve the $-A$ amplification in a differential LNA, cross-coupled capacitors are used as illustrated in figure 2.13.

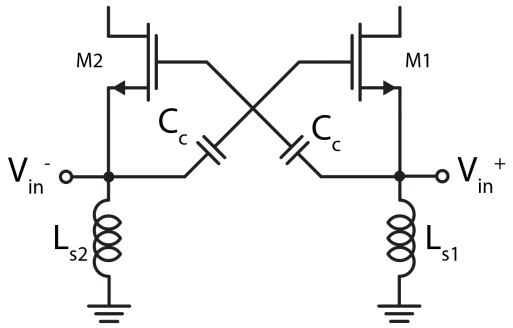


Figure 2.13: CCC-CG LNA

Neglecting the effects of C_{gd}, A becomes the voltage division ratio of the capacitors given by

$$A \approx \frac{C_c}{C_c + C_{gs}} = \frac{1}{1 + \frac{C_{gs}}{C_c}} \tag{2.10}$$

resulting in an effective $G_{m,eff}$ of

$$G_{m,eff} = \left(\frac{C_{gs} + 2C_c}{C_{gs} + C_c}\right) g_m \approx 2g_m \tag{2.11}$$

assuming $C_c >> C_{gs}$.

The input impedance of a standard CG LNA is defined as $Z_{in} \approx \frac{1}{g_m}$. In this configuration the input impedance becomes $Z_{in} \approx \frac{1}{G_{m,eff}} \approx \frac{1}{2g_m}$, decreasing the g_m requirement by a factor of 2 for the same input impedance matching condition. This also reduces the power consumption of the CG stage by a factor of 2.

Additionally, ignoring the effect of gate noise and only considering the drain current noise, the noise figure of the CG LNA is expressed as

$$NF = 1 + \frac{\gamma}{\alpha}\frac{g_m}{\frac{1}{R_s}}\left(\frac{1}{G_{m,eff}R_s}\right)^2 = 1 + \frac{1}{4}\frac{\gamma}{\alpha}\frac{g_m}{\frac{1}{R_s}}\left(\frac{1}{g_m R_s}\right)^2 \tag{2.12}$$

γ and α are bias dependent parameters and R_s is the input source resistance. Thus, for a given g_m value, the noise figure will be reduced by approximately a quarter compared to the standard CG LNA. In other words, a given noise figure now only requires half of the original g_m and current consumption. As a result, noise figure and input impedance matching is achieved for half the power consumption. Implemented in the ULP-BT receiver, this LNA reached a minimum total noise figure of 11.9 dB [1].

2.4 Architecture Drawbacks

Nevertheless, this architecture has its shortcomings. Firstly, the use of feedback to perform input impedance matching is only viable for continuous wave input signals. Because of the time delay associated with the feedback path, modulated signals that arrive at varying time intervals cannot be matched if they do not propagate fast enough through the feedback path. In order to combat this, a synchronization mechanism must be introduced at the antenna interface such that the signal at the LNA input matches that of the feedback path. The negative g_m stage also does not track well over PVT and may cause instability issues if the positive feedback path introduces a 360° phase shift. Additionally, the noise figure of this architecture is rather high compared to previous work and can be further optimized. A subsequent chapter will introduce a design that eliminates the positive feedback path and focuses on achieving a lower noise figure with low power while preserving the input impedance matching and out-of-band rejection introduced through the N-path filter.

Chapter 3

Noise-Canceling LNA Architectures

3.1 Common-Source Noise-Canceling LNA

Noise-cancellation is another technique introduced in recent literature as a means of reducing noise figure [3, 6, 7] and will be the primary method of achieving low noise in the design presented in the next chapter. Fundamentally, noise cancellation introduces an additional auxiliary noise-canceling path that is able to destructively add noise while constructively adding signals at the output, as illustrated in figure 3.1. Multiple topologies will be explored in this chapter that take advantage of this idea.

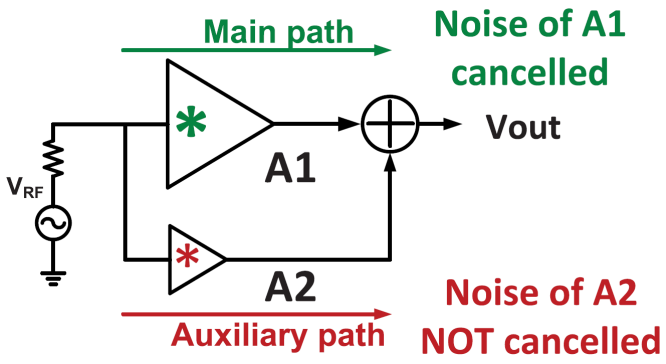


Figure 3.1: Conceptual Block Diagram of Noise-Cancellation [3]

The first utilizes a common-source amplifier with the gate and drain connected in resistive feedback as the main signal path, shown in figure 3.2.

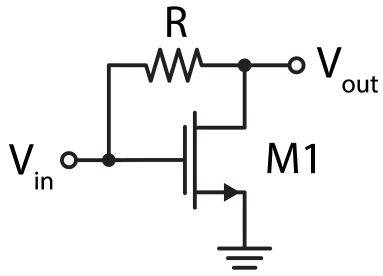


Figure 3.2: Common-Source LNA with Resistive Feedback

By inspection, the input impedance and voltage gain is determined as follows

$$Z_{in} \approx \frac{1}{g_{m,1}} \tag{3.1}$$

$$A_{v,i} = 1 - g_{m,1}R \tag{3.2}$$

In analyzing the noise characteristics of M1 using figure 3.3, it is observed that the noise voltage at V_Y possess the same sign as that of V_X, while the signal voltages are opposite in sign.

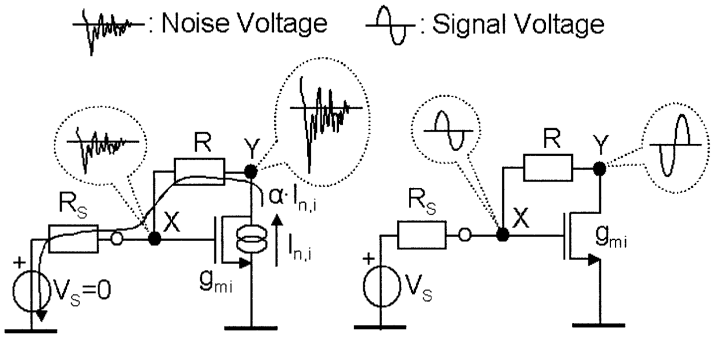


Figure 3.3: Noise and Signal Voltages in the Resistive Feedback Common-Source LNA [6]

If the difference between V_X and V_Y is taken at the output, then the noise voltages are destructively canceled while the signal voltages are constructively added. This is implemented by amplifying and inverting the voltage at V_X and adding it to V_Y, as depicted in figure 3.4.

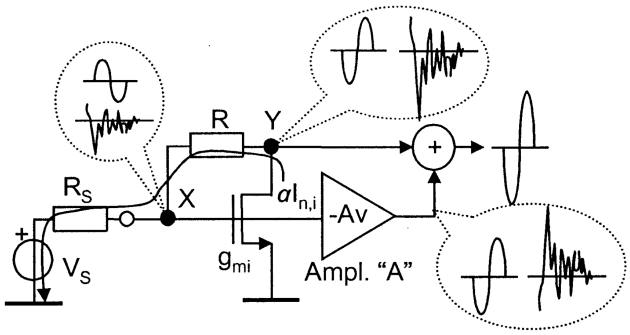


Figure 3.4: Noise-Cancellation in the Resistive Feedback Common-Source LNA [6]

Assuming a drain noise current of $i_{d,n}$, the noise voltages at V_X and V_Y are as follows.

$$V_{X,n} = i_{d,n} R_s \tag{3.3}$$

$$V_{Y,n} = i_{d,n}(R_s + R) \tag{3.4}$$

Thus, the necessary $A_{v,n}$ needed to cancel the noise at V_o is

$$V_{o,n} = V_{Y,n} - V_{X,n}A_{v,n} \tag{3.5}$$

$$= i_{d,n}(R_s + R - A_{v,n}R_s) = 0 \Rightarrow A_{v,n} = 1 + \frac{R}{R_s} \tag{3.6}$$

Under a matched condition such that $\frac{1}{g_{m,1}} = R_s$, the gain of the signal path becomes

$$A_v = 1 - g_{m,1}R - A_{v,n} = 1 - \frac{R}{R_s} - 1 - \frac{R}{R_s} = -2\frac{R}{R_s} \tag{3.7}$$

Figure 3.5 illustrates the full implementation using another common-source stage as $A_{v,n}$ and a source-follower as the adder stage.

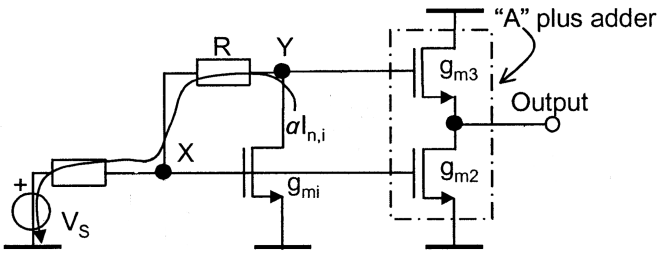


Figure 3.5: Full Implementation of the Noise-Canceling Common-Source LNA [6]

In this implementation, the required $g_{m,2}$ and $g_{m,3}$ to perform noise cancellation must satisfy

$$A_{v,n} = \frac{g_{m,2}}{g_{m,3}} = 1 + \frac{R}{R_s} \tag{3.8}$$

This technique also cancels any small signal current that is modeled on the drain of M1 (i.e. flicker noise, gate resistance thermal noise, bias noise on V_Y, distortion). However, the noise of R is only partially canceled. If the noise of R is modeled as two uncorrelated noise currents on nodes X and Y, then only the noise on node Y is canceled through the noise-cancellation mechanism.

From [6], assuming a matched condition such that $\frac{1}{g_{m,1}} = R_s$ the noise figure expression is written as

$$NF = 1 + NF_{M1} + NF_R + NF_{M2,M3} \tag{3.9}$$

$$NF_{M1} = \frac{\gamma g_{d0}}{R_s}\left(\frac{R + R_s - A_{v,n}R_s}{A_v}\right)^2 \tag{3.10}$$

$$NF_R = \frac{1}{A_{v,n} - 1} = -\frac{2}{A_v} \tag{3.11}$$

$$NF_{M2,M3} = \frac{\gamma g_{d0}}{g_{m,1}}\frac{8 - 6A_v + A_v^2}{g_{m,2}R_sA_v^2} \tag{3.12}$$

After noise cancellation (i.e. $A_{v,n} = 1 + \frac{R}{R_s}$),

$$NF_{M1} = 0 \tag{3.13}$$

$$NF_R = \frac{R_s}{R} \tag{3.14}$$

$$NF_{M2,M3} = \frac{\gamma g_{d0}}{g_{m,1}}\frac{1}{g_{m,2}}\left(\frac{1}{R_s} + \frac{3}{R} + \frac{2R_s}{R^2}\right) \tag{3.15}$$

From these equations, it is clear that the noise from R, M2, and M3 are not canceled. The lack of cancellation in the auxiliary path (M2 and M3) will also be present in the common-gate noise-canceling LNA discussed next, but is remedied with a mutual noise-cancellation configuration in the subsequent section. From equation 3.15, the noise figure is further optimized by increasing $g_{m,2}$ at the cost of power consumption. However, in order to maintain the noise-canceling condition such that $\frac{g_{m,2}}{g_{m,3}} = 1 + \frac{R}{R_s}$, either R or $g_{m,3}$ must also be increased. Evidently, increasing R also decreases noise figure. Note, the value of $g_{m,1}$ must be preserved for input impedance matching.

3.2 Common-Gate Noise-Canceling LNA

The second architecture follows the same vein as the first, but instead uses a common-gate amplifier as the main path, as depicted in figure 3.6.

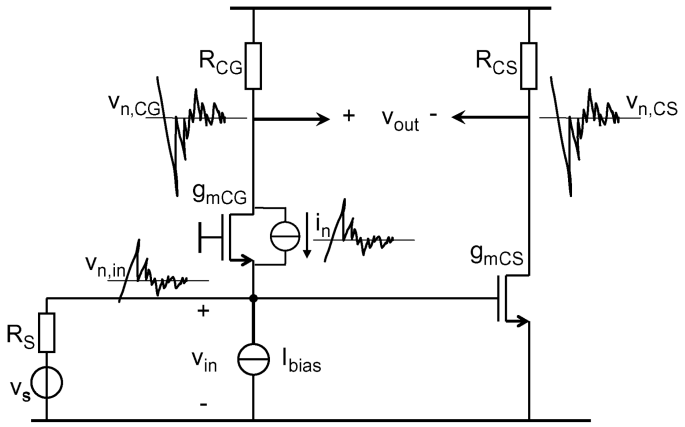


Figure 3.6: Noise-Cancellation in the Common-Gate LNA [7]

Using the small-signal noise model, $v_{n,in}$, $v_{n,CG}$, and $v_{n,CS}$ are derived as

$$v_{n,in} = i_n R_s \frac{\frac{1}{g_{m,CG}}}{R_s + \frac{1}{g_{m,CG}}} \tag{3.16}$$

$$v_{n,CG} = -i_n R_{CG} \frac{\frac{1}{g_{m,CG}}}{R_s + \frac{1}{g_{m,CG}}} \tag{3.17}$$

$$v_{n,CS} = A_{v,CS} v_{n,in} = A_{v,CS} i_n R_s \frac{\frac{1}{g_{m,CG}}}{R_s + \frac{1}{g_{m,CG}}} \tag{3.18}$$

Because $A_{v,CS} < 0$, $v_{n,CG}$ and $v_{n,CS}$ will have the same sign and the differential output is able to perform noise-cancellation. Equating 3.17 and 3.18 results in a noise-cancellation gain requirement on the CS stage of

$$A_{v,CS} = -g_{m,CS} R_{CS} = -\frac{R_{CG}}{R_s} \tag{3.19}$$

The signal characteristics of the LNA are also derived below.

$$V_{CG} = g_{m,CG} V_s \frac{\frac{1}{g_{m,CG}}}{R_s + \frac{1}{g_{m,CG}}} R_{CG} \tag{3.20}$$

$$V_{CS} = A_{v,CS} V_s \frac{\frac{1}{g_{m,CG}}}{R_s + \frac{1}{g_{m,CG}}} \tag{3.21}$$

The output signal taken differentially between the CG and CS stages are balanced and behave as a balun if the two expressions above are equated and solved for $A_{v,CS}$. Assuming the necessary value on $A_{v,CS}$ for noise-cancellation, the following is deduced.

$$|A_{v,CS}| = g_{m,CG} R_{CG} = \frac{R_{CG}}{R_s} \Rightarrow R_s = \frac{1}{g_{m,CG}} = Z_{in,CG} \tag{3.22}$$

This suggests that output balancing and noise-cancellation also results in input matching. The noise figure of this configuration is derived in [7] and written below.

$$NF = 1 + NF_{CG} + NF_{CS} + NF_{R_{CG,CS}} \tag{3.23}$$

$$NF_{CG} = \frac{\gamma g_{m,CG}}{R_s} \left(\frac{R_{CG} - R_s g_{m,CS} R_{CS}}{A_v} \right)^2 \tag{3.24}$$

$$NF_{CS} = \frac{\gamma g_{m,CS}}{R_s} \left(\frac{R_{CS}(1 + g_{m,CG} R_s)}{A_v} \right)^2 \tag{3.25}$$

$$NF_{R_{CG,CS}} = \frac{R_{CG} + R_{CS}}{R_s} \left(\frac{1 + g_{m,CG} R_s}{A_v} \right)^2 \tag{3.26}$$

where $A_v = g_{m,CG} R_{CG} + g_{m,CS} R_{CS}$. With noise cancellation, $NF_{CG} = 0$, though the CS transistor and load resistors still contribute additional noise. In order to cancel the noise in this auxiliary path and eliminate additional resistor noise, a mutual noise-canceling LNA is introduced in the next section.

3.3 Ultra-Low Power Mutual Noise-Canceling LNA

In either of the above designs, it is evident that only the noise on the main path is canceled, while the auxiliary path noise still degrades the noise figure. The ultra-low power LNA in [3] alleviates this issue by combining the two topologies to perform noise cancellation in both paths. An innovation on this architecture for the low power blocker tolerant receiver front-end will be discussed in the next chapter. The mutual noise-canceling LNA is shown below in figure 3.7.

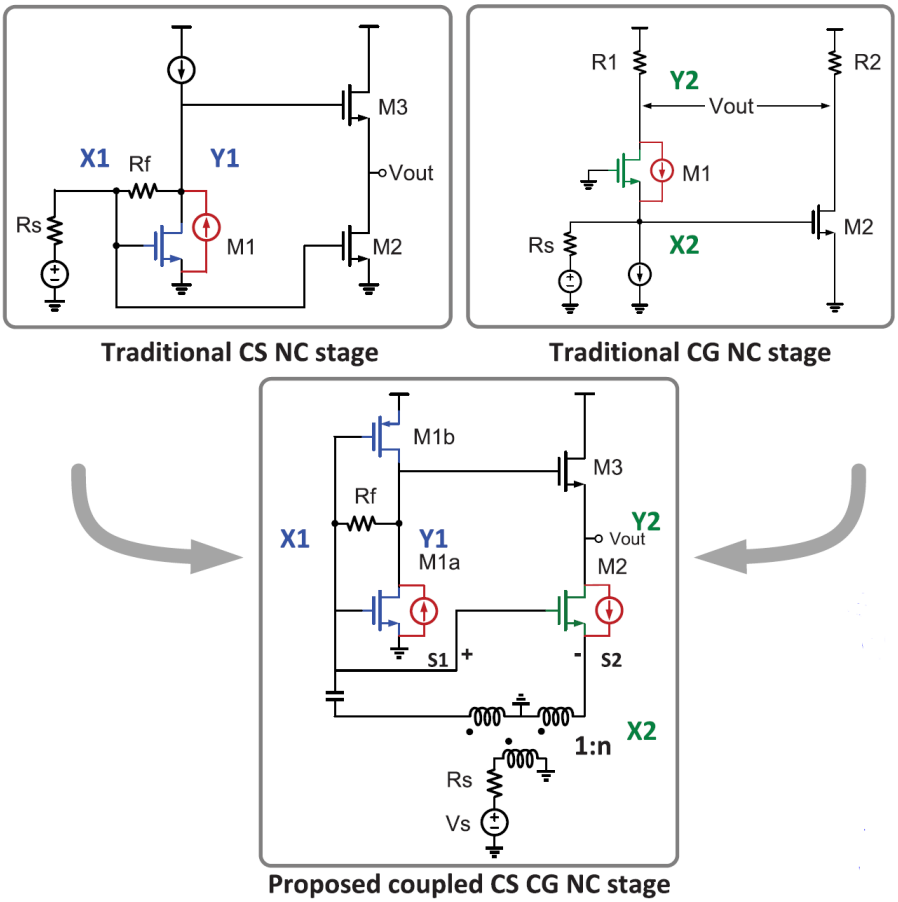


Figure 3.7: Mutual Noise-Canceling LNA [3]

A step-up balun is used at the antenna interface to provide a higher impedance for matching at the inputs of M1A/M1B and M2. This is able to decrease total power consumption by the square of the balun transform ratio, as the input impedance on either of the balun's secondary terminals is defined by $\frac{1}{g_m}$. In this particular design, a transform ratio of 1:3 was used. Thus, the differential impedance seen across S1 and S2 with a 50 Ω source is 450 Ω, and the single-ended impedance on S1 and S2 is $R_{s,1} = R_{s,2} = 225\ \Omega$.

Though a M1B load is added to the common-source stage, the noise-canceling operation remains the same compared to that of the common-source noise-canceling LNA introduced earlier, as the noise current of M1B is superimposed on M1A. Shown below in figure 3.8 is the effect of mutual noise-cancellation, which operates in a similar fashion compared to the noise-canceling common-source and common-gate LNAs introduced earlier.

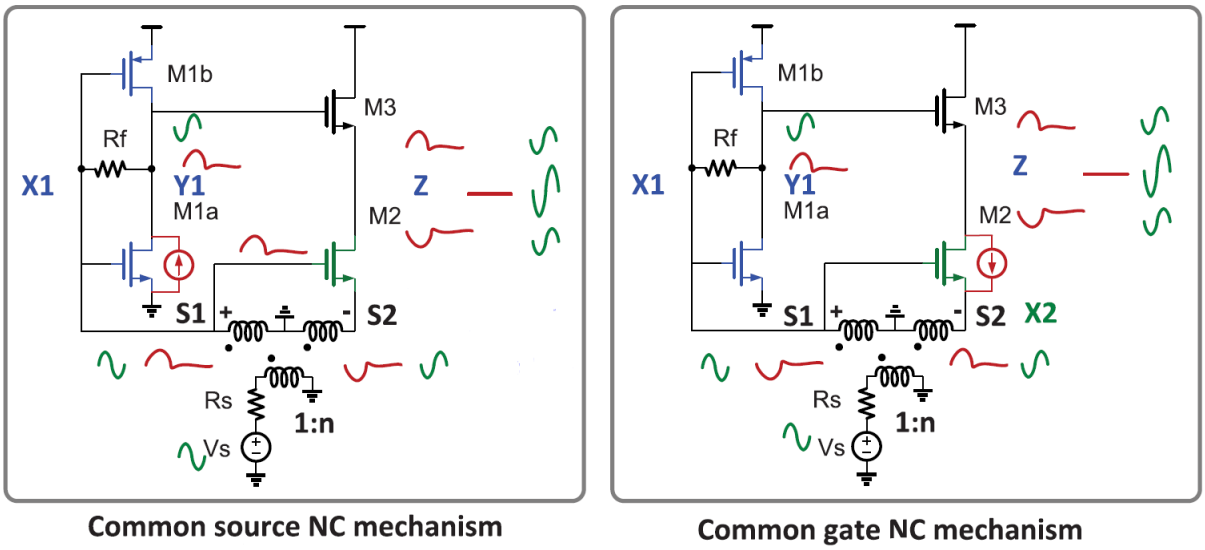


Figure 3.8: Noise-Cancellation Mechanism in the Mutual Noise-Canceling LNA [3]

Figure 3.8 shows that the signal voltages propagating through M2 and M1A/M1B will add constructively at the output for either mechanism. The noise-cancellation will be discussed below.

In the case of the common-source noise-cancellation mechanism, M1A/M1B constitutes the main path while M2 is used as the auxiliary path for noise cancellation. The noise current of M1A/M1B flows through R_f and produces a noise voltage at Y1 and X1. This current continues to flow through $R_{s,1}$, producing a noise voltage at S1 that is inverted through the balun at S2. Because a differential signal now appears on the gate and source of M2, its effective g_m is doubled. The noise voltage at S1 is also inverted through the amplification of M2 and appears at Z. Likewise, the Y1 noise voltage is present at Z due to the M3 source follower. These two noise voltages add destructively and are canceled at the output. Following the analysis presented earlier in the chapter, the required gain for the second stage is derived for this model as

$$A_{v,2} = 1 + \frac{R_f}{R_{s,1}} = \frac{2g_{m,2}}{g_{m,3}} \tag{3.27}$$

Assuming a matched condition, namely $R_{s,1} = \frac{1}{g_{m,1}}$ and $R_{s,2} = \frac{1}{2g_{m,2}}$, the following expression for $g_{m,3}$ is derived.

$$g_{m,3} = \frac{1}{R_f + R_{s,1}} \tag{3.28}$$

Thus, for this particular value of $g_{m,3}$, better input matching suggests better noise-cancellation of M1N/M1P.

For the common-gate stage, M2 now becomes the main path while M1A/M1B serves as the auxiliary path for noise cancellation. The noise current of M2 flows through S2 and produces a noise voltage at this node. However, because a current is also generated through M3 in the same direction, the noise voltage on Z is inversely correlated with that of S2. The noise voltage at S2 is then inverted through the balun and reproduced at S1, where it is inverted again by the amplification of M1A/M1B and appears at Y1. This noise voltage is out-of-phase with that of Z, and thus the source-follower M3 is able to cancel these two noise voltages. This particular noise cancellation technique is modeled in figure 3.9.

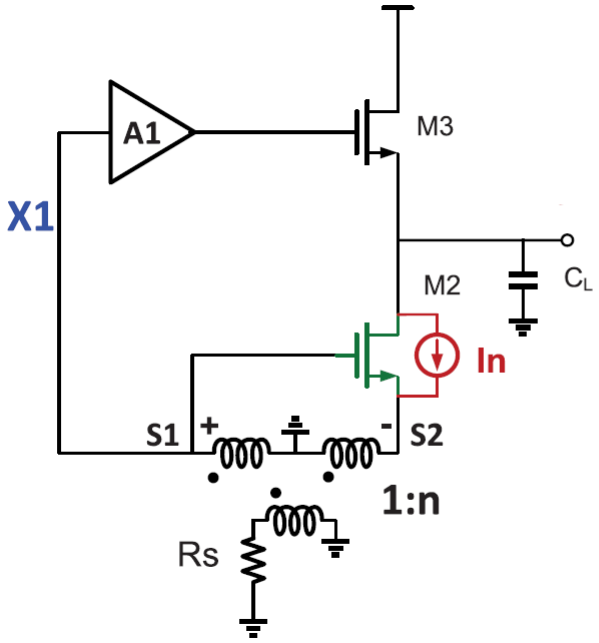


Figure 3.9: Noise-Cancellation Model for M2 [3]

Using the small signal model and assuming a voltage of V_s on S2 (and thus $-V_s$ on S1) and V_o on the output node, the derivation below demonstrates that only 50% of M2's noise is canceled. However, this is under the assumption that both stages are matched to the input impedance ($R_s = R_{s,1} = R_{s,2} = \frac{1}{g_{m,1}} = \frac{1}{2g_{m,2}}$), full-cancellation occurs in A1 ($g_{m,3} = \frac{1}{R_f+R_s}$), and frequency response effects are neglected.

$$\frac{V_s}{R_s} = -2g_{m,2}V_s + I_n \Rightarrow V_s = I_n \frac{1}{\frac{1}{R_s} + 2g_{m,2}} = \frac{1}{2} I_n R_s \tag{3.29}$$

$$= g_{m,3}(-A_{v,1}V_s - V_o) \Rightarrow V_s = -\frac{V_o}{A_{v,1} + \frac{1}{g_{m,3}R_s}} = -\frac{V_o}{1 - g_{m,1}R_f + \frac{R_f+R_s}{R_s}} \tag{3.30}$$

$$\begin{aligned} V_s = V_s \Rightarrow V_o &= -\frac{1}{2} I_n R_s (1 - g_{m,1}R_f + \frac{R_f}{R_s} + 1) \\ &\approx -\frac{1}{2} I_n R_s (-g_{m,1}R_f + \frac{R_f}{R_s} + 1) \\ &= -\frac{1}{2} I_n R_s (-\frac{R_f}{R_s} + \frac{R_f}{R_s} + 1) \\ &= -\frac{1}{2} I_n R_s \end{aligned} \tag{3.31}$$

Additionally, the nonlinearity of M1A/M1B and M2 due to input and output conductance is modeled as a dependent current source connected between the drain and source of the respective transistors, similar to figure 3.8. These current sources are dependent on V_{gs} and V_{ds} and thus model the g_m and g_{ds} nonlinearities as well as other effects such as drain-induced barrier lowering. This model suggests that distortion undergoes the same cancellation processes described above.

Chapter 4

Receiver Front-End Design

4.1 Design Approach

The primary goal of this design is to improve the performance of [1, 2] by utilizing a mutual noise-canceling LNA. The new architecture incorporates out-of-band filtering, input impedance matching, and lower noise figure and borrows the idea from [1, 2] of integrating a 4-phase N-path filter as a passive mixer at the input of a mutual noise-canceling LNA [3]. The two architectures that will be presented in this chapter differ based on the position of the mixer within the M2 stage of the mutual-noise canceling LNA. A step-up balun with a transform ratio of 1:3 is used at the antenna interface for the same reasons as discussed in the previous chapter. It is extracted using EMX simulation and mimics that of [1, 2] in terms of loss and other performance characteristics. In this implementation, the balun does not significantly degrade performance.

Positive feedback is not utilized in this case to eliminate the need for input signal synchronization, reduce power consumption from the additional mixers, and decrease design complexity. To compensate for the impedance-boosting effect of the positive feedback and negative g_m combination, full input matching is achieved with a more precise design of the mixers and baseband impedance. This chapter will compare and contrast the two variations that follow this general mixer-first architecture.

4.2 Symmetrical Mixer-First Architecture

The proposed symmetrical mixer-first architecture is shown below in figures 4.1 and 4.2. The general idea integrates two N-path filter passive mixers at the inputs of the M1A/M1B (A1) and M2 (A2) stages of the mutual noise-canceling LNA discussed in the previous chapter.

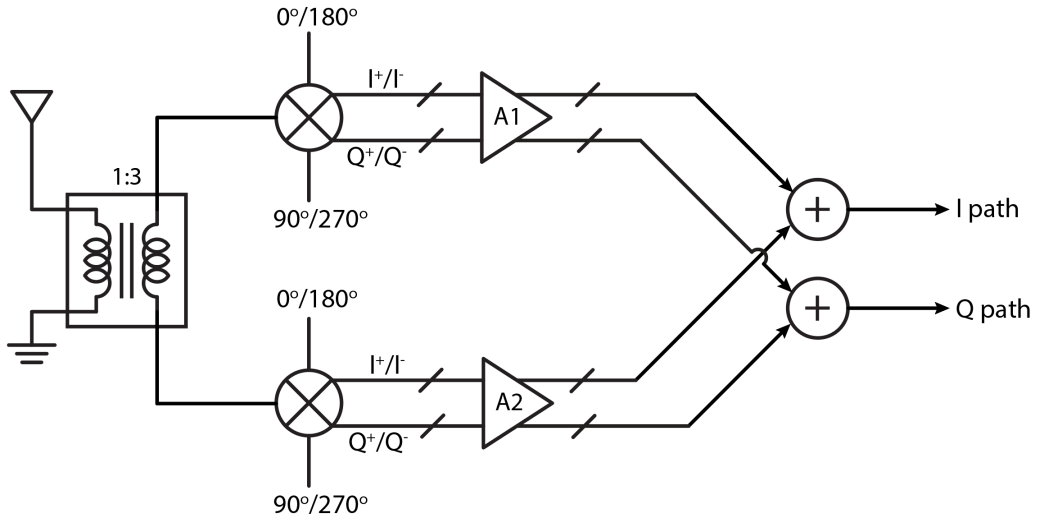


Figure 4.1: Block Diagram of the Mutual Noise-Canceling LNA with a Symmetrical Mixer Input

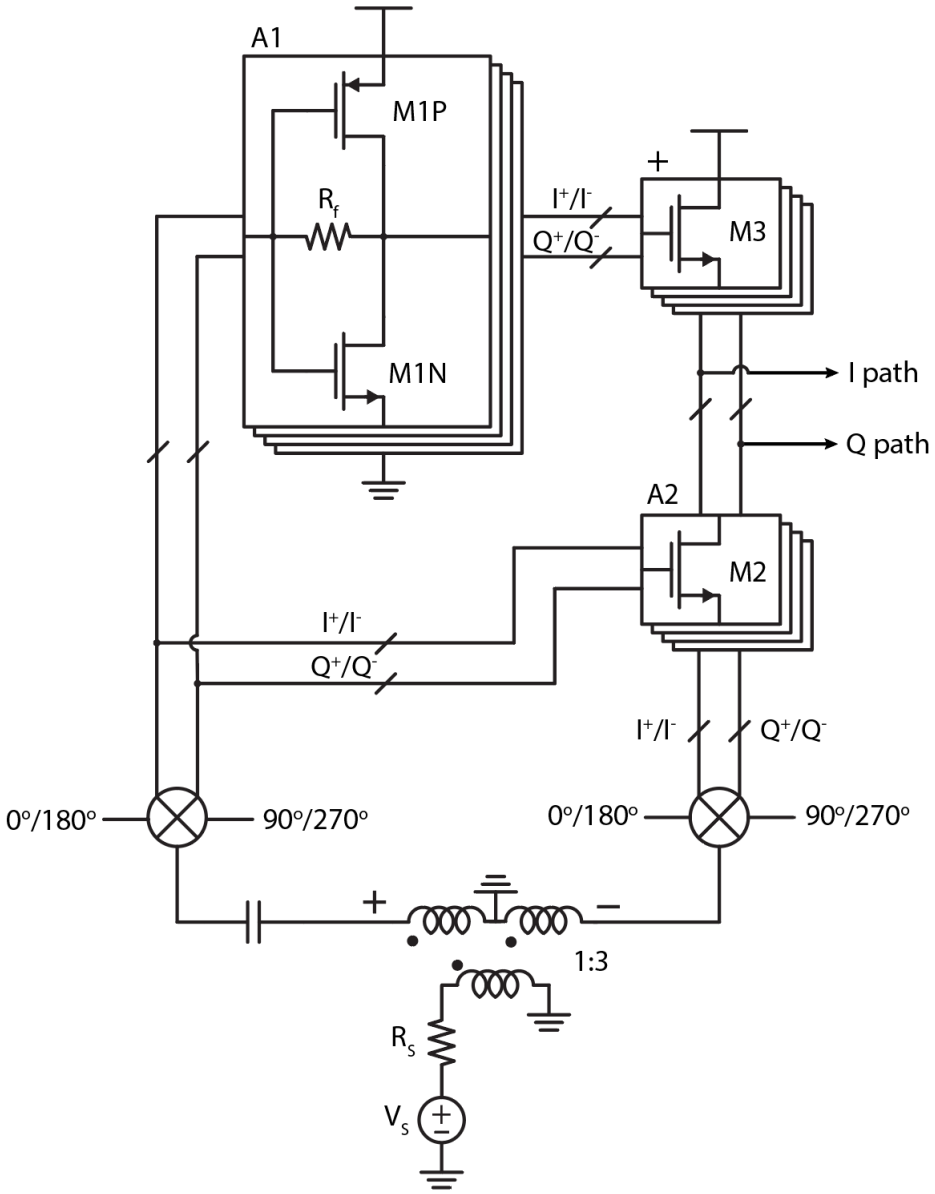


Figure 4.2: Mutual Noise-Canceling LNA with a Symmetrical Mixer Input

The primary advantage of utilizing this topology is the balanced input matching and out-of-band filtering that arises from mixers at both stages' inputs. With this configuration, the baseband input impedance of A1 and A2 are both upconverted to RF and designed to

provide equivalent input impedance matching on both secondary terminals of the balun. This introduces a differential input impedance that is matched to the transformed 50 Ω source. The improvement in matching also provides better mutual noise-cancellation for a given value of $g_{m,3}$, as discussed in the previous chapter. Additionally, out-of-band blocker rejection and IIP3 is enhanced compared to the subsequent topology because of the mixers at the input of both stages.

However, this configuration does have its drawbacks. For instance, because both stages of the LNA are operating at baseband, additional overhead on power consumption is introduced, as each mixer contains four outputs. However, because frequency translation of the impedance scales the $\frac{1}{g_m}$ input impedance by a factor of $\gamma \approx 0.203$ from equation 2.3, g_m is reduced for the same input impedance matching condition and current consumption is kept relatively low. The baseband stages also introduces flicker noise that greatly degrades the noise figure if it is not fully canceled. Additionally, all DC bias points become coupled, forcing M2 and M3 to be biased by the gates of M1N/M1P. This adds another layer of complexity in achieving the optimal $\frac{2g_{m2}}{g_{m3}}$ ratio for noise-cancellation. The noise-cancellation equations, which will be discussed in more detail later in the chapter, dictate that g_{m3} must be kept relatively low. Thus, a degree of noise-cancellation is sacrificed to reach the correct bias points. In particular, the size of M3 is increased to decrease its V_{gs} and raise the drain of M2 until it is operating in saturation. However, the V_{ds} requirement of M2 forces M3 into sub-threshold. Fortunately, the small g_{m3} in sub-threshold is used to retain noise-cancellation, though small variations in the operating point may now sacrifice more noise-cancellation.

4.3 Asymmetrical Mixer-First Architecture

The proposed asymmetrical mixer-first architecture is shown below in figures 4.3 and 4.4. The general idea integrates one N-path filter passive mixer at the input of A1 and another at the output of A2, decoupling the stages of the mutual noise-canceling LNA.

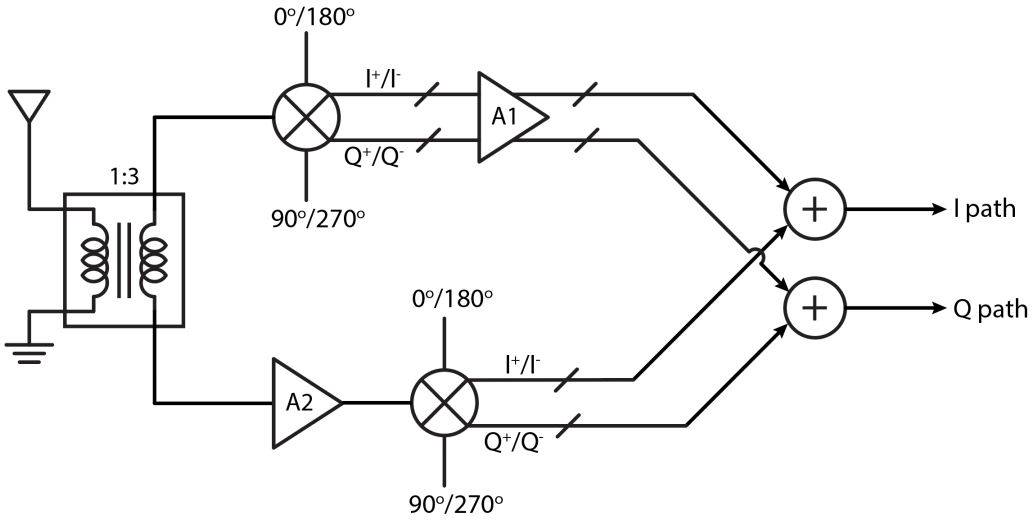


Figure 4.3: Block Diagram of the Mutual Noise-Canceling LNA with an Asymmetrical Mixer Input

A clear advantage of this architecture is the decoupling of M2 from the rest of the amplifier. This enables more flexibility in biasing and thus optimal noise-cancellation is achieved much more easily. In particular, the gate of M2 is biased at a lower voltage compared to the previous topology, decreasing the V_{ds} requirement and increasing M3's V_{gs} to prevent it from entering sub-threshold.

However, the trade-off here lies in the input matching and out-of-band filtering. Because of the asymmetrical nature, the out-of-band rejection will be dominated by the switch re-

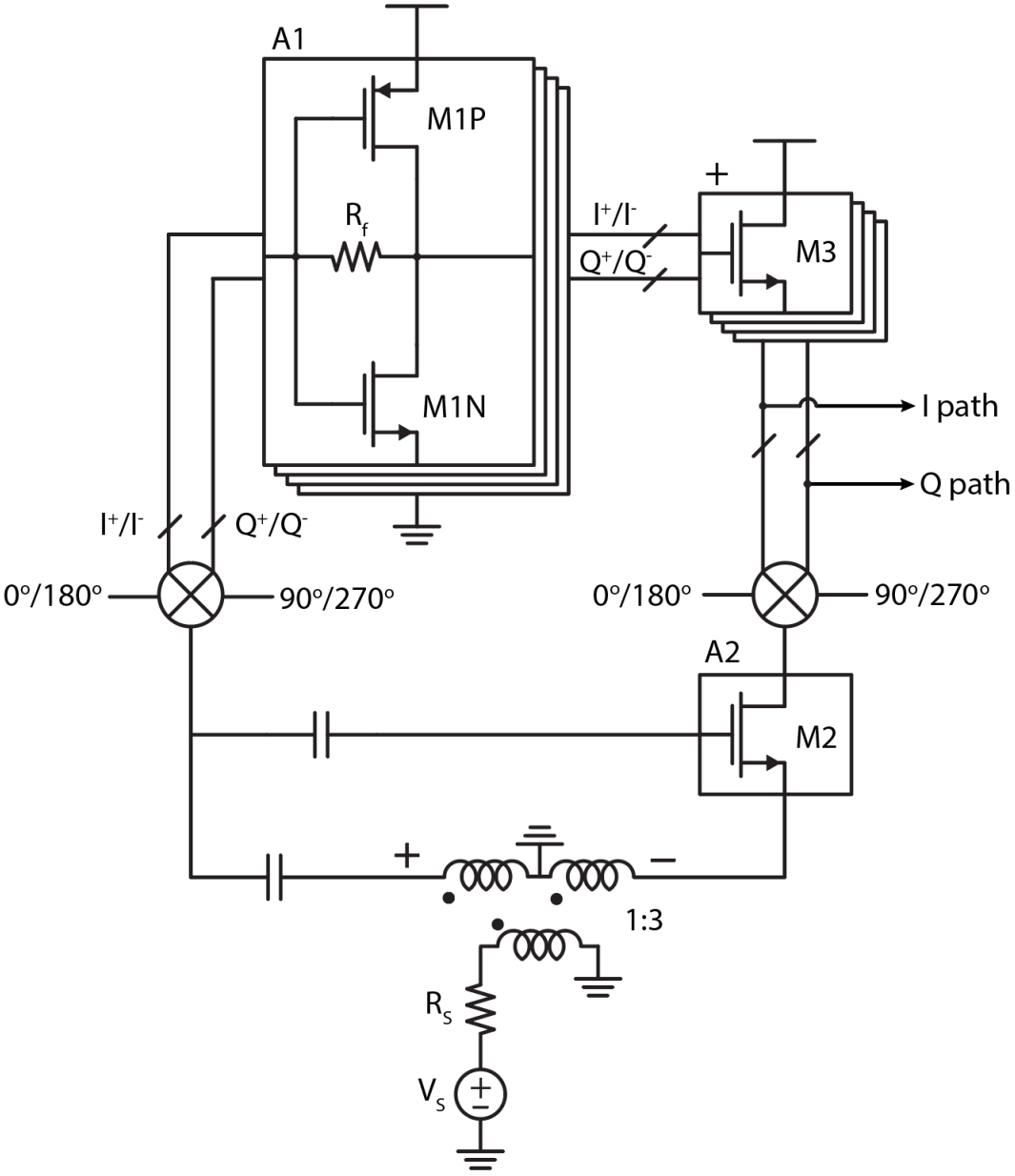


Figure 4.4: Mutual Noise-Canceling LNA with an Asymmetrical Mixer Input

sistance of the A1 path in shunt with $\frac{1}{2g_{m2}}$, which have mismatched frequency responses to maintain in-band input impedance matching. This will also sacrifice noise-cancellation of one stage over the other, as the noise of M1N/M1P and M2 undergoes asymmetrical cancellation

paths that introduce multiple frequency conversions. For instance, the noise of M2 is down-converted and canceled at baseband in both the main and auxiliary paths. However, the noise of M1N/M1P is both upconverted and downconverted on the auxiliary path through M2 before being canceled with the original baseband noise. This introduces additional losses that are compensated for by increasing the gain of M2, limiting the cancellation capabilities of both stages and sacrificing input matching.

4.4 Input Matching

This front-end is designed to achieve optimal input impedance matching at the operating frequency of 2.4 GHz. In order to increase the equivalent impedance seen by the LNA for input matching, a balun with a transform ratio of 1:3 is placed at the antenna interface. As previously discussed, this lowers the g_m requirement and current consumption of A1 and A2. The N-path filter passive mixers at the input of the LNA are driven by ideal square wave LO pulses with 25% duty cycle at 2.4 GHz. Analysis is similar to the N-path filter passive mixer input impedance matching discussed in the previous chapter. Figure 4.5 depicts the input matching network as seen from one end of the balun's secondary terminal.

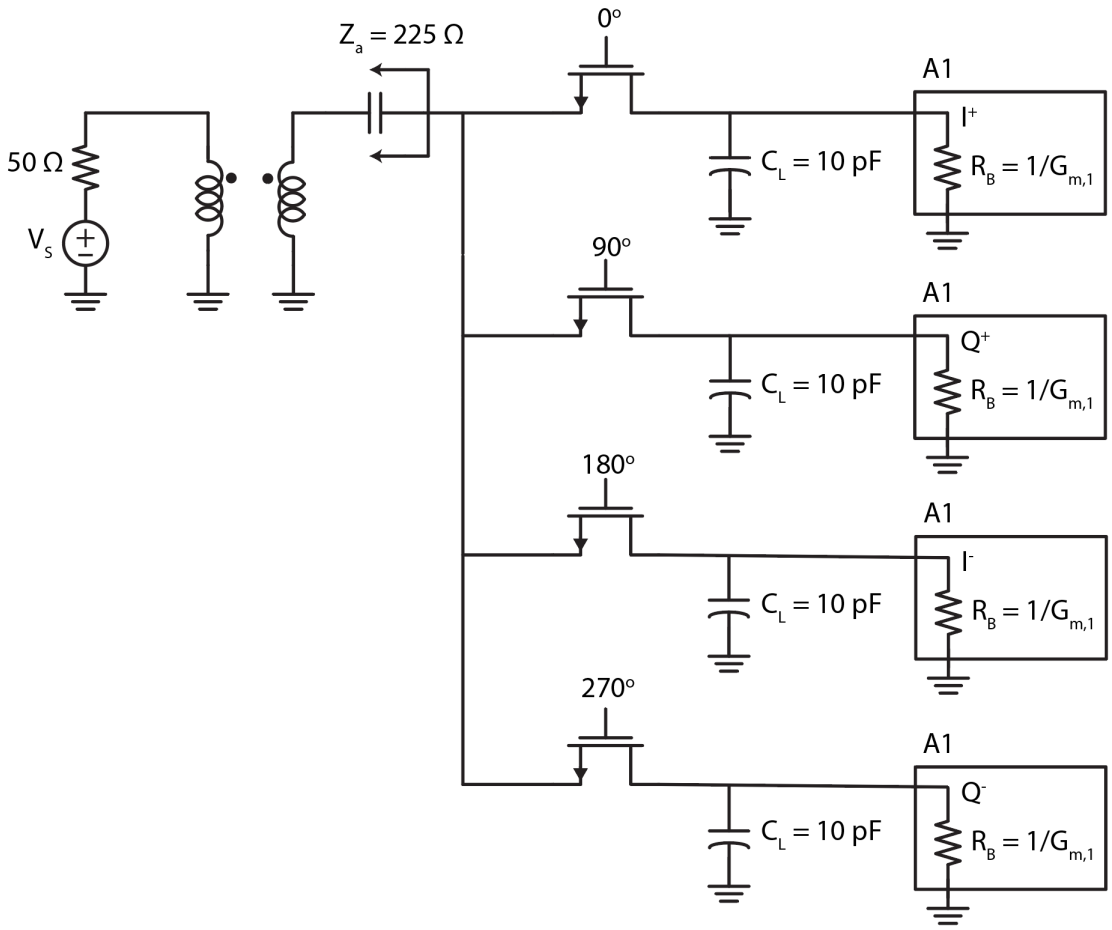


Figure 4.5: Half-Circuit (A1 Side) Input Matching Network

In this case, with a balun ratio of 1:3, $Z_A = 225\ \Omega$ becomes the target matching impedance. Though the switch resistance adds another layer to the design space, $R_{sw} = 50\ \Omega$ is chosen to provide adequate out-of-band filtering and enable low $R_B = \frac{1}{g_m}$ values for noise-cancellation and gain. To achieve adequate bandwidth and in-band roll-off, $C_L = 10$ pF is used.

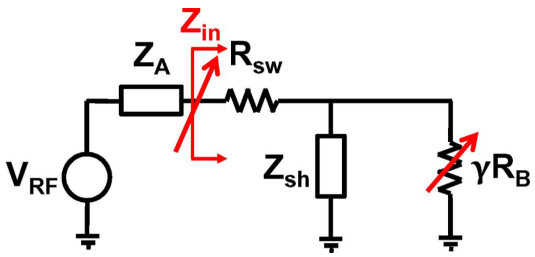


Figure 4.6: LTI Equivalent Circuit for the N-path Filter [9]

As previously discussed, the equivalent input impedance from the LTI model given in figure 4.6 is

$$Z_{in} = R_{sw} + \gamma R_B || Z_{sh} \tag{4.1}$$

where

$$\gamma = \frac{2}{\pi^2} \approx 0.203 \tag{4.2}$$

$$Z_{sh} = \frac{4\gamma}{1 - 4\gamma}(R_{sw} + Z_A) \approx 4.3(R_{sw} + Z_A) \tag{4.3}$$

Thus, the input impedance $Z_{in,1}$ of A1 is derived as follows. Let $R_B = \frac{1}{G_{m1}}$, where $G_{m1} = g_{m1,n} + g_{m1,p}$.

$$Z_{in,1} = R_{sw} + \frac{1}{\frac{1}{\gamma R_B} + \frac{1}{Z_{sh}}} \tag{4.4}$$

$$= R_{sw} + \frac{1}{\frac{G_{m1}}{\gamma} + \frac{1}{Z_{sh}}} \tag{4.5}$$

$$= R_{sw} + \frac{\gamma Z_{sh}}{G_{m1} Z_{sh} + \gamma} \tag{4.6}$$

$$= R_{sw} + \frac{Z_{sh}}{\frac{G_{m1} Z_{sh}}{\gamma} + 1} \tag{4.7}$$

With $\frac{G_{m1} Z_{sh}}{\gamma} >> 1$,

$$Z_{in,1} \approx R_{sw} + \frac{\gamma}{G_{m1}} \tag{4.8}$$

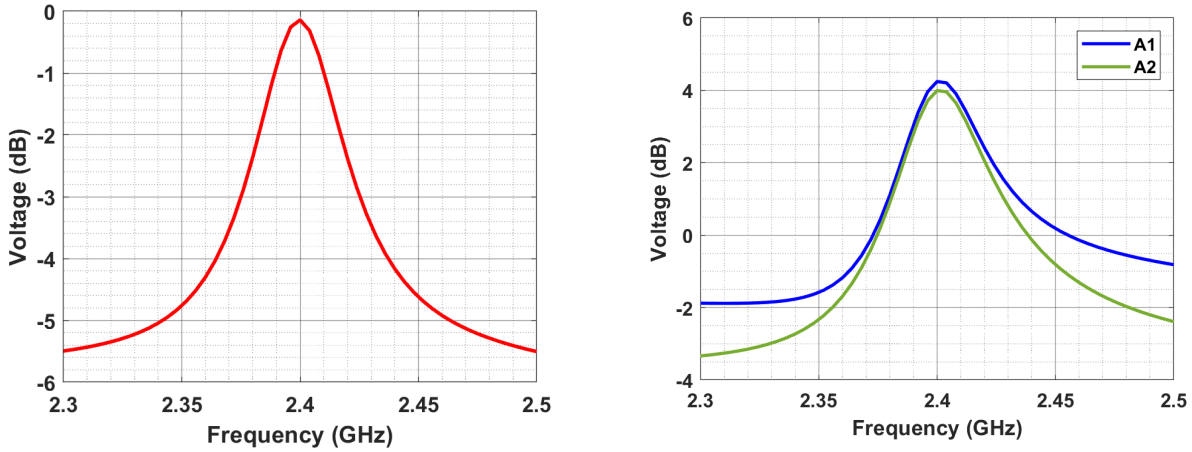
$$225 = 50 + \frac{0.203}{G_{m1}} \Rightarrow G_{m1} = 1.16mS \tag{4.9}$$

Similar analysis is done with the impedance of the A2 stage, which is given by

$$Z_{in,2} \approx R_{sw} + \frac{\gamma}{G_{m2}} \tag{4.10}$$

where $G_{m2} = 2g_{m2}$ because of the differential signal on the gate and source of M2. Note, this analysis is concurrent with the symmetrical topology. The asymmetrical topology follows the same analysis for $Z_{in,1}$, while $Z_{in,2}$ is simply $\frac{1}{G_{m2}}$.

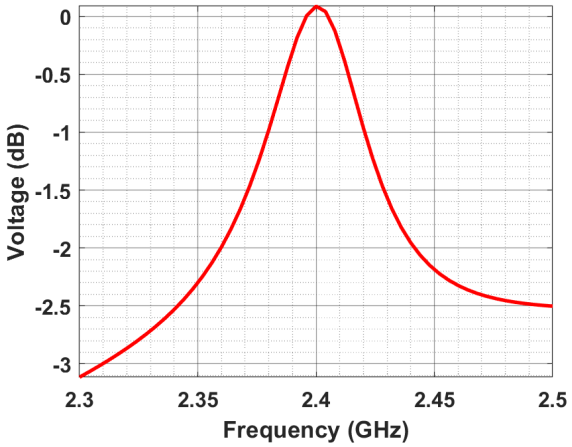
Figures 4.7 and 4.8 demonstrate the optimal matching condition for both configurations. The corresponding S_{11} graphs are also shown in figure 4.9. The voltage is plotted as a ratio of the source voltage and the balun's primary terminal voltage. Thus, 0 dB indicates an input that is matched perfectly to the 50 Ω source.



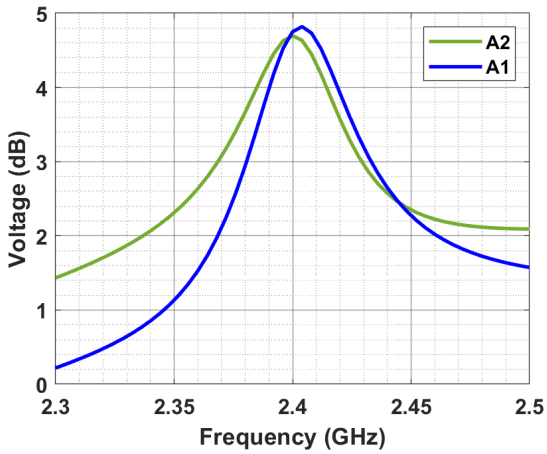
(a) Primary Terminal Voltage

(b) Secondary Terminal Voltages

Figure 4.7: Balun Terminal Voltages for the Symmetrical Architecture

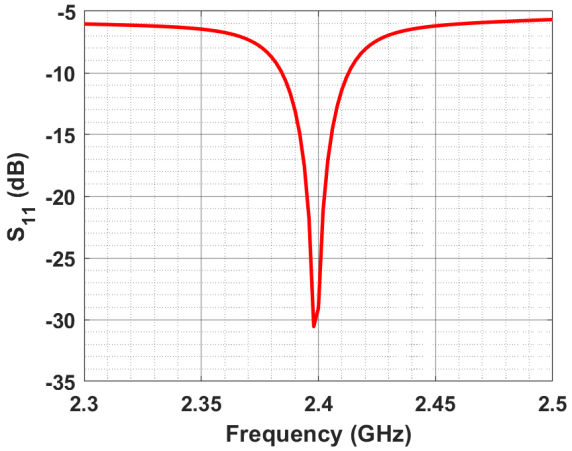


(a) Primary Terminal Voltage

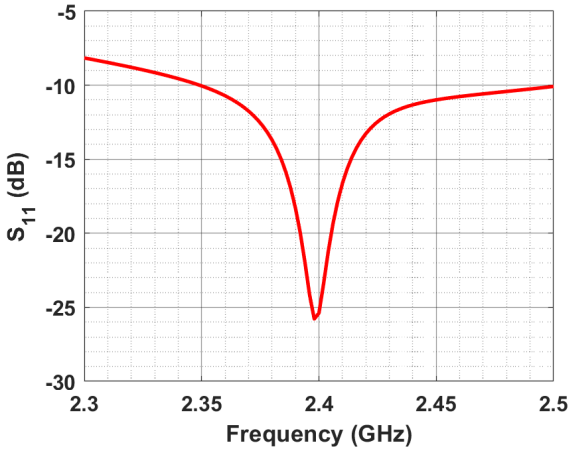


(b) Secondary Terminal Voltages

Figure 4.8: Balun Terminal Voltages for the Asymmetrical Architecture



(a) Symmetrical LNA S_{11}



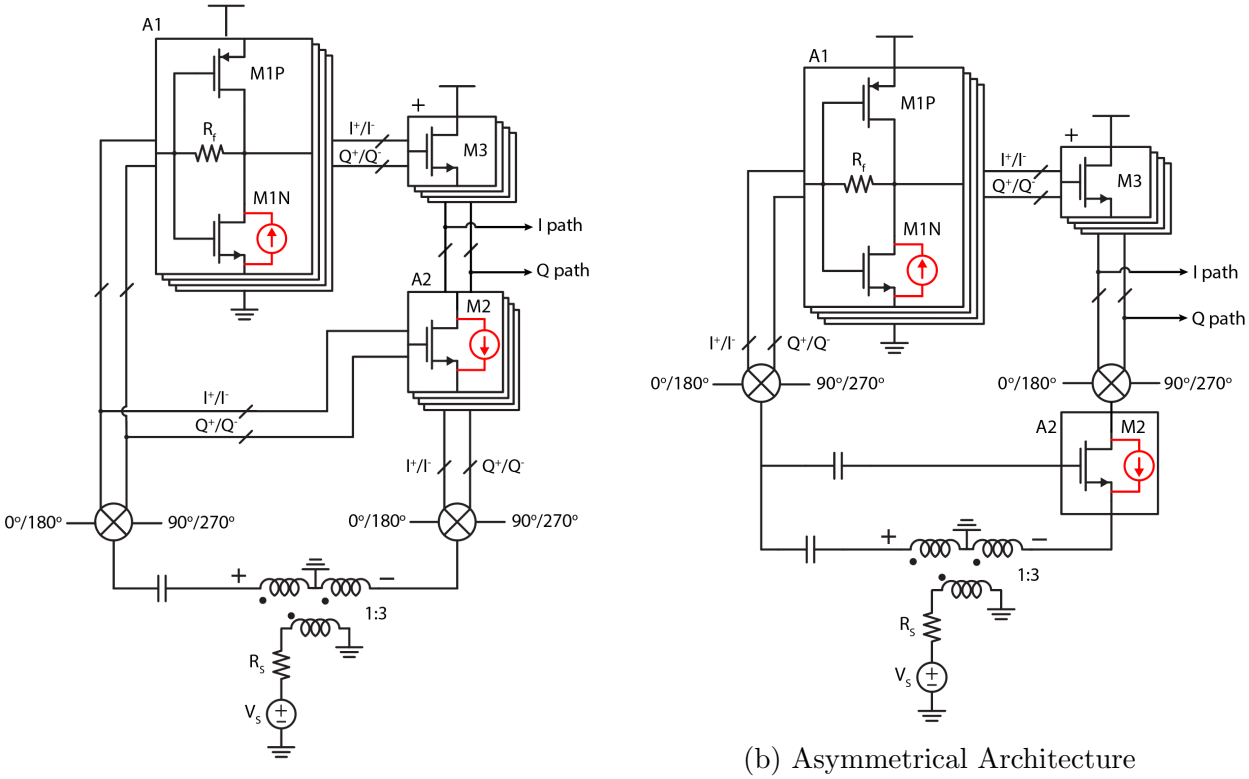
(b) Asymmetrical LNA S_{11}

Figure 4.9: S_{11} Optimized for Matching

The difference in voltage between the two stages in either architecture is caused by the differing equivalent baseband capacitance. When designing the matching network, the frequency response of the input impedance is not taken into account. For the asymmetrical

case, matching differs between the A1 and A2 stages, with the former providing more out-of-band rejection due to the mixer at its input.

4.5 Noise-Cancellation



(a) Symmetrical Architecture

(b) Asymmetrical Architecture

Figure 4.10: Noise Model in the Proposed Architectures

The noise-cancellation mechanism of M2 follows a similar manner as that of the standard mutual noise-canceling LNA. However, the frequency conversion effects must now be taken into account. In the symmetrical architecture, the noise of M2 will exhibit a frequency upconversion and downconversion in the auxiliary path before it is canceled with the main

path noise at baseband. This will introduce a G_c^2 conversion factor in the auxiliary path expression. Because typically $G_c < 1$, this loss must be compensated for by increasing the gain of the auxiliary path (A1) in order to achieve full noise-cancellation of M2. In the asymmetrical architecture, because the noise in both the main and auxiliary paths undergo downconversion, this factor simply cancels out and the equations for M2 hold from the mutual noise-canceling LNA discussed in the previous chapter.

Compared to those in [3], the equations required for noise-cancellation of M1N/M1P do not undergo significant change with the presence of the mixers. The derivations below reveal the required A_{v2} and g_{m3} for noise-cancellation of M1N/M1P. The analysis follows in similar fashion to that of the common-source noise-canceling LNA. V_Y and V_X will be used in the same manner as in the previous chapter from figure 3.3. G_c represents the conversion gain factor in either mixer and going in either direction. In practice, this is not necessarily the case, but it is assumed in this derivation for simplicity.

The required A_{v2} and g_{m3} for the symmetrical architecture are derived below.

$$\begin{aligned} V_Y &= i_n(R_f + G_c R_{s1}) \\ V_X &= i_n G_c R_{s1} \end{aligned} \tag{4.11}$$

$$V_Y = V_X A_{v2} \Rightarrow R_f + G_c R_{s1} = G_c R_{s1} A_{v2} \Rightarrow A_{v2} = 1 + \frac{1}{G_c}\frac{R_f}{R_{s1}} \tag{4.12}$$

$$\frac{2g_{m2}}{g_{m3}} = 1 + \frac{1}{G_c}\frac{R_f}{R_{s1}} \Rightarrow g_{m3} = \frac{1}{R_{s1} + \frac{R_f}{G_c}} \tag{4.13}$$

Likewise, the asymmetrical architecture requires A_{v2} and g_{m3} given below.

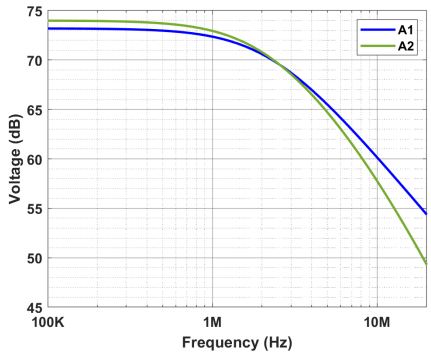
$$\begin{aligned} V_Y &= i_n(R_f + G_c R_{s1}) \\ V_X &= i_n G_c R_{s1} \end{aligned} \tag{4.14}$$

$$V_Y = V_X A_{v2} G_c \Rightarrow R_f + G_c R_{s1} = G_c R_{s1} A_{v2} G_c \Rightarrow A_{v2} = \frac{1}{G_c}\Big(1 + \frac{1}{G_c}\frac{R_f}{R_{s1}}\Big) \tag{4.15}$$

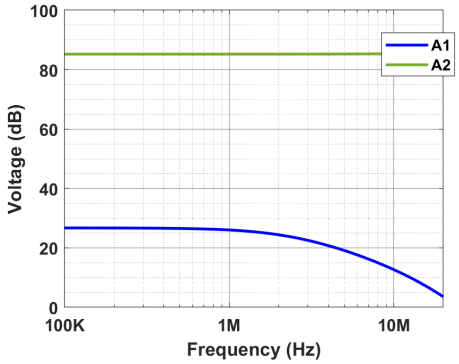
$$\frac{2g_{m2}}{g_{m3}} = \frac{1}{G_c}\Big(1 + \frac{1}{G_c}\frac{R_f}{R_{s1}}\Big) \Rightarrow g_{m3} = \frac{1}{G_c R_{s1} + R_f} \tag{4.16}$$

These equations suggest an inverse relationship between R_f and g_{m3} for noise cancellation. If R_f is chosen to reach an adequate gain value, (i.e. $R_f > R_{s1}$), then g_{m3} must be kept low to maintain full noise-cancellation of M1N/M1P. However, this comes at the cost of canceling only 50% of M2's noise following previous analysis. It is observed in simulation that with full cancellation on M1N/M1P, both architectures cancel less than 50% of the noise from M2 due to the conversion gain loss.

In order to demonstrate the noise-cancellation mechanism and design the optimal g_{m3} value, M3 is replaced with an equivalent resistor of value $\frac{1}{g_{m3}}$. With 1 A ideal current sources modeling the noise currents of M1N/M1P and M2, this substitution allows for the output voltages of A1 and A2 to be individually observed. If the voltages of these two nodes are equivalent in magnitude and out-of-phase, then the noise has undergone full cancellation. Figure 4.11 shows the output voltages of A1 and A2 with g_{m3} designed to perform full noise-cancellation of M1N/M1P, while figure 4.12 shows the same voltages for full noise-cancellation of M2. In this model, the numerical values are irrelevant.

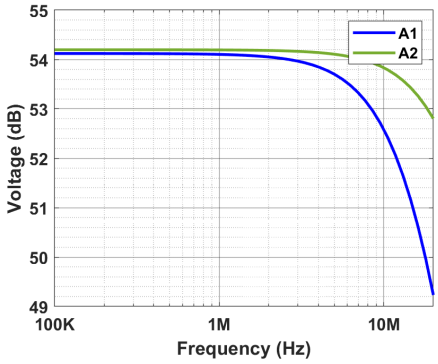


(a) Full Noise-Cancellation of M1N/M1P

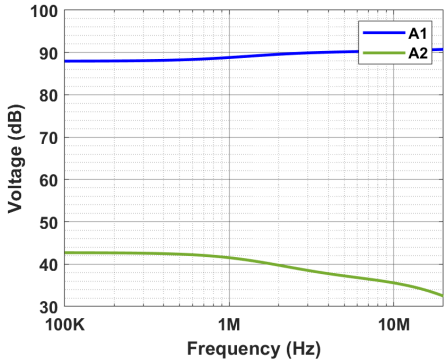


(b) Partial Noise-Cancellation of M2

Figure 4.11: Output Voltages with Full Noise-Cancellation of A1



(a) Full Noise-Cancellation of M2

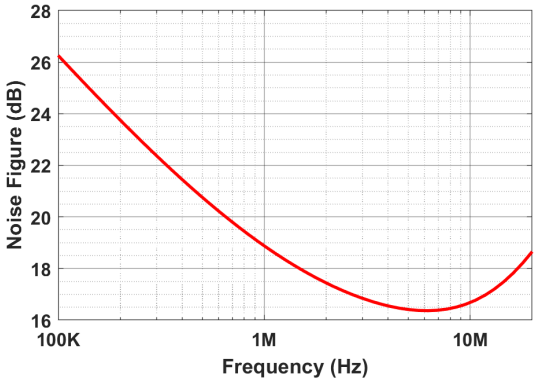


(b) Partial Noise-Cancellation of M1N/M1P

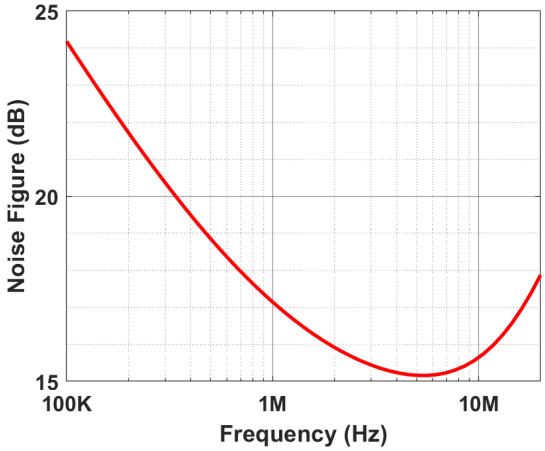
Figure 4.12: Output Voltages with Full Noise-Cancellation of A2

These results suggest a potential optimal point that performs partial noise-cancellation of both stages. Specifically, relaxing the noise-cancellation of A1 will improve that of A2. However, based on empirical results, this does not improve the overall noise figure, as the difference between the output noise voltages of the partially canceled stage is much too large. In other words, sacrificing noise-cancellation of the fully canceled path does not compensate for the noise-cancellation that is gained on the partially canceled path.

Upon further analysis and simulation, due to partial noise-cancellation and the flicker noise of M3, adequate noise figure is still unachievable with this design. The noise figure plots are shown in figure 4.13 for the symmetrical LNA under perfect matching conditions and full noise cancellation of either stage. The asymmetrical LNA results are not shown but exhibit similar noise figure values.



(a) Noise Figure with Full Noise-Cancellation of M1N/M1P



(b) Noise Figure with Full Noise-Cancellation of M2

Figure 4.13: Noise Figure of the Symmetrical Architecture with Full Noise-Cancellation

To further improve noise figure, the net gain of the LNA is increased in order to decrease the relative contribution from these extraneous noise sources. In other words, because the general noise figure equation is written as $NF = \frac{GN_s+N_a}{GN_s} = 1 + \frac{N_a}{GN_s}$, where G is the gain of the amplifier, N_s is the noise contribution from the source, and N_a is the noise added by the amplifier, increasing the gain will decrease the overall noise figure. The overall DC gain of the amplifier is given below.

$$A_v = A_{v1} + A_{v2} \tag{4.17}$$

$$A_{v1} = n(1 - G_{m1}R_f) \tag{4.18}$$

$$A_{v2} = \frac{-2ng_{m2}}{g_{m3}} \tag{4.19}$$

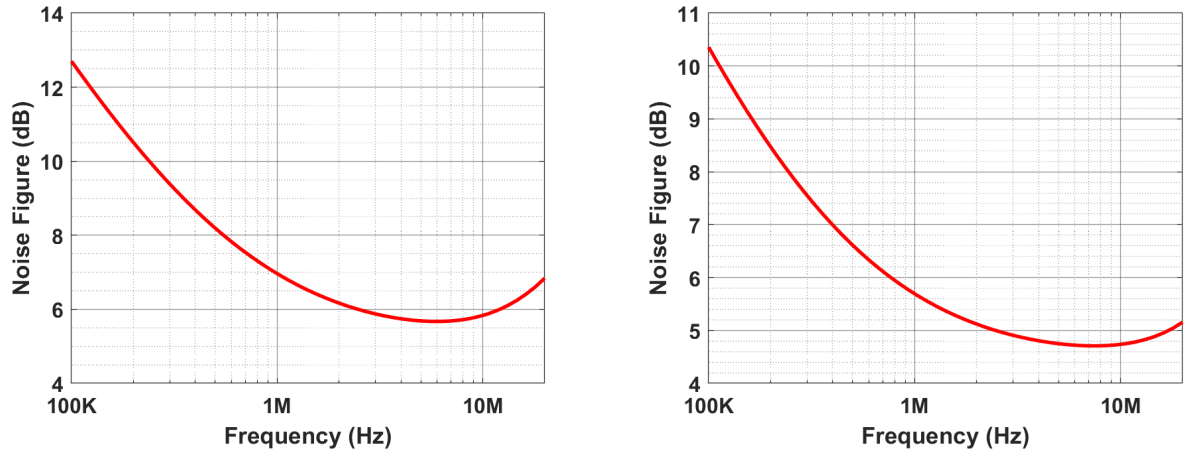
where n is the balun transform ratio. Therefore, the gain is increased through either R_f, $\frac{g_{m2}}{g_{m3}}$, or G_{m1}. Increasing R_f requires careful design in order to maintain an input impedance of $\frac{1}{G_{m1}}$ on A1. With comparable values of R_f and r_{o1}, the input impedance of A1 becomes the following

$$Z_{in,1} = \frac{R_f + r_{o1}}{1 + G_{m1}r_{o1}} \tag{4.20}$$

Thus, for $R_f >> r_{o1}$ and $G_{m1}r_{o1} >> 1$, $Z_{in,1} \approx \frac{R_f}{G_{m1}r_{o1}}$. However, this will compromise the impedance matching design methodology discussed above. Therefore, R_f must remain at a value that is considerably less than r_{o1} to preserve $Z_{in,1} = \frac{1}{G_{m1}}$. Additionally, linearity and a suitable bias condition for M2 and M3 limits the $\frac{g_{m2}}{g_{m3}}$ ratio. Because the same current flows through M2 and M3, this ratio is dependent on the $V_{d,sat}$ ratio of both transistors, which cannot be too large to preserve linearity. Additionally, as previously discussed, this variable has much more stringent limitations in the symmetrical configuration due to DC coupling. $1 + \frac{R_f}{R_{s1}}$ and $\frac{-2g_{m2}}{g_{m3}}$ must also remain equivalent for noise-cancellation. Thus, G_{m1} must be increased to increase the overall gain at the cost of current consumption and input impedance matching. However, because the N-path filter passive mixers introduce a R_{sw} series resistance in addition to a $\gamma \approx 0.203$ scaling factor on $R_B = \frac{1}{g_m}$, matching degradation is reduced for higher G_{m1} values.

The noise figure plots after increasing gain and maintaining full noise-cancellation of

M1N/M1P are shown in figure 4.14. The design for full noise-cancellation of M2 achieves similar results in both architectures. Based on the simulation noise summary, the slight increase in noise figure of the symmetrical LNA is due to the flicker noise of M2 that is present at baseband.



(a) Noise Figure of Symmetrical LNA (b) Noise Figure of Asymmetrical LNA

Figure 4.14: Noise Figure After Gain Optimization and Full Noise-Cancellation of M1N/M1P

4.6 Other Design Considerations

Linearity

The linearity of both architectures is also investigated. Ideally, nonlinearity undergoes the same cancellation mechanism as noise in the noise-canceling LNA. However, because of the large gain, the linearity is ultimately output compression limited. As a result, decreasing the gain improves the IIP3. This comes at the cost of degrading noise figure because its low

value is largely dependent on the high gain. Thus, a trade-off is made between linearity and noise figure. A final optimum point is chosen that meets both specifications in at least one architecture.

LO Generation

A particular portion of the design that cannot be ignored is the influence of the LO on the overall performance. In this case, ideal square wave pulses are used in simulation rather than a real LO source. Each pulse has a rise and fall time of 1 fs. As a result, overhead from the LO generation in terms of noise figure, power, and linearity is not taken into account. Future iterations of this work would incorporate the LO generation circuit used in [1, 2].

Future Directions

In addition to using a non-ideal LO source, specifications associated with the LO will also be analyzed in future iterations of this work, including LO feedthrough, LO self-mixing, and phase noise. Other performance metrics typical in direct-conversion receivers, such as DC offset, IQ mismatch, and even order distortion, are also future areas to investigate. Additionally, integrating the full receiver requires baseband amplifiers that will be borrowed from [1, 2]. To complete the ultra-low power Bluetooth/Wi-Fi IoT radio, this receiver will be integrated with an ultra-low power transmitter while taking into account die area and cost.

Chapter 5

Summary of Performance

5.1 Specifications

The specifications listed in 5.1 are derived from the previous ULP-BT receiver measurements [1]. As previously discussed, the primary intention of this design is to improve noise figure and minimize trade-offs with other metrics.

Parameter	ULP-BT Receiver	Mutual NC-BT Target
Gain (dB)	19	20
Noise Figure (dB)	11.56	7
In-Band IIP3 (dBm)	-6.5	-5
Out-of-Band IIP3 (dBm)	+3.3	+0
S_{11} (dB)	-10.5	-10
1-dB Compression Point (dBm)	-	-25
Power Consumption (mW)	0.58	1

Table 5.1: Table of Specifications

5.2 Measurement Description

Two different in-band IIP3 measurements are taken. The first fixes the IM3 frequency and changes the spacing between the two in-band tones (Δf) under test. The second measurement fixes the tone spacing and sweeps the frequency of the two tones, thereby changing the output IM3 frequency. In general, linearity is expected to degrade with higher Δf/IM3 frequencies corresponding to the signal transfer function.

The out-of-band IIP3 measurement is taken with two out-of-band tones spaced such that the output IM3 product falls in-band. Both architectures use a baseline IM3 product of 1 MHz. For the symmetrical architecture, f_1 = 2.4 GHz + 80 MHz and f_2 = 2.4 GHz + 159 MHz. For the asymmetrical architecture, f_1 = 2.4 GHz + 30 MHz and f_2 = 2.4 GHz + 59 MHz. These frequency values are determined based on the bandwidth of the respective amplifiers, as depicted in the gain plots.

The high noise figure in the $<$ 1 MHz region is primarily due to the flicker noise of the respective baseband stages. By increasing the bandwidth, each design is ensured to decrease the influence of the flicker noise corner frequency on the overall minimum achievable noise figure

5.3 Symmetrical Mixer-First Performance

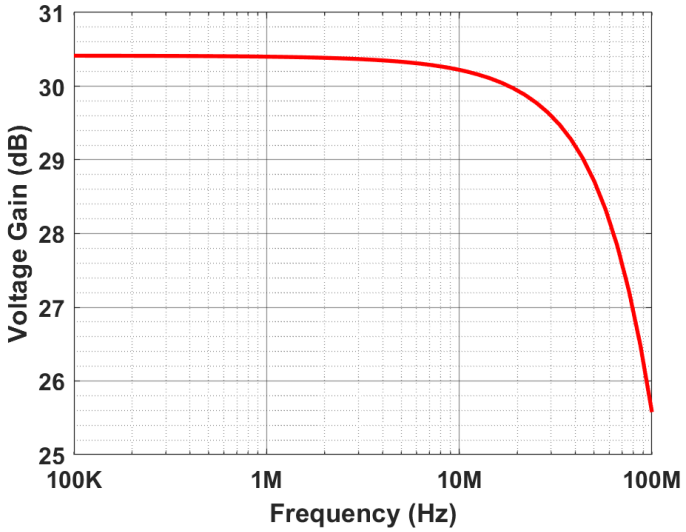


Figure 5.1: Conversion Gain of the Symmetrical Architecture
3-dB Bandwidth = 70 MHz

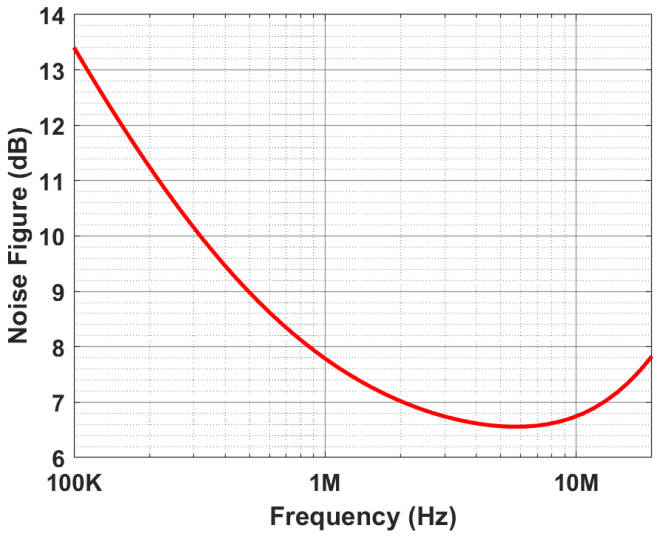


Figure 5.2: Noise Figure of the Symmetrical Architecture

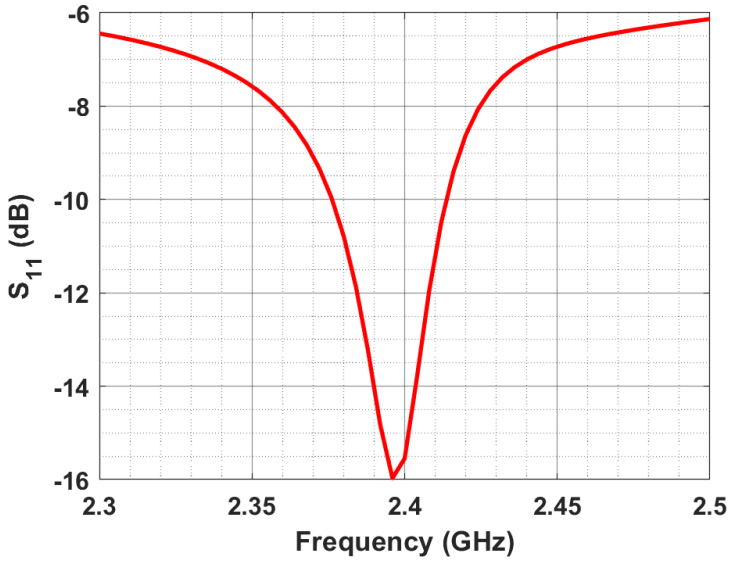


Figure 5.3: S_{11} of the Symmetrical Architecture

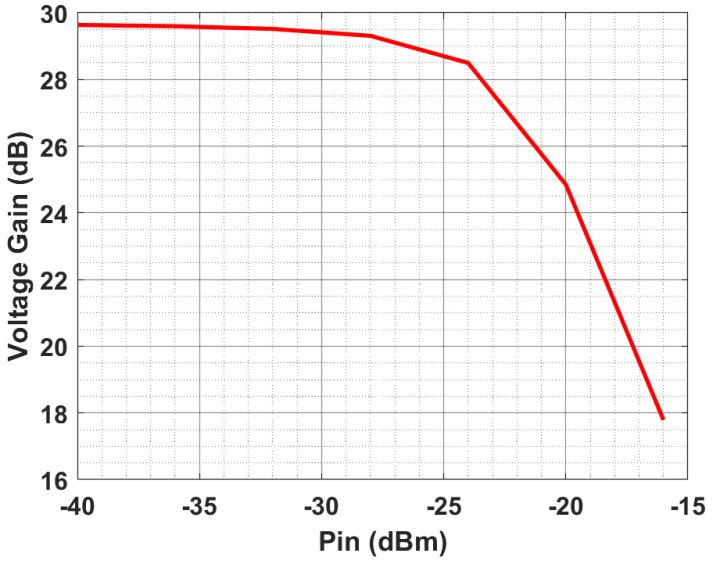


Figure 5.4: Gain Compression of the Symmetrical Architecture

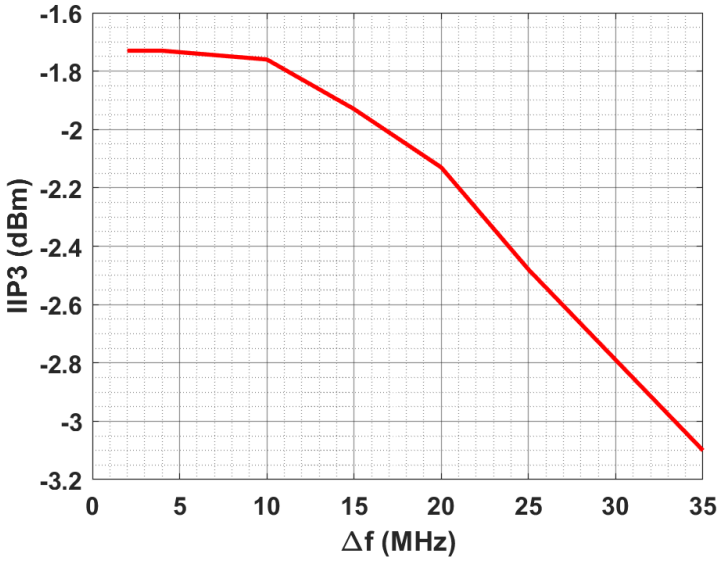


Figure 5.5: In-Band IIP3 vs. Δf with IM3 = 1 MHz of the Symmetrical Architecture

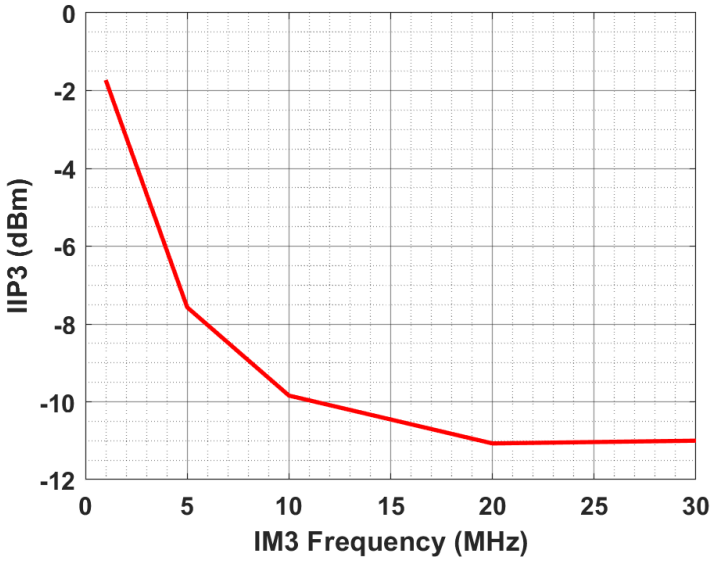


Figure 5.6: In-Band IIP3 vs. IM3 with Δf = 2 MHz of the Symmetrical Architecture

5.4 Asymmetrical Mixer-First Performance

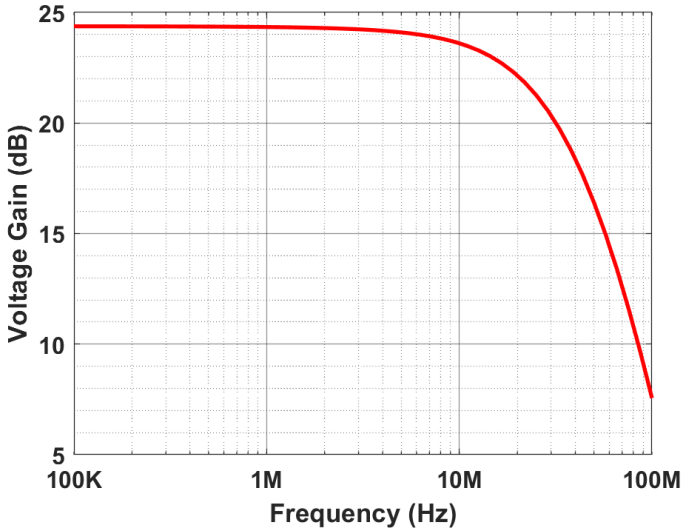


Figure 5.7: Conversion Gain of the Asymmetrical Architecture
3-dB Bandwidth = 25 MHz

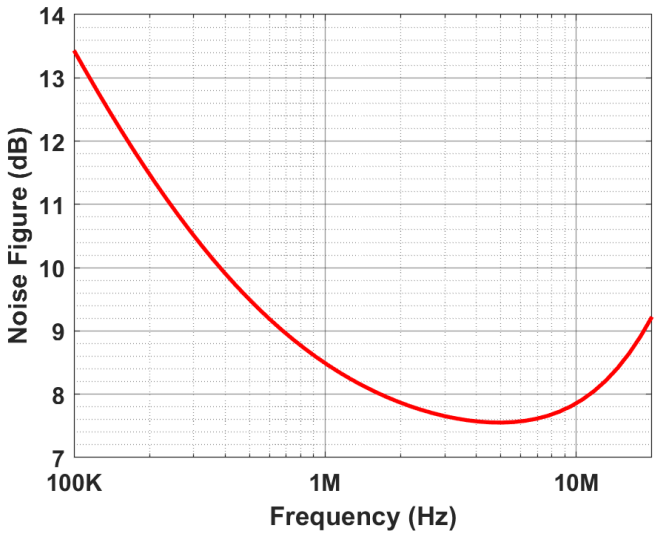


Figure 5.8: Noise Figure of the Asymmetrical Architecture

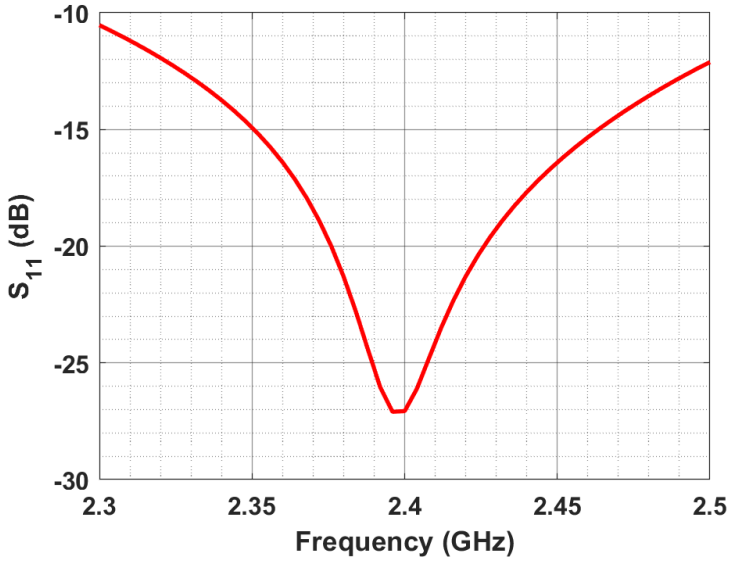


Figure 5.9: S_{11} of the Asymmetrical Architecture

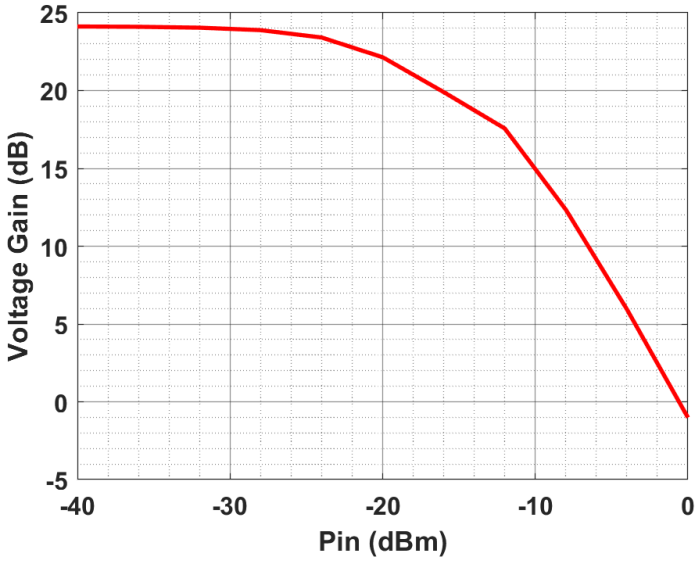


Figure 5.10: Gain Compression of the Asymmetrical Architecture

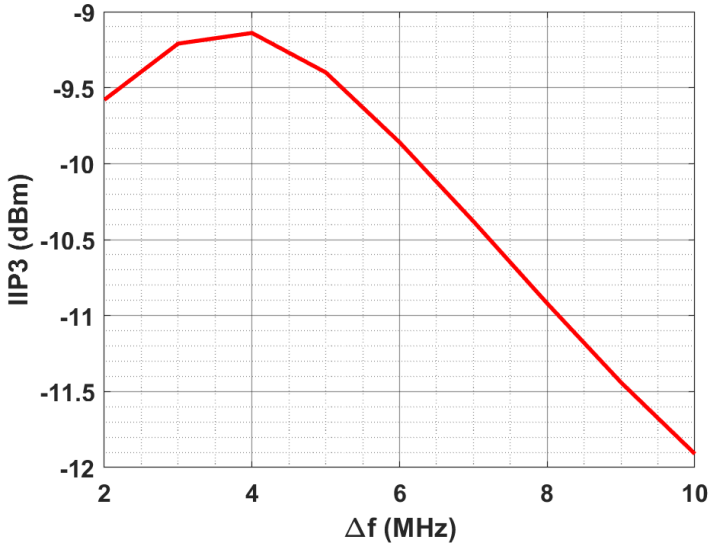


Figure 5.11: In-Band IIP3 vs. Δf with IM3 = 1 MHz of the Asymmetrical Architecture

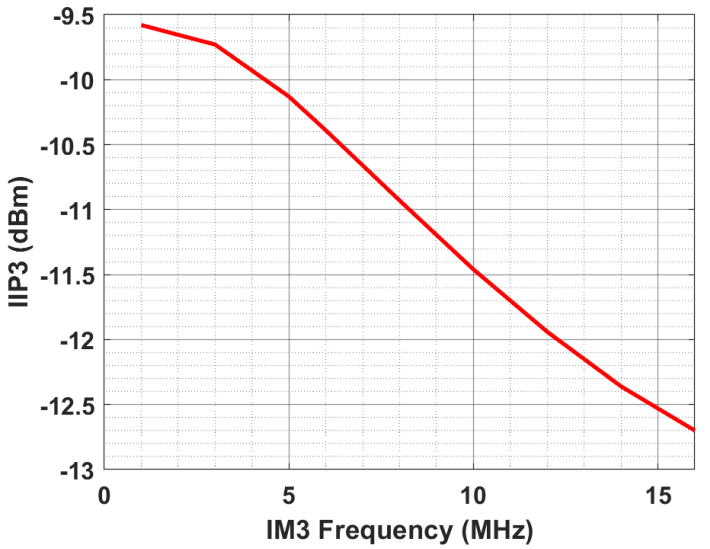


Figure 5.12: In-Band IIP3 vs. IM3 with Δf = 2 MHz of the Asymmetrical Architecture

5.5 Final Performance Metrics

Parameter	Specification	Symmetrical	Asymmetrical
Gain (dB)	20	**30.4**	24.3
Noise Figure (dB)	7	**6.5**	7.5
In-Band IIP3 (dBm)	-5	**-1.75**	-9.58
Out-of-Band IIP3 (dBm)	0	**+0.36**	-7.4
S_{11} (dB)	-10	-16	**-27**
1-dB Compression Point (dBm)	-25	**-22**	-23
Power Consumption (mW)	1	1.38	**0.83**

Table 5.2: Comparison of Both Architectures' Final Performance Metrics

5.6 Comparison with State-of-the-Art

Parameter	This Work	[1]	[3]	[4]	[5]
Gain (dB)	30.4	19	17.4	20.6	58
Noise Figure (dB)	6.5	11.9	2.8	6.55	1.9
In-Band IIP3 (dBm)	-1.75	-6.5	-10.7	-9.2	-
Out-Of-Band IIP3 (dBm)	+0.36	+3.3	-	-	+12
Power (mW)	0.83	0.58	0.475	0.194	49.4 - 99.8
Frequency (GHz)	2.4	2.4	2.4	2.4	0.3 - 2.9
CMOS Technology	28 nm	28 nm	65 nm	65 nm	40 nm

Table 5.3: Comparison with State-of-the-Art Noise-Canceling Receivers

Chapter 6

Conclusion

The growth of sub-6 GHz and IoT devices has dramatically increased the demand for ultra-low power Wi-Fi/Bluetooth radios. However, in radio receivers, power consumption comes at the cost of noise figure and linearity. This work breaks the trade-off between these metrics by presenting two innovative receiver front-end architectures. A previous ULP-BT receiver and noise-canceling LNAs are first analyzed in terms of out-of-band IIP3 and noise figure to provide insight on current state-of-the-art designs. The final architecture combines mutual noise-cancellation with N-path filtering to create two comparable receiver front-ends. A comprehensive comparison of the two indicates the overall advantage of the symmetrical mixer-first architecture. A noise figure of 6.5 dB is achieved with an out-of-band IIP3 of +0.36 dBm using only 0.83 mW of power in a 28 nm bulk CMOS technology. Future iterations of this work would incorporate a real LO generation scheme, baseband amplifiers, and integration with an ultra-low power transmitter.

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