Efficient D-Band Power Amplifier Design for Massive MIMO Systems

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Technical Report No. UCB/EECS-2020-155
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2020/EECS-2020-155.html

August 13, 2020

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by

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Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

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Abstract

There has been an uptick in interest for increasing data rate of wireless communication systems over the past decade. This is mainly driven by increasing mobile data traffic and emergence of new industrial and entertainment applications. Higher frequency operation to get more bandwidth and Multi-User MIMO (MU-MIMO) architecture to stream multiple beams to different users simultaneously have been the dominant ways to increase channel capacity. A project supported by the ComSenTer focuses on design of a large array MU-MIMO transceiver at 140GHz (D-band). Power amplifier is the most important part of the transmitter and the first half of report presents the design of a compact efficient D-band power amplifier in 28nm CMOS. The design utilizes layout optimization of active and passive devices to realize a high-gain, efficient and compact power amplifier. Packaging and integration of chip with the rest of system is of high importance in extremely high frequencies (D-band) and therefore, the second half will discuss the design of a patch antenna for a new interconnect called mm-wave contactless interconnect.

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1 Introduction

1.1 Wireless Communication

Consumer demand for wireless data capacity has been skyrocketing over the past decade. According to Ericsson mobility report [1], the mobile network data traffic grew 56 percent between first quarter of 2019 and first quarter of 2020 (Figure 1.1). With world facing a pandemic due to Coronavirus disease, WiFi and mobile data traffic has been increasing even more. The average time spent on WiFi increased by two and half hours per day while mobile broadband usage increased by one hour per day [1]. This increasing demand in data has been the motivation for evolution of wireless communication and emergence of new standards to provide higher speed and larger capacity. As a result, the data rate of cellular networks has increased from less than 1Mbps to more than 100Mbps today. Moving to higher frequency bands with more bandwidth and using more complex modulations have been the dominant ways of increasing data rate. An older standard like 802.11g operated at 2.4GHz with 20MHz bandwidth and utilized 64QAM scheme to provide a maximum theoretical rate of 54Mbps. A more recent standard like 802.11ac operates at 5GHz band with 160MHz bandwidth and 256QAM modulation scheme to reach a maximum theoretical rate of 1Gbps. Another approach to increase the data rate was the introduction of multi-user MIMO (MU-MIMO) in 802.11ac standard in which multiple streams are directed to multiple users simultaneously, increasing the overall data throughput of the entire network. All industrial standards are using available spectrum below 10GHz currently but this spectrum is limited and with growing demand for higher data rates, it is hard to meet the future need.

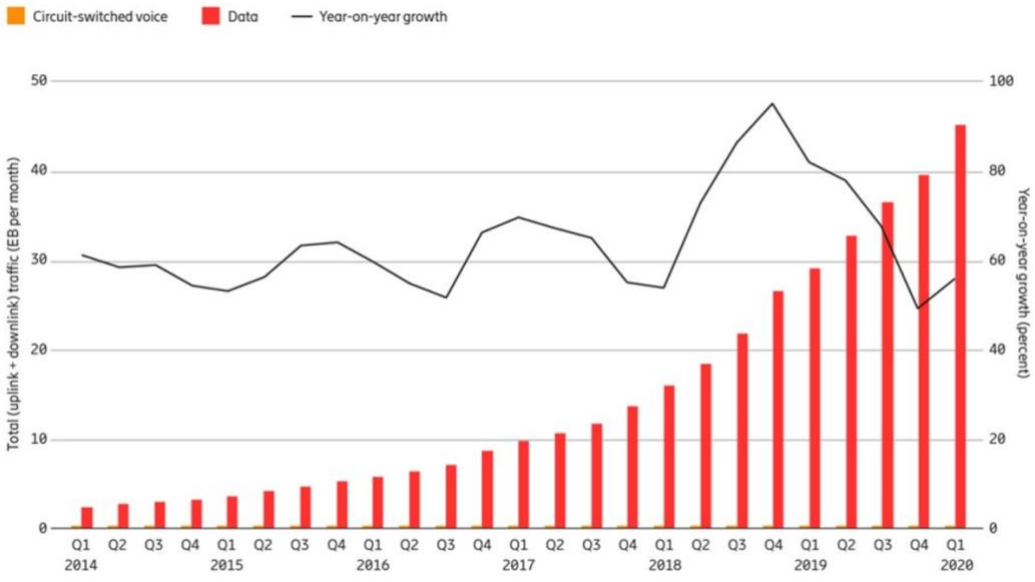


Figure 1.1. Global mobile network data traffic and year-on-year growth (EB per month).

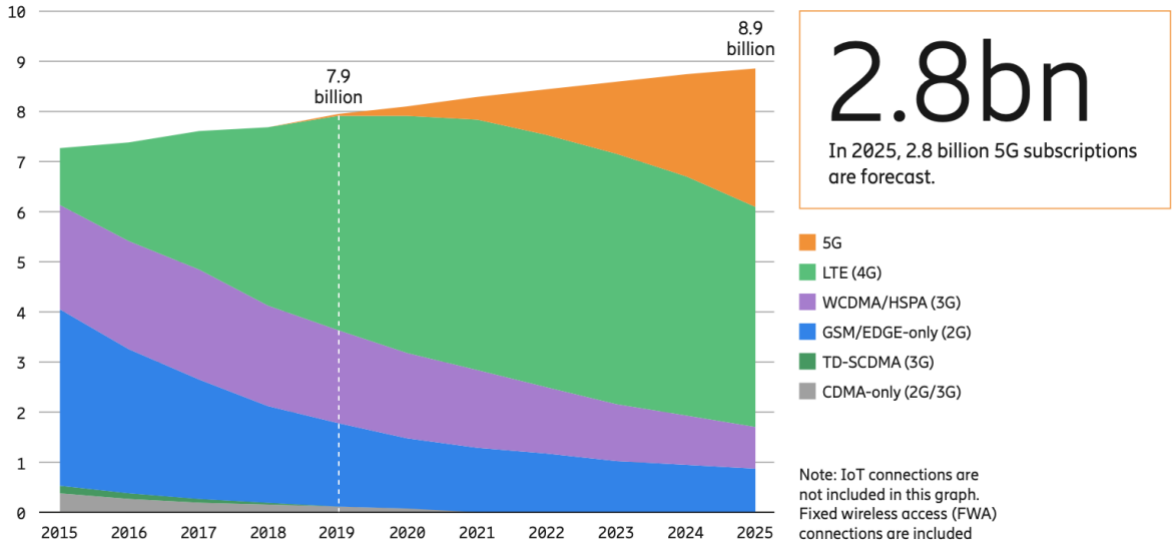


Figure 1.2. Mobile subscriptions by technology (billion).

mm-wave frequency spectrum has much larger bandwidth and very small commercial usage. 5G as the next evolution of wireless networks, is targeting to utilize low mm-wave frequency range 25-39GHz to provide practical gigabit per seconds data rate for lots of users in contained areas. It is projected that the increase in 5G subscriptions to be significantly faster than that of 4G (LTE). A total of 2.8 billion 5G subscriptions are forecast by 2025 [1] (Figure 1.2). Other examples of deployment of mm-wave band are the 60GHz Wireless Personal Area Networks (WPAN) and E-band (71-76GHz, 81-86GHz) cellular backhaul.

With 5G exploiting the lower mm-wave frequency band and more demand for higher data rates, it is expected that 6G will be using higher frequency ranges and possibly above 100GHz. Designing higher bandwidth circuits at higher frequencies is easier and extremely high bandwidth could be achieved. Therefore, a project was defined in the Communication Sensing Terahertz (ComSenTer) center to design a 140GHz transceiver which its architecture will be discussed in the next sections.

1.2 mm-Wave Wireless Transceivers

There are many mm-wave wireless transceivers presented in the literature. Focusing on CMOS ones and starting with simple on-off keying (OOK) modulation, the design of a 260GHz fully integrated CMOS transceiver exhibiting 10Gb/s wireless link is discussed in [2]. A single channel wireless link at 130GHz supporting 12.5Gb/s using also OOK modulation is presented in [3]. OOK modulation is simple to implement but the only way to increase the data rate beyond reported data rates is to move to extremely higher carrier frequencies which could be inefficient given poor performance of CMOS transistors at those frequencies. Therefore, more complex modulations should be used to increase data rate while maintaining reasonable efficiency. A 155GHz QPSK transceiver demonstrating 20Gb/s is reported in [4]. A recent work from Berkeley utilizes

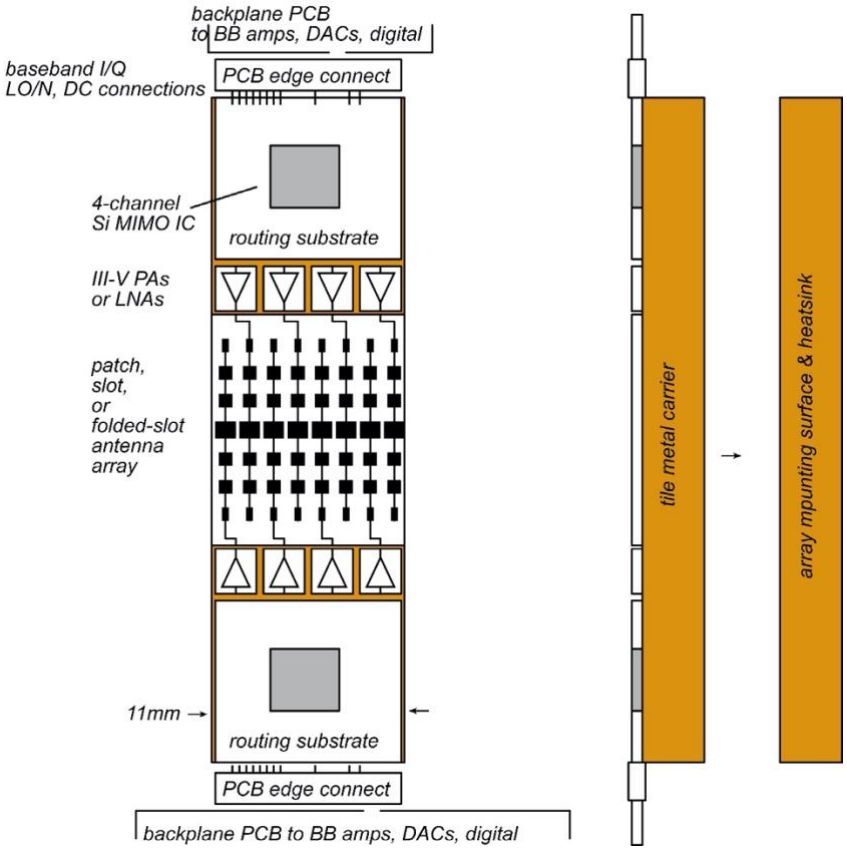


Figure 1.3. Proposed MU-MIMO 140GHz transceiver at ComSenTer (Ref: Prof. Rodwell from UCSB).

polarization diversity on top of complex modulation to demonstrate a dual- channel dual-polarized full wireless link at 113GHz supporting 80Gb/s data rate using 16QAM and QPSK modulations [5].

The architecture in ComSenTer attempts to combine the high bandwidth available at high frequencies with spatial beam streaming of MU-MIMO architecture to achieve total data rate of 1Tbps. The architecture of the proposed system is shown in Figure 1.3. Four channels are shown in the schematic but the architecture is easily scalable to much larger arrays. The very first stage of receiver (Low Noise Amplifier) and last stage of transmitter (Power Amplifier) are supposed to be designed in an III-V process due to much better RF performance and higher f_{max} of III-V device. However, III-V process is not suitable for complex baseband operation. Therefore, CMOS is considered for the design of baseband. A recent work by students in Berkeley Wireless Research Center demonstrated the design of a scalable massive MIMO uplink at E-band by implementing an effective two-stage beam-forming algorithm on distributed hardware [6]. This project aims to leverage that system and therefore, the CMOS chips in this project will be designed to perform similar processing but using a 140 GHz carrier. This report specifically will be focused on design of the CMOS power amplifier which is responsible for providing enough input power for the III-V power amplifier. A suitable packaging and chip-to-PCB transition is also desirable to be able to connect the CMOS chip to the III-V chip.

1.3 mm-Wave Power Amplifiers

Power amplifiers or transmitters can be categorized into two groups: digital and analog. In the digital architecture, the data is directly up-converted to RF frequency and power amplifier is basically an array of switches controlled by amplitude bits [7]. The phase information could be imposed on the phase of clock driving the switches or there could be I/Q power amplifier arrays with different amplitudes combining at the output and therefore reconstructing the phase of signal at the antenna port [8]. Digital PA provides better back-off efficiency compared to a linear analog PA as the power consumption is reduced when the output power level is decreased. Therefore, the overall system efficiency is better in a digital transmitter. Although, digital transmitters have been deployed mostly in RF and low frequencies, there are several examples of works reported in mm-wave frequencies [9] [10].

Digital PAs are an obvious choice for lower frequencies but we decided to proceed with an analog PA in this project due to multiple reasons: 1- The efficiency improvement margin of digital PA compared to analog PA starts to diminish as we go to higher frequencies mainly due to performance degradation of transistor as a switch. 2- This project aims to implement a large array where we have hundreds of PAs. With beamforming feature in place, each PA needs different amplitude and phase bits and therefore, there would be thousands of digital bits and design would be super complicated. 3- Due to many CMOS chips in this large array, it is important that the design is super compact and the cost of each transmitter is low. Digital PA usually takes more area compared to a compact analog PA. 4- This project aims to leverage HYDRA project E-band MIMO architecture and that system uses analog head module.

There are several examples of mm-wave linear analog power amplifiers in the literature. [11] discusses the design of a 77GHz 3-stack PMOS power amplifier which achieves 90mW output power with 24% efficiency. A two-stage 60GHz PA with a new stacked transformer (STF)-based parallel combiner exhibiting OP_{1dB} of 16.2dBm is presented in [12]. A compact D-band power amplifier with two-way power combining achieving 15dBm saturated output power and 12.8% PAE is reported in [13]. Callendar *et al* demonstrate the design of a three-stage E-band wideband power amplifier in FinFET CMOS process achieving OP1dB of 5.7dBm [14]. The PA in this work is compact and optimizes efficiency with including passive losses in the earlier stages of design.

The CMOS power amplifier in this project is supposed to drive the III-V power amplifier as a pre-amplifier. This means the CMOS PA wouldn't be the last stage of transmitter and therefore, its efficiency at peak and back-off would have small impact on the overall transmitter efficiency. Projected InP power amplifier has a simulated gain of 16dB with OP_{1dB}=19dBm. This means the CMOS PA is responsible for providing around 3dBm power at its output. A high-gain and compact power amplifier is the main target in this design.

2 D-Band Power Amplifier Design

2.1 Architecture

The power amplifier architecture is depicted in Figure 2.1 which uses a three-stage transformer coupled design to achieve high power gain at D-band frequency range. The sizing of last amplifier stage, i.e. the output stage, is decided such that the output inductor has a reasonable size (not too small) and a high-quality factor. Fortunately, this sizing meets the 3dBm required output power discussed before. For other amplifier stages, the sizing was decreased relative to output stage to decrease power consumption while providing a reasonable input capacitance for input matching purposes.

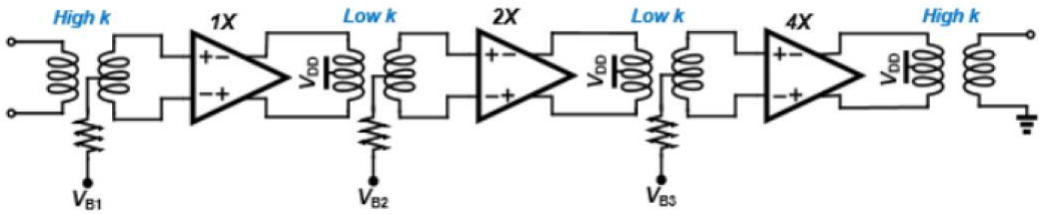


Figure 2.1. Power amplifier architecture

Loss of output matching network is very critical as it directly affects the overall efficiency and output power of amplifier. Therefore, output matching network was designed using a high-k transformer to minimize output loss. Inter-stage matching networks were designed using lower-k transformers to achieve high bandwidth while maximizing stage-to-stage signal transmission. It's important to notice there's no need to match the input and output of inter-stages to 50Ω. The input transformer was designed to match the input of the amplifier to 50Ω with relatively good S_{11} over a wide bandwidth.

2.2 Differential Common-Source Neutralized Amplifier

Achieving robust stability and high power gain becomes more difficult as we move to higher frequencies, mainly due to gate-to-drain capacitance of a transistor [15]. Neutralization techniques were introduced to overcome this issue and make the transistor unilateral. With neutralization, i.e. making the effective y_{12} of circuit equal to zero, stability is ensured. There are two dominant types of neutralization in literature: 1- transformer-based method which relies on ratio of inductor to capacitor and could be challenging given the fact that passive devices must be accurately modeled and inductors introduce significant loss [16]. 2- Capacitor neutralization with cross-coupling which is more suitable for high-frequencies as capacitors are relatively high Q at high frequencies and easier to model. One downside of this method is doubling the input and output capacitor of the circuit [17].

Capacitor neutralization is adopted in this design. Conventionally, a MOM cap using top-level metals is used to cancel the gate-to-drain capacitor of transistor. The value and quality factor of

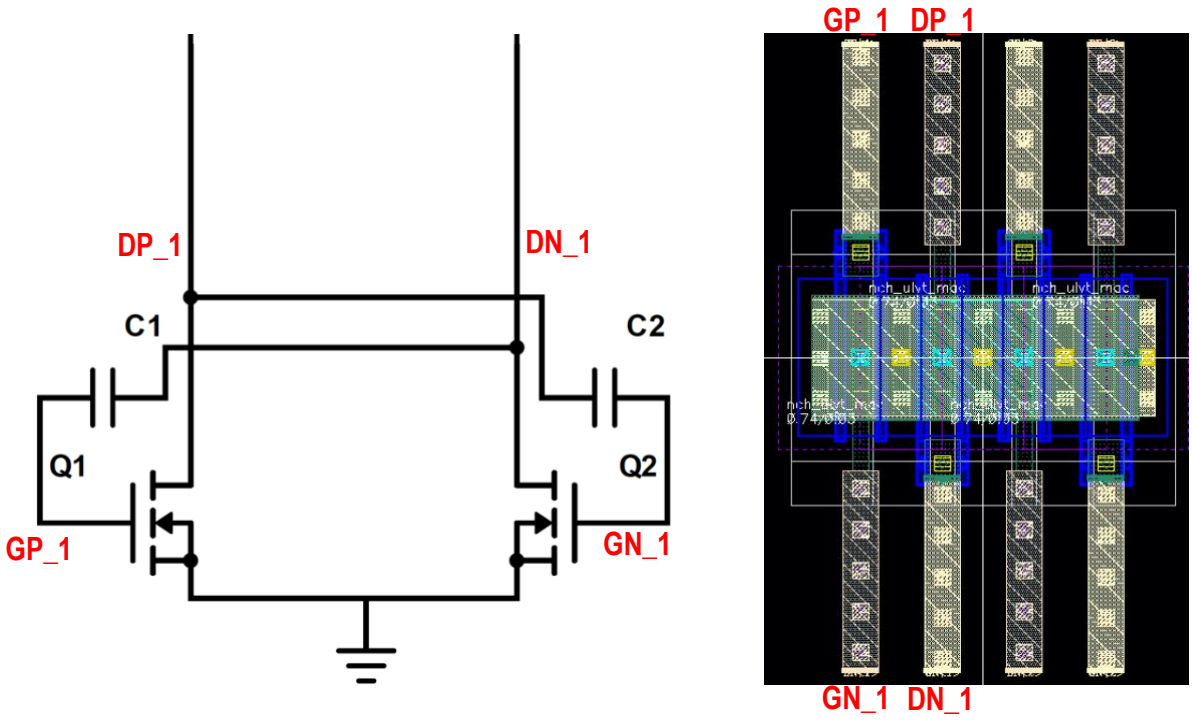


Figure 2.2. Schematic and 2D view of neutralized unit cell

this MOM capacitors depends on the size of transistor. In power amplifier design, the size of output amplifier transistor is large and it is challenging to realize a large neutralization MOM capacitor with extremely high-Q at D-band frequency range. A distributed capacitor approach is utilized to mitigate this effect.

To understand the proposed approach, it is worth mentioning that a modular layout approach is used to build amplifiers of different stages in power amplifier, meaning that amplifiers are built out of a number of unit cells connected in parallel. In other words, each amplifier is implemented in layout as a linear array of these unit cells. Each unit cells consists of a unit (1 finger) differential common-source amplifier with width of transistor being set to achieve the maximum stable gain. Simulations shows a width of 370nm is optimum in terms of having space for enough opening contacts (3 vias in this case as you can see in Figure 2.2) and achieving maximum gain. Therefore, each unit cell is a differential pair with 370nm/30nm size.

In order to mitigate gate-to-drain capacitance of transistors, a specific layout approach is used as depicted in Figure 2.2. As you can see, positive/negative gate and drain connections are routed next to each other to obtain a negative cap and compensate the gate-drain capacitance of the transistors. This method results in a stable unit cell that could be used to build a stable amplifier of desired size.

2.3 Output Stage Design

2.3.1 Amplifier Layout

In order to meet power requirement of the power amplifier and have enough margin for output matching and pad loss, the output stage was designed to have 29.6um/30nm size which is

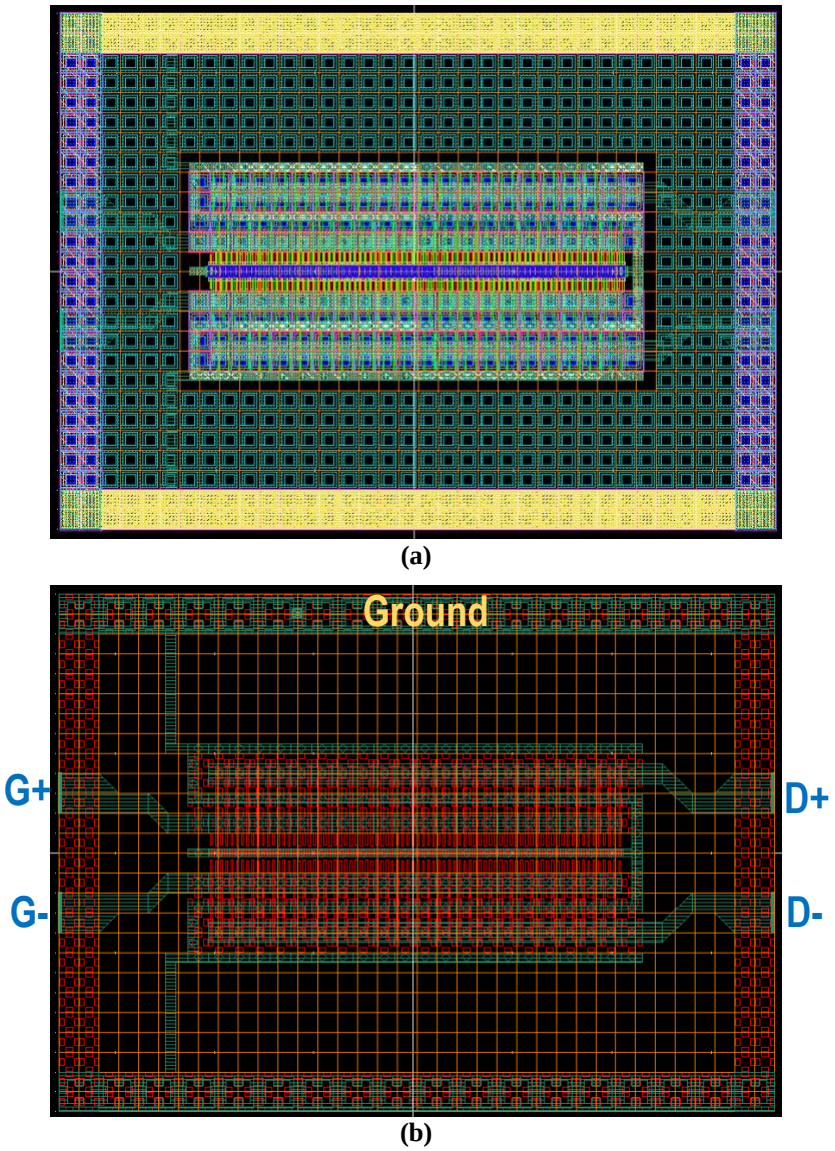


Figure 2.3. (a) Amplifier layout (b) Amplifier layout view in M10

constructed out of 80 unit cells (370nm/30nm) discussed in previous section. The full layout of output amplifier is shown in Figure 2.3. Input/output taper transitions are designed and optimized to connect the gate and drain of amplifier to 100Ω differential input/output transmission lines without introducing much parasitics. A ground layer has been used to isolate the gate and drain lines to prevent more capacitance between gate-drain. The amplifier is surrounded by a ground ring at M6. The source of amplifier is connected to this ring and outside ground planes through M4-M10 with appropriate width to carry the ground current and meet the electro-migration rules.

2.3.2 Amplifier Simulation

Transistors are extracted using local RC parasitic extractions while all the metal interconnections, both inside unit cells and the ones that connect unit cells, are extracted using an electromagnetic field solver which in this case is Integrated EMX. The amplifier is biased at

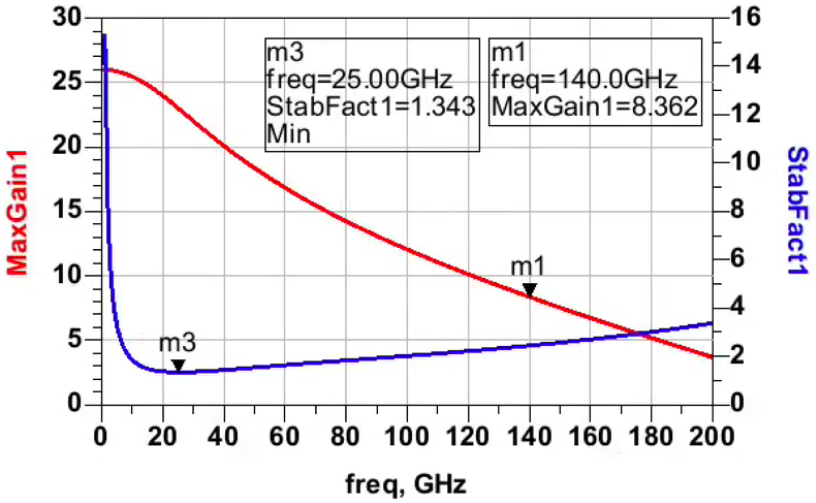


Figure 2.4. Gain and stability simulation of output stage amplifier

420uA/um to achieve maximum gain at 140GHz. The gain/stability simulation results in typical-typical (TT) corner are illustrated in Figure 2.4. The amplifier is unconditionally stable at all frequencies and has a maximum gain of 8.3dB at 140GHz. It is noteworthy to mention that the gain for smaller size amplifiers built out of same unit cells is larger than 10dB and it drops as the amplifier gets bigger because the gate/drain routings become longer and show more loss.

The load pull simulation result of output stage amplifier in TT corner is shown in Figure 2.5. As you can see, the optimum load to achieve maximum output power is slightly different from the one for achieving maximum PAE. To obtain efficiency and gain compression curves of Figure 2.5(b), the load was set to optimum load for achieving maximum power and input power was swept. Saturated output power is around 10dBm while the output power at 1dB compression point is around 7.4dBm. The amplifier has a peak PAE of 21.9% while exhibiting 18.7% PAE at 1dB compression point.

2.3.3 Amplifier with Output Matching Network

The output matching network was designed using a 1-1 high-k transformer to minimize the loss. A view of output matching network in HFSS is depicted in Figure 2.6. M9 and M10 metal layers are used for the transformer. A parallel capacitor at the output port of transformer was necessary to realize the optimum load needed for amplifier. This capacitor, as you can see in Figure 2.6, is built using distributed interwinding metal fingers on the secondary port of the transformer. M9 and M10 were used to realize this capacitor due to their small loss compared to lower metal layers. Center taps of both primary and secondary of transformer is symmetrically routed to both sides and wave ports are used to excite them for more accurate simulation purposes, especially for checking common mode oscillation as will be discussed later in this chapter. Finally, a transition from 100Ω differential transmission line was designed to connect the output of the amplifier to single ended output pad for measurement purposes.

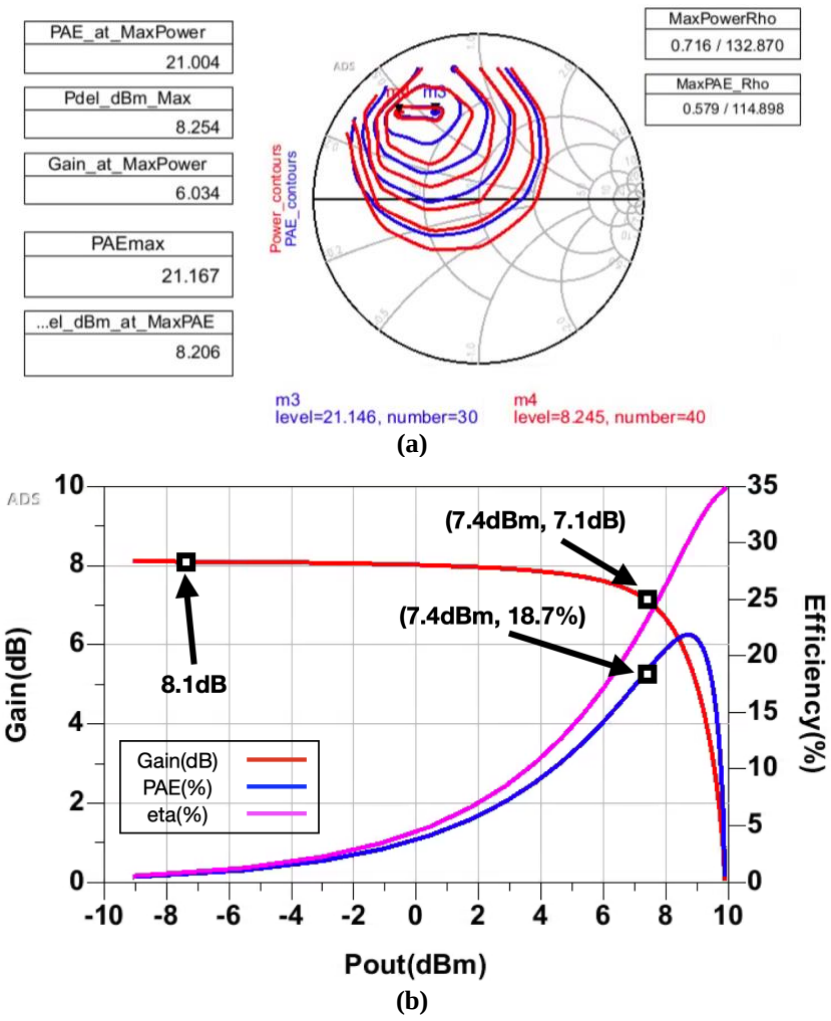


Figure 2.5. (a) Load-pull simulation of the amplifier (b) Efficiency and gain compression curves (in TT corner).

The next step in the design is to simulate the output amplifier with output matching. The output stage is driven using a variable power source at 140GHz and the simulation results are shown in Figure 2.7. The output stage exhibits an output power of 4.4dBm with 7.7% PAE at 1dB compression point. Saturated output power is around 7.4dBm but only could be achieved at high gain compression region. The output matching network has around 2.8dB insertion loss.

2.4 Driver Stage Design

In order to achieve a reasonable gain (~10dB) for the entire power amplifier, the driver uses a two-stage transformer-coupled amplifier. As you can see in Figure 2.1, the first stage has 1/4 and second stage has 1/2 size of the output stage amplifier to achieve minimum power consumption while providing enough input power for the output stage. The amplifiers are constructed out of common-source neutralized unit cells discussed before. Inter-stage transformers have low-k to achieve wideband operation and were designed to maximize the stage-to-stage signal transmission. A HFSS view of these transformers are shown in Figure 2.8 . Simulations show that the two-stage

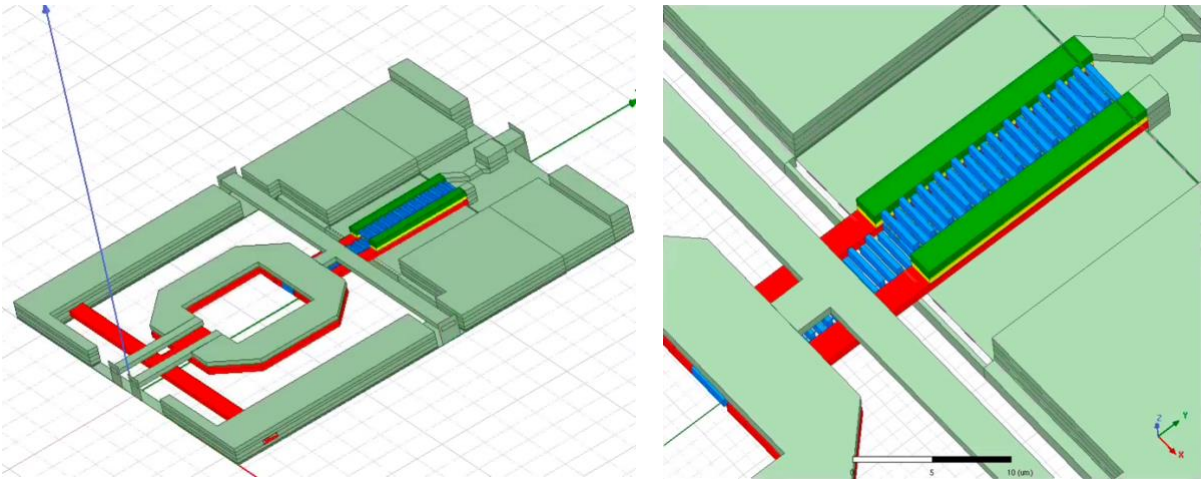
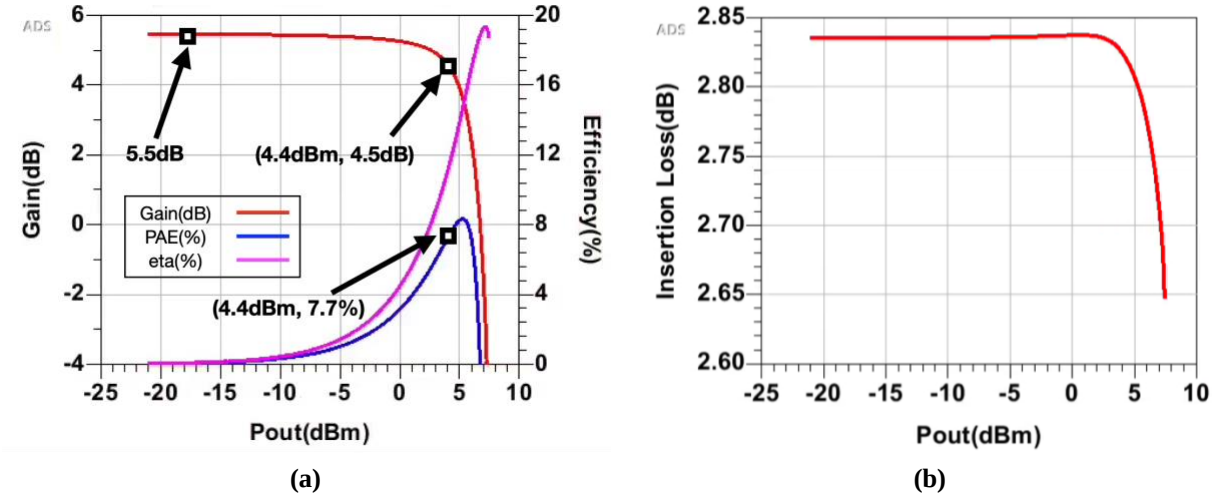


Figure 2.6. Differential to single-ended output matching network including 1-1 transformer and distributed cap

driver provides around 11dB power gain when terminated to a load impedance equal to the input impedance of the output stage with each stage contributing fairly equal to this total gain.



(a) **(b)**

Figure 2.7. (a) Output stage efficiency and gain compression curves (b) Loss of output matching network

The driver stage also utilizes an input matching network using a transformer to provide good S_{11} and the ability for the power amplifier to be driven using an external 50Ω RF source. The first stage of the driver is a common-source neutralized amplifier and as expected, exhibits a high quality factor capacitive input impedance. Therefore, the input matching would inevitably have high insertion loss which is 6dB in this case. It is worthy to mention that in integrated transmitter design, it is absolutely unnecessary to provide 50Ω input impedance for the power amplifier. The integrated design simply matches the input impedance of driver stage to the output impedance of the upconverter with much lower insertion loss. A view of single-ended to differential input matching network is shown in Figure 2.8.

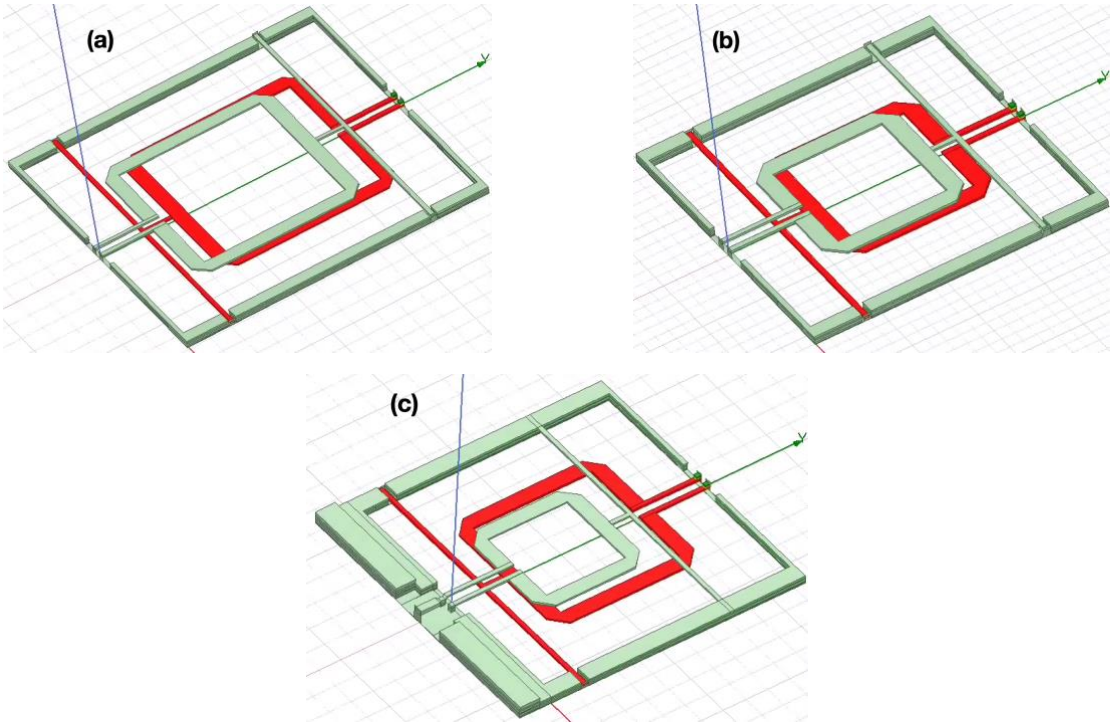


Figure 2.8. (a) First inter-stage transformer (b) second inter-stage transformer (c) input matching network

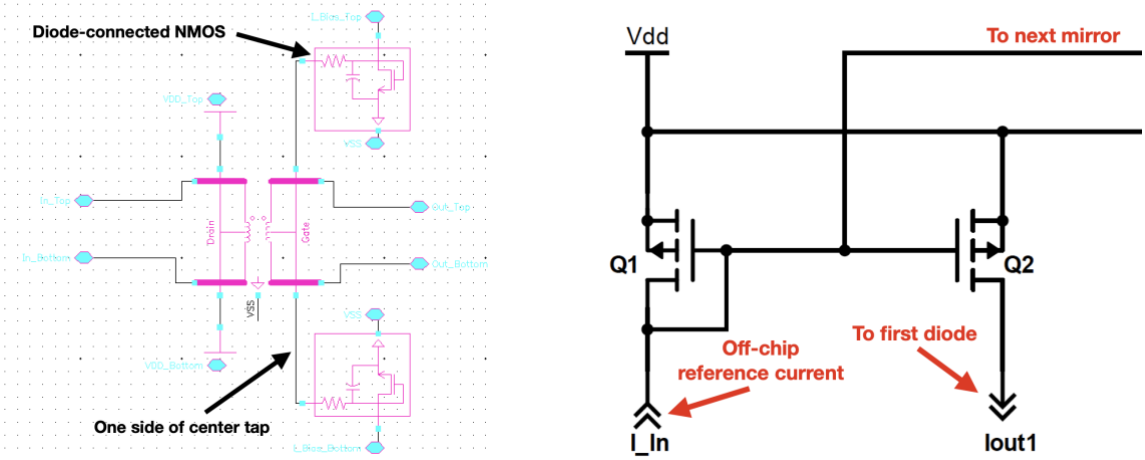


Figure 2.9. Bias network

2.5 Bias Network

A current mirror approach is utilized to bias the amplifiers. A diode-connected NMOS transistor is connected to each side of the center tap of transformers as depicted in Figure 2.9. A shunt capacitor along with a series resistance in the drain of diode connected NMOS ensures common-mode stability. Simulations show that a 230fF capacitor and 400Ω resistor results in unconditional stability at all frequencies. PMOS mirrors are used to mirror the off-chip reference current to these diode-connected NMOS transistors as depicted in Figure 2.9. The value of off chip reference current is 290uA.

2.6 Full Power Amplifier Circuit

2.6.1 Layout

The full layout of power amplifier including input and output pads as well as V_{DD} and input bias pad is shown in Figure 2.10. The center to center distance between input and output pads is 1.5mm and was fixed. The PA has a dimension of 680um X 176um. A 430um transmission line (TL) is used between the input pad and input transformer to fit the PA into the space between input/output pads. This long TL introduces 1dB insertion loss. Reference current is hooked up to the chip using a general-purpose pad and then is connected through a long wire on M6 to the PMOS current mirror network placed next to one of transformers.

The input/output pads were designed by Nima Baniasadi (PhD student at BWRC) to have an optimum transition to PCB. 3D Electromagnetic simulation results of the pad including chip-to-PCB transition is depicted in Figure 2.11. As you can see, input and output are matched in 120GHz-160GHz frequency range with 140GHz center frequency.

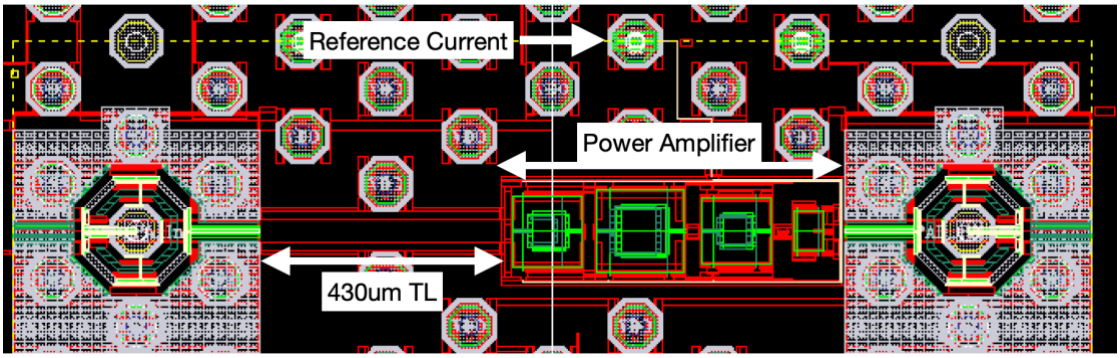


Figure 2.10. Power amplifier layout

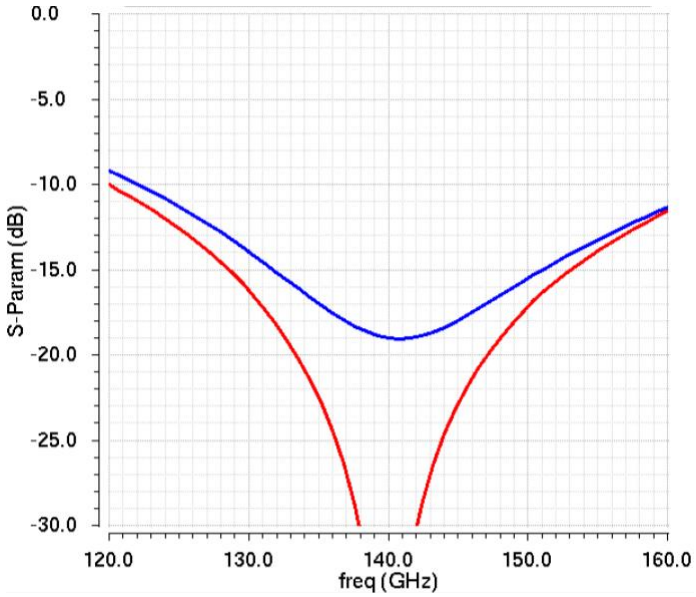


Figure 2.11. Input and output return loss of chip to PCB transition.

2.6.2 Simulation Results of Standalone PA

Before diving into simulation of the whole PA circuit including input/output pads, it is good to first simulate the behavior of standalone PA. The small signal simulation results are plotted in Figure 2.1. The PA has a peak gain of 10.5dB at 137GHz with a 3dB bandwidth of 20GHz, from 126.6GHz to 146.6GHz. The input and output return loss are below -10dB over 133GHz-150GHz and 120GHz-150GHz, respectively.

The large signal performance of the PA at 140GHz is illustrated in Figure 2.13(a). The PA exhibits 2.3dBm output power at 1dB compression point with a PAE of 3.8%. Comparing this to the large signal result of only output stage (OP_{1dB}=4.4dBm) in Figure 2.7, the OP_{1dB} has decreased by 2dB. This is because of non-linearity of the driver stage which makes the $P_{in,1dB}$ smaller than it would have been otherwise if the driver stage was sufficiently linear. Figure 2.13(b) plots the frequency response of output power and PAE at 1dB compression point, demonstrating a peak output power of 2.6dBm and PAE of 4% at 137GHz. The PA was then driven using corresponding $P_{in,1dB}$ obtained from Figure 2.13(a) to obtain these results.

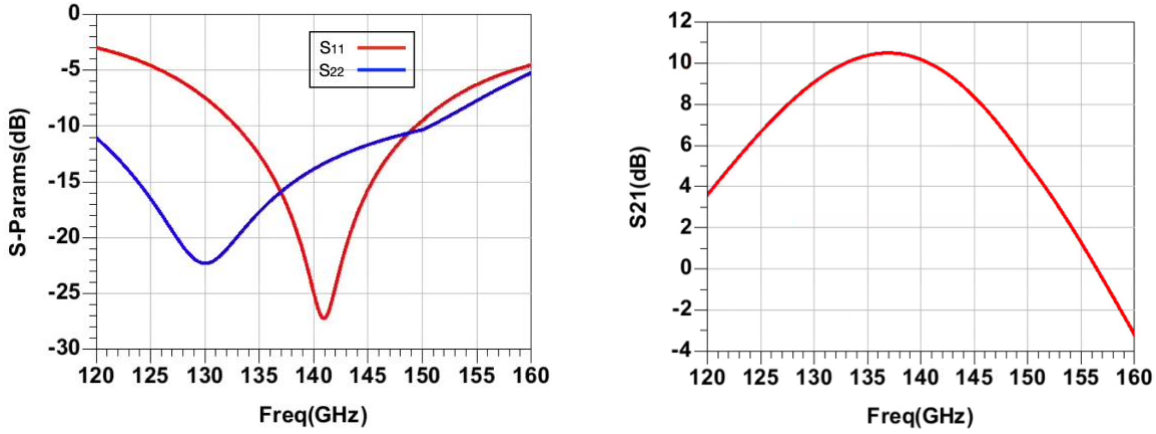


Figure 2.12. Simulated S-parameters of standalone PA

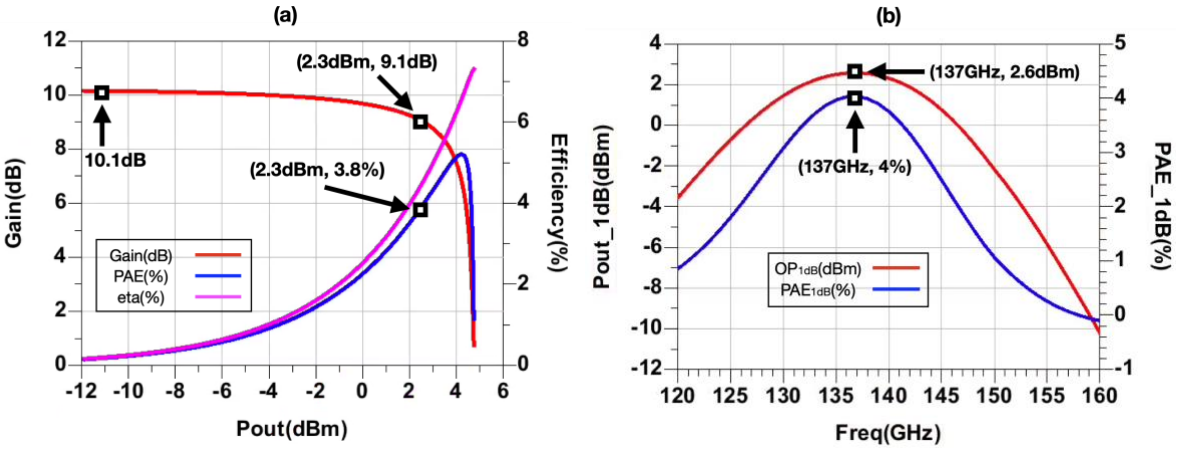


Figure 2.13. (a) PA gain compression and efficiency curves at 140GHz. (b) Frequency response of PAE_{1dB} and OP_{1dB}

2.6.3 Simulation Results of PA with Input/Output Pads

The simulated S-parameters of the power amplifier including input/output pads and chip-to-PCB transition as well as 430um long input TL is shown in Figure 2.14 . The power amplifier has a peak gain of 7.7dB at 137GHz with 3dB bandwidth of 19GHz (128GHz-147GHz). 3dB loss in gain due to pads and input TL is clear from this result. The input and output return loss are below -10dB in 130GHz-160GHz frequency band. The large signal performance of PA at 140GHz is depicted in Figure 2.15(a). The PA shows 1.4dBm output power at 1dB compression point with a PAE of 2.7%. Figure 2.15(b) demonstrates the frequency response of output power and PAE at 1dB compression point, demonstrating a peak output power of 2.6dBm and PAE of 4% at 137GHz.

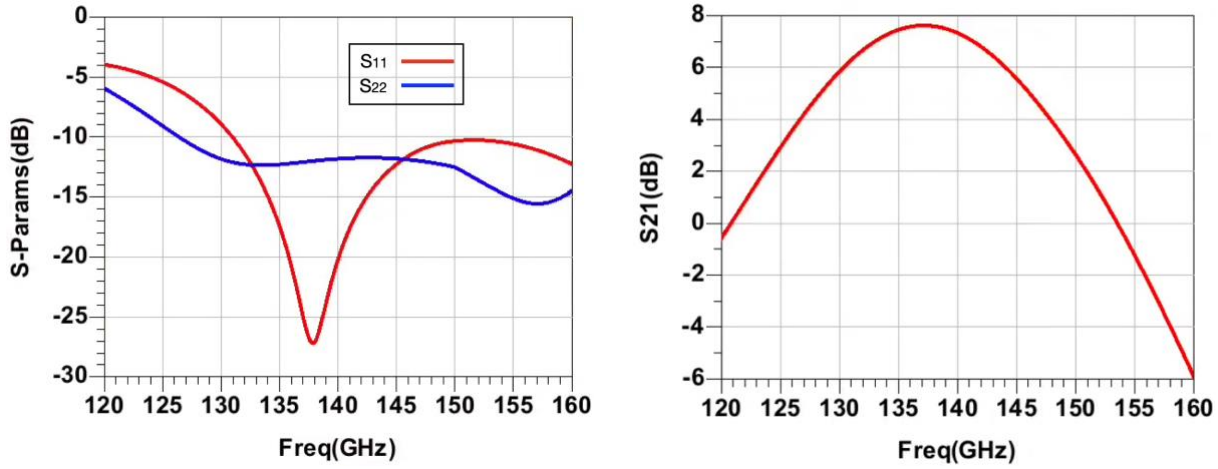


Figure 2.14. Simulated S-parameters of PA chip including input/output pads.

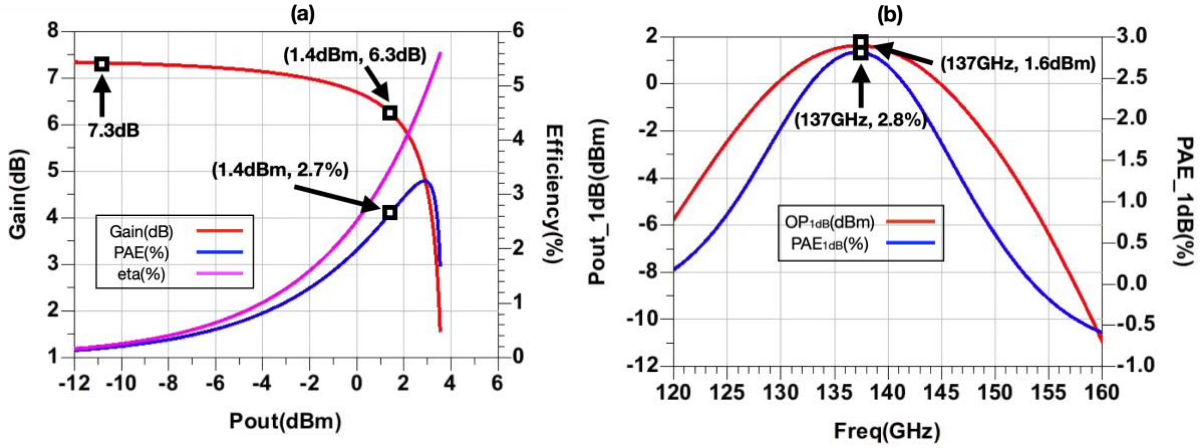


Figure 2.15. (a) Gain compression and efficiency curves at 140GHz (b) PAE_{1dB} and OP_{1dB}.

It is worthy to mention that in reality and designing the integrated transmitter, the input pad and long input TL as well as the input 50Ω matching network would not exist because the PA would be driven using on-chip mixer. Therefore, the gain of PA would be around 7-8dB higher than the current reported numbers. However, the loss due to output pad which also includes

chip-to-PCB transition is inevitable in real life applications and affects the output power of transmitter.

2.7 Performance Summary and Future Design Suggestions

The performance summary of standalone PA, PA with only output pad and full PA chip is listed in Table 2.1. We observed that output P_{1dB} of the standalone PA is 2dB less than the output stage only and this is due to non-linearity of driver stage. To improve the design and increase output P_{1dB}, one solution could be to increase the bias current of driver stage to make them more linear. This method would increase the output P_{1dB} but will decrease the total PAE of system due to more power consumption by drivers. Another approach could be to use inductor degenerated amplifier for the driver stage [18]. Using one of these two linearization methods, the P_{1dB} of PA would get close to P_{1dB} of standalone PA and would be around 4.6dBm at the center frequency.

Another way to increase the output power would be to use two or more versions of current PA design and combine their output power using one of the many on-chip power combining methods [13] [19] [20]. In this approach, the input and output matching network need to be redesigned to split input power and combine output power. The output power will increase by at least 3dB using this method. The output P_{1dB} would then be around 5.5dBm by linearizing the driver stage and using power combining.

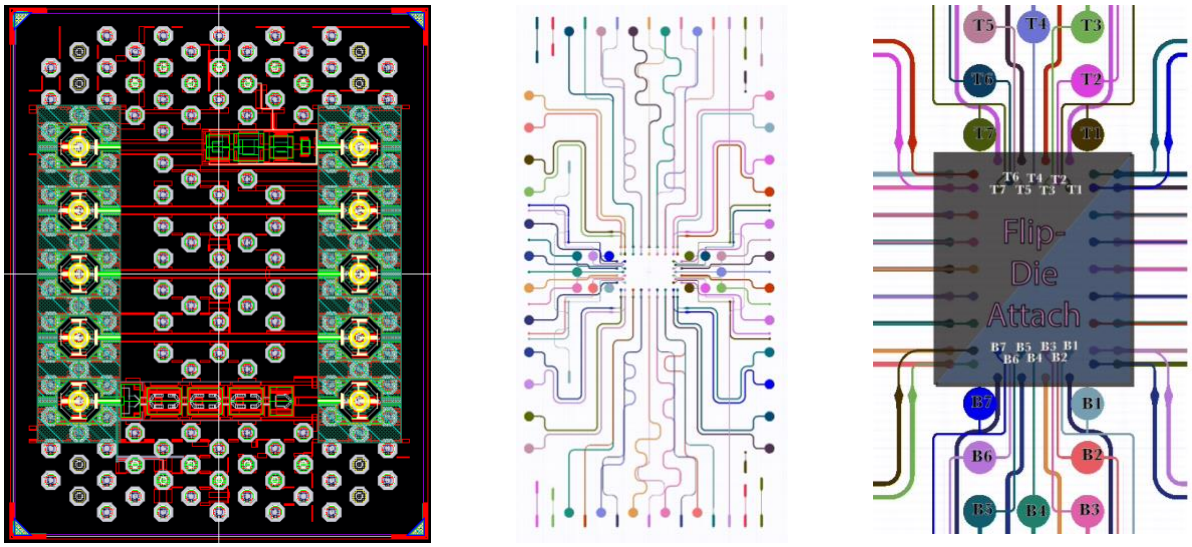
Table 2.1. Performance of power amplifier with and without input/output pads

	Standalone PA	PA with input/output pad
Center Frequency	137 GHz	137 GHz
Bandwidth (3dB)	~ 20 GHz	~ 20 GHz
Gain	10.5 dB	7.7 dB
P_{sat}	5 dBm	4 dBm
$P_{out,1dB}$	2.6 dBm	1.6 dBm
PAE_{max}	5.5%	3.5%
PAE_{1dB}	4%	2.8%

2.8 Packaging and Measurement Provision

A view of final chip layout along with interposer signal routing is shown in Figure 2.16. The chip includes the PA on the top side, a LNA and some test structures designed by my colleague on the bottom and middle part. The interposer was also designed by my colleague. The chip will be flipped to sit on the interposer (flip-die attach). There are 7 pads for bias purposes on the top as well as on the bottom side. The PA chip only uses one of them to guide the reference current to the diode connected PMOS on the chip. The other six pads are pulled-up to VDD using off-chip 100kΩ resistors (Figure 2.17).

The PCB design for measurement of PA chip is depicted in Figure 2.17. An adjustable off-chip resistor is connected to the bias pad of the chip which we know is connected to a PMOS diode connected transistor on the chip. By adjusting the value of resistor, the reference current will change. MAX5477 is a potentiometer used for this purpose. MAX9611 is a current sensor chip to measure the reference current going to chip so we could manually adjust the potentiometer and reference bias current until we find the nominal/optimum bias current. A microcontroller is used to send/receive I2C_SCL and I2C_SDA signals to read the measured current and adjust the potentiometer. A filter is also put on the bias pad for stability purposes. Since the PA circuit is on the same die as the LAN, there should be a way to turn off the PA. A jumper is used in series with potentiometer to provide open circuit. With bias pad being open circuit, the reference current will be close to zero and PA circuit would be turned off. In a later design version, the jumper was replaced with a 3-state buffer (74AUP2G126) which basically either provides open circuit or connects the lower side of potentiometer to ground based on an input enable signal.



(a) **(b)** **(c)**

Figure 2.16. (a) Chip layout (b) Interposer routing (c) A close-up of interposer routing.

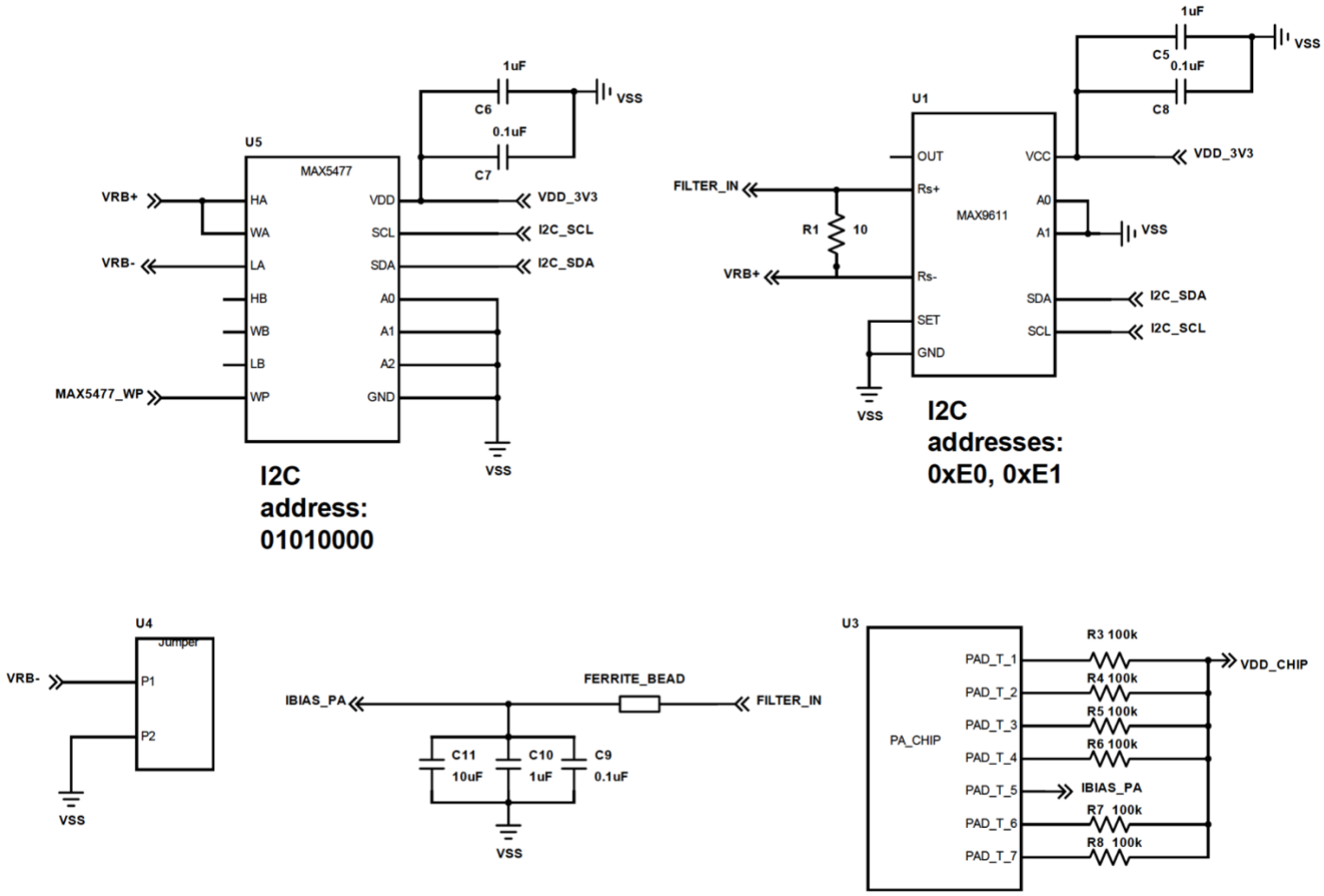


Figure 2.17. PCB schematic design

3 mm-Wave Contactless Interconnect

3.1 Architecture

In academic papers, the performance of chip is usually reported with on-die probe measurement or in a little bit more realistic scenario, with on-interposer probe measurement. However, in real world applications like the ComSenTer project where we need to connect the CMOS chips to III-V chips, a PCB is the best viable and cost effective solution. In the previous chapter, we discussed the design of power amplifier, interposer and PCB. Interposer pads are connected to PCB pads using bumps shown in Figure 3.1. This connection is good enough for bias and low frequency signals. However, how the RF signal is routed from interposer to PCB has critical impact on the final performance of system. The normal pitch between these bumps is around 1mm which is around half-wavelength at 140GHz. This critical distance almost negates the polarity of signal and will have huge detrimental effect on the measurement.

Our team proposed to design a contactless interconnect in which the signal is transmitted from interposer to PCB using near field coupling of two antennas. Numerous bumps and vias on PCB and interposer will be provided to form a confined medium for the wave to propagate from one antenna to another. In this way, the leakage and loss of transmission will be minimized. I was involved in the design of the PCB antenna. The design approach of antenna as well as the interconnect is explained in the next sections.

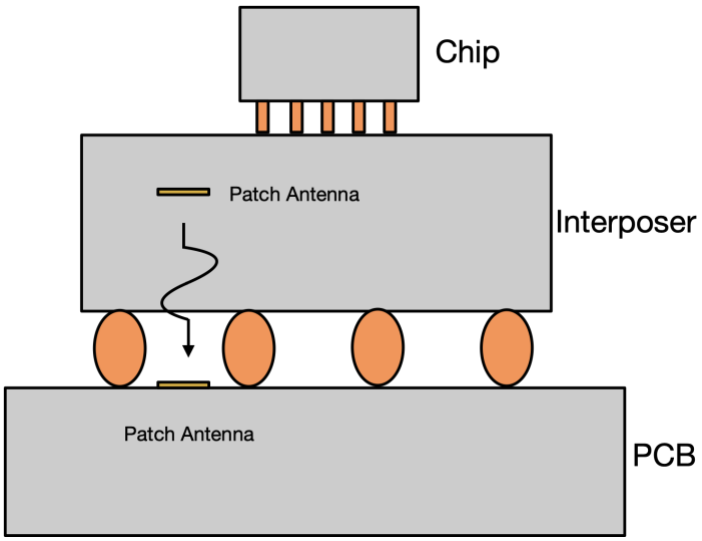


Figure 3.1. mm-wave contactless interconnect scheme

3.2 Initial Design Approach

The first approach that we took to design the interconnect was to design each antenna separately and obtain good far-field performance. In this approach, all bumps and vias are also considered to minimize the field leakage to the sides of antenna and achieve a directive pattern. A patch antenna

is chosen for the PCB antenna. The schematic of path antenna is shown in Figure 3.2. A square type patch is considered and design criteria forces the length of the patch to be equal to $\lambda/2$. A patch antenna by itself has high input impedance but this input impedance could be reduced by moving the excitation point towards the center of patch and also creating an opening in the excitation side of the patch. The distance of patch to the ground is determined through a trade-off between bandwidth and surface waves. The further the ground is from the patch, the more bandwidth would be achieved but this would also increase the chance of exciting surface waves which eventually degrades the performance of antenna. $\lambda/8$ is chosen for the first design iteration. A potential PCB stack-up is depicted in Figure 3.2(b). A different ground for input transmission line is needed to realize a 50Ω characteristic impedance. Megtron6 material is chosen for substrates.

The initial simulation result of the individual patch antenna is illustrated in Figure 3.3. Return loss is more than 10dB over a bandwidth of 9GHz. The bumps have a diameter of 500um diameter and a pitch of 1mm. Vias have 3mil diameter and a pitch of 13mil which are the minimum size and pitch allowed by the PCB manufacturer (Sierra Circuits). There is still some field leakage from the sides due to wide opening between bumps. This gap could be filled with vias which is done in the next design iteration.

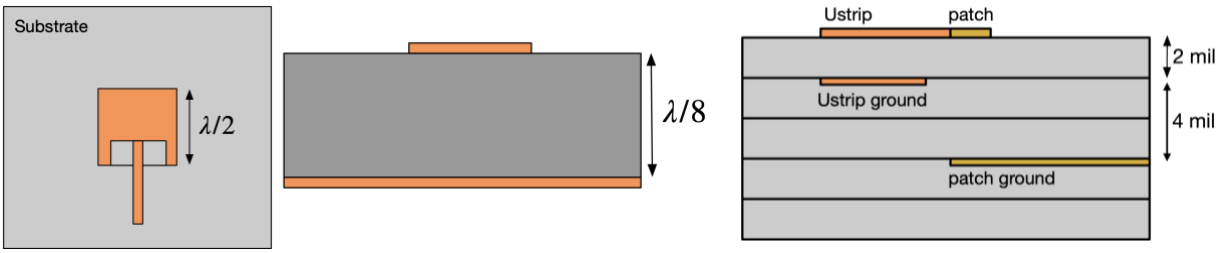


Figure 3.2. (a) General patch antenna view (b) Symmetric PCB stack-up for the antenna

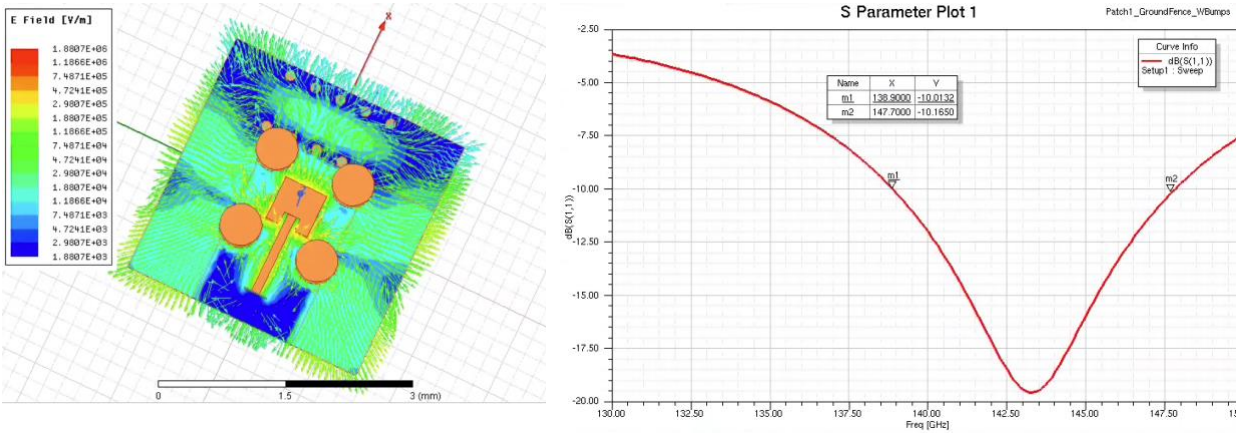
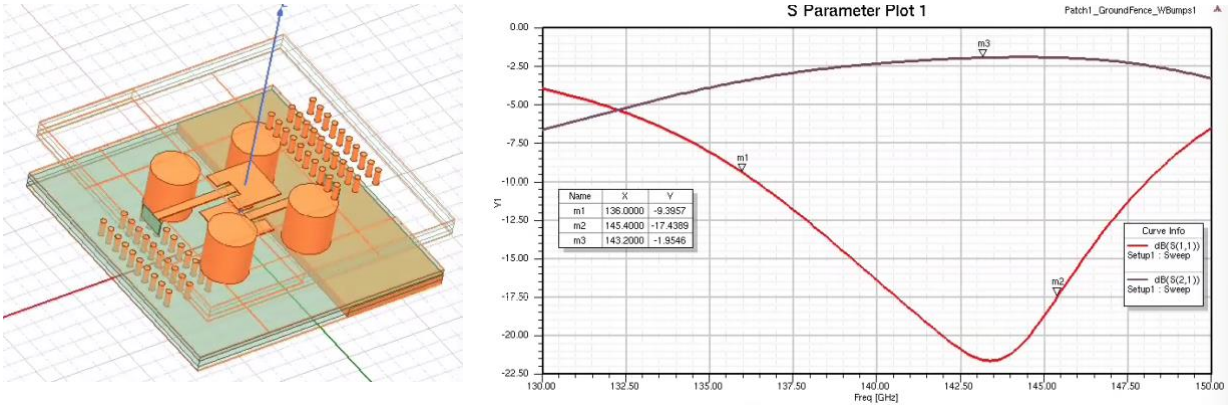
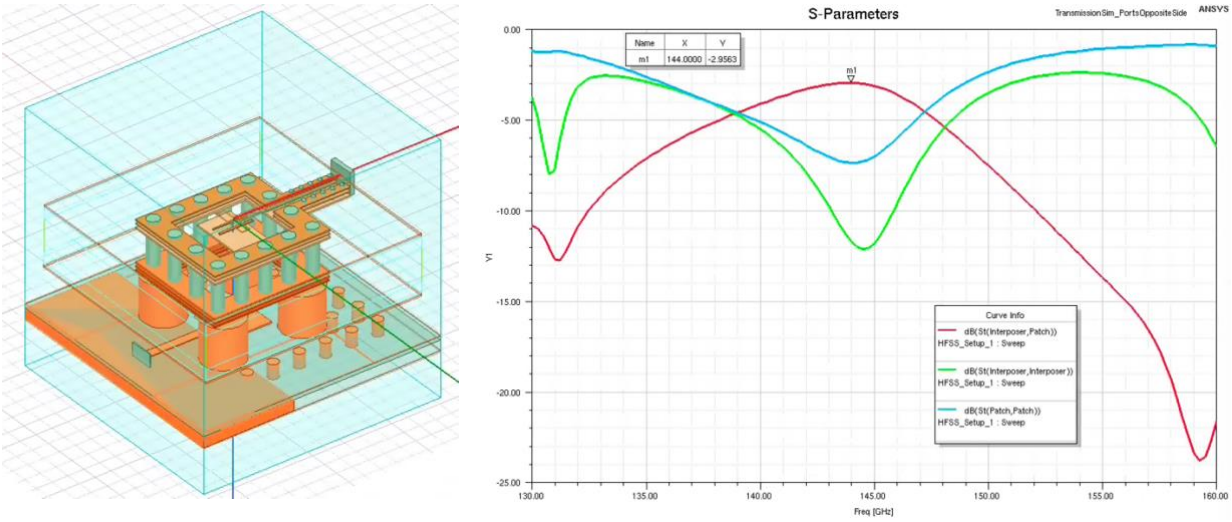


Figure 3.3. (a) Patch Antenna with simulated filed distribution in HFSS (b) return loss



(a) **(b)**

Figure 3.4.(a) Two patch antenna placed 0.5mm away from each other (b) Return loss and transmission



(a) **(b)**

Figure 3.5. (a) Patch antenna placed 0.5mm away from interposer antenna (b) Simulated S-parameters

The next step in design would be to put two of similar patch antennas and measure the signal transmission between them. The simulation picture as well the results are shown in Figure 3.4. As you can see, the bandwidth for return loss of better than 10dB has increased to 11.5GHz. The near field coupling nature of this structure increases the bandwidth compared to a single antenna scenario. The transmission loss is around 2dB at center frequency. This loss could be improved by placing vias in the free space between the bumps but we keep that improvement for the next design iteration. Therefore, the approach sounds feasible with relatively good performance.

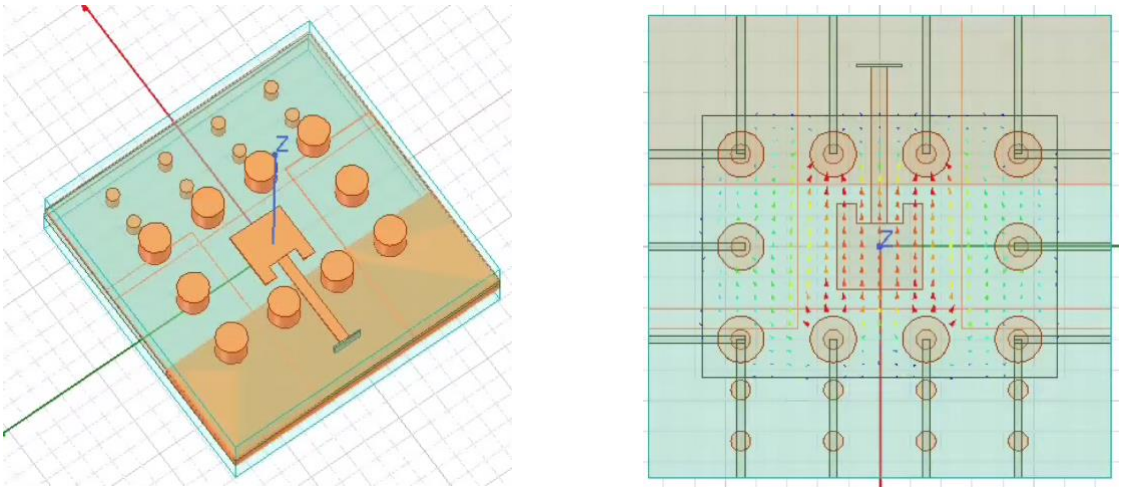
As the next step to ensure the correctness of the design, I simulated the response of patch antenna when it is placed next to the interposer antenna designed by my colleague. The interposer antenna is a variation of a slot antenna. Unfortunately, the results are extremely disappointing and far from what we expected. The simulated return loss and transmission could be found in Figure 3.5. The return loss is pretty much worse than 10dB in the entire frequency range and transmission loss has a best value of around 3dB at center frequency. Lots of tuning to patch antenna parameters was done to try to match both antennas but these efforts were unsuccessful.

3.3 Two-Port Matched Design Approach

We saw that good standalone performance of antennas wouldn't necessarily result in good results for the interconnect behavior. Naive solution would be to actually design the interconnect including two antennas as a whole. However, pursuing this approach requires to tune too many parameters. The simulation time is also much longer than a single antenna simulation. In a search of a method to overcome this issue while providing accurate design procedure, our team studied the behavior of interconnect and reached an approach for this problem: Instead of the second antenna, an imaginary port should be placed on top of antenna, its excitation field should be such that it excites the dominant mode in the medium between two antennas, and the design should be matched both at the input port of antenna as well as at this imaginary port. A schematic of new antenna configuration as well as simulations setup is show in Figure 3.6. The bump pitch and diameter has reduced to 600um and 300um, respectively. This helps to reduce leakage more than the previous design. A view of imaginary port and its field distribution could be found in Figure 3.6(b).

Initial simulation of the new antenna is depicted in Figure 3.7. Two substrates with thickness of 2mil and 5mil are used. Both ports are matched over 7GHz bandwidth and the transmission loss is 1.4dB. Vias have a pitch of 600um as well and as you can see, there is still some field leakage between bumps. This pitch is reduced to 300um, which is the minimum via pitch, in the next simulations.

In an effort to increase the bandwidth and reduce the transmission loss, the via pitch was reduced to 300um which is pretty close to minimum via pitch of PCB manufacturer. The thickness of second substrate is also increased from 5mil to 10mil. The simulation results of antenna with these modifications is illustrated in Figure 3.8. Both ports are matched over 8.5GHz and transmission loss is 0.65dB.



(a) **(b)**

Figure 3.6. (a) Patch antenna with new configuration (b) A close-up view of antenna showing imaginary port and its field distribution

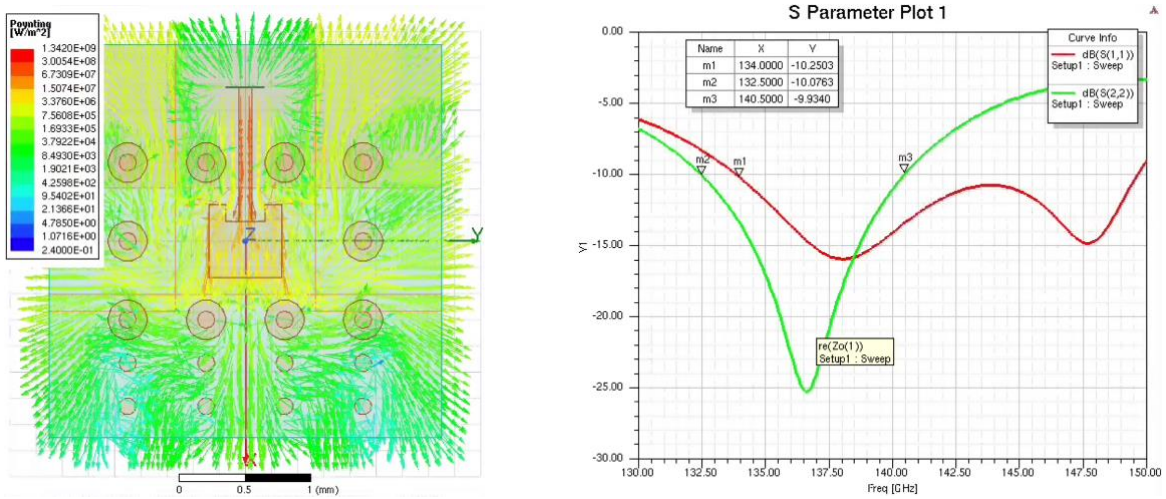


Figure 3.7. Initial simulation result of new antenna configuration

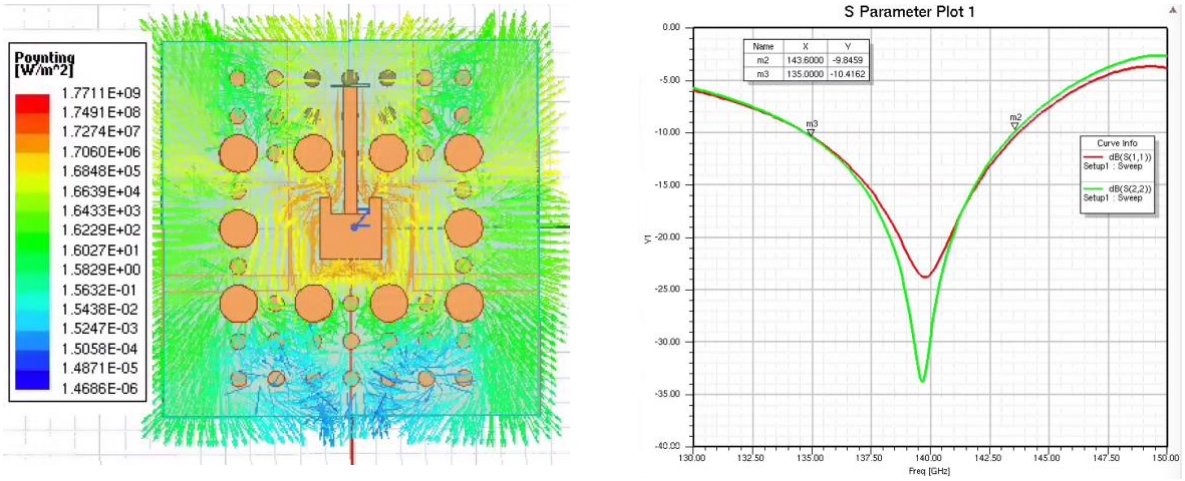


Figure 3.8. Simulation results for 300um via pitch as well as 2mil and 10mil substrate thicknesses

There are ground planes around the patch to help confine the field as you can see in above figures. Simulation shows the further these planes are, the more bandwidth could be achieved. Therefore, these planes are pushed away towards bumps as could be seen in Figure 3.9. The second substrate thickness was also increased to 10mil in previous simulation scenario. In reality, Megtron6 doesn't provide such a thickness and therefore, a three substrates scheme was utilized for designing the antenna and transmission line. The top substrate is a laminate with 2mil thickness, the second one a prepreg with 5mil thickness and third one is a laminate with 4mil thickness.

The final view of antenna and its simulated performance are shown in Figure 3.9. The ground plane on top is connected to transmission line ground as well as the patch ground through stacked vias. Therefore, we have stacked ground planes extending from top layer to patch ground. The field is completely confined and antenna shows 11GHz bandwidth for return loss of better than 10dB and transmission loss is only 0.6dB.

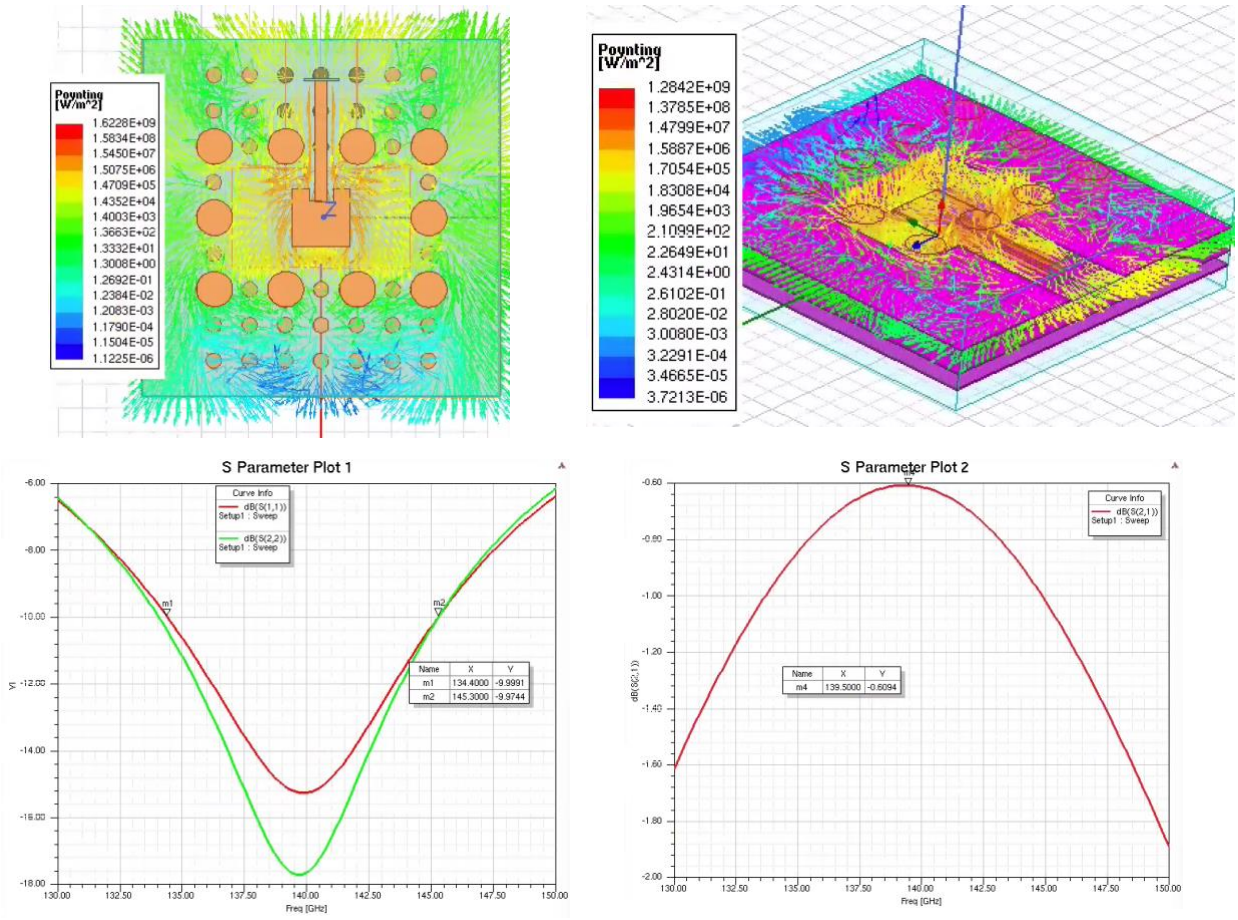


Figure 3.9. Final design and simulation result of PCB patch antenna

This summarizes the design of patch antenna for the contactless interconnect. Further effort on bandwidth improvement is needed, for example by increasing only the width of patch or exciting the patch through a different feeding mechanism such as slot-coupled. However, this method needs a transition of microstrip TL from top layer to bottom layer using vias and this process at 140GHz could add too much parasitics that ends up being worse than microstrip fed patch antenna.

4 Conclusion

4.1 Summary

The design of a compact D-band power amplifier in 28nm CMOS as well as the antenna design for a contactless interconnect are presented in this report. Careful circuit and electromagnetic simulations are used to ensure the correctness of the design.

First, an optimum layout to achieve maximum gain and stability for the transistors is explored. The optimum transistor is then used to do load-pull simulations and determine the proper size to meet output power requirement. By careful EM simulations, a 1:1 transformer implemented on top metal layers of the process is designed to realize the optimum load obtained from load-pull simulation. The driver and intermediate stages are then designed by utilizing low-k transformers to achieve a relatively high bandwidth operation. Packaging and PCB designs are also briefly discussed for measurement purposes.

After presenting the power amplifier chip, the concept of a mm-wave contactless interconnect is introduced. The design utilizes two antennas placed on interposer and PCB to form a near field wireless channel for transferring the RF signal. Step by step design of a patch antenna for PCB side with a thorough analysis of different design parameters as well as optimum simulation setup are discussed. The final interconnect simulation demonstrates 0.6dB loss at 140GHz with 11GHz bandwidth.

4.2 Future Work

There are several modifications that could be done to improve the design. For the power amplifier, designing a more linear driver stage would result in up to 2dB increase in output P_{1dB} as the non-linearity of the current driver stage is preventing the output stage to operate close to its 1dB compression point. A compact and on-chip power combining technique could be explored to increase the output power if longer communication range is needed. After all these steps, one could design the upconverter mixer and complete the transmitter design. Increasing the bandwidth of the PCB antenna is also another improvement to the system performance that could be done through a variety of techniques.

Design and tape-out of a multi-channel transmitter using improved version of current power amplifier and contactless interconnect and adding more circuitry is the next step in this project.

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