Towards Wideband Signal Acquisition Systems

Nima Baniasadi
Ali Niknejad, Ed.

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2020-171
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2020/EECS-2020-171.html

August 14, 2020

Towards Wideband Signal Acquisition Systems

by

Nima Baniasadi

A thesis submitted in partial satisfaction of the

requirements for the degree of

Master of Science, Plan II

in

Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Ali M. Niknejad, Chair
Professor Kristofer S. J. Pister

Summer 2020

The thesis of Nima Baniasadi, titled Towards Wideband Signal Acquisition Systems, is approved:

Chair _____ Date 8/13/2020

_____ Date Aug 14/2020

University of California, Berkeley

IEEE Copyright Notice

Abstract

Towards Wideband Signal Acquisition Systems

by

Nima Baniasadi

Master of Science, Plan II in Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Ali M. Niknejad, Chair

Deep scaling of CMOS technology has provided an exceptional opportunity for wideband high data-rate digital communication. However, since the medium between transceivers accept only analog signals, use of analog to digital converters is inevitable. Currently, ADCs are the bottleneck of communication links, where speed trades off with resolution. Moreover, all digital equalization is desirable but necessitates higher resolution and higher bandwidth ADCs. Several methods for increasing the speed of ADCs are considered in this thesis. An extensive analysis, confirmed by simulations, on the jitter-induced error shows that proper system architecture can improve the total SNDR of ADCs.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

The semiconductor industry has been one of the rapidly-growing industries in the past several decades with an expected annual revenue of more than $500 billion in 2020[1]. As shown in Fig. 1.1, more than one-third of this revenue comes from communication electronics (including wired and wireless electronics) where many different applications such as hand-held mobile electronics and backbone infrastructure demand for higher communication capacity. This industry trend has resulted in 10-fold increase in data rates every five years [1] [3].

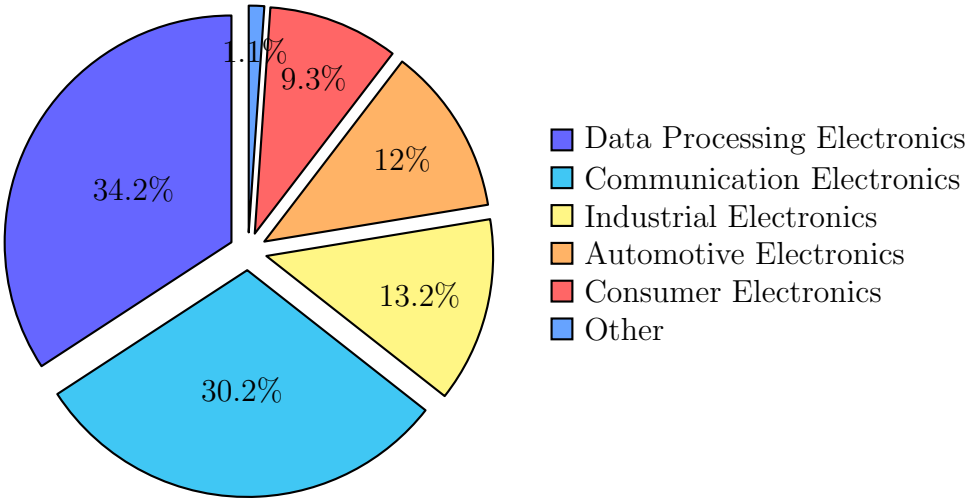


Figure 1.1: Expected global semiconductor sales revenue per category in 2022 [1].

Thanks to the several decades of technology advances based on Moore's law and Dennard's law, digital circuits using CMOS technology and digital signal processing are well-

[1]Compare this with the capacity of batteries used in mobile devices which has improved by only 5-10 percent every year.

suited for such high data-rate applications and incomparable with other technologies when considering performance with other factors such as implementation density, power consumption, integration level, and cost. However, in most of the communication applications, two or more transceivers are talking with each other through a channel medium which naturally carries analog signals (electrical or other). Analog and mixed signal circuits scale poorly with process technology in terms of size and speed compared to digital circuits, so it has encouraged designers to simplify analog and RF circuits for high data rates and large bandwidths to save power and compensate for the impairments by adding complexity on the digital baseband side [3]. This means that before and after each channel medium, analog/digital conversion is required.

The analog-to-digital converter (ADC) is also currently the bottleneck for high data-rate communication systems [4]. This has led researchers to explore the possible fundamental computational limits [5] and also limits coming from the implementation [6]. It can be shown [7] that the maximum capacity C for a receiver with an ADC at the front-end (assuming everything else is ideal) is:

$$C = f_S \times B \tag{1.1}$$

where B is the number of bits of the ADC and f_S is the sampling rate. Intuitively, it should have been expected since unpredictability defines information and with an ADC with B bits, we cannot have more than $f_S \times B$ elements of surprise every second. Although Eq. 1.1 sets a principal upper limit to the capacity based on the number of bits, it is not clear how other ADC nonidealities affect the data rate. Shannon-Hartley theorem can be employed which takes other noise sources into account:

$$C = BW \log_2\left(1 + \frac{P_{Sig}}{P_{Noise}}\right) \tag{1.2}$$

where $BW \leq \frac{f_S}{2}$ is the bandwidth of the input signal, P_{Sig} is its power, and P_{Noise} is the sum of the power of all white noise sources[2]. By statistical modeling in Chapter 2, we will show that the limited number of bits (B) from the ADC results in an effective pseudo-white quantization noise with $P_{QN} = \frac{\Delta^2}{12}$ where Δ is the difference between quantization levels. Therefore, the maximum capacity expected (neglecting all other noise sources) based on Shannon-Hartley theorem is

$$\begin{aligned} C_{max} &= \frac{f_S}{2} \log_2\left(1 + \frac{\left(\frac{2^B \Delta}{2}\right)^2}{\frac{\Delta^2}{12}}\right) \\ &\approx f_S \times \left(B + \frac{\log_2(3)}{2}\right) \end{aligned} \tag{1.3}$$

The extra factor in Eq. 1.3 compared to Eq. 1.1 comes from the error of separate statistical modeling of quantization noise and channel capacity. The result of both theorems are shown

[2]If noise is colored or partially correlated with the input signal, the Eq. 1.2 is not correct.

in Fig. 1.2 where for the benefit of clarity, a continuous range of values of B has been considered.

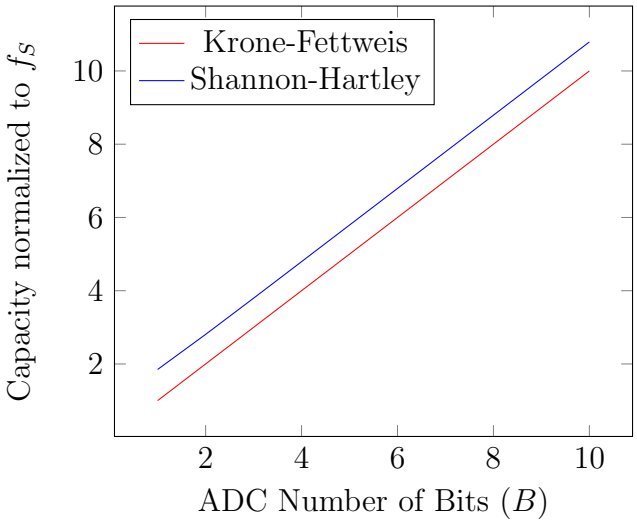


Figure 1.2: Maximum capacity of a channel with an ADC at the receiver.

Both theorems clearly show that the path for increasing the data rate is increasing the speed-resolution product. However, looking into the published results from different surveys [2], one can observe that speed and resolution come with a trade-off. This is shown in Fig. 1.3 where the maximum input frequency $f_{in,hf}$ is used as a proxy for the speed[3], and SNDR[4] or ENOB[5] as a proxy for the resolution.

Speed-resolution trade-off has been linked to the Heisenberg uncertainty principle (at least at higher sample rates). Although the original link in [8] is disputed [5], quantum theory still sets an upper limit to the maximum achievable data rate [7]. However, this fundamental limit is many orders of magnitude higher than the performance of the current state-of-the-art systems. As it will be shown in the next chapters of this thesis, speed-resolution product tends to be limited by our ability to make a low-jitter clock [9].

It should be mentioned that the proxies we used here cannot be directly substituted in Eq. 1.1. It is due to the fact that SNDR and ENOB are most of the times characterized based on a pure sinusoidal input signal. Depending on the different schemes and applications, the system-in-use can beat the expected performance based on those proxies.

[3]Based on the Nyquist sampling theory, $f_{in,hf} \leq \frac{f_S}{2}$, however, ADCs are typically running at higher-than-Nyquist sampling rates.

[4]Signal-to-Noise-and-Distortion-Ratio

[5]Effective Number Of Bits

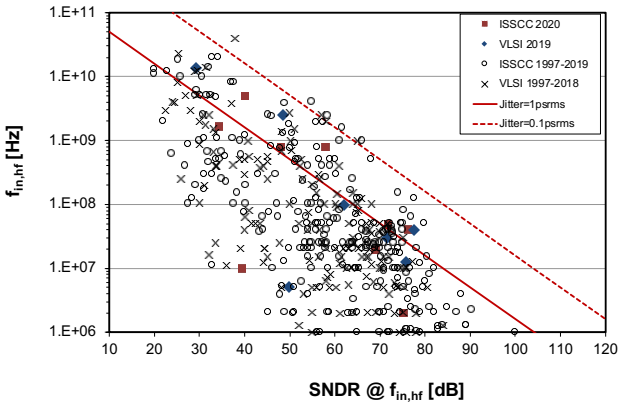


Figure 1.3: 2020 ADC survey showing the speed-resolution trade off [2].

1.2 Increasing the information rate

As mentioned earlier, the channel capacity is ultimately limited by the speed-resolution product. However, SNR[6] of high-speed ADCs in Fig. 1.3 is limited by the clock jitter. Therefore, in this article, we will investigate on methods to increase the effective sampling rate of the ADC, and also methods to mitigate jitter-induced SNR degradation.

It should be mentioned that the data rate and information rate are net necessarily the same. For example, consider a situation in which the channel is shared among multiple users. In this case, the digitized output of ADC has the data for all different users, however, only a portion of that is relevant information for a specific user. Obviously, information rate (R_{info}) is smaller than data rate (R_{data}). If resources were equally shared among M users, information rate for a specific user will be M times lower than the data rate expected by Eq. 1.1. Therefore, with prior processing[7] in the analog domain, the ADC can be substituted by an analog-to-information converter (AIC) which relaxes the speed-resolution. Although AICs are typically more suitable for IoT applications [10] where a priori knowledge such as sparsity in any domain can be exploited, the concept can be expanded to cover to all sorts of applications. Without going too much into details, we will explain AICs in next chapters and how they link to several different parallel architectures.

1.3 Utilizing other technologies, domains, and modalities

As mentioned in the first section, CMOS is the designers' choice for digital processing. However, other technologies may be used next to the CMOS chip in order to relax the

[6]As a proxy for resolution.

[7]Prior processing can be as simple as a mixer or filter or delayed sampler.

CMOS design. For example, in a jitter-limited system, sampling can be done in another semiconductor technology [11] and then rely on the CMOS for quantization.

Furthermore, if sampling is preferred to be done in CMOS, the incoming signal can be continuously stretched in different domains such as time [12] or space [13]. Given that the input signal has a wave nature, spatio-temporal characteristics of the wave can be used [14, 15] to increase the effective sampling rate without an explicit stretching.

Finally, the input signal can be continuously converted from one modality to another one, and samples are taken afterwards. For example, a voltage-to-time converter (VTC) can be used before time-to-digital conversion [16]. Although power consumption can be potentially higher in this architecture [17], it matches well with the scaling trends of the semiconductor industry [18] for area reduction [19].

We will discuss about a few of these strategies in next chapters, however, detailed modeling and analysis are beyond the scope of this thesis.

1.4 Thesis Organization

In this thesis, the focus will be on issues and system design aspects of a wideband signal acquisition while CMOS implementation is explained in details in [20]. In the next chapter, we will cover different strategies designers have proposed to increase the output rate of an analog to digital converter. In Chapter 3, we will briefly review basic concepts and definitions in analog to digital converters since some of them need to be adapted later. As mentioned earlier, jitter is the main limitation of the high-speed ADCs which will be explained in details in chapter 4. Chapter 5 is dedicated to the frequency-interleaved architecture and different noise sources are modeled and simulated. Finally, the last chapter concludes the thesis.

Chapter 2

ADC Basics and Considerations

In this chapter, we will review some of the basic concepts in analog to digital converters. Although this topic is very well covered by the literature, we will review the root cause of some of the problems and debunk common mistakes among published papers.

2.1 Quantization Error

Here we briefly review the model for the quantization error. Let us assume that the input range of $[-1, 1)$ is divided into 2^B bins. If each of these bins is represented by the mid-value, the output error $QN(t)$ will be bounded to $\left[-\frac{\Delta}{2}, \frac{\Delta}{2}\right) = \left[-\frac{1}{2^B}, \frac{1}{2^B}\right)$[1], as illustrated in Fig. 2.1. Therefore, the output can be written as[2]

$$V_{out}(t) = V_{in}(t) + QN(t) \tag{2.1}$$

Assuming that the quantization error is uniformly distributed in the aforementioned range with the error probability of $P(e) = \frac{1}{\Delta}$, the root mean square (RMS) of the quantization error can be calculated as

$$\begin{aligned} {QN_{RMS}}^2 &= \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} |e|^2 \times P(e)\,\mathrm{d}e \\ &= 2 \times \int_0^{\frac{\Delta}{2}} e^2 \times \frac{1}{\Delta}\,\mathrm{d}e \\ &= \frac{\Delta^2}{4 \times 3} \end{aligned} \tag{2.2}$$

Assuming that the quantization error of consecutive samples are uncorrelated[3], $QN(t)$ can be modeled as a white noise with a uniformly distributed power spectral density over

[1] $\Delta = \frac{2}{2^B}$.

[2] Since the input signal is sampled before quantization, t will have discrete values in Eq. 2.1.

[3] In other words, $R_{QN}(\tau) = 0$ if $\tau \neq 0$ where $R_{QN}(\tau)$ is the auto-correlation function.

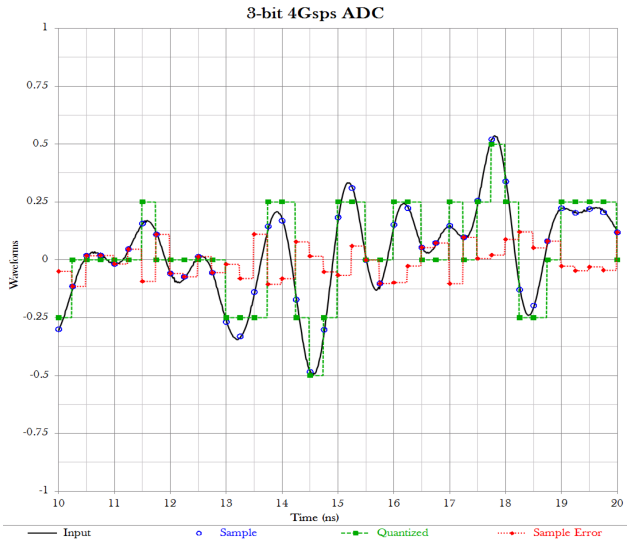
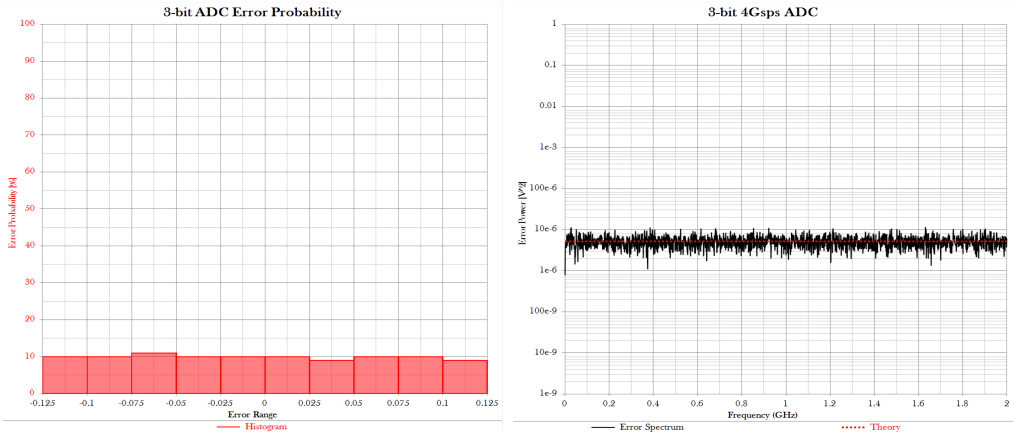


Figure 2.1: Waveforms for a 3-bit 4Gsps ADC



(a) Histogram (b) Spectrum

Figure 2.2: Quantization noise for a 3-bit 4Gsps ADC

the whole ADC frequency range. Strictly speaking, none of the previous assumptions is necessarily valid, but they are very good approximations as Fig. 4.10 suggests [4].

It is very helpful if the quantization noise can be reported as SNR or ENOB. With a

[4]Note that y-axis of Fig. 2.2b has dimension of V^2. In other words, power spectral density is multiplied by the frequency width of each frequency bin.

sinusoidal wave covering the full scale input range of the ADC $[-1, 1)$, we get:

$$\begin{aligned} SNR_{ADC} &= \frac{Signal}{QN} \\ &= \frac{\frac{1^2}{2}}{\frac{\Delta^2}{12}} \\ &= \frac{3}{2}\left(2^B\right)^2 \qquad (2.3) \\ &= 6.02 \times B + 1.76\,[dB] \qquad (2.4) \end{aligned}$$

2.2 Jitter-Induced Error

Since jitter analysis is an integral part of this thesis, we will briefly introduce its impact here and postpone details to the next chapters. First let us find what happens when a sampling stage has $\sigma(t) = \frac{Phase\,Noise}{\omega_{Sampling}}$[5] uncertainty on the sampling edge. For a sinusoidal input with frequency of ω_{in} and amplitude of A, the sampled output is:

$$V_{in}(t) = A\sin(\omega_{in}t) \xrightarrow{After Sampling} V_{Out}(kT_S) = A\sin(\omega_{in}(kT_S - \sigma(kT_S))) \qquad (2.5)$$

where T_s is the ideal sampling period. Note that sampling happens when

$$t + \sigma(t) = kT_S$$

Assuming small $\sigma(t)$, we can divide the signal and noise in the previous equation:

$$V_{Out}(kT_s) \approx A\sin(\omega_{in}kT_S) - \omega_{in}\sigma(kT_S)A\cos(\omega_{in}kT_S) \qquad (2.6)$$

Therefore, the noise components in Laplace domain is nothing but the convolution of jitter and the derivative of the input signal:

$$V_{Noise}(s) \approx -\sigma(s) * (s\,V_{in}(s)) \qquad (2.7)$$

and therefore, at the presence of sampling time uncertainty, the SNR will be limited to

$$SNR = \frac{\frac{1}{2}A^2}{\frac{1}{2}(\omega_{in}\sigma_{RMS}A)^2} = \frac{1}{(\omega_{in}\sigma_{RMS})^2} \qquad (2.8)$$

where σ_{RMS} is the RMS power of jitter. Statistical analysis also confirms that the SNR is independent from the the jitter profile[6], as long as jitter power stays constant [21]. Results of simulation (Fig. 2.3) shows agreement with the theory. Although it may seem boundless, increasing $\sigma(t)$ at some point breaks the assumption made earlier. A large signal analysis shows that for almost any input signals, SNR due to the jitter approaches $-3dB$ at the limit when DC component is removed [22].

[5]Note that in this section, $\sigma(t)$ is defined as phase error normalized by the oscillation frequency.

[6]Assuming that $\sigma(t)$ has no DC component.

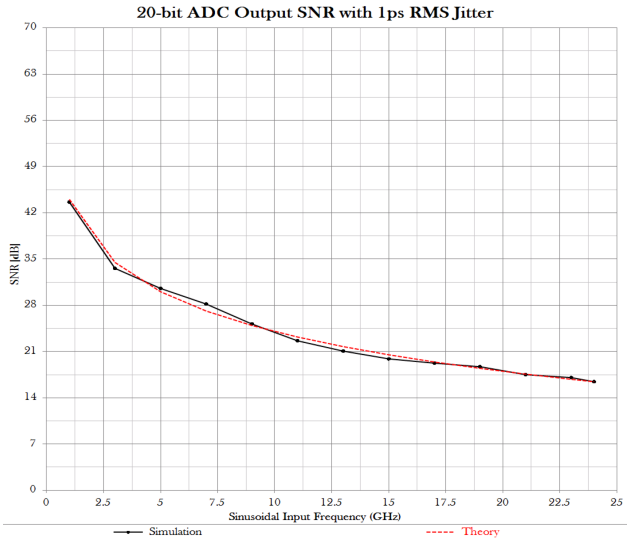


Figure 2.3: Output SNR of a 20-bit ADC with 1ps RMS Jitter as a function of input frequency

2.3 Misinterpretation: Correlated vs Uncorrelated

One common place to make a mistake is whether two nodes in a system are correlated or not, considering both desired signals and undesired noise sources[7]. For example, let us consider a situation for an M-channel time-interleaved ADC. Neglecting quantization error, the output of each ADC, $y_m(t)$, can be written as:

$$y_m(t) = x(t) \sum_k \delta \left(t - kT_{CK} - \frac{(m-1)T_{CK}}{M} \right) \tag{2.9}$$

where $m \in [1, M]$ is the channel index and T_{CK} is the sampling period of each channel while $\frac{(m-1)T_{CK}}{M}$ takes care of proper time-interleaving. Author of [23] states that "the signal power in $Y_1(f) + Y_2(f)$ is equal to $4P_X$ because the desired components $Y_1(f)$ in $Y_2(f)$ and add in-phase" where P_X is the power of $x(t)$ and $Y_m(f)$ is the frequency domain representation of $y_m(t)$. This interpretation may lead to the question of whether M interleaved stages can help to improve the output SNR. The rational here is that signals will be correlated and add in-phase while quantization noise will be uncorrelated[8]. In order to answer this question, Let us calculate the correlation between $y_1(t)$ and $y_2(t)$ once the continuous-time analog signal

[7] We will deal with correlated jitter-induced errors in the next chapter.

[8] Similar to phased array systems.

is reconstructed:

$$
\begin{aligned}
R_{y_1,y_2} &= \lim_{T\to\infty}\frac{1}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}}\left[\operatorname{sinc}\left(\frac{t}{\frac{T_CK}{M}}\right)*y_1(t)\right]\left[\operatorname{sinc}\left(\frac{t}{\frac{T_CK}{M}}\right)*y_2(t)\right]\mathrm{d}t \\
&= \lim_{T\to\infty}\frac{1}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}}\left[\operatorname{sinc}\left(\frac{t}{\frac{T_CK}{M}}\right)*\sum_k x(t)\delta\left(t-kT_{CK}\right)\right]\times \\
&\qquad\left[\operatorname{sinc}\left(\frac{t}{\frac{T_CK}{M}}\right)*\sum_{k'} x(t)\delta\left(t-k'T_{CK}-\frac{T_{CK}}{M}\right)\right]\mathrm{d}t \\
&= \lim_{T\to\infty}\frac{1}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}}\int\int\sum_k\sum_k{}'\, x(t-u)x(t-u')\,\mathrm{d}t\,\mathrm{d}u\,\mathrm{d}u'\times \\
&\qquad\delta\left(t-u-kT_{CK}\right)\operatorname{sinc}\left(\frac{u}{\frac{T_CK}{M}}\right)\delta\left(t-u'-k'T_{CK}-\frac{T_{CK}}{M}\right)\operatorname{sinc}\left(\frac{u'}{\frac{T_CK}{M}}\right) \\
&= \lim_{T\to\infty}\frac{1}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}}\sum_k\sum_k{}'\, x(kT_{CK})x(k'T_{CK}+\frac{T_{CK}}{M})\,\mathrm{d}t\times \\
&\qquad\operatorname{sinc}\left(\frac{t-kT_{CK}}{\frac{T_CK}{M}}\right)\operatorname{sinc}\left(\frac{t-k'T_{CK}-\frac{T_{CK}}{M}}{\frac{T_CK}{M}}\right) \\
&\qquad=\sum_k\sum_k{}'\, x(kT_{CK})x(k'T_{CK}+\frac{T_{CK}}{M})\times \\
&\qquad\left[\lim_{T\to\infty}\frac{1}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}}\operatorname{sinc}\left(\frac{t-kT_{CK}}{\frac{T_CK}{M}}\right)\operatorname{sinc}\left(\frac{t-k'T_{CK}-\frac{T_{CK}}{M}}{\frac{T_CK}{M}}\right)\mathrm{d}t\right]
\end{aligned}
\tag{2.10}
$$

The term in the bracket is the auto-correlation of the $\operatorname{sinc}(t)$ function, which is another $\operatorname{sinc}(t)$ function:

$$R_{\operatorname{sinc}}(t) = \operatorname{sinc}(t) \tag{2.11}$$

Therefore, for integer values of k and k', we get

$$
\begin{aligned}
R_{\operatorname{sinc}}(M(k-k')-1) &= \operatorname{sinc}(M(k-k')-1) \\
&= 0
\end{aligned}
\tag{2.12}
$$

which means that $y_1(t)$ and $y_2(t)$ are uncorrelated.

$$R_{y_1,y_2} = 0 \tag{2.13}$$

This means that ADCs' outputs are uncorrelated and the quoted statement of [23] is not accurate. Moreover, time-interleaving neither helps nor degrades output SNR since

$$SNR_{TI-ADC} = \frac{M\times Signal}{M\times QN} = SNR_{ADC} \tag{2.14}$$

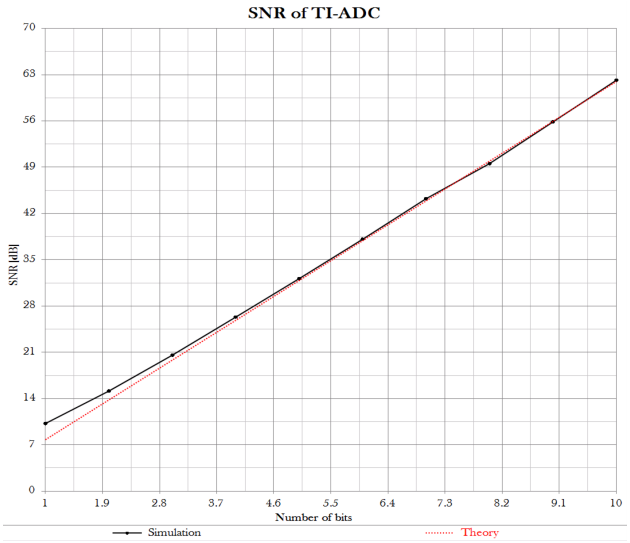


Figure 2.4: SNR vs ADC resolution in TI-ADC

Fig. 2.4 shows the SNR in TI-ADC simulation vs ADC resolution in comparison with the theory developed in Eq. 2.3.

Similar misinterpretation may occur in the context of frequency-folded ADCs (Fig. 3.7[9]). Authors of [24] state that "since each baseband path and sub-ADC is independent, noise injected into each path will be uncorrelated. However, signal content in each path is correlated, with only a relative phase shift between paths. Thus the signals add in voltage while the baseband noise adds in power." First, it should be noted that relative shift is enough to make signals uncorrelated (e.g. $\sin(t)$ and $\cos(t)$). Second, any signal processing should be considered before one can conclude on the correlation of two different paths. From our discussion on the Hadamard modulation in section 3.1, we will show that perfect signal recovery requires multiplication of the each channel's output by interleaved pulse sequences. Let us find the correlation of the signal content in the first two paths:

$$\begin{aligned} R_{y_1,y_2} &= \lim_{T\to\infty} \frac{1}{T} \int_{\frac{-T}{2}}^{\frac{T}{2}} y_1(t) y_2(t) \mathrm{d}t \\ &= \lim_{T\to\infty} \frac{1}{T} \int_{\frac{-T}{2}}^{\frac{T}{2}} \left(\left[x(t) \sum_k \Pi_{\frac{T_{CK}}{M}} \left(t - kT_{CK}\right) \right] * h(t) \right) \sum_k \Pi_{\frac{T_{CK}}{M}} \left(t - kT_{CK}\right) \mathrm{d}t \times \\ &\left(\left[x(t) \sum_k \Pi_{\frac{T_{CK}}{M}} \left(t - kT_{CK} - \frac{T_{CK}}{M} \right) \right] * h(t) \right) \sum_k \Pi_{\frac{T_{CK}}{M}} \left(t - kT_{CK} - \frac{T_{CK}}{M} \right) \\ &= 0 \end{aligned} \tag{2.15}$$

[9]This architecture will be introduced in the next chapter.

where $h(t)$ is the impulse response of low-pass filters and $\Pi_{\frac{T_{CK}}{M}}(t)$ is the rectangular pulse train with pulse width of $\frac{T_{CK}}{M}$. Note that since the pulse train functions in the digital domain are non-overlapping, the final output of different channels are uncorrelated. N times SNR boosting due to oversampling is expected if only one the sub-bands are considered, which is explained next.

2.4 Oversampling

Consider a situation in which the sample rate (f_S) of the ADC is OSR times higher than the Nyquist rate of a bandwidth-limited (BW) input signal[10].

$$f_S = 2 \times BW \times OSR \tag{2.16}$$

In this situation, any source of noise with flat spectral density (including thermal noise, quantization noise, and jitter induced errors as long as jitter itself has a white spectral content) at the output of ADC can be filtered out since only a fraction ($\frac{1}{OSR}$) of the output spectrum contains data. Therefore, from Shannon's point of view (Eq. 1.2), data-rate can be maintained if for each 1-bit reduction in the number of bits of ADC, sampling rate grows by a factor of 4.

$$B - \alpha \Leftrightarrow f_S \times 4^{\alpha} \tag{2.17}$$

Now, let us examine the total capacity (Eq. 1.1) under this frequency scaling condition:

$$C = (B - \alpha) \times f_S \times 4^{\alpha} \tag{2.18}$$

This shows that for a bandwidth-limited input signal, choosing quantization resolution B between 1 bit and 2 bits ($B = \ln(4) = 1.38$) minimizes the capacity limitations due to the ADC. It is worth mentioning that from Heisenberg's uncertainty principle, existence of an optimum for quantization resolution B between 1 bit and 2 bits ($B = \frac{1}{\ln(2)} = 1.44$ in this case) for maximum data rate is expected [7].

2.5 Testing Methods and Drawbacks

The concept of converting analog signals to digital words is very simple. Yet quantifying the performance and how it limits the system as a whole is challenging given that in most systems, the output of ADC is not the ultimate goal of the system. The IEEE standard [25] provides different test methods for this purpose by considering an ADC as a standalone block.

The most commonly used test setup uses a sine wave as the input of the ADC. The advantage of using a sine wave is that:

[10]It should be mentioned that the input signal does not need to be in the first Nyquist zone.

- Appropriate signals are readily available using a sine wave generator.
- It is easy to establish the quality of the sine wave using spectrum analyzer.
- Filters can easily remove harmonics (or sub-harmonics) of the sine wave for a clean input waveform.
- Locked frequency synthesizers can be used to generate the sine wave and the ADC clock for precise timing.

Therefore, many performance metrics such as SNR or ENOB are measured using a sine wave input. However, this convention might not be appropriate for some cases, such as in a hybrid filter bank or a frequency-interleaved architecture where input signal gets completely filtered out before sub-ADCs in undesired channels. Therefore, we have to either re-consider testing methods, or try to rationally correct for any errors.

Moreover, a sine wave test performance does not necessarily represent the performance of the system. For example, while a test sine wave can use the whole ADC's input full scale range, in practice, enough margin should exist such that ADC's input does not saturate. In fact, saturation of input or output of ADC changes the statistical models used in different parts which results in deviation of measurement results from simulations.

Although in this thesis, we will mostly consider standalone ADCs and methods to improve their functionality and performance, since ADCs are usually used as a part of a system with predefined parameters, optimum ADC specifications and architecture changes based on the application.

For example, consider an ADC with clock jitter in a data link where the incoming signal with limited bandwidth of ω_{max} is random in time (uniform power spectral density of $P(\omega) = \frac{P_{sig}}{\omega_{max}}$). Using Eq. 2.6 and breaking the input spectrum into small sub-bands, we can write

$$\begin{aligned} P_{noise} &= \int_0^{\omega_{max}} (\omega\sigma_{RMS})^2 P(\omega)\,\mathrm{d}\omega \\ &= \frac{(\omega_{max}\sigma_{RMS})^2}{3} P_{sig} \end{aligned} \tag{2.19}$$

The factor of 3 (nearly $10dB$ improvement compared to Eq. 2.8) is due to the fact that in the conventional test method, a distributed quantity (spectral content) is approximated by a lumped quantity (sinusoidal wave at ω_{max}) [23]. Similar results can be derived by performing a statistical analysis [21]. Therefore, in a wideband system, jitter specifications can be almost $10dB$ relaxed.

Better performance does not necessarily come from wide bandwidth. Consider a software-defined radio receiver for example, in which only a narrow portion of the converted signal is relevant. Per wireless standards, these systems should tolerate out-of-band interfering signals

with known maximum power based on the wireless standard. Since jitter-induced noise is the convolution of (the derivative of) the input signal and the jitter, low-frequency content[11] of the jitter will not show up in the band-of-interest which means the system can tolerate much higher RMS jitter. In fact, based on the wireless standard, the optimum jitter spectrum can be calculated [26]. Therefore, we will try to distinguish between low-frequency content and wideband content of the jitter when it comes to SNR calculation since low-frequency content can be tolerated in many applications and even compensated (e.g. by using a CDR loop).

[11] Close-in phase noise.

Chapter 3

Increasing Information Rate

In this chapter, we try to go over different structures proposed to increase the effective speed of the analog-to-digital converter. Remember that based on the sampling theorem, in order to perform a perfect digital reconstruction of an analog input signal with a bandwidth of f_{max}, samples at a rate of $f_S = 2 \times f_{max}$ are required.

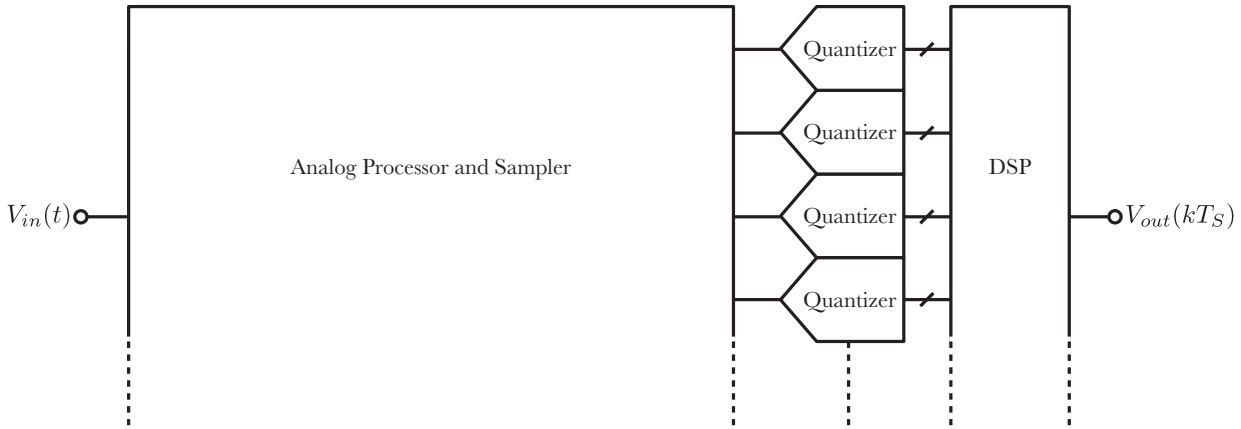


Figure 3.1: Running multiple quantizers in parallel.

Methods of increasing the speed of an ADC can be divided into two general categories:

1. Increasing the speed of the quantizer unit: In this category, designer aims to increase the speed of the quantizer. Popular topologies are flash, pipelined, successive-approximation register (SAR), and their combinations.

2. Utilizing quantizers in parallel: In this category, with the assumption of a *fixed quantization time*, multiple low-speed quantizers are working in parallel. Before and after quantizer banks, proper analog (analysis) and digital (synthesis) processing are re-

quired for a perfect signal reconstruction. It should be mentioned that processing units still have to satisfy the Nyquist criteria.

Since the assumption of *fixed quantization time* is not realistic, in order to increase the effective speed of an ADC, there always exists a trade-off between the two aforementioned categories; whether the designer should increase the speed of the each quantizer unit or increase the number of units working in parallel. We will mostly focus on the second category in this chapter as depicted in Fig. 3.1, while providing insight into the trade-offs.

3.1 Modulation techniques

In this section, we will introduce some of the proposed methods to use multiple quantizers by modulating the signal before digitizing. While pros and cons are briefly mentioned, details can be found in other references such as [27, 28].

Time Interleaving

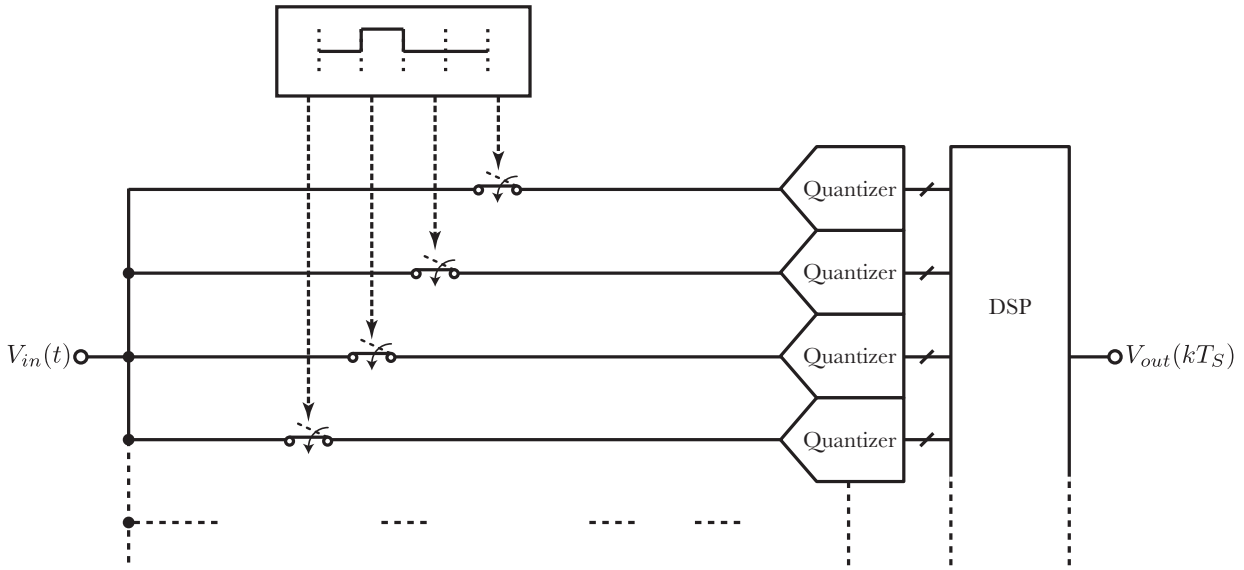


Figure 3.2: Time-interleaved structure.

Time interleaving (shown in Fig. 3.2) is currently the most popular method of increasing the speed. In this method, each quantizer is connected to a separate sampler (sampling at $\frac{f_S}{N}$) which are driven from N different clock edges. Therefore, quantizer conversion time is N-times relaxed.

Moreover, this method may reduce the power consumption of the whole ADC. Since most of the state-of-the-art quantizers are already working at the limits of the technology, power-speed trade-off is nonlinear, and relaxing conversion time by N results in more than N times reduction in the power consumption of the quantizer [23]. Therefore, considering the total power consumption, we expect that:

$$P_{Quantizer_{f_S}} \geq N \times P_{Quantizer_{\frac{f_S}{N}}} \tag{3.1}$$

It should be mentioned that using 50% duty cycle for the sampler relaxes the step-response time of the sampler, however, the small-signal bandwidth of the sampler still has to exceed the bandwidth of the input signal which will become the bottleneck. In fact, [23] shows that a medium-resolution ADC negligibly benefits from interleaving for $N > 4$.

Finally, it should be mentioned that while gain and offset mismatch of the quantizers can be calibrated since the corresponding error is either a DC error or fully correlated with the input signal, sampling time mismatches, which manifest themselves in both the generation and the distribution of the clock phases, cannot be easily calibrated since the corresponding error has no resemblance to the input signal [23].

Quadrature Mirror Filter Banks (QMF)

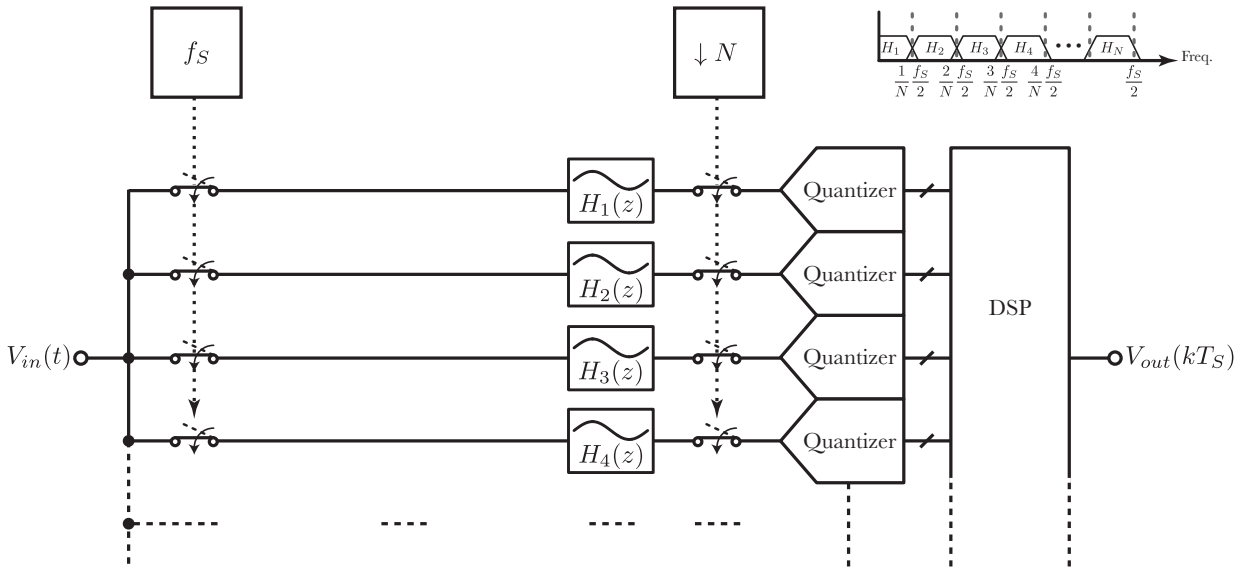


Figure 3.3: High-speed ADC incorporating a QMF Bank.

Using quadrature mirror filter banks (shown in Fig. 3.3) can relax the timing mismatch problem. In a simplified model, after sampling at a rate of f_S, discreet-time samples are

passed though discrete-time filters, usually designed by switched capacitors. Each filter is designed to pass a specific Nyquist Zone and filter out any spectral content outside of the selected Nyquist zone. The output of the filter is then down-sampled by N and passed to quantizers. Since the input signal passes through a proper bandpass filter, despite sub-sampling, harmonic folding does not introduce any problems [29].

Since all samplers are driven from the same clock source (as opposed to the time-skewed clocks in in a time interleaved ADC), this architecture is less prone to the time-mismatch issue. Furthermore, assuming that filters are ideal, each channel is only responsible for a specific frequency band. Therefore, in applications where phase distortion can be tolerated, this approach offers an interesting alternative [30].

Finally, it should be mentioned that this technique does not overcome the need for high-speed sampling circuits.

Hadamard Modulation

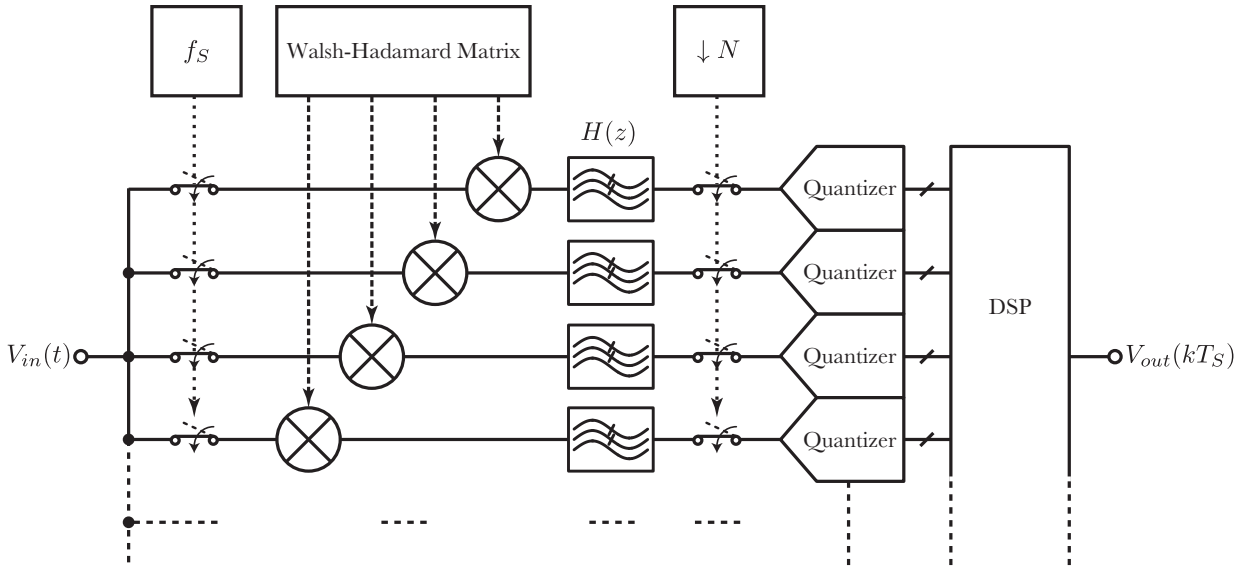


Figure 3.4: Parallel quantization using Hadamard modulation.

In QMF architecture, N different analog filters should be designed separately. If sampled data is modulated before the filters, all the filters can be identical.

One such modulation is Hadamard modulation which was originally proposed to be used in the context of $\Pi\Delta\Sigma$ modulators [31]. A Hadamard matrix ($M_{N\times N}$) consists exclusively of plus and minus ones and has the property that $M^T M = NI$ [1]. Samples on each channel are

[1] I is the identity matrix.

multiplied by a periodically-extended sequence from one row of Hadamard matrix, filtered, quantized, and multiplied by the same sequence[2]. A sufficient condition for existence of an $N \times N$ Hadamard matrix is that N be a positive power of two in which the Walsh matrix can be used.

Eq. 3.2 shows an 8×8 Walsh matrix. By analyzing this matrix, it can be observed that multiplying each row by the input signal is effectively mixing different frequency components. The advantage of multiplying by a Walsh matrix instead of mixing by sine and cosine functions is that the circuit implementation of multiplying by plus and minus ones[3] is much easier than mixing by corresponding functions. Furthermore, Walsh matrix takes care of harmonic folding which is not an easy task in conventional mixing by sinusoidal functions. In fact, N-path filters can be implemented using Walsh matrices [32]. Due to the required harmonic correction, rows of Walsh matrices of higher order cannot be associated with one single frequency.

$$M_8 = \begin{bmatrix} +1 & +1 & +1 & +1 & +1 & +1 & +1 & +1 & DC \\ +1 & +1 & +1 & +1 & -1 & -1 & -1 & -1 & I : \frac{f_S}{8} \\ +1 & +1 & -1 & -1 & -1 & -1 & +1 & +1 & Q : \frac{f_S}{8} \\ +1 & +1 & -1 & -1 & +1 & +1 & -1 & -1 & I : \frac{2f_S}{8} \\ +1 & -1 & -1 & +1 & +1 & -1 & -1 & +1 & Q : \frac{2f_S}{8} \\ +1 & -1 & +1 & -1 & -1 & +1 & -1 & +1 & I : \frac{3f_S}{8} \\ +1 & -1 & -1 & +1 & -1 & +1 & +1 & -1 & Q : \frac{3f_S}{8} \\ +1 & -1 & +1 & -1 & +1 & -1 & +1 & -1 & \frac{4f_S}{8} \end{bmatrix} \tag{3.2}$$

Discrete-time analysis is provided in [31]. However, here we provide a generalized and simplified continuous-time mathematical framework. Let us assume that modulation in row k is performed by multiplying the input signal with modulation function $M_k(t)$. Then, the modulated signal is passed through a filter and demodulated by multiplication by $M'_k(t-t_d)$ where t_d is the relative delay of the modulation and demodulation functions.

$$V_{out}(t) = \sum_{k=1}^{N} M'_k(t - t_d)\left[(V_{in}(t)M_k(t)) * H(t)\right] \tag{3.3}$$

where $(*)$ is the convolution operation and $H(t)$ is the impulse response of the filter. By

[2]Or a delayed version of the sequence.

[3]Either pass the signal or invert its polarity.

representing the convolution operation in the integral form, we get

$$V_{out}(t) = \sum_{k=1}^{N} M'_k(t - t_d) \int_{-\infty}^{\infty} V_{in}(t - \tau) M_k(t - \tau) H(\tau) \mathrm{d}\tau \tag{3.4}$$

By changing the order of summations and multiplications, we arrive to a simplified equation

$$V_{out}(t) = \int_{-\infty}^{\infty} V_{in}(t - \tau) \left[\sum_{k=1}^{N} M'_k(t - t_d) M_k(t - \tau) H(\tau) \right] \mathrm{d}\tau \tag{3.5}$$

If $\sum_{k=1}^{N} M'_k(t - t_d) M_k(t - \tau)$ is chosen to be independent of t, the above equation can be further simplified as

$$V_{out}(t) = \int_{-\infty}^{\infty} V_{in}(t - \tau) \left[R_{t_d}(\tau) H(\tau) \right] \mathrm{d}\tau \tag{3.6}$$

where $R_{t_d}(\tau) = \sum_{k=1}^{N} M'_k(t - t_d) M_k(t - \tau)$. In the frequency domain, we have

$$V_{out}(f) = \left[R_{t_d}(f) * H(f) \right] V_{in}(f) \tag{3.7}$$

A useful scenario is when $R_{t_d}(f)$ is an impulse train and $H(f)$ is a brick-wall filter. By choosing the right bandwidth for the filter, its impact can be completely compensated after demodulation. Implementation of a brick-wall filter might not be feasible depending on the application. As a popular alternative, integrate-and-dump (H_{I-D}) filters can replace the brick-wall filter[4] as long as

$$R_{t_d}(t) H_{I-D}(t) = \delta(t) \tag{3.8}$$

where $\delta(t)$ is the Dirac delta function. Therefore, for $H_{I-D}(t)$, $R_{t_d}(t)$ needs to have a single impulse inside the integration window and any arbitrary value out of that. This criterion can be easily satisfied by making sure that the integration window is equal to the periodicity of the modulator.

Hybrid Filter Banks (HFB)

Switched capacitors incorporated in the QMF method limits the speed of the system. Therefore, it makes sense to replace discrete-time QMF filters with continuous-time filters (e.g. LC filters). The new architecture, shown in Fig. 3.5, is called a hybrid filter bank ADC since analysis filters are in the analog domain while synthesis filters [5] are in the digital domain.

Frequency-band separation before sampling allows the sampler to work at N-times lower rate. However, samplers used in higher frequency bands still have to support the high input bandwidth of the corresponding frequency range [33].

[4] Although there is no obvious penalty in the continuous-time analysis, down-sampling by N after the filter may introduce errors since integrate-and-dump filters do not provide enough bandwidth reduction.

[5] Reconstruction of the signal in the digital domain is called synthesis "filter" in the literature since it is usually composed of an up-sampler followed by band-selection filters.

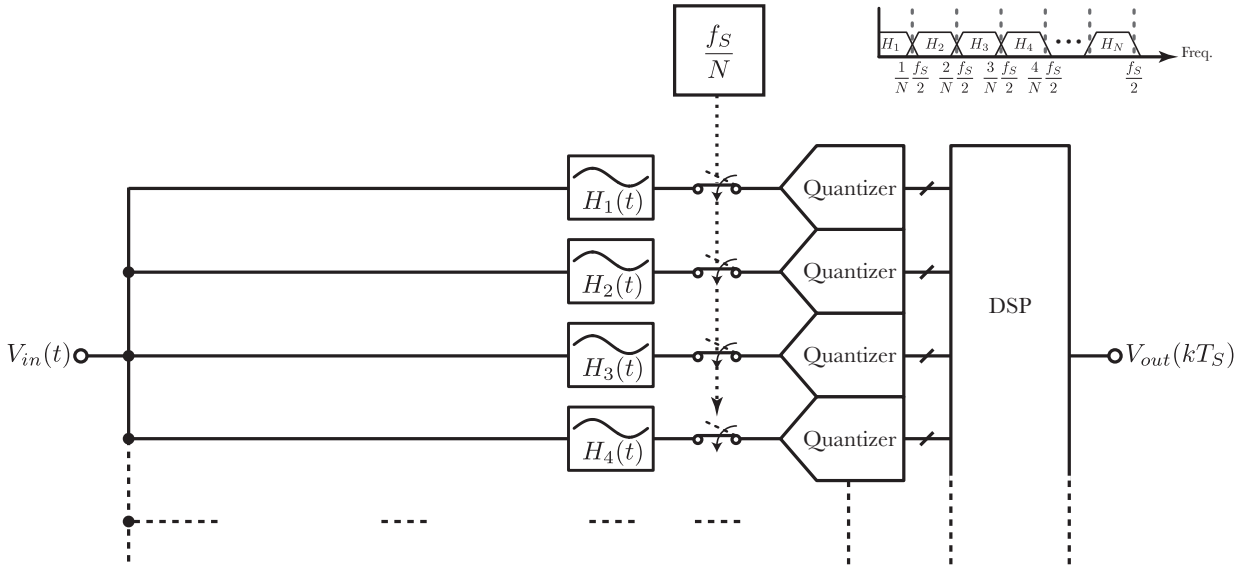


Figure 3.5: High-speed ADC incorporating hybrid filter banks.

The practical challenge in constructing an HFB is to compensate for the effects of hardware components whose characteristics are imprecise and drift with time and temperature [34]. The filter response can be included in the design of the corresponding quantizer using continuous-time bandpass $\Delta\Sigma$ modulators (CTBPDSM) [35].

Frequency-Translating Hybrid Architecture

Instead of designing separate filters for each channel in HFB, input signal can be first down-converted with a proper LO frequency and then passed to identical low-pass filters (which can be implemented with no inductors). This frequency-translating hybrid architecture [36], also known as frequency channelized [37] or frequency-interleaved ADC [38] is shown in Fig. 3.6.

In this architecture, sub-ADCs are working in the first Nyquist zone. The reduced input bandwidth of the sampler relaxes the required small-signal bandwidth by N and provides higher tolerance to sampling jitter. Discussion on the filter design can be found in [39]. We will discuss in details about this architecture in next chapters.

Frequency-Folded ADC

As is was previously mentioned, proper modulation before filtering can remove the impact of bandwidth reduction. Modulation can be applied to continuous-time signals. Given that identity matrix (continuously extended in the time domain) can satisfy Eq. 3.8, a

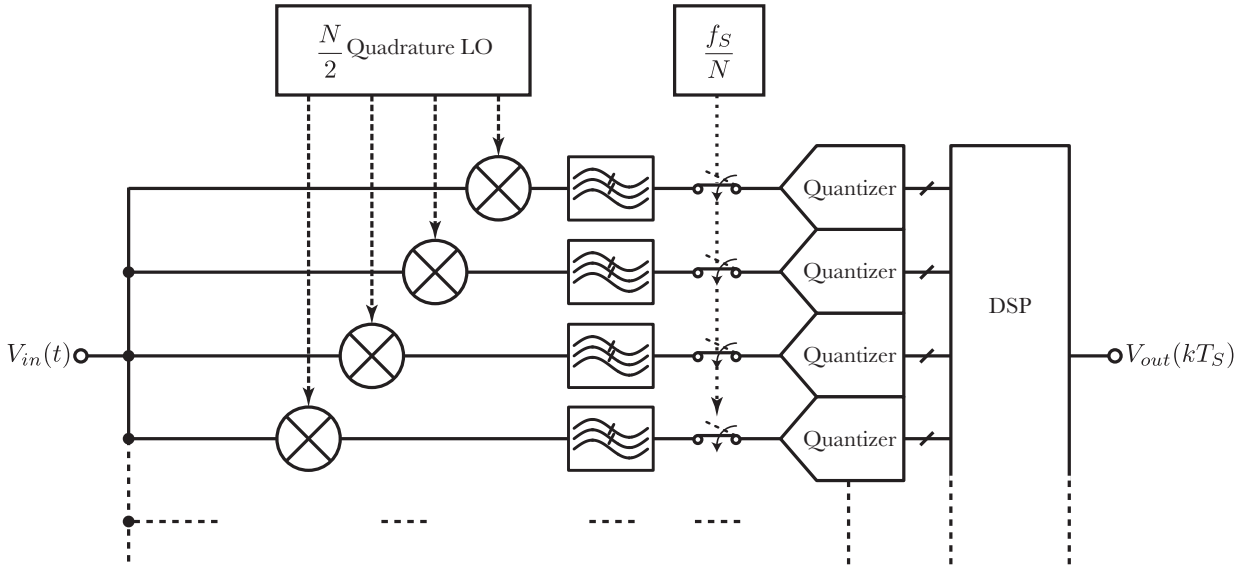


Figure 3.6: Frequency-translating hybrid architecture.

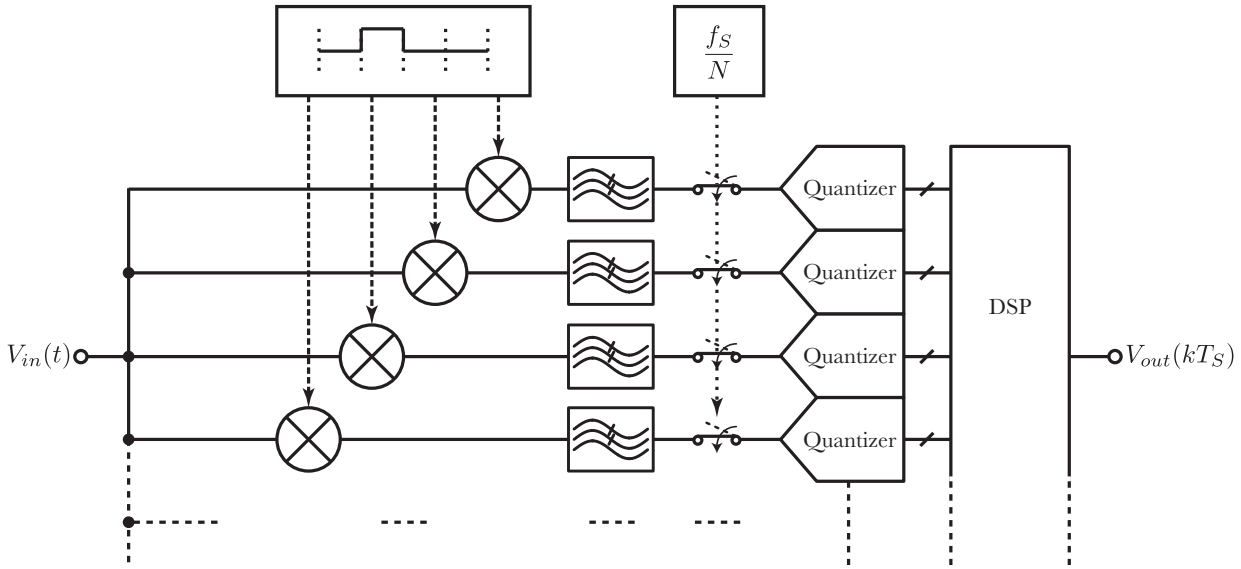


Figure 3.7: Architecture of a frequency-folded ADC.

frequency-folded architecture based on the architecture in Fig. 3.7 can be realized. An interesting advantage of this architecture is that since the full-scale range of the signal before quantization is reduced by N, a gain stage can be used after the filter to increase the total signal power by N. It means that, despite the similarity of this architecture to

time-interleaved ADCs, higher number of channels also result in lower quantization noise. Filter design considerations for this architecture can be found in [40].

3.2 Analog-to-Information Conversion

Nyquist rate sampling guarantees full reconstruction of the original signal without taking into account any heuristic or a priori side information about the signal or its information content other than the physical bandwidth [10]. However, a priori information such as sparsity in any domain can be used to reduce the sampling rate well below the physical bandwidth. Therefore, analog-to-information converters (AIC) are proposed in which the input signal is first pre-processed in the analog domain (which is still running at Nyquist rate or higher). For example, an audio signal ($20KHz$) modulated on an RF carrier ($2GHz$) is sparse in its bandwidth ($2.000002GHz$). Analog pre-processing (down-conversion of the RF signal) can relax the Nyquist rate by 5 orders of magnitude while the audio signal is perfectly reconstructed. Sparsity of the incoming signal[6] is the key and as it gets less sparse, the required sample rate gets closer to the Nyquist rate [41].

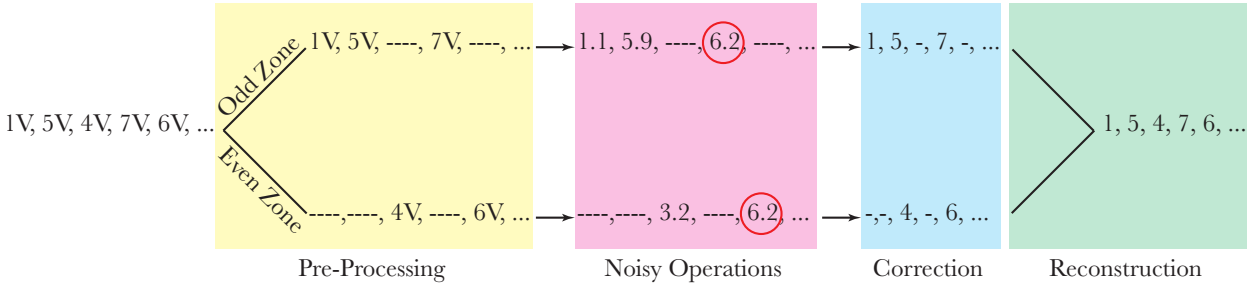


Figure 3.8: Pre-processing at the absence of a priori knowledge.

What happens at the absence of a priori knowledge? Does analog pre-processing still help? Consider the scheme in Fig. 3.8 in which the random analog input voltage generated by a DAC is divided into two zones of odd and even. After pre-processing, each sequence has a higher error margin for any additive noise. Note that at the absence of the pre-processing, 6.2 could be either 6 or 7, however, there is no ambiguity in this scheme. Therefore, the answer is affirmative, and analog pre-processing can still benefit the system if stages later on add considerable noise.

In fact, all of the modulation techniques mentioned in section 3.1 can be considered as special cases of analog to information converters where there is no enhancement due to the input signal sparsity, but design relaxation and noise reduction is achieved through the means of analog pre-processing. When sparsity is provided, same techniques can be combined with compressive sensing algorithms [42].

[6]Here in the frequency domain.

Although it has been shown that jitter and other clock nonidealities impact AIC performance [43], as it will be shown in the following chapters, the system as a whole can potentially outperform conventional ADCs.

3.3 Performing Modulations

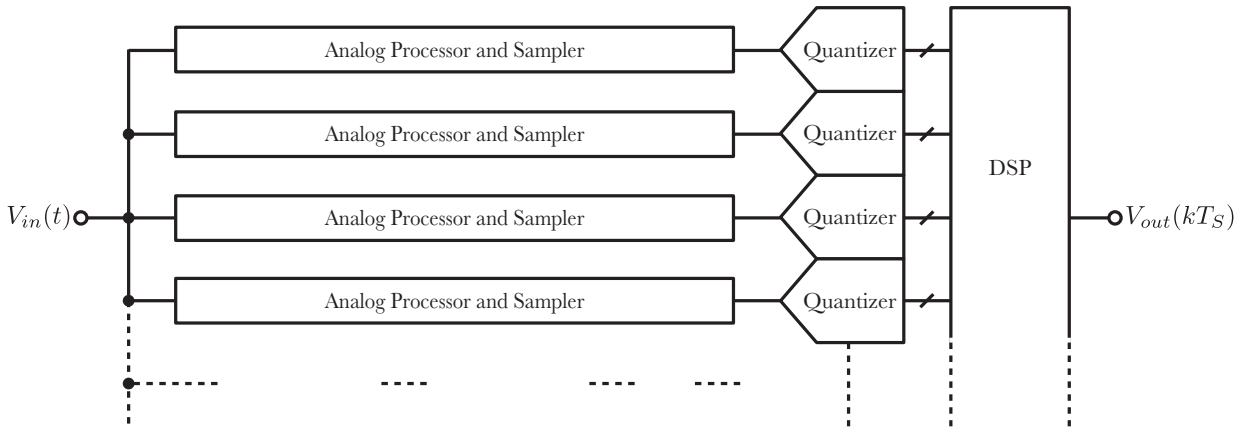


Figure 3.9: Processing all channels in parallel.

Modulation techniques can be immediately applied to the input signal, or the scheme is first dissected into several parts and then sequentially performed on the input signal. Up to here, we assumed that the input signal is directly fed into all of modulators simultaneously as shown in Fig. 3.9. However, it is also possible to dissect the modulation scheme into several parts and perform them sequentially. For example, a balanced[7] tree, as in Fig. 3.10, can be utilized to avoid generating multiple LOs on chip [44]. Also, QMF architecture was originally implemented with a balanced tree structure [45]. From the circuit point of view, having a balanced tree makes the whole system less prone to systematic mismatch between channels. However, the circuit mismatch reduction may introduce other issues. For example, [46] proposes to use an unbalanced tree structure, as depicted in Fig. 3.11, to reduce the error due to the finite harmonic rejection and I/Q imbalance of quadrature mixers.

3.4 Spatio-Temporal Stretching

Another way of dealing with fast signals is to stretch them. Stretching can be done in one domain (e.g. time, space, ...) or a combination of them. Here we will discuss about a few techniques from the literature.

[7]Balanced in terms of the circuitry that the signal has to go thorough before it gets sampled.

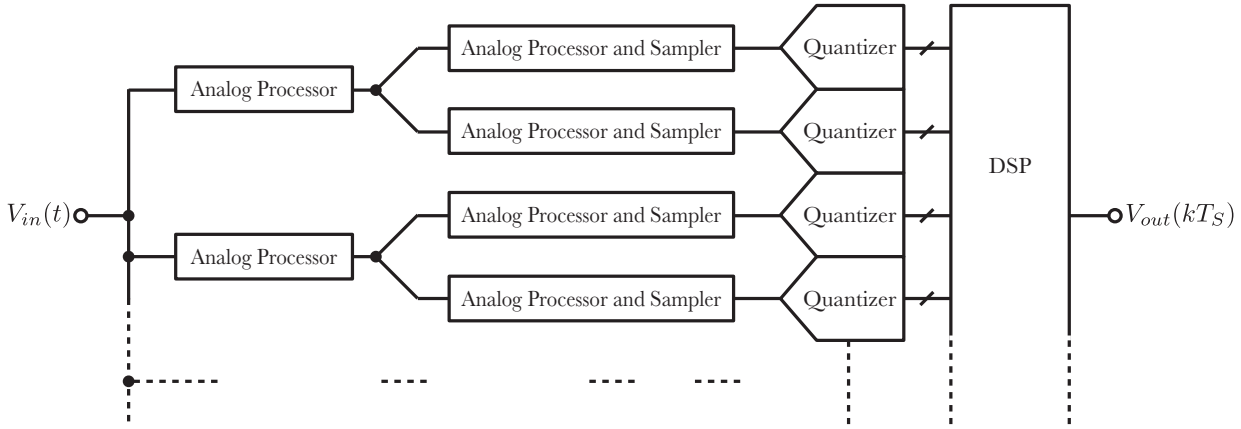


Figure 3.10: Sequentially processing all channels in a balanced tree.

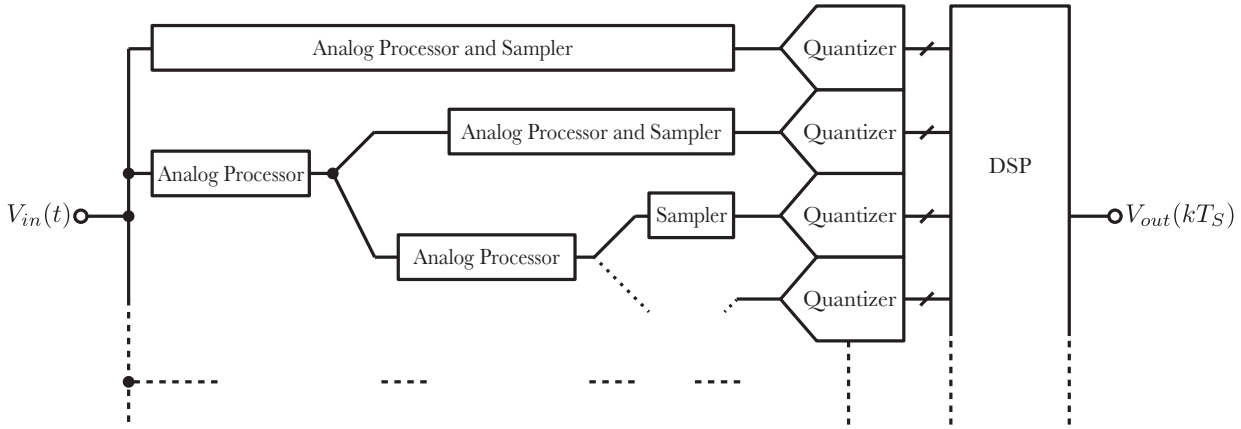


Figure 3.11: Processing channels in an unbalanced tree.

Spatial-Stretching

The key observation here is that a set of parallel quantizers are located separately in space. Therefore, the delay between the travel time of the clock signal and the input signal through the chip and to the input of samplers has be carefully considered and any mismatches should be compensated [47]. However,the mismatch between the travel time can be exploited as a new degree of freedom to relax the system requirements.

For example, consider the architecture in Fig. 3.12 where travel time of the input signal is explicitly increased by extended length of transmission lines. It works like a time-interleaved ADC, but with single clock shared among all ADCs. Similar idea was proposed by [13], however, the spacial stretching does not need to be always implemented artificially. For example, the traveling nature of electromagnetic waves in air can be used, as shown in

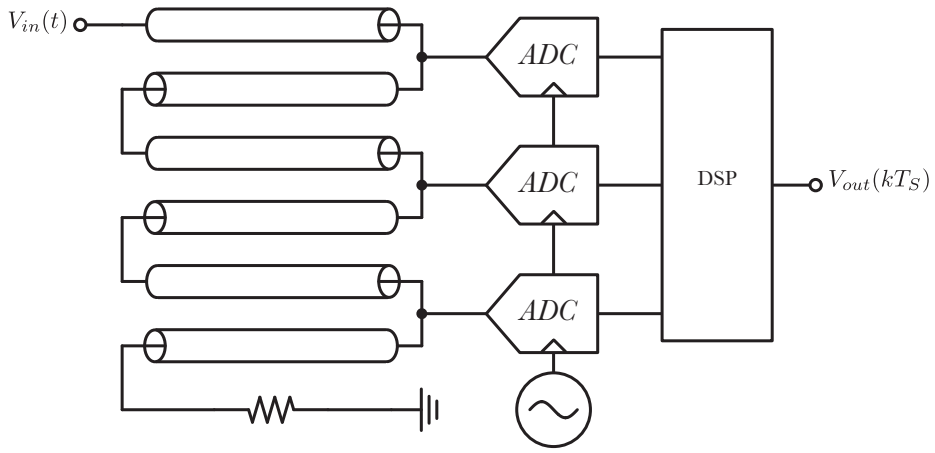


Figure 3.12: Spatial stretching using extended transmission line.

Fig. 3.13 [14]. It should be noted that despite relaxed quantization time, the sampler at each ADC still has to cover the whole bandwidth of the input signal, unless modulation techniques are used before samplers.

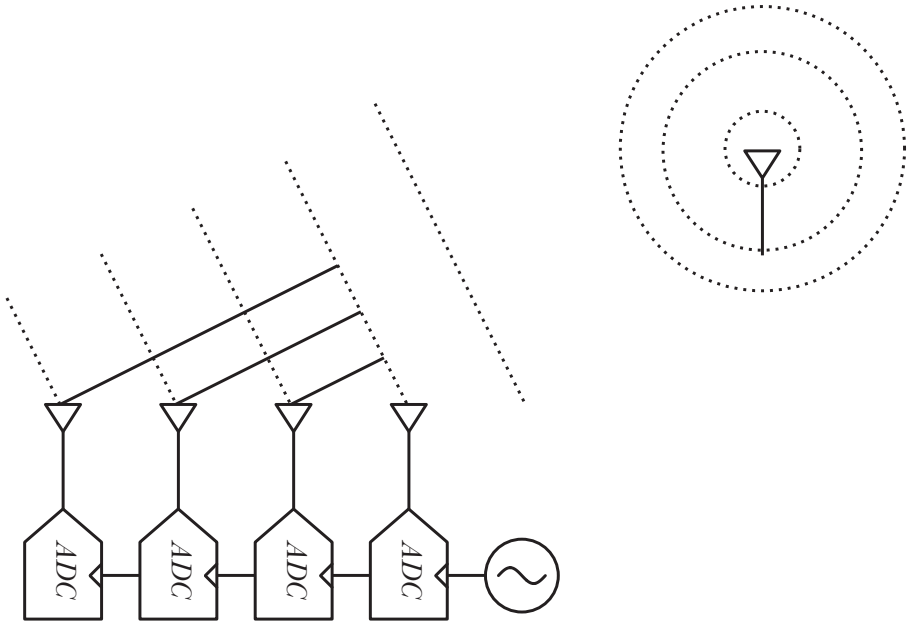


Figure 3.13: Spatial stretching using antenna array.

Time-stretching

Without lose of generality, if we could stretch the signal in time *before* the sampler, not only is the quantization time relaxed, but also the sampling stage would have relaxed timing-related specifications such as small signal bandwidth or rms jitter.

Stretching *before* the sampling stage is the key here, otherwise the sampler still has to support the whole input bandwidth and the sampling circuity will become the bottleneck [23] eventually. For example, time-interleaving stretches the already-taken samples for the following quantizer. Similarly, in a time-to-digital converter, the processor has more time to quantize the time-domain representative of the input signal after it is generated.

Despite the promising benefits of the time-stretching approach, a direct time-manipulation seems impossible[8]. However, the delay it takes for the input signal to pass through a "time-stretching block" can be modulated over time. It has to be noted that although dispersion can smooth a sharp transition, it is not considered as time-stretching since the mechanism of smoothing the signal is just distorting the frequency components. Now, Let us assume that we have designed a block such that

$$V_{out}(t) = V_{in}(t - \tau(t)) \tag{3.9}$$

where τ is the delay between input and output and is a function of time. If we take the time derivative of both sides, we get

$$\frac{\mathrm{d}V_{out}(t)}{\mathrm{d}t} = \left.\frac{\mathrm{d}V_{in}(t')}{\mathrm{d}t'}\right|_{t'=t-\tau(t)} \left(1 - \frac{\mathrm{d}\tau(t)}{\mathrm{d}t}\right) \tag{3.10}$$

This shows that rate of changes at the output will be smaller than the rate of changes at the input by the stretch factor S of:

$$S = \frac{1}{1 - \frac{\mathrm{d}\tau(t)}{\mathrm{d}t}} \tag{3.11}$$

Now, let us consider the all-pass filter in Fig. 3.14. Assuming a limited rate of changes for $R(t)$ such that $\frac{\mathrm{d}R(t)C}{\mathrm{d}t} \ll 1$, the output phase as a function of frequency can be written as

$$\Phi_{out}(\omega, t) = -2 \arctan\left(\omega R(t) C\right) \tag{3.12}$$

Calculating the group-delay as $\tau_g(\omega, t) = -\frac{\mathrm{d}\Phi_{out}(\omega,t)}{\mathrm{d}\omega}$, we get

$$\tau_g(\omega, t) = \frac{2R(t)C}{1 + (\omega R(t) C)^2} \tag{3.13}$$

[8] Assuming no relativistic velocities or Doppler shift!

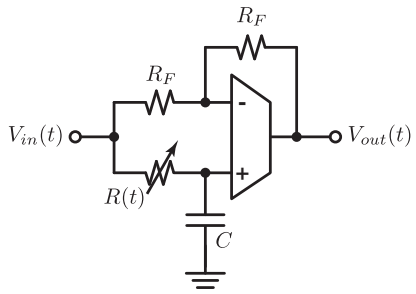


Figure 3.14: Time-varying all-pass filter.

and therefore, the rate of changes in the group delay is

$$\frac{\mathrm{d}\tau_g(\omega,t)}{\mathrm{d}t} = 2\left[\frac{1-(\omega R(t)C)^2}{(1+(\omega R(t)C)^2)^2}\right]\frac{\mathrm{d}R(t)C}{\mathrm{d}t} \tag{3.14}$$

The term in the bracket is negligible if $\omega \ll \frac{1}{R(t)C}$. Therefore, the stretching factor is

$$S \approx \frac{1}{1-2\frac{\mathrm{d}R(t)C}{\mathrm{d}t}} \tag{3.15}$$

Time-stretching is confirmed by simulation and Fig. 3.15 shows the results where the time-varying resistor is implemented using an NMOS transistor.

It can be seen that since $R(t)$ has a limited variation range, at some point, it has to be reset. Therefore, some sort of segmentation is required (not shown). Hence, time-stretched ADCs are also referred to as *segment-interleaved ADCs*[48].

The feedback loop here sets the upper limit of the input bandwidth due to the technology limits. In order to avoid the feedback loop, another approach can be taken [49] as shown in Fig. 3.16:

1. Generate a chirped local oscillator[9].
2. Pass the LO signal through a dispersive block.
3. Use the input signal to modulate the envelope of the LO signal.
4. Pass the modulated wave through a multiple a cascade of N dispersive blocks identical to the one used in the second step[10].
5. Use an envelope detector to recover the stretched input signal.

[9]It can be in electrical or optical domain.

[10]Amplification might be used between stages. It is due to the temporal spreading of the energy and also dissipation.

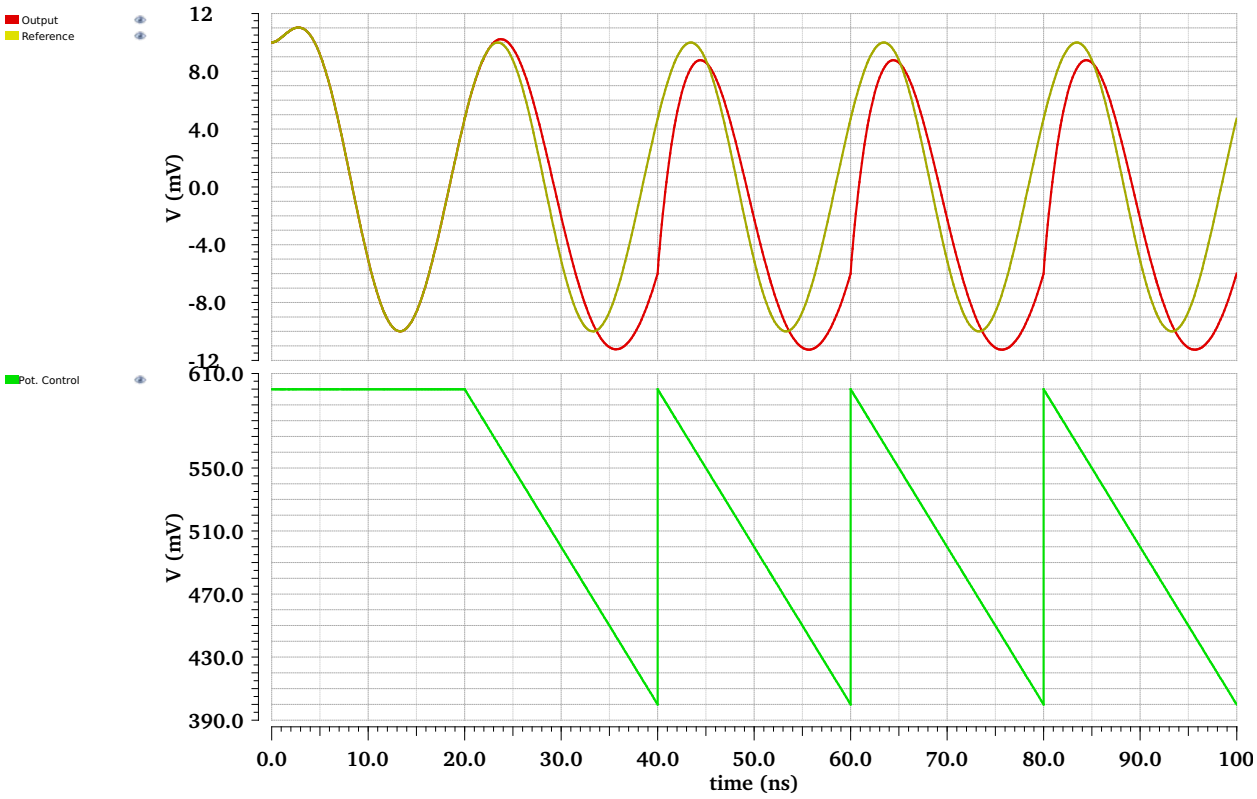


Figure 3.15: Simulation results for time-stretching using time-varying all-pass filter.

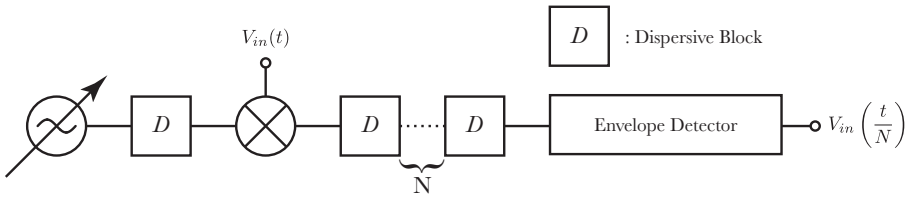


Figure 3.16: Time-stretching with envelope modulation.

It can be shown the stretch factor here is $S = N$. Time-stretching based on the aforementioned procedure has been reported in optical domain [50, 51] where low-jitter optical clocks formed by mode-locked lasers are available[12]. Segmentation can be done using filters that pass only a portion of the oscillator's frequency range, and hence called wavelength-interleaved [52]. Electrical domain implementation of a similar idea is also reported [53, 54].

Chapter 4

Jitter Error

In this chapter, we investigate the impact of non-ideal LO and clock signals. First, we briefly review the basics of jitter and phase noise and their relationship. Then, we explain about what happens when our time reference is not ideal.

4.1 Sampling Error

There are many mechanisms that introduce error to samples of an analog signal from timing perspective which stem from [9]:

1. **The clock signal** driving the sampling stage (assuming ideal sampling circuit) or
2. Non-ideal response of **the sampling circuitry** to the clock signal

or a mixture of both. Let us bring examples for each of them considering an NMOS transistor (as a sampling switch) where its gate is being driven by a clock signal.

- **Jitter Error**: This type of error is coming from the uncertainty on the instance of the analog input which the sampler holds until the next period. The input clock always has phase uncertainty due to different noises added during the generation and distribution. However, even if the clock signal has no phase noise, the sampling circuit itself may cause additional error. For example, the channel response of the transistor switch strongly depends on V_{gs} where the source port has thermal noise. It also depends weakly on V_{sb} where the bulk port may have strong supply-induced noise. The slope of the otherwise-ideal clock signal determines how much those noise sources affect the sampling time.
- **Aperture error:** Since the clock signal has a finite slope, the NMOS transistor does not switch abruptly and the gradual switching adds error to the sample which is not frequency-flat (if modeled as a windowed integration [43]). Moreover, the sampling

switch has dependency on other ports which may make the aperture window tighter or wider.

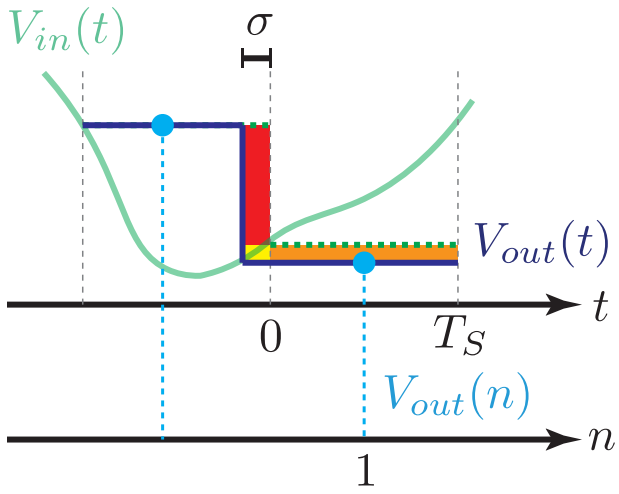


Figure 4.1: Errors due to the clock edge jitter.

In this thesis, we will focus on the jitter error from the clock signal assuming that the clock has a sharp edge to minimize other impacts. Consider Fig. 4.1 where clock edge at $t = 0$ arrives σ earlier. The continuous-time error has three components (colored as yellow, orange, and red) while the discrete-time error is only sensitive to the final value (colored as orange). The discrete-time error ($E_{DT}(n)$: colored as orange) can be approximated as:

$$E_{DT}(n) = -\sigma(n)\frac{\mathrm{d}V_{in}(t)}{\mathrm{d}t}\bigg|_{t=nT_s} \tag{4.1}$$

Discrete-time error persists for T_S in the continuous-time domain. As long as $\sigma \ll T_S$, we can ignore the error area colored as yellow. Moreover, with the same assumption, we can model the red error area as an impulse with the same area. Therefore, continuous-time-specific error[1] ($E_{CT}(t)$: colored as red) can be written as:

$$E_{CT}(t) = [V_{in}(t) - V_{in}(t - T_S)] \sum_n \sigma(t)\delta(nTs) \tag{4.2}$$

It should be noted that the total error in the continuous-time domain is $E_{CT}(t) + E_{DT}(t)$ where $E_{DT}(t)$ is simply the convolution of $E_{DT}(n)$ and the zero-order hold function.

[1]Meaning that it only shows up in the continuous-time domain.

4.2 Phase Noise and Jitter

Phase Noise vs Jitter

"Phase noise" and "jitter" are terms that are referring to the same issue: the LO generation circuitry and the LO distribution network have noise and other nonidealities which effectively manipulate the output phase (ϕ) of the sinusoidal LO output. "Phase noise" is the (normalized) power of the noise manipulating the output phase and is usually reported in dBc/Hz which refers to the spectral content of the phase noise in the frequency domain ($\mathcal{L}(f)$). If the circuit driven by the LO is only sensitive to zero-crossings (or the clock "edge"), timing uncertainty can be reported with jitter (σ usually reported in ps or fs) which refers to the deviation of the output zero-crossing time from the ideal zero-crossing time. Keep in mind that both ϕ and σ are functions of time implicitly. A popular conversion of phase noise to jitter relies on

$$\begin{aligned} V_{LO}(t) &= \cos(\omega_{LO}t + \phi) \\ &= \cos(\omega_{LO}(t + \sigma)) \end{aligned}$$

and thus[2]

$$\sigma = \frac{\phi}{\omega_{LO}}$$

however, subtleties are ignored in this equation. First, phase noise $\phi(t)$ is defined with the spontaneous variations of LO output ($V_{LO}(t)$). However, jitter $\sigma(t)$ deals with the occurrence of zero-crossings at incorrect time ($V_{LO}(t') = 0$):

$$\begin{aligned} \phi(t) &: V_{LO}(t) = \cos(\omega_{LO}t + \phi(t)) \\ \sigma(t) &: V_{LO}(t - \sigma(t)) = \cos(\omega_{LO}t) \end{aligned}$$

In other words, as depicted in Fig. 4.2, phase noise at each time adds a (phase) error parameter to match the y-axis (voltage) of the ideal LO with the noisy LO while jitter has to look ahead and behind in x-axis (time) to find the (time) error parameter which matches with the zero-crossing. For example, in a sampling system, if the phase error at the nominal sampling time is $\sigma(kT_S)$, at $t = kT_S - \sigma(kT_S)$ we have

$$t + \sigma(t)|_{t=kT_S-\sigma(kT_S)} = kT_S - \sigma(kT_S) + \sigma(kT_S - \sigma(kT_S)) \neq 0$$

since $\sigma(kT_S) \neq \sigma(kT_S - \sigma(kT_S))$ (specially at the presence of noise with high-frequency content). However, if $\sigma(kT_S) \approx \sigma(kT_S - \sigma(kT_S))$, the earlier approximation is very close to the simulation results. While the conversion of phase noise to jitter at the absence of high frequency noise is just a matter of finding the right slope[3], it is not easy to do the conversion

[2]Later we show that this equation is not precise.

[3]Even with this simplified case, the actual slope may not match with the slope of ideal LO.

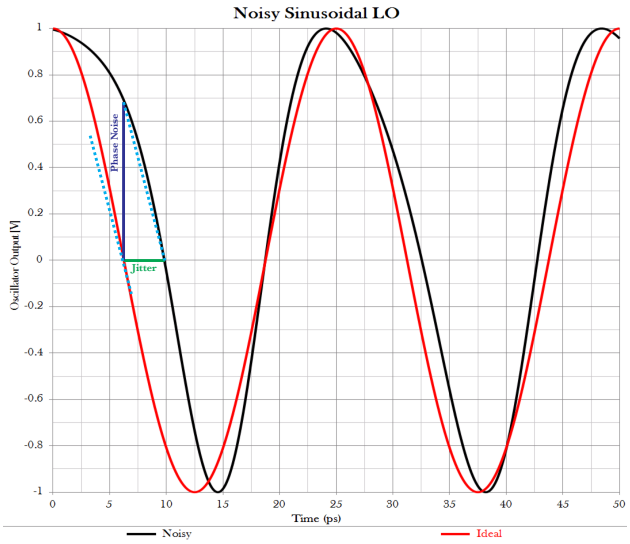


Figure 4.2: Subtleties in the definition of the jitter and phase noise.

at the presence of high-frequency noise. Unfortunately there is no easy way of calculating jitter from phase noise other than the equations provided earlier. Therefore, while we keep in mind that modeling error may exist, we will use aforementioned equations.

There is one more issue with the previous sets of equations which cannot be ignored. Remember that jitter only cares about the "clock edges", and therefore it only considers LO output at specific times. In other words, jitter takes samples of time-error only when zero-crossing occurs. This is not a typical sampling scenario, yet as long time-error is small enough compared to the period of the output signal, it can be approximated as a sampling system. Therefore:

1. Jitter in the frequency domain has be to described inside the bandwidth of $[0, \omega_{LO})$[4] while phase noise is described for the whole frequency range $[0, \infty)$. Phase noise spectral content above ω_{LO} will be folded back into the jitter bandwidth of $[0, \omega_{LO})$.

2. The phase noise to jitter conversion equation is valid only if we consider the rms power[5]

$$\overline{\sigma} = \frac{\overline{\phi}}{\omega_{LO}} \tag{4.3}$$

3. While derivation of jitter from phase noise is possible, it is not possible to do the opposite.

[4] Assuming both rising and falling edges.

[5] Strictly speaking, since jitter only cares about zero-crossings, if for any reason the LO output is more or less noisy around zero-crossings, Eq. 4.3 is not valid. However, we will ignore this case.

Edge-sensitive Circuitry Driven by Noisy LO

In this part, we assume that LO signal is driving edge-sensitive circuitry. Although the LO is sinusoidal, as long as the circuitry driven by the LO is edge sensitive, there will be an inherent LO sharpening which makes the LO signal look like a square wave. As a reminder, the Fourier series of a square wave $\Pi(\omega_{LO}t)$ is:

$$\Pi(\omega_{LO}t) = \frac{4}{\pi}\sum_{n:odd}^{\infty}\frac{1}{n}\sin(n\omega_{LO}t) \tag{4.4}$$

Therefore, if the LO signal has σ jitter, it can be written as:

$$\begin{aligned}\Pi\left(\omega_{LO}\left(t+\sigma\right)\right) &= \frac{4}{\pi}\sum_{n:odd}^{\infty}\frac{1}{n}\sin\left(n\omega_{LO}\left(t+\sigma\right)\right)\\ &\approx \frac{4}{\pi}\sum_{n:odd}^{\infty}\frac{1}{n}\left(\sin(n\omega_{LO}t)+n\omega_{LO}\sigma\cos(n\omega_{LO}t)\right)\\ &\approx \frac{4}{\pi}\sum_{n:odd}^{\infty}\frac{1}{n}\sin(n\omega_{LO}t)+\omega_{LO}\sigma\cos(n\omega_{LO}t)\end{aligned} \tag{4.5}$$

Note that although the power of the first term in the series decreases as the n increases, the power of the second term (which indicates the phase noise) remains constant[6]. As Fig. 4.3 depicts, jitter will be up-converted and repeated over the whole frequency band. Before ending this section, let us consider the situation in which jitter σ is white noise and try to simplify Eq. 4.5. Given that white noise has a uniform spectral density, the double side-band power spectral density is $|\sigma_{DSB}(\omega)|^2 = \frac{{\sigma_{RMS}}^2}{2\omega_{LO}}$. This jitter is multiplied in the time domain by $\omega_{LO}\sum_{n:odd}^{\infty}\cos(n\omega_{LO}t)$ which means a convolution of $\sigma_{DSB}(\omega)$ with $\omega_{LO}\sum_{-\infty}^{\infty}\frac{1}{2}\delta((2n+1)\omega_{LO})$ in the frequency domain. The result of this convolution is

$$\begin{aligned}|\sigma'_{DSB}(\omega)|^2 &= \left|\mathcal{L}\left\{\sigma(t)\times\omega_{LO}\sum_{n:odd}^{\infty}\cos(n\omega_{LO}t)\right\}\right|^2\\ &= \left|\sigma_{DSB}(\omega)*\omega_{LO}\sum_{-\infty}^{\infty}\frac{1}{2}\delta((2n+1)\omega_{LO})\right|^2\\ &= \frac{{\sigma_{RMS}}^2}{2\omega_{LO}}\times\frac{{\omega_{LO}}^2}{2^2}\\ &= \frac{\omega_{LO}{\sigma_{RMS}}^2}{8}\end{aligned} \tag{4.6}$$

[6]It may seem like that the noise power approaches infinity if the noise remains constant over the whole bandwidth. However, remember that σ is a discrete function of time and this "mathematical" modeling error occurs since we are mixing discrete-time and continuous-time functions together.

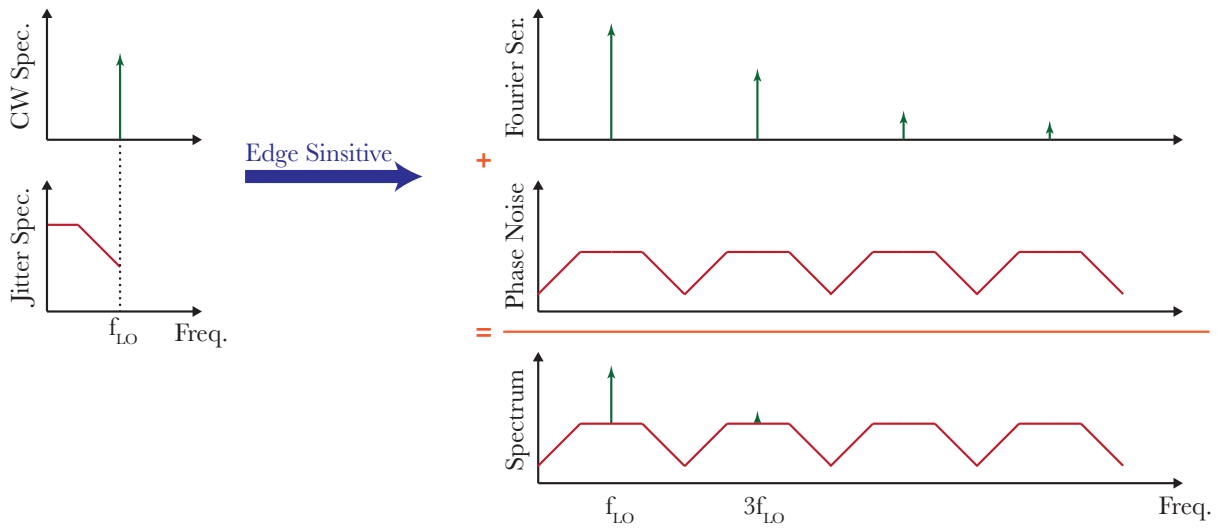


Figure 4.3: Effective spectrum of a noisy LO (with jitter) after passing through an edge-sensitive circuitry.

Therefore, in the case of white jitter, Eq. 4.5 can be written as

$$\begin{aligned}\Pi\left(\omega_{LO}\left(t+\sigma\right)\right) &\approx \frac{4}{\pi}\left(\left[\sum_{n:odd}^{\infty}\frac{1}{n}\sin(n\omega_{LO}t)\right]+\sigma'(t)\right)\\ &\approx \Pi\left(\omega_{LO}t\right)+\frac{4}{\pi}\sigma'(t)\end{aligned} \tag{4.7}$$

where $\sigma'(t)$ has a single side-band power spectral density of

$$\left|\sigma'_{SSB}(\omega)\right|^2 = \frac{\omega_{LO}{\sigma_{RMS}}^2}{4} \tag{4.8}$$

Frequency Division

In this part, we will review the impact of frequency division on the jitter and its spectral content. Such a circuitry effectively divides the phase accumulation of sinusoidal signal:

$$\sin(\phi) \xrightarrow{Freq.\,Div.} \sin\left(\frac{\phi}{DR}\right)$$

where $DR = \frac{\omega_{LO}}{\omega_{Div}}$ stands for "Division Ratio". If we substitute $\phi = \omega_{LO}(t+\sigma)$, we have:

$$\sin(\omega_{LO}(t+\sigma)) \xrightarrow{Freq.\,Div.} \sin\left(\frac{\omega_{LO}}{DR}(t+\sigma)\right) = \sin(\omega_{Div}(t+\sigma))$$

Therefore, after frequency division, **rms of jitter** remains almost the same[7]. Could we say that the jitter of the LO signal is the same as the frequency-divided signal[8]? It depends on the application and modeling precision needed. Remember that the jitter of an oscillator with angular frequency of ω_{osc} is a discrete function of time with a bandwidth of $[0, \omega_{osc})$. After division, the new jitter is a sampled version of the undivided-LO jitter in the time domain and thus, in the frequency domain, aliasing happens and the divided-LO's jitter spectrum looks completely different. In order to simplify the aliasing analysis, we assume that the LO jitter has two separate contributors:

1. "Close-in" phase noise concentrated at frequency below the divided frequency $[0, \omega_{Div})$.
2. "Far-out" phase noise uniformly distributed in the bandwidth of $[0, \omega_{LO})$ like a white noise.

With these assumptions, the jitter spectral content of the divided LO ($S_{LO,Div}$) will be as following:

- The close-in portion of the jitter is the same as the close-in portion of the LO jitter (S_{LO}) with no aliasing.
- The far-out portion is uniformly distributed in the bandwidth of $[0, \omega_{Div})$ while in the frequency domain, the spectral content is DR times higher due to aliasing. Keep in mind that the total far-out noise power is almost the same since $\omega_{LO} \times S_{LO} = \frac{\omega_{LO}}{DR} \times [DR \times S_{LO}] = \omega_{Div} \times S_{LO,Div}$.

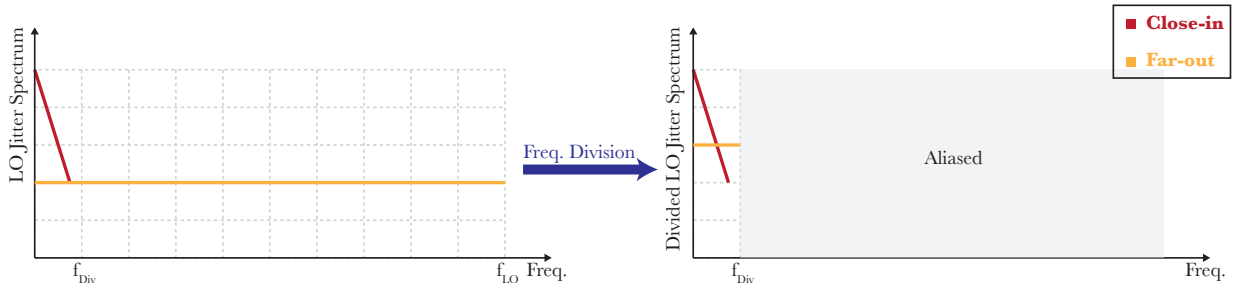


Figure 4.4: Jitter spectrum before and after frequency division.

Fig. 4.4 shows the impact of division on the jitter profile. Now let us mathematically investigate what the phase noise looks like for an edge-sensitive circuitry. Using Eq. 4.5, we

[7]Phase noise power at the harmonics of divided output will vanish.
[8]Assuming ideal noise-less division.

observe that

$$\Pi\left(\omega_{Div}\left(t+\sigma_{Div}\right)\right) \approx \frac{4}{\pi}\sum_{n:odd}^{\infty}\frac{1}{n}\sin(n\omega_{Div}t)+\omega_{Div}\sigma_{Div}\cos(n\omega_{Div}t) \tag{4.9}$$

the effective power of each noise term is DR^2 times lower. Therefore,

- The close-in content of the LO jitter will repeatedly appear at the phase noise spectrum every $2\omega_{Div}$ with a DR^2 lower spectral power level.
- The far-out content of the LO jitter will uniformly appear all over the frequency range $[0, \infty)$ with a DR lower spectral power level.

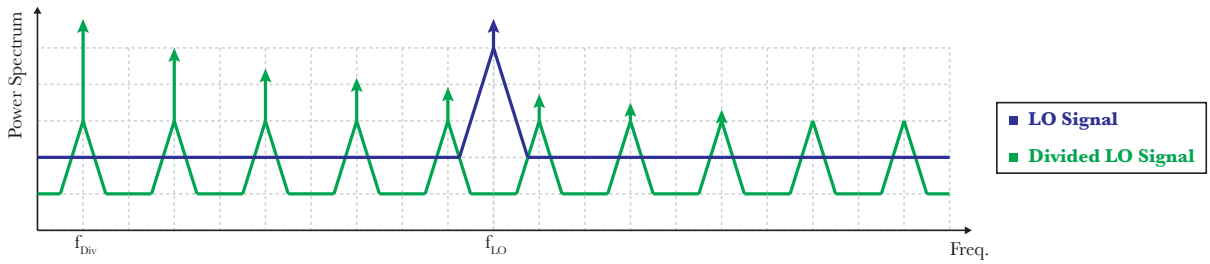


Figure 4.5: Effective LO spectrum for an edge-sensitive circuitry before and after frequency division.

Fig. 4.5 summarizes what the LO signal looks like for an edge-sensitive block after frequency division. Also, simulation results (Fig. 4.6) confirms the theory provided here.

4.3 Phase Noise Sources

In this section, we will briefly discuss about the origin of the jitter error. Fig. 4.7 shows a simplified architecture with focus on the LO generation and distribution. Different contributors are:

- Off-chip time reference is usually modeled to have a white phase noise.
- The PLL usually has a bandwidth much smaller than the reference frequency and therefore, the close-in phase noise of the VCO is controlled by the PLL. State-of-the-art locked oscillators have around $50fs \sim 100fs$ of RMS jitter [55] from close-in phase noise.
- Out of the PLL bandwidth, the VCO is the dominant noise source. While a ring oscillator has white far-out phase noise, an LC oscillator's phase noise scales with $\frac{1}{f^2}$.

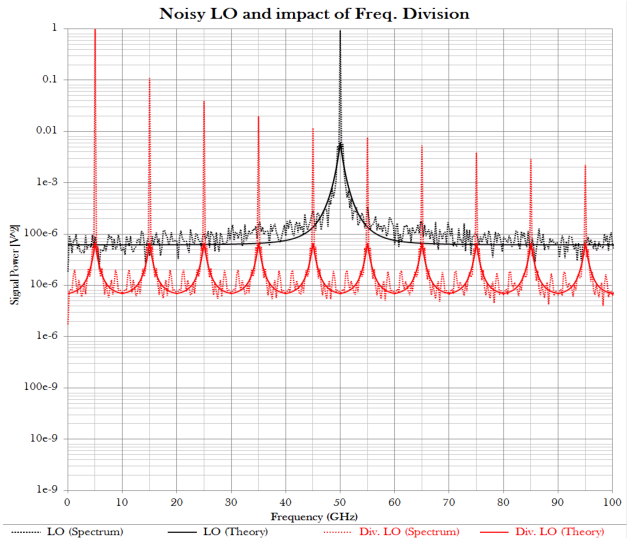


Figure 4.6: Simulation of the effective LO spectrum for an edge-sensitive circuitry before and after frequency division.

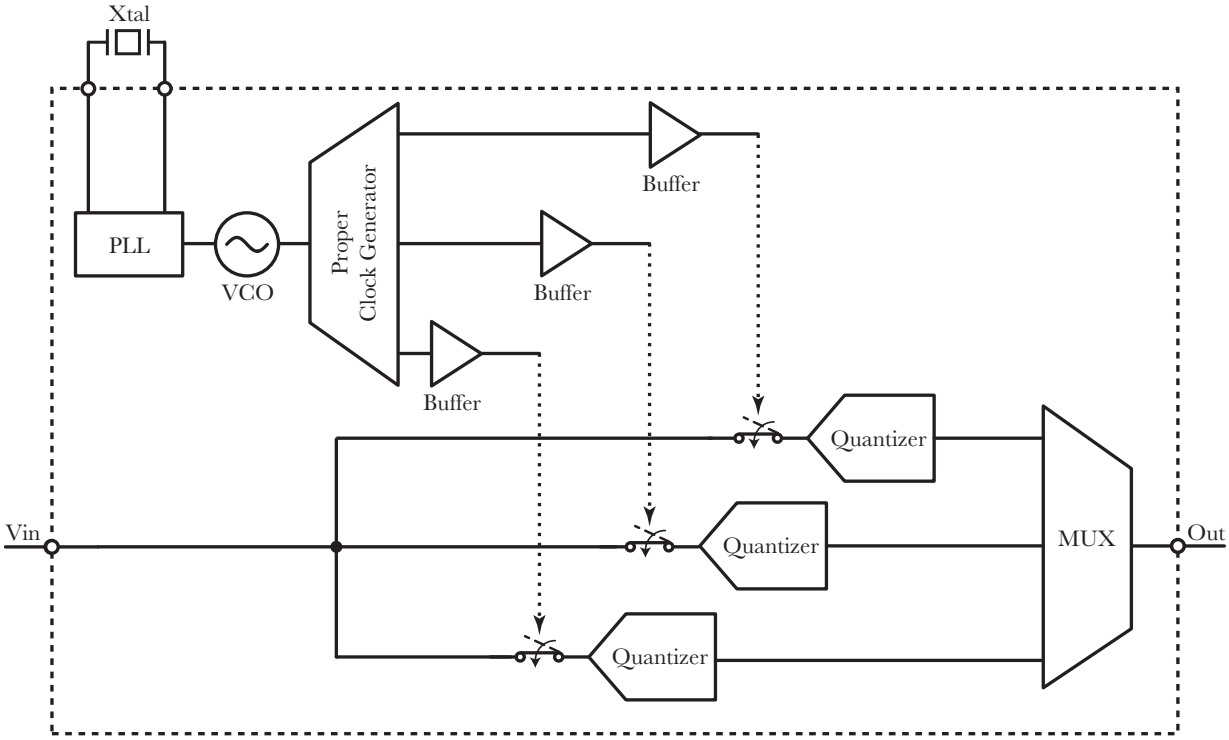


Figure 4.7: Simplified model of LO generation and distribution to the sampling stage.

- Noise added by any blocks after VCO is not controlled by the PLL. Therefore, buffers

and all other circuitry to generate sampling clocks (from the master VCO) has to burn enough power to lower the phase noise. State-of-the-art generation and distribution networks also have around $50fs \sim 100fs$ of RMS jitter [2] from far-out phase noise.

It should be noted that since sharp clock edges are favorable, using LC tuned networks, specially at low sampling rates[9], is not desirable. Therefore, buffers usually contribute to a flat phase noise.

4.4 Principles of Improving Jitter-limited SNR

In this section, we will discuss about the principles of how the SNR can be improved in a system which the noise level is dominated by the sampling jitter. We will show that the system architecture by itself cannot improve jitter-limited SNR unless more "timing units" are used. Keep in mind that a "timing unit" is not always an off-chip crystal oscillator. We can use anything else which has memory effect:

- A notch filter with a specific center frequency.[10].
- Time domain response of a filter.
- Delay of a transmission line[11].
- Multiple oscillators (as long as they are independent with uncorrelated noise).

Mix then Sample

Let us investigate what happens if the input signal is first down-converted and then passed to the ADC.

$$\begin{aligned} V_{in}(t) &= A\cos(\omega_{in}t) \\ V_{LO}(t) &= \cos(\omega_{LO}(t+\sigma)) \\ V_{CLK}(t) &= \cos(\omega_{CLK}(t+\sigma)) \end{aligned}$$

where $V_{in}(t)$ is the ADC input, $V_{LO}(t)$ is the mixer LO, and $V_{CLK}(t)$ is the clock to the sampler, as illustrated in Fig. 4.8. Assuming that the lower side-band is the desired one after the mixer, at the input of the sampler ($V_S(t)$) we have:

$$\begin{aligned} V_S(t) &= A\cos(\omega_{in}t - \omega_{LO}(t+\sigma)) \\ &= A\cos((\omega_{in}-\omega_{LO})t - \omega_{LO}\sigma) \end{aligned}$$

[9]Remember that even high sampling rate ADCs usually have time-interleaved channels were sampling of each channel does not exceed a few gigahertz.

[10]The most famous on-chip time reference, the LC circuit, is a notch filter.

[11]In general, any physical routing.

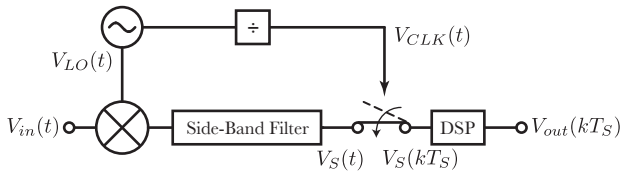


Figure 4.8: Mixer-assisted sampler with only one time reference

Now $V_S(t)$ should be sampled by the zero-crossing of $V_{CLK}(t)$. Keep in mind that if V_{CLK} is σ seconds ahead of time, sampling happens σ seconds earlier which means that the sample belongs to $kT_S - \sigma$.

$$\begin{aligned} V_S(kT_S) &= A\cos((\omega_{in} - \omega_{LO})(kT_S - \sigma) - \omega_{LO}\sigma) \\ &= A\cos((\omega_{in} - \omega_{LO})kT_S - (\omega_{in} - \omega_{LO})\sigma - \omega_{LO}\sigma) \\ &= A\cos((\omega_{in} - \omega_{LO})kT_S - \omega_{in}\sigma) \end{aligned}$$

When the output is digitally up-converted, we end up with

$$\begin{aligned} V_{out}(kT_S) &= A\cos(\omega_{in}kT_S - \omega_{in}\sigma) \\ &= A\cos(\omega_{in}(kT_S - \sigma)) \end{aligned}$$

which is the same as Eq. 2.5 and the same SNR is be expected. It should have been obvious from the beginning that if you have one and only one (time) reference which is used to conduct any type of measurement, **the accuracy of the result will not be better than the accuracy of the reference in a memory-less system**.

Now, let us quickly do the same math again, but this time, we will take the delay of the frequency divider t_d into account and define $\sigma_d(t) = \sigma(t - t_d)$. Therefore, we have

$$\begin{aligned} V_{in}(t) &= A\cos(\omega_{in}t) \\ V_{LO}(t) &= \cos(\omega_{LO}(t + \sigma)) \\ V_{CLK}(t) &= \cos(\omega_{CLK}(t + \sigma_d)) \end{aligned}$$

$$\begin{aligned} V_S(t) &= A\cos(\omega_{in}t - \omega_{LO}(t + \sigma)) \\ &= A\cos((\omega_{in} - \omega_{LO})t - \omega_{LO}\sigma) \end{aligned}$$

$$\begin{aligned} V_S(kT_S) &= A\cos((\omega_{in} - \omega_{LO})(kT_S - \sigma_d) - \omega_{LO}\sigma) \\ &= A\cos((\omega_{in} - \omega_{LO})kT_S - (\omega_{in} - \omega_{LO})\sigma_d - \omega_{LO}\sigma) \end{aligned}$$

$$\begin{aligned} V_{out}(kT_S) &= A\cos(\omega_{in}kT_S - (\omega_{in} - \omega_{LO})\sigma_d - \omega_{LO}\sigma) \\ &\approx A\cos(\omega_{in}kT_S) + [(\omega_{in} - \omega_{LO})\sigma_d + \omega_{LO}\sigma]\, A\sin(\omega_{in}kT_S) \end{aligned}$$

Note that here we have two noise terms (σ and σ_d) which are summed up with different weighs. It will be easier to conduct the calculations in the frequency domain noting that $\mathcal{F}\{\sigma_d\} = \mathcal{F}\{\sigma\}e^{-t_d s}$:

$$\mathcal{F}\{(\omega_{in} - \omega_{LO})\sigma_d + \omega_{LO}\sigma\} = \left[(\omega_{in} - \omega_{LO})e^{-t_d s} + \omega_{LO}\right]\mathcal{F}\{\sigma\} \tag{4.10}$$

Noise power can be calculated by integrating the spectral density over the whole output frequency range:

$$P_N = \int_0^{\omega_{NBW}} \left[(\omega_{in} - \omega_{LO})e^{-t_d s} + \omega_{LO}\right]^2 \mathcal{F}\{\sigma\}^2 d\omega \tag{4.11}$$

where ω_{NBW} is the frequency range of phase noise. The above equation is complicated and does not give us any intuition about what we should expect. We will simplify the above equation for two cases:

1. if $\sigma(t)$ is slow-changing with power concentrated at low frequencies: then we can assume that for the most range of frequencies in which $\mathcal{F}\{\sigma\}^2$ is non-zero, $t_d \ll \frac{1}{s}$ and $e^{-t_d s} \approx 1$ and thus:

$$\begin{aligned} P_N &\approx \int_0^{\omega_{NBW}} \left[(\omega_{in} - \omega_{LO}) \times 1 + \omega_{LO}\right]^2 \mathcal{F}\{\sigma\}^2 d\omega \\ &\approx \int_0^{\omega_{NBW}} \omega_{in}^2 \mathcal{F}\{\sigma\}^2 d\omega \\ &\approx \omega_{in}^2 \int_0^{\omega_{NBW}} \mathcal{F}\{\sigma\}^2 d\omega \\ &\approx \omega_{in}^2 {\sigma_{RMS}}^2 \end{aligned} \tag{4.12}$$

   In other words, if the delay is small compared to pace of phase changes, delay of t_d can be ignored which intuitively make sense. SNR will be the same as in the Eq. 2.8.

2. if $\sigma(t)$ is a random white noise: then σ and σ_d have the same spectral density of $\mathcal{F}\{\sigma\}^2 = \frac{{\sigma_{RMS}}^2}{\omega_{NBW}}$. Let us provide a simplified approximation in the time domain and then use the frequency domain representation to prove the result.
   For a random white noise of $\sigma(t)$, we know that the auto-correlation is 1 for no delay and 0 otherwise. If we assume that σ and σ_d are approximately uncorrelated with the same RMS value, the output SNR of this approximation SNR_{Approx} is:

$$SNR_{Approx} = \frac{1}{((\omega_{in} - \omega_{LO})\sigma_{RMS})^2 + (\omega_{LO}\sigma_{RMS})^2} \tag{4.13}$$

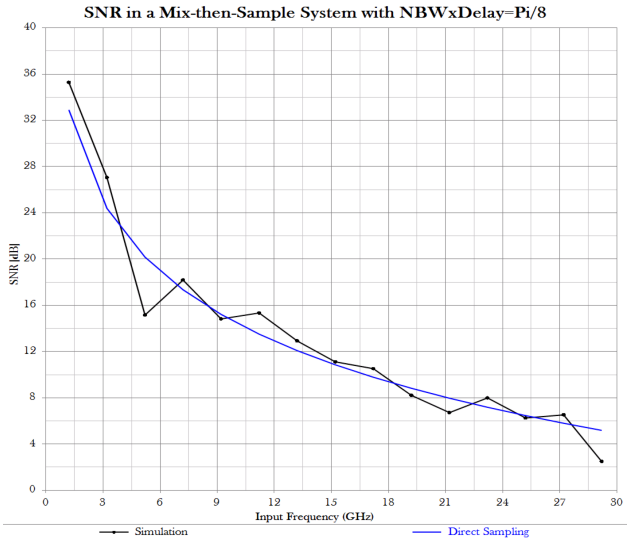


Figure 4.9: SNR of a Mix-then-Sample system with phase noise dominated by close-in part

We can also use the frequency domain to get an accurate theory[12].

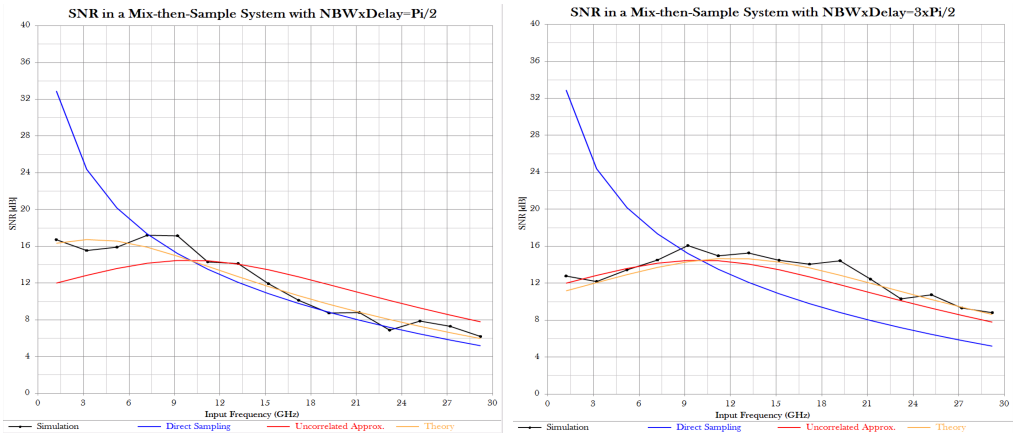
$$\begin{aligned} P_N &\approx \int_0^{\omega_{NBW}} \left[(\omega_{in}-\omega_{LO})e^{-t_d s}+\omega_{LO}\right]^2 \mathcal{F}\{\sigma\}^2 d\omega \\ &\approx \frac{{\sigma_{RMS}}^2}{\omega_{NBW}} \int_0^{\omega_{NBW}} \left[(\omega_{in}-\omega_{LO})e^{-t_d s}+\omega_{LO}\right]^2 d\omega \\ &\approx {\sigma_{RMS}}^2 \left[(\omega_{in}-\omega_{LO})^2+{\omega_{LO}}^2+\frac{2\omega_{LO}(\omega_{in}-\omega_{LO})\sin(t_d\omega_{NBW})}{t_d\omega_{NBW}}\right] \end{aligned} \tag{4.14}$$

It should be obvious that as $t_d > \frac{1}{\omega_{NBW}}$, the uncorrelated approximation gets close to the theory. It should be mentioned that in a real system, side-band filter usually has much higher delay than a frequency divider[13] and also serves as an anti-aliasing filter before the sampling stage. This filter can be either one moderate-order filter or a cascade of low-order filters. In both cases, (group) delay is comparable with the inverse of the corner frequency $\frac{1}{\omega_{Pass}}$ and therefore, the uncorrelated approximation can be used to expedite SNR estimation when we are dealing with wide-band white-noise.

To conclude this section, we want to emphasize that all "time-parameters" should be considered in calculations otherwise, no SNR improvement will be achieved.

[12]Please refer to section 4.2 for a discussion on the modeling limits.

[13]In our previous calculations, we can consider a negative t_d to match with this case.

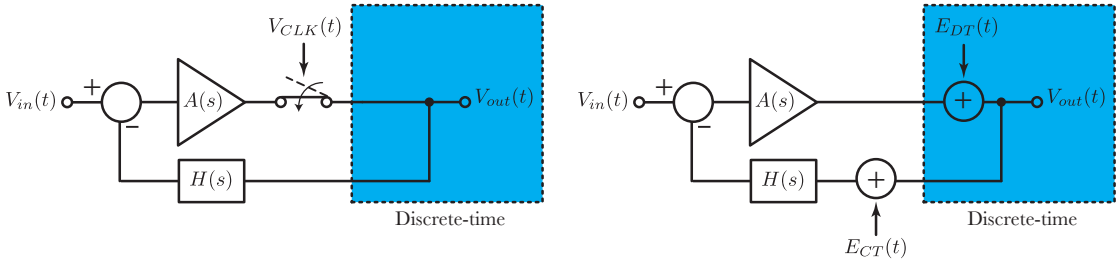


(a) Small delay ($t_d\omega_{NBW} = \frac{\pi}{4}$) (b) Large delay ($t_d\omega_{NBW} = \frac{3\pi}{4}$)

Figure 4.10: SNR of a Mix-then-Sample system with white phase noise

Hybrid Feedback Loop

In this part, we will examine the effect of a feedback loop on reducing the jitter-induced noise. Consider Fig. 4.11a where samples are fed back to be compared with the input signal. Such a hybrid loop has been used in the context of PLLs and continuous-time $\Delta\Sigma$ modulators. Due to the stability issues, the loop bandwidth should be much smaller than the sampling rate such that generated harmonics at the sampling stage is heavily attenuated before feeding back to the input.



(a) Loop architecture. (b) Noise model.

Figure 4.11: Hybrid feedback loop.

Assuming that sample rate is high enough such that harmonics can be ignored, the noise model of Fig. 4.11b can be used where $E_{CT}(t)$ and $E_{DT}(t)$ are defined in section 4.1. Note that the blue shaded area in this figure contains only the signals relevant to discrete samples. However, since the feedback is in the continuous-time domain, the continuous-time-specific error is added later on. With the assumption of high sampling rate, we can derive the

Laplace-domain representation of the errors as

$$\begin{aligned} E_{DT}(s) &= \left[-\left[sV_{in}(s)\right] * \sigma(s)\right] ZOH(s) \\ &= -\left[\left[sV_{in}(s)\right] * \sigma(s)\right] \frac{1-\mathrm{e}^{-sT_S}}{s} \\ &\approx -T_S \left[sV_{in}(s)\right] * \sigma(s) \end{aligned} \tag{4.15}$$

where $ZOH(s)$ is the zero-order hold function and

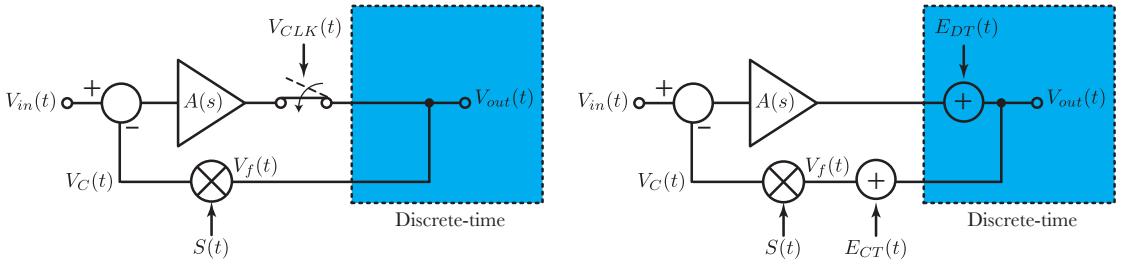
$$\begin{aligned} E_{CT}(s) &= \left[V_{in}(s)(1-\mathrm{e}^{-sT_S})\right] * \sigma(s) \\ &\approx T_S \left[sV_{in}(s)\right] * \sigma(s) \end{aligned} \tag{4.16}$$

$E_{DT}(s) + E_{CT}(s) \approx 0$ is fed-back in the loop, which means that the hybrid feedback loop cannot correct the error. Keep in mind that the transfer of the two noise sources are different from each other:

$$TF_{E_{DT}} = \frac{1}{1 + A(s)H(s)} \tag{4.17}$$

$$TF_{E_{CT}} = \frac{-A(s)H(s)}{1 + A(s)H(s)} \tag{4.18}$$

Since $E_{DT}(t)$ and $E_{CT}(t)$ are still very much distinguishable in small time scales, high-speed signal processing before feedback might be helpful. Consider Fig. 4.12a where the output is shaped by function $S(t)$ and then fed back to the loop. Keep in mind that, although the loop bandwidth should be much smaller than the sampling rate for the stability, $S(t)$ can be very fast to differentiate between $E_{DT}(t)$ and $E_{CT}(t)$.



(a) Loop architecture. (b) Noise model.

Figure 4.12: Hybrid feedback loop with noise shaping.

In an ideal situation, the signal which is compared with the input is

$$V_C(t) = V_f(t)S(t) \tag{4.19}$$

Due to jitter on the sampling stage and also on the noise shaping stage, $V_C(t)$ will deviate from the ideal case, and the difference is

$$\begin{aligned}\Delta V_C(t) &= \Delta(V_f(t)S(t)) \\ &= S(t)\Delta V_f(t) + V_f(t)\Delta S(t) \\ &= S(t)(E_{DT}(t) + E_{CT}(t)) + V_f(t)\Delta S(t)\end{aligned} \tag{4.20}$$

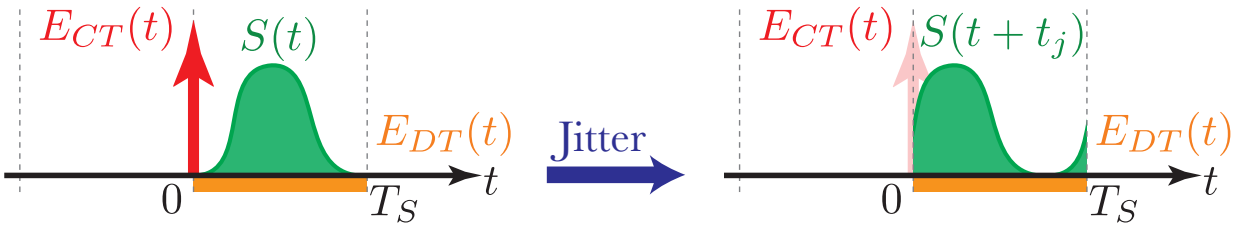


Figure 4.13: Noise Shaping in a hybrid feedback loop.

If the shaping function is chosen such that $S(nT_S) \approx 0$, for example $S(t) = 1 - \cos(\omega_S t)$ as shown in Fig. 4.13, $E_{CT}(t)$ can be completely removed by $S(t)$[14]. Under this assumption

$$\Delta V_C(t) \approx S(t)E_{DT}(t) + V_f(t)\Delta S(t) \tag{4.21}$$

Since the loop bandwidth is small, it filters out the high frequency components of the $S(t)$, which means that $E_{DT}(t)$ will be multiplied by the DC value of the shaping function and then passed through the transfer function we calculated in Eq. 4.17.

So far, we effectively removed the impact of $E_{CT}(t)$ and attenuated the impact of $E_{DT}(t)$ by the feedback loop. However, the analysis is not done until we determine the impact of the jitter of noise shaping function from $V_f(t)\Delta S(t)$. The noisy output $V_C(t)$ only due to the jitter of shaping function is

$$V_C(t) = V_f(t)S(t+\sigma) \tag{4.22}$$

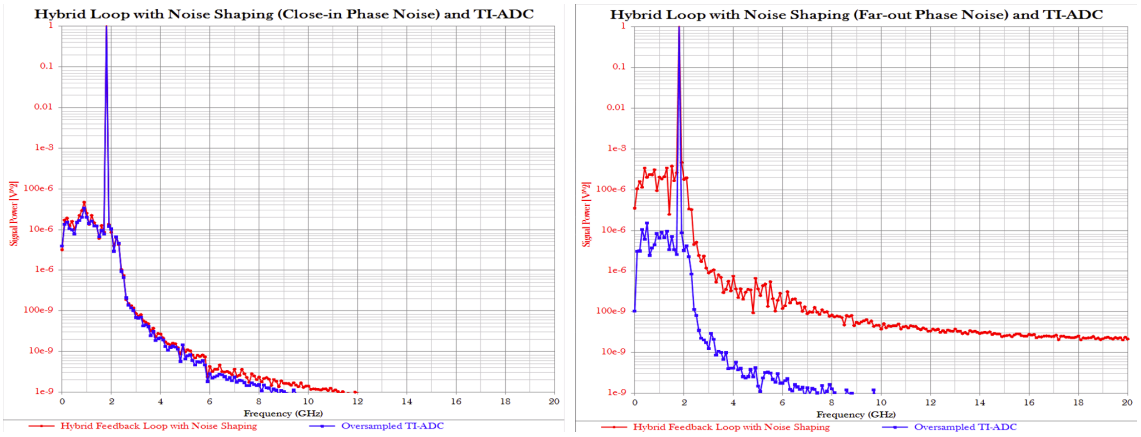
which can be written as

$$V_C(t-\sigma) = V_f(t-\sigma)S(t) \tag{4.23}$$

Now, using small signal approximation, we can write

$$\begin{aligned}V_C(t) &= V_C((t-\sigma)+\sigma) \\ &= V_C(t-\sigma) + \sigma \left.\frac{\mathrm{d}V_C(\tau)}{\mathrm{d}\tau}\right|_{\tau=t-\sigma} \\ &= V_f(t-\sigma)S(t) + \sigma\frac{\mathrm{d}(V_f(t-\sigma)S(t))}{\mathrm{d}t}\end{aligned} \tag{4.24}$$

[14]In a $\Delta\Sigma$ modulator, shaping is achieved by a DAC in feedback loop which is only sensitive to the discrete output value.



(a) Jitter dominated by close-in phase noise. (b) Jitter dominated by far-out phase noise.

Figure 4.14: Simulation results for comparison of direct sampling versus employing hybrid feedback loop.

Remember that we chose the shaping function such that when $V_f(t)$ has transitions, $S(t) \approx 0$. Therefore, we can further simplify the output as

$$V_C(t) \approx V_f(t-\sigma)S(t) + \sigma V_f(t-\sigma)\frac{\mathrm{d}S(t)}{\mathrm{d}t} \tag{4.25}$$

Note that once loop filters apply to the noisy output, $V_f(t-\sigma) \approx V_{in}(t-\sigma)$ shows up again, which adds the same sampling-like error to the loop. Fig. 4.14 shows two scenarios. In Fig. 4.14a, the first term in Eq. 4.25 is dominant since the second term is effectively filtered by the loop filters. In Fig. 4.14b however, the second term of Eq. 4.25 is dominant since $\frac{\mathrm{d}S(t)}{\mathrm{d}t}$ is very high and modulated by a white noise of $\sigma(t)$ which produces high power white noise that the loop filter cannot remove.

Different noise shaping methods such as SC (Switched-Capacitor), SI (Switched- Current), SSI (Switched-Shaped-Current), Sine-Shaped, and Delayed RZ have been explored [56] in the context of $\Delta\Sigma$ modulators since in those type of ADCs, the quantization noise of $\Delta\Sigma$ modulators will be modulated with the DAC jitter and fed back to the input which limits the effectiveness of the feedback loop for increasing the resolution [57]. In fact, it has been shown that the loop dynamic trades off quantization noise with jitter [58], however, when the input frequency is high, the dominant error is due to the sampling-similar error, not the mixing of the quantization noise [59].

Chapter 5

Frequency-Interleaved ADC

5.1 Architecture

The block diagram of Frequency-Interleaved ADC (FIADC) is shown in Fig. 5.1. This architecture is similar to the frequency-transnational hybrid filter bank which was introduced in Chapter 3.

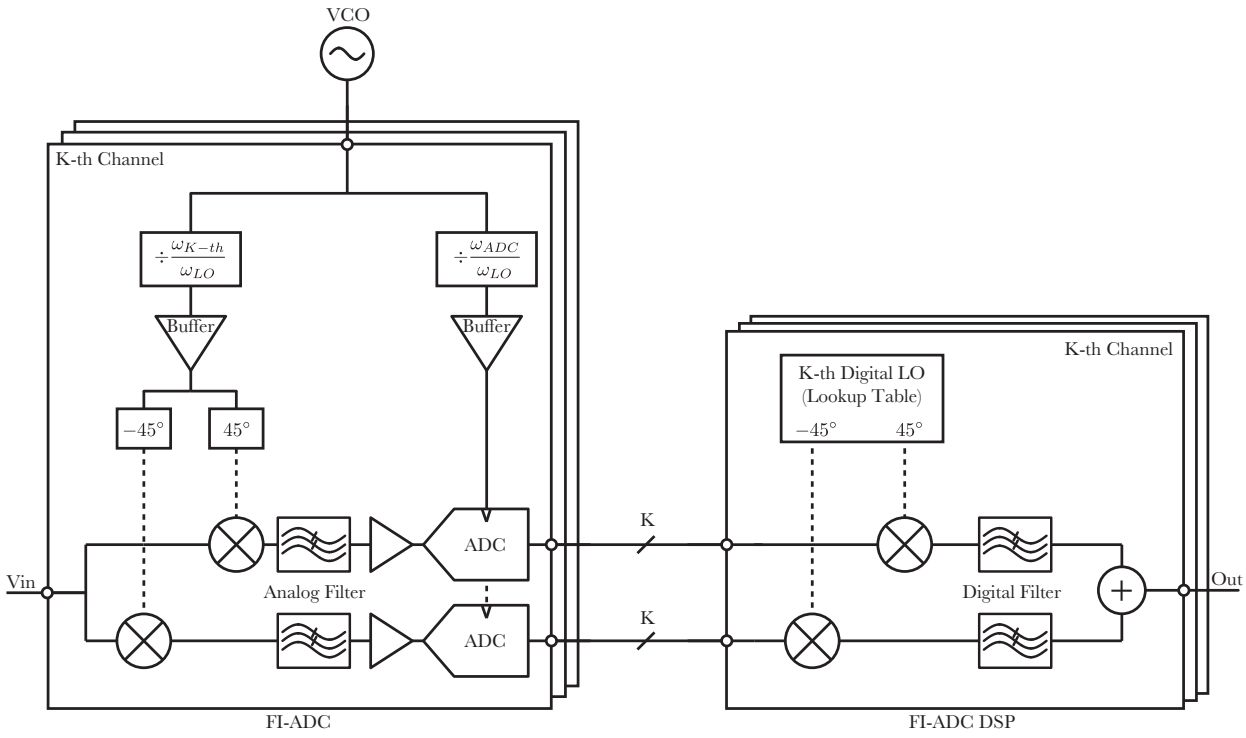


Figure 5.1: Block diagram of a frequency-interleaved ADC and digital signal processing.

The incoming signal goes though several parallel channels and then mixed with the channel-specific I/Q LO. Afterwards, each path is filtered and amplified to match to the full-scale of the following ADC. Once digitized, I/Q channels are first up-sampled[1] and then up-converted with digital mixers. Finally, I/Q paths are digitally filtered before summed with the output of other channels. We choose this particular architecture for further investigation since it has been speculated that frequency interleaving can mitigate the jitter error. The rational is that in such a architecture, all sub-ADCs are running at much lower speed (set by the maximum IF frequency of the system). Therefore, since the bandwidth of the input signal is reduced, higher jitter in sub-ADCs can be tolerated. With this interesting feature, we will analyze the noise, particularly quantization and jitter-induced noise, in this chapter.

5.2 Quantization Noise

First, let us get an intuitive idea of what we should expect and later on, we will take care of subtleties left behind. Let us assume that we have M number of parallel ADCs interleaved in frequency domain with different center frequencies. For a sinusoidal input signal, only one of the channels accepts the input signal while other channels filter it out. Therefore, despite having N channels, signal power will be provided by only one of them. However, all of the channels will add uncorrelated quantization noise. Therefore:

$$SNR_{FI-ADC} = \frac{Signal}{N \times QN} = \frac{SNR_{ADC}}{N} \tag{5.1}$$

In other words, frequency-interleaving degrades output SNR. Now, let us explain the subtleties:

1. If only ADCs in the desired channel receive signal, why do we expect quantization noise from all channels?
   Quantization noise is in fact tricky since the conventional SNR definition excites the ADC with a single-frequency CW wave which on the paper, leaves undesired channels at their resting state. In other words, at the absence of other nonidealities, undesired channels receive no input signal and generate no quantization noise. This situation in fact happens in ideal system simulations. However, it should be mentioned that this scenario is not practical in the real world where, for example, the input signal has wideband thermal noise. Therefore, while the factor of N exists in a practical situation, it may or may not show up in the system simulation depending on available nonidealities. Fig. 5.2 shows the output spectrum in a simulation of 3-channel FI-ADC with no nonidealities other than quantization error.

2. Why did we assume that signal power and quantization noise of each channel is similar to their counterparts in a conventional ADC? After all, each channel has two ADCs for

[1] To match with the Nyquist rate.

I/Q processing and despite the time-interleaving, signals from both ADCs are processed together for each output value.
Before providing the mathematical answer, let us explain what happens intuitively. For each channel, we have two sub-ADCs (for I/Q paths) with the same sampling clock and sampling edge. Since the input of the two ADCs are different, we still use the previous assumption that quantization errors are uncorrelated. Speaking of signal power, since each ADC carries either I or Q signals, after processing, they will be add in power and not in voltage. Therefore:

$$SNR_{FI-ADC,\,channel} = \frac{I+Q}{2 \times QN} = SNR_{ADC} \tag{5.2}$$

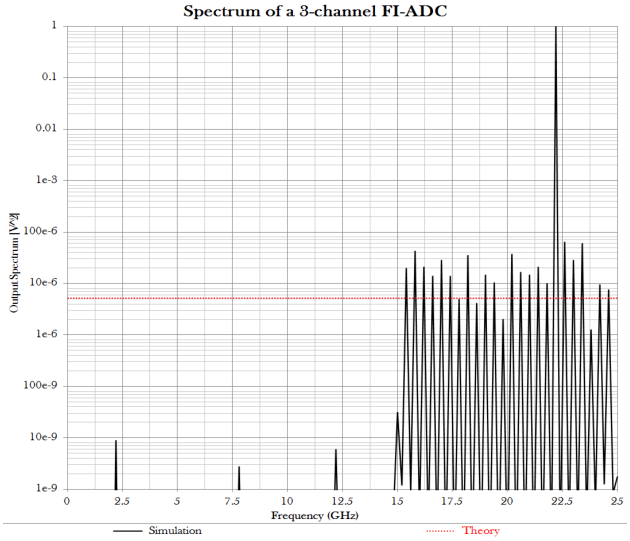


Figure 5.2: Output spectrum of a 3-channel FI-ADC with no nonidealities.

Now, let us prove our previous thoughts. Assuming that the LO frequency of the desired channel is ω_{LO} and $V_{in}(t) = A\sin(\omega_{in}t)$, after the mixing and filters ($\mathcal{F}$):

$$V_{Mixer,I} = \mathcal{F}\{A\sin(\omega_{in}t) \times \cos(\omega_{LO}t)\} = \frac{1}{2}\sin\left((\omega_{in} - \omega_{LO})\,t\right)$$
$$V_{Mixer,Q} = \mathcal{F}\{A\sin(\omega_{in}t) \times \sin(\omega_{LO}t)\} = \frac{1}{2}\cos\left((\omega_{in} - \omega_{LO})\,t\right)$$

Remember that in section 5.1, we mentioned that a gain stage after mixers and before ADCs are necessary. It should be clear now that in order to use the full input range of ADCs, a proper gain[2] is required. Otherwise, the signal power to the input of ADC will be

[2]The exact gain depends on the mixer topology, considering the Fourier coefficients of a hard mixer.

low while the quantization noise is unaltered[3]. With appropriate gain, the ADC output is:

$$\begin{aligned} V_{ADC,I} &= A\sin\left(\left(\omega_{in}-\omega_{LO}\right)t\right)+QN_I(t) \\ V_{ADC,Q} &= A\cos\left(\left(\omega_{in}-\omega_{LO}\right)t\right)+QN_Q(t) \end{aligned} \tag{5.3}$$

In the signal reconstruction unit, ADCs' outputs will be digitally up-converted. Keep in mind that since we are in the digital domain, up-conversion can be done by multiplying the ADC output with a real sinusoidal signal with no nonidealities[4].

$$\begin{aligned} V_{out}(t) &= \mathcal{F}\{V_{ADC,I}\times\cos(\omega_{LO}t)\}+\mathcal{F}\{V_{ADC,Q}\times\sin(\omega_{LO}t)\} \\ &= A\sin(\omega_{in}t)+[QN_I(t)\times\cos(\omega_{LO}t)+QN_Q(t)\times\sin(\omega_{LO}t)] \end{aligned} \tag{5.4}$$

Assuming that QN_I and QN_Q are uncorrelated, total noise power is the sum of power of each therm in the bracket in Eq. 5.4 and

$$SNR_{Out}=\frac{Signal}{QN\times\frac{1}{2}+QN\times\frac{1}{2}}=SNR_{ADC} \tag{5.5}$$

Therefore, for an N-channel frequency-interleaved ADC, the total quantization noise is:

$$QN_{FIADC,\,Direct}=N\times QN_{ADC} \tag{5.6}$$

Fig. 5.3 shows the simulation results. It can be seen that at absence of other nonidealities, the factor of N in Eq. 5.1 does not show up since single-tone CW input signal only excites the desired channel (Fig. 5.2). However, we can expect that in a practical situation (for example when LO jitter is considered), other channels will show quantization noise too and therefore, the factor of N can be predicted.

5.3 Jitter-induced Noise

Let us consider the SNR degradation due to the jitter in a frequency-interleaved ADC. Before we proceed, let us clarify on the assumptions we will use:

1. The close-in phase noise of the VCO will be correlated among all channels as explained in section 4.4. Moreover, we assume that the bandwidth of close-in phase noise is smaller than the pass-band of analog filters.

2. The far-out noise of the VCO will be assumed to be white and the spectral power uniformly distributed in $[0,\omega_{LO}]$.

[3]Quantization noise is calculated based on Eq. 2.2

[4]No hard mixing and thus no extra harmonics, no jitter and thus no SNR degradation, higher precision and thus no extra quantization noise.

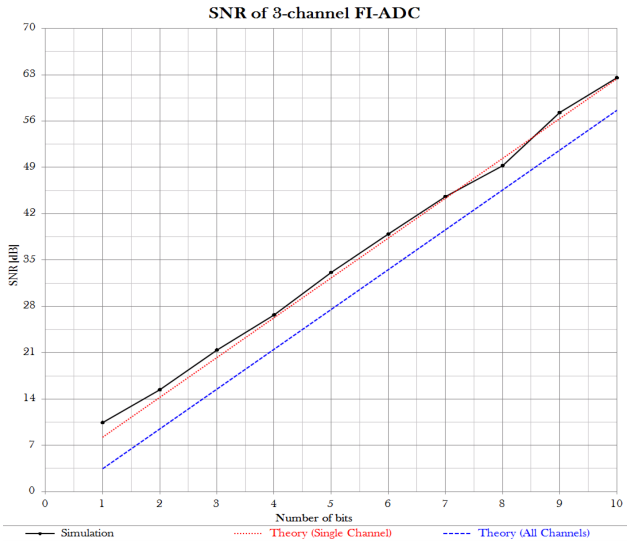


Figure 5.3: SNR vs ADC resolution in an ideal FI-ADC.

3. The far-out phase noise of the VCO will be assumed to be uncorrelated between mixer and ADC based on the discussion in section 4.4 given that analog filters provide enough delay.

4. Buffers will only add white noise with the spectral power uniformly distributed in $[0, \omega_{Buff}]$ where ω_{Buff} is the oscillation frequency of the LO signal passing through the buffer.

Now, we will find how each of phase-noise sources distorts the reconstruction of the input signal ($V_{in}(t) = A\sin(\omega_{in}t)$):

Sampling jitter of sub-ADCs

Here we assume that the master VCO is an ideal clock source and the clock distribution and buffers add white jitter noise to the clean VCO clock.

$$V_I(t) = 2\mathcal{F}\{A\sin(\omega_{in}t) \times \cos(\omega_{LO}t)\} = A\sin(\omega_{IF}t)$$
$$V_Q(t) = 2\mathcal{F}\{A\sin(\omega_{in}t) \times \sin(\omega_{LO}t)\} = A\cos(\omega_{IF}t)$$

where $\omega_{IF} = \omega_{in} - \omega_{LO}$. Since only the desired channels will have a strong signal at the input of its sub-ADCs, we will ignore the noise from other channels. Using the same method

used in section 2.2, we can write the ADC output[5] as

$$\begin{aligned} V_I(kT_s) &= A\sin(\omega_{IF}(kT_s - \sigma_I)) \\ &\approx A\sin(\omega_{IF}kT_s) - \omega_{IF}\sigma_I A\cos(\omega_{IF}kT_s) \\ V_Q(kT_s) &= A\cos(\omega_{IF}(kT_s - \sigma_Q)) \\ &\approx A\cos(\omega_{IF}kT_s) + \omega_{IF}\sigma_Q A\sin(\omega_{IF}kT_s) \end{aligned}$$

where σ_I and σ_Q represent the sampling clock uncertainty of in the I and Q paths respectively. Sub-ADCs' outputs will be passed to the DSP unit where they are up-converted by quadrature digitally-generated LO and then summed up.

$$\begin{aligned} V_{Out}(kT_s) &= V_I(kT_s) \times \cos(\omega_{LO}kT_s) + V_Q(kT_s) \times \sin(\omega_{LO}kT_s) \\ &= A\sin(\omega_{in}kT_s) \\ &- \omega_{IF}\sigma_I A\cos(\omega_{IF}kT_s)\cos(\omega_{LO}kT_s) + \omega_{IF}\sigma_Q A\sin(\omega_{IF}kT_s)\sin(\omega_{LO}kT_s) \end{aligned}$$

We will consider two cases for the correlation of σ_I and σ_Q:

- **Totally correlated $\sigma_I = \sigma_Q = \sigma$:** In this case, the output can be simplified to

  $$V_{Out}(kT_s) = A\sin(\omega_{in}kT_s) - \omega_{IF}\sigma A\cos((\omega_{IF} + \omega_{LO})kT_s)$$

  And therefore the normalized noise power is

  $$P_N|_{ADC,Correlated} = (\omega_{IF}\sigma)^2$$

- **Totally uncorrelated $\overline{\sigma_I} = \overline{\sigma_Q} = \overline{\sigma}$:** In this case, we just need to add the power of each noise term. And thus, the normalized noise power is

  $$P_N|_{ADC,Uncorrelated} = (\omega_{IF}\sigma)^2 \times \frac{1}{2} + (\omega_{IF}\sigma)^2 \times \frac{1}{2} = (\omega_{IF}\sigma)^2$$

Therefore, no matter whether the jitter is correlated or uncorrelated, the normalized noise power will be

$$\boxed{P_N|_{ADC} = (\omega_{IF}\sigma)^2} \tag{5.7}$$

Close-in phase noise of the master VCO

Let us assume that the master LO signal in the desired channel contributes to an effective jitter of σ_{LO}. At the input of sub-channel ADCs, we have:

$$\begin{aligned} V_I(t) &= 2\mathcal{F}\{A\sin(\omega_{in}t) \times \cos(\omega_{LO}(t + \sigma_{LO})\} = \mathcal{F}\{A\sin\left((\omega_{in} - \omega_{LO})\,t - \omega_{LO}\sigma_{LO}\right)\} \\ V_Q(t) &= 2\mathcal{F}\{A\sin(\omega_{in}t) \times \sin(\omega_{LO}(t + \sigma_{LO})\} = \mathcal{F}\{A\cos\left((\omega_{in} - \omega_{LO})\,t - \omega_{LO}\sigma_{LO}\right)\} \end{aligned}$$

[5]Quantization noise is neglected in this chapter.

Here we assumed that the filter takes care of the removing the unwanted mixing component[6]. After sub-channel ADCs, we have

$$\begin{aligned} V_I(kT_s) &= \mathcal{F}\{A\sin\left(\left(\omega_{in}-\omega_{LO}\right)\left(kT_s-\sigma_{LO}\right)-\omega_{LO}\sigma_{LO}\right)\} \\ &= \mathcal{F}\{A\sin\left(\left(\omega_{in}-\omega_{LO}\right)kT_s-\omega_{in}\sigma_{LO}\right)\} \\ V_Q(kT_s) &= \mathcal{F}\{A\cos\left(\left(\omega_{in}-\omega_{LO}\right)\left(kT_s-\sigma_{LO}\right)-\omega_{LO}\sigma_{LO}\right)\} \\ &= \mathcal{F}\{A\cos\left(\left(\omega_{in}-\omega_{LO}\right)kT_s-\omega_{in}\sigma_{LO}\right)\} \end{aligned}$$

Assuming small jitter, we can make approximations:

$$\begin{aligned} V_I(kT_s) &\approx \mathcal{F}\{A\sin\left(\left(\omega_{in}-\omega_{LO}\right)kT_s\right)-A\omega_{in}\sigma_{LO}\cos\left(\left(\omega_{in}-\omega_{LO}\right)kT_s\right)\} \\ V_Q(kT_s) &\approx \mathcal{F}\{A\cos\left(\left(\omega_{in}-\omega_{LO}\right)kT_s\right)+A\omega_{in}\sigma_{LO}\sin\left(\left(\omega_{in}-\omega_{LO}\right)kT_s\right)\} \end{aligned}$$

Assuming that the bandwidth of the close-in phase noise is much smaller than the pass-band of filter, we have:

$$\begin{aligned} V_I(kT_s) &\approx A\sin\left(\left(\omega_{in}-\omega_{LO}\right)kT_s\right)-A\omega_{in}\sigma_{LO}\cos\left(\left(\omega_{in}-\omega_{LO}\right)kT_s\right) \\ V_Q(kT_s) &\approx A\cos\left(\left(\omega_{in}-\omega_{LO}\right)kT_s\right)+A\omega_{in}\sigma_{LO}\sin\left(\left(\omega_{in}-\omega_{LO}\right)kT_s\right) \end{aligned}$$

After digital up-conversion and reconstruction, we have

$$V_{Out}(kT_s) \approx A\sin\left(\omega_{in}kT_s\right)-A\omega_{in}\sigma_{LO}\cos\left(\omega_{in}kT_s\right) \tag{5.8}$$

And therefore, the total normalized noise is

$$\boxed{P_N|_{Close-in,VCO} = \left(\omega_{in}\sigma_{LO}\right)^2} \tag{5.9}$$

Fig. 5.4 shows that the theory matches well with the simulation. Note that close-in phase-noise does not show up in undesired channels.

Far-out phase noise of the master VCO and buffers

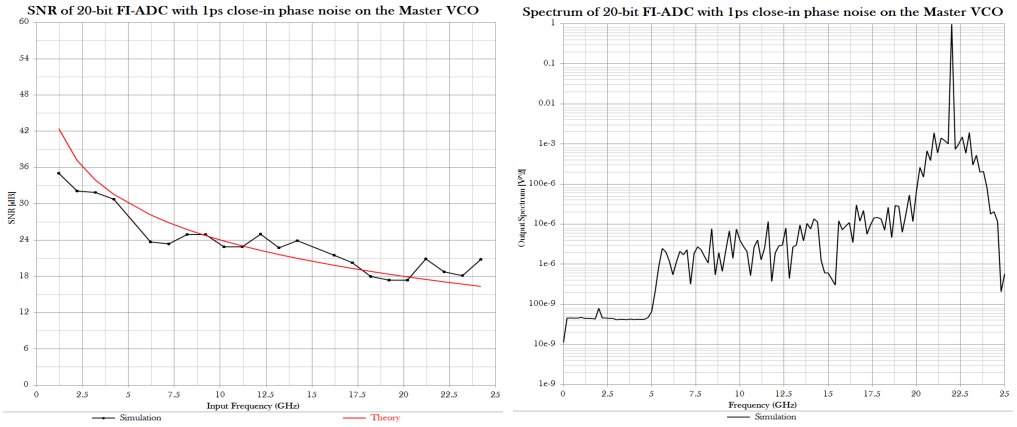
Let us assume that the master LO signal in the desired channel has a white jitter of σ_{RMS}. Given that analog filters add delay to the data path, as explained in section 4.4, we will make the assumption that noise appears uncorrelated on the mixing stage and ADC sampling stage. If FI-ADC has N channels (0-th channel only has dummy mixers and the rest of N-1 channels are I/Q mixing (Fig. 5.5[7])), then the bandwidth of the analog filters are [8]

$$\omega_{Pass} = \frac{\omega_{in,max}}{2(N-1)+1} = \frac{\omega_{in,max}}{2N-1} \tag{5.10}$$

[6]We also ignored the delay of the signal passing through the filter since it is much smaller than (the inverse of) the noise bandwidth.

[7]In this particular example, 3rd harmonic rejection is required, either in the analog domain (by extra mixers) or the digital time (by removing the deterministic errors).

[8]Assuming brick-wall filters.



(a) SNR (b) Spectrum

Figure 5.4: Simulation of 20-bit 3-channel FI-ADC with $1ps$ of RMS Jitter ($1GHz$ bandwidth) on the Master VCO

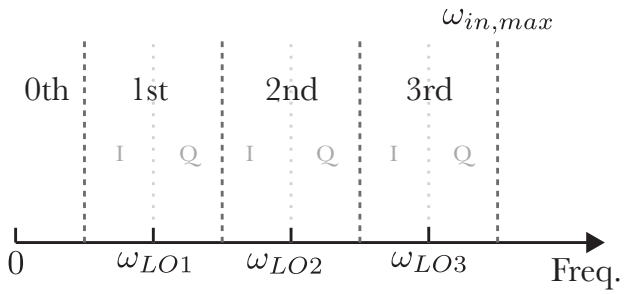


Figure 5.5: Example of 4-channel FI-ADC

Also, as explained in section 4.2, if hard mixers are used, skirt of the phase noise will show up in all channels. However, analog filters here also help in attenuating the noise that lies out their bandwidth. Since we are only interested in the white noise power, we use Eq. 4.8 and the equivalent noise source introduced there:

$$V_{N,I}(t) = \mathcal{F}\{2A\cos(\omega_{in}t) \times \sigma'_{LO,K,I}(t)\}$$
$$V_{N,Q}(t) = \mathcal{F}\{2A\cos(\omega_{in}t) \times \sigma'_{LO,K,Q}(t)\}$$

Remember that a gain of 2 is necessary to bring the down-converted signal to the full range of ADC. Keep in mind that $\sigma'_{LO,K,I}(t)$ and $\sigma'_{LO,K,Q}(t)$ have the same power spectral density of $\frac{\omega_{LO,K}{\sigma_{RMS}}^2}{4}$, however, they are coming from separate edges, which means that they are

uncorrelated. Therefore, the total noise after the filter is

$$V_{N,I,RMS} = 2^2\frac{A^2}{2} \times \frac{\omega_{LO,K}{\sigma_{RMS}}^2}{4} \times \frac{\omega_{in,max}}{2N-1} = P_{in} \times \frac{\omega_{in,max}{\sigma_{LO}}^2}{2N-1}\omega_{LO,K}$$
$$V_{N,Q,RMS} = 2^2\frac{A^2}{2} \times \frac{\omega_{LO,K}{\sigma_{RMS}}^2}{4} \times \frac{\omega_{in,max}}{2N-1} = P_{in} \times \frac{\omega_{in,max}{\sigma_{LO}}^2}{2N-1}\omega_{LO,K}$$

Where $P_{in} = \frac{A^2}{2}$. In the processing unit, these two signals will be multiplied by quadrature LO and summed together:

$$V_{N,Out}(t) = V_{N,I}(t)\sin(\omega_{LO,K}) + V_{N,I}(t)\cos(\omega_{LO,K}) \tag{5.11}$$

And therefore, the RMS noise at the output of each channel can be easily calculated:

$$\begin{aligned} V_{N,Out,RMS} &= \left[P_{in} \times \frac{\omega_{in,max}{\sigma_{LO}}^2}{2N-1}\omega_{LO,K}\right] \times \frac{1}{2} + \left[P_{in} \times \frac{\omega_{in,max}{\sigma_{LO}}^2}{2N-1}\omega_{LO,K}\right] \times \frac{1}{2} \\ &= P_{in} \times \frac{\omega_{in,max}{\sigma_{LO}}^2}{2N-1}\omega_{LO,K} \end{aligned} \tag{5.12}$$

As shown in the example of Fig. 5.5, $\omega_{LO,K}$ can be calculated based on the maximum input bandwidth

$$\omega_{LO,K} = \frac{2K}{2N-1}\omega_{in,max}$$

Note that $K \in [0, N-1]$. Therefore, total normalized noise[9] from mixers of each channel can be simplified to

$$N|_{K-Ch} = \frac{\omega_{in,max}{\sigma_{LO}}^2}{2N-1} \times \frac{2K}{2N-1}\omega_{in,max} = \frac{2K}{(2N-1)^2}(\omega_{in,max}\sigma_{LO})^2$$

Adding up the total noise from mixers of all channels, we get

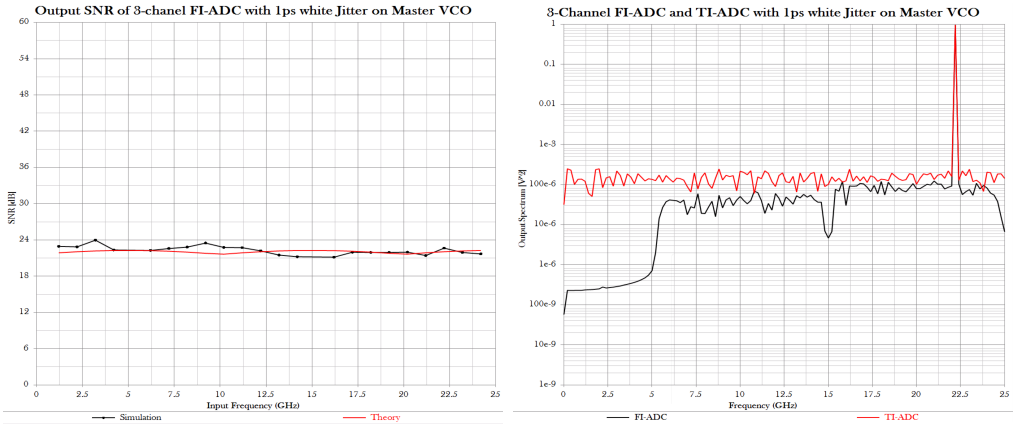
$$N|_{far-out,VCO,mixers} = (\omega_{in,max}\sigma_{LO})^2 \sum_{0}^{N-1} \frac{2K}{(2N-1)^2} = (\omega_{in,max}\sigma_{LO})^2 \frac{N(N-1)}{(2N-1)^2}$$

Now, let us add the impact of ADC's sampling jitter. First, note that only the desired channel has a large input power into the ADCs and other channels only have noise. Using uncorrelated jitter approximation based on the discussion in section 4.4, we can modify Eq. 5.7 as

$$P_N|_{far-out,VCO,ADC} = (\omega_{IF}\sigma_{LO})^2 \tag{5.13}$$

Therefore, the total noise of an N-channel FI-ADC due to the far-out phase noise of the master VCO is

$$\boxed{P_N|_{far-out,VCO} = (\omega_{IF}\sigma_{LO})^2 + (\omega_{in,max}\sigma_{LO})^2 \frac{N(N-1)}{(2N-1)^2}} \tag{5.14}$$



(a) SNR (b) Spectrum

Figure 5.6: 3-channel FI-ADC with 1ps or RMS white jitter on the master VCO

Fig. 5.6a compares the simulation results with the theory developed. Fig. 5.6b shows the output spectrum of a 3-channel FI-ADC compared to the output spectrum of a TI-ADC. It would be helpful to understand what is happening intuitively. As $N \to \infty$[10] in Eq. 5.14, $\omega_{IF} \to 0$ and in limit we get

$$\lim_{N\to\infty} P_N|_{far-out,VCO} = \frac{(\omega_{in,max}\sigma_{LO})^2}{4} \tag{5.15}$$

It means that we get $6dB$ SNR improvement from FI-ADC compared to TI-ADC considering only the VCO's far-out phase noise. The first $3dB$ comes from the fact that by mixing the input signal with different LO frequencies, they add noise to the output at different rates which shows itself as the "slope" of noise floor. The other $3dB$ comes indirectly from I/Q mixing. Although I/Q processing does not improve the SNR[11], quadrature LO signals are coming from separate edges of an oscillator that is running at twice higher frequency[12]. Since we assumed that jitter is a random white noise, separate edges means uncorrelated jitter for I/Q LO signals. Fig. 5.7 illustrates this theory which can be compared with Fig. 5.6b.

[9]Normalized to P_{in}.

[10]We are ignoring the fact that for $N > 3$, harmonic rejection for hard mixers are required in either of the analog or digital domains.

[11]Since two noise sources are adding up with two quadrature-orthogonal signals which they add in power.

[12]That means in the analog domain, we are "oversampling".

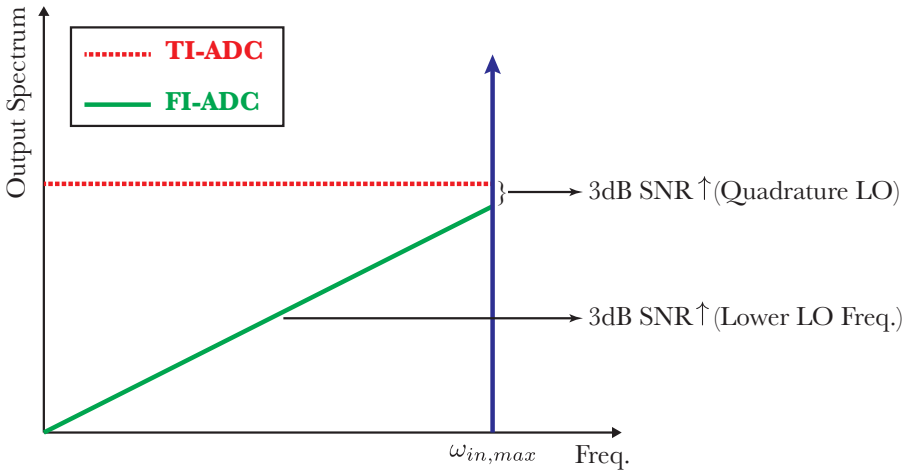


Figure 5.7: Intuitive explanation of FI-ADC SNR improvement over TI-ADC

Chapter 6

Conclusion

In this thesis, we reviewed several methods used to increase the data (or information) rate in analog converters and mitigate the jitter-induced SNR degradation. In this chapter, we will conclude our discussion.

6.1 TI-ADC vs FI-ADC

As we mentioned earlier, state-of-the-art high speed ADCs are currently limited by the jitter-induced noise. Frequency interleaved architecture outperforms time-interleaved counterparts by $6dB$ for CW signals, considering only the far-out phase noise of VCO. However, SNR in the FI-ADC is almost independent the input signal while in TI-ADC, it does depend on the spectral content of the input signal. For a wideband input signal with flat spectral content, TI-ADC achieves $10dB$ higher SNR compared to a CW tone. Therefore, the choice of time-interleaving or frequency-interleaving depends on the application and the characteristics of the incoming signal.

Another important factor is the number of channels in an FIADC. If we include all the noise sources we considered in the previous chapter, we get

$$\begin{aligned} SNR^{-1} =& N \times \frac{2}{3} \times 2^{-2B} + (\omega_{in,max}\sigma_{LO,far-out})^2 \frac{N(N-1)}{(2N-1)^2} \\ &+ (\omega_{in}\sigma_{LO,close-in})^2 \\ &+ (\omega_{IF}\sigma_{LO,far-out})^2 + (\omega_{IF}\sigma_{ADC})^2 \end{aligned}$$

The first two terms are independent of the input signal and set an upper limit to the achievable SNR in FIADC[1]. Neglecting the close-in phase noise of the VCO, Fig. 6.1 shows the SNR vs number of channels in FIADC. It should be clear that an optimum exists for different noise combinations.

[1]Note that if $N = 1$, a TIADC is achieved

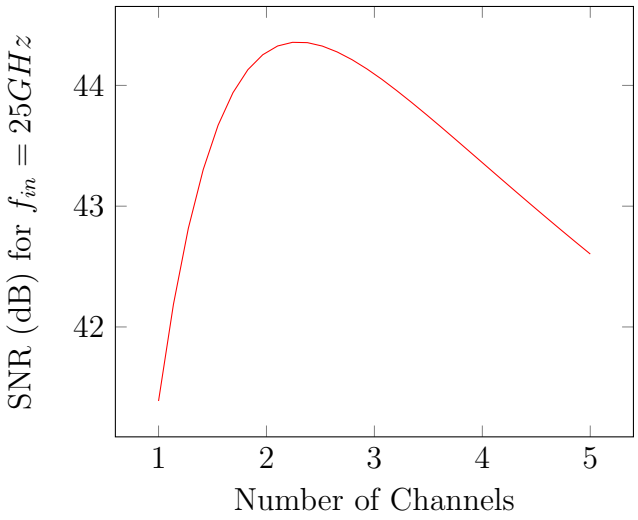


Figure 6.1: FIADC with 8-bit sub-ADCs, $100fs$ far-out jitter on the master VCO, and $300fs$ ADC jitter.

6.2 Implementation Considerations

This thesis dealt with the analog-to-digital converter nonidealities from a system perspective. However, circuit implementation can make dramatic changes. For example, we assumed a that jitter has the same profile for both time-interleaved and frequency-interleaved architectures. However, the LO generation and distribution circuitry in a frequency-interleaved system utilizes LC tuned networks which potentially results in much lower integrated jitter.

6.3 Future Directions

Oversampling

In the digital domain, oversampling helps to widen the same white noise power over a larger bandwidth which can be filtered using digital filters. In the analog domain, oversampling means using harmonic rejection mixers even if the harmonic band does not have any content to fold on top of the desired signal. By doing so, white jitter power will be spread over a larger bandwidth which will be filtered using analog filters. As it was mentioned in previous the chapter, $3dB$ of noise improvement in FIADC comes from analog oversampling.

Combining Several Techniques

Combining different methods provided in this thesis can potentially solve many issues. Here, we will provide two examples.

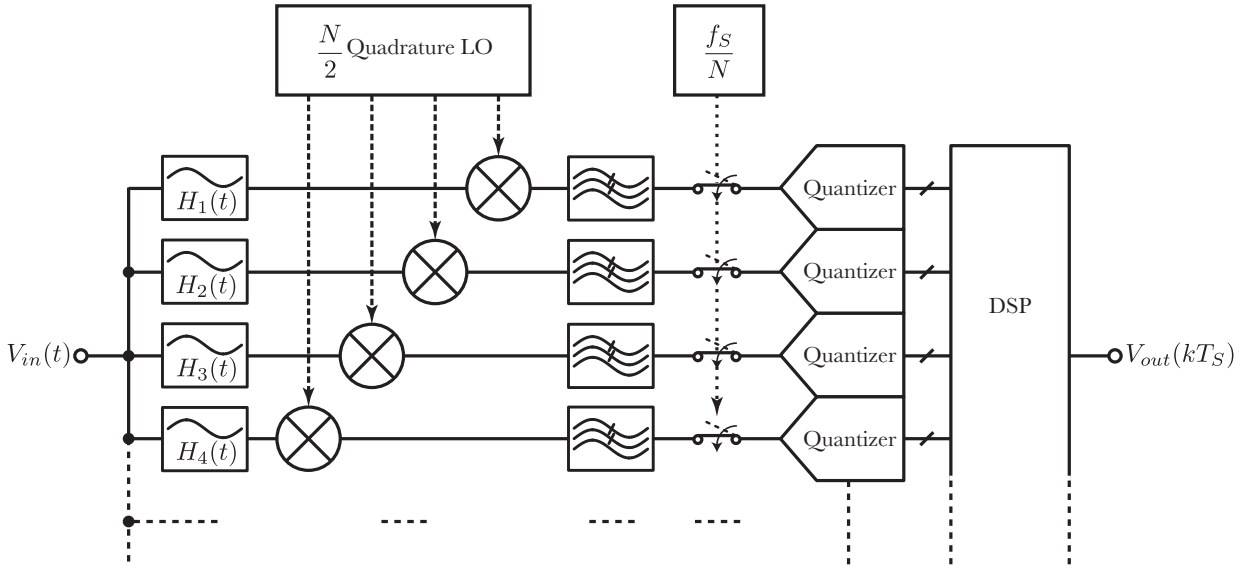


Figure 6.2: Frequency interleaved architecture with initial coarse channel filtering.

Consider Fig. 6.2 in which coarse filters are added to the normal frequency-interleaved architecture. We showed that the jitter skirt shows up in the undesired channel since it still gets mixed with the incoming signal. A coarse filter before mixer, which can extend beyond each channels bandwidth, can remove the impact of reciprocal mixing and improve the SNR.

Since laser sources have very low jitter, they can be utilized to lower the RMS jitter, as shown in Fig. 6.3, where photo-conductive switches are used for sampling. In order to avoid producing time-interleaved laser pulses, spatial stretching can be exploited using an interposer or any other technologies. Quantization task is passed to a CMOS chip in which digitization can be done very efficiently. If the bandwidth of the interconnect between photonic and CMOS chips is an issue, frequency-folded architecture can be a viable solution.

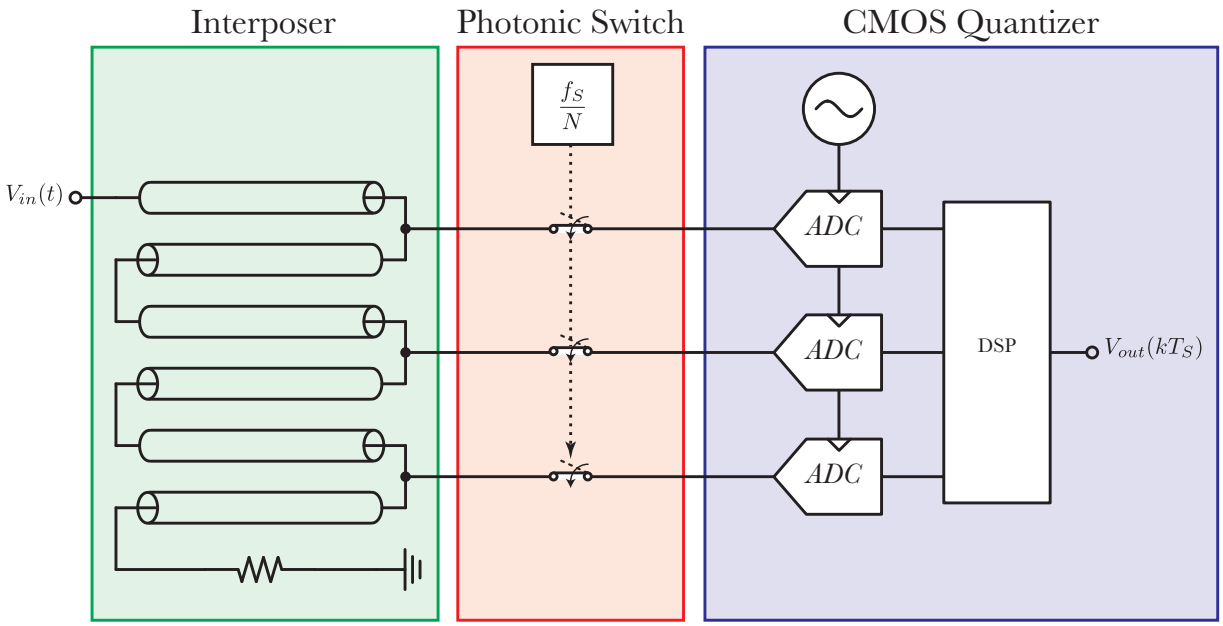


Figure 6.3: High speed sampling using mixed technologies.

Bibliography

[1] Deloitte, "Semiconductors – the Next Wave Opportunities and winning strategies for semiconductor companies," *Deloitte*, no. April, pp. 1–58, 2019. [Online]. Available: https://www2.deloitte.com/content/dam/Deloitte/cn/Documents/technology-media-telecommunications/deloitte-cn-tmt-semiconductors-the-next-wave-en-190422.pdf

[2] B. Murmann, *"ADC Performance Survey 1997-2020,"*. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

[3] S. Rajagopal, "Power efficiency: The next challenge for multi-gigabit-per-second Wi-Fi," *IEEE Communications Magazine*, vol. 52, no. 11, pp. 40–45, 2014.

[4] J. Singh, S. Ponnuru, and U. Madhow, "Multi-Gigabit communication: The ADC bottleneck," *Proceedings - 2009 IEEE International Conference on Ultra-Wideband, ICUWB 2009*, vol. 2009, pp. 22–27, 2009.

[5] Seth Lloyd, "Ultimate physical limits to computation," *Nature*, vol. 406, no. August, pp. 1047–1054, 2000.

[6] J. Singh, O. Dabeer, and U. Madhow, "Capacity of the discrete-time AWGN channel under output quantization," *IEEE International Symposium on Information Theory - Proceedings*, pp. 1218–1222, 2008.

[7] S. Krone and G. Fettweis, "Fundamental limits to communications with analog-to-digital conversion at the receiver," *IEEE Workshop on Signal Processing Advances in Wireless Communications, SPAWC*, pp. 464–468, 2009.

[8] R. H. Walden, "Analog-to-digital converter survey and analysis," *Software Radio Technologies: Selected Readings*, vol. 17, no. 4, pp. 82–93, 2001.

[9] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter Analysis of High-Speed Sampling Systems," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, pp. 220–224, 1990.

[10] M. Verhelst and A. Bahai, "Where Analog Meets Digital: Analog?to?Information Conversion and beyond," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 3, pp. 67–80, 2015.

[11] L. Y. Nathawad, R. Urata, B. A. Wooley, and D. A. Miller, "A 40-GHz-Bandwidth, 4-Bit, Time-Interleaved A/D Converter Using Photoconductive Sampling," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2021–2030, 2003.

[12] A. Mahjoubfar *et al.*, "Time stretch and its applications," *Nature Photonics*, vol. 11, no. 6, pp. 341–351, 2017. [Online]. Available: http://dx.doi.org/10.1038/nphoton.2017.76

[13] B. Grave and A. Arbabian, "Spatially interleaved architecture for high-frequency data converters," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2016-July, pp. 1450–1453, 2016.

[14] K. J. Koh and H. Elyasi, "Time-interleaved phased arrays with parallel signal processing in RF modulations," *IEEE Transactions on Antennas and Propagation*, vol. 62, no. 2, pp. 677–689, 2014.

[15] M. Jarrahi, R. F. W. Pease, D. A. Miller, and T. H. Lee, "Optical spatial quantization for higher performance analog-to-digital conversion," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 9, pp. 2143–2150, 2008.

[16] G. W. Roberts and M. Ali-Bakhshian, "A brief introduction to time-to-digital and digital-to-time converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 3, pp. 153–157, 2010.

[17] A. Pathan and A. Liscidini, "Thermal noise limit for time-domain analogue signal processing in CMOS technologies," *Electronics Letters*, vol. 52, no. 18, pp. 1567–1569, 2016.

[18] R. B. Staszewski *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, 2004.

[19] S. Ziabakhsh, G. Gagnon, and G. W. Roberts, "The Peak-SNR Performances of Voltage-Mode versus Time-Mode Circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 12, pp. 1869–1873, 2018.

[20] S. Callender, "Wideband signal acquisition via frequency-interleaved sampling," Ph.D. dissertation, EECS Department, University of California, Berkeley, Dec 2015. [Online]. Available: http://www2.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-224.html

[21] N. Da Dalt, M. Harteneck, C. Sandner, and A. Wiesbauer, "On the jitter requirements of the sampling clock for analog-to-digital converters," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 9, pp. 1354–1360, 2002.

[22] H. Kobayashi, M. Morimura, K. Kobayashi, and Y. Onaya, "Aperture jitter effects in wideband ADC systems," *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems*, vol. 3, no. 4, pp. 1705–1708, 1999.

[23] B. Razavi, "Design considerations for interleaved ADCs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1806–1817, 2013.

[24] T. Forbes and R. Gharpurey, "A 2 GS/s frequency-folded ADC-based broadband sampling receiver," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 9, pp. 1971–1983, 2014.

[25] S. J. Tilden *et al.*, *IEEE Std.1241-2010 - IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters (Revision of IEEE Std.1241-2000)*, 2011, no. 1241. [Online]. Available: http://dx.medra.org/10.1109/IEEESTD.2011.5692956

[26] V. J. Arkesteijn, E. A. Klumperink, and B. Nauta, "Jitter Requirements of the Sampling Clock in Software Radio Receivers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 2, pp. 90–94, 2006.

[27] A. Eshraghi and T. Fiez, "Comparison of three parallel $\Delta\Sigma$ A/D converters," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 517–520, 1996.

[28] A. Eshraghi and T. S. Fiez, "A comparative analysis of parallel delta-sigma ADC architectures," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 3, pp. 450–458, 2004.

[29] R. G. Vaughan, N. L. Scott, and D. R. White, "The Theory Of Bandpass Sampling," *IEEE Transactions on Signal Processing*, vol. 39, no. 9, pp. 1973–1984, 1991.

[30] A. Petraglia and S. K. Mitra, "High-Speed A/D Conversion Incorporating a QMF Bank," *IEEE Transactions on Instrumentation and Measurement*, vol. 41, no. 3, pp. 427–431, 1992.

[31] I. Galton and H. T. Jensen, "Delta-Sigma Modulator Based A/D Conversion without Oversampling," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 773–784, 1995.

[32] A. Agrawal and A. Natarajan, "Analysis and Design of N-Path RF Bandstop Filters Using Walsh-Function-Based Sequence Mixing," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 11, pp. 4830–4843, 2018.

[33] M. Patel, I. Darwazeh, and J. J. O'reilly, "Bandpass sampling for software radio receivers, and the effect of oversampling on aperture jitter," *IEEE Vehicular Technology Conference*, vol. 4, pp. 1901–1905, 2002.

[34] S. R. Velazquez, T. Q. Nguyen, and S. R. Broadstone, "Design of hybrid filter banks for analog/digital conversion," *IEEE Transactions on Signal Processing*, vol. 46, no. 4, pp. 956–967, 1998.

[35] H. Chae and M. P. Flynn, "A 69 dB SNDR, 25 MHz BW, 800 MS/s Continuous-Time Bandpass $\Delta\Sigma$ Modulator Using a Duty-Cycle-Controlled DAC for Low Power and Reconfigurability," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 649–659, 2016.

[36] S. J. Mazloumar and S. Mirabbas, "A frequency-translating hybrid architecture for wide-band analog-to-digital converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 7, pp. 576–580, 2007.

[37] K. Lee and W. Namgoong, "A 0.25μm CMOS 3b 12.5GS/S frequency channelized receiver for serial-links," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, vol. 48, pp. 336–337, 2005.

[38] G. Ding, C. Dehollain, M. Declercq, and K. Azadet, "Frequency-interleaving technique for high-speed A/D conversion," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 857–860, 2003.

[39] S. Hoyos *et al.*, "Clock-jitter-tolerant wideband receivers: An optimized multichannel filter-bank approach," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 2, pp. 253–263, 2011.

[40] V. K. Singh, W. G. Ho, and R. Gharpurey, "A Frequency-Folded ADC Channelizer with Digital Equalization and Relaxed Anti-Alias Filtering," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 7, pp. 2304–2317, 2018.

[41] X. Chen, Z. Yu, S. Hoyos, B. M. Sadler, and J. Silva-Martinez, "A sub-nyquist rate sampling receiver exploiting compressive sensing," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 3, pp. 507–520, 2011.

[42] O. U. Khan and D. D. Wentzloff, "1.2 GS/s Hadamard Transform front-end for compressive sensing in 65nm CMOS," *IEEE Radio and Wireless Symposium, RWS*, pp. 181–183, 2013.

[43] O. Abari, F. Lim, F. Chen, and V. Stojanovic, "Why analog-to-information converters suffer in high-bandwidth sparse signal applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 9, pp. 2273–2284, 2013.

[44] R. Gharpurey and P. Kinget, "Channelized front ends for broadband analog & RF signal processing with merged LO synthesis," *Proceedings of the 2009 IEEE Dallas Circuits and Systems Workshop: Energy Efficient Circuits and Systems, DCAS-2009*, pp. 23–26, 2009.

[45] C. R. Galand and D. J. Esteban, "Design and Evaluation of Parallel Quadrature Mirror Filters (PQMF)." *ICASSP, IEEE International Conference on Acoustics, Speech and Signal Processing - Proceedings*, vol. 1, pp. 224–227, 1983.

[46] H. Krishnaswamy *et al.*, "RF channelizer architectures using Iterative Downconversion for concurrent or fast-switching spectrum analysis," *Midwest Symposium on Circuits and Systems*, pp. 977–980, 2014.

[47] X. Q. Du, M. Grozing, M. Buck, and M. Berroth, "A 40 GS/s 4 bit SiGe BiCMOS flash ADC," *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, vol. 2017-October, pp. 138–141, 2017.

[48] B. Asuri, Y. Han, and B. Jalali, "Time-stretched ADC arrays," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, no. 7, pp. 521–524, 2002.

[49] W. J. Caputi, "Stretch: A time-transformation technique," *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-7, no. 2, pp. 269–278, 1971.

[50] F. Coppinger, A. S. Bhushan, and B. Jalali, "Photonic time stretch and its application to analog-to-digital conversion," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 7 PART 2, pp. 1309–1314, 1999.

[51] A. S. Bhushan, P. V. Kelkar, B. Jalali, O. Boyraz, and M. Islam, "130-GSa/s photonic analog-to-digital converter with time stretch preprocessor," *IEEE Photonics Technology Letters*, vol. 14, no. 5, pp. 684–686, 2002.

[52] T. R. Clark, J. U. Kang, and R. D. Esman, "Performance of a time- and wavelength-interleaved photonic sampler for analog-digital conversion," *IEEE Photonics Technology Letters*, vol. 11, no. 9, pp. 1168–1170, 1999.

[53] B. Xiang, A. Kopa, Z. Fu, and A. B. Apsel, "Theoretical analysis and practical considerations for the integrated time-stretching system using dispersive delay line (DDL)," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 11, pp. 3449–3457, 2012.

[54] B. Nikfal, Q. Zhang, and C. Caloz, "Comments on 'theoretical analysis and practical considerations for the integrated time-stretching system using dispersive delay line (DDL)'," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 5, p. 1973, 2013.

[55] H. Y. Chang, Y. L. Yeh, Y. C. Liu, M. H. Li, and K. Chen, "A low-jitter low-phase-noise 10-GHz sub-harmonically injection-locked PLL with self-aligned DLL in 65-nm CMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 3, pp. 543–555, 2014.

[56] H. Chang and H. Tang, "A simple technique to reduce clock jitter effects in continuous-time delta-sigma modulators," *Proceedings - IEEE International Symposium on Circuits and Systems*, pp. 1870–1873, 2008.

[57] A. Ashry and H. Aboushady, "Jitter analysis of bandpass continuous-time ΣΔMs for different feedback DAC shapes," *ISCAS 2010 - 2010 IEEE International Symposium on Circuits and Systems: Nano-Bio Circuit Fabrics and Systems*, vol. 2, no. 1, pp. 3997–4000, 2010.

[58] K. Reddy and S. Pavan, "Fundamental limitations of continuous-time delta-sigma modulators due to clock jitter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 10, pp. 2184–2194, 2007.

[59] J. Chi, R. Ritter, J. Wagner, J. Anders, and M. Ortmanns, "Phase noise vs. jitter analysis in continuous-time LP and BP ΣΔ modulators with interferers," *2016 IEEE International Conference on Electronics, Circuits and Systems, ICECS 2016*, pp. 476–479, 2017.