Low Noise Integrated CMOS Receiver Front-End

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Low Noise Integrated CMOS Receiver Front-End

by Ahmed Khidre

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Second Reader

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ABSTRACT

This project presents design and simulation results for a low noise receiver front-end subsystem, which consists of LNA, IQ Mixer, buffer for LO signal, and IF VGA. The cascaded blocks have input return loss of < -15 dB, overall noise figure (NF) of < 5 dB, overall input-referred third-order intercept point (IIP_3) of > -26 dBm and input-referred second-order intercept point (IIP_2) of > 10 dBm.

Practical biasing circuits are used in blocks simulation to consider performance impairments due to their non-idealities, such as noise. The only ideal source used in simulations is the VDD supply rail. A commercial FD-SOI 28nm CMOS process by STMicroelectronics foundry is used throughout the project.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

I. INTRODUCTION

A. ZIF Receivers

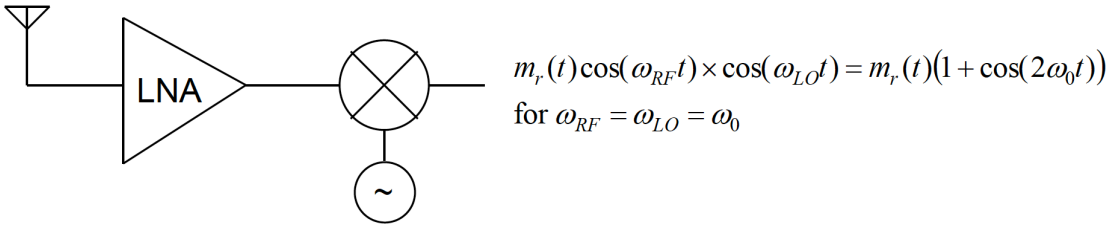


Figure 1-1. Block diagram for RF down conversion

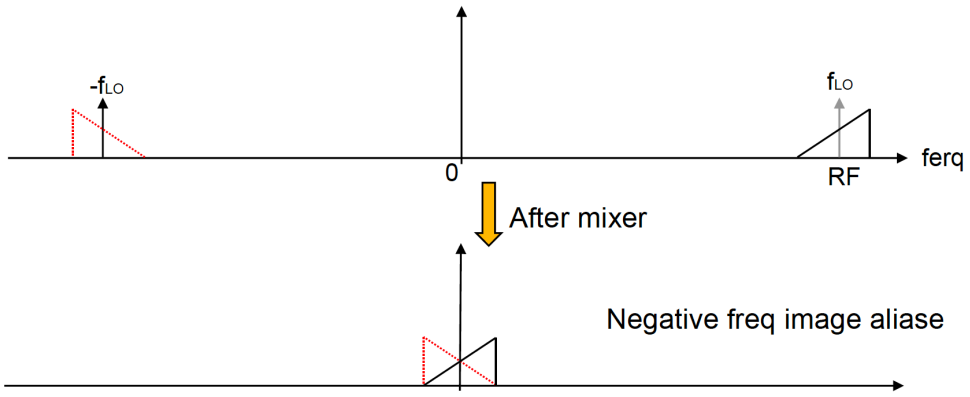


Figure 1-2. Frequency aliasing mechanism in direct conversion receiver of complex modulated signals

In zero IF (ZIF) architecture, the LO frequency is set same as RF signal and hence the down converted signal is set at DC. Such architecture avoids image problem in the super heterodyne and hence OFF-chip SAW image rejection filter is not required. Therefore, ZIF architecture permits whole front-end integration on one chip and hence widely used in most modern wireless systems such as WiFi, 3G WCDMA/UMTS, $G LTE and 5G. It also a great platform for multi band receivers. For complex modulated

signals, the negative frequency band aliases into the positive frequency band and in such case, image becomes the signal itself.

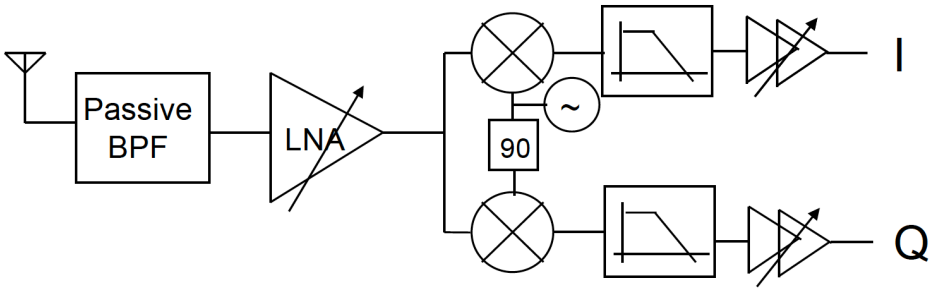
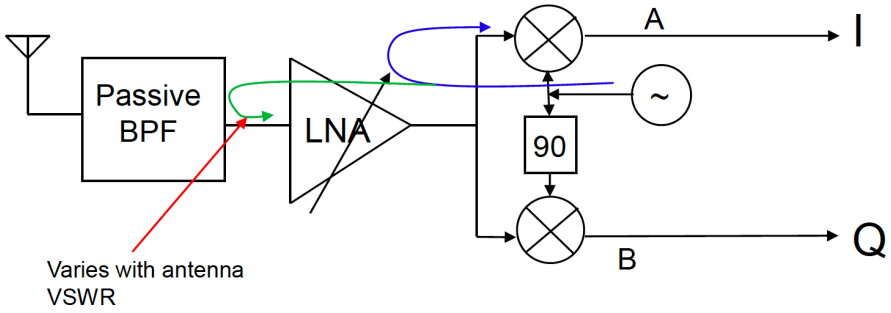


Figure 1-3. The orthogonal mixing scheme in radio front end receiver

Aliasing (negative band folding on positive band) is avoided by using orthogonal mixing, also known by IQ, scheme is used as shown in figure 3. The IQ mixing also sustains information on both I and Q paths for multi symbol modulation, such as QPSK. The image rejection requirement is alleviated in ZIF architecture since the image is the signal itself so, I/Q matching is not as critical (required image rejection is set by the target SNR).

B. Problems with ZIF receiver architecture

1. LO self-mixing



$$LO = p(t)\cos(\omega_{LO}t + \varphi(t))$$

$$LO \times LO = p(t)^2 + p(t)^2\cos(2\omega_{LO}t + 2\varphi(t))$$

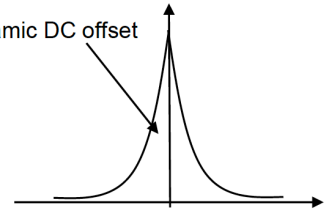


Figure 1-4. illustration for LO self-mixing mechanism

LO self-mixing degrades DC-offset in direct-conversion receiver. Static one can be calibrated out but dynamic one (time varying) can be a problem

2. DC Offset

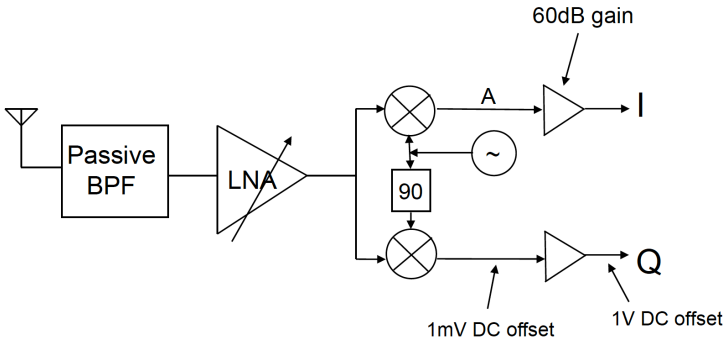


Figure 1-5 schematic diagram illustrating DC offset problem in ZIF receivers

Since the signal is converted down to DC, the signal path post mixer is DC coupled. This makes a slight DC offset to appear as volts and most likely to saturate the subsequent baseband circuitry. AC coupling is expensive since large AC coupling caps should be used to achieve low high pass corner (<1kHz). Also, any offset transients due to RF gain switching will result in a large DC transient that will take long time (few ms for a 1kHz corner) to settle. Two common techniques for DC offset removal: A) analog servo loops B) digital DC-offset calibrations

3. Sensitivity to second order distortion (IP2)

Let us assume two jammers separated by Δf

$$s1 = m_1(t)\cos(\omega_1 t)$$
$$s2 = m_2(t)\cos(\omega_1 + \Delta\omega)t$$
$$(s1+s2)^2 = \left[m_1(t)\cos(\omega_1 t)\right]^2 + \left[m_2(t)\cos(\omega_1 + \Delta\omega)t\right]^2 + 2m_1(t)m_2(t)\cos(\omega_1 t)\cos(\omega_1 + \Delta\omega)t$$
$$= m_1(t)^2 + m_2(t)^2 + m_1(t)m_2(t)\cos(\Delta\omega t)$$

It can be seen than the second order distortion in the receiver results in two low frequency distortion that folds into the desired signal after being down converted around DC:

1. The baseband modulation around the jammer carrier gets folded into baseband with twice bandwidth
2. The two jammers beat against each other and produce a component only Δf away from DC. If Δf is close enough, the IM2 distortion will fall into the desired signal band. Even if Δf does not fall within the desired signal band, it can be close

enough to clip the entire receiver if it does not get filtered out properly before it reaches the VGA. Note that *s2* can be a simple CW jammer in some systems

4. Sensitivity to 1/f flicker noise

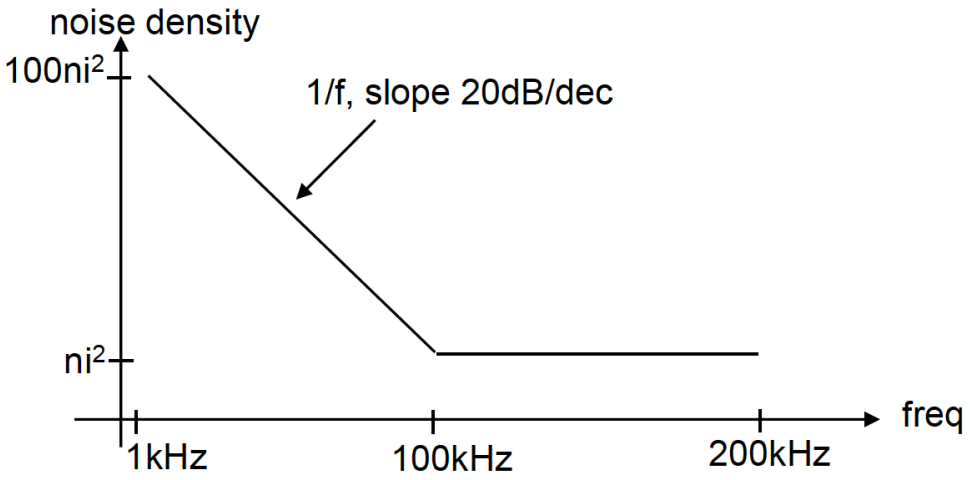


Figure 1-6 spectral noise density of CMOS transistor vs. frequency

Since the down converted signal is centered around DC (low frequency), the device 1/f noise becomes important. For example, if the 1/f noise corner of a GSM receiver is at half the desired signal bandwidth as shown above, the degradation this could cause to the effective noise is (assuming noise integration starting at 1kHz):

$$\overline{n_{ave}^2} = \frac{1}{200k}\left[\int_{1kHz}^{100kHz}\frac{a}{f}df + \int_{100kHz}^{200kHz} b\,df\right] \quad ; \quad \text{where } a = 1k\left(100\overline{n_i^2}\right); b = \overline{n_i^2}$$

$$\Rightarrow \overline{n_{ave}^2} = \frac{1}{200k}\left[a\ln\frac{100k}{1k} + b\left(200k - 100k\right)\right] = \frac{1}{200k}\left[11.5a + 100kb\right] = 6.25\overline{n_i^2}$$

This is a very challenging task in CMOS design given the relatively large 1/f noise corner compared to bipolar. Therefore, device sizing is necessary to bring the device 1/f noise corner to an acceptable level (< 0.5dB noise impact).

C. Low IF Receivers

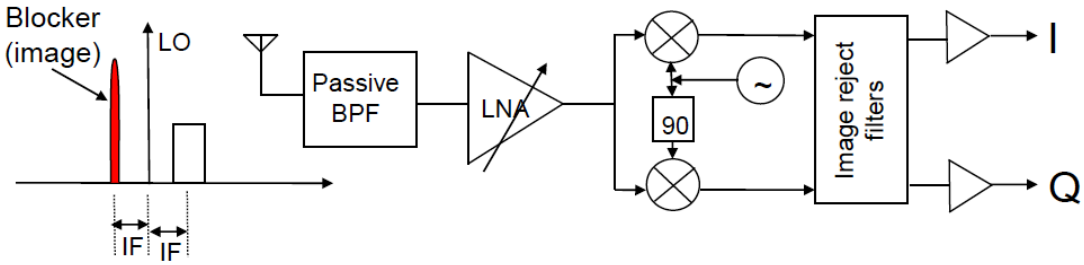


Figure 1-7 low IF receiver architecture

When LO frequency is shifted from RF frequency, signal around DC is avoided. The LO frequency is chosen such that IF is low enough so IF filters and circuitry can be integrated on chip, yet high enough to avoid the problems around DC in ZIF receivers. A typical low IF frequency is one or twice the signal bandwidth. Such architecture is conventionally named low IF receiver which is one type of super heterodyne architecture for receivers. The single quad architecture shown in figure 1-7 still suffers sensitivity of image rejection to phase and gain mismatch. A typical 35dB image rejection is not enough for most systems to be able to handle a large image signal with finite dynamic range integrated IF circuitry. Need IRR calibrations. The image rejection filters perform both channel selection and image rejection at the same time. The Low IF super

heterodyne is a popular architecture for systems with narrow-band signals that has large energy content close to DC (such as Bluetooth, GPS, and GSM).

D. Specifications

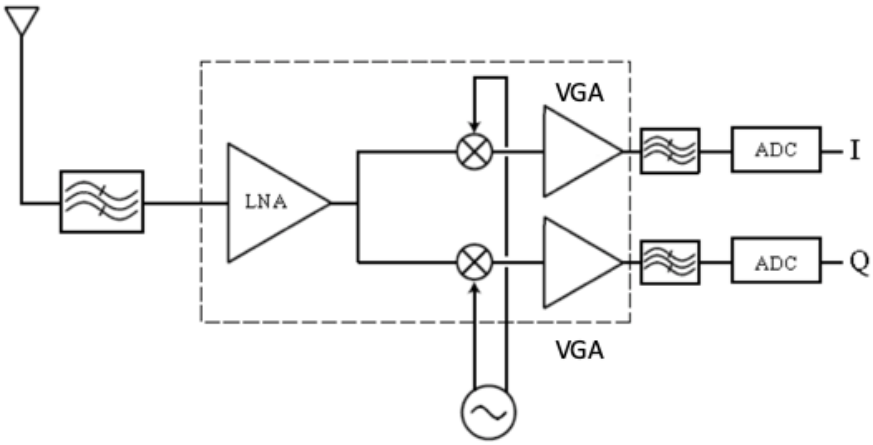


Figure 1- 8 low noise 2.4GHz receiver

The specification for chain of blocks in a dashed rectangle of figure 1-8 is listed in Table 1-1. These specifications will be used as guidelines for estimation of each block specification as will be discussed later in chapter 5.

Table 1-1 Receiver specification

Guideline Specification	Typical
Supply (V)	1
Band (GHz)	2.4 -2.5
Return Loss (dB)	< -15
Noise Figure (dB)	< 5
RF fixed Gain (dBV)	20 dB
Max gain (dBV)	80 dB
IIP2 (dBm)	> +10
IIP3 (dBm)	> -20
LO swing (mV)	300 guaranteed
IF pole	5 MHz

II. LOW NOISE AMPLIFIER

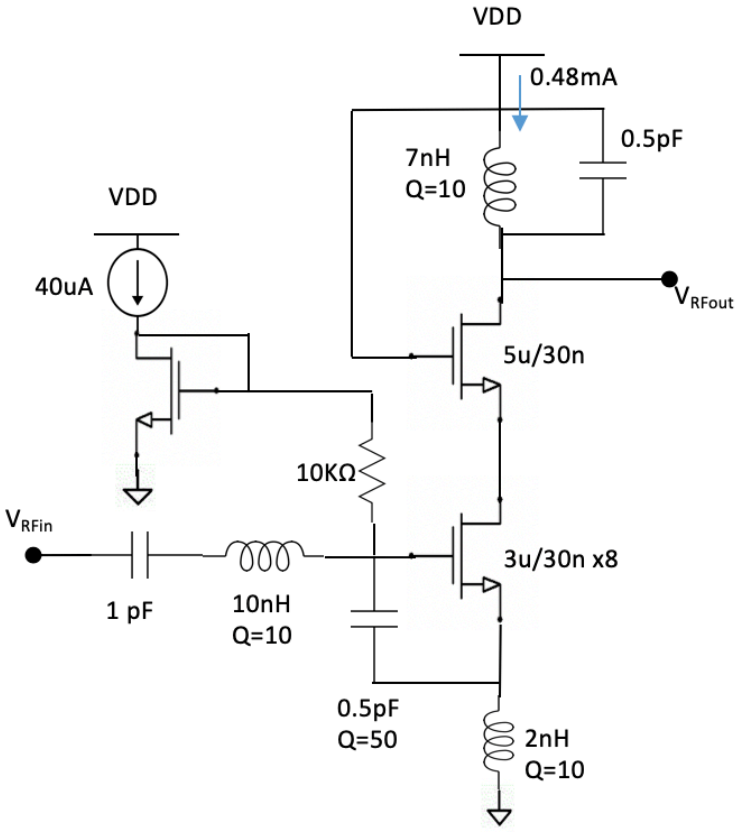


Figure 2-1. LNA Schematic Diagram

The low noise amplifier (LNA) circuit is shown in figure 2-1, where components values and transistor sizes are labeled. The common source architecture is selected because it offers superior low noise figure (NF) performance compared to others. Figure 3-1 shows NF performance overlaid with the NF_{min} vs. frequency. The NF is *3.6 - 3.8 dB* in *2.4 -2.5 GHz*, with zero difference from NF_{min} limit.

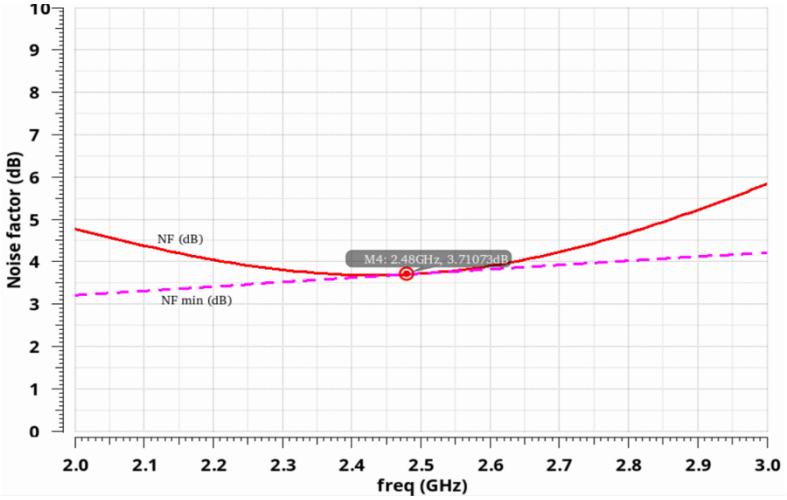


Figure 2-2. Noise figure performance vs. frequency: a) NF (solid line); b) NF_{min} (dashed)

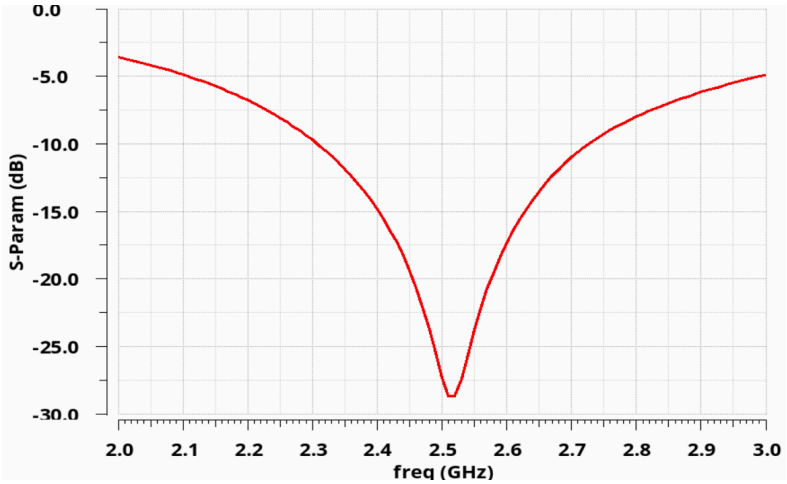


Figure 2-3. Input Reflection coefficient vs. frequency

In *2.4 -2.5 GHz,* the input reflection coefficient is < *-15 dB* in *2.4 -2.6 GHz*, whereas output impedance is ~1kΩ as shown in figure 2-3, 2-4 respectively. Since voltage signal is going to be used for link budget calculation of receiver blocks lineup, voltage gains will be only considered and presented, rather than power gain. Indeed, power matching for the LNA output as well as succeeding stages input/output is not of

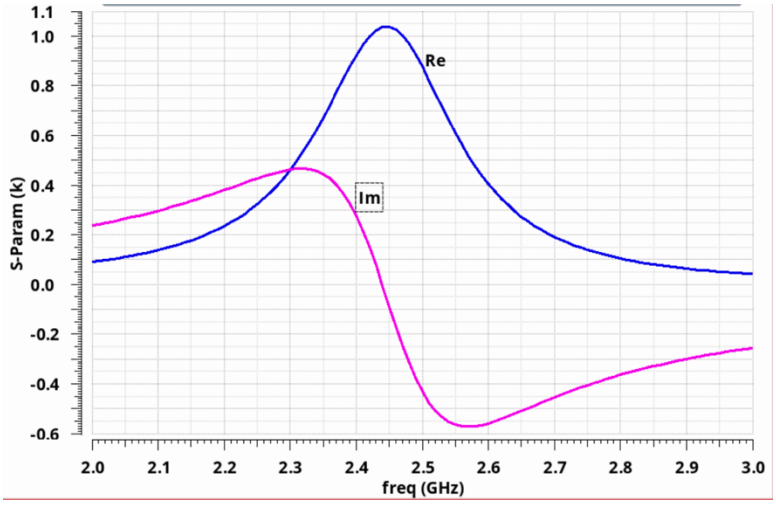


Figure 2-4. Output impedance of the LNA vs. frequency.

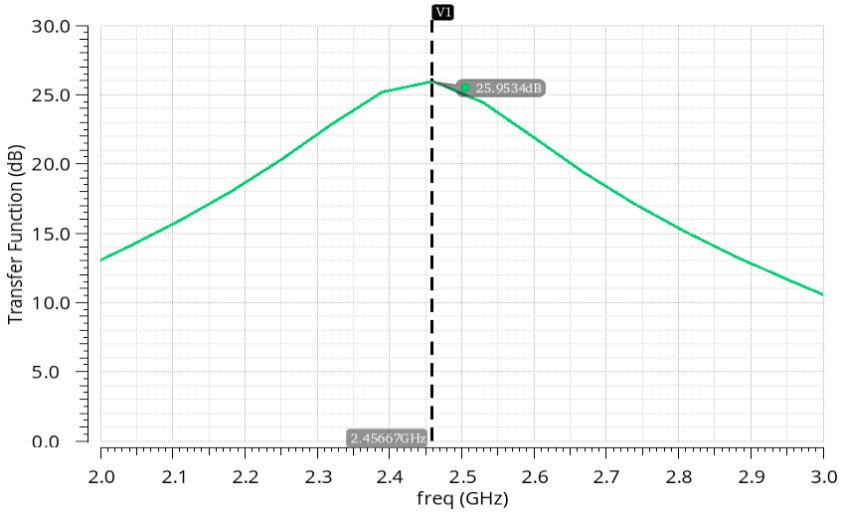


Figure 2-5. Voltage gain of LNA vs frequency.

concern. One exception is at the input of LNA, where power matching is necessary because signal at antenna port is a power signal and it is desired to accept the incident signal with minimal reflection or loss, which is the case as shown earlier in figure 2-3.

The LNA voltage gain, defined as V_{RFout}/V_{RFin}, is presented in figure 2-5. As could be

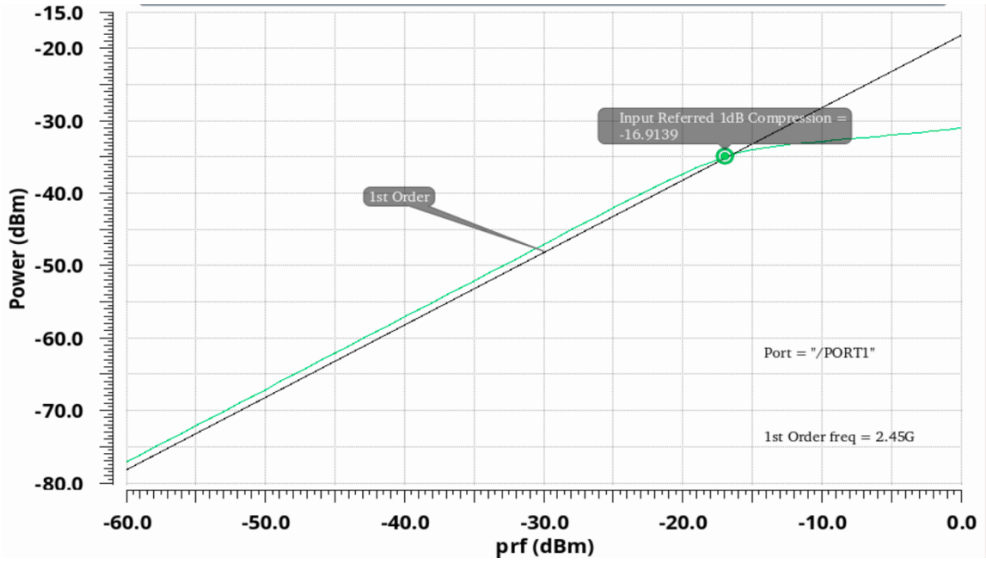


Figure 2-6. Output power vs. input power sweep

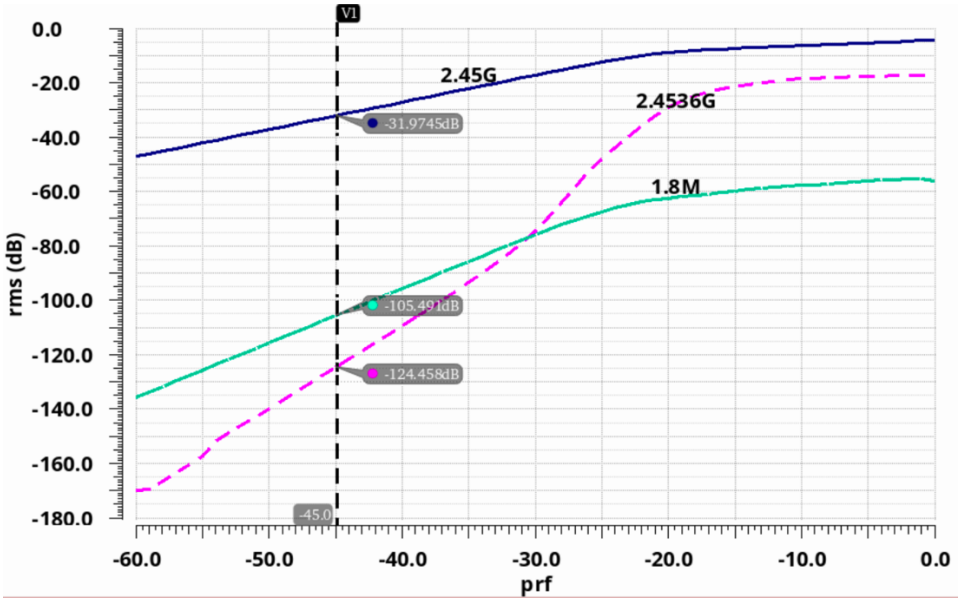


Figure 2-7. IM2 an IM3 products vs. input power sweep

observed the voltage gain is above 25 dB in 2.4 - 2.5 GHz. The LNA 1dB compression point (P1dB) is presented in figure 2-6, where output power is plotted versus input power sweep. As could be seen, the achieved input referred 1dB compression point is *-16.9 dBm*. The 2nd and 3rd order intermodulation products are swept with input power and plotted in figure 2-7. From calculation, IIP2 =28 dBm and IIP3 = 1.24 dBm.

The LNA input transistor is biased at $g_m/Id\ (V^{-1}) = 17.2\ V^{-1}$ with $I_d = 0.48mA$. Therefore, the power consumption is 0.48mW(with 1V supply), which is pretty decent given the achieved specification discussed above. A summary for LNA performance metrics is tabulated in Table 2-1.

Table 2-1. LNA metrics summary

Metric	**2.4 -2.5 GHz**
Supply (V)	*1*
Band (GHz)	*2.4 -2.5*
Return Loss (dB)	*< -15*
Noise Figure (dB)	*3.6 -3.7*
$R_{out}\ (\Omega)$	*~1k*
Id	*0.486*
Gain(dBV)	*26*
Id (mA)	*0.48*
$g_m/Id\ (V^{-1})$	*17.2*

III. MIXER

A. Architecture

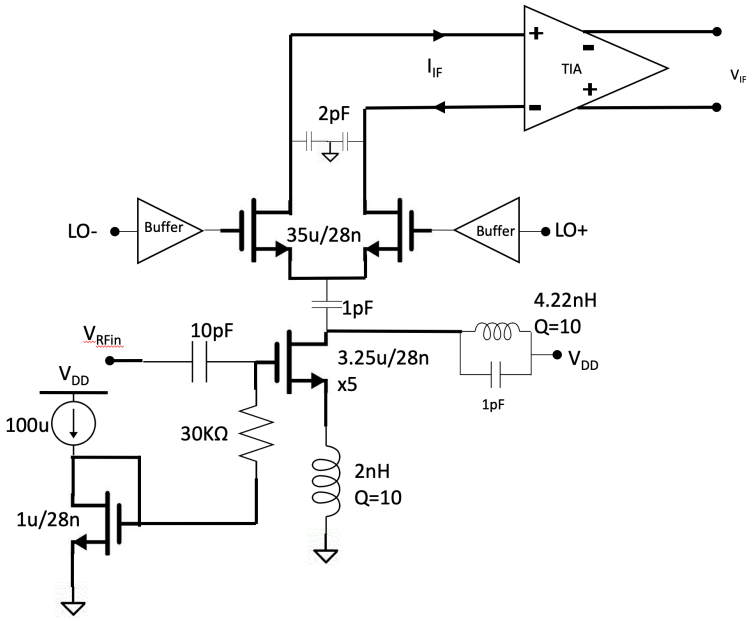


Figure 3-1. Single balanced current commutating mixer with its associated biasing circuits and LO buffer

A single balanced current commutating mixer topology is used as shown in figure 3-1. It consists of an input G_m stage to convert radio frequency (RF) input voltage into RF current. The RF current is then commutated with pair of switches, biased in triode region (passive switching) and controlled by local oscillator (LO) signal. Therefore, RF current is mixed and down converted to IF frequency at output of switches. It should be noted that body terminal for each transistor is by default connected to its source terminal unless explicitly shown in the schematic.

B. Buffer

The LO signal is assumed to be 0-300mV peak-to-peak guaranteed output from LO frequency divider, which is not enough to turn on the switching pair. Therefore, switches are driven through a buffer to raise peak-to-peak LO signal level to 1V with minimal rise and fall time. Tradeoff between attained rise/fall time vs. current consumed by buffer should be considered. Leveraging CMOS advantage in digital circuits, two stages CMOS inverter topology is adopted for buffer as shown in figure. 3-2.

The first stage is AC input coupled using *1pF* cap so that buffer biasing is independent of DC supply of LO generation circuit. *10KΩ* feedback resistor is included to self-bias the first stage to *VDD/2* and subsequently the second stage. Figure. 3-3 shows differential LO signal that comes out from frequency divider and the differential output signal from buffer that drives the switches. As could be seen the output signal peak-to-peak swing settles to *1V* at steady state, which is reached after the first few cycles. The real time supply current of buffer is plotted in figure 3-4, whose average is *0.17 mA*. Therefore, total of *0.32mA* is consumed for pair of buffers.

C. Mixer core

The core of mixer (GM stage + switching quad) could be studied by replacing TIA of Fig.3 with ideal OP-AMP + feedback

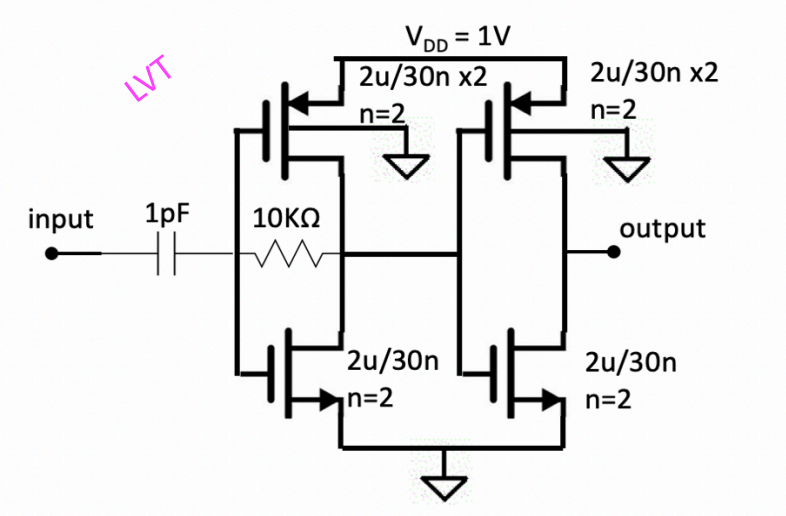


Figure 3-2. Buffer circuit for I/Q LO

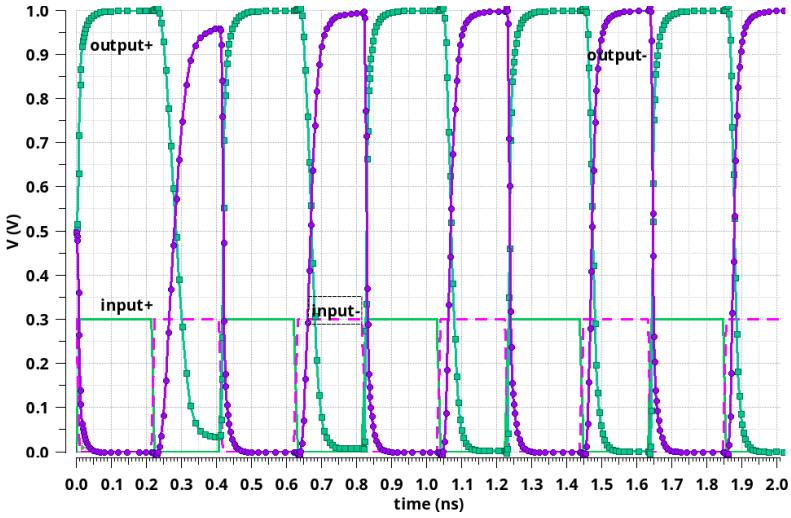


Figure 3-3. Differential input signal (no symbol) and output signal (square symbol) of the buffer

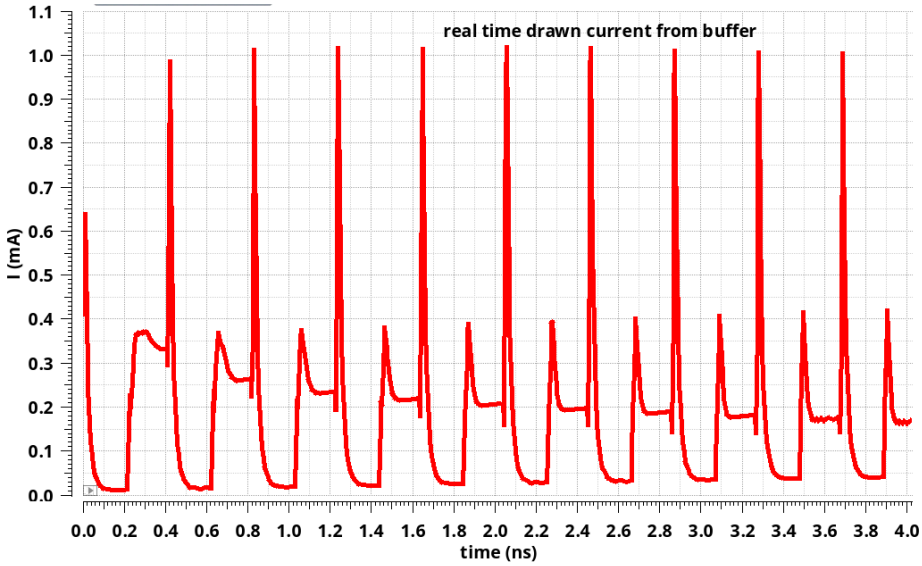


Figure 3-4. Real time supply current of buffer block

resistor. Such setup isolates noise and non-linearity impairments of TIA. For fixed bias current, the G_m stage (g_m/I_d) is very critical for mixer linearity and input referred noise. The higher g_m/I_d leads to large g_m and hence lower input referred noise. On the other hands higher g_m/I_d yields lower overdrive voltage and subsequently higher IM products and poor linearity. Therefore, trade-off between noise and linearity versus burnt power is necessary. $g_m/I_d = 8.35$ v^{-1} is chosen for mixer core to attain *IP3 = -5 dBVrms* as shown in figure 3-5, which is above margine by 5 dB. Note, IP3 will deteriorate with non-ideal TIA + variation over PVT.

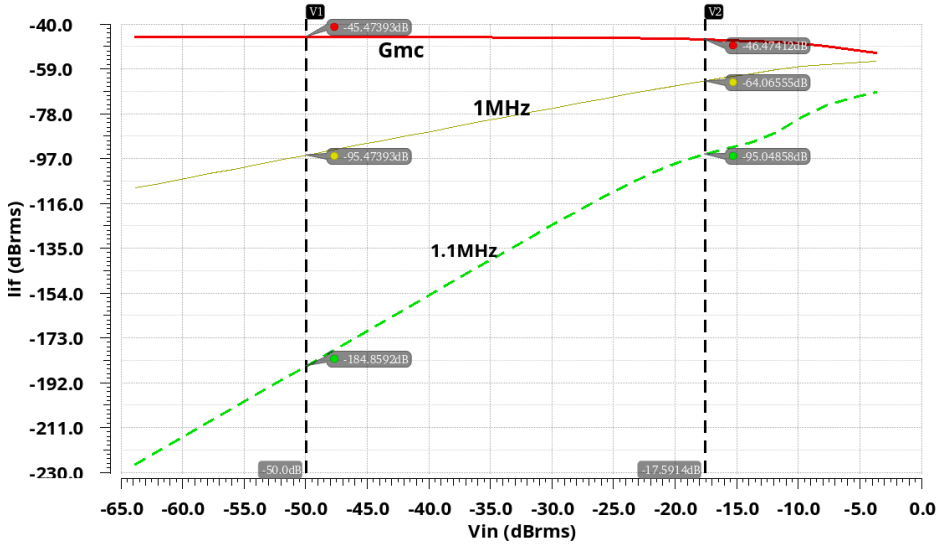


Figure 3-5. Core mixer (no TIA) output IF current for fundamental (1MHz) and IM3 (1.1MHz) along with conversion transconductance $G_{mc} = I_{if}/V_{RF}$

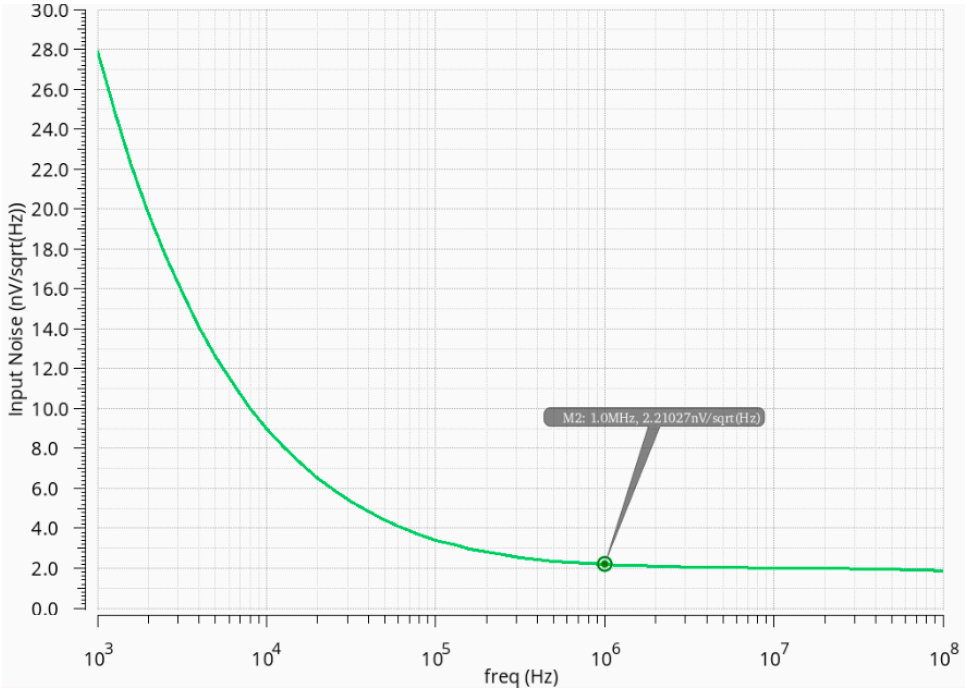


Figure 3-6. Input referred noise of core mixer (without TIA) in nV/√Hz at g_m =17.8mS

The conversion transconductance is also plotted in figure 3-5 at specific bias (discussed in next paragraph), where *P1dB = -17.6 dBVrms* is attained (1.5 dB above spec)

The equivalent input referred noise is shown in figure 3-6. From the figure, at 1MHz the noise is 2.2nV/√Hz with $g_m = 17.8\ mS$, leaving 3.8nV/√Hz spec margin for noise from TIA + variation over PVT. The bias current of Gm stage could be determined with known g_m *and* g_m/I_d such that:

$$I_d = \frac{g_m}{\frac{g_m}{I_d}} = 2.02mA$$

D. TIA

A current mode trans-imepdance amplifier shown in figure 3-7 is used as TIA, whose output load is $R_L = 1\ K\Omega$, therefore TIA Gain $R_T \approx 1K\Omega$. Dominant pole ~ $1/R_LC_L$ and could be set to 5MHz by adjusting C_L. The input impedance of TIA is desired to be minimal over frequencies of in-band IF signal as well as out of band blockers. $|Z_{in}|$ is shown in figure 3-8. As could be observed, the differential input impedance is < 175Ω and starts to decrease after few hundred MHz. This is an advantage for current mode TIA over voltage mode with shunt feedback, where input impedance quickly grows at frequencies approaching unity gain.

The current supplying above TIA is *4 x 0.45mA = 1.8mA* which is gross. The reason for this high current is the circuit topology, where TIA ac gain and DC output common

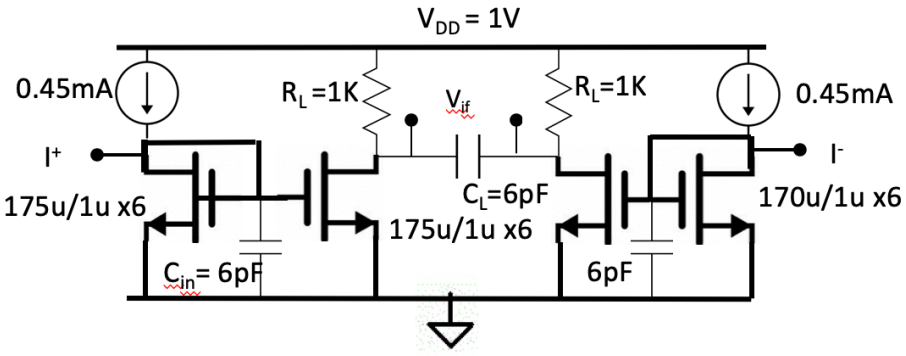


Figure 3-7. CMOS current Mode TIA

mode (CM) are dependent on output load resistor. In other words, the above circuit doesn't allow to control AC gain and DC CM independently. To overcome this problem current sources (active load) should be used instead of resistors along with a CMFB circuit to set the CM, whereas the load resistors connected to output through coupling

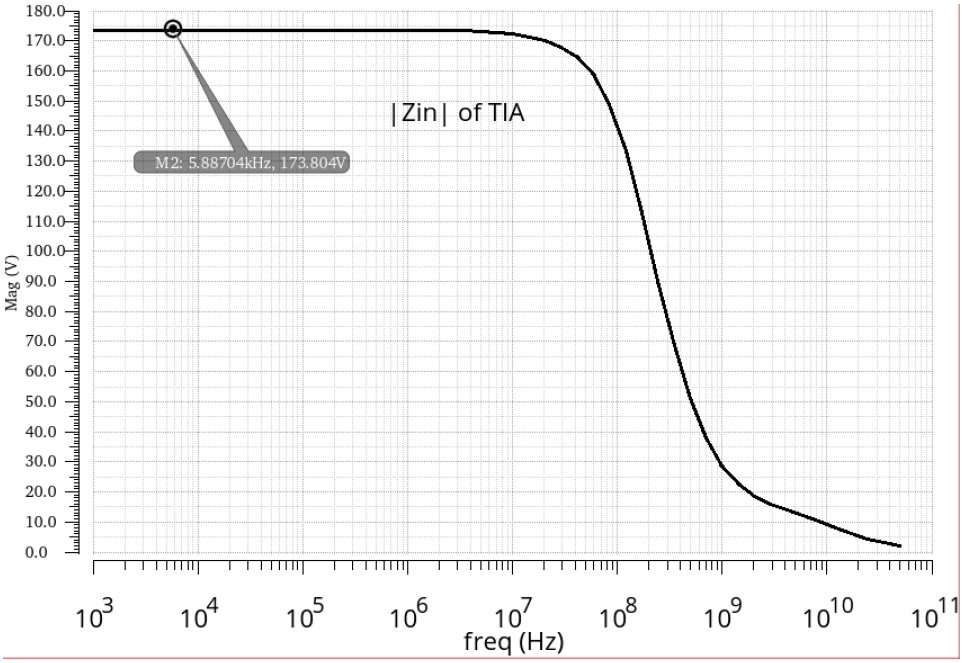


Figure 3-8. Differential small signal input impedance of TIA

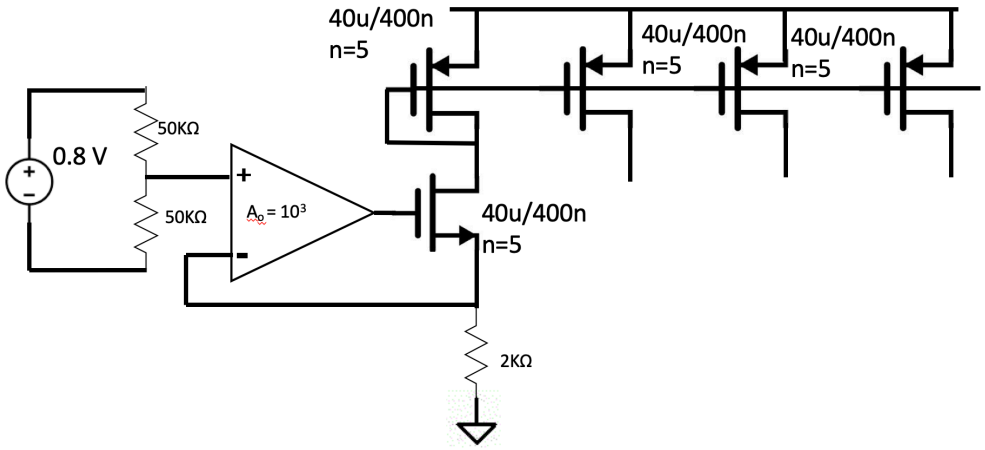


Figure 3-9. Current source generation from chip reference band gap voltage of 55nV/√Hz

capacitors. This way offers freedom to set AC gain independently of the CM and the total supply current could be remarkably reduced.

E. Biasing circuitry

The chip has one reference band gap voltage = 0.8V with 55nV/√Hz. The reference voltage is used to generate all the current sources used in the above presented circuits as shown in figure 3-9. Therefore, no ideal source is considered in this work except the VDD rail.

F. Mixer + TIA

The full Mixer + TIA along with buffer and biasing circuit associates in figure 3-1 are simulated as a whole and results are discussed below.

The mixer conversion gain (V_{IF}/V_{RF}) versus frequency is shown in figure 3-10. The achieved gain is 16.8 dB with first order IF pole at 5 MHz, where roll off is 20

dB/decade. Figure 3-11 shows the simulated input referred voltage noise of mixer. At 1MHz the input noise level is equal to 4.6nV/√Hz which is larger than noise of core mixer shown in figure 3-6 due to noise from TIA.

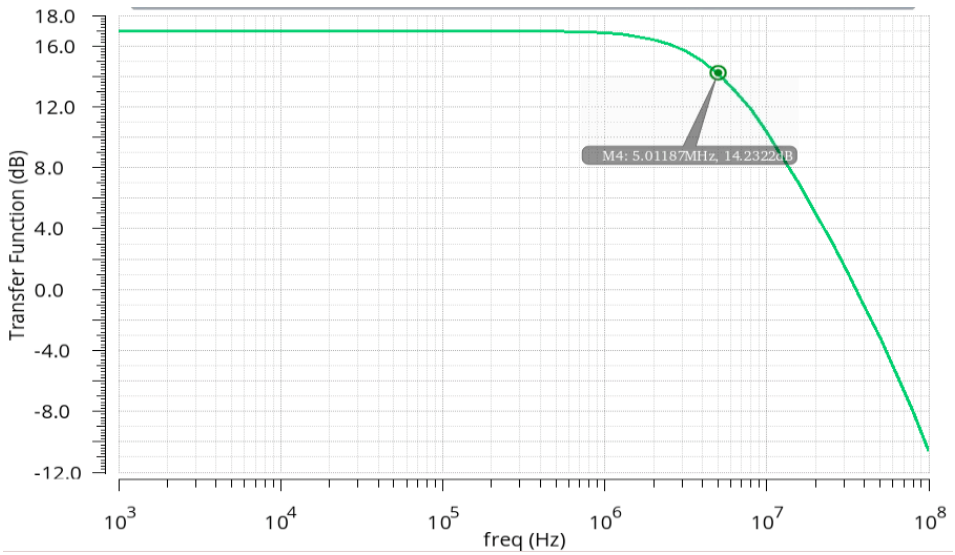


Figure 3-10. Mixer conversion gain (V_{IF}/V_{RF}) vs. frequency

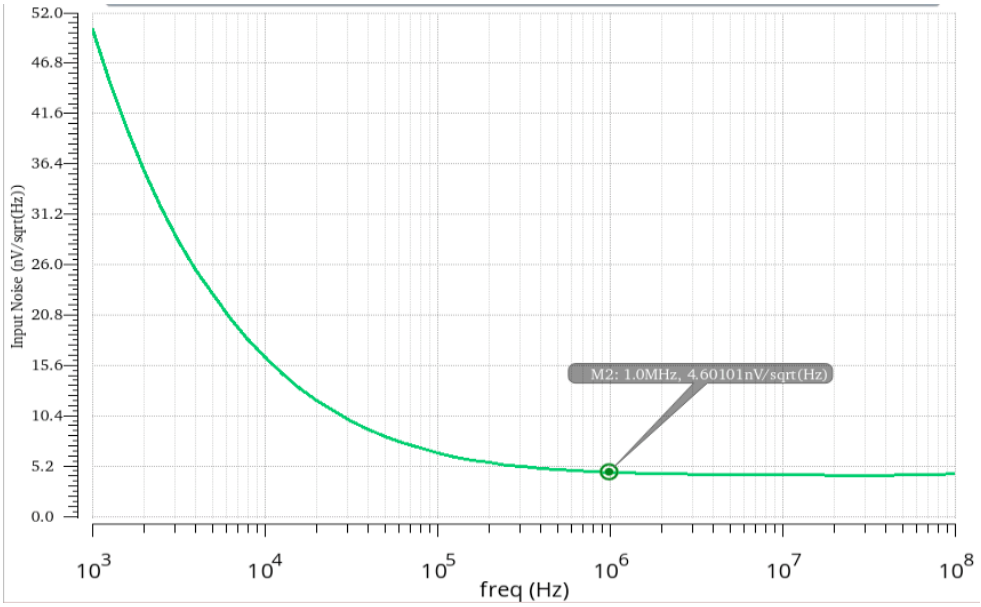


Figure 3-11. Mixer input referred voltage noise of whole

The mixer linearity performance is tested by injecting two tones at $f_1 = 2450.9$ and $f_2 = 2452$ MHz. Figure 3-12, shows curves for conversion gain, fundamental IF tone (1 MHz), and IM3 tone (1.1 MHz) versus input RF voltage. The input referred 1dB compression point is -22.7 dBVrms, whereas the IIP3 is -13 dBVrms. According to figure 3-5, the linearity performance is output limited.

The output DC offset due to transistor mismatch is estimated with Monte Carlo simulation and shown in figure3-13, where $3\sigma = 16.74$mV is observed.

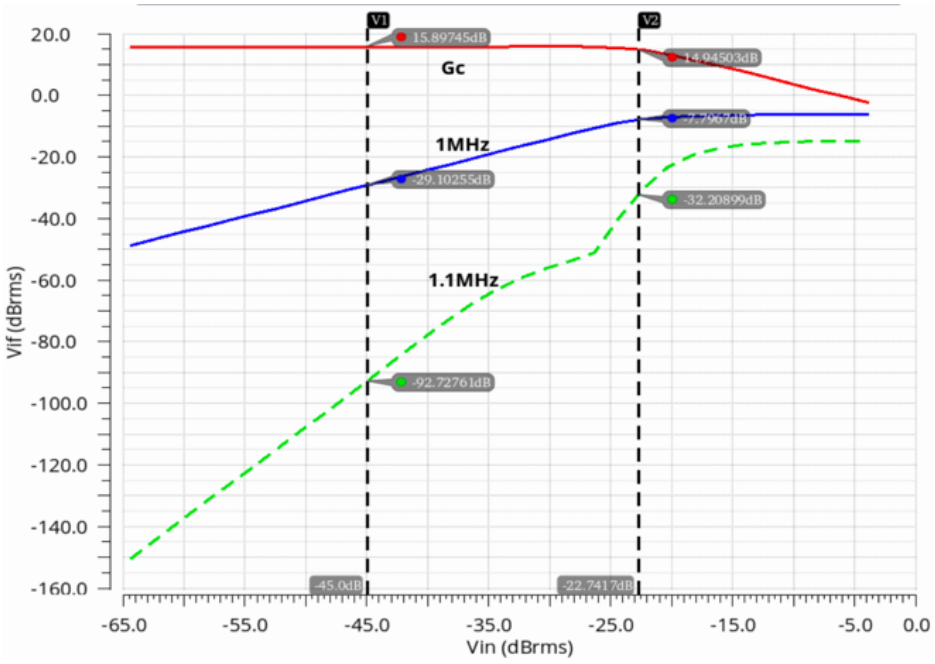


Figure 3-12. Mixer conversion gain, IF fundamental, and IM3 vs. input RF voltage.

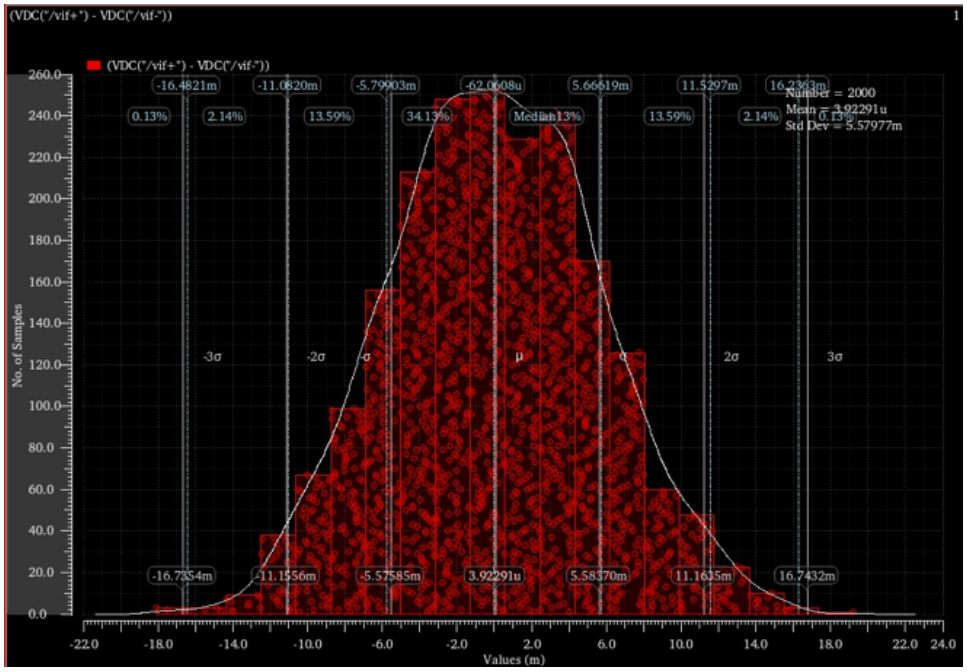


Figure 3-13. DC offset due to transistor mismatch

Table 3-1 Mixer +TIA metrics summary

Spec	Condition	min	typ	max	Achieved
f (GHz)	input	2.4		2.5	2.4 -2.5
IF (MHz)			0.9/1.8		0.9/1.8
VDD		1	1.2	1.32	1
Current (mA)	I+Q			3.5	8.52
Voltage Gain (dB)	RF to IF	13	15	17	15.8
Input referred noise (nV)	I or Q referred to RF input		5	6	4.6
OIIP3 (dBVrms)	15, 29 MHz	-12	-9		-13
OIIP2 (dBVrms)	25, 26 MHz	17			∞
IIP3 (dBVrms	In-band	-12	-9		-13
IP1dB (dBVrms)	In-band	-22	-19		-22.7
Mixer IF pole (MHz)		4	5	6	5.2
IF Output CM (mV)		550	600	650	550
DC offset (mV)	3σ			+12mV	16.74
I/Q Imbalance for IRR (dB)		30			NA

Summary for typical attained performance is tabulated in Table II. The P1dB, IIP3, and IIP3 due to blockers, are marginally below minimum spec by 1 dB because of limited voltage headroom at the output. At 1.2V supply voltage, the IIP3 increased to be -6 dBVrms. The current is grossly above budget and this is due to two reasons:

1- The circuit topology used for TIA has high current noise at its input because of direct connection to transistors drains. Therefore, drain noise currents directly appears at the TIA input without being scaled. Subsequently, larger current for mixer gm stage is needed to obtain higher gm which in turn reduces the input referred noise at mixer input because noise current get scaled by 1/gm at the mixer input.
2- The biasing scheme for TIA has AC gain and output DC CM dependent on R_L, leading to large biasing current for specific gain as discussed in section c.

One solution to overcome first problem is to use voltage mode CS topology with resistive feedback, where current noise is scaled by 1/gm. The second problem could be tackled by using current sources instead of R_L with CMFB circuit to set output CM as discussed in section c.

IV. CONCLUSION AND SUMMARY

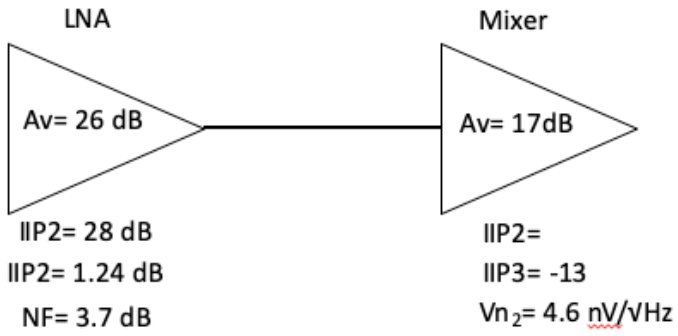


Figure 4-1 cascaded system of LNA and mixer discussed in chapter 2, and 3.

$$\frac{1}{IIP3} = \frac{1}{IIP3_{LNA}} + \frac{{Av_{LNA}}^2}{IIP3_{Mixer}} \rightarrow IIP3 = -39 \text{ dBVrms} = -26\, dBm \quad (1)$$

$$NF_{LNA} = 3.5dB \rightarrow 0.518\, nV/\sqrt{Hz} \quad (2)$$

$$NF_{tot} = 1 + \frac{V_{n1}^2 + \frac{V_{n2}^2}{Av_{lna}^2}}{4KTR_s\frac{1}{4}} \approx 2.56 \approx 4.1dB \quad (3)$$

The blocks (LNA, Mixer, and associated circuits) presented in previous chapters are cascaded as shown in fig. 4-1, where each block achieved specifications are labeled. The line-up IP3 and NF are calculated with equations (1) - (3) using blocks specification discussed in previous chapters and end results are tabulated in Table 4-1.

Table 4-1. Cascaded front-end system metrics summary

Spec	Guide	Achieved
IIP2 (dBm)	+ > 20	
IIP3 (dBm)	> -20	-26
NF (dB)	5	4.1 dB
S_{11} (dB)	< -15	< -20
DC offset (3σ)		16.7mV
VLO Leakage	< -100 dBm	< -177 dBm
Fixed Gain (dB)	20	37

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