Design of Negative Capacitance Field-Effect Transistor

Ming-Yen Kao

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2020-59
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2020/EECS-2020-59.html

May 25, 2020

Design of Negative Capacitance Field-Effect Transistor

by Ming-Yen Kao

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

Approval for the Report and Comprehensive Examination:

Committee:

Professor Chenming Hu
Research Advisor

April 27, 2020

(Date)

* * * * * * *

Professor Sayeef Salahuddin
Second Reader

(Date)

Contents

I. Introduction

Gordon Moore proposed Moore's law in 1975, and after that, the number of components per integrated circuit doubles every 12-24 months [1]. The fast downscaling of the transistor benefits the whole world in many ways, including communication electronics (like iPhone and Internet router), personal computer… However, the growth of exponential is difficult to maintain at the same growth rate forever. For example, the exponential growth of the bacteria would be limited by the resources finally. There is no exception for semiconductor industry. For a long time, metal-oxide-semiconductor field-effect transistor (MOSFET) benefits from scaling and increase of clock frequency. By scaling effective oxide thickness (EOT), the same charge density can be achieved at lower gate voltage. By reducing the gate length, the same current density could be achieved at lower drain voltage. Several great inventions, including H-K metal gate, immersion lithography, and FinFET, keep the scaling continuing on. Scaling of EOT and increase of clock frequency together increase the performance per area. Recently, scaling of EOT is slowed down because of physical limitation, including direct tunneling, oxide breakdown, and mobility degradation, and the increase of clock frequency is hindered by the difficulty of heat dissipation.

Negative Capacitance Field-Effect Transistor (NCFET) is a promising near future solution to the slowed down of EOT scaling. The scaling can be pushed a few more nodes if NCFET is properly designed. The theory of NCFET will be explained in the next section.

II. Theory of Negative Capacitance Field-Effect Transistor

Before explaining NCFET, let's start from how negative capacitance (NC) comes from. Fig. 1 (a) shows the energy of energy versus charge in ferroelectric (FE) and dielectric (DE) without external electric field [2]. The minimum energy of FE is not at zero charge, leading to the ferroelectricity (remanent polarization when there is no electric field). In contrast, the minimum energy of DE is at zero charge, and the shape is parabolic. If the FE is stacked on top of the DE, the total energy is plotted as the red curve in Fig. 1 (a). The equilibrium point is the small black ball at zero electric field, where the individual energy is not minimum for the FE, but the total energy of the system is minimum. Voltage is the derivative of energy with respect to the charge, and voltage versus charge plot is shown in Fig. 1 (b). Capacitance is the derivative of voltage with respect to charge, which is the slope in Fig. (b). The slope of the black curve in Fig. 1 (b) is negative, showing the negative capacitance within the red box.

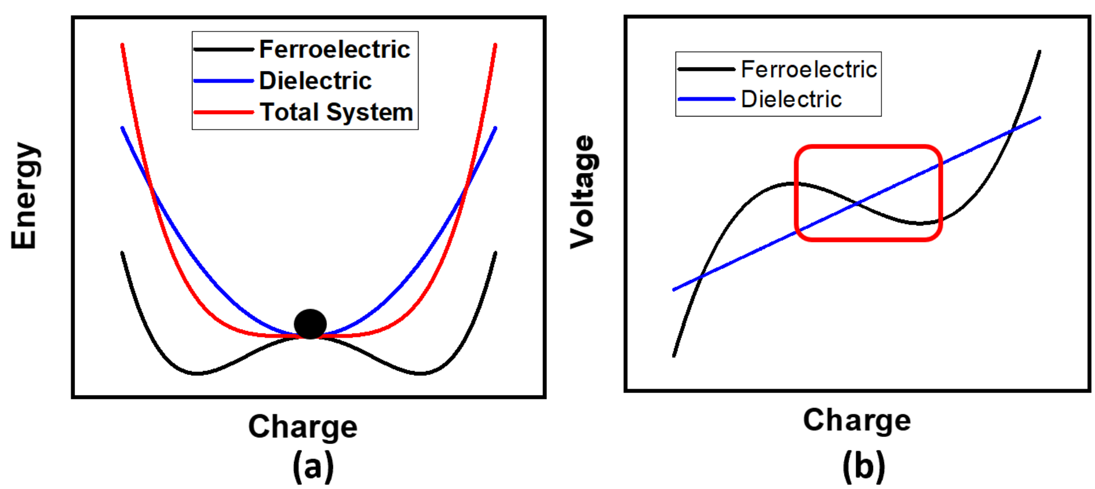


Fig. 1 (a) Energy versus charge plot of FE, DE, and the total system of FE and DE. (b) Voltage versus charge plot of FE and DE.

Fig. 2 shows the cartoon graph of a MOSFET. The capacitance from gate to channel can be simplified into two components, insulator capacitance (C_{ins}) and semiconductor capacitance (C_s). The total capacitance can be expressed as Eq. (1)

$$C_{total} = \frac{C_s C_{ins}}{C_s + C_{ins}} \quad (1)$$

If the value of C_{ins} is negative, C_{total} could be larger than C_s. It is even better than EOT -> 0 scenario. Another way to demonstrate the benefits of NCFET is by looking into the equation of subthreshold slope (SS) [3]:

$$SS = \frac{\partial V_g}{\partial(log_{10}I)} = \frac{\partial V_g}{\partial \varphi s} \frac{\partial \varphi s}{\partial(log_{10}I)} \quad (2)$$

The SS of the device is limited by two parts. The first part is $\frac{\partial V_g}{\partial \varphi s}$, which is determined by the capacitance divider as shown in Fig. 2.

$$\frac{\partial V_g}{\partial \varphi s} = 1 + \frac{C_s}{C_{ins}} \quad (3)$$

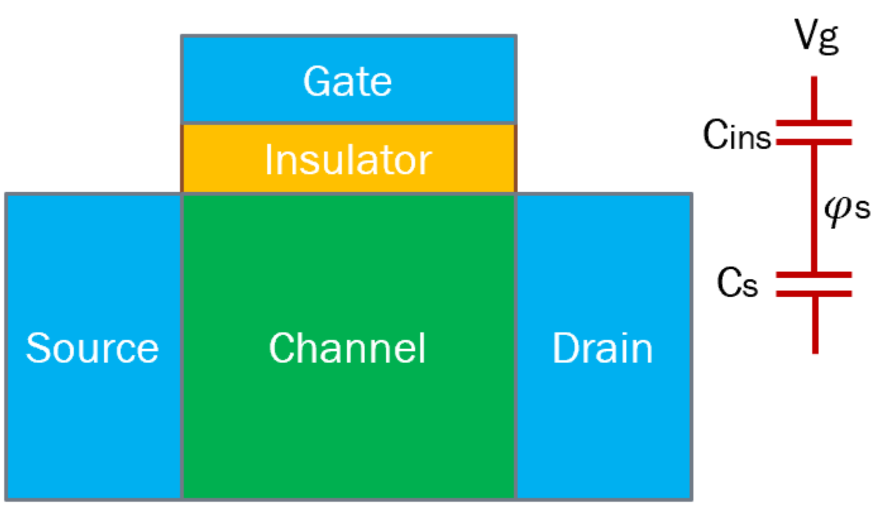


Fig. 2. Cartoon graph of a MOSFET.

From Eq. (3), $\frac{\partial V_g}{\partial \varphi s}$ is possible to be smaller than one if C_{ins} is negative. The second part is $\frac{\partial \varphi s}{\partial (log_{10} I)}$, which is limited by the current control mechanism of the transistor and the temperature. For the conventional MOSFET, the minimum value of $\frac{\partial \varphi s}{\partial (log_{10} I)}$ is about 60 mV/dec at room temperature, and that is why 60mV/dec is called Boltzmann Tyranny. NC can help to overthrow the Boltzmann Tyranny by providing gain to $\frac{\partial V_g}{\partial \varphi s}$.

III. Optimization of NCFET by Matching Dielectric and Ferroelectric Nonuniformly Along the Channel

A new design to overcome the nonuniformity of capacitance matching along the channel of a negative capacitance field-effect transistor (NCFET) is presented in this section. By introducing nonuniform oxidation, the thickness of SiO_2 at the edge regions of the channel can be increased while maintaining the thickness of SiO_2 at the center region of the channel. As a result, the capacitance along the channel becomes more uniform, and better capacitance matching between the dielectric (DE) and ferroelectric (FE) can be achieved. The Sentaurus TCAD results show improvement of matching in the center region and a significant boost of on-current (20% improvement).

A. Motivation

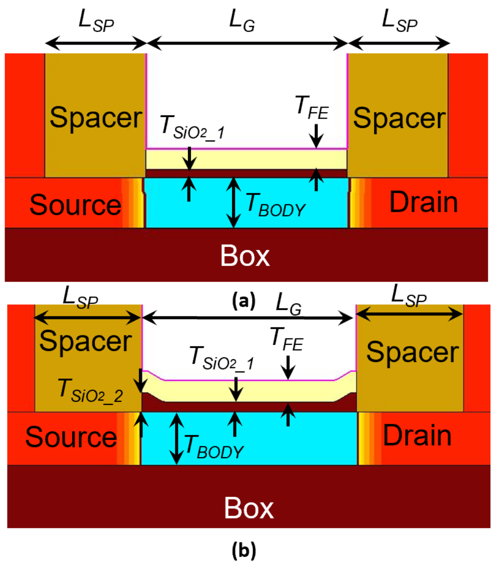
The fundamental limit imposed by the Boltzmann distribution (60 mV/decade) which hinders scaling of CMOS technology is referred to as the Boltzmann Tyranny [3]-[5]. Tunneling field-effect transistors (TFETs), nano-electromechanical (NEM) switches [6], and negative capacitance field-effect transistors (NCFETs) are promising ways to overcome the Boltzmann Tyranny [7]. However, the NEM switch is subject to reliability and scalability issues [5], while the TFET suffers from low on-current and other non-ideal effects [8]-[9]. NCFETs, on the other hand, can achieve an improved subthreshold slope (SS) while maintaining high on-current (compared to TFETs), and furthermore are fabricated through CMOS-compatible processes [10]. Many NCFETs have been made experimentally [10]-[15]. Nevertheless, many of them demonstrate a subthreshold swing (SS) of only 50-60 mV/decade without hysteresis and without an internal metal gate. An internal metal gate breaks the ferroelectric into multiple domains, causing hysteresis [16], and introduces other non-ideal effects like charge trapping which lead to problems during device operation. Despite this, NCFETs without an internal metal gate usually demonstrate worse performance than NCFETs with an internal metal gate [17] because of bad capacitance matching in the center region of the channel. A possible solution to this problem will be proposed in this study. Many papers have discussed the nonuniformity in electric field, nonuniformity in FE [18]-[21], and methods of improving the degree of capacitance matching [22]-[23].

In this study, the difficulty of further reducing the SS below 60 mV/decade of hysteresis-free NCFETs without an internal metal gate will be demonstrated in B (i) and B (ii). The fringing field from the source and drain plays an important role in the capacitance matching in the subthreshold region, but the fringing field also limits the capacitance matching at the center of the channel. A possible solution will be proposed in B (iii) to further improve the performance of NCFETs.

B. Device Characterization and Discussion

i. Baseline UTB-SOI Device Structure

The baseline structure and design parameters are shown in Fig. 3, but without the FE layer. The electric field at V_g = 0V and V_d = 0.7V is plotted in Fig. 4 (a). The electric field is stronger at the edges of the gate oxide, as indicated by the red circles. The stronger electric field at the edges is caused by both the inner-fringing field (passing through the Si channel) and outer-fringing field (passing through the Si_3N_4 spacer) [24], leading to nonuniform capacitance along the channel as shown in Fig. 4 (b) and imposing the



Parameter	Value
Gate Length (L_G)	20 nm
Spacer Length (L_{SP})	10 nm
Body Thickness (T_{BODY})	5 nm
SiO2 thickness at Center (T_{SiO2_1})	0.9 nm
SiO2 thickness at Edge (T_{SiO2_2})	1.8 nm
Supply Voltage (V_{DD})	0.7 V
FE Thickness (T_{FE})	2 nm
Baseline ON Current (I_{ON})	429 μA/μm
Baseline OFF Current (I_{OFF})	188 pA/μm
Baseline Subthreshold Slope (SS)	80.3 mV/dec
Basline Threshold Voltage (V_{TH})	327.5 mV

Fig. 3. The simulated device structure with (a) uniform thickness of interfacial layer and with (b) nonuniform thickness of interfacial layer. Table on the right-hand side lists important device parameters. The shaded parameters are for the baseline device. The baseline device has the same structure as (a), but without an FE layer.

limitation on capacitance matching. Note that the capacitance shown in Fig. 4 (b) is from the structures with an FE layer, and the vertical electric field in the SiO_2 (perpendicular to the FE) right below the FE layer is used to extract the nonuniform C_{mos} by using Eq. (4) from the TCAD results.

$$C_{mos} = \frac{dQ}{dV} = \frac{d(E_{\perp FE} \times \epsilon_{SiO2})}{dV(x)} \quad (4)$$

where $E_{\perp FE}$ is the electric field perpendicular to and right below the FE, ϵ_{SiO2} is the permittivity of SiO_2, and $dV(x)$ is the step size of electric potential at the interface of SiO_2 and FE as a function of position along the channel. To avoid hysteresis, the data in Fig. 4 (b) is extracted at $V_g = 0.7V$ and $V_d = 0.7V$, where the minimum absolute value of FE capacitance is not smaller than any value of the curve.

ii. Uniform interfacial layer NCFET

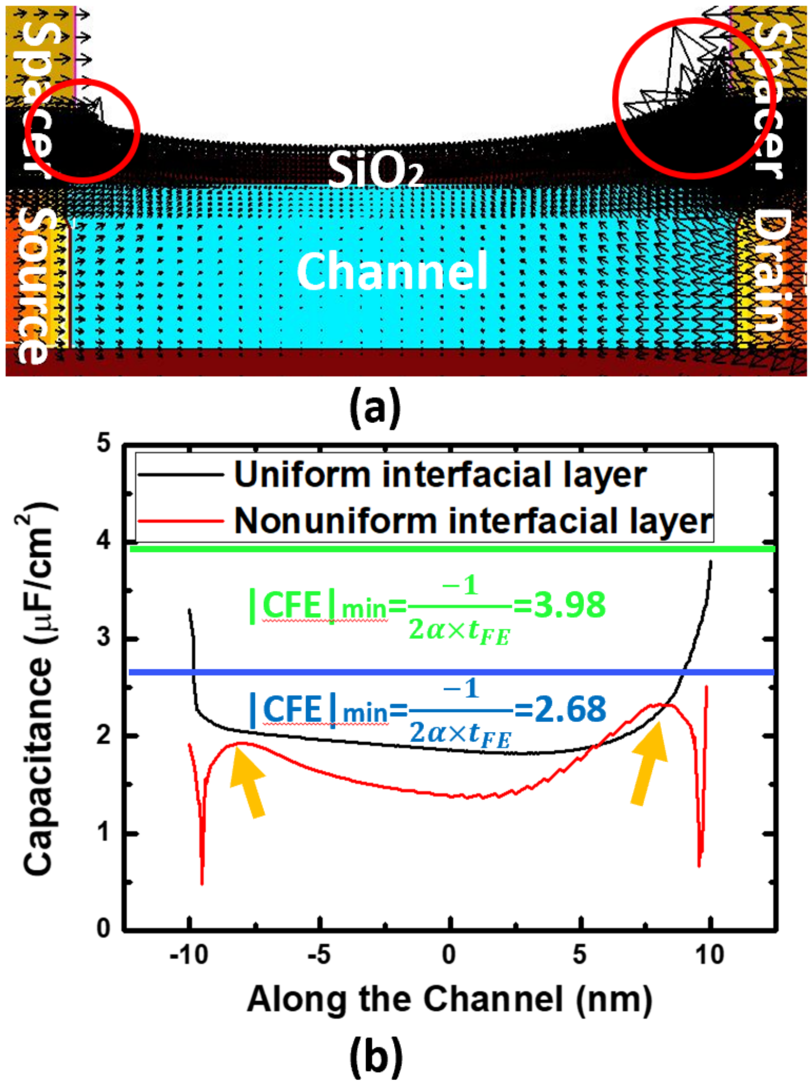


Fig. 4. (a) The electric field at V_g = 0V and V_d = 0.7V. The red circles highlight the higher electric field at the edges of the channel. (b) Capacitance versus position along the channel at V_g = 0.7V. The green line and the black curve are the traditional capacitance matching design, and the blue line and the red curve are our proposed capacitance matching design.

In traditional NCFET design, a uniform thickness of the interfacial layer along the channel is assumed, and the corresponding ferroelectric capacitance (C_{FE}) is matched to its limit with C_{mos}. In HfO_2-based NCFETs, the remanent polarization (P_r) is more sensitive to ferroelectric doping concentration than coercive field (E_c) [25]. Therefore, E_c is fixed to 2MV/cm, and P_r is decreased until C_{FE} touches the largest C_{mos} along the channel. The smallest P_r reached in the TCAD simulation is 11.5 μC/cm^2, which is equivalent to -3.98 μF/cm^2 (dielectric constant = 16 is included from [26]) by using Eq. (5). The physics models used in TCAD include the Ginzburg-Landau model for ferroelectric materials, Fermi Statistics, velocity saturation, Philips unified mobility model, Shockley-Read-Hall process, and quantum potential [27]. The Ginzburg-Landau model is shown in Eq. (6).

$$C_{FE} = \frac{1}{2\alpha t_{FE}} + \frac{16\varepsilon_0}{t_{FE}} \quad (5)$$

$$\mathrm{E} = 2\alpha \mathrm{P} + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho\frac{dP}{dt} \quad (6)$$

In Eqs. (5) and (6), |CFE| is the estimation of the minimum absolute value of FE capacitance; t_{FE} is the thickness of the FE; $\varepsilon_0$is vacuum permittivity; α, β, γ are the parameters for the FE; g is the strength of the polarization gradient (domain coupling) which is set to be 8E-5 cm^3/F in this study (on the same order as [27]); and ρ is the viscosity that represents the finite time required for the polarization to switch. α, β, and γ are related to P_r and E_c by $\alpha = -\frac{3\sqrt{3}}{4} \times \frac{E_c}{P_r}$ and $\beta = \frac{3\sqrt{3}}{8} \times \frac{E_c}{{P_r}^3}$, and $\gamma = 0$ [29]. K. Chatterjee et. al. reports that the intrinsic delay of a doped hafnium oxide-based ferroelectric is negligible in digital circuits [30], so ρ is set to be zero in this study.

iii. Proposed nonuniform interfacial layer NCFET

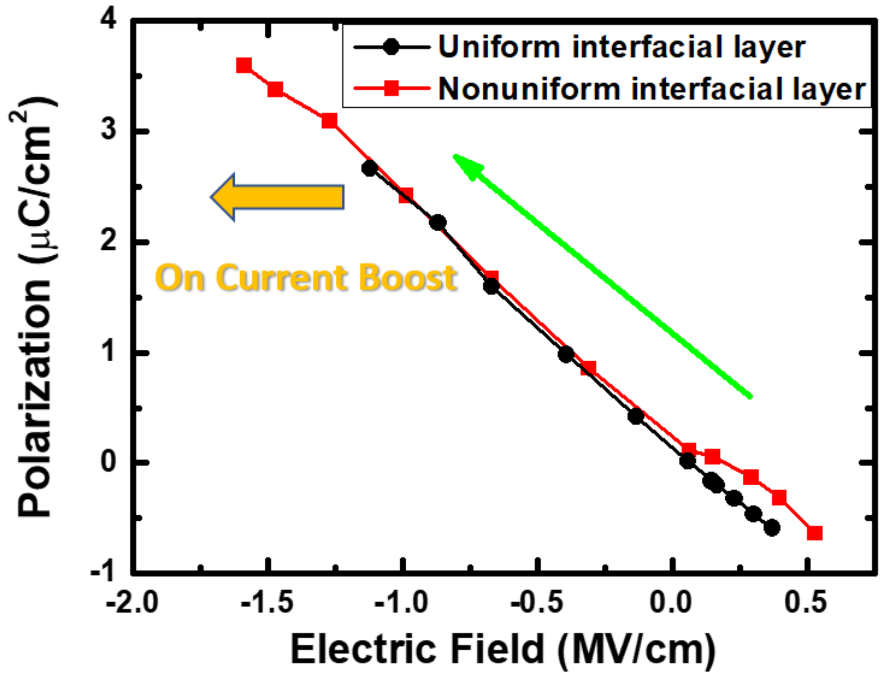


Fig. 5. Polarization and electric field of the FE right above the top of barrier (TOB). The transition from bottom right (deamplification) to upper left (amplification) represents the change of the state of the FE from Vg = 0V to Vg = 0.7V.

An NCFET with a nonuniform interfacial layer is proposed as shown in Fig. 3 (b). By tuning the thermal gradient or by introducing mask oxidation techniques during processing, a thicker SiO_2 can be grown at the edge regions of the channel without affecting the thickness of the SiO_2 at the center region of the channel. The P_r of the FE is now reduced to 10.1 μC/cm^2, which is equivalent to -2.68 μF/cm^2 (using dielectric constant = 16 from [24]) by using Eq. (5). The improvement from the perspective of polarization and electric field in the FE is shown in Fig. 5. Note that the metal gate work functions of the two cases are shifted to match the off-current of the baseline, so at $V_g = 0$ V (bottom right), there is not much difference in the bias points. At $V_g = 0.7$

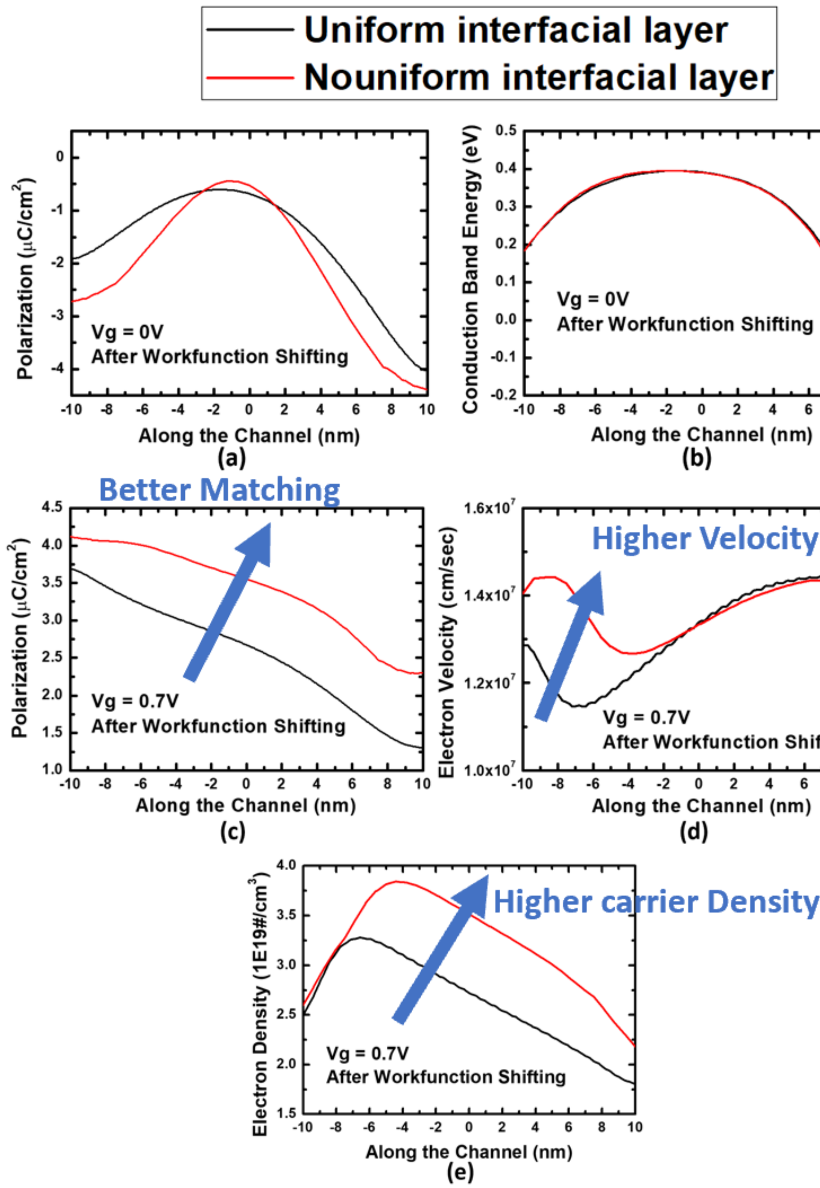


Fig. 6. (a) Polarization and (b) conduction band energy versus position along the channel in the off-state. (c) Polarization, (d) electron velocity, and (e) electron density versus position along the channel in the on-state. The black curves represent an NCFET with uniform thickness of the interfacial layer. The red curves represent an NCFET with a thicker interfacial layer at the edges of the channel.

V, the bias point of the proposed NCFET demonstrates an improvement via a left-shift as indicated by the yellow arrow (more voltage amplification).

Fig. 6 (a) plots polarization versus position along the channel at V_g = 0V (off-state). The profile of FE polarization changes because the capacitance matching condition along the channel changes. Fig. 6 (b) shows conduction band energy versus position along the channel. The barrier heights are the same because the metal gate work function is shifted to match the off-current of the baseline. Note that the position of the TOB is at the middle of the channel, which is why the matching between the FE and DE in the center of the channel is also critical. Fig. 6 (c) shows the FE polarization which is higher in the NCFET with nonuniform interfacial layer (more voltage amplification) compared to the normal NCFET. Fig. 6 (d) and 6 (e) show the carrier density and carrier velocity at a depth where the carrier concentration is highest (which is not close to the surface due to the quantum confinement effect). At the source side, a higher current can be supported by higher electron velocity, which can be seen in Fig. 6 (d). On the other hand, carriers at the drain side have already reached velocity saturation, so the carrier concentration increases more significantly near the drain side, as shown in Fig. 6 (e). It is evident from Fig. 7 that the proposed NCFET has better ON current (20% improvement) and better SS (minimal SS is 33 mV/decade). In Fig. 7, there are two bias points which show a surge in current. The first is around 0.265V and the second is around 0.615V. Better capacitance matching happens at these two gate voltages. Areas with better capacitance matching are indicated by two gold arrows in Fig. 4 (b). Better capacitance matching over the two areas accounts for the surge in current of the blue curve in Fig. 7 at 0.265V (which corresponds to the left hump of the red curve in Fig. 4(b)) and at 0.615V

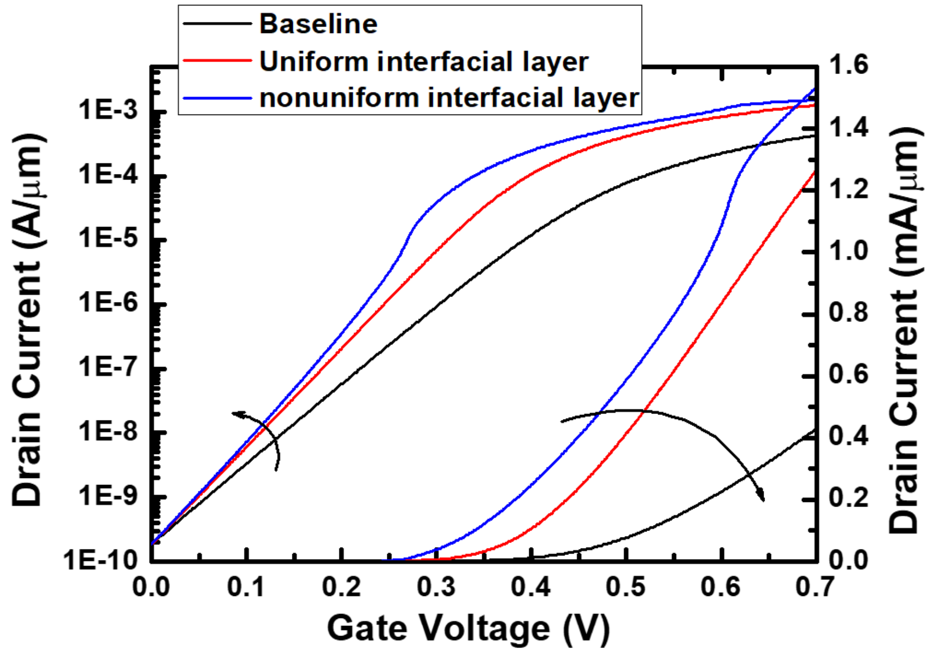


Fig. 7. Drain current versus gate voltage of baseline UTBSOI, traditional uniform-interfacial-layer NCFET, and proposed nonuniform-interfacial-layer NCFET.

(which corresponds to the right hump of the red curve in Fig. 4(b)). Note that these three cases are confirmed to be hysteresis-free by running the transient forward and reverse sweeping test. In comparison, the traditional design has no surge of current because the "good matching" parts are not in the channel and therefore contribute little current to the channel.

C. Section Summery

The difficulty of capacitance matching due to the nonuniformity of capacitance along the channel is pointed out first in Fig. 4. To overcome this difficulty, a new design scheme utilizing a thicker interfacial SiO2 at the edges of the channel is proposed. The results show that the performance of the NCFET can be significantly boosted with this scheme. Therefore, the nonuniform capacitance caused by fringing fields should be taken into consideration when NCFETs are designed.

IV. Variation Caused by Spatial Distribution of Dielectric and Ferroelectric Grains in a Negative Capacitance Field-Effect Transistor

A new scheme to consider the dielectric (DE) phases inside polycrystalline ferroelectric (FE) materials will be proposed in this section. The scheme is used to extract material parameters from experimental Polarization-Electric Field (P-E) measurements from the literature. A Sentaurus TCAD structure is constructed with the extracted parameters, and the simulated P-E curve is in good agreement with experimental data. Furthermore, variation of the device performance in a negative capacitance field-effect transistor (NCFET) due to the spatial distribution of DE and FE phases is studied using Sentaurus TCAD. It is found that the resultant variations of ON and OFF currents can be up to 14.44% and 30.23%, respectively, thus showing the impact of inhomogeneous crystalline phases of the FE material on device performance.

A. Motivation

As CMOS technology is aggressively scaled, power consumption becomes the most critical issue. To mitigate this issue, high mobility channel materials and three-dimensional transistors have been explored [31], [32]. However, the Boltzmann distribution poses a fundamental limit for lowering the energy dissipation in conventional electronics, and this limit is often referred to as the Boltzmann Tyranny [3]-[5], [9]. Negative capacitance FETs (NCFETs) are promising devices to overcome the subthreshold swing limit (60 mV/decade) imposed by the Boltzmann Tyranny and to achieve high Ion [3], [11]-[13], [33]-[39]. Although NCFETs experimentally exhibit sub-60 mV/decade performance [10]-[15], the non-uniformity effects of phases inside the ferroelectric (FE) haven't been investigated. To properly design NCFETs, the non-uniformity effects of phases should be carefully addressed. For example, X-ray diffraction (XRD) experimental data of HfO_2-based ferroelectric thin films [10] shows that, other than the ferroelectric orthorhombic phase, there also exist cubic and monoclinic phases, which are dielectric (DE). Lun Xu et al. also reported the existence of monoclinic phases in ferroelectric HfO_2 films [40]. In previous work [41]-[42], the ferroelectric layer is assumed to be homogeneous so that its properties can be solely predicted by the Landau equation in the simulation, which fails to consider the essential physics in real devices.

In this section, we investigate how the locations of the dielectric grains affect the behavior of NCFETs using Sentaurus TCAD after extracting the material parameters from experimental data. The percentage of the dielectric phase in the ferroelectric is assumed to be the same under the same process conditions, but the position of the dielectric grains vary, which further affects the behavior of NCFETs. This random dielectric distribution imposes an additional variation on top of the variation from fabrication, and this variation should be properly understood to evaluate and minimize the impact on NCFET performance.

B. Device Characterization

i. Ferroelectric parameters extraction

Symbol	Quantity	Unit
DE %	33.3	%
FE %	66.7	%
α	-5.810E+10	cm/F
β	3.286E+19	$cm^5/(F \cdot C^2)$
γ	2.165E+28	$cm^9/(F \cdot C^4)$
P_0	0.307	$\mu C/cm^2$
E_0	0.185	MV/cm
ε_r	16.38	unit less

Table I. Hysteresis loop fitting results

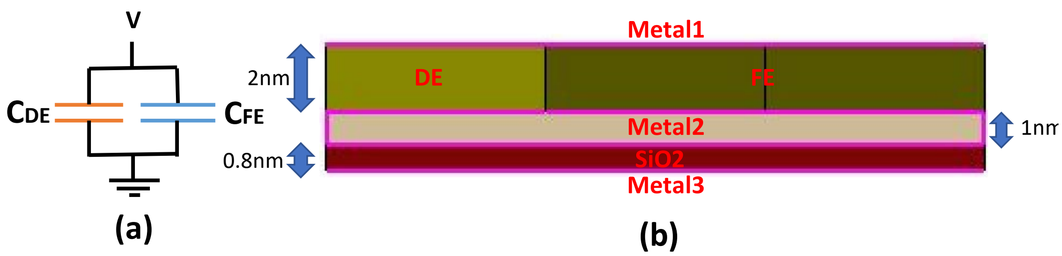


Fig. 8. (a) The circuit model used in Eq. (7) to (13) (b) MFMIM structure for TCAD

To set up the NCFET simulation using Sentaurus TCAD, the measured hysteresis loop of a 10nm ferroelectric from [14] is used to extract the ferroelectric parameters. As mentioned earlier, there are dielectric grains in the ferroelectric thin film, so only using the Landau equation to fit the hysteresis loop is insufficient. The expression for the Polarization-Electric Field (P-E) relation should include a dielectric component in addition to the Landau equation in the simulation. The model therefore should consist of a negative capacitor and a positive capacitor in parallel (Fig. 8 (a)). Note that the dielectric response is incorporated into the model to extend the sixth-order-polynomial approximation of Landau theory which has limited fitting capability in positive capacitance regions (the first and the third quadrants). This value of the dielectric constant is assumed to be the same as in DE grains.

Therefore, the polarization for a ferroelectric-dielectric-mixed thin film can be expressed as the following equations:

$$E_{FE} = 2\alpha \times P_{LD} + 4\beta \times {P_{LD}}^3 + 6\gamma \times {P_{LD}}^5 \quad (7)$$

$$\mathrm{P_{FE}} = P_{LD} + \mathrm{E_{FE}} \times \varepsilon_r \times \varepsilon_o \quad (8)$$

$$\mathrm{E_{mix}} = E_{FE} \quad (9)$$

$$\mathrm{P_{mix}} = Area_{DE} \times \mathrm{E_{mix}} \times \varepsilon_r \times \varepsilon_o + Area_{FE} \times P_{FE} \quad (10)$$

where E_{FE} is the electric field across negative capacitance; α, β, and γ are Landau coefficients; P_{LD} is the polarization of ferroelectric given by Landau Equation; $\mathrm{P_{FE}}$ is the polarization of FE part with built-in dielectric constant; ε_r is the dielectric constant; ε_o is the permittivity of vacuum; $\mathrm{E_{mix}}$ is the electric field across the thin film; $\mathrm{P_{mix}}$ is the total polarization with units of C/cm^2; $Area_{DE}$ and $Area_{FE}$ are the area percentages of DE and FE in total area.

Two assumptions have to be made in order to properly extract the material parameters. It is assumed that the ferroelectric layer consists of 66.7% ferroelectric grains and 33.3% dielectric grains: a reasonable assumption because it has been reported [40] that the percentage of the monoclinic phase inside HfO2-based ferroelectric layers can range from 10% to 50%, depending on the processing conditions; and furthermore, there are cubic, tetragonal, and orthorhombic-dielectric phases possibly coexisting in the ferroelectric thin film. Another assumption is that the dielectric constants of all the grains are the same. Based on these assumptions, we can rewrite the polarization equation from (7), (8), (9) and (10):

$$E_{mix} = 2\alpha \times (P_{LD} - P_0) + 4\beta \times (P_{LD} - P_0)^3 + 6\gamma \times (P_{LD} - P_0)^5 + E_0 \quad (11)$$

$$\mathrm{P_{FE}} = P_{LD} + \mathrm{E_{mix}} \times \varepsilon_r \times \varepsilon_o \quad (12)$$

$$P_{mix} = 33.3\% \times E_{mix} \times \varepsilon_r \times \varepsilon_o + 66.7\% \times P_{FE} \quad (13)$$

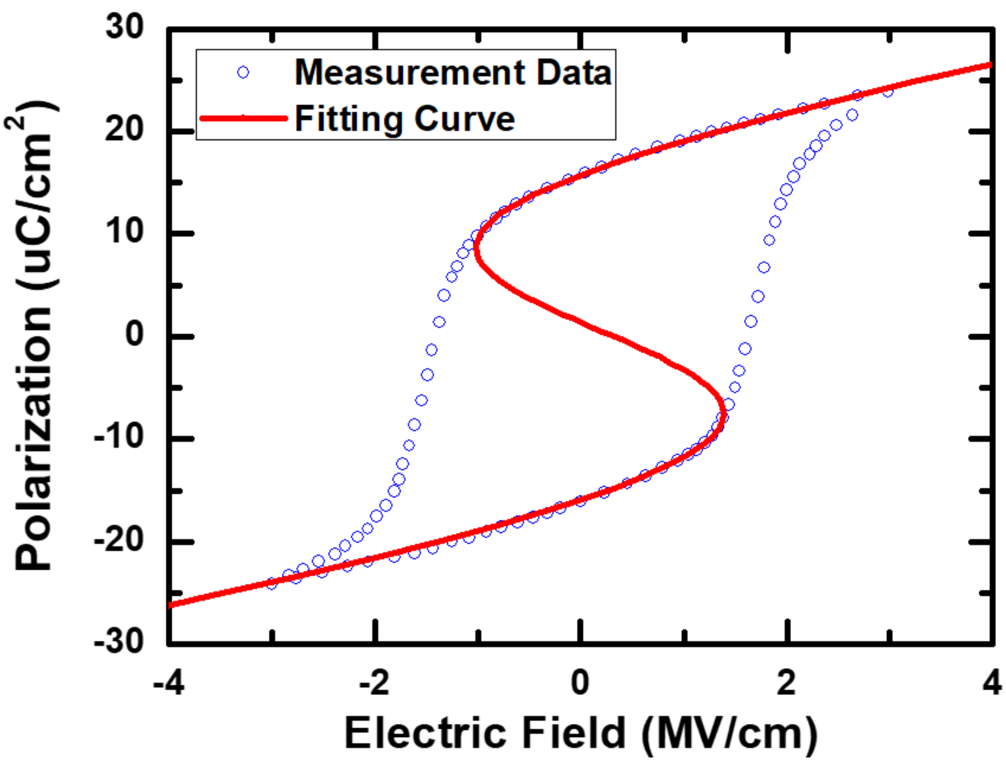


Fig. 9. Polarization-Electric Field loop of the proposed model (red line) and measured data (blue dots).

where P_0 and E_0 are the offset polarization and electric field due to the leakage in the thin film [43]. The extracted parameters are listed in Table 1, and the fitting results are shown in Fig. 9.

ii. Sentaurus TCAD MFMIM structure verification

To study the impact of the dielectric positions on NCFETs, the ferroelectric model (Landau equation) adopted in Sentaurus TCAD should be carefully calibrated. The physical models used in TCAD include the Ginzburg-Landau model for ferroelectric materials, mobility degradation due to carrier-carrier scattering, coulombic scattering, interface scattering, velocity saturation, and the Shockley-Read-Hall process [27]. The structure

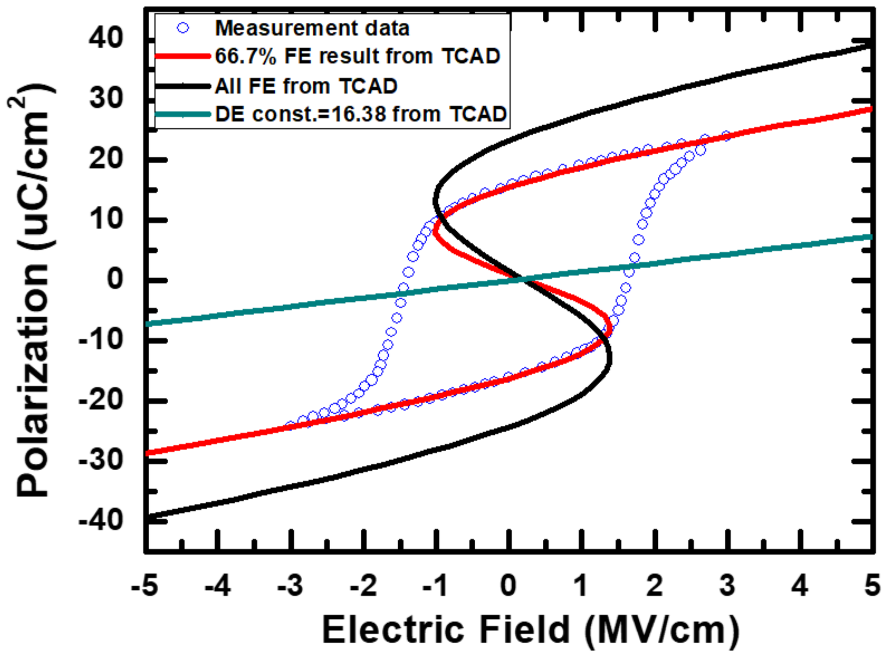


Fig. 10. Polarization versus electrical field plot.

for TCAD simulation is shown in Fig. 8 (b). In Fig. 8 (b), there is a FE-DE mixed layer which consists of 2/3 FE and 1/3 DE sandwiched by metal 1 and metal 2. The SiO_2 layer stabilizes the ferroelectric in the negative capacitance region. The α, β, and γ values of ferroelectric here are the same as the values in TABLE 1. Note that it is assumed no leakage in the FE layer in TCAD, so P_o and E_o is not used here. In Fig. 10, the curve generated by TCAD is shifted by P_o and E_o in the y-direction and x- direction respectively to align with experimental data.

To mimic the P-E loop from experimental measurement, the voltage of metal 1 is swept with metal 2 floating and metal 3 grounded. P-E loop is measured by sandwiching FE layer by two metal electrodes, so an internal metal is added in the TCAD simulation. The P-E curve can be extracted by plotting the charge density in metal 1 (P_{mix}) versus the potential difference of metal 1 and

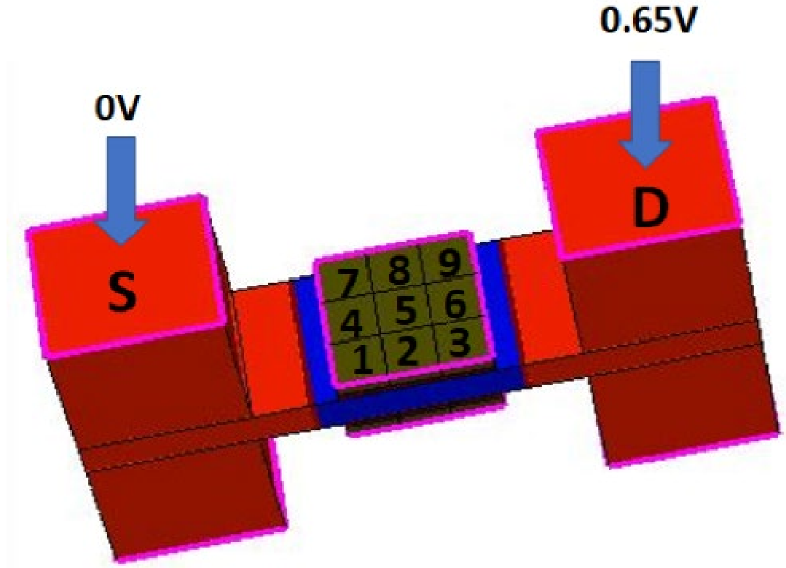


Fig. 11. NCFET structure in Sentaurus TCAD simulation. The red regions are source and drain. The blue region is 5nm-thick channel sandwiched by the gate stack, which consists of 0.8nm SiO_2, 2nm segmented FE-DE mixed layer, and metal contact. The n-type source and drain doping are 2E20(#/cm^3), and the p-type channel doping is 1E17(#/cm^3). Gate work function is 4.6eV.

metal 2 over thickness of FE film (E_{mix}). The P-E curve result from TCAD is shown in Fig. 10. Note that, in Fig. 10, the actual remnant polarization is higher, because the ferroelectric accounts for only 66.7% of the whole FE-DE mixed layer. At zero electric field, the DE portion contributes zero polarization so that the FE part needs 1.5 times of average remnant polarization to build up 1 time of average remnant polarization, showing that mixed FE-DE phases in the thin film would degrade the ferroelectricity.

iii. Sentaurus NCFET DE-FE mixed simulation

The ferroelectric layers of the n-channel double-gate NCFET with a gate length of 18 nm and a channel thickness of 5 nm are segmented into 3-by-3 matrix elements in the Sentaurus TCAD simulation as shown in Fig. 4. It is known that the grain size of HZO is in the same order as HZO thin film

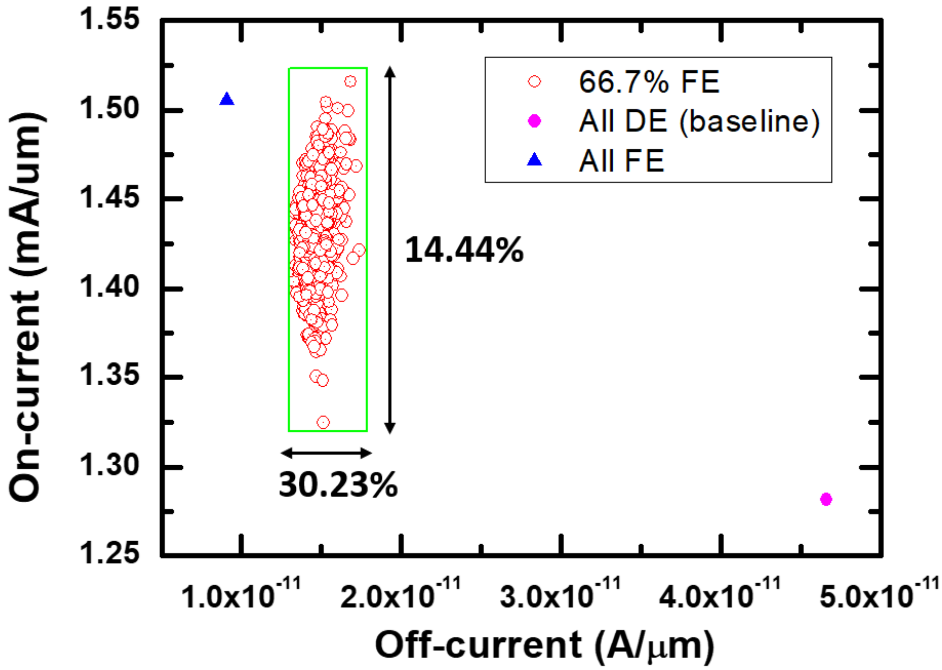
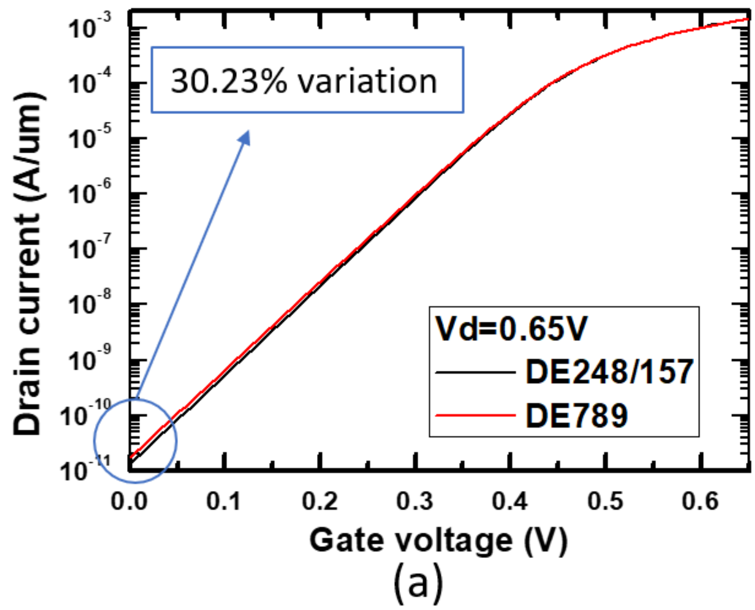


Fig. 12. Scatter plot of the random simulation results. The red circles are random simulation results, the pink dot represents that all the segments are DE (baseline), and the blue triangle represents that all the segments are FE.

thickness from the experiment [44], so grain size of 6nm by 6nm by 2nm is a reasonable assumption. Each element is either ferroelectric or dielectric with the same material parameters obtained from section B (ii). The gate stack is the same as the previous MFMIM structure shown in Fig. 9 except the intermediate metal layer is removed. Note that without intermediate metal layer, the spatial distribution of FE and DE matters, and that is why the same characterized FE film can bring out different characteristic in this part.

As mentioned in the previous section, 66.7% of the FE-DE layers are ferroelectric which means two thirds of segments/grains are ferroelectric. Note that the double-gate NCFET has top and bottom gate stacks with independent distributions of the DE and FE grains but 66.7% of each stack



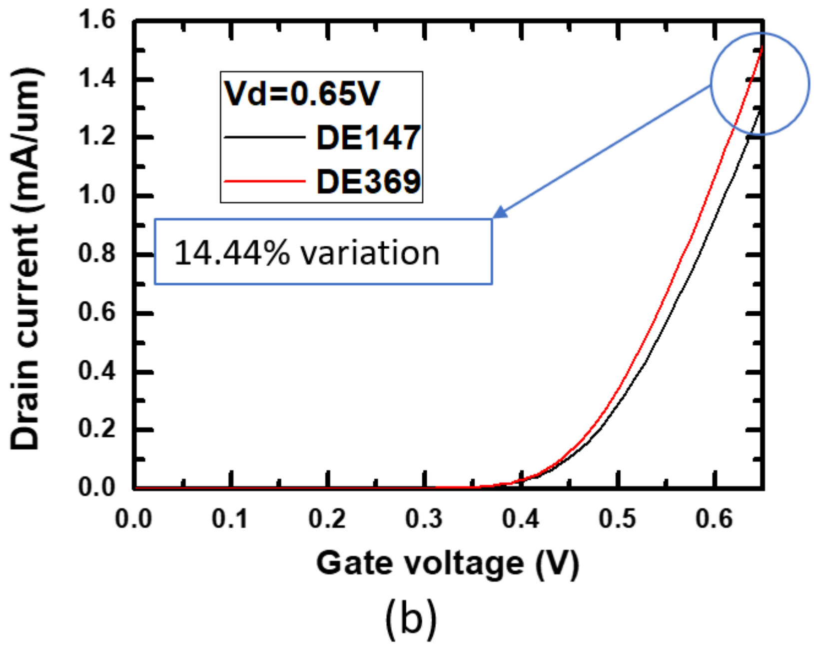


Fig. 13. Drain current versus gate voltage characteristics for (a) I_{off} extreme cases with variation of 30.23% and (b) I_{on} extreme cases with variation of 14.44%.

consists of FE grains. To examine how the distribution of the DE and FE grains would affect the current of the NCFET, a random simulation is carried out. There are 1128 possible combinations by considering two symmetric

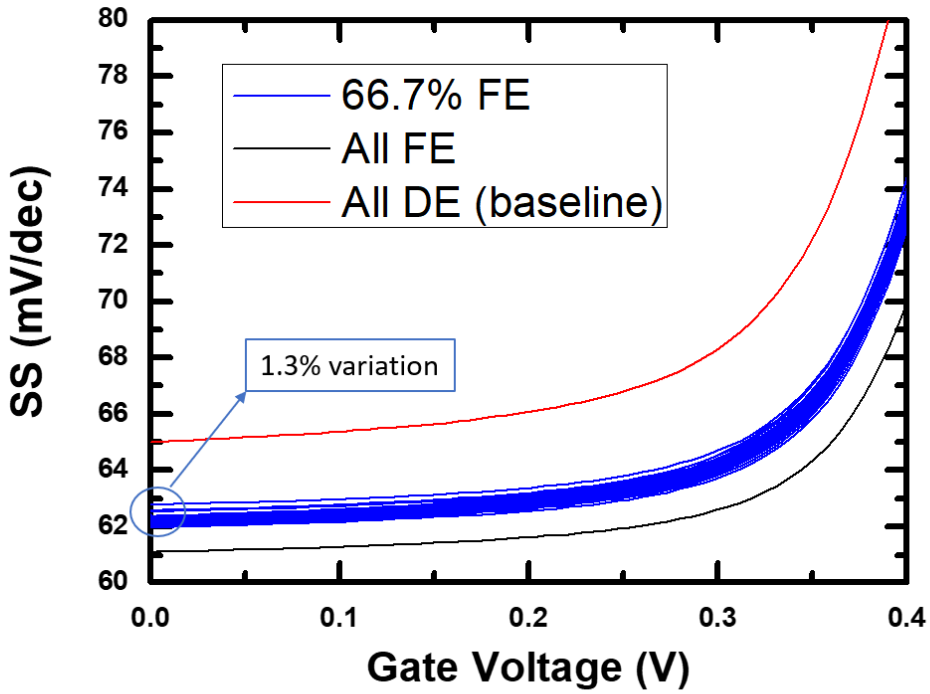


Fig. 14. The subthreshold slope versus gate voltage plot of the random DE and FE distribution simulation.

planes, and 1128 cases are simulated. For each case, V_{DD} is fixed at 0.65V. I_{off} and I_{on} are defined at $V_{GS} = 0$ and V_{DD} at $V_{DS} = V_{DD}$, respectively. The results are shown in the scatter plot in Fig. 12.

In Fig. 12, the green box encloses the boundary of variation due to the different locations of FE and DE grains. Note that the all FE case means there is no dielectric, but α, β, and γ are modified to fit on the experimental P-E loop. The highest and lowest of I_{off} and I_{on} are shown in Fig. 13 (a) and (b), respectively. The highest I_{off} (red curve in Fig. 13(a)) happens when the DE grains on both gates are at the positions of 7, 8, and 9, whereas the lowest I_{off} (black curve) happens when the DE grains are at 2, 4, and 8 on the top gate and at 1, 5, and 7 on the bottom gate. In Fig. 13 (b), the highest I_{on} is obtained when the DE grains are at 3, 6, and 9 on both the top and bottom gates, which

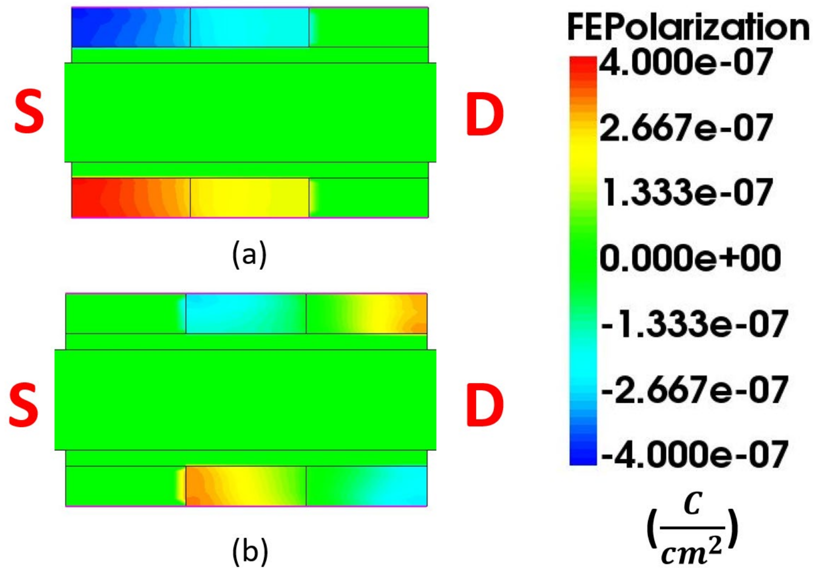


Fig. 15. Ferroelectric polarization 2-D plot at $V_{GS} = V_{DD}$. (a) Source-side ferroelectric (location of DE at number 3, 6, and 9 in Fig. 4) with the highest Ion, and (b) drain-side ferroelectric (location of DE at number 1, 4, and 7 in Fig. 4) with the lowest Ion.

means all FE grains are on the source side. On the other hand, the lowest Ion appears when DE grains are at 1, 4, and 7 on both top and bottom gates, which means that all FE grains are on the drain side. The subthreshold slope (SS) versus gate voltage is plotted in Fig. 14. The SS variation due to random spatial distribution of DE and FE is approximately 1.3%. Significant SS improvement from the baseline can be seen after adding FE.

C. Discussion

In the previous section, the random simulation shows the influence of the DE and FE distributions on the variation in drain current and SS. The physics of the simulation results will be analyzed in detail as follows.

i. On current extreme cases

As mentioned in the previous section, the highest I_{on} happens when the ferroelectric grains are at the source side, and the lowest I_{on} happens when

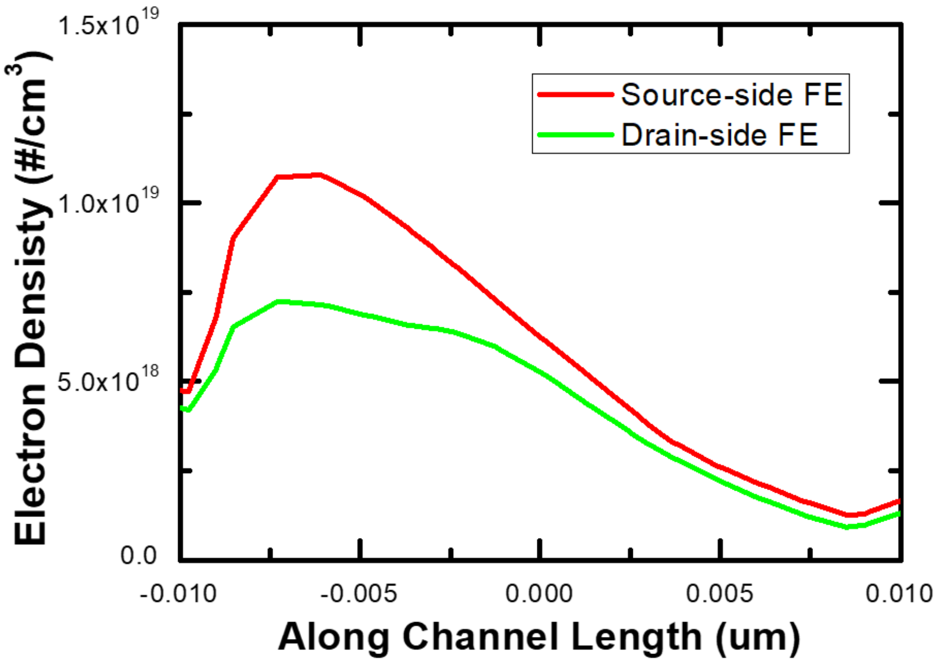


Fig. 16 Electron density near the surface along the channel.

ferroelectric grains are at the drain side. In Fig. 15 (a) and 15 (b), the polarization directions of the top and bottom FE are opposite, since the electric fields point in opposite directions for the top and bottom gate stacks. To make sure that the FE is in negative capacitance region, the absolute values of the FE polarization shown in Fig. 15 (range from -0.4 μC/cm^2 to 0.4 μC/cm^2) should be within the range of negative capacitance region (range from -10 μC/cm^2 to 10 μC/cm^2) as determined by the black curve in Fig. 10. Therefore, in the simulation the FE is always in the negative capacitance region. For the top gate in Fig. 15 (a), negative P_{FE} (polarization pointing from gate to channel) means that the electric field points from channel to gate in the negative capacitance region. The electric field pointing from channel to gate means that the voltage at the interface of the FE and SiO_2 is higher than the applied gate voltage. The voltage amplification on bottom gate in Fig. 15 (a) can also be

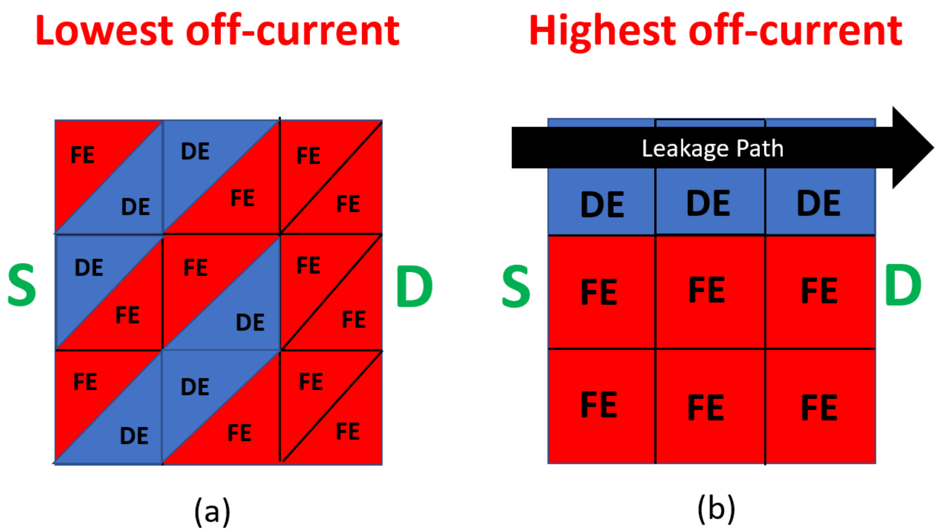


Fig. 17. Layout of DE and FE for (a) the lowest I_{off} case (the upper triangles and the lower triangles refer to top gate and bottom gate, respectively) and (b) the highest I_{off} case.

explained in the same way. However, in Fig. 15 (b) the sign of the polarization changes from source to drain because of the fringing field from the drain to gate [41], which reduces the voltage on drain side.

To compare the ON current between these two cases, the inversion electron density along the channel length near the surface is plotted in Fig. 16. When the FE is at the source side (the carrier injection point of a MOSFET), the source inversion electron density increases due to voltage amplification. In contrast, when the FE is at the drain side, voltage de-amplification occurs because the positive drain voltage induces negative gate charges, which reduces the surface potential and inversion electron density. Therefore, the ON current of source-side FE is highest whereas that of the drain-side FE is lowest.

ii. Off current extreme cases

Fig. 10 (a) shows the lowest I_{off} case where the upper triangles refer to top gate, and the lower triangles refer to bottom gate. The highest leakage path is

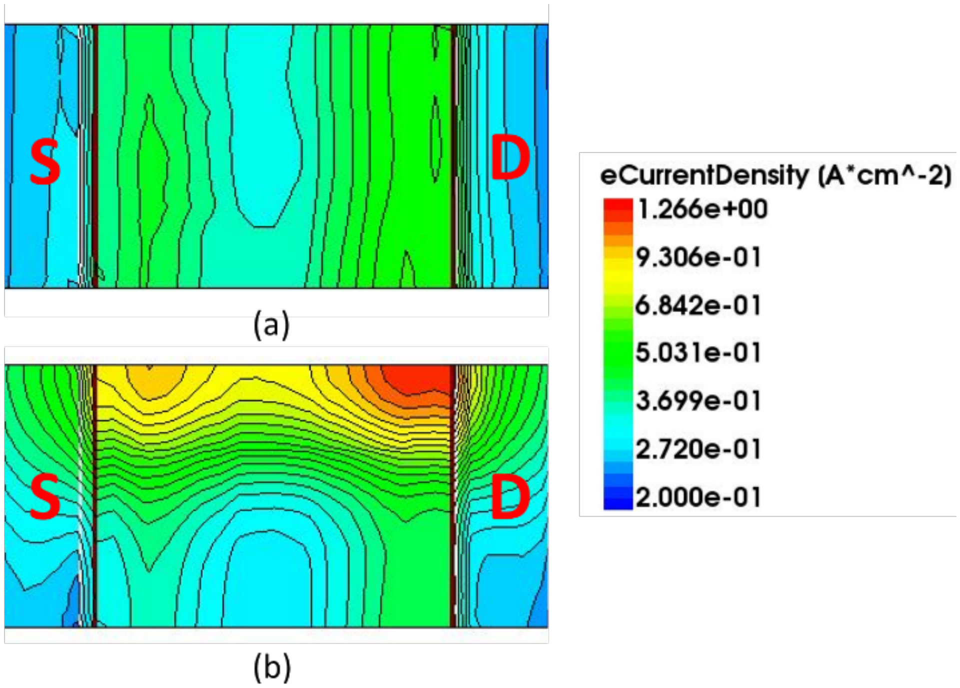


Fig. 18. Electron current density in the middle of the channel for (a) the lowest Ioff case (least leakage one and (b) the highest Ioff case (most leakage one).

at the center of channel due to degraded gate control. The layout of DE and FE grains in Fig. 17 (a) can control the leakage best among all the cases because the FE grains cover the entire drain side so that the fringing field from the drain can help the ferroelectric suppress the leakage current [41], and also evenly cover over the rest of the channel (see Fig. 18 (a)). In contrast, in Fig. 17 (b) all the DE grains are in a line along the channel, causing a leakage path along the DE region, which can be clearly seen in Fig. 18 (b).

iii. Method of estimating the variation

The proposed method can be used to estimate the additional variation caused by the random spatial distribution of DE and FE grains. First of all, the percentage of DE and FE grains present should be quantified by XRD or other measurements. Following that, the parameters can be extracted by the method described in section B (i). After getting all the parameters required for the simulation, one can get the extrema of I_{on} by putting the FE grains all near the source and the drain, respectively. By putting the DE grains in a line along the channel, the highest I_{off} can be obtained. By putting FE grains in a line on drain side and distributing the rest of FE grains evenly but complementary on two sides, the lowest I_{off} can be obtained. Due to the inevitability of the existence of dielectric phases inside the ferroelectric [40], this additional variation should be taken into consideration. By using this method, device designers can estimate the window of variation by just running four cases of TCAD simulations.

iv. The Capacitance matching when FE and DE are mixed

As shown in Fig. 10, the actual ferroelectricity is higher than the effective measured ferroelectricity. As a result, the capacitance matching is actually not good when the matching is made between an effective negative capacitance and a positive capacitance. By considering the FE-DE mixed model after extracting both DE and FE parameters, device designers can design their NCFETs better.

D. Section Summery

A dielectric-ferroelectric mixed model is proposed to extract dielectric and ferroelectric material parameters by fitting the experimental hysteresis loop from literature. Based on these parameters, Sentaurus TCAD is properly calibrated using a MFMIM capacitor. After that, the impact of spatial distribution of dielectric and ferroelectric on NCFET performance is analyzed via Sentaurus TCAD, showing that the ON and OFF current variations can be up to 14.44% and 30.23% respectively. This dielectric-ferroelectric mixed model is good to evaluate the variations in NCFET design.

V. Conclusion

NCFET is a promising technology to extend the Moore's Law by reducing the EOT without reducing the physical gate oxide thickness or interfacial SiO_2 thickness. Therefore, the gate control can be enhanced without sacrificing gate leakage current or mobility. Two topics are brought up in this research project, including "optimization of NCFET by matching FE and DE nonuniformly along the channel" and "variation caused by spatial distribution of dielectric and ferroelectric grains in a negative capacitance field-effect transistor." The former studies how the NCFET device designer can improve the capacitance matching further, and the latter discusses how the circuit designer and the device designer can evaluate the variation of the NCFET device caused by DE grains in the FE film. If both the capacitance matching and the variation of NCFET are carefully considered, better NCFET can be made in the future.

Reference

[1] G. E. Moore, "Cramming More Components Onto Integrated Circuits," in Proceedings of the IEEE, vol. 86, no. 1, pp. 82-85, Jan. 1998. doi: 10.1109/JPROC.1998.658762

[2] S. Salahuddin and S. Datta, "Can the subthreshold swing in a classical FET be lowered below 60 mV/decade?," 2008 IEEE International Electron Devices Meeting, San Francisco, CA, 2008, pp. 1-4. doi: 10.1109/IEDM.2008.4796789

[3] S. Salahuddin and S. Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices,” Nano Letters, vol 8, no. 2, pp. 405-410. doi: 10.1021/nl071804g

[4] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, and S. Salahuddin, “Negative capacitance in a ferroelectric capacitor,” Nature Materials, vol. 14, pp. 182–186, Dec. 2014, doi:10.1038/nmat4148.

[5] V. V. Zhirnov, and R. K. Cavin, “Negative capacitance to the rescue,” Nature Nanotech, vol. 3, pp. 77–78, Feb. 2008, doi: 10.1038/nnano.2008.18.

[6] O. Y. Loh and H. D. Espinosa, “Nanoelectromechanical contact switches,” Nature Nanotech., vol. 7, pp. 283–295, May 2012. doi: 10.1038/NNANO.2012.40.

[7] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, “Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec,” IEEE Electron Device Lett., vol. 28, no. 8, pp. 743–745, Aug. 2007. doi: 10.1109/LED.2007.901273.

[8] U. E. Avci, B. Chu-Kung, A. Agrawal, G. Dewey, V. Le, R. Rios, D. H. Morris, S. Hasan, R. Kotlyar, J. Kavalieros, and I. A. Young, “Study of TFET non-ideality effects for determination of geometry and defect density requirements for sub-60mV/dec Ge TFET,” in IEDM Tech. Dig., Dec. 2015, pp. 891–894. doi: 10.1109/IEDM.2015.7409828.

[9] T. N. Theis, P. M. Solomon, “It’s Time to Reinvent the Transistor,” Science, vol. 327, no. 5973, pp. 1600-1601, Mar. 2010, doi: 10.1126/science.1187597

[10] Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J.Liu, J.Shi, H. J. Kim, R. Sporer, C. Serrao, A. Busquet, P. Polakowski, J. Müller, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, and S. Banna, “14nm Ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications,” in IEDM, San Francisco, CA, USA, 2017, doi: 10.1109/IEDM.2017.8268393.

[11] M. H. Lee, P.-G. Chen, C. Liu, K. Chu, C.-C. Cheng, M.-J. Xie, S.-N. Liu, J.-W. Lee, S.-J. Huang, M.-H. Liao, M. Tang, K.-S. Li, and M.-C. Chen, “Prospects for ferroelectric HfZrOx FETs with experimentally CET=0.98 nm, SSfor=42 mV/dec, SSrev=28 mV/dec, switch-off <0.2 V, and hysteresis-free strategies,” in IEDM Tech. Dig., Dec. 2015, pp. 22.5.1–22.5.4, doi: 10.1109/IEDM.2015.7409759.

[12] K.-S. Li, P.-G. Chen, T.-Y. Lai, C.-H. Lin, C.-C. Cheng, C.-C. Chen, Y.-J. Wei, Y.-F. Hou, M.-H. Liao, M.-H. Lee, M.-C. Chen, J.-M. Sheih, W.-K. Yeh, F.-L. Yang, S. Salahuddin, and C. Hu, “Sub-60 mV-swing negative-capacitance FinFET without hysteresis,” in IEDM Tech. Dig., Dec. 2015, pp. 22.6.1–22.6.4, doi: 10.1109/IEDM.2015.7409760

[13] A. Rusu, G. A. Salvatore, D. Jimenéz, and A. M. Ionescu, “Metal-ferroelectric-meta-oxide-semiconductor field effect transistor with sub-60 mV/decade subthreshold swing and internal voltage amplification,” in IEDM Tech. Dig., Dec. 2010, pp. 16.3.1–16.3.4, doi: 10.1109/IEDM.2010.5703374.

[14] W. Chung, M. Si, and P. D. Ye, “Hysteresis-free negative capacitance germanium CMOS FinFETs with Bi-directional Sub-60 mV/dec,” in IEDM, San Francisco, CA, USA, 2017, doi: 10.1109/IEDM.2017.8268395.

[15] C.-C. Fan, C.-H. Cheng, Y.-R. Chen, C. Liu, and C.-Y. Chang, “Energy-efficient HfAlOx NCFET: Using gate strain and defect passivation to realize nearly hysteresis-free sub-25mV/dec switch with ultralow leakage,” in IEDM, San Francisco, CA, USA, 2017, doi: 10.1109/IEDM.2017.8268444.

[16] M. Hoffmann, M. Pesic, S. Slesazeck, U. Schroeder, and T. Mikolajick, “On the stabilization of ferroelectric negative capacitance in nanoscale devices,” Nanoscale, vol. 10, pp. 10891–10899, May 2018. doi: 10.1039/C8NR02752H.

[17] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, “Physical Insights on Negative Capacitance Transistors in Nonhysteresis and Hysteresis Regimes: MFMIS Versus MFIS Structures,” IEEE Trans. Electron Devices, vol. 65, no. 3, pp. 867-873, Mar. 2018, doi: 10.1109/TED.2018.2794499.

[18] V. Garcia, and M. Bibes, “Ferroelectric tunnel junctions for information storage and processing,” Nature Communications, no. 5, pp 4289, Jul. 2014, doi: 10.1038/ncomms5289.

[19] A.K. Saha, P. Sharma, I. Dabo, S. Datta, and S. K. Gupta, “Ferroelectric transistor model based on self-consistent solution of 2D Poisson's, non-equilibrium Green's function and multi-domain Landau Khalatnikov equations,” in IEDM, San Francisco, CA, USA, 2017, doi: 10.1109/IEDM.2017.8268385.

[20] Z. C. Yuan, S. Rizwan, M. Wong, K. Holland, S. Anderson, T. B. Hook, S. Kienle, S. Gadelrab, P. S. Gudem, M. Vaidyanathan, “Switching-Speed Limitations of Ferroelectric Negative-Capacitance FETs,” IEEE Trans. Electron Devices, vol. 63, no. 10, pp. 4046-4052, Oct. 2016, doi: 10.1109/TED.2016.2602209.

[21] A. Cano, and D. Jimenez, “Multidomain ferroelectricity as a limiting factor for voltage amplification in ferroelectric field-effect transistors,” Appl. Phys. Lett. Vol. 97, no. 13, Sep. 2010, doi: 10.1063/1.3494533.

[22] A. I. Khan, U. Radhakrishna, S. Salahuddin, and D. Antoniadis, “Work Function Engineering for Performance Improvement in Leaky Negative Capacitance FETs,” IEEE Electron Device Letters, vol. 38, no. 9, pp. 1335-1338, Sept. 2017, doi: 10.1109/LED.2017.2733382.

[23] J. Zhou, Y. Peng, G. Han, Q. Li, Y. Liu, J. Zhang, M. Liao, Q.-Q. Sun, D. W. Zhang, Y. Zhou, Y. Hao, “Hysteresis Reduction in Negative Capacitance Ge PFETs Enabled by Modulating Ferroelectric Properties in HfZrOx,” IEEE Journal of the Electron Devices Society, vol. 6, pp. 41-48, Oct. 2017, doi: 10.1109/JEDS.2017.2764678.

[24] G. Pahwa, A. Agarwal, and Y. S. Chauhan, “Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior,” IEEE Trans. Electron Devices, Sep. 2018, doi: 10.1109/TED.2018.2870519.

[25] M. H. Park, Y. H. Lee, H. J. Kim, Y. J. Kim, T. Moon, K. D. Kim, J. Muller, A. Kersch, U. Schroeder, T. Mikolajick, and C. S. Hwang, “Ferroelectricity and antiferroelectricity of doped thin HfO2-based films,” Adv. Mater., vol. 27, no. 11, pp. 1811–1831, Mar. 2015. doi: 10.1002/adma.201404531.

[26] M.-Y. Kao, A. B. Sachid, Y.-K. Lin, Y.-H. Liao, H.Agarwal, P. Kushwaha, J. P. Duarte, H.-L. Chang, S. Salahuddin, and C. Hu, “Variation Caused by Spatial Distribution of Dielectric and Ferroelectric Grains in a Negative Capacitance Field-Effect Transistor,” IEEE Trans. Electron Devices, vol. 65, no. 10, pp. 4652-4658, Oct. 2018, doi: 10.1109/TED.2018.2864971.

[27] Sentaurus Device, Synopsys, Inc., CA, USA, 2017.

[28] M. Hoffmann, M. Pesic, S. Slesazeck, U. Schroeder, and T. Mikolajick, “On the stabilization of ferroelectric negative capacitance in nanoscale devices,” Nanoscale, no. 23, pp. 10891-10899, May. 2018, doi: 10.1039/C8NR02752H.

[29] C.-I. Lin, A. I. khan, S. Salahuddin, and C. Hu, “Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics,” IEEE Trans. Electron Devices, vol. 63, no. 5, pp. 2197-2199, Jan. 2016, doi: 10.1109/TED.2016.2514783

[30] K. Chatterjee, A. J. Rosner, and S. Salahuddin, “Intrinsic speed limit of negative capacitance transistors,” IEEE Electron Device Letters, vol. 38, no. 9, pp. 1328-1330, Sept. 2017, doi: 10.1109/LED.2017.2731343.

[31] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, “FinFET—A self-aligned double-gate MOSFET scalable to 20 nm,” IEEE Trans. Electron Devices, vol. 47, no. 12, pp. 2320–2325, Dec. 2000, doi: 10.1109/16.887014.

[32] S. Joglekar, U. Radhakrishna, D. Piedra, D. Antoniadis, and T. Palacios, “Large Signal Linearity Enhancement of AlGaN/GaN High Electron Mobility Transistors by Device-level VT Engineering for Transconductance Compensation,” in IEDM, San Francisco, CA, USA, 2017, doi: 10.1109/IEDM.2017.8268457.

[33] S. Dasgupta, A. Rajashekhar, K. Majumdar, N. Agrawal, A. Razavieh, S. Troiier-McKinstry, and S. Datta, “Sub-kT/q switching in strong inversion in PbZr0.52Ti0.48O3 gated negative capacitance FETs,” IEEE J. Exploratory Solid-State Comput. Device Circuits, vol. 1, pp. 43–48, Dec. 2015, doi: 10.1109/JXCDC.2015.2448414.

[34] A. I. Khan, K. Chatterjee, J. P. Duarte, Z. Lu, A. Sachid, S. Khandelwal, R. Ramesh, C. Hu, and S. Salahuddin, “Negative capacitance in short-channel FinFETs externally connected to an epitaxial ferroelectric capacitor,” IEEE Electron Device Lett., vol. 37, no. 1, pp. 111–114, Jan. 2016, doi: 10.1109/LED.2015.2501319

[35] A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, and T. Palacios, “Subthreshold swing improvement in MoS2 transistors by the negative-capacitance effect in a ferroelectric Al-doped-HfO2/HfO2 gate dielectric stack,” Nanoscale, vol. 9, pp. 6122–6127, Apr. 2017, doi: 10.1039/C7NR00088J.

[36] J. Zhou, G. Han, Q. Li, Y. Peng, X. Lu, C. Zhang, J. Zhang, Q.-Q. Sun, D. W. Zhang, and Y. Hao, “Ferroelectric HfZrOx Ge and GeSn PMOSFETs with sub-60 mV/decade subthreshold swing, negligible hysteresis, and improved Ids,” in IEDM Tech. Dig., Dec. 2016, pp. 12.2.1–12.2.4, doi: 10.1109/LED.2015.2501319.

[37] C. Hu, S. Salahuddin, C. I. Lin, and A. Khan, “0.2V adiabatic NC-FinFET with 0.6mA/ um ION and 0.1nA/um IOFF,” in IEEE 73rd Annual Device Research Conference (DRC), Columbus, OH, USA, 2015, doi: 10.1109/DRC.2015.7175542.

[38] J. P. Duarte, S. Khandelwal, A. I. Khan, A. Sachid, Y.-K. Lin, H.-L. Chang, S. Salahuddin, and C. Hu, “Compact models of negative-capacitance FinFETs: Lumped and distributed charge models,” in IEDM, San Francisco, CA, USA, 2016, doi: 10.1109/IEDM.2016.7838514.

[39] H. Agarwal et al., "Engineering Negative Differential Resistance in NCFETs for Analog Applications," in IEEE Transactions on Electron Devices, vol. 65, no. 5, pp. 2033-2039, May 2018. doi: 10.1109/TED.2018.2817238

[40] L. Xu, T. Nishimura1, S. Shibayama1, T. Yajima1, S. Migita, and A. Toriumi, “Kinetic pathway of the ferroelectric phase formation in doped HfO2 films,” Journal of Applied Physics, vol. 122, no. 12, pp. 124104, Sep. 2017, doi: 10.1063/1.5003918.

[41] A. K. Saha, P. Sharma, I. Dabo1, S. Datta and S. K. Gupta, “Ferroelectric Transistor Model based on Self-Consistent Solution of 2D Poisson’s, Non-Equilibrium Green’s Function and Multi-Domain Landau Khalatnikov Equations,” in IEDM, San Francisco, CA, USA, 2017, doi: 10.1109/IEDM.2017.8268385.

[42] H. Ota, K. Fukuda, T. Ikegami, J. Hattori, H. Asai, S. Migita, and A. Toriumi, “Perspective of Negative Capacitance FinFETs Investigated by Transient TCAD Simulation,” in IEDM, San Francisco, CA, USA, 2017, doi: 10.1109/IEDM.2017.8268394.

[43] L. D. Filip, L. Pintilie, W.-S. Tam, C.-W. Kok, “Leakage current for thin film metal-ferroelectric-metal device,” in Next-Generation Electronics, Hsinchu, Taiwan, 2016, doi: 10.1109/ISNE.2016.7543292.

[44] M. H. Park, H. J. Kim, Y. J. Kim, T. Moon, and C. S. Hwanga, “The effects of crystallographic orientation and strain of thin Hf0.5Zr0.5O2 film on its ferroelectricity,” Appl. Phys. Lett., vol. 104, no. 7, Feb. 2014, doi: 10.1063/1.4866008.