

# Millivolt Micro-Electro-Mechanical Relay Devices & Circuits

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Millivolt Micro-Electro-Mechanical Relay Devices & Circuits

by

Zhixin Alice Ye

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering and Computer Science

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Tsu-Jae King Liu, Chair

Professor Vladimir Stojanović

Professor Junqiao Wu

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## Abstract

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The emergence of the Internet of Things (IoT) has brought energy consumption to the forefront of challenges for future information processing devices. Digital logic integrated circuits (ICs) implemented with complementary metal-oxide-semiconductor (CMOS) transistors have a fundamental lower limit on energy consumption due to their non-zero OFF-state current ( $I_{OFF}$ ) and finite sub-threshold slope. In contrast, micro-electro-mechanical (MEM) switches (relays) can achieve zero  $I_{OFF}$  and have abrupt switching characteristics; therefore, they have attracted growing interest for ultra-low-power computing applications.

This dissertation first addresses challenges for realizing millivolt operation of relay ICs. The impact of electrode configuration on contact resistance and hysteresis voltage is investigated, and it is found that reducing the number of contact dimples from 4 to 2 improves the tradeoff between on-state resistance and minimum operating voltage. With an anti-stiction self-assembled monolayer (SAM) coating, a variety of pass-gate logic circuits using the new 2-contact-dimple relay design are demonstrated to operate with sub-50 mV voltage signals; these include AND, OR and XOR gates and a 2:1 multiplexer (MUX). Multi-functional MEM relay circuits are also demonstrated including a majority gate, 2-bit 2:1 MUX, and dual-polarity gates (XOR/XNOR).

Next, this dissertation addresses remaining practical challenges and discusses opportunities for MEM relay technology. A new method using voltage pulses to reliably break down native oxide on contact-electrode surfaces is developed. SAM coating and operation in liquid dielectric media are explored for improving on-state resistance stability for tungsten contacts in ambient conditions. Finally, MEM relays are demonstrated to function well in extreme environments across a wide temperature range.

Finally, this dissertation proposes a novel relay design that incorporates a beam with negative stiffness to reduce the body bias voltage necessary for millivolt operation. This compensated relay design is investigated with the aid of computer simulations, and is found to provide for

improved tradeoff between relay switching energy and turn-on delay under certain conditions. The effects of process-induced variations on relay switching voltage are studied and compared for the compensated relay design *vs.* a conventional relay design.

To my parents Qiubo and Jing  
and my brother Edward

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# Chapter 1

## Introduction

### 1.1 The CMOS Energy Efficiency Limit

#### Modern Computing Trends

The growth of computing technology in the past several decades has had revolutionary impact on innovation, technology, and the transfer of information. Cloud computing, artificial intelligence, cryptocurrency, and more have fundamentally changed the way that people interact with the world surrounding them. Underlying the datacenters, the widespread internet access, and the consumer devices (cell phones, smart devices, etc.), the proliferation of computing can be attributed in part to improvements to a fundamental computer building block: the transistor.

Since the invention of the transistor in 1947, computing ability has grown exponentially; in fact, in 1967 Gordon Moore first observed the trend that the number of complementary metal-oxide-semiconductor (CMOS) transistors doubles on the leading microprocessor chip every 18 months (known as Moore's Law). The semiconductor industry has managed to sustain this trend for more than 5 decades. However, various limitations are now arising, causing the cadence of shrinking transistor size, increased cost-effectiveness, and improved performance and energy efficiency of integrated circuits to slow down (see Fig. 1.1).

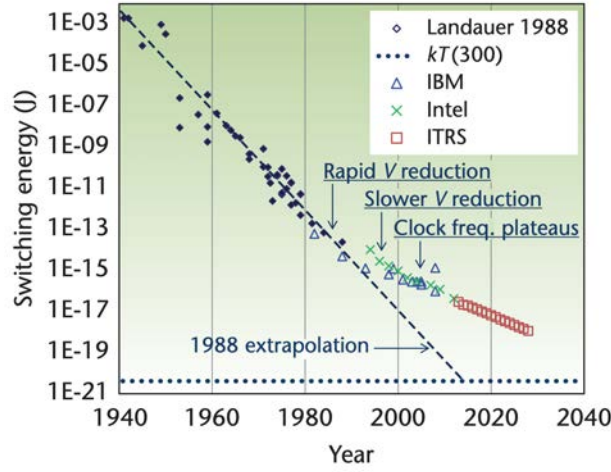


Figure 1.1: Gordon Moore’s observed trends in comparison to the expected reduction in switching energy using current transistor technologies (reproduced from [1]).

Computational energy efficiency is a key metric to evaluate the performance of digital integrated circuits. With densely packed devices, the ability to dissipate heat limits the compactness and speed of circuit operation. Also, considerable increases in chip temperature can cause circuit failure. For off-grid electronics powered via battery or other sources, the total amount of stored energy is also limited; thus energy efficiency determines the operating time in-between battery charges or changes. Finally, datacenters are growing in number and size, with expected electricity consumption of up to 8% of total electricity consumption in 2030 [2]. Reducing their electricity consumption can have significant impact on global carbon emissions as well.

## CMOS Transistors and Circuits

A metal-oxide-semiconductor field-effect-transistor (MOSFET) is used as an electronic switch in digital computing applications. It consists of 4 terminals: *gate*, *source*, *drain*, and *body*, as shown in Fig 1.2. If the transistor is in the ON state, current ( $I_{DS}$ ) can flow through the channel between the source and drain provided there is a voltage difference across the source and drain terminals.

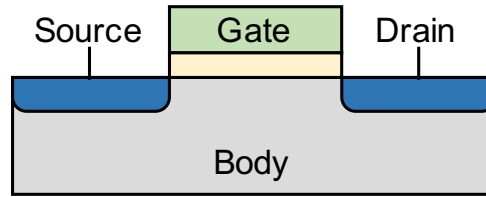


Figure 1.2: Schematic cross-section of a MOSFET

If the channel current is composed of negative charges (electrons), the transistor is considered an n-channel MOSFET, or NMOS transistor. An NMOS transistor turns ON when the voltage applied to the gate electrode is increased, causing the voltage across the gate and source terminals ( $V_{GS}$ ) to be greater than the threshold voltage ( $V_T$ ). If the channel current is composed of positive charge (holes), the transistor is considered a p-channel MOSFET, or PMOS transistor. A PMOS transistor turns ON when the voltage applied to the gate electrode is decreased, causing the voltage across the source and gate ( $V_{SG}$ ) to be greater than  $|V_T|$ . NMOS and PMOS switches are usually used together in a complementary fashion to implement CMOS digital circuits. The symbols for NMOS and PMOS transistors are shown below.

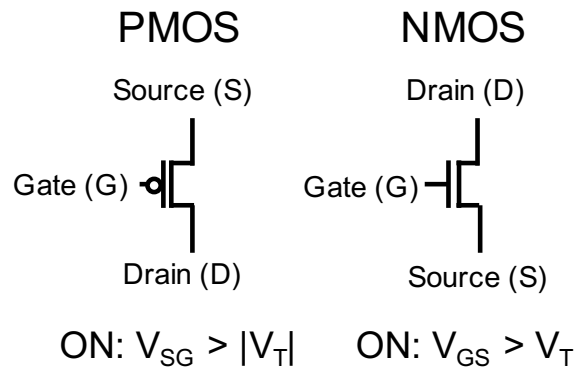


Figure 1.3: CMOS circuit symbols for PMOS transistor and NMOS transistor

In digital computing, voltage signals have binary values, *i.e.*, a binary digit (bit) ‘0’ is represented by a low voltage ( $V_{SS}$ ), and a bit ‘1’ is represented by a high voltage ( $V_{DD}$ ). An example of a CMOS digital logic circuit (inverter) is shown below. The gates of the PMOS and NMOS transistors are connected together; when the input voltage ( $V_{IN}$ ) is high, the NMOS transistor is ON (because  $V_{GS} > V_T$ ) and will discharge the output  $V_{OUT}$  to  $V_{SS}$ . Meanwhile, the PMOS transistor is OFF (because  $V_{SG} = 0 < |V_T|$ ). When the input voltage

( $V_{IN}$ ) is low, then the situation is reversed; the NMOS transistor is OFF and the PMOS transistor is ON and will charge the output  $V_{OUT}$  to  $V_{DD}$ . Note that a PMOS transistor is typically used for passing a logic signal ‘1’ (to ‘pull-up’ the output node to  $V_{DD}$ ) but if it were to pass a ‘0’ signal, the device would turn OFF and stop conducting current when  $V_{SG} < |V_T|$ , so the output voltage  $V_{OUT}$  would be  $V_{SS} + |V_T|$ . This is referred to as a ‘weak 0’ because the output voltage is not pulled down completely to  $V_{SS}$ . A complementary scenario can be described for the NMOS transistor, which passes a weak ‘1’ and strong ‘0’. The speed of the inverter circuit depends on the size (width of the channel region) of the transistors - larger transistor size means more ON-state current, so it will operate faster.

## CMOS Inverter

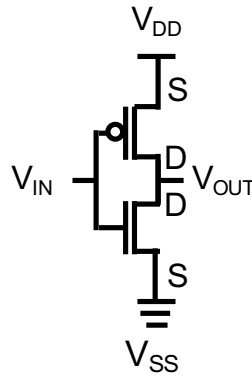


Figure 1.4: CMOS implementation of an inverter circuit.

The most popular style of digital logic computing takes this into account by utilizing a set of basic logic gates (*e.g.* NAND/NOR/NOT) with a pull-up network and pull-down network, as shown in Fig. 1.5a. The pull-up network, which charges  $V_{OUT}$  to  $V_{DD}$ , consists entirely of PMOS transistors. The pull-down network, which discharges  $V_{OUT}$  to  $V_{SS}$ , consists entirely of NMOS transistors. Pass-gate logic is another style of logic that uses transistors to propagate voltage signals, as shown in Fig. 1.5b. A transmission gate consists of one PMOS transistor and one NMOS transistor, with their sources connected together to form the input node and their drains tied together to form the output node. Complementary signals are applied to the gates of the pair of PMOS and NMOS transistors, such that they are either both turned ON to pass the (high or low) voltage signal or both turned OFF. Note that both transistors are required to be able to pass both a ‘strong 0’ and ‘strong 1’ signal [3]. For CMOS circuits, the pass-gate logic architecture can sometimes be more attractive, for example to implement multiplexer (MUX) style or exclusive-OR (XOR) logic.

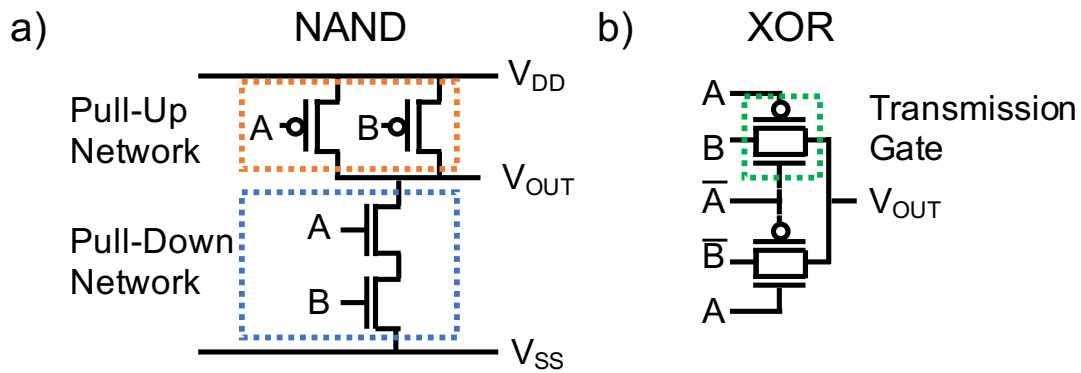


Figure 1.5: a) CMOS implementation of a 2-input NAND gate, using a pull-up network of PMOS transistors and a pull-down network of NMOS transistors. b) CMOS implementation of 2-input XOR gate, using two pass gates.

### $V_{DD}$ Scaling Limit for CMOS Technology

A typical semi-log plot of the drain current ( $\log(I_{DS})$ ) vs. gate voltage ( $V_{GS}$ ) characteristic of an NMOS transistor is shown in Fig. 1.6.

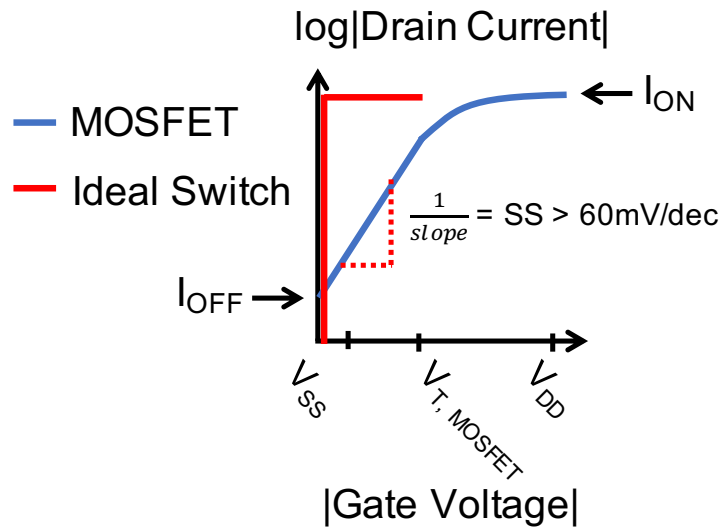


Figure 1.6: Illustrative transfer characteristic for a MOSFET compared to that for an ideal switch. A MOSFET is a non-ideal switch because it has non-zero off-state leakage current.

Below the threshold voltage ( $V_{T,MOSFET}$ ),  $I_{DS}$  shows exponential dependence on gate voltage. The inverse slope of the  $I_{DS} - V_{GS}$  curve in this region is known as the subthreshold swing (SS), which is limited to be  $> 60$  mV/decade at room temperature due to the Boltzmann distribution of electrons [4, 5]. In the OFF state ( $V_{GS} = 0$ ), non-zero leakage current ( $I_{OFF} > 0$ ) flows through a MOSFET, causing CMOS circuits to consume power in their static state. Increasing the threshold voltage can improve (lower) off-state leakage current and reduce static power consumption (due to  $I_{OFF}$  decreasing exponentially), but with the trade-off of lower on-state current ( $I_{ON}$ ) or the need for larger  $V_{DD}$  to maintain the same  $I_{ON}$  for high circuit operating speed. In contrast, reducing the threshold voltage increases  $I_{ON}$  for faster circuit operation, but with the trade-off of exponentially larger  $I_{OFF}$ . Thus there is an inherent trade-off between energy efficiency and circuit operating speed in the choice of  $V_T$  for CMOS circuits.

The total energy dissipated ( $E_{tot}$ ) by a digital logic circuit is composed of a dynamic energy dissipation component ( $E_{dyn}$ ) and a static energy dissipation component ( $E_{leak}$ ).  $E_{dyn}$  is dissipated due to charging capacitive circuit elements, while the  $E_{leak}$  is dissipated due to transistor OFF-state leakage current (allowing current to flow continuously between  $V_{DD}$  and  $V_{SS}$ ).

$$E_{tot} = E_{dyn} + E_{leak} \quad (1.1)$$

The dynamic energy is proportional to the average capacitance charged per clock cycle ( $C_{eff}$ ), the operating frequency ( $f$ ), time duration of one circuit operation cycle ( $\tau$ ), and square of the supply voltage ( $V_{DD}^2$ ):

$$E_{dyn} \propto C_{eff} V_{DD}^2 f \tau \quad (1.2)$$

The leakage energy is proportional to the OFF-state leakage current,  $I_{OFF}$ , time duration of one circuit operation cycle, and supply voltage:

$$E_{leak} \propto I_{OFF} V_{DD} \tau \quad (1.3)$$

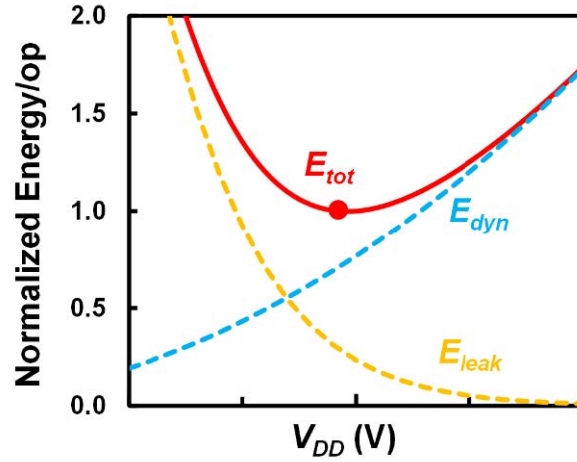


Figure 1.7: Tradeoff between dynamic energy and static energy of a CMOS digital logic circuit vs.  $V_{DD}$  (reproduced from [6]).

The total energy for one clock cycle of operation,  $E_{tot}/op$ , is illustrated in Fig. 1.7. As  $V_{DD}$  decreases, the time to perform a digital operation ( $\tau$ ) increases due to reduced  $I_{ON}$ , thus increasing  $E_{leak}$ . Another option is to decrease  $V_T$  along with  $V_{DD}$  to maintain the same time to perform an operation; however in this case,  $I_{OFF}$  increases, thus still increasing static energy dissipation. As  $V_{DD}$  is lowered below the threshold voltage, the total energy increases; in other words, the energy efficiency of a CMOS circuit is limited due to non-zero  $I_{OFF}$ . In order to overcome this energy efficiency limit, alternative electronic switching devices with zero off-state leakage current and more steeply switching characteristics are of interest. An ideal switch, as illustrated in Fig. 1.6, would have abrupt switching characteristics and  $V_T$  near 0 V to enable millivolt gate voltage swing for switching operation.

## 1.2 Why MEM Relays?

Microelectromechanical (MEM) relays are attractive alternatives to CMOS transistors because they can achieve zero  $I_{OFF}$  for zero static power consumption and be operated with much smaller gate voltage swing, providing for order-of-magnitude lower supply voltage  $V_{DD}$ . The ability to achieve millivolt computing with ideally abrupt switching characteristics (to minimize  $V_{DD}$  and therefore  $E_{dyn}$ ) and zero  $I_{OFF}$  (to eliminate  $E_{leak}$ ) represents the ultimate goal for energy-efficient digital computing.

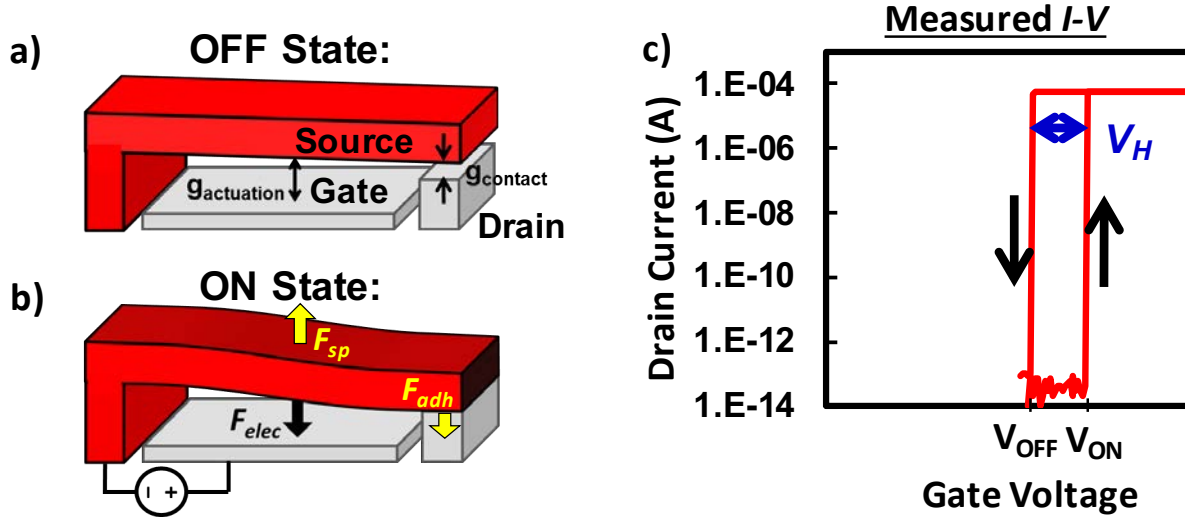


Figure 1.8: Illustration of a 3-terminal MEM switch in a) OFF state, and b) ON state. c) Illustrative semi-log  $I_{DS}$ -vs.- $V_{GS}$  characteristics, showing abrupt switching characteristics (adapted from [7]).

Fig. 1.8 shows a 3-terminal MEM switch, consisting of a suspended source electrode and a fixed drain electrode separated by an electrically insulating air gap. In the OFF-state, current does not flow between these electrodes because they are physically separated by an air gap. An applied voltage difference across the gate and source electrodes induces an attractive electrostatic force ( $F_{\text{elec}}$ ) that deforms the source electrode downward toward the fixed gate electrode. If the voltage difference is such that  $V_{GS} \geq V_{\text{ON}}$ , this force is sufficient to bring the source into physical contact with the drain, turning ON the device and allowing current to flow between source and drain. To turn off the switch, the voltage difference across the gate and source should be reduced below  $V_{\text{OFF}}$  so that the spring restoring force ( $F_{\text{sp}}$ ) can overcome  $F_{\text{elec}}$  plus the contact adhesion force ( $F_{\text{adh}}$ ) to bring the source electrode out of contact with the drain electrode. The hysteresis voltage ( $V_H$ ) is defined as  $V_H = |V_{\text{ON}} - V_{\text{OFF}}|$ . Note that the MEM switch can conduct charges in either direction, thus it can pass both a ‘strong 0’ and ‘strong 1.’ MEM switches can incorporate multiple elements into a single movable structure to perform more complex switching functions. For example, there can be multiple source-drain pairs or multiple gates, to enable more compact integrated circuit implementation.

### 1.3 MEM Relay Integrated Circuits

To fully understand the potential benefit of MEM relay technology for integrated systems, circuit-level benefits should also be evaluated in addition to switching device performance. MEM relays have some features that are different than those of CMOS transistors, which make them more suitable for different styles of circuit design. The operation of a MEM relay is limited largely by the time required to physically actuate the movable electrode, *i.e.*, the mechanical delay, rather than the charging or discharging of the drain node capacitance, *i.e.*, the electrical delay. The mechanical delay of a nanometer-scale relay can approach 10 ns, while the RC time constant for a relay driving the gate of another identical relay is less than 1 ps [8]. Thus, optimal design of MEM relay integrated circuits generally minimizes the number of mechanical delays. Therefore, although the mechanical delay of a relay may be significantly larger than that of a CMOS inverter, a complete CMOS logic block (spanning clocked latches) will typically require 10-20 logic gate delays whereas an optimally designed relay-based implementation may comprise only one mechanical delay, so that relay-based integrated circuits can achieve comparable operating speed [9]. Pass-gate circuit topologies are especially attractive for MEM relays because they can be designed with few mechanical delays, and a single relay can act as a transmission gate (whereas two transistors are required to implement a CMOS transmission gate).

A variety of MEM relay integrated circuits (ICs) already has been demonstrated; these include latches, adders and multipliers [6, 9, 10] designed following the principle of minimizing the number of mechanical switching delays between clocked latches to achieve the fastest possible computing speed. By endowing MEM relays with greater functionality, the complexity of relay-based ICs can be reduced for performance gains.

### 1.4 Dissertation Overview

Recently, reliable operation of individual MEM relays with gate voltage swings as low as 50 mV at room temperature has been demonstrated [11–13]. This dissertation builds upon prior work to explore MEM relay IC operation with millivolt supply voltages, making key contributions in relay switch design and integrated circuit design to demonstrate ultra-low-voltage (down to 25-mV) relay-based ICs with versatile functionality.

Chapter 2 presents the implementation of reliable millivolt relay-based circuits. First an overview of the MEM relay fabrication process and device design is presented. The first sub-50 mV logic gates (AND/OR, etc) are demonstrated using an improved single-contact relay design and a self-assembled monolayer coating, with appropriate body-bias voltages. In addition, multi-input relays and ICs implemented using them are demonstrated to operate reliably at sub-1 V supply voltage, and their voltage scaling limitations are discussed.

Chapter 3 discusses practical challenges and opportunities for ultra-low-voltage MEM

relay circuits. The effect of relay contact oxidation and device reliability are examined. Methods to mitigate contact oxidation and extend device reliability are tested, compared and discussed. Relay operation across a wide range of temperatures is demonstrated, posing new opportunities for MEM relay circuit application.

Chapter 4 investigates a novel approach to improve the energy-delay tradeoff for MEM relay design, by incorporating negative stiffness beams to compensate the stiffness of the movable electrode suspension beams. The theory for the switching behaviour of the compensated relay design is derived. The effects of scaling and process variation on switching voltage are estimated. The compensated relay design is optimized to minimize  $V_{DD}$ , and shown to provide for improved energy-delay tradeoff in certain cases as compared to the conventional relay design.

Chapter 5 summarizes the key findings and contributions of this dissertation. Suggestions for future work are also offered.

## Chapter 2

# Millivolt MEM Relay Integrated Circuits

### 2.1 Introduction

The first functional MEM relay integrated circuits (ICs) required  $>1$  V supply voltages [9, 14–16]. This falls short of the goal to demonstrate operating voltages lower than those required for CMOS ICs, which today operate with  $V_{DD}$  down to approximately 0.5 V (for  $I_{ON}/I_{OFF} > 10^6$ ). In recent years, significant progress has been made in the development of MEM relay technology for digital computing applications. The design of electrostatically actuated MEM relays has been refined to lower the gate voltage swing (hence  $V_{DD}$ ) and to improve physical contact properties for more reliable low-voltage operation, while the benefits of relay miniaturization and design optimization for maximum energy efficiency have been discussed [12, 17, 18]. Refinements to the relay fabrication process have improved device manufacturing yield and reliability. For example, improvements to the structural-layer deposition process helped to minimize residual stress and undesired strain gradient resulting in out-of-plane deflection [19]; self-assembled monolayer coatings reduced contact adhesive force to further reduce the relay operating voltage [12]. These advancements have made it possible to investigate ultra-low-voltage MEM relay ICs.

This chapter describes the culminating steps of the journey towards achieving the first millivolt relay-based digital ICs. First an overview of basic relay operation and the fabrication process is provided. Then device design improvements, self-assembled monolayer coatings and body-biasing are described to enable relay switching with millivolt gate voltage swing and thereby millivolt relay IC operation. Next the benefit of incorporating two source-drain pairs is demonstrated to reduce circuit-design complexity. Finally, the benefit of partitioning the gate electrode to accommodate multiple input voltage signals for greater device functionality is discussed.

## 2.2 Body-biased MEM Relay Operation

An electrostatically actuated MEM relay can be modelled as a parallel plate capacitor, as shown in Fig. 2.1. The bottom plate is mechanically fixed while the top plate is movable, mechanically suspended by a spring with effective spring constant  $k$ . One plate is referred to as the *gate* electrode, while the other is referred to as the *body* electrode. The gate and body designations are interchangeable because the attractive electrostatic force is ambipolar. The electrically conducting *source* and *drain* electrodes are separated by a compressible dielectric material such as air.  $g_0$  and  $g_d$  are the as-fabricated actuation gap and contact "dimple" gap thicknesses, respectively.  $x$  is the displacement of the top plate in the direction of the bottom plate.

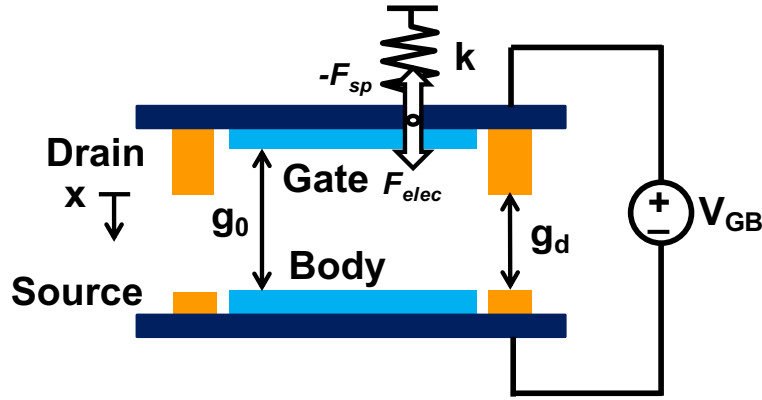


Figure 2.1: Simplified model of an electrostatically actuated parallel-plate MEM relay design incorporating two pairs of source/drain conducting electrodes for a total of 6 terminals.

With an applied voltage across the gate and body ( $V_{GB}$ ), electrical potential is converted into a force that actuates the gate toward the body and hence the drain towards the source. The spring restoring force and electrostatic force acting on the top plate can be written as:

$$F_{sp} = -kx \quad (2.1)$$

and

$$F_{elec} = \frac{1}{2} \frac{\epsilon A_{ACT}}{(g_0 - x)^2} V_{GB}^2 \quad (2.2)$$

where  $\epsilon$  is the dielectric permittivity,  $A_{ACT}$  is the overlapping area of the parallel plate capacitor, and  $\frac{\epsilon A_{ACT}}{(g_0 - x)^2}$  is the capacitance of the parallel plate capacitor. The net force is therefore:

$$\sum F = F_{sp} + F_{elec} \quad (2.3)$$

$$\sum F = 0 = -kx + \frac{1}{2} \frac{\epsilon_0 A_{ACT}}{(g_0 - x)^2} V_{GB}^2 \quad (2.4)$$

Since the electrostatic force increases superlinearly with decreasing actuation gap size, it is possible for the electrostatic actuation force to exceed the spring restoring force, resulting in instability that causes the top plate to snap down toward the bottom plate. This 'pull-in' phenomenon occurs when  $dF/dx = 0$  (as shown in Eq. 2.5); the pull-in displacement  $x_{PI}$  is the displacement of the top plate at which the instability condition occurs.

$$\frac{dF}{dx} = 0 = -k - \frac{\epsilon_0 A_{ACT}}{(g_0 - x)^3} V_{GB}^2 \quad (2.5)$$

$$k = -\frac{2}{(g_0 - x)} \left( \frac{1}{2} \frac{\epsilon_0 A_{ACT}}{(g_0 - x)^2} V_{GB}^2 \right) \quad (2.6)$$

Substituting Eq. 2.4 into Eq. 2.6, we arrive at the following:

$$k = -\frac{2}{(g_0 - x)} kx \quad (2.7)$$

Rearranging and solving for  $x = x_{PI}$ , we find the pull-in displacement for the MEM relay:

$$x_{PI} = \frac{g_0}{3} \quad (2.8)$$

A parallel-plate MEM relay can be designed to operate in pull-in (PI) mode by appropriately designing the contact dimple gap size  $g_d$  (the as-fabricated air gap thickness between the source and drain in the contact dimple region) to be greater than 1/3 of the as-fabricated actuation gap size  $g_0$ . For a MEM relay to operate in non-pull-in (NPI) mode, the ratio  $g_d/g_0$  should be less than one-third.

For PI-mode relay designs, the turn-ON voltage is found by substituting Eq. 2.8 into Eq. 2.4 and solving for  $V_{GB} = V_{ON-PI}$ :

$$V_{ON-PI} = \sqrt{\frac{8}{27} \frac{k g_0^3}{\epsilon_0 A_{ACT}}} \quad (2.9)$$

For NPI-mode relay designs, the turn-ON voltage is found by substituting  $x = g_d$  into Eq. 2.4 and solving for  $V_{GB} = V_{ON-NPI}$ :

$$V_{ON-NPI} = \sqrt{\frac{2(k g_d)(g_0 - g_d)^2}{\epsilon_0 A_{ACT}}} \quad (2.10)$$

For a MEM relay to turn off, the spring restoring force of the movable electrode structure must overcome the electrostatic actuation force plus the contact adhesive force. The force balance equation is as follows:

$$\sum F = F_{sp} + F_{elec} + F_{adh} \quad (2.11)$$

$$0 = -kx + \frac{1}{2} \frac{\epsilon_0 A_{ACT}}{(g_0 - x)^2} V_{OFF}^2 + F_{adh} \quad (2.12)$$

$$V_{OFF} = \sqrt{\frac{2(kg_d - F_{adh})(g_0 - g_d)^2}{\epsilon_0 A_{ACT}}} \quad (2.13)$$

The hysteresis voltage is defined as the magnitude of the difference between the turn-ON voltage and the turn-OFF voltage:

$$V_H = |V_{ON} - V_{OFF}| \quad (2.14)$$

For the NPI-mode MEM relay design with  $kg_d > F_{adh}$ ,  $V_H$  can be approximated [18]:

$$V_{H-NPI} = |V_{ON-NPI} - V_{OFF}| \approx F_{adh} \sqrt{\frac{2g_d}{k\epsilon_0 A_{ACT}}} \quad (2.15)$$

In order to achieve minimum switching energy, a PI-mode relay must have a relatively compliant (lower  $k$ ) structure, which makes it susceptible to stuck-ON failure [11]. Therefore, recent work has focused on body-biased NPI-mode relay designs, which can be designed with relatively higher  $k$  structures, yet still operate with very low gate voltage swing [12, 18, 20, 21]. For NPI-mode relays, the minimum switching energy is dependent on  $V_H$  which is in turn dependent on the contact adhesive force [22]. Therefore, throughout this dissertation, NPI-mode MEM relay designs are investigated unless stated otherwise.

Depending on the body bias voltage ( $V_B$ ), a relay can turn on with either increasing or decreasing gate voltage ( $V_G$ ) because of the ambipolar nature of electrostatic force. If  $V_B$  is negative, then the relay turns on with increasingly positive  $V_G$ , similarly as an n-channel MOSFET; in this case, it is referred to as a N-relay, as shown in Fig. 2.2. If  $V_B$  is positive, then the relay turns on with increasingly negative  $V_G$  or decreasingly positive  $V_G$ , similarly as a p-channel MOSFET; in this case, it is referred to as a P-relay, as shown in Fig. 2.3. Circuit symbols for N-relay and P-relay are also shown.

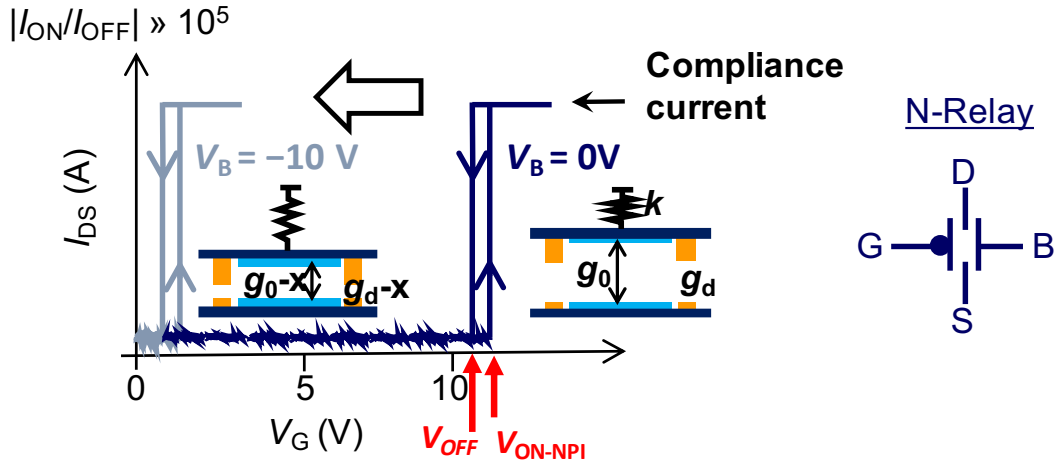


Figure 2.2: (left) By applying a negative voltage to the body electrode, the gate voltage swing required to switch a N-relay is reduced. (right) N-relay circuit symbol.

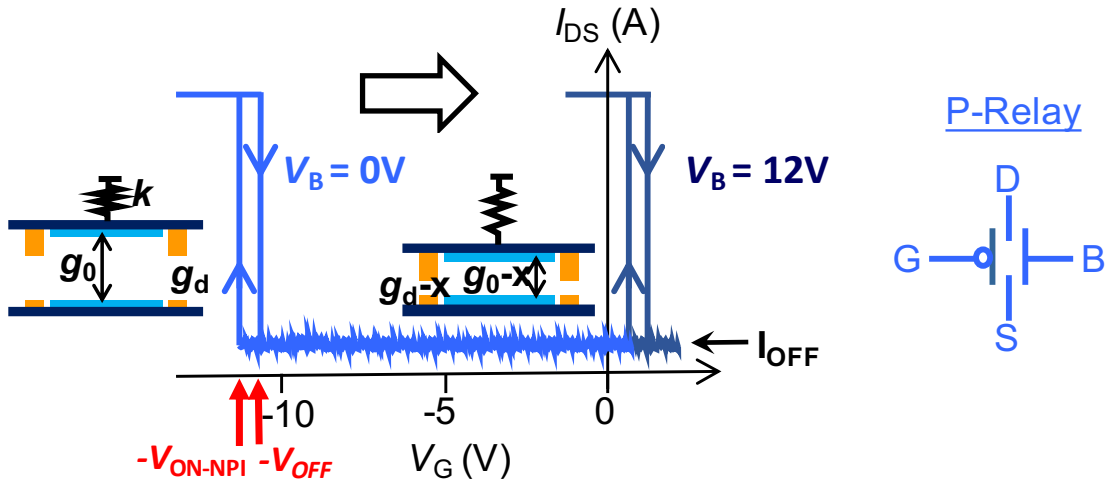


Figure 2.3: (left) By applying a positive voltage to the body electrode, the gate voltage swing required to switch a P-relay is reduced. (right) P-relay circuit symbol.

To reduce the operating voltage  $V_{DD}$  of a relay integrated circuit, body-bias voltages ( $V_{BN}$  for N-type and  $V_{BP}$  for P-type) are applied to partially actuate the relays, as shown in Figures 2.2 and 2.3, so that each one operates with gate voltage swing  $V_{SS} < V_G < V_{DD}$ . (In order to turn on a MEM relay, the difference between the applied gate and body voltages

must be greater than  $V_{ON}$ .) As can be seen from Figure 2.4,  $V_{DD}$  scaling is ultimately limited by the hysteresis voltage, *i.e.*  $V_{DD} > V_H$ .

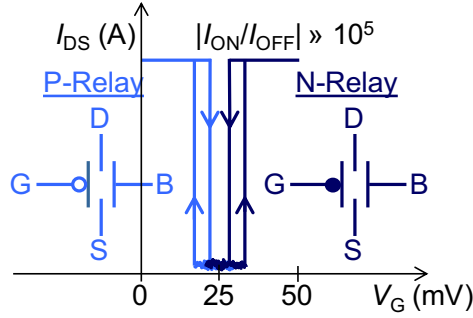


Figure 2.4: Idealized body-biased N-relay and P-relay switching characteristics allowing for millivolt integrated circuit operation ( $V_{SS} = 0V$  and  $V_{DD} = 50mV$ ).

For N-relay operation with negative  $V_B$ , the conditions for proper relay operation to turn ON and OFF in the range of  $V_{SS}$  and  $V_{DD}$  are:

$$V_{GB} \geq V_{ON-NPI} \quad (2.16)$$

and

$$V_{DD} \geq V_{OFF} + V_H + V_B \quad (2.17)$$

so that

$$-V_B < V_{ON-NPI} - V_H = V_{OFF} \quad (2.18)$$

Similarly for P-relay operation with positive  $V_B$ :

$$V_{GB} \leq -V_{ON-NPI} \quad (2.19)$$

$$V_{DD} \geq -V_{ON-NPI} + V_H + V_B \quad (2.20)$$

$$V_B > |V_{ON-NPI}| \quad (2.21)$$

In this chapter various approaches for reducing the hysteresis voltage are presented, culminating in the demonstration of MEM relay circuits operating with sub-50 mV  $V_{DD}$ .

## 2.3 MEM Relay Design and Fabrication

Figure 2.5 illustrates the structure of a 6-terminal body-biased MEM relay referred to herein as the Dual-Bridge (4C) design. The movable *gate* electrode is suspended by four folded-flexure beams over a fixed *body* electrode, and comprises two sets of *source/drain* electrodes

(*i.e.*, two electrical switches). A conductive channel layer (attached underneath the gate electrode with an intermediary insulating layer) is patterned to form a bridge for each pair of source and drain electrodes (which are formed from the same layer as the body electrode) in the ON state. As a result, there are two contact dimples (source-to-channel and drain-to-channel) for each pair of source/drain electrodes.

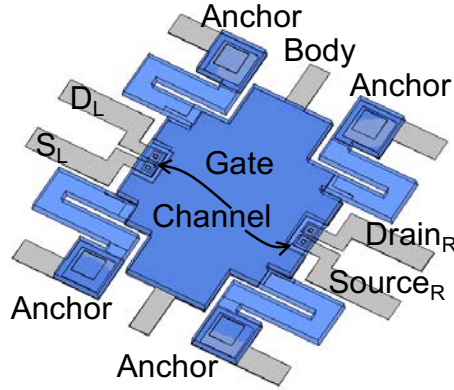


Figure 2.5: Isotropic schematic of the 4C MEM relay design, with bridging contacts between source and drain electrodes.

To reduce the hysteresis voltage, it is desirable to reduce the contact adhesive force. One approach is to reduce the contact area; however this leads to higher contact resistance. An alternative approach is to design a relay with fewer contact dimples [23].

For reduced contact adhesive force, the Dual-Direct (2C) relay design shown in Fig 2.6 was developed. Since the number of contact dimples is reduced from 4 to 2, the total contact adhesive force is reduced, thereby reducing  $V_H$ .

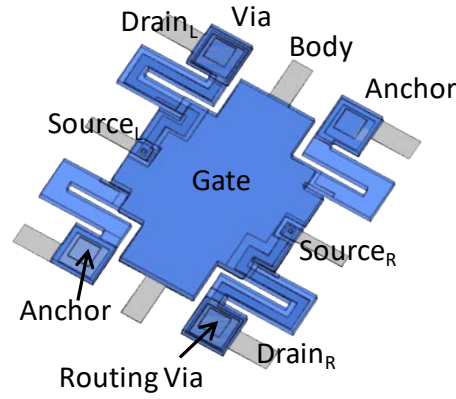
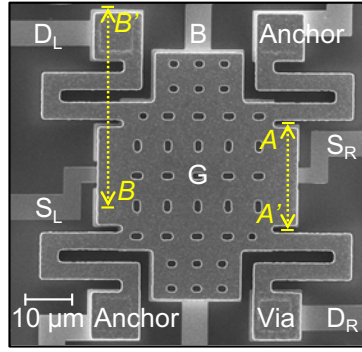


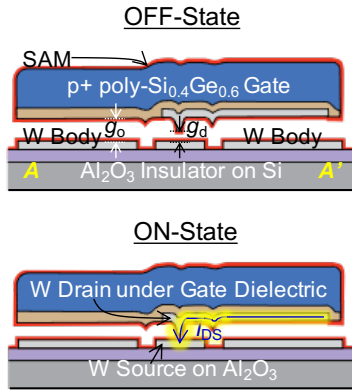
Figure 2.6: Isotropic schematic of the 2C MEM relay design with direct contact between source and drain electrodes.

A plan-view scanning electron micrograph (SEM) of a fabricated 2C relay is shown in Fig. 2.7a. As fabricated, air gaps exist between the conductive source and drain electrodes so that no current can flow between them, *i.e.*,  $I_{DS} = 0$  A (Fig. 2.7b). When a voltage ( $V_{GB}$ ) is applied between the gate and body, the movable structure is actuated downward by the electrostatic force; if  $|V_{GB}|$  is larger than a certain threshold pull-in voltage ( $V_{ON-NPI}$ ), the conductive electrodes are brought into physical contact so that current can flow between the source and drain electrodes (Fig. 2.7b). When  $|V_{GB}|$  is subsequently reduced toward 0 V, the spring restoring force of the suspension beams pulls the movable structure out of contact so that  $I_{DS}$  drops abruptly to zero at a certain release voltage ( $V_{OFF}$ ).  $V_H$  is defined as  $-V_{ON-NPI} - V_{OFF}$ .

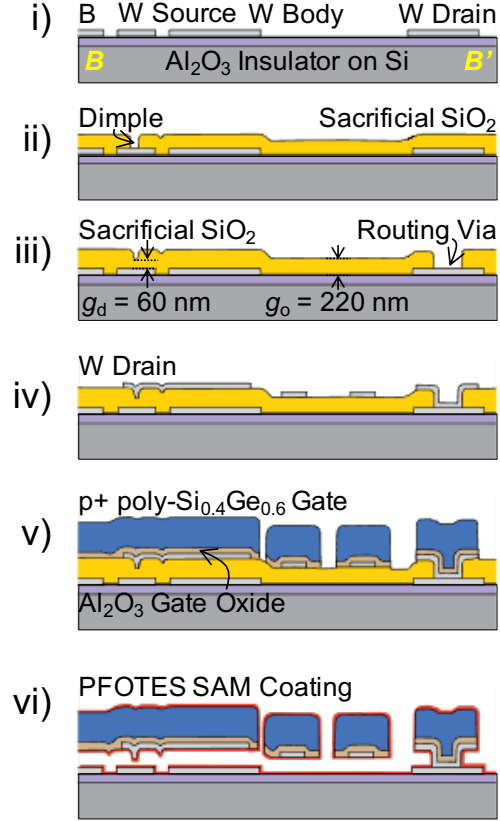
Fig. 2.7c illustrates key steps in the relay fabrication process along cutline B-B': (i) Initially, 60 nm tungsten (W) source and body electrodes are formed on an 80 nm-thick  $\text{Al}_2\text{O}_3$  insulating layer. (ii) Next, the first 160 nm-thick sacrificial  $\text{SiO}_2$  layer is then deposited, followed by contact dimple region definition. (iii) A second 60 nm-thick sacrificial  $\text{SiO}_2$  layer is deposited followed by definition of routing via regions. (iv) Afterwards, 60 nm-thick W drain electrodes are formed. (v) A 55 nm-thick  $\text{Al}_2\text{O}_3$  gate insulator is then deposited and patterned to define via/anchor regions (not shown, since these regions lie beyond the B-B' cutline), followed by 1.9  $\mu\text{m}$  heavily doped p-type poly- $\text{Si}_{0.4}\text{Ge}_{0.6}$  structural layer formation (gate electrode). (vi) Finally the structural layer is released by selectively removing sacrificial oxide layers in HF vapor. To reduce  $V_H$  further, relays were then coated with a hydrophobic anti-stiction self-assembled monolayer (SAM) of Perfluorooctyltriethoxysilane (PFOTES) using a vapor-phase process [12]. As fabricated, the relays in this work have an actuation-gap thickness ( $g_0$ ) to dimple-gap thickness ( $g_d$ ) ratio larger than three so that they operate in non-pull-in mode to avoid unnecessarily large  $V_H$  [17].



(a) Plan-view SEM of a fabricated 2C Relay.



(b) Schematic cross-sectional views of a MEM relay in the OFF state (top) and in the ON state (bottom) along cutline A-A'.



(c) Illustration of the 2C MEM relay fabrication process, along cutline B-B'.

Figure 2.7: (a) Plan view and (b) cross-sectional view of 2C dual-direct relay, and (c) fabrication process flow.

Measured  $I_{DS} - V_G$  characteristics for body-biased 2C N-relay and P-relay devices, as well as for body-biased 4C N-relay and P-relay devices, are shown in Fig. 2.8 for comparison. Immeasurably-low OFF-state leakage current and  $> 10^7$  ON/OFF current ratio are observed for all devices, as expected. Note that  $V_H$  values (summarized in Fig. 2.9) are much lower for SAM-coated relays due to reduced surface adhesive force between the contacting electrode surfaces.

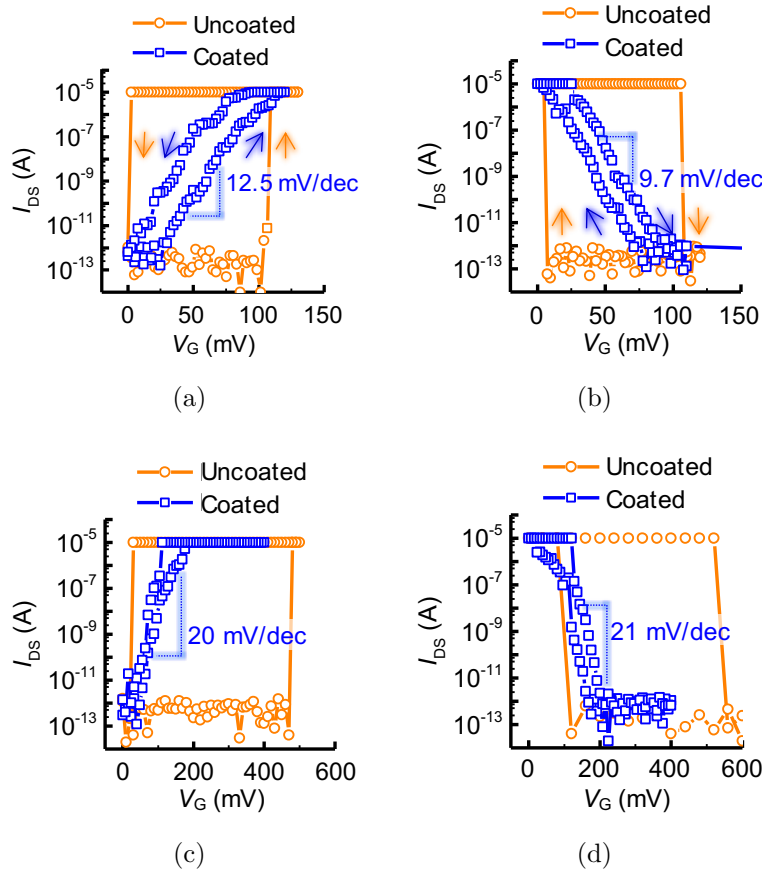


Figure 2.8: Comparison of a) N-type and b) P-type 2C dual-direct relay  $I_{DS}$  vs.  $V_G$  characteristics with c) N-type and d) P-type 4C dual-bridge relay  $I_{DS}$  vs.  $V_G$  characteristics, with and without self-assembled monolayer coating. Body-bias voltage  $|V_B| \sim 15V$ .

The reduction in  $V_H$  afforded by PFOTES coating comes with the tradeoff of increased subthreshold swing (SS), due to tunneling conduction through the PFOTES coating that is modulated by  $V_G$ . Average  $V_H$  and SS values for PFOTES-covered relays are compared for 2C and 4C relay designs in Fig. 2.9a. (The error bars indicate one standard deviation of variation, measured across eight relays.) SS is approximately twice as large for the 4C design as compared with the 2C design, since twice as much force is needed to compress the PFOTES in a 4C relay. (The PFOTES coating between the conducting electrodes can be mechanically modeled as a spring; springs in parallel combination have equivalent stiffness equal to the sum of the individual springs, as shown in the Fig. 2.9b inset.)

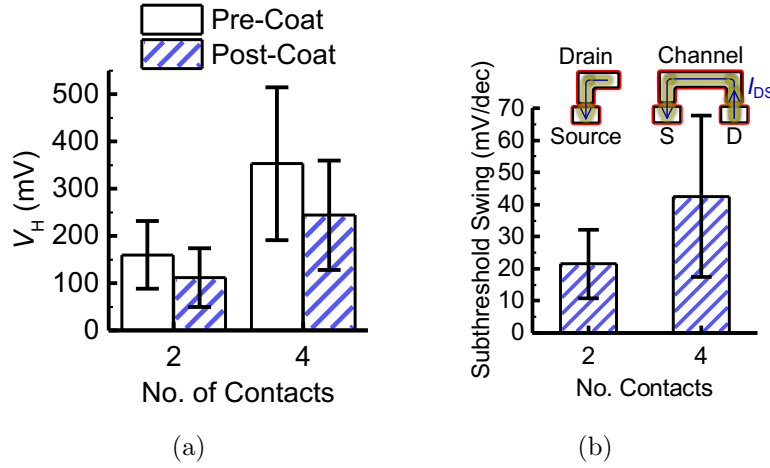


Figure 2.9: Comparison of a) hysteresis voltage ( $V_H$ ) and b) subthreshold swing (SS) values for 2C Dual-Direct and 4C Dual-Bridge relays measured at 300 K and 10  $\mu$ Torr.  $V_{DS} = 200$  mV,  $|V_B| = \sim 15$  V. The error bars indicate one standard deviation of variation, measured across eight relays.

Digital integrated circuits are implemented using the same process flow in Fig. 2.7. The interconnections between devices are formed using the same tungsten layers as the contacts of the relay. Routing vias are formed by etching through portions of the sacrificial  $\text{SiO}_2$  to form a tungsten-tungsten connection. Since the signal propagation delay in a relay-based IC is dominated by mechanical switching delay, which is much larger than RC charging/discharging delay; an optimally designed relay circuit should minimize the number of mechanical delays, *i.e.*, all relays should switch simultaneously to achieve the fastest possible circuit operation. Since each relay comprises two electrical switches, it is straightforward to implement dual-polarity pass-gate logic, *i.e.*, generate complementary output signals, which eliminates the need for inversions (incurring additional mechanical delays) along the signal path. This topology minimizes the number of mechanical delays and also the number of relays per digital function [8].

## 2.4 Multi-Function Relay Integrated Circuits

### Inverter Circuit

Fig. 2.10 shows the circuit diagram and measured voltage waveforms (timing diagram) for a relay-based inverter circuit comprising one N-relay and one P-relay with their gates connected together to receive the input signal and their drains connected together to form the output node. Note that the N-relay serves to pass  $V_{SS}$  while the P-relay serves to pass

$V_{DD}$ . The measured voltage waveforms confirm that this circuit functions properly for  $V_{DD}$  down to 50 mV.

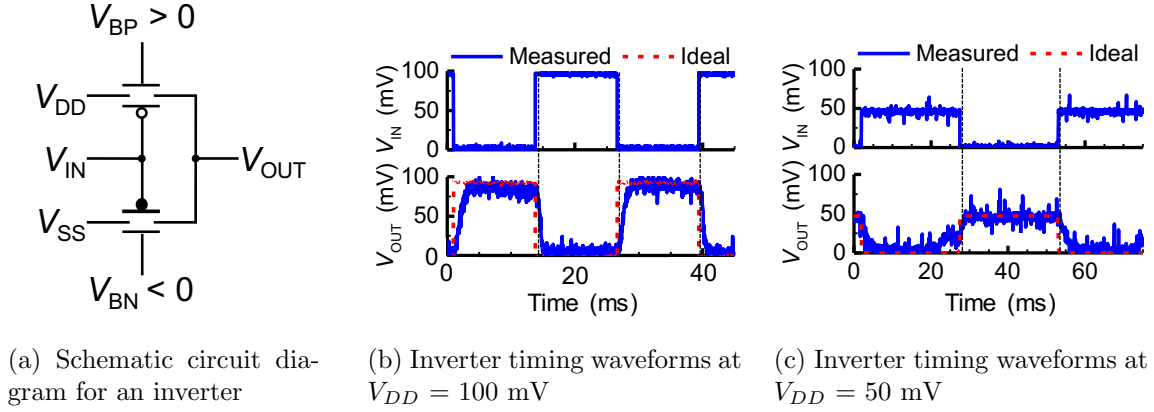


Figure 2.10: PFOTES-coated relay inverter circuit operation at 300 K and 10  $\mu$ Torr.  $|V_B| = \sim 15$  V.

## 2:1 Multiplexer Circuit (1-Bit)

The identical circuit as for the inverter can function as a 2:1 multiplexer (MUX), if configured as shown in Fig. 2.11 such that the source electrode of each relay is connected to an input signal line and the gates are connected to a select signal line. The measured voltage waveforms in Fig. 2.11 confirm that this circuit functions properly for  $V_{DD}$  down to 50 mV.

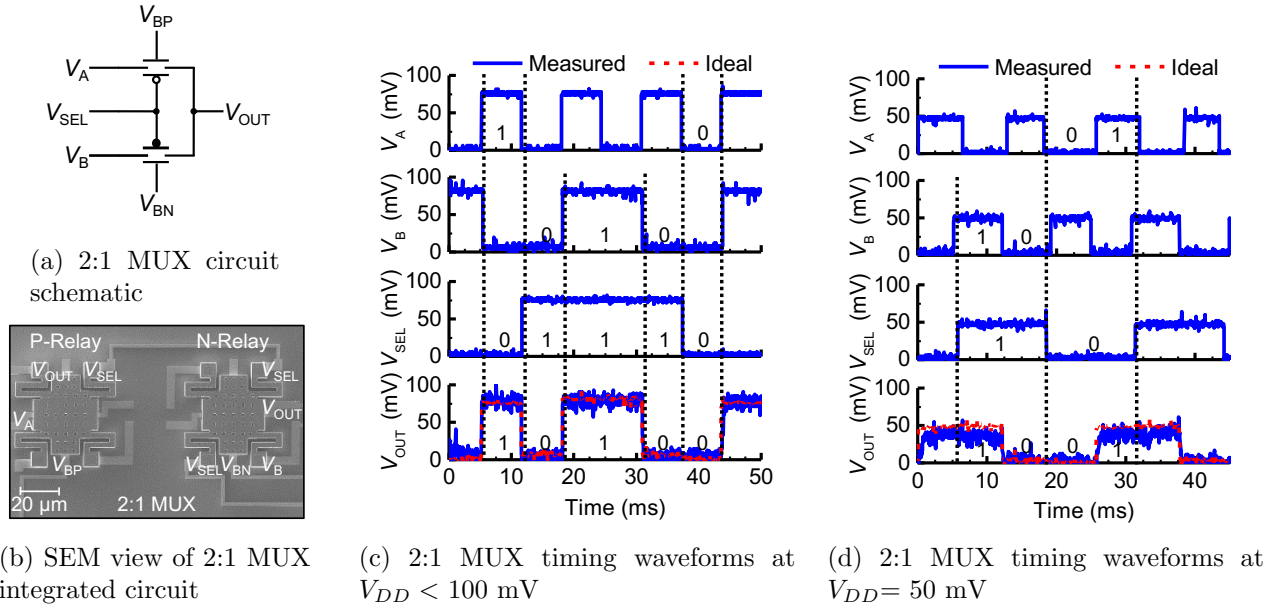


Figure 2.11: 2:1 Multiplexer pass-gate logic PFOTES-coated relay circuit operation at 300 K and 10  $\mu$ Torr.  $|V_B| = \sim 15$  V.

## XOR Circuit

Furthermore, the same physical circuit as the 2:1 MUX and Inverter circuits also can be used to implement an XOR gate, as shown in Fig. 2.12. Again, this circuit is demonstrated to function properly for  $V_{DD}$  as low as 50 mV.

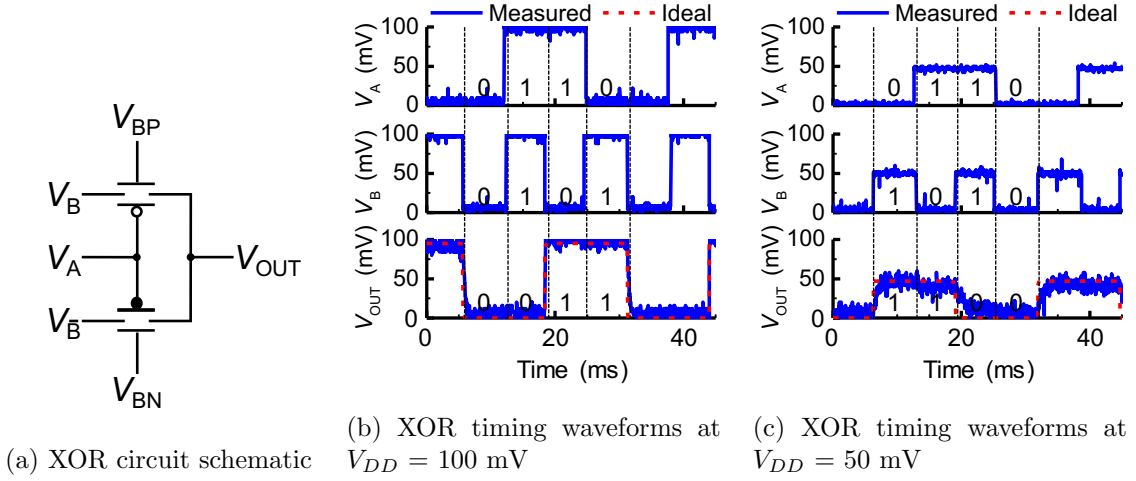


Figure 2.12: XOR circuit operation at 300 K and 10  $\mu$ Torr.  $|V_B| = \sim 15$  V. Relays were coated with PFOTES self-assembled monolayer.

## 2.5 Dynamically Reconfigurable Circuit Functionality

### AND/OR Circuit

The measured voltage waveforms in Fig. 2.13 and Fig. 2.14 are achieved with the same physical circuit but with opposite polarities of applied body bias voltages. This demonstrates the dynamically reconfigurable nature of body-biased relay ICs.

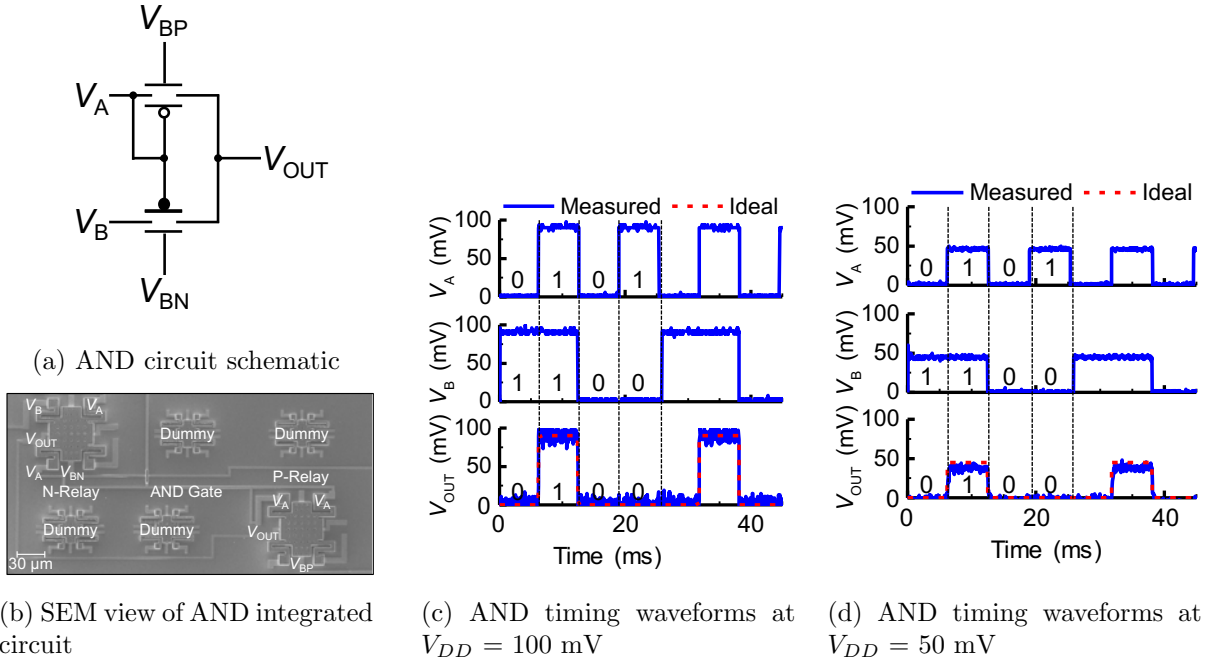


Figure 2.13: AND circuit operation at 300 K and 10  $\mu$ Torr.  $|V_B| = \sim 15$  V. Relays were coated with PFOTES self-assembled monolayer.

Note in Fig. 2.14 that the OR circuit is able to operate with 50 mV gate voltage swing, but the output voltage does not completely reach  $V_{DD}$ ; this is discussed in greater detail in Section 2.8.

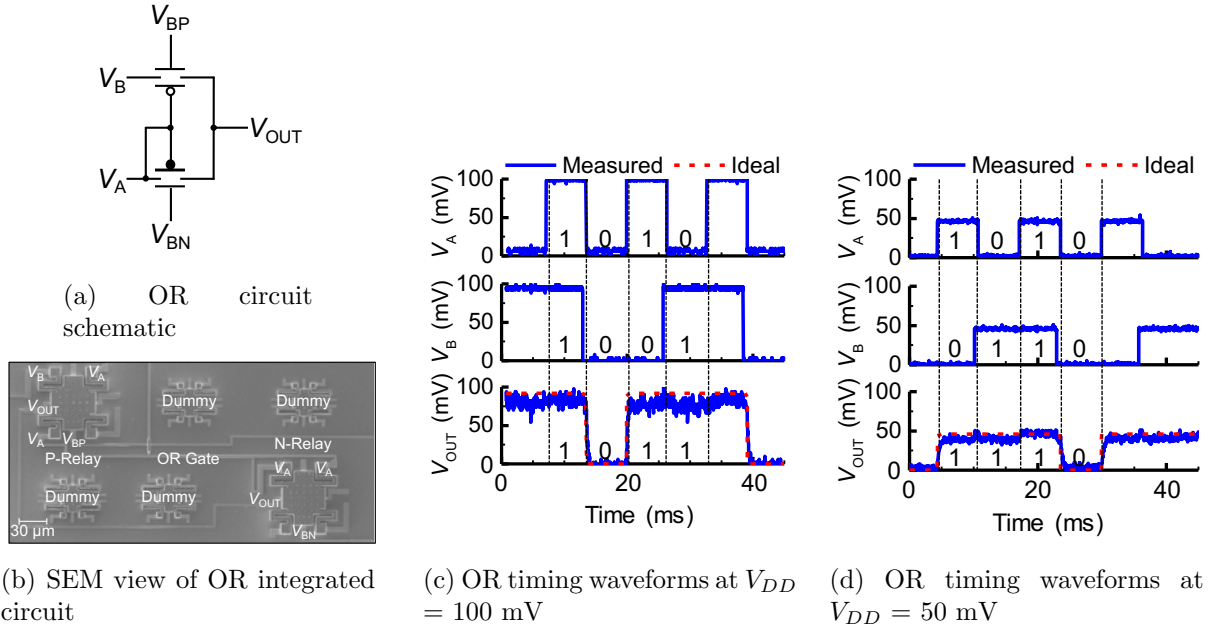


Figure 2.14: OR circuit operation at 300 K and 10  $\mu$ Torr.  $|V_B| = \sim 15$  V. Relays were coated with PFOTES self-assembled monolayer.

## Generalized Case Analysis

The example above of the AND/OR relay integrated circuit shows that it is possible to implement different functions using the same physical circuit, by changing the polarity of the relay body-bias voltages such that an N-relay operates as a P-relay and vice versa. For logic gates that are not designed as pass-gate circuits,  $V_{DD}$  and  $V_{SS}$  should also be interchanged. In general, this conversion will allow any MEM relay circuit design to also perform the corresponding contrapositive function. The contrapositive function can be derived by finding the logically equivalent function where the input signals are inverted and the output function is also inverted.

In general, the function  $f$

$$f(a, b) = y \quad (2.22)$$

has a contrapositive function  $f'$  such that

$$y = \overline{f'(\bar{a}, \bar{b})} \quad (2.23)$$

In the example of the AND/OR circuit, we can show using DeMorgan's Theorem that:

$$AND(A, B) = A \cdot B = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A} + \overline{B}} \quad (2.24)$$

Suppose there is a function  $f'$  such that  $\overline{\overline{A} + \overline{B}} = \overline{f'(\overline{A}, \overline{B})}$ . It is clear to see by inspection that  $f'$  in this case is the OR function.

Another method to determine the contrapositive function is to examine the truth table of the corresponding function. The contrapositive function can be obtained by inverting the output values of the truth table, then mirroring the truth table along the diagonal.

Below is the truth table for an AND gate:

A \ B	0	1
0	0	0
1	0	1

Inverting the output values, we arrive at:

A \ B	0	1
0	1	1
1	1	0

Mirroring the output values of the truth table along the diagonal, we arrive at the truth table output for an OR gate.

A \ B	0	1
0	0	1
1	1	1

### Example: XOR/XNOR Reconfigurable Circuit

As another example, consider the XOR gate. The contrapositive function can be found by determining the corresponding  $f'$  again:

$$XOR(A, B) = A \cdot \overline{B} + \overline{A} \cdot B = \overline{\overline{A} \cdot \overline{B} + A \cdot B} \quad (2.25)$$

Again by inspection it can be seen that the function that inverts the inputs of A,B and also the output is XNOR.

Note that while it is also possible to swap the rail voltages in a CMOS logic circuit, the output voltage swing of the CMOS-based contrapositive circuit may not fully span the range from  $V_{SS}$  to  $V_{DD}$ . Thus the ability to dynamically reconfigure a digital logic circuit to perform its contrapositive function without degrading the output voltage margins is unique to MEM relay technology.

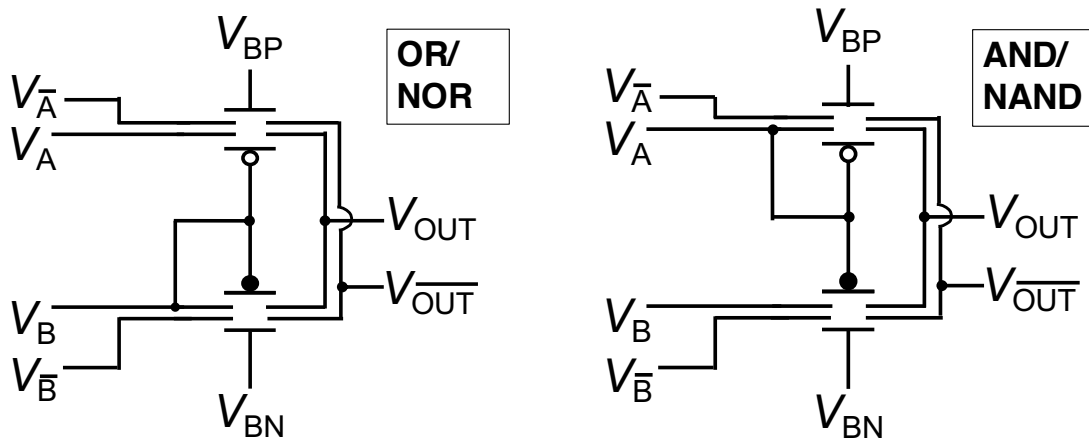
## 2.6 Multi-Output Relay Circuits

The potential for more compact circuit implementation using relays with multiple pairs of source/drain electrodes can outweigh the disadvantage of their larger hysteresis voltage due to larger contact adhesive force associated with two contact dimples *vs.* one contact dimple.

### Differential Logic MEM Relay Circuit Demonstration

By externally measuring the power consumed for certain input signals, it is possible to ‘hack’ a computer by detecting the sequence of bits of a security lock or key exchange. The use of differential logic can potentially prevent physical side-channel attacks and enable secure IC operation [24]. It is straightforward to implement differential logic using MEM relays with two pairs of source/drain electrodes to simultaneously output both a voltage signal and its complement. This circuit design style provides for uniform power dissipation, regardless of input vector sequence.

Examples of differential logic circuits implemented with dual-source/drain MEM relays are shown in Fig. 2.15:



(a) Circuit schematic for OR/NOR Gate

(b) Circuit schematic for AND/NAND Gate

Figure 2.15: Examples of differential logic gates implemented with dual-S/D MEM relays

It should be noted that differential logic circuitry typically consumes more energy compared to conventional logic circuitry. By employing MEM relays with complementary source/drain pairs, however, the dynamic power consumption due to charging and discharging the input node (gate electrode) is not necessarily higher for differential logic than for conventional logic; only the dynamic power consumption due to charging and discharging the output nodes is higher due to the additional interconnects/wires.

As a proof-of-concept, implementation of a 2-bit XOR/XNOR circuit is shown in Fig. 2.16, with 50 mV  $V_{DD}$ .

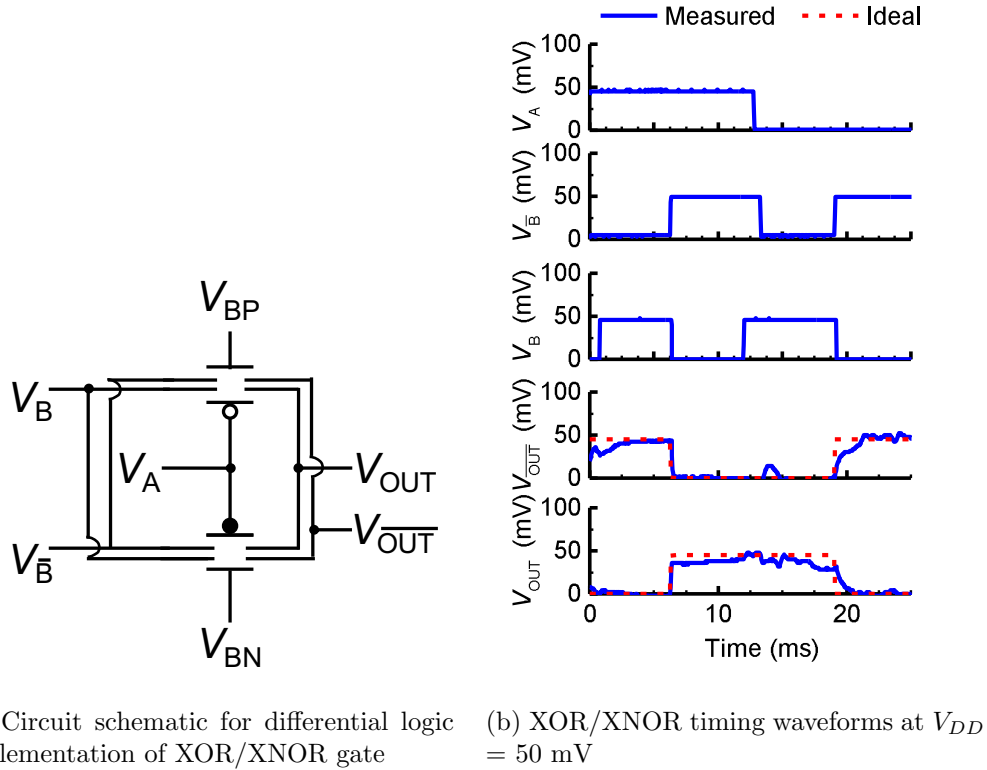


Figure 2.16: Demonstration of XOR/XNOR circuit operation at 300 K and 10  $\mu$ Torr.  $|V_B| = \sim 15$  V. Relays were coated with PFOTES self-assembled monolayer.

## Multiple-Bit "Bus" Logic Demonstration

### 2-bit 2:1 MUX

Another circuit design opportunity afforded by MEM relays is to utilize multiple source/drain pairs to pass multiple voltage signals with the same logic function, *i.e.*, implement "bus" style logic. This is useful when conducting the same logical operation on multiple bits of

information. Shown in Fig. 2.17 is a demonstration of a 2-bit 2:1 Multiplexer. The circuit is able to operate with 25 mV gate voltage swing but with the trade-off of degraded relay ON/OFF current ratio (hence higher effective on-state resistance,  $R_{ON}$ ) due to increased subthreshold swing with SAM coating; because of the finite impedance of the oscilloscope probe, the output voltage does not fully reach  $V_{DD}$  or  $V_{SS}$  (see Section 2.8).

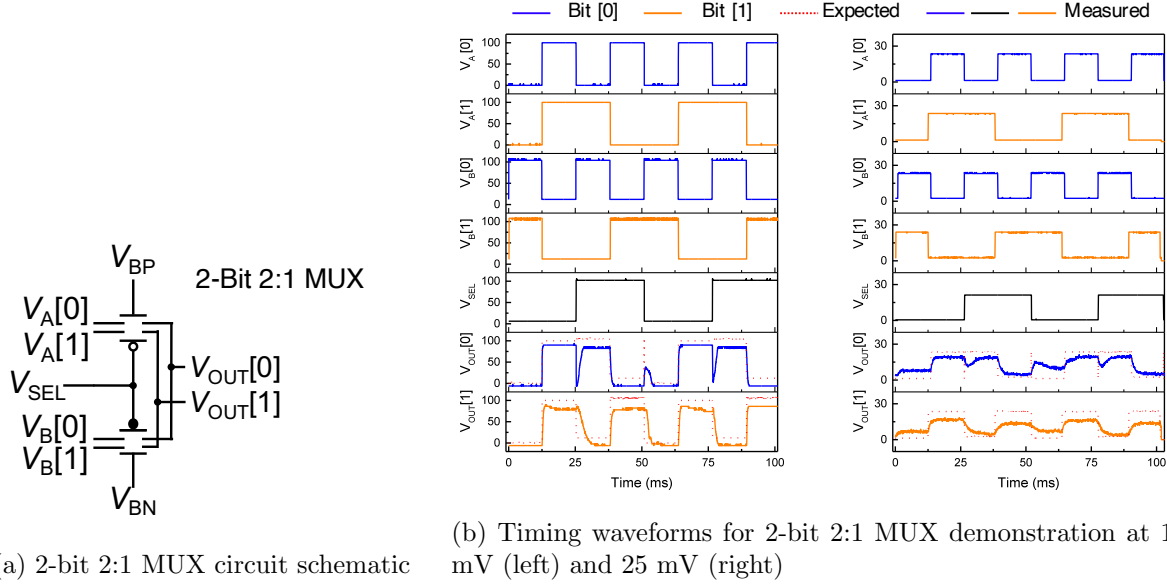


Figure 2.17: 2-bit 2:1 Multiplexer circuit operation at 300 K and 10  $\mu$ Torr.  $|V_B| = \sim 15$  V. Relays were coated with PFOTES self-assembled monolayer.

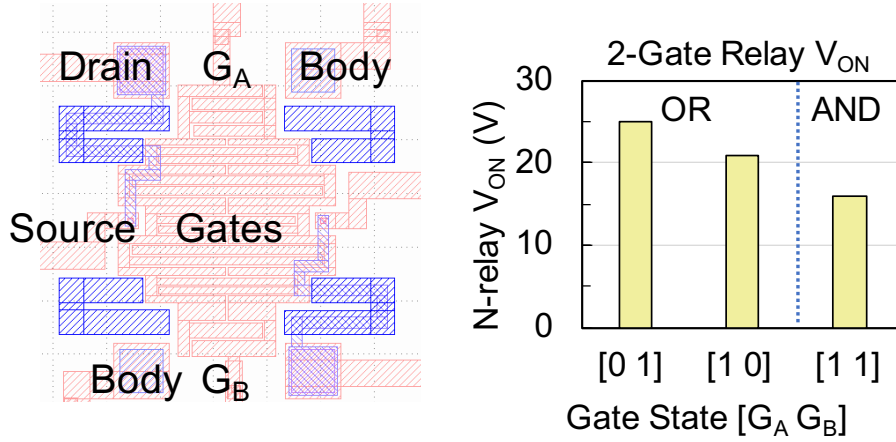
## 2.7 Multiple-Gate MEM Relays

Relay designs with the gate electrode partitioned into multiple separately driven electrodes of equal area can be used to perform various digital logic functions for the same low operating voltage ( $V_{DD}$ ), by adjusting the body bias voltage. Multiple-gate relays were previously proposed to provide for greater device functionality; however, previous demonstrations of multiple-gate relay operation used gate voltage swings in the range of 10-25 V [25]. Herein two-gate and three-gate relay designs are demonstrated to function with sub-1V gate voltage swings. The same fabrication process as in Fig. 2.7c is used to fabricate multiple-gate MEM relays, except that no anti-stiction coating is applied (unless stated otherwise).

### Two-Gate Relay

The layout of a 2-Gate relay design is shown in Fig. 2.18a to introduce the concept of multiple-gate relays. The fixed electrodes are treated as the electrical gates, named  $G_A$

and  $G_B$ , respectively, while the movable electrode suspended over the gates (not shown, for clarity) is considered to be the body electrode. The gates have roughly equal actuation area. The state of the gate voltage signals is denoted as  $[G_A \ G_B]$ , using ‘0’ to indicate 0 V applied voltage on the corresponding gate electrode and ‘1’ to indicate non-zero applied voltage. Measured turn-on voltages for each gate are shown in Fig. 2.18b.



(a) Computer-aided design layout of a 2-Gate relay showing the fixed electrode layer patterned to form interdigitated gate electrodes  $G_A$  and  $G_B$ .

(b) Measured N-relay turn-on voltages for various Gate States, measured at 300 K at 10  $\mu$ Torr.  $V_B = 0$  V.

Figure 2.18: Layout and measured  $V_{ON}$  values for a 2-Gate relay.

Depending on the absolute value of the body bias voltage, such a device can perform either an AND or OR switching function. Thus, the functionality of a MEM relay is dynamically tunable. A non-ideal aspect of this particular 2-Gate relay design is that the overlap between the body and the gate is slightly different for the two gate electrodes  $G_A$  and  $G_B$ , resulting in slightly different turn-on voltages. This issue is rectified in the 3-Gate MEM relay design described below.

### Three-Gate Relay

Fig. 2.19 shows the structure of a 3-Gate MEM relay comprising three *gate* electrodes ( $G_A$ ,  $G_B$ ,  $G_C$ ) of equal actuation area ( $A_A$ ,  $A_B$ ,  $A_C$ ), one *body* electrode and two pairs of *source-drain* electrodes. The movable polycrystalline silicon-germanium body electrode is suspended over the three fixed tungsten gate electrodes by four folded-flexure suspension beams. When electrostatic force ( $F_{elec}$ ) induced by applying voltage(s) to one or more of the gate electrodes relative to the body electrode exceeds a threshold level, the body is actuated downward sufficiently to bring each of the drain electrodes (attached underneath

the body via an intermediary insulating layer of aluminum oxide) into physical contact with their corresponding source electrode, turning ON the relay so current ( $I_{DS}$ ) can flow between each source-drain pair. To turn OFF the relay,  $F_{elec}$  must be reduced below the threshold level such that the spring restoring force of the beams ( $F_{sp}$ ) exceeds  $F_{elec}$  plus the contact adhesive force ( $F_{adh}$ ), causing the source and drain electrodes to break contact. Due to non-zero  $F_{adh}$ , the magnitude of the turn-off voltage ( $|V_{OFF}|$ ) is always smaller than the magnitude of turn-on voltage ( $|V_{ON}|$ ). The hysteresis voltage  $V_H = |V_{ON} - V_{OFF}|$ .

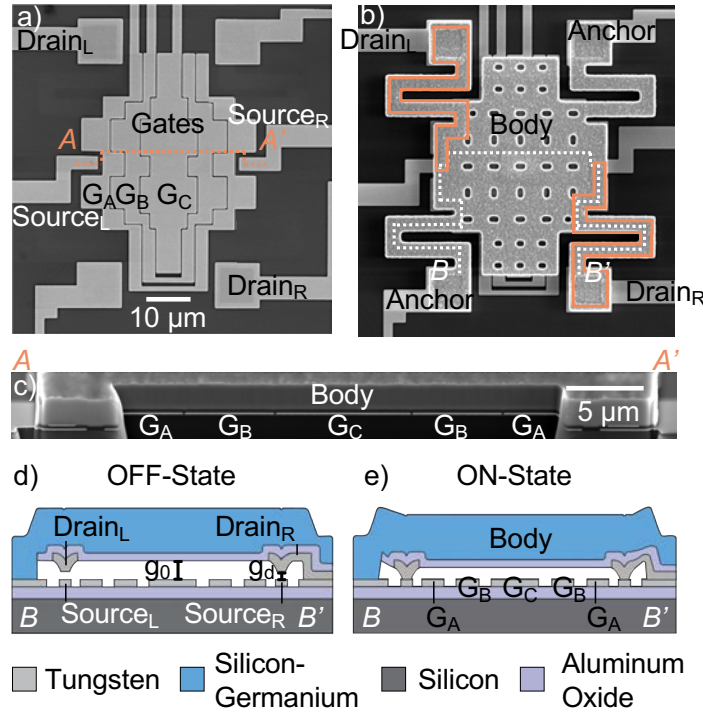


Figure 2.19: SEM images of the 3-input MEM relay. (a) Plan view of the patterned electrode layer, and (b) plan view of the completed relay. (c) A-A' cross-section. B-B' cross-section schematics in the (d) OFF state and (e) ON-state.

If a positive voltage is applied to the body, then the relay can be switched ON by lowering the gate voltage to increase  $F_{elec}$ ; in this case the relay behaves similarly as a p-channel MOSFET and hence is referred to as a P-relay. In contrast, for negative body bias, the relay is switched ON by raising the gate voltage to increase  $F_{elec}$ ; in this case the relay behaves similarly as an n-channel MOSFET and hence is referred to as a N-relay. P-relay and N-relay circuit symbols and generic current-vs.-voltage (I-V) characteristics are shown in Fig. 2.20.

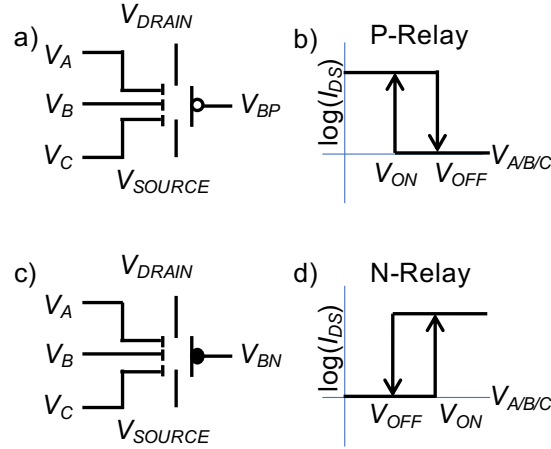


Figure 2.20: Three-gate (a) P-relay circuit symbol and (b) I-V characteristics. Three-gate (c) N-relay circuit symbol and (d) I-V characteristics.

Herein the logic state of the gate voltage signals is denoted as  $[G_A \ G_B \ G_C]$ , using ‘0’ to indicate low voltage and ‘1’ to indicate a non-zero voltage. Fig. 2.20 shows measured  $V_{ON}$  values for various combinations of switching gate voltage signals, for N-relay and for P-relay operation, with zero body bias.  $V_{ON}$  was determined by sweeping one or more gate voltages using a Keithley 4200A and measuring  $I_{DS}$ . If only one gate is switching, a larger magnitude gate voltage is needed to induce sufficient electrostatic force to turn on the relay, since the effective actuation area is smaller than with multiple gates simultaneously switching. As the number of switching gates increases, the effective actuation area increases, so a lower magnitude gate voltage is sufficient to induce the electrostatic force needed to turn on the relay. Depending on the gate operating voltage ( $V_{DD}$ ), the relay can act as an AND gate (smallest  $|V_{DD}|$ ), a MAJORITY gate or an OR gate (largest  $|V_{DD}|$ ).

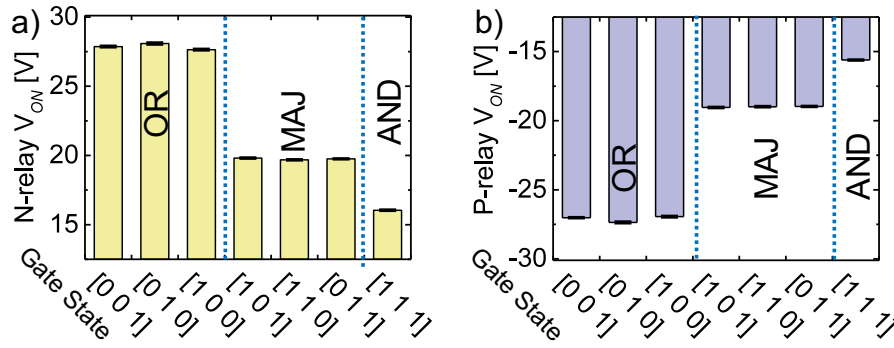


Figure 2.21: Measured average  $V_{ON}$  values for different combinations of switching gate voltage signals, with  $V_B = 0$  V, for (a) N-relay and (b) P-relay operation. Error bars indicate  $\pm 1$  standard deviation measured across 10  $I_{DS}$ - $V_{A/B/C}$  DC sweeps for one relay.

### Body-Biased Operation

By applying a non-zero bias voltage to the body electrode (to actuate it part way), the gate voltage required to turn ON the relay can be reduced. Furthermore, as shown in Fig. 2.22a, by adjusting the body bias voltage ( $V_B$ ), the number of gates  $N$  that must be in state ‘1’ (with an applied voltage of  $V_{DD}$ ) in order to turn ON the N-relay can be varied. The following force balance equation can be solved to find the value of  $V_B$  required in order for the relay to turn ON with  $N$  gates in state ‘1’:

$$\frac{1}{2} \frac{\epsilon_0 A}{(g_0 - g_d)^2} (N(V_{DD} + |V_B|)^2 + (3 - N)V_B^2) = k g_d \quad (2.26)$$

where  $k$  is the effective spring constant, and  $A$  is the actuation area of one of the three equally-sized gates. Therefore, by adjusting  $V_B$ , different relay switching functionality can be achieved: AND (with lowest  $|V_B|$  such that all of the gates must be at  $V_{DD}$  to induce sufficient additional electrostatic force to turn ON the N-relay), MAJORITY or OR (with highest  $|V_B|$  such that only one of the gates must be at  $V_{DD}$  to induce sufficient additional electrostatic force to turn ON the N-relay). Fig. 2.22b shows analogous multi-functionality for the P-relay.

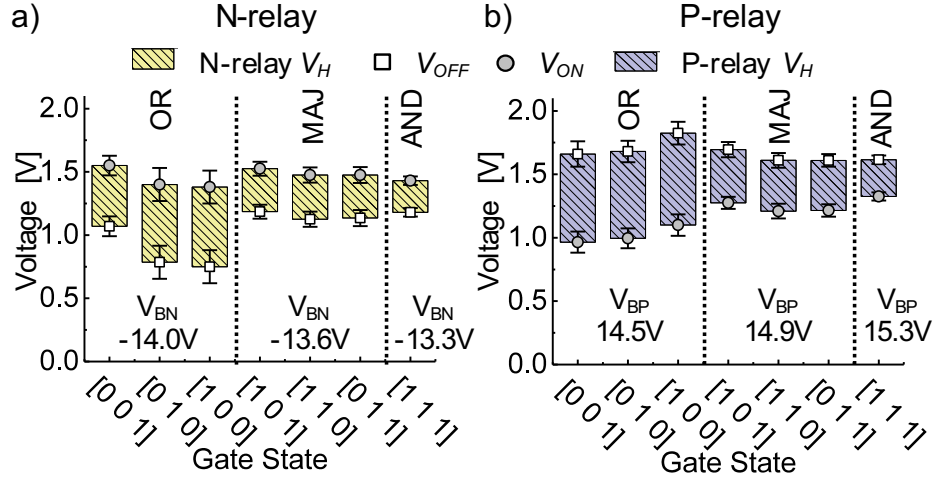


Figure 2.22: Measured average values of  $V_{ON}$  and  $V_{OFF}$  for different combinations of switching gate voltage signals, with body biasing, for (a) N-relay and (b) P-relay operation. Error bars indicate  $\pm 1$  standard deviation, measured across 10  $I_{DS}$ - $V_{A/B/C}$  DC sweeps for one relay.

The lower limit for  $V_{DD}$  is equal to  $V_H$ ; therefore, both  $V_{ON}$  values and  $V_{OFF}$  values are plotted in Fig. 2.22. It can be seen that  $V_H$  is larger for fewer transitioning input voltage signals. This is because a larger change in gate voltage is needed to effect the required reduction in  $F_{elec}$ , if the effective actuation area of the switching input voltage signal is smaller. To turn OFF the N-relay with  $N$  gates switching from state ‘1’ to state ‘0’, the following inequality must be satisfied:

$$\frac{2}{\epsilon_0}(g_0 - g_d)^2(F_{sp} - F_{adh}) > N(V_{OFF} + |V_B|)^2 + (3 - N)V_B^2 \quad (2.27)$$

By solving Equations 2.26 and 2.27, we can determine the expected turn-ON and turn-OFF voltages at each switching condition. Fig. 2.23 plots theoretically calculated values of  $V_H$  against measured values, for all possible gate switching voltage combinations that turn OFF the N-relay. For each combination,  $V_B$  was adjusted for  $V_{DD} = 1.5V$ ; that is,  $|V_B|$  is larger for the cases where more gates start (and end) in the ‘0’ state, *i.e.*, the N-relay was turned ON with fewer gates in the ‘1’ state. It can be seen from Fig. 2.23 that  $V_H$  is smaller if more gates are transitioning from the ‘1’ state to ‘0’ state; this is because the effective actuation area is larger, so a smaller reduction in gate voltage is needed to effect the necessary reduction in electrostatic force to turn OFF the relay. Also, for the same number of transitioning gates, the calculated  $V_H$  is slightly smaller for larger  $|V_B|$  because the gate voltage swing required for switching is smaller. It can be seen that the measured

values are well explained by theory, and that the minimum operating voltage of this relay is approximately 0.75 V.

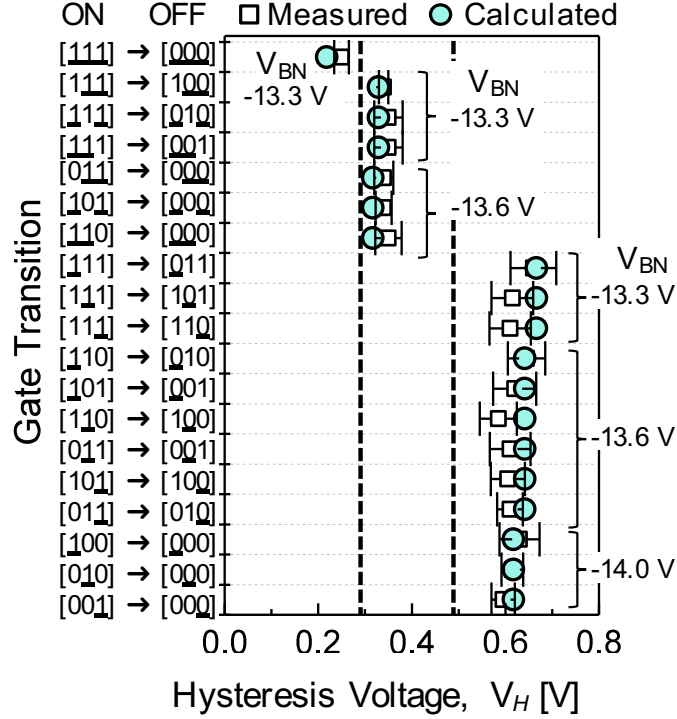


Figure 2.23: Measured and calculated values of  $V_H$  for N-relay operation, for different turn-OFF gate switching voltage combinations.  $V_B$  was adjusted so that  $V_{DD} = 1.5$  V. Error bars indicate  $\pm 1$  standard deviation, measured across 10  $I_{DS}$ - $V_{A/B/C}$  DC sweeps for one relay.

Fig. 2.24 plots a comparison of the calculated  $V_H$  if  $|V_B|$  is adjusted such that  $V_{DD} = 1.5$  V *vs.* the calculated  $V_H$  without body bias ( $V_B = 0$  V). Including the effect of the body-bias voltage  $|V_B|$  increases the hysteresis voltage (if one or more gates start (and end) in the ‘0’ state) because of the reduction in gate switching voltage ( $V_{DD}$ ) contributing to reduced difference in  $F_{elec}$ . However, the maximum calculated hysteresis voltage remains the same.

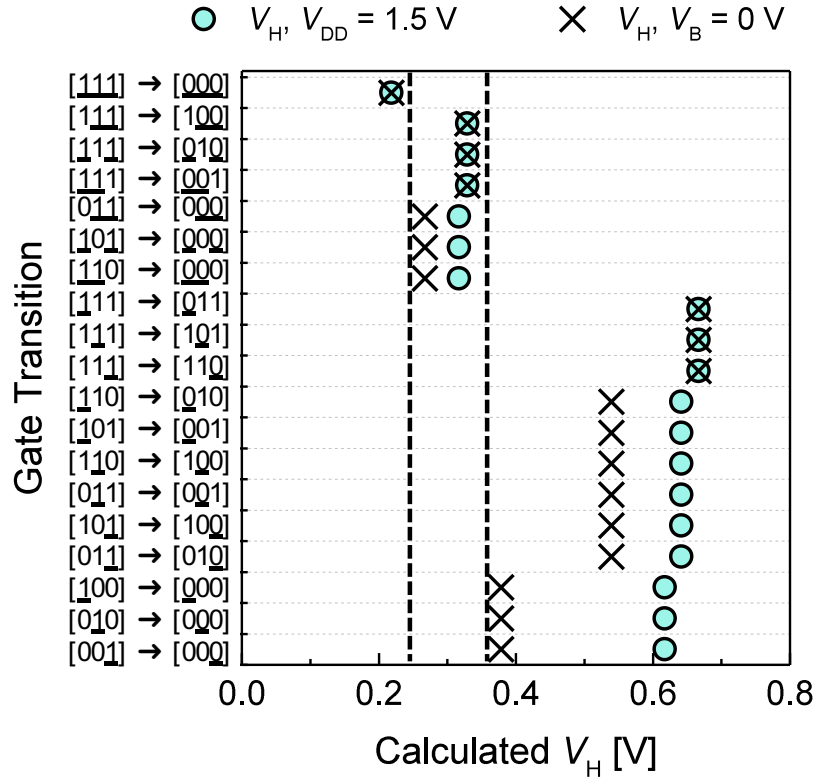


Figure 2.24: The effect of body bias on  $V_H$  for each different gate transition.  $V_H$  was calculated for  $V_B = 0 \text{ V}$ , as well as for varied  $V_B$  such that  $V_G = 1.5 \text{ V}$ .

### Complementary Multiple-Gate Relay Operation

The voltage at the output node of a digital logic circuit should be driven either high (corresponding to logic state ‘1’) or low (corresponding to logic state ‘0’). Therefore, two relays - one to pull-up the output node to  $V_{DD}$  and the other to pull-down the output node to  $V_{SS}$ , operating in a complementary manner are needed to implement a logic gate. Depending on the circuit configuration, the 3-Gate MEM relay can function either as a pull-up (P-U) switch (Fig. 2.25a) or as a pull-down (P-D) switch (Fig. 2.25b), with AND, OR or MAJORITY functionality.

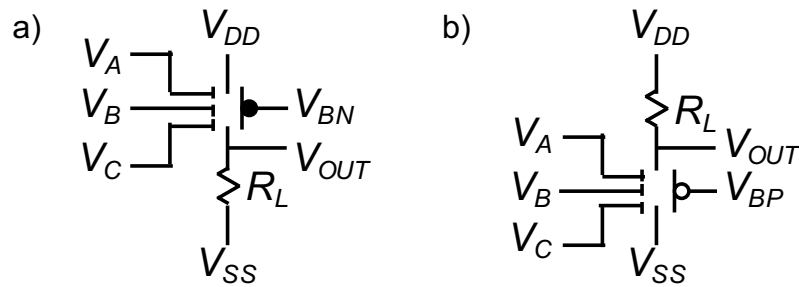


Figure 2.25: Circuit diagrams for (a) N-relay acting as a pull-up (P-U) switch and P-relay acting as a pull-down (P-D) switch.  $R_L = 100 \text{ k}\Omega$ .

Measured voltage waveforms are shown in Fig. 2.26 and compared against expected waveforms, for all possible ON and OFF transitions of the logic gate. It can be seen that the relay functions with versatility as expected.

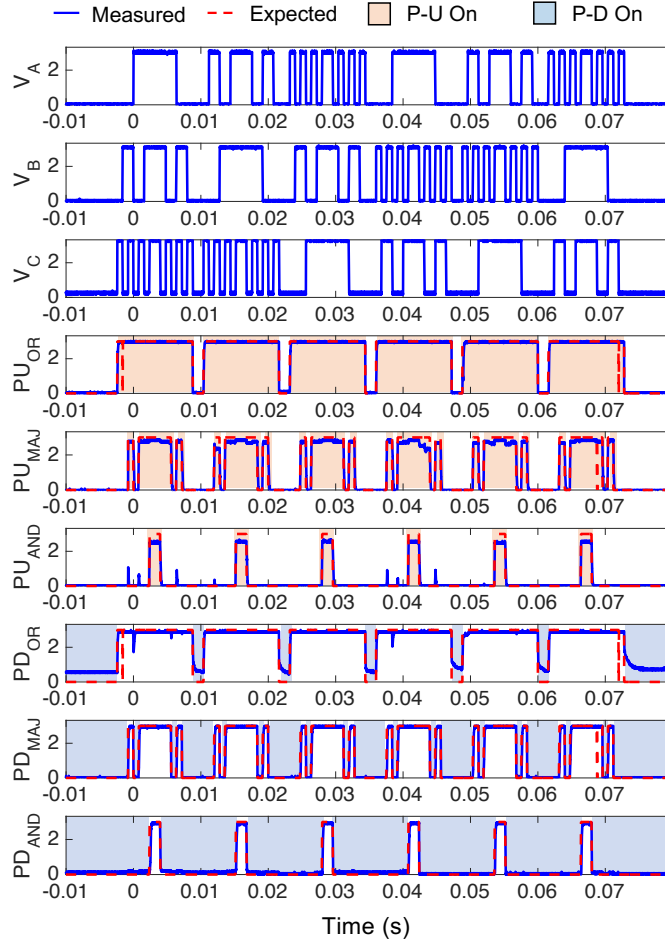


Figure 2.26: Voltage waveforms demonstrating versatile functionality of a 3-input MEM relay acting as a N-relay pull-up (P-U) switch or as a P-relay pull-down (P-D) switch with AND, OR or MAJORITY functionality.

With a PFOTES self-assembled monolayer coating applied, the hysteresis voltage is reduced so that the 3-Gate relay operates with an input (gate) voltage swing of 275 mV, as shown in Fig. 2.27. Note that the output voltage swing does not reach  $V_{DD}$  in some cases, due to high effective ON-state resistance with SAM coating (see Section 2.8). In addition, due to non-zero strain gradient in the polycrystalline silicon-germanium structural layer, the movable body electrode tends to deflect out-of-plane upon being released, resulting in slight variations in the as-fabricated actuation gap ( $g_0$ ) for the different gates of the device (because the actuation gap near the center of the body is larger than the actuation gap near the perimeter of the body). Such differences in actuation gap can cause milli-Volt differences in the turn-OFF and turn-ON voltages for the different gates, which become significant for

sub-1 V  $V_{DD}$  operation. Thus it can be seen that in Region I, when  $G_C$  (with the largest actuation gap and hence largest turn-OFF voltage) turns OFF, the MAJ output voltage does not reach  $V_{SS}$  ( $V_{OUT} \sim 100$  mV). Next, if  $G_B$  turns OFF as shown in Region II, the MAJ output voltage comes somewhat closer to  $V_{SS}$  ( $V_{OUT} \sim 50$  mV). If  $G_A$  and  $G_B$  both turn OFF in Region III, the MAJ output voltage is finally able to reach  $V_{SS}$ .

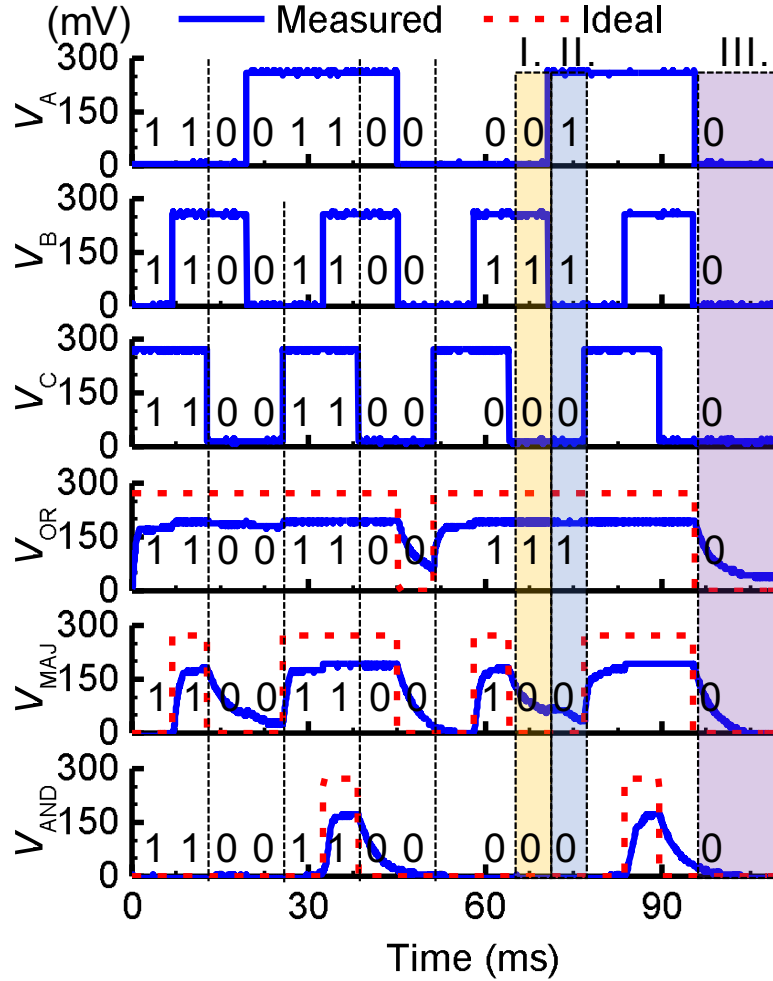


Figure 2.27: Voltage waveforms demonstrating a SAM-coated 3-Gate MEM relay operating as a pull-up (P-U) switch with AND, OR or MAJORITY functionality for  $V_{DD} < 275$  mV at 300 K.

### Generalized Case: Maximum Number of Gates

In principle, more complex logic functions can be implemented by a pair of complementary relays if the number of gate electrodes is increased. This increased functionality comes at the cost of larger operating voltage  $V_{DD}$  (hence switching energy  $E_{tot}$ ) because the hysteresis voltage increases with decreasing effective actuation area; therefore, there may be a practical upper limit for the number of gate electrodes. Suppose  $M$  is the number of equally sized gate electrodes,  $A_0$  is the total actuation area of all of the gates, and each gate has actuation area  $A_0/M$ . The maximum switching hysteresis voltage can be derived as follows, where we assume NPI-mode operation for simplicity.

The generalized versions of the equations for turn-ON voltage (Eq. 2.26) and turn-OFF voltage (Eq. 2.27) for  $M$  gates are derived as follows:

To calculate  $V_{ON}$ :

$$\frac{1}{2} \frac{\epsilon_0}{(g_0 - g_d)^2} \sum_{m=1}^M A_m (V_{ON} - V_B)^2 = k g_d \quad (2.28)$$

To calculate  $V_{OFF}$ :

$$\frac{2}{\epsilon_0} (g_0 - g_d)^2 (k g_d - F_{adh}) > \sum_{m=1}^M A_m (V_{OFF} - V_B)^2 \quad (2.29)$$

where  $A_m = A_0/M$  is the actuation area of each gate.

To derive the maximum hysteresis voltage, we can consider the worst-case hysteresis voltage, which occurs in the gate transition where the relay begins with all gates ON ( $M$ ), then transitions to one gate OFF ( $M - 1$ ). In this case, Equation 2.28 simplifies to:

$$V_{ON_M} = \sqrt{\frac{2k g_d (g_0 - g_d)^2}{\epsilon_0 A_0}} \quad (2.30)$$

and Equation 2.29 simplifies to:

$$\frac{1}{2} \frac{\epsilon_0 A_0 (M - 1)}{M (g_0 - g_d)^2} \left( \frac{2k g_d (g_0 - g_d)^2}{\epsilon_0 A_0} \right) + \frac{1}{2} \frac{\epsilon_0 A_0}{M (g_0 - g_d)^2} V_{OFF_{M-1}}^2 = k g_d - F_{adh} \quad (2.31)$$

$$\frac{1}{2M} \left( (M - 1)(2k g_d) + \frac{\epsilon_0 A_0}{(g_0 - g_d)^2} V_{OFF_{M-1}}^2 \right) = k g_d - F_{adh} \quad (2.32)$$

$$V_{OFF_{M-1}} = \sqrt{\frac{(g_0 - g_d)^2 [-(M-1)(2kg_d) + 2M(kg_d - F_{adh})]}{\epsilon_0 A_0}} \quad (2.33)$$

Solving for  $V_H$ :

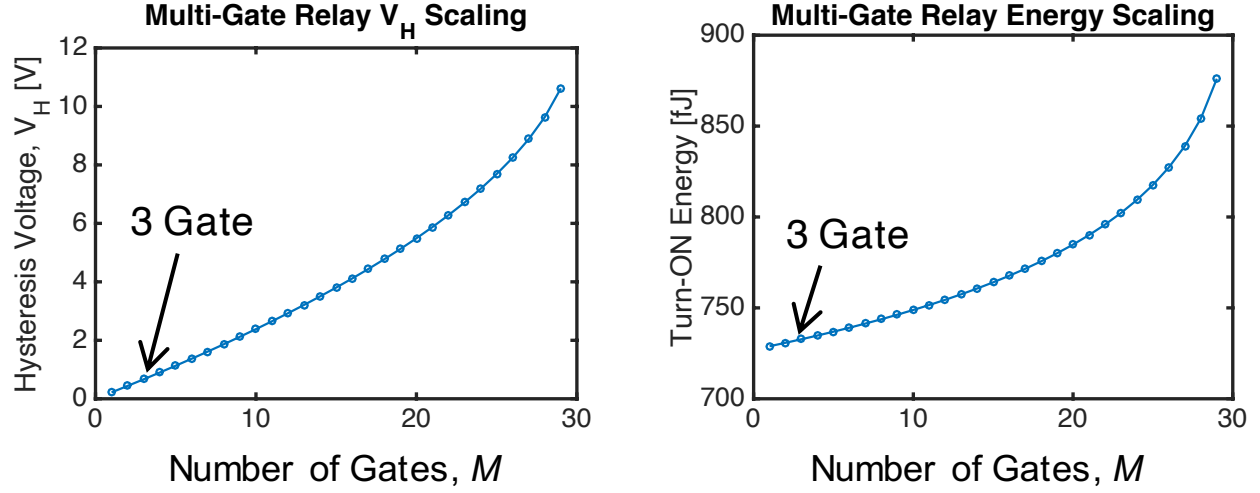
$$V_H = \sqrt{\frac{2kg_d(g_0 - g_d)^2}{\epsilon_0 A_0}} - \sqrt{\frac{(g_0 - g_d)^2 [2M(kg_d - F_{adh}) - (M-1)(2kg_d)]}{\epsilon_0 A_0}} \quad (2.34)$$

$$V_H = \frac{g_0 - g_d}{\sqrt{\epsilon_0 A_0}} \sqrt{2kg_d} \left[ 1 - \sqrt{M \left( 1 - \frac{F_{adh}}{kg_d} \right) - (M-1)} \right] \quad (2.35)$$

$$V_H = \sqrt{\frac{2kg_d(g_0 - g_d)^2}{\epsilon_0 A_0}} \left[ 1 - \sqrt{1 - \frac{MF_{adh}}{kg_d}} \right] \quad (2.36)$$

$$V_H = V_{ON-NPI} \left[ 1 - \sqrt{1 - \frac{MF_{adh}}{kg_d}} \right] \quad (2.37)$$

where  $V_{ON-NPI}$  is the turn-ON voltage for a relay with one gate electrode with area  $A_0$ . If  $MF_{adh} > kg_d$ , the spring restoring force is insufficient to overcome  $F_{elec} + F_{adh}$  and thus the relay will be stuck ON. If  $F_{adh} = 1.4\mu\text{N}$ , the maximum number of gate electrodes is 30, as shown in Fig. 2.28. This implies an interesting energy-delay tradeoff to explore in the future between the energy required to switch ON the relay vs. the potential circuit-level savings of reducing circuit complexity with multiple-gate relays.



(a) Trend in hysteresis voltage as the number of gates in a multi-gate relay of total actuation area  $A_0$  increases.

(b) Trend in switch-ON energy as the number of gates in a multi-gate relay of total actuation area  $A_0$  increases.

Figure 2.28: Trend in scaling the number of  $M$  gates of equal actuation area, in a multi-input relay of total actuation area  $A_0$ .

## 2.8 Non-Idealities in Relay Performance

For some of the circuit demonstrations above, the output voltage swing was less than  $V_{DD}$ . From Fig. 2.9b, it can be seen that there is some variation in SS for SAM-coated relays, which indicates that the coating process was non-uniform. For very low operating voltage, poor SS results in lower ON-state current (nA range for  $V_{DD} = 50$  mV, cf., Fig. 2.8) and hence higher effective on-state resistance  $R_{ON}$ . In this work, the output voltage waveforms were measured using an oscilloscope probe with internal resistance ( $R_{OSC}$ ) of 10 M $\Omega$ , which is not much larger than  $R_{ON}$  for relays with poor SS operating at very low  $V_{DD}$ . As a result, the output voltage does not reach  $V_{DD}$  in some cases (for example, Fig. 2.14d) due to the resistive voltage divider effect modeled by the equivalent circuit shown in Fig. 2.29. When either the N-relay or P-relay is turned on (and the input voltage at the corresponding source of the relay is  $V_{DD}$ ), the voltage divider consisting of  $R_{ON}$  connected in series with  $R_{OSC}$  limits the output voltage to be less than  $V_{DD}$ . If both relays are turned on, the output voltage swing changes depending on the input voltages and  $R_{ON}$  of each relay. It should be noted that, since relays have nearly infinite OFF-state resistance (in contrast to the  $R_{OSC}$  of the oscilloscope) due to zero OFF-state leakage, high effective  $R_{ON}$  should not prevent proper operation of relay-based ICs with complementary logic. Nevertheless, improvement in the uniformity of the SAM coating process is expected to provide for uniformly low SS (and thereby low  $R_{ON}$ ) in the future.

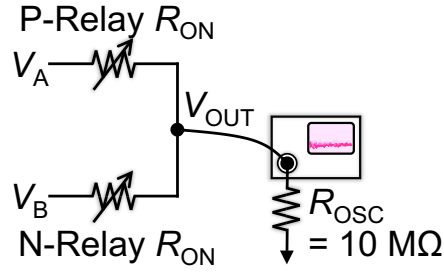


Figure 2.29: Equivalent circuit for relay measurement setup, explaining the high on-state resistance  $R_{ON}$  with subthreshold swing due to self-assembled monolayer.

It is also important to consider the mechanical switching delay of MEM relays. Fig. 2.30 shows how the mechanical turn-ON delay ( $\tau_{ON}$ ) of the 2C relay can be improved by increasing  $V_{DD}$ , albeit at a tradeoff of higher dynamic power consumption. In this measurement, a 2C relay is measured in vacuum conditions with  $V_G$  varied from 50mV to 750mV,  $V_B = -14.3$  V, and  $V_{DS} = 2$  V. It is shown that the turn-ON delay is less than  $1.5 \mu\text{s}$ .

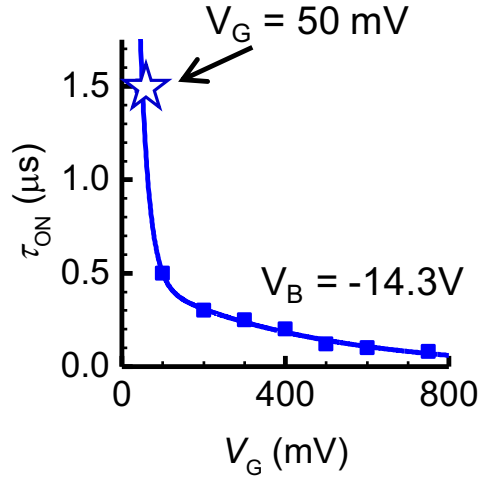


Figure 2.30: Measured 2C MEM relay turn-on delay  $\tau_{ON}$  vs.  $V_G$  at 300 K and  $10 \mu\text{Torr}$ .  $V_B = -14.3$  V.

## 2.9 Summary

In this chapter, a new body-biased MEM relay design is introduced to reduce the number of contact dimples and thereby reduce the switching hysteresis voltage ( $V_H$ ) to enable lower

voltage operation. A self-assembled monolayer coating of PFOTES is effective for further reducing  $V_H$ , albeit with a tradeoff of degraded subthreshold swing. Together, these improvements enabled the first relay-based digital ICs to operate reliably with a supply voltage of 50 mV at room temperature.

A variety of MEM-relay based circuits are demonstrated to operate with a supply voltage of 50 mV at room temperature, including an inverter, OR, XOR, AND and 2:1 MUX. MEM-relay circuits also are demonstrated to have greater versatility due to dynamic re-configurability and the possibility of passing multiple signals simultaneously. Body-biasing is demonstrated to be effective for reducing the operating voltage ( $V_{DD}$ ) of a multiple-gate MEM relay and for adjusting its functionality.  $V_{DD}$  scaling is limited by the relay switching hysteresis voltage, which increases with the number of gate electrodes for a fixed total gate area. These experimental findings indicate that scaled electromechanical switches are promising for ultra-low-power digital computing.

## Chapter 3

# Practical Challenges and Opportunities for MEM Relay Circuits

In order to practically achieve large-scale MEM relay integrated circuits, a number of challenges remain to be overcome. Tungsten originally was chosen as the contact electrode material because it is CMOS-process compatible, and a relatively hard material with good mechanical wear properties [26]. However, exposed tungsten surfaces are susceptible to oxidation, increasing the on-state resistance,  $R_{ON}$ , over the operating lifetime of a relay [27]. The rate of oxidation is affected by operating conditions such as the contact force and the operating frequency [28–30]. Alternative contact metals have been explored, for example ruthenium, but they have their own set of process integration challenges [31]. Methods to ‘break down’ the native oxide on tungsten electrode surfaces have been used in order to achieve functional relay integrated circuits, as a sufficiently large applied electric field across the oxide (between contacting electrodes) can cause it to become electrically conductive [32]. The current understanding is that the breakdown process creates defects in the oxide, forming a pathway through the oxide for electronic charges to percolate through [33, 34].

Contact electrode material property requirements are different for ultra-low-voltage relay operation than for high-voltage relay operation, because native oxide cannot easily be broken down and the contact impact velocity is lower for ultra-low-voltage operation. More suitable contact materials (that would not oxidize in air) or packaging methods that can prevent contact oxidation and  $R_{ON}$  degradation are needed to enable large-scale MEM relay circuits operating at ultra-low voltage.

This chapter addresses some of the aforementioned remaining challenges for achieving reliable MEM relay integrated circuit operation. First the method of contact oxide breakdown is re-examined. The hot-switching breakdown approach is compared with a new cold-

switching approach to elucidate the mechanism of contact failure, and a new method of oxide breakdown using short voltage pulses is proposed to reliably break down native oxide at the contact. Then the issue of  $R_{ON}$  degradation in ambient conditions is addressed by investigating the use of liquid dielectric media.

Since MEM relays exhibit ideal characteristics (zero OFF-state leakage and abrupt switching behavior) under a wide range of operating conditions (in contrast to CMOS transistors), they hold promise for operation in extreme environments. This is confirmed through the demonstration of MEM relay integrated circuits operating across a wide range of temperatures.

### 3.1 Relay Contact Oxide Breakdown

In prior work it was shown that the on-state resistance of a MEM relay can be improved by applying a sufficiently large voltage across the source/drain contacts and switching the relay into the ON state, causing the oxide to break and current to flow more easily, as shown in Fig. 3.1. It is known that mechanical strain increases oxide defect density and aids the breakdown process [35], so that physical impact upon electrode contact could play an important role in the relay contact oxide breakdown process. Note that before the oxide is broken down,  $R_{ON}$  is so high that there is initially no measurable increase in drain current when the relay is switched ON. Increasing the gate voltage well beyond the turn-ON voltage increases the mechanical force on the contacting region, causing some leakage current to flow between contacting surface asperities. Also, the hysteresis voltage seems to be significantly larger prior to oxide breakdown, likely due to larger  $F_{adh}$  for the contacting oxidized surfaces.

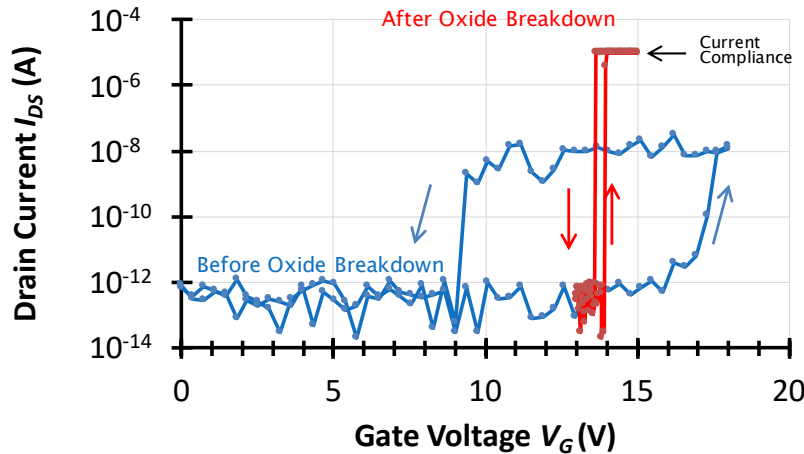


Figure 3.1: Measured  $I_{DS}$  vs.  $V_G$  characteristics of a 2C N-relay before and after oxide breakdown.  $V_B = 0$  V.

The contact oxide breakdown method described above tends to have varying  $R_{ON}$  results, sometimes causing contact welding (so that the relay is stuck ON), and sometimes not consistently breaking the oxide. To find a method that provides more consistent results, several different oxide breakdown procedures were tested and compared. If  $R_{ON}$  after the breakdown procedure was  $> 1k\Omega$ , the breakdown procedure was repeated and the lowest  $R_{ON}$  value was recorded.

## Hot Switching Oxide Breakdown

The conventional oxide breakdown procedure is known as ‘hot switching’ oxide breakdown; a voltage of  $3V$  is first applied across the drain-source  $V_{DS}$  before the relay is turned ON by applying a gate voltage  $V_G$ . Fig. 3.2 shows the circuit schematic and timing waveform for the hot switching oxide breakdown procedure. The gate voltage is increased to  $V_{ON} + 2V$  step-by-step; at each step the drain current is measured before proceeding to the next voltage step. A current compliance on  $I_{DS}$  is set so that the drain current does not exceed  $1\mu A$ . This process is conducted using a Keithley 4200A or Agilent B1500 Semiconductor Device Parameter Analyzer.

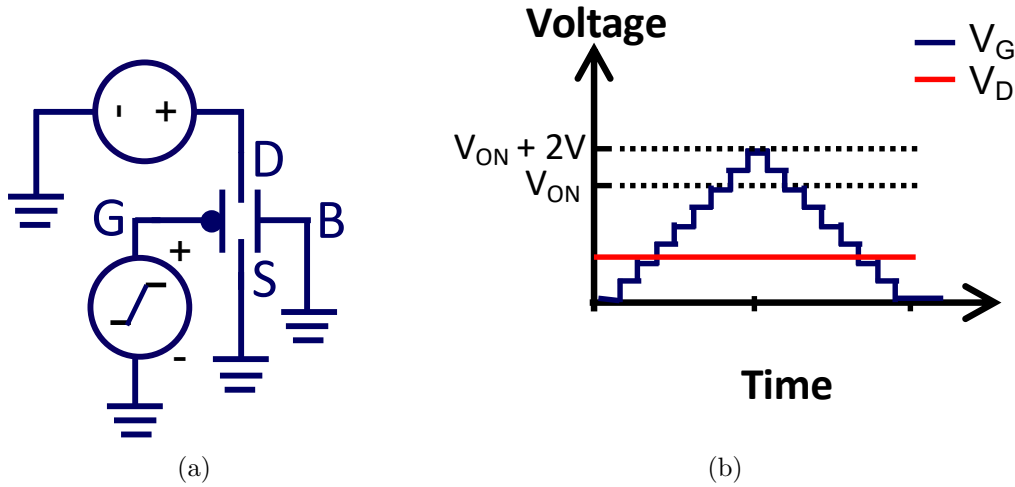


Figure 3.2: Hot switching oxide breakdown procedure (a) circuit schematic and (b) voltage timing waveform (not to scale).

This method is fairly effective in breaking down the oxide; however, sometimes it causes contact welding or damage due to the applied voltage across the contact, and  $R_{ON}$  afterwards is not consistently low (see Fig. 3.3). Also, it is difficult to precisely implement this procedure because the time duration of source/drain contact is not well-defined.

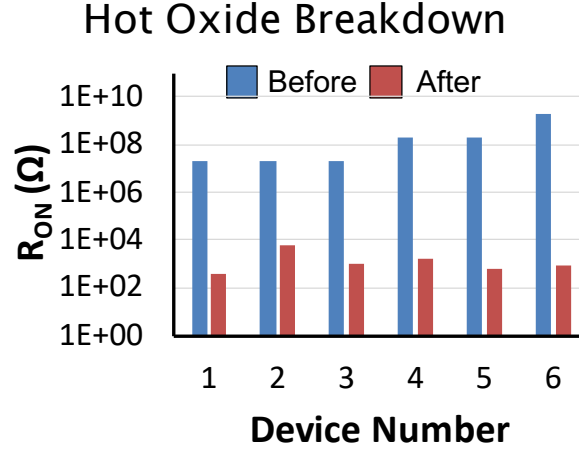


Figure 3.3: Hot switching oxide breakdown procedure results. Average  $R_{ON}$  before oxide break is  $410 \pm 784 \text{ M}\Omega$ . Average  $R_{ON}$  after oxide break is  $1.7 \pm 2.1 \text{ k}\Omega$ .

### Cold Switching Oxide Breakdown

An alternative ‘cold switching’ oxide breakdown procedure was studied to compare with the hot switching oxide breakdown procedure. Here, ‘cold’ refers to the fact that there is no voltage difference between the source and drain prior to contact. The relay is switched ON by applying  $V_{GS} = V_{ON} + 2\text{V}$ . Then a millisecond voltage pulse  $V_{DS}$  is applied across the contact using the Agilent B1500A Semiconductor Device Parameter Analyzer. Tunable oxide breakdown process parameters include the magnitude (*e.g.*, 3 V) and duration (*e.g.*, 5 ms) of the voltage pulse.  $R_{ON}$  is measured afterward, and if the oxide is not successfully broken, then an additional voltage pulse  $V_{DS}$  is applied.

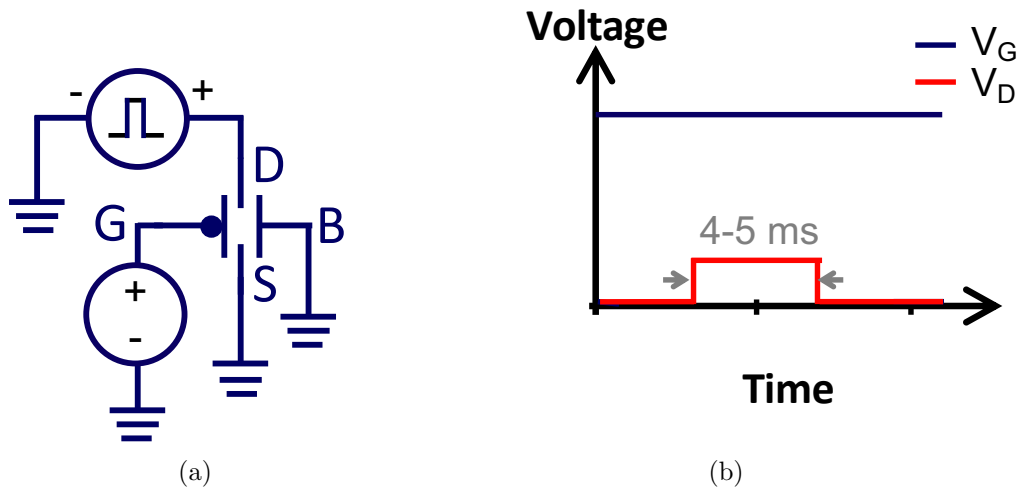


Figure 3.4: Cold switching oxide breakdown procedure (a) circuit schematic and (b) voltage timing waveform (not to scale).

Results for the cold switching oxide breakdown procedure are shown in Fig. 3.5. This method was also found to have some issues with contact welding, suggesting that the issue with the hot switching procedure is not metal-metal arcing during switching ON and OFF, but rather due to Joule heating. The welding in the cold switching case may be due to the fact that the voltage pulses were too long in duration, or that there is no current compliance limit. However, shorter pulse duration was found to be less effective in breaking down the oxide. This suggests that the cold switching oxide breakdown procedure alone is not sufficient for effective oxide breakdown: some other means of preventing Joule heating is required.

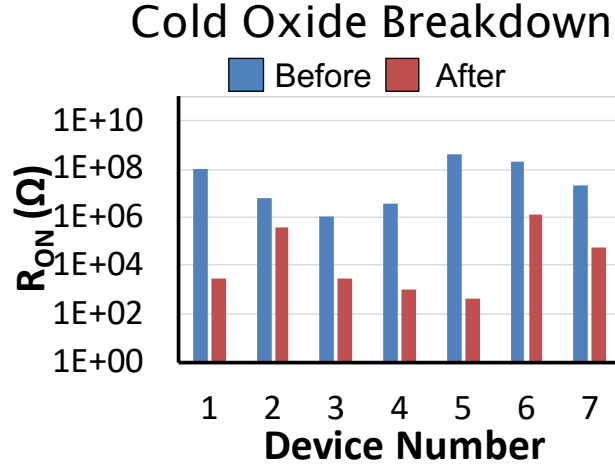


Figure 3.5: Cold switching oxide breakdown procedure results. Average  $R_{ON}$  before oxide breakdown is  $90.2 \pm 154 M\Omega$ . Average  $R_{ON}$  after oxide breakdown is  $250 \pm 494 k\Omega$ .

### Pulsed Cold Switching Oxide Breakdown

The final oxide breakdown procedure studied in this work uses multiple short  $V_{DS}$  pulses, approximately  $10 \mu s$  in duration, applied using the pulse measurement unit (PMU) of the Agilent B1500A Semiconductor Device Parameter Analyzer. A gate voltage of  $V_{GS} = V_{ON} + 2V$  is initially applied to turn ON the relay. Then, a voltage pulse train comprising 3 pulses is applied across the drain-source contact, each  $10 \mu s$  in duration, with a  $300 \mu s$  delay between each pulse. The voltage magnitude is initially set to  $V_{DS} = 6V$ . If found to be ineffective, the procedure is then repeated but with a higher voltage  $V_{DS} = 8V$ . We hypothesize that a shorter pulse duration is effective for reducing Joule heating and metal material transfer, thus allowing for a more consistent oxide breakdown. The results in Fig. 3.7 show that short-pulse oxide breakdown can consistently achieve sub- $1k\Omega$  resistance with reduced  $R_{ON}$  variation.

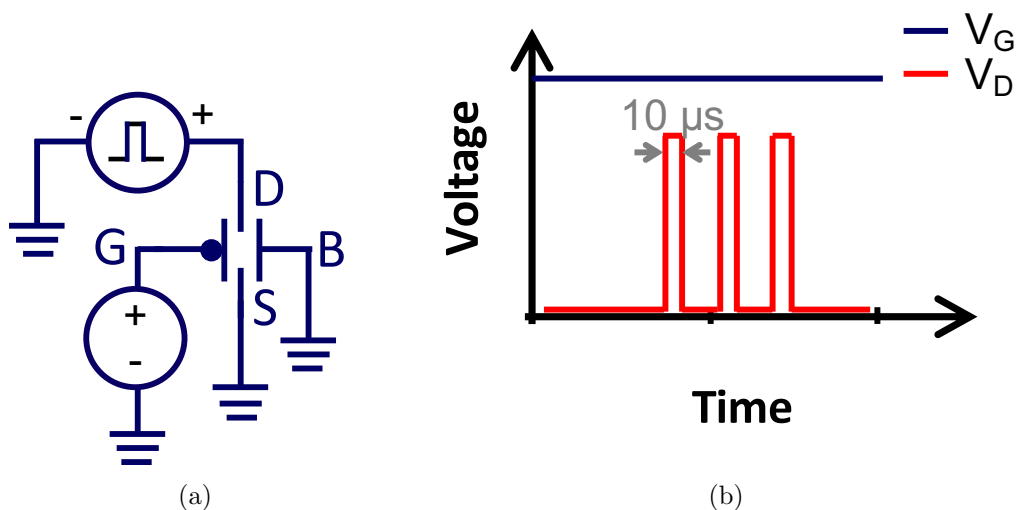


Figure 3.6: Pulsed cold switching oxide breakdown (a) circuit schematic and (b) voltage timing waveform (not to scale).

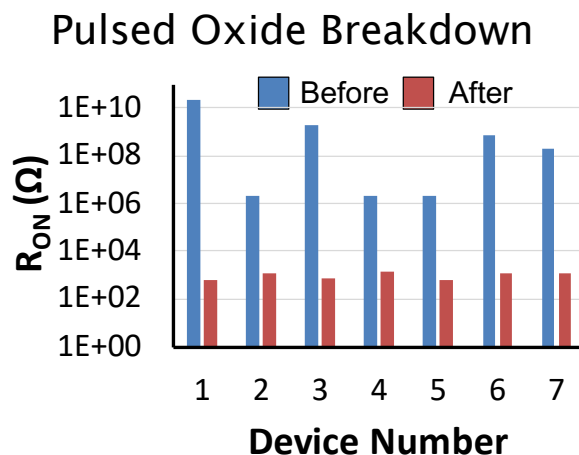


Figure 3.7: Multiple drain-pulse oxide breakdown. Before oxide breakdown, average  $R_{ON} = 3.3 \pm 7.41\ \text{G}\Omega$ . After breakdown, average  $R_{ON} = 0.95 \pm 0.30\ \text{k}\Omega$ .

To summarize this section, a study of contact oxide breakdown procedures was conducted to elucidate the primary failure mechanism after oxide breakdown. Contact Joule heating is identified as most likely, rather than metal-metal contact arcing. A new cold-switching

oxide breakdown procedure using 10  $\mu s$  voltage pulses provides for reliable oxide breakdown without causing contact welding or damage via Joule heating.

## 3.2 Study of Relay Operation under Ambient Conditions

MEM relays must operate reliably in order for relay-based integrated circuits to find practical application. On-state resistance ( $R_{ON}$ ) increase due to contact oxidation has been identified as the main failure mode for proper MEM relay operation, and has been studied extensively in the past [28]. For millivolt operation target of relay integrated circuits, this issue is exacerbated because ultra-low drain-to-source voltage and reduced contact velocity are less effective to break down the native oxide [27]. The relay integrated circuits that have been demonstrated to operate with millivolt supply voltage all were tested in a vacuum chamber in order to slow contact oxidation and thereby maintain low  $R_{ON}$ . The vacuum probe station accommodates only a very limited number of probe tips, however, which precludes testing of large-scale integrated relay circuits. Therefore, a means to achieve reliable relay operation under room ambient conditions is desirable.

Herein we assess the impact of millivolt switching operation (enabled by body biasing) and PFOTES self-assembled monolayer coating on the evolution of on-state resistance under room ambient conditions. Then the use of dielectric liquid media to mitigate the issue of contact oxidation is investigated.

### $R_{ON}$ Degradation under Room Ambient Conditions

2C MEM relays were initially subjected to an oxide breakdown procedure such that the initial  $R_{ON}$  was below 1 k $\Omega$ . The relay test setup shown in Fig. 3.8 was then used to monitor  $R_{ON}$  over many ON/OFF switching cycles. Note that the device is configured as an N-relay pull-down device in an inverter circuit; a voltage pulse train is applied to the gate electrode.

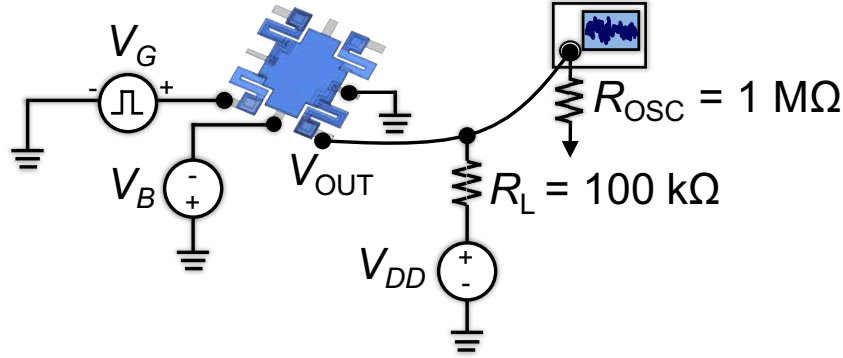
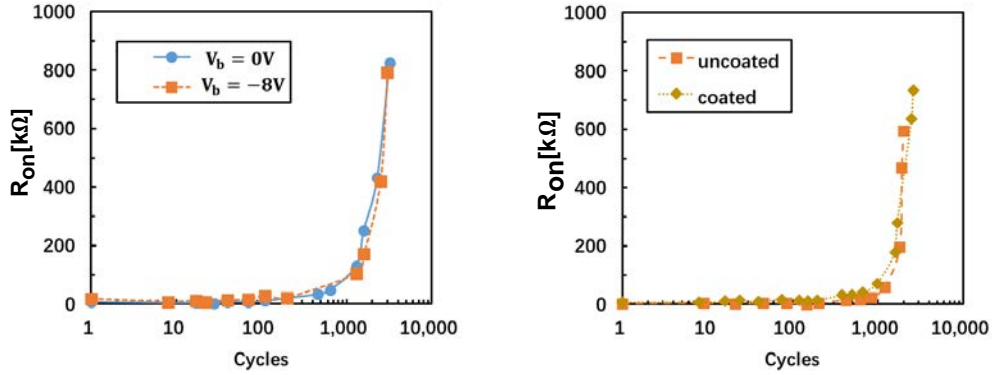


Figure 3.8: Schematic illustrating the test setup used to monitor  $R_{ON}$  for a MEM relay operating under room ambient conditions.

Testing of the 2C MEM relays was conducted under room ambient conditions of  $\sim 60\%$  relative humidity, 1 atm pressure, and  $T \sim 300$  K. The switching frequency was 1 kHz, with peak  $|V_{GB}| = 17$  V. As can be seen from Fig. 3.9,  $R_{ON}$  increases rapidly after approximately 1000 switching cycles with  $V_{DD} = 0.5V$  under room ambient conditions. This is in contrast to previously published results in [27] which show stable  $R_{ON}$  over  $10^6$  switching cycles with  $V_{DD} = 4V$  under  $10 \mu\text{Torr}$  pressure. Body biasing (enabling lower gate voltage swing) does not significantly affect the evolution of  $R_{ON}$ .

The effect of a PFOTES self-assembled monolayer (SAM) coating on contact oxidation can be ascertained from Fig. 3.9b. (We were curious to ascertain whether the SAM can prevent oxygen diffusion and reduce the rate of oxidation of the contacts.) It can be seen that the SAM does not help to mitigate contact oxidation, since  $R_{ON}$  degrades just as quickly (or even slightly more quickly). Therefore, oxygen easily permeates the SAM layer.



(a)  $R_{ON}$  degradation for uncoated MEM relays without vs. with body biasing to lower the gate voltage swing (b)  $R_{ON}$  degradation for body-biased MEM relays uncoated vs. SAM-coated ( $V_B = -8V$ )

Figure 3.9:  $R_{ON}$  degradation under room ambient operating conditions, with  $V_{DD} = 0.5V$ .

To conclude, body-biasing and SAM coating do not have significant impact on  $R_{ON}$  stability for MEM relays operating under room ambient conditions. Based on a comparison with prior published works [27, 28, 36], the drain-source voltage and ambient environment are two major factors contributing to  $R_{ON}$  degradation. (Low drain-source voltage is less effective for continually breaking down the native oxide during relay operation, while higher oxygen content in the ambient environment increases the rate of contact oxidation.)

## Alternative dielectric media

To prevent contact oxidation in relays operating under room ambient conditions, the use of an alternative dielectric media has been proposed [37–39]. Oil as a liquid dielectric, with relative permittivity greater than 1, provides for lower  $V_{ON}$  as well as improved device reliability (albeit at the tradeoff of longer turn-ON delay).

Fig. 3.10 shows the effects of immersing a 2C MEM relay in rotary pump fluid oil (PELCO Ultra Grade 19 Rotary Pump Oil) with a dielectric constant of  $\epsilon_r = 1.5$ . The drain current vs. gate voltage characteristics were measured under room ambient conditions.

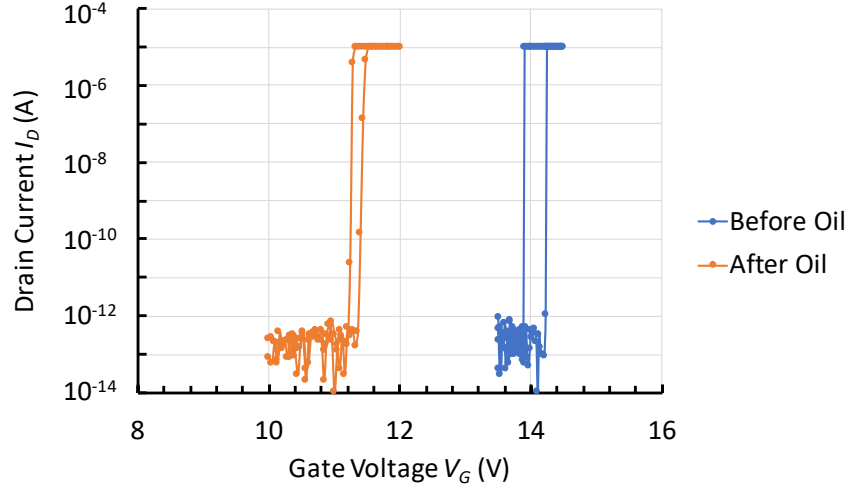


Figure 3.10:  $I_D - V_G$  characteristics of a 2C MEM relay before and after submersion in oil. (The current is artificially limited to  $10 \mu\text{A}$  to prevent excessive Joule heating during the DC measurement.)

Because oil has larger permittivity than air/vacuum, enhancing the electrostatic force induced by an applied voltage across the gate and body, the turn-ON voltage is reduced upon immersion in oil. The hysteresis voltage is reduced from 300 mV to 200 mV, beyond the  $1/\sqrt{\epsilon_0}$  dependence expected due to the change in dielectric constant alone, which suggests that contact adhesive force is reduced and/or the oil induces force to help separate the contacting electrodes. An initial study of  $R_{ON}$  stability for an oil-immersed relay operating under room ambient conditions shows promise for this approach to mitigating contact oxidation. Fig. 3.11 compares  $I_D - V_G$  characteristics for 50 consecutive gate-voltage sweeping cycles, measured using an Agilent B1500 Semiconductor Device Parameter Analyzer under room ambient conditions, for relays with air vs. oil dielectric media. The ON-state current is limited by the current compliance limit. After many cycles (indicated by the color changing from blue to red in Fig. 3.11),  $R_{ON}$  degrades for the relay with air as the dielectric, so that its ON-state current eventually does not reach the current compliance limit. In contrast, the relay with oil as the dielectric operates without noticeable degradation in  $R_{ON}$ .

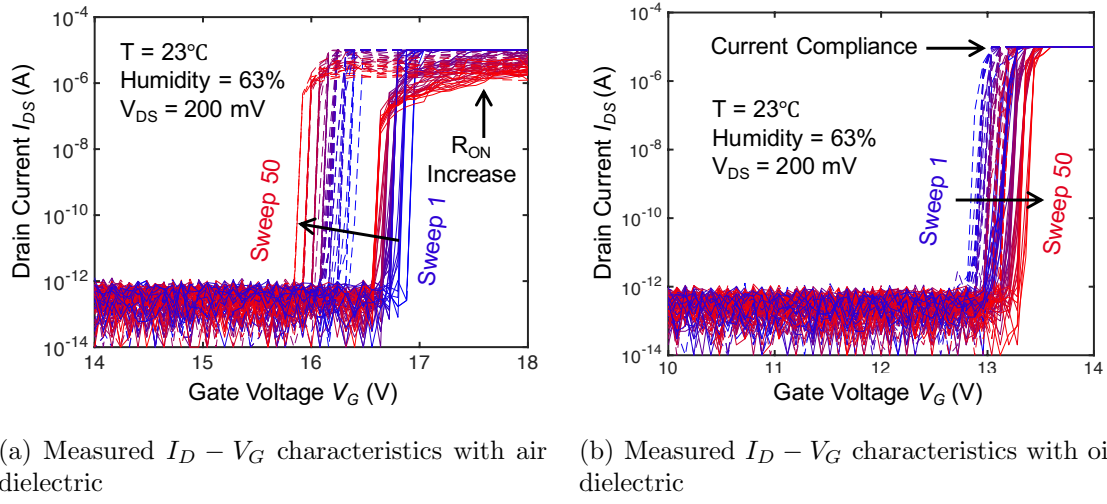


Figure 3.11: Measured  $I_D - V_G$  characteristics of a 2C MEM relay over 50 gate voltage sweeping cycles (a) with ambient air dielectric and (b) oil dielectric.  $V_{DS} = 200$  mV,  $T = 300$  K and relative humidity = 63%. The ON-state current was limited to  $10 \mu\text{A}$  to prevent excessive Joule heating.

Fig. 3.12 shows the evolution of turn-ON and turn-OFF voltages of the 2C MEM relays over 50  $I_{DS} - V_G$  sweeps, for air vs. oil dielectric media.  $V_{ON}$  and  $V_{OFF}$  tend to decrease over the operating lifetime of the relay in air, possibly due to degradation of the polycrystalline silicon-germanium structural material in oxidizing ambient (which affects the structural stiffness). In contrast,  $V_{ON}$  and  $V_{OFF}$  increase slightly over the operating lifetime of the relay immersed in oil, possibly due to heating of the oil affecting its dielectric permittivity.

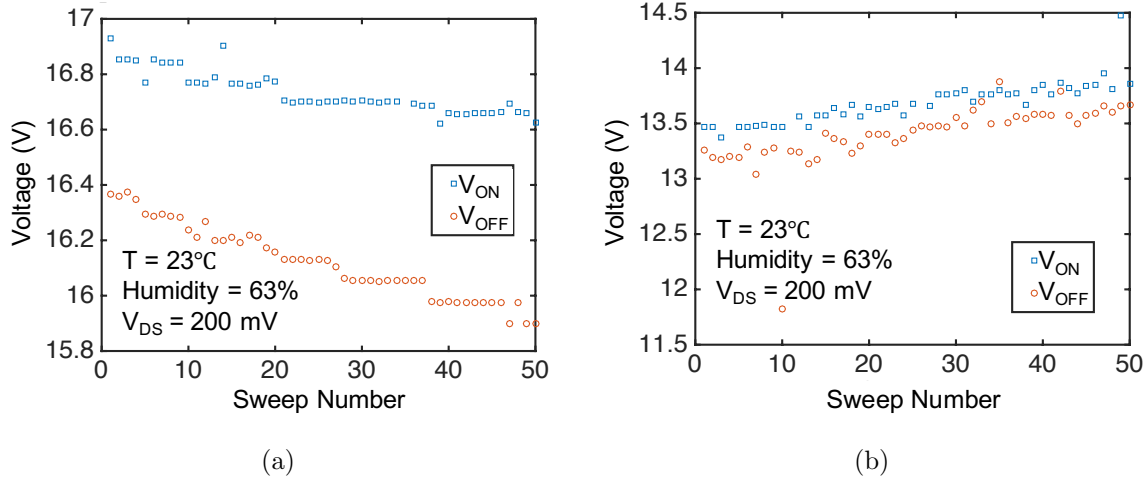


Figure 3.12: Evolution of relay switching voltages for (a) relay in room ambient and (b) relay immersed in oil with  $V_B = 0\text{V}$  and  $V_{DS} = 0.2\text{V}$ . The current compliance limit was set to  $10 \mu\text{A}$ .

To conclude, the use of alternative dielectric media is promising for achieving millivolt relay integrated circuits operating under room ambient conditions. Further exploration is needed to determine the best media to use. An ideal dielectric medium has a large permittivity (to minimize  $V_{ON}$ ) that is stable over a large temperature range. In addition, other properties of dielectric media such as viscosity (which affects relay mechanical switching delay) should be considered.

### 3.3 Operation in Extreme Environments

For electronics in extreme environments (for example, in outer space), packaged devices and circuits must be able to operate reliably over a wide range of temperatures and also be able to withstand irradiation. MEM relays have inherent resilience to extreme environments and can operate across a wide temperature range [36, 40]. This is particularly advantage for edge devices (in the Internet of Things) that must operate reliably across a wider range of environmental conditions than cloud devices (in data centers).

#### Temperature Dependence of Relay Performance Characteristics

Large changes in temperature primarily induce significant structural expansion or contraction and also can affect the Young's modulus (hence stiffness) and thin-film strain gradient (hence out-of-plane deflection) of the movable structure; they also can affect contact adhesive force. Prior work showed that at cryogenic temperatures (below 90 K),  $R_{ON}$  stability is greatly

improved due to the lack of oxygen gas [36]. Figure 3.13 compares measured  $I_D - V_G$  characteristics for MEM relays operated at 300 K and 70 K. The hysteresis voltage can be seen to be significantly smaller at cryogenic temperature. Therefore, low-temperature operation of MEM relays seems especially promising.

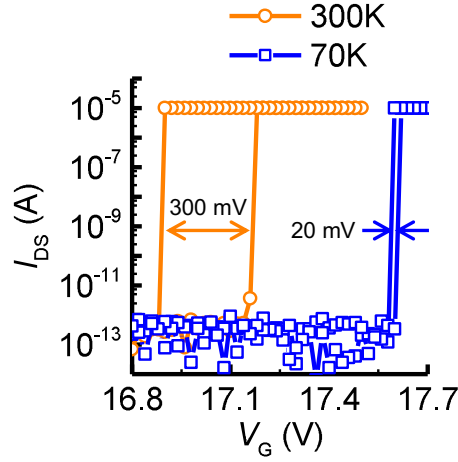


Figure 3.13: Measured  $I_D - V_G$  characteristics of a MEM relay operated at room temperature (300K) vs. at low temperature (70K).

The hysteresis voltage ( $V_H$ ) sets a lower limit for the switching gate voltage swing ( $V_{DD}$ ) of body-biased MEM relays. A comparison of  $V_H$  measured at different temperatures in Fig. 3.14 shows that  $V_H$  is lower at extreme temperatures (77 K and 400 K) than at room temperature.

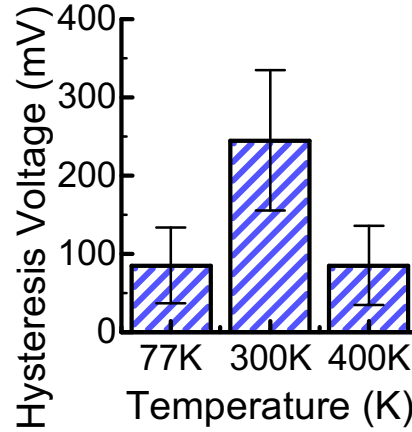


Figure 3.14: Switching hysteresis voltage for MEM relays measured at different temperatures under  $10 \mu\text{Torr}$  pressure. The error bars indicate  $\pm 1$  standard deviation, measured across five relays.

A possible explanation for these observed results is that the presence of water molecules adsorbed on the surface the tungsten electrodes increases capillary forces. Capillary forces are strongest when water is in the liquid phase, which suggest a high adhesion force at 300 K. When operating at temperatures below 273.15 K ( $0^\circ\text{C}$ ) or above 373.15 K ( $100^\circ\text{C}$ ), capillary forces are expected to decrease due to freezing or evaporation of water droplets [41]. Other contributing forces to total adhesion force include van der Waals forces and electrostatic force, which do not vary significantly with temperature [42].

Another possible explanation is the effect of temperature on tungsten oxidation. At high temperature, the thickness of the native oxide is likely slightly thicker due to increased oxygen diffusivity. While tungsten is a moderately hydrophilic material (contact angle  $\sim 63^\circ$  [43]), tungsten oxide can be either hydrophobic or hydrophilic, depending on the material structure [44]. Since a hydrophobic surface would also reduce capillary forces, the difference in surface wettability of tungsten oxide compared to tungsten plays a role in adhesion force. If capillary forces indeed play the largest role in relay contact adhesion force, a bake-out procedure (conducted by subjecting the measurement chamber to high temperature and high vacuum conditions for an extended period of time) prior to measurement can help to remove water from the contacting surfaces. Another option is to develop a thin coating with desirable hydrophobic surface properties that can reduce capillary forces and prevent formation of native tungsten oxide by acting as a diffusion-blocking layer [45].

In any case, the non-monotonic behavior of contact adhesive force (hence  $V_H$ ) indicates that relay integrated circuits that function with low gate voltage swing at room temperature also can be expected to function with low gate voltage swing at extreme temperatures. Fig.

3.15 shows turn-ON voltage ( $V_{ON}$ ) values for a MEM relay measured across a wide range of operating temperatures. The folded-flexure suspension beam design provides for relatively stable native  $V_{ON}$  (less than 10 percent variation over a 250 K range).

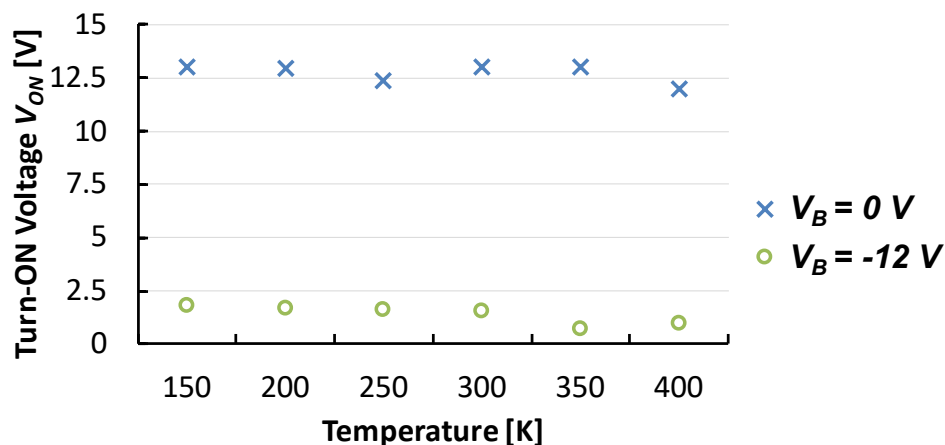


Figure 3.15: Measured turn-ON voltage of a MEM relay for temperatures ranging from 150 K to 400 K, with and without body bias voltage. Pressure = 10  $\mu$ Torr.

## Relay IC Operation Across a Wide Temperature Range

Because the hysteresis voltage is lower, relay integrated circuits can be operated with lower gate voltage swing at extreme temperatures than at room temperature, as shown in the figures below. Although contact oxidation does not occur at temperatures below 90 K, relay contacts may still be oxidized during the process of cooling to low temperature; thus it is still possible to have high  $R_{ON}$  for cryogenic operation of relay ICs. Also, at  $T = 400$  K, the contacting electrodes tend to oxidize quickly, resulting in high-on-state resistance. The high  $R_{ON}$  limits the output voltage swing due to the non-infinite internal impedance of the oscilloscope, as explained in the previous chapter.

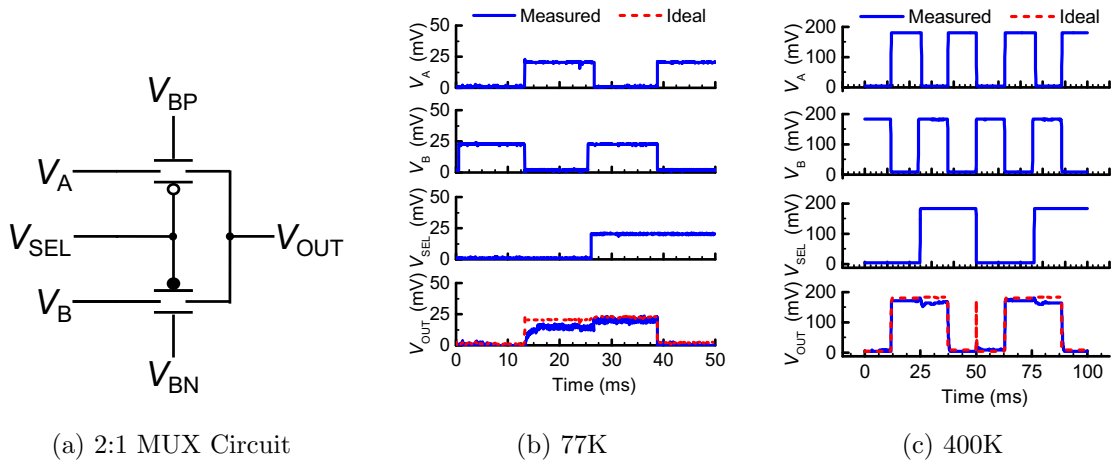


Figure 3.16: 2:1 MUX (a) circuit schematic (b) measured voltage waveforms (timing diagrams) demonstrating 25 mV operation at 77 K and (c) 200 mV operation at 400 K.

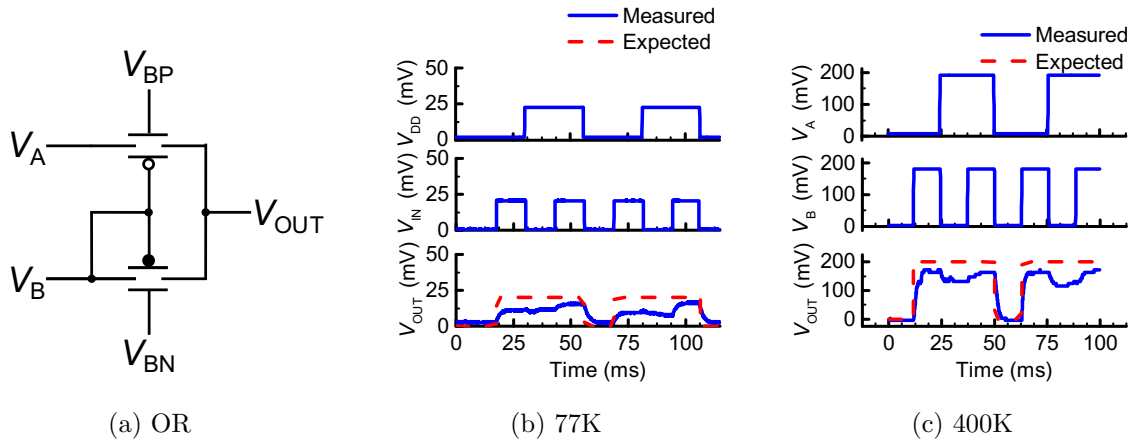


Figure 3.17: 2-input OR gate (a) circuit schematic (b) measured timing diagrams demonstrating 25 mV operation at 77 K and (c) 200 mV operation at 400 K.

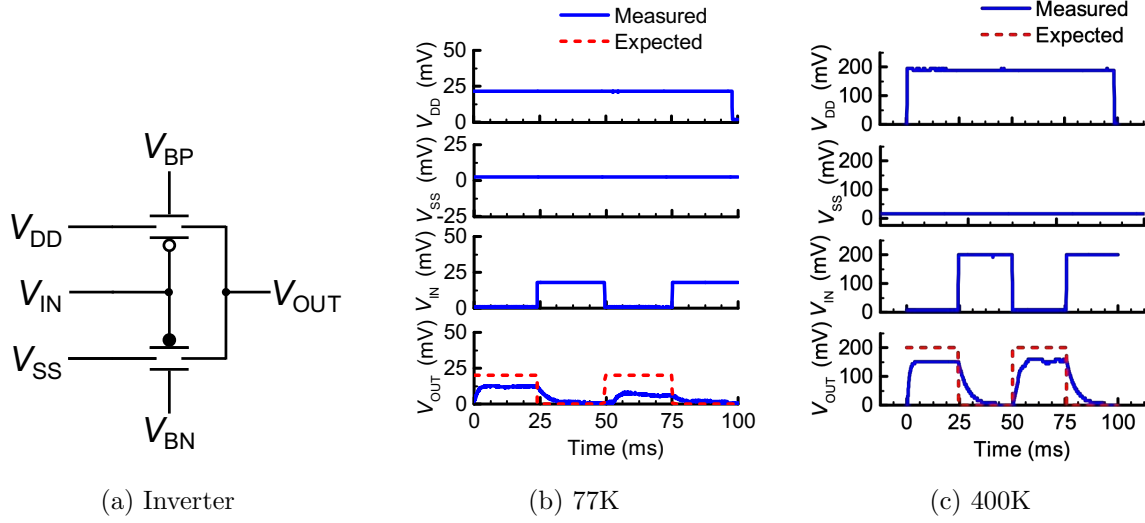


Figure 3.18: Inverter (a) circuit schematic (b) measured timing diagrams demonstrating 25 mV operation at 77 K and (c) 200 mV operation at 400 K.

## Summary

The ability to test relay circuits under room ambient conditions is desirable to demonstrate very large scale integrated circuit functionality. Contact oxidation resulting in high ON-state resistance is the limiting factor for achieving reliable MEM relay circuit operation. In this chapter, a contact oxide breakdown procedure using short voltage pulses was developed to consistently achieve  $< 1 \text{ k}\Omega$  ON-state resistance with low variability. The evolution of ON-state resistance under room ambient operating conditions was investigated for low-voltage ( $V_{DD} = 0.5 \text{ V}$ ) operation. Alternative dielectric materials are suggested to improve ON-state resistance stability in room ambient environment. Finally, MEM relays are shown to be capable of operating reliably over a wide range of temperatures from 70K to 400K. Various relay integrated circuits (2:1 MUX, OR, and Inverter) are demonstrated at 77K and 400K with  $V_{DD}$  as low as 25 mV, showing promise for extreme environment applications.

# Chapter 4

## Compensated Stiffness Relay Design

### 4.1 Introduction

For a conventional MEM relay, there are various design trade-offs in optimizing the structural stiffness. A reduction in the effective spring constant ( $k$ ) results in lower actuation voltage hence lower dynamic energy consumption, but also increases the likelihood of stuck-ON failure. Body biasing can be used to lower the switching energy by pre-actuating the relay so that the gate voltage swing required to switch the relay is reduced, allowing for higher  $k$  to reduce the likelihood of stuck-ON failure while simultaneously improving the energy-delay tradeoff. The magnitude of the body-bias voltage required ( $> 500$  mV for an aggressively scaled relay) still can be a practical challenge for  $V_{DD}$  scaling, however [18, 22].

In this chapter, a novel method is proposed to improve the trade-off between low MEM relay switching energy and high spring restoring force. Specifically, structural elements with negative stiffness are incorporated to reduce the switching energy and thereby improve the energy-delay trade-off. The concept of fixed-fixed buckling beams operating with negative stiffness is first introduced in Section 4.2. Then, in Section 4.3, a compensated stiffness relay design is proposed and analyzed for both pull-in (PI) mode and non-pull-in (NPI) modes of operation. Section 4.4 discusses design optimization strategies to minimize  $V_{DD}$  for a scaled compensated stiffness relay. Section 4.5 discusses the impact of process induced variations on switching voltage for the compensated stiffness relay design and methods to improve tolerance to such variations. Section 4.6 concludes this chapter with a summary.

### 4.2 Compensated Stiffness Beam Design

Negative stiffness in a MEM relay is analogous to negative capacitance in a field-effect transistor to reduce the gate voltage swing required for switching [46]. Although negative capacitance also has been proposed to reduce the switching voltage of MEM relays [47–50],

negative stiffness provides an additional opportunity to reduce the switching voltage of a MEM relay without the use of ferroelectric materials.

Compressive stress in a fixed-fixed beam can cause the beam to buckle due to an axial load, as shown in Fig. 4.1a. According to Euler buckling theory, this point occurs if:

$$F_{axial} \leq -\frac{\pi^2 EI}{(KL)^2} \quad (4.1)$$

where  $E$  is the Young's Modulus of Elasticity,  $I = WH^3/12$  is the second moment of area of the cross-section of the beam (in this case a rectangle), and  $W$ ,  $H$ , and  $L$  are the width, thickness, and length of the beam, respectively.  $K$  is the column effective length factor, and  $K = 0.5$  for a fixed-fixed beam.

Axial force can be applied by designing a beam to be under compressive stress

$$F_{axial} = \sigma_0 WH \quad (4.2)$$

where  $\sigma_0$  is the value of axial stress (a negative value indicates compressive stress while a positive value indicates tensile stress). Note that  $WH$  is the cross-sectional area of the beam.

If a point load is applied in the center of the fixed-fixed beam in the  $x$ -direction, as shown in Fig. 4.1a, the spring restoring force of a fixed-fixed beam is modeled using the following equation [51]:

$$F_{NS}(x) = \underbrace{\left(\frac{\pi^2 \sigma_0 WH}{2L} + \frac{\pi^4 EWH^3}{6L^3}\right)}_{k_{NS-LIN}} x + \underbrace{\frac{\pi^4 EWH}{8L^3}}_{\kappa_{NS-CUB}} x^3 \quad (4.3)$$

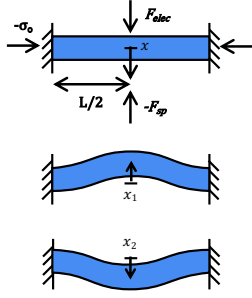
where  $x$  is the displacement of the beam. Under compressive stress, if  $|\frac{\pi^2 \sigma_0 WH}{2L}| > |\frac{\pi^4 EWH^3}{6L^3}|$ , then  $k_{NS-LIN}$  is negative and the beam will buckle.

The spring stiffness  $k_{NS}$  is defined as the slope  $dF_{NS}/dx$ . The relay region of operation corresponding to a negative slope is considered the negative stiffness region.

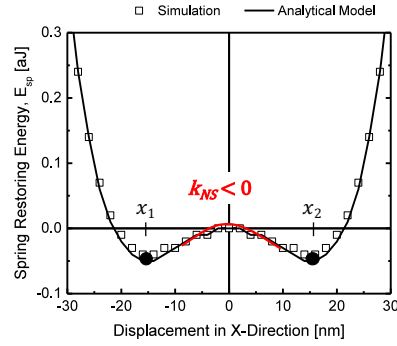
$$k_{NS} = \frac{dF_{NS}(x)}{dx} = \underbrace{\left(\frac{\pi^2 \sigma_0 WH}{2L} + \frac{\pi^4 EWH^3}{6L^3}\right)}_{k_{NS-LIN}} + 3 \underbrace{\frac{\pi^4 EWH}{8L^3}}_{\kappa_{NS-CUB}} x^2 \quad (4.4)$$

Buckled fixed-fixed beams have a bistable energy landscape, in which the beam reaches its lowest-energy state in one of two positions, as shown in Fig. 4.1a-b. By taking the first

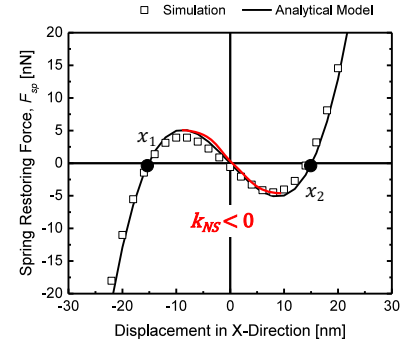
derivative of the energy vs. displacement curve, one can find the spring restoring force of the beam  $F_{sp} = dE_{sp}/dx$  (where  $E_{sp}$  is the stored spring energy), as shown in Fig. 4.1c. Negative stiffness (NS) is indicated by a negative slope of the  $F_{sp}$  vs.  $x$  plot. If sufficient force is applied to overcome the spring restoring force in one stable state, then the beam position can switch to the other stable state.



(a) Sufficient compressive stress causes buckling in a fixed-fixed beam, which has 2 stable states.



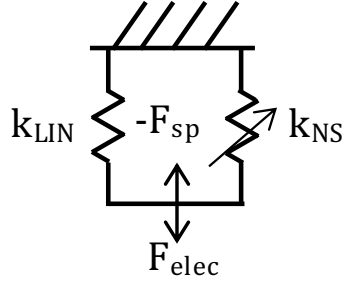
(b) Energy vs. displacement of fixed-fixed buckled beam.



(c) Force vs. displacement of fixed-fixed buckled beam.

Figure 4.1: Behavior of a fixed-fixed buckled beam

When two springs are connected in parallel, the effective stiffness is the sum of the stiffnesses of the individual springs. We propose to combine conventional positive stiffness beams in parallel with a NS beam, resulting in an overall ‘compensated’ spring structure with nonlinear effective stiffness ( $k_{eff}$ ), as illustrated in Fig. 4.2.



$$F_{sp} = (k_{LIN} + k_{NS-LIN})x + \kappa_{NS-CUB}x^3$$

$$k_{eff} = k_{LIN} + k_{NS-LIN} + \underbrace{3\kappa_{NS-CUB}x^2}_{k_{NS-CUB}}$$

Figure 4.2: Model of a compensated spring structure

For a **fully compensated** spring system, the magnitude of the positive stiffness (linear) term is equal to the magnitude of the NS linear term, *i.e.*,  $k_{LIN} = -k_{NS-LIN}$ , and the resulting spring restoring force  $F_{sp}$  has a cubic dependence on displacement. Effectively, the negative stiffness linear component is ‘compensated’ by the positive spring. Such a stabilized spring amplifies the effect of the applied actuation voltage on the displacement of the movable component of the MEM relay, thereby lowering the voltage needed to operate the switch. Note that even though conventional MEM relays already have abrupt switching characteristics (in contrast to CMOS transistors), negative stiffness beams are still advantageous for reducing relay switching energy and can improve the energy-delay design trade-off.

An initial proof-of-concept compensated spring design is shown in Figure 4.3a-c. A fixed-fixed buckled beam of linear stiffness  $k_{NS-LIN}$  (Fig. 4.3a) is combined with a folded flexure spring of stiffness  $k_{LIN} = -k_{NS-LIN}$ , which acts as a linear spring (Fig. 4.3b). The linear spring is designed as a folded flexure to help relieve residual stress and is based on [17]. The total effective spring restoring force is thus:

$$F_{sp} = \kappa_{NS-CUB} \cdot x^3 \quad (4.5)$$

In Figure 4.3, the initial double-well energy landscape of the NS beam is simulated using Coventorware, and it is shown that by compensating the structure with a linear spring, the overall energy landscape can be stabilized (flattened).

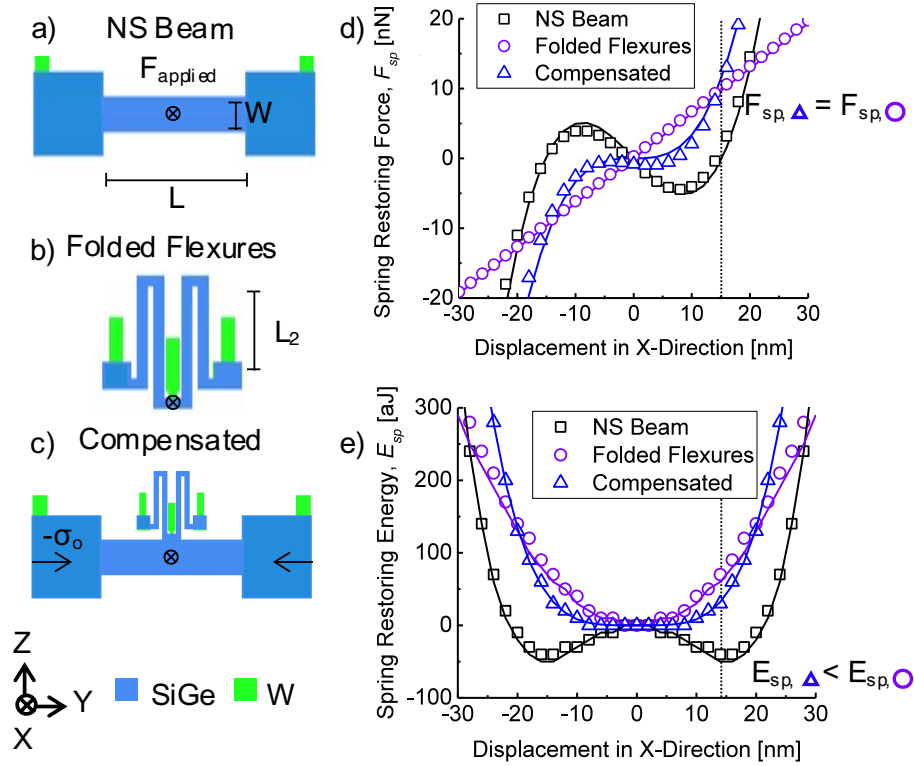


Figure 4.3: Coventorware simulations of (a) Fixed-fixed buckled beam, (b) Folded flexure linear spring, and (c) Compensated spring structure. (d) Spring restoring force of each effective spring and (e) Spring restoring energy of each effective spring.

## Buckled Beam Spring Coefficient

In this subsection, practical limitations on beam dimensions for a fixed-fixed buckled beam are discussed. Recall the stiffness terms of the fixed-fixed buckled beam from Eq. 4.3:

$$k_{NS-LIN} = \left( \frac{\pi^2 \sigma_0 W H}{2L} + \frac{\pi^4 E W H^3}{6L^3} \right) \quad (4.6)$$

and

$$\kappa_{NS-CUB} = \frac{\pi^4 E W H}{8L^3} \quad (4.7)$$

The design goals are 1) to develop NS beams that have linear spring coefficient  $k_{NS-LIN} < 0$ , and 2) to maximize the non-linear spring coefficient  $\kappa_{NS-CUB}$  in order to achieve high effective stiffness to overcome the adhesive force of the MEM relay contact. Fig. 4.4 shows

how the linear and cubic spring coefficients depend on various design parameters. The structural beam material is assumed to be polycrystalline  $\text{Si}_{0.4}\text{Ge}_{0.6}$ , with nominal beam thickness  $H = 30\text{nm}$ . Typical thin-film residual stress ranges from  $-100\text{ MPa}$  to  $-160\text{ MPa}$  [19].

There are several design criteria that limit the feasible range of  $k_{NS-LIN}$  and  $\kappa_{NS-CUB}$ . While increasing the magnitude of compressive residual stress can result in a high  $\kappa_{NS-CUB}$  and  $k_{NS-LIN}$ , devices with high residual stress exhibit undesirable out-of-plane deformation of the actuated electrode (plate) resulting in failure to actuate correctly. In Fig. 4.4, this high-residual-stress design region is marked as Region I. Regions II and V correspond to designs for which the  $k_{NS-LIN} < 0$  requirement is not satisfied. The remaining feasible design regions are marked as Regions III and IV. In short, while it is desirable to increase  $\kappa_{NS-CUB}$  to achieve large spring restoring force, increasing the cubic stiffness term too much may cause buckling failure or not result in negative stiffness.

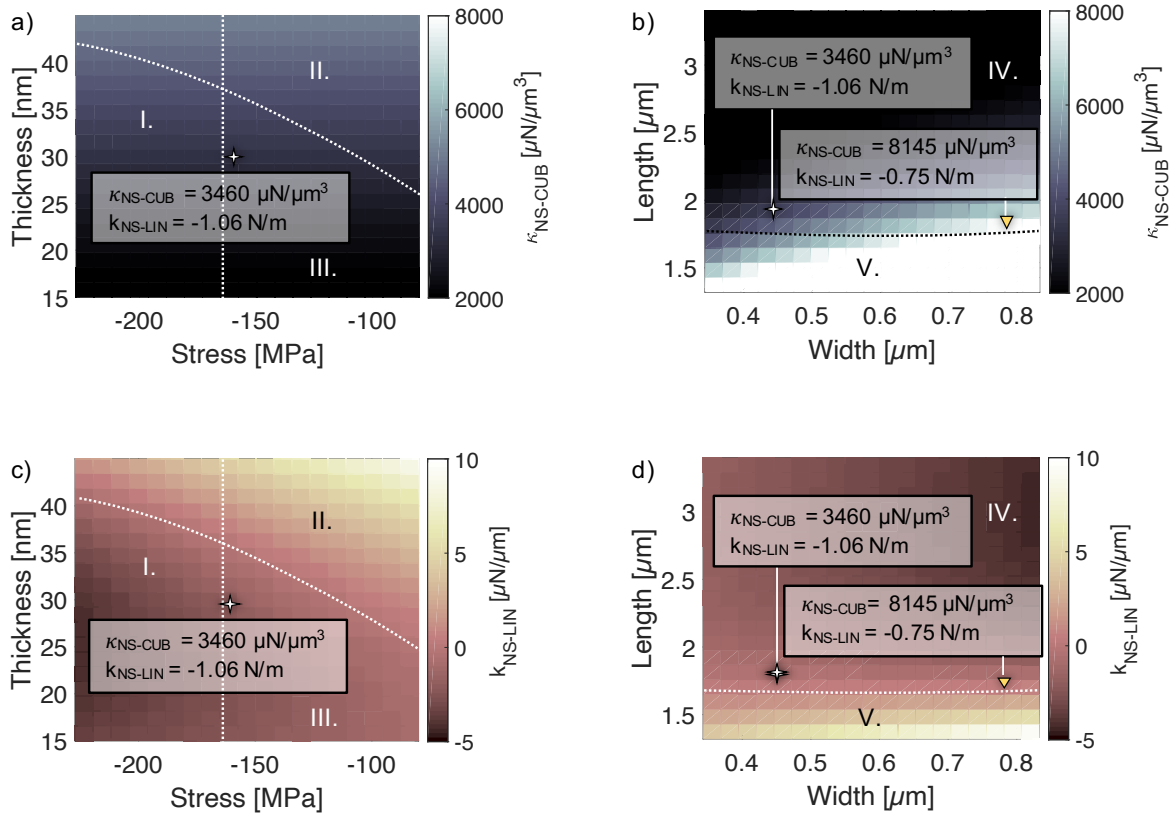


Figure 4.4: Parameters for tuning the linear and non-linear spring coefficients of the NS Beam. For Figs. (a) and (c), beam width  $W = 0.49 \mu\text{m}$  and beam length  $L = 2 \mu\text{m}$ . For Figs. (b) and (d), the stress  $\sigma_0 = -160\text{ MPa}$ , and Thickness  $H = 30\text{ nm}$ .

In order to meet design feasibility requirements, a realistic maximum value of  $\kappa_{NS-CUB} \sim 8000\mu\text{N}/\mu\text{m}^3$  is used in this work. If higher effective stiffness is required, multiple fixed-fixed buckled beams can be used.

### 4.3 Switching Energy and Voltage Analysis

In this section, equations for the switching voltages of fully compensated relays are derived. Similarly as for a conventional MEM relay described in Ch. 2.2, a compensated stiffness relay can be designed for pull-in mode or non-pull-in mode operation.

#### Pull-In Mode Compensated Stiffness Relay Analysis

To analyze the compensated stiffness relay operating in pull-in mode, first consider the following simplified model:

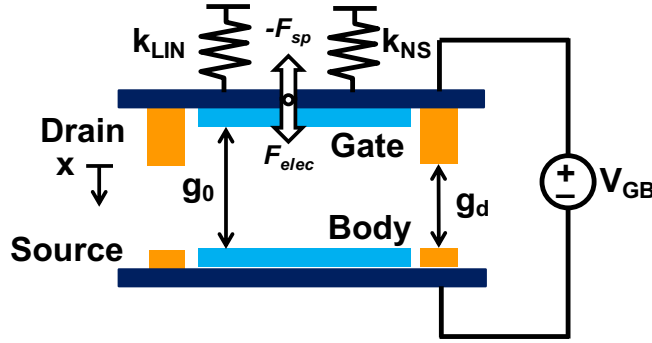


Figure 4.5: Simplified model of compensated stiffness relay.

To develop the analytical model for this device, we combine Eq. 2.2 and Eq. 4.5, repeated here for convenience:

$$F_{elec} = \frac{1}{2} C_{GB} V_{GB}^2 \quad (4.8)$$

$$F_{sp} = F_{LIN} + F_{NS} = \kappa_{NS-CUB} \cdot x^3 \quad (4.9)$$

By Newton's second law,  $\sum F = 0$ , so the quasi-static displacement can be derived:

$$\sum F = 0 = \frac{1}{2} \frac{\epsilon_0 A_{ACT}}{g_0 - x} V_{GB}^2 - \kappa_{NS-CUB} \cdot x^3 \quad (4.10)$$

The displacement at which pull-in instability occurs is found by solving for  $x_{PI-NS}$  such that  $dF/dx = 0$ . This yields  $x_{PI-NS} = 3/5 \cdot g_0$ . If the device is designed such that  $g_d > x_{PI-NS}$ , then the relay will turn on when the voltage applied across the gate and body causes the displacement to reach  $x_{PI-NS}$ .

Solving Eqn. 4.10 for  $V_{GB} = V_{ON-PI-NS}$ , the turn-on voltage is:

$$V_{ON-PI-NS} = \sqrt{\frac{216}{3125} \kappa_{NS-CUB} g_0^5 \epsilon_0 A_{ACT}} \quad (4.11)$$

Fig. 4.6 shows how both the electrostatic force ( $F_{elec}$ ) and compensated spring restoring force ( $F_{sp}$ ) increase with increasing displacement. The relay turns ON when the displacement reaches  $x_{PI-NS}$ .

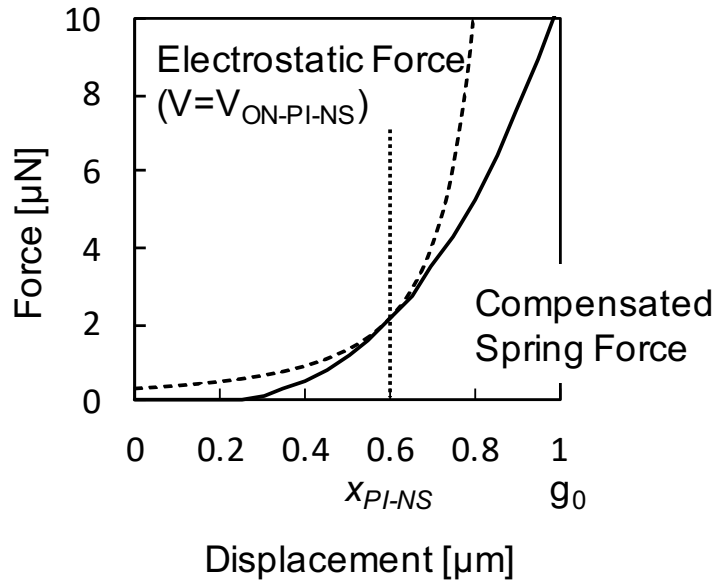


Figure 4.6: Compensated spring restoring force ( $F_{sp}$ ) and electrostatic actuation force ( $F_{elec}$ ) vs. gate displacement ( $x$ ) for a device with actuation gap  $g_0 = 1\mu m$ . Pull-in occurs at  $x_{PI-NS} = (3/5)g_0$ .

To turn OFF the device, the spring restoring force must overcome the electrostatic force plus the contact adhesive force, *i.e.*

$$F_{sp} > F_{elec} + F_{adh} \quad (4.12)$$

$$V_{OFF-NS} = \sqrt{\frac{2(\kappa_{NS-CUB}g_d^3 - F_{adh})(g_0 - g_d)^2}{\epsilon_0 A_{ACT}}} \quad (4.13)$$

The hysteresis voltage,  $V_H$  is the difference between the turn-ON and turn-OFF voltages:

$$V_{H-PI-NS} = \sqrt{\frac{216}{3125}\kappa_{NS-CUB}g_0^5\epsilon_0 A_{ACT}} - \sqrt{\frac{2(\kappa_{NS-CUB}g_d^3 - F_{adh})(g_0 - g_d)^2}{\epsilon_0 A_{ACT}}} \quad (4.14)$$

### Scaling Analysis

To understand the impact of a compensated spring system (compared against a conventional linear spring system) on relay turn-ON voltage and switching energy, consider the simple 2-terminal parallel-plate MEM switch in Fig. 4.7 as a model system. The movable conductive anode of doped polycrystalline  $\text{Si}_{0.4}\text{Ge}_{0.6}$  with residual stress  $\sigma_0 = -100$  MPa is suspended above a fixed cathode. The spring structure comprises one fixed-fixed buckled beam and 4 folded-flexure beams. When a voltage difference is applied across the anode and cathode, the anode is actuated towards the cathode, moving through the air gap of thickness  $g_0$ . When the anode is displaced by  $g_0$ , it contacts the cathode allowing current to flow between the cathode and anode.

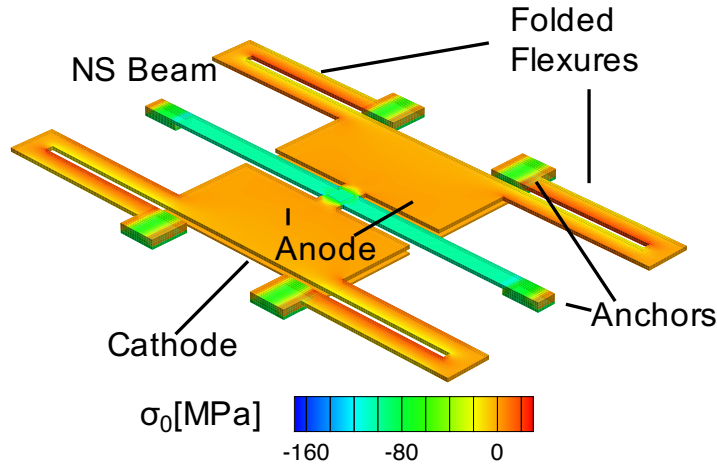


Figure 4.7: Model 2-terminal MEM switch with compensated stiffness.

Fig. 4.8 compares  $V_{ON-PI_{NS}}$  for relays of equal spring restoring energy.

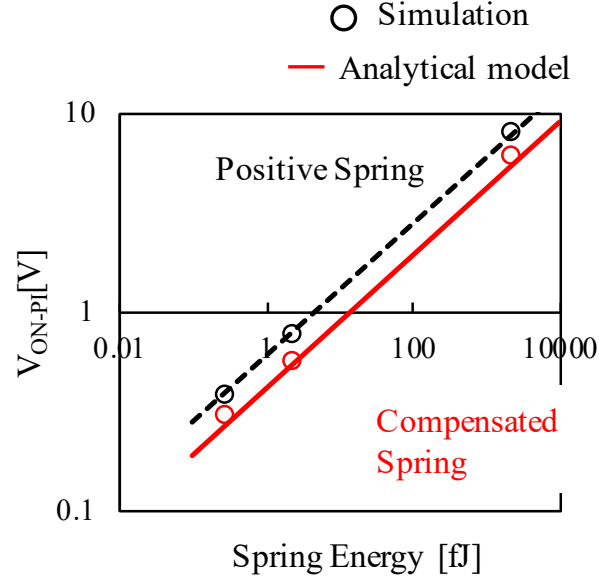


Figure 4.8: Comparison of turn-ON voltage as a function of spring restoring energy for compensated vs. conventional pull-in mode MEM switch designs.

Note that the maximum spring restoring energies ( $E_{sp}$ ) for the conventional (positive stiffness spring) design and the compensated-stiffness spring design are  $E_{sp} = 0.5kg_0^2$  and  $E_{sp} = 0.25k_2g_0^4$ , respectively. Substituting into the corresponding  $V_{ON-PI}$  formulas, the ratio of pull-in voltage values is:

$$\frac{V_{ON-PI_{NS}}}{V_{ON-PI}} = \sqrt{\frac{216\kappa_{NS-CUB}g_0^5}{3125\epsilon_0 A_{ACT}}} / \sqrt{\frac{8kg_0^3}{3125\epsilon_0 A_{ACT}}} \quad (4.15)$$

$$\frac{V_{ON-PI_{NS}}}{V_{ON-PI}} = \sqrt{\frac{864E_{SP}g_0}{3125\epsilon_0 A_{ACT}}} / \sqrt{\frac{16E_{SP}g_0}{27\epsilon_0 A_{ACT}}} \quad (4.16)$$

This indicates a turn-ON voltage reduction  $> 30\%$ , which provides for  $> 50\%$  reduction in switching energy since  $E_{dyn} = \frac{1}{2}CV_{DD}^2$ .

As the relay size is scaled down in all dimensions, its pull-in voltage also is reduced according to the following table:

Table 4.1: Pull-in voltage scaling for the compensated-stiffness pull-in mode relay design.

Device Parameter	Scaling Factor
W	$1/S$
H	$1/S$
L	$1/S$
$\kappa_{NS} = \frac{\pi^4 EWH}{8L^3}$	$\frac{\frac{1}{S} \cdot \frac{1}{S}}{\frac{1}{S^3}} = S$
$g_0$	$1/S$
$A_{ACT}$	$1/S^2$
$V_{ON-PI_{NS}}$	$\sqrt{\frac{1}{S}}$

Coventorware simulations were found to match well theoretical predictions that compensated-stiffness switches retain a switching energy advantage with scaling, as shown in Fig. 4.9.

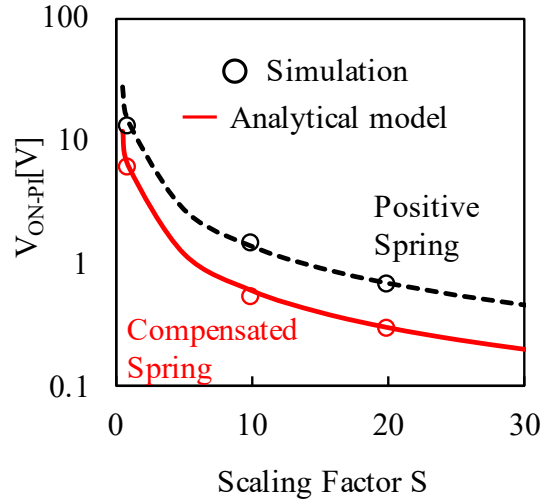


Figure 4.9: Turn-ON voltage scaling for pull-in mode relays.

## Non-Pull-In Mode Compensated Stiffness Relay Analysis

If the as-fabricated contact gap size is smaller than 3/5 of the actuation gap, *i.e.*,  $g_d \leq x_{PI-NS}$ , a compensated-stiffness relay will turn ON prior to reaching the pull-in condition; thus the device operates in non-pull-in ( $NPI - NS$ ) mode. By solving Eq. 4.10 for  $V_{GB} = V_{ON-NPI_{NS}}$  when  $x = g_d$ , the turn-ON voltage for a compensated-stiffness relay operating in non-pull-in mode can be found:

$$V_{ON-NPI_{NS}} = \sqrt{\frac{2\kappa_{NS-CUB}g_d^3(g_0 - g_d)^2}{\epsilon_0 A_{ACT}}} \quad (4.17)$$

The turn-OFF voltage remains the same:

$$V_{OFF-NS} = \sqrt{\frac{2(\kappa_{NS-CUB}g_d^3 - F_{adh})(g_0 - g_d)^2}{\epsilon_0 A_{ACT}}} \quad (4.18)$$

Therefore, the hysteresis voltage for a compensated-stiffness NPI-mode relay is:

$$V_{H-NPI} = \sqrt{\frac{2\kappa_{NS-CUB}g_d^3(g_0 - g_d)^2}{\epsilon_0 A_{ACT}}} - \sqrt{\frac{2(\kappa_{NS-CUB}g_d^3 - F_{adh})(g_0 - g_d)^2}{\epsilon_0 A_{ACT}}} \quad (4.19)$$

The switching energy can be modeled as the change in energy stored in the capacitor, from the ON state to the OFF state.

$$E = V_{GB}(C_{ON}V_{GB} - C_{OFF}|V_B|) \quad (4.20)$$

## Comparison between Conventional and Compensated-Stiffness Relays

Conventional wisdom suggests that the minimum switching energy is achieved by reducing the spring stiffness; however, prior work found that body-biased relay designs with increased stiffness can achieve improved energy-delay tradeoff [18, 22]. In this section, the hysteresis voltage and switching energy of low-stiffness vs. high-stiffness compensated relay designs are examined.

Fig. 4.10 shows how the hysteresis voltage depends on actuation gap to contact gap ratio, for conventional vs. compensated-stiffness relays with fixed contact gap  $g_d$  and increasing  $g_0$ , and barely enough spring restoring force to overcome the contact adhesive force (*i.e.*, for

the compensated relay  $F_{sp} = F_{adh} = \kappa_{NS-CUB} g_d^3$  (or  $\kappa_{NS-CUB} = \kappa_0 = F_{adh}/g_d^3$ ), and for the conventional relay  $F_{sp} = F_{adh} = k_0 g_d$ .

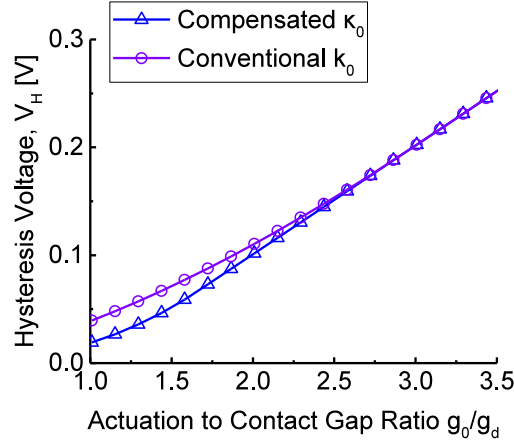


Figure 4.10: Hysteresis voltage vs. actuation-to-contact-gap ratio for conventional vs. compensated-stiffness relay designs with minimum spring restoring force ( $F_{sp} = F_{adh}$  when  $x = g_d$ ).

From this figure it can be seen that, for a low stiffness spring, the minimum hysteresis voltage is achieved with  $g_0 = g_d$  (PI-mode operation). However, this design is more susceptible to stuck-ON failure.

As can be seen from Fig. 4.11 for relays with high spring stiffness ( $\kappa_{NS-CUB} = 10\kappa_0$  for the compensated-stiffness relay design and  $k = 10k_0$  for the conventional relay design), the minimum hysteresis voltage is achieved with a gap ratio at the boundary between PI-mode and NPI-mode operation, at  $g_0 = 3g_d$  for the conventional design and  $g_0 = (5/3)g_d$  for the compensated-stiffness design.

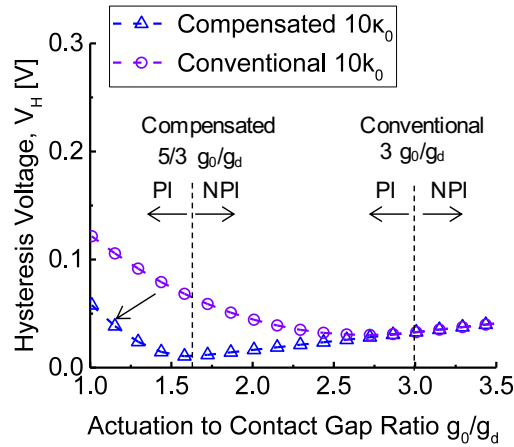


Figure 4.11: Hysteresis voltage vs. actuation-to-contact-gap ratio for a conventional and compensated-stiffness relay design with high spring restoring force ( $F_{sp} = 10F_{adh}$  when  $x = g_d$ ).

Note that compensated-stiffness relay designs can achieve lower hysteresis voltage than conventional relay designs of equal spring restoring force. To minimize the hysteresis voltage, it is ideal to select a high-spring-restoring-force compensated-stiffness design with  $g_d = 0.6g_0$ .

The effect of the actuation gap-to-contact gap ratio on switching energy is shown in Fig. 4.12. For the high-stiffness designs, which can provide for improved device manufacturing yield due to larger spring restoring force (to avoid stuck-ON failure), the switching energy of a compensated-stiffness relay is lower than for a conventional relay. In each case (for high- $F_{sp}$  or low- $F_{sp}$ ) the minimum switching energy for a compensated-stiffness relay is lower.

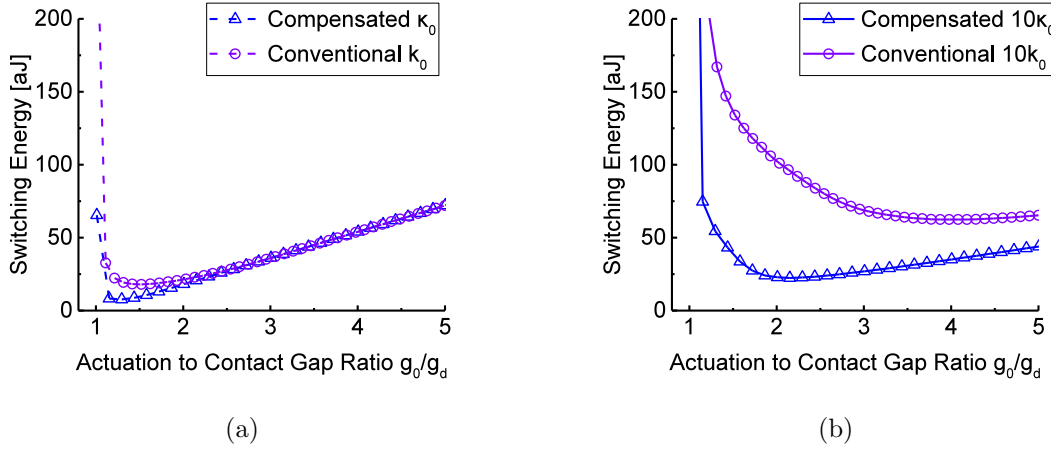


Figure 4.12: Switching energy  $E_{sp}$  vs. actuation-to-contact gap ratio for conventional and compensated relay designs with (a) minimum spring restoring force to overcome  $F_{adh}$ , and (b) high spring restoring force ( $F_{sp} = 10F_{adh}$  when  $x = g_d$ ).

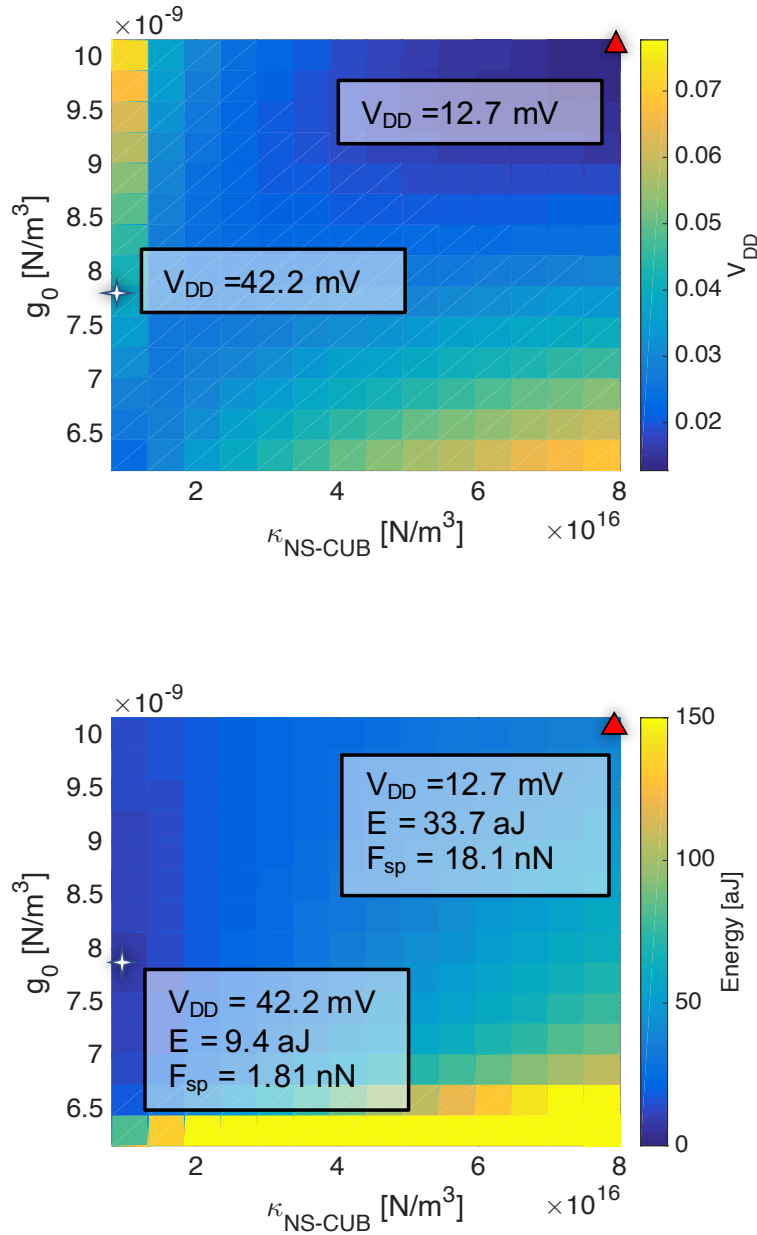
## 4.4 Compensated-Stiffness Relay Design Optimization

In the previous sections, the dependence of compensated-stiffness MEM relay performance characteristics on various structural design parameters was presented. The important parameters to consider for design optimization are the contact adhesion force ( $F_{adh}$ ), as-fabricated contact air gap thickness ( $g_d$ ), as-fabricated actuation air gap thickness ( $g_0$ ), actuation area ( $A_{ACT}$ ), structural poly-Si<sub>0.4</sub>Ge<sub>0.6</sub> layer thickness ( $H$ ), cubic spring coefficient ( $\kappa_{NS-CUB}$ ), body bias voltage ( $V_B$ ) and operating voltage ( $V_{DD}$ ).  $F_{adh}$  is dependent on the area of the contact dimple region and should be as small as possible.  $A_{ACT}$  may be limited by device density and cost considerations. Herein the following parameter values are assumed to be achievable with the capabilities of current manufacturing technology:  $g_d \geq 5nm$ ,  $A_{ACT} = 1 \mu m^2$ ,  $H = 30 nm$ , and  $F_{adh} = 1.81 nN$ . A practical challenge for compensated-stiffness relay design is that, although a high value of  $\kappa_{NS-CUB}$  is beneficial, it is difficult to achieve this in practice based on material properties. Below we consider both the case where the value of  $\kappa_{NS-CUB}$  is unlimited and also the case where  $\kappa_{NS-CUB} \leq 8 \times 10^{15} N/m^3$ .

### $V_{DD}$ Optimization with Unlimited $\kappa_{NS-CUB}$

Minimizing  $V_{DD}$  can be the design objective if the energy consumption is dominated by interconnect delay. If this is the case, then we can set  $V_{DD}$  to the minimum voltage of  $V_H$  and set  $V_B$  to  $-V_{RL}$ . In this case,  $g_0$ ,  $g_d$ , and  $\kappa_{NS-CUB}$  remain to be optimized.

For a large value of cubic stiffness  $\kappa_{NS-CUB}$  it is best to minimize  $g_d$  for low switching energy.  $g_d$  is therefore set to a value of 6.1 nm ( $= \sqrt[3]{F_{adh}/8 \times 10^{15} \text{N/m}^3}$ ) for the contour plots in Fig. 4.14 which show the dependence of  $V_{DD}$ , switching energy and switching delay on  $\kappa_{NS-CUB}$  and  $g_0$ . In these plots  $\kappa_{NS-CUB}$  is set to be within the range from  $8 \times 10^{15} \text{N/m}^3$  ( $= F_{adh}/g_d^3$ , or the minimum value required to ensure  $F_{sp} > F_{adh}$ ) to  $8 \times 10^{16} \text{N/m}^3$ , and  $g_0$  is set to be within the range from 6.1 nm to 10 nm, traversing PI-mode and NPI-mode operation. It can be seen that  $V_{DD}$  is minimized by increasing both  $\kappa_{NS-CUB}$  and  $g_0$ .



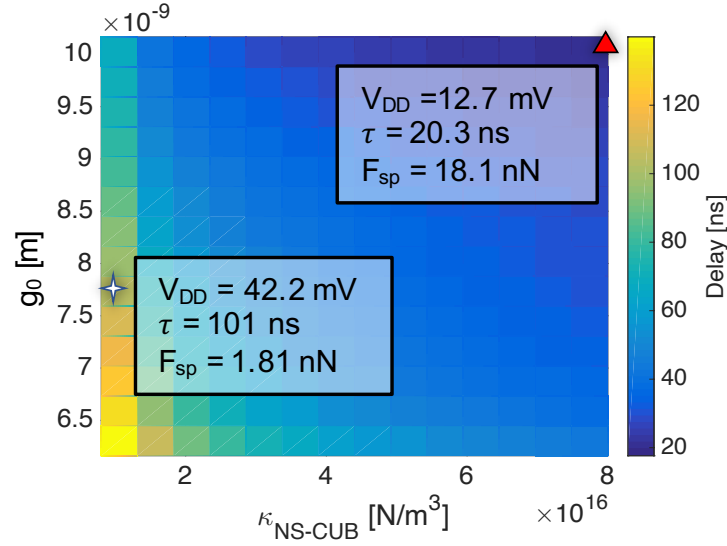


Figure 4.14:  $V_{DD}$ , switching energy and switching delay as a function of the cubic spring coefficient  $\kappa_{NS-CUB}$  and actuation gap  $g_0$ .  $g_d = 6.1$  nm. A high- $\kappa_{NS-CUB}$  design provides for minimum  $V_{DD}$  (denoted by the red triangle) while a lower- $\kappa_{NS-CUB}$  design achieves minimum switching energy (denoted by the white star).

For low- $F_{sp}$  relay operation with no body biasing, Fig. 4.15 compares the energy-delay trade-off for a compensated-stiffness relay against that for an optimized conventional relay as designed in [18]. It can be seen that the compensated-stiffness design has slightly lower minimum switching energy but increased switching delay relative to the conventional design.

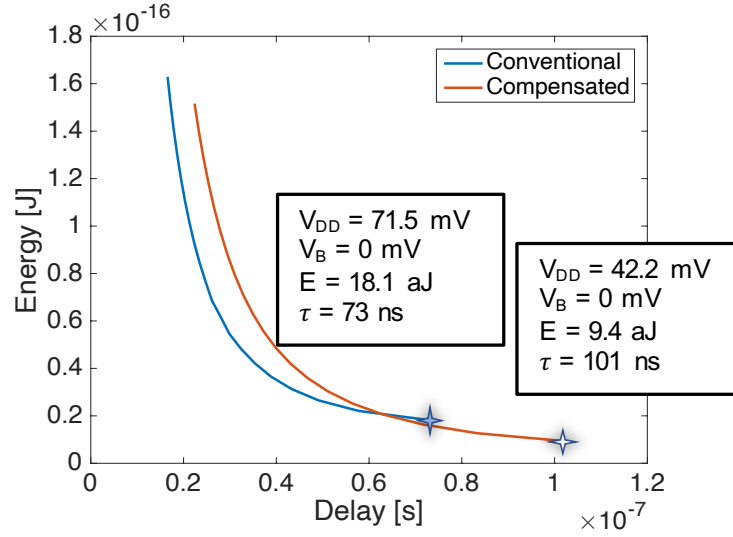


Figure 4.15: Energy-delay trade-off for minimum- $F_{sp}$  relay designs for operation with zero body bias voltage.

For high- $F_{sp}$  relay operation with body biasing to enable low  $V_{DD}$ , Fig. 4.16 compares the energy-delay trade-off for a compensated-stiffness relay against that for an optimized conventional relay. The curves (labeled "Constant  $V_{DD} + |V_B|$ ") show how relay switching energy can be decreased by increasing the magnitude of the body bias voltage in order to lower  $V_{DD}$ . The symbols (labeled "Increase  $V_{DD}$ ") show how the switching delay can be improved further by increasing  $V_{DD}$  (with a fixed maximum value of  $|V_B|$ ) with improved overall energy-delay tradeoff. It can be seen that the compensated-stiffness design provides for substantially lower switching energy at sub-20 ns switching delays.

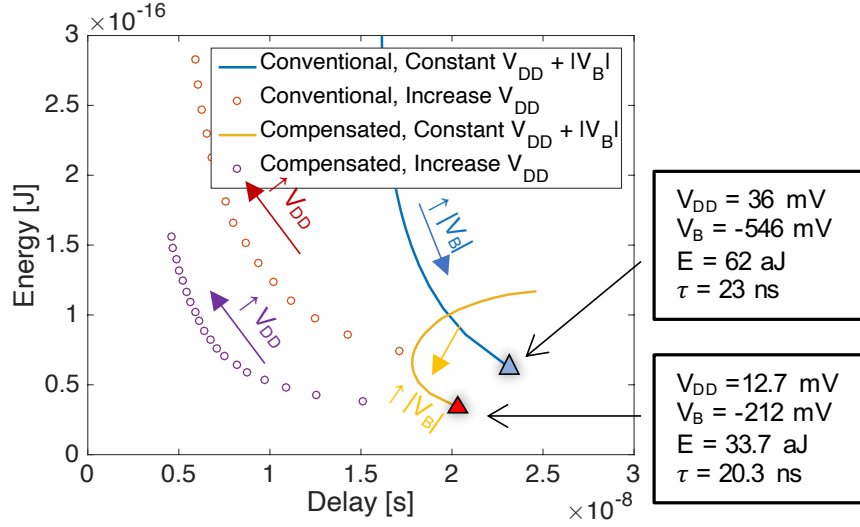


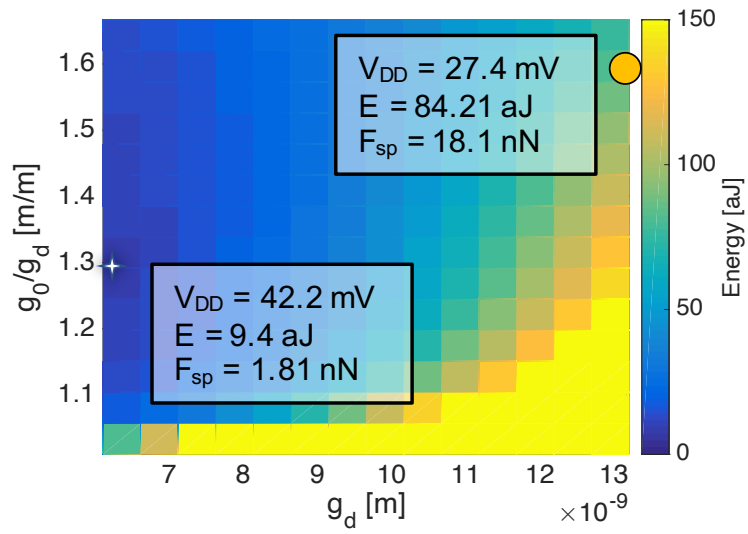
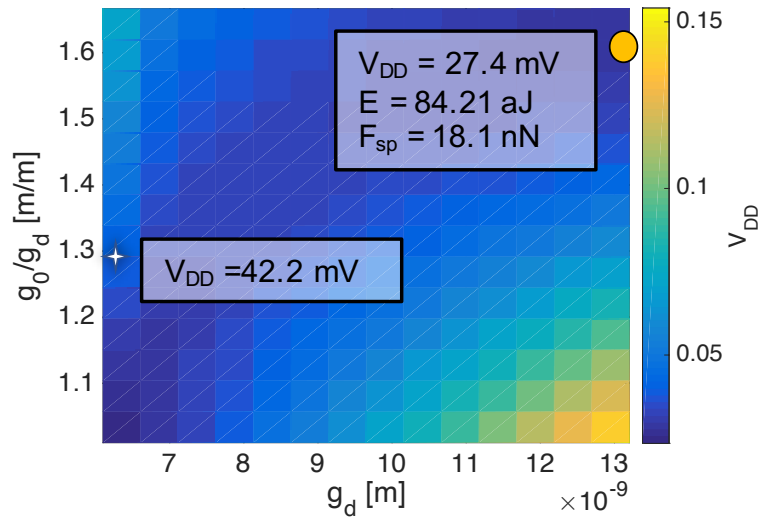
Figure 4.16: Energy-delay trade-off for high- $F_{sp}$  ( $= 10F_{adh}$  when  $x = g_d$ ) relay designs for operation with body biasing.

Interestingly, for the compensated-stiffness relay design, increasing  $V_B$  while keeping  $V_{DD} + |V_B|$  constant shows a non-monotonic relationship between switching energy and switching delay: initially, increasing  $|V_B|$  improves delay as the spring restoring force increases at a slower rate than the electrostatic actuation force; however, the spring restoring force eventually increases at a faster rate as  $|V_B|$  continues to increase, causing the switching delay to increase.

### $V_{DD}$ Optimization with Limited $\kappa_{NS-CUB}$

If polycrystalline  $\text{Si}_{0.4}\text{Ge}_{0.6}$  is used as the structural material, it is difficult to achieve very high  $\kappa_{NS-CUB}$ ; therefore, in order to increase  $F_{sp}(= \kappa_{NS-CUB}g_d^3)$ ,  $g_d$  must be increased. Herein the case where  $\kappa_{NS-CUB}$  is limited to be no greater than  $8 \times 10^{15} \text{ N/m}^3$  (an achievable value of spring coefficient, cf. Fig. 4.4), is analyzed.

The contour plots in Fig. 4.18 show how  $V_{DD}$ , switching energy and delay depend on  $g_d$  and the actuation gap-to-contact gap ratio.  $g_d$  ranges from 6.1 nm to 13.1 nm, corresponding to the value required to achieve  $F_{sp} = 10F_{adh}$  when  $x = g_d$ . It can be seen that although increasing  $g_d$  can help to reduce  $V_{DD}$ , this comes at a trade-off of larger switching energy.



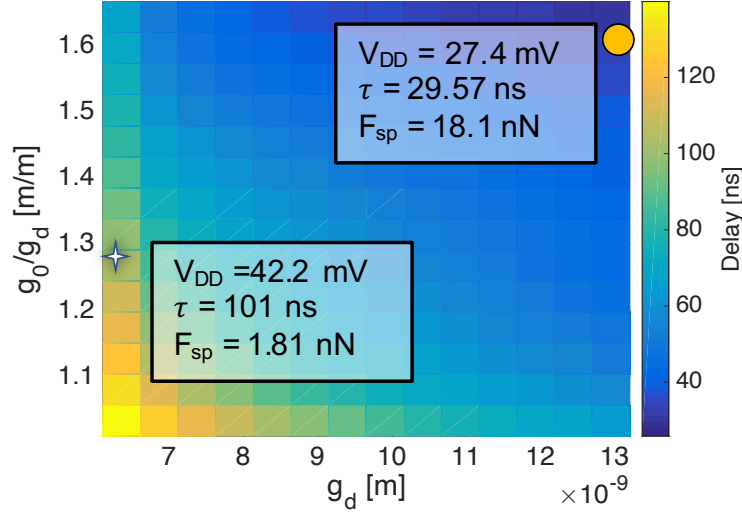


Figure 4.18:  $V_{DD}$ , switching energy and switching delay as a function of the contact gap  $g_d$  and actuation gap-to-contact gap ratio.  $\kappa_{NS-CUB} = 8 \times 10^{15} \text{ N/m}^3$ . A large- $g_d$  design provides for minimum  $V_{DD}$  (denoted by the yellow circle) while a lower- $g_d$  design achieves minimum switching energy (denoted by the white star).

In summary, compensated-stiffness relay designs can achieve lower  $V_{DD}$  than can conventional relay designs, which is beneficial if energy consumption is interconnect-dominated. The manufacturing yield for compensated-stiffness relays can be improved by increasing the contact gap size  $g_d$  to increase  $F_{sp}$ , at the trade-off of larger switching energy. It is a practical challenge to achieve fixed-fixed beams with sufficiently high  $F_{sp}$  to avoid stuck-ON failure. Optimized non-linear springs designs or different material systems may allow larger values of  $\kappa_{NS-CUB}$  to be achieved in the future.

## 4.5 Impact of Process-Induced Variations

The addition of the fixed-fixed buckled beam in a compensated-stiffness relay can result in greater sensitivity of the turn-ON voltage ( $V_{ON}$ ) and turn-OFF voltage ( $V_{OFF}$ ) to variations in the device fabrication process. In this section, an aggressively scaled compensated-stiffness relay is proposed and studied to identify critical process variation parameters.

In developing the scaled relay design, some challenges and practical considerations were taken into account. The design window for the fixed-fixed beam is quite small, since adjustments to design parameters to increase  $|k_{NS-LIN}|$  will also decrease  $\kappa_{NS-CUB}$ . Also, it is

unrealistic to have very high residual stress in the structural material, because this would undesirable buckling of the movable plate electrode. To relax the design constraints, a relay design incorporating two fixed-fixed buckled beams is proposed, as shown in Fig. 4.19.

In this compensated-stiffness relay design, the doped polycrystalline- $\text{Si}_{0.4}\text{Ge}_{0.6}$  gate electrode is suspended above a fixed tungsten body electrode by two compensated-stiffness spring structures, separated by an actuation gap ( $g_0 = 10$  nm). Each compensated-stiffness spring structure consists of a fixed-fixed buckled beam and two folded-flexure beams (linear springs) designed such that  $k_{LIN}$  is close to  $-k_{LIN-NS}$ . When a voltage is applied across the gate and body, the movable gate is actuated toward the body until the tungsten drain electrodes (attached beneath the movable gate electrode and separated from it by a thin layer of electrically insulating  $\text{Al}_2\text{O}_3$ ) physically contacts underlying source electrodes (coplanar with the fixed body electrode). Note that this relay design incorporates two pairs of source/drain electrodes, so that it has a total of six terminals. To turn off the device, the spring restoring force must be greater than the electrostatic actuation force plus the contact adhesive forces.

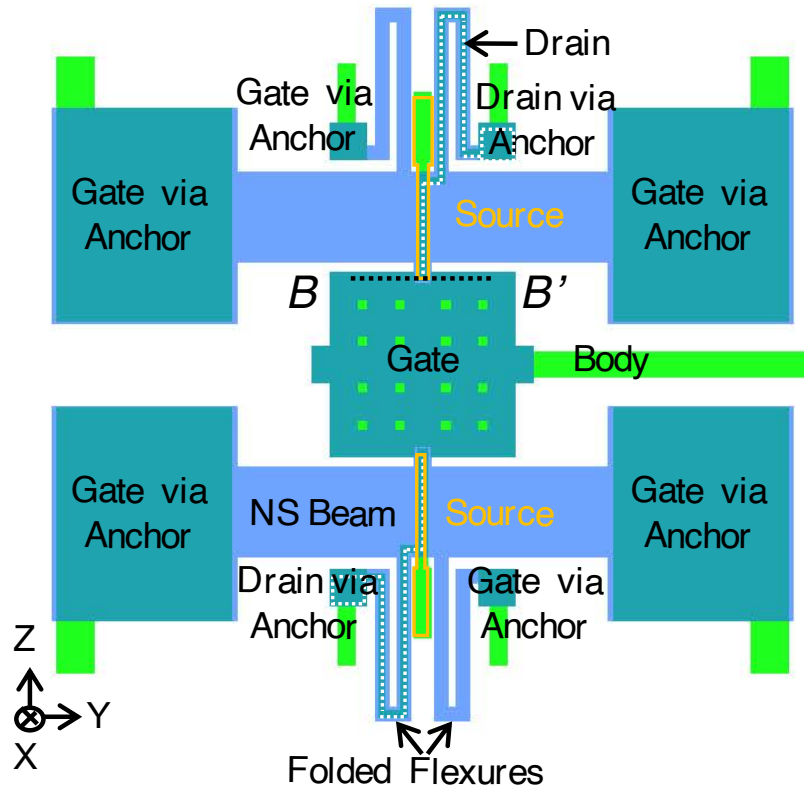


Figure 4.19: Plan view schematic illustrating the scaled compensated-stiffness relay design.

In principle this relay can be fabricated using the following process steps, starting with an insulating substrate (*e.g.*, Al<sub>2</sub>O<sub>3</sub>-coated silicon wafer): a 3 nm-thick tungsten (W) layer is deposited and patterned to form the body electrode, source electrodes, and drain anchors. Then, a 4.2 nm-thick SiO<sub>2</sub> layer (SiO<sub>2</sub>-1) is deposited as a first sacrificial layer. The contact dimples are defined by etching away the SiO<sub>2</sub>-1 in the source electrode contact regions. A 5.8 nm-thick second sacrificial layer of SiO<sub>2</sub> (SiO<sub>2</sub>-2) is then deposited. (The sum of the two SiO<sub>2</sub> layer thicknesses corresponds to  $g_0$ , while the thickness of SiO<sub>2</sub>-2 corresponds to  $g_d$ .) Afterwards, the SiO<sub>2</sub> in the drain anchor regions is etched away (not shown), and a second layer of 3 nm-thick W is deposited and patterned to form the dimpled drain electrodes. Then another 1 nm-thick layer of Al<sub>2</sub>O<sub>3</sub> is deposited to electrically insulate the drain electrodes from the movable gate electrode. Anchor regions for the movable gate electrode are then formed by removing the Al<sub>2</sub>O<sub>3</sub> and underlying SiO<sub>2</sub> in these regions before deposition of 30 nm-thick heavily p-type doped (p+) poly-Si<sub>0.4</sub>Ge<sub>0.6</sub> structural film (assumed to have residual compressive stress  $\sigma_0 = -100$  MPa). A hard-mask layer of SiO<sub>2</sub> is deposited prior to patterning the structural film and the topmost Al<sub>2</sub>O<sub>3</sub> layer, exposing the SiO<sub>2</sub>-2 layer. Finally vapor HF is used to selectively remove the sacrificial SiO<sub>2</sub>, to avoid capillary-force-induced stiction. Fig. 4.20 shows a schematic cross-section of the relay along the B-B' cutline prior to sacrificial oxide removal.

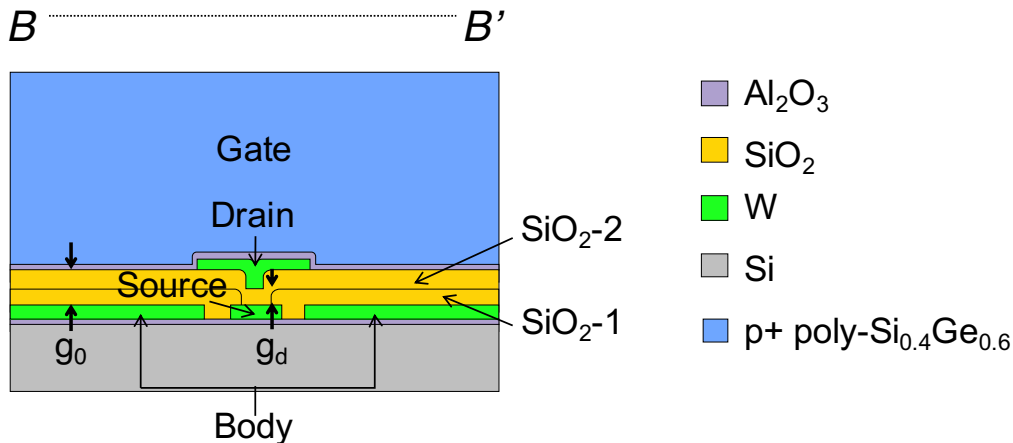


Figure 4.20: Schematic cross-section of the proposed scaled compensated-stiffness relay, prior to removal of the sacrificial oxide layers.

Four of the aforementioned steps are selected for process-induced variation study. The SiO<sub>2</sub>-1 and SiO<sub>2</sub>-2 deposition steps are important because they determine  $g_0$  and  $g_d$ . In addition, the Si<sub>0.4</sub>Ge<sub>0.6</sub> deposition step is important because the structural film thickness affects the spring stiffnesses  $k_{LIN}$  and  $k_{NS}$ . Patterning of the Si<sub>0.4</sub>Ge<sub>0.6</sub> layer is also important because overetch can affect the spring stiffness as well as the actuation area.

## Fully Compensated Stiffness Relay

To study the sensitivity of the compensated stiffness relay switching voltages to process-induced variations, the impact of  $\pm 5\%$  change in each process parameter on  $V_{ON-NPI_{NS}}$  was assessed using an analytical method. Values of  $g_0$ ,  $g_d$ ,  $k_{LIN}$ ,  $k_{NS}$  and  $\kappa_{NS-CUB}$  were calculated and used in the force balance equation 4.10, assuming non-pull-in mode operation, to numerically solve for the turn-ON voltage ( $V_{ON-NPI_{NS}}$ ):

$$\frac{1}{2} \frac{\epsilon_0 A_{ACT}}{g_0 - g_d} V_{ON-NPI_{NS}}^2 \geq \kappa_{NS-CUB} g_d^3 + k_{NS-LIN} g_d + k_{LIN} g_d \quad (4.21)$$

The corresponding equation was numerically solved to find  $V_{OFF_{NS}}$ :

$$\frac{1}{2} \frac{\epsilon_0 A_{ACT}}{g_0 - g_d} V_{OFF_{NS}}^2 + F_{adh} \leq \kappa_{NS-CUB} g_d^3 + k_{NS-LIN} g_d + k_{LIN} g_d \quad (4.22)$$

Fig. 4.21 shows the effects of process-induced variations in SiO<sub>2</sub>-1 thickness, SiO<sub>2</sub>-2 thickness, Si<sub>0.4</sub>Ge<sub>0.6</sub> thickness, and Si<sub>0.4</sub>Ge<sub>0.6</sub> overetch on the switching voltages for a relay designed to have *i.e.*,  $k_{LIN} = k_{NS-LIN}$  for 0% process variation. It can be seen that the most critical parameters to tightly control in the manufacturing process are the Si<sub>0.4</sub>Ge<sub>0.6</sub> layer thickness and the SiO<sub>2</sub>-2 layer thickness, and that it is possible for  $V_{OFF-NPI_{NS}}$  to have no real solutions (so that the relay does not turn OFF for zero gate voltage) if these layers are too thin.

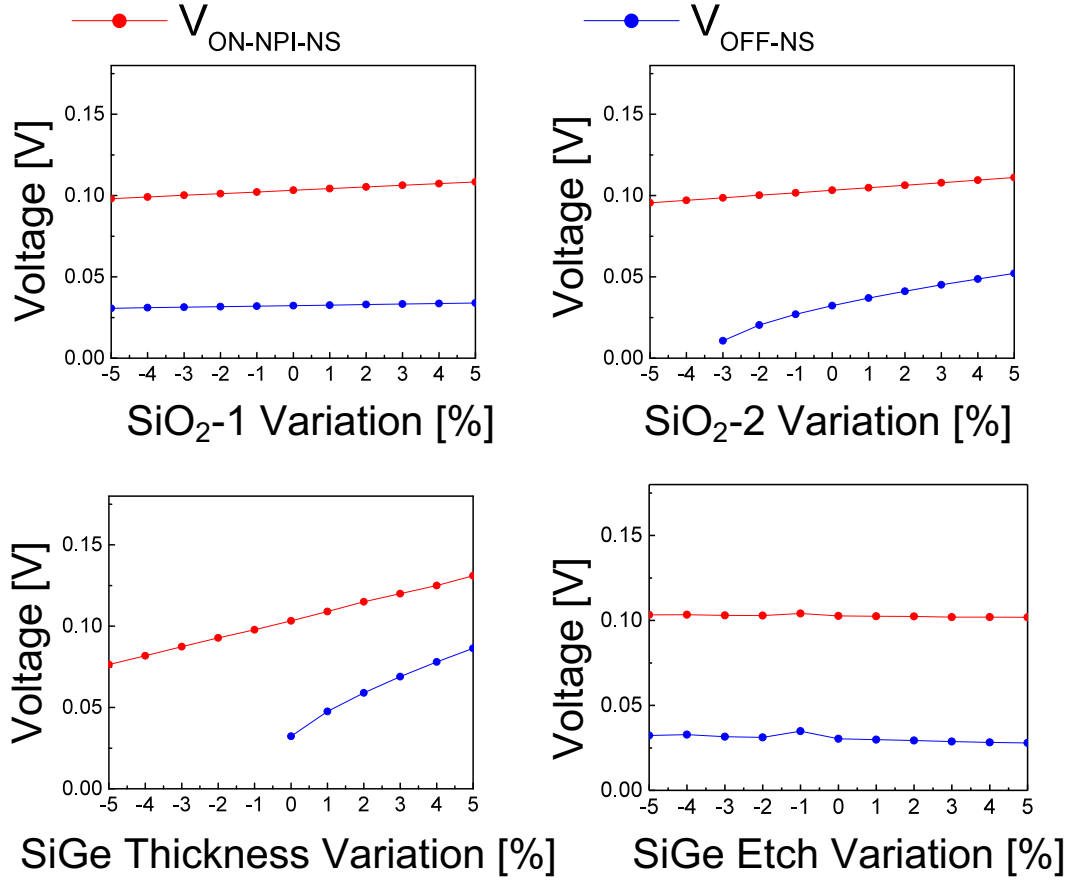


Figure 4.21: Impact of process-induced variations on the switching voltages for a scaled, fully compensated-stiffness relay design.

With a decrease in the thickness of the  $SiO_2$ -2 layer,  $g_d$  decreases, which reduces the total spring restoring force ( $F_{sp} = \kappa_{NS-CUB}g_d^3$ ). In this case, the spring restoring force is no longer sufficient to overcome the adhesion force with  $F_{elec} = 0$  N and hence the device will be susceptible to stuck-ON failure. To avoid this mode of failure, the relay should be designed to have larger spring restoring force.

A decrease in poly- $Si_{0.4}Ge_{0.6}$  thickness ( $H$ ) causes the spring restoring force to no longer be fully compensated. This can be understood by examining the coefficients of linear stiffness:  $k_{LIN} \propto H^3$  and  $k_{NS-LIN} \propto \alpha H + \beta H^3$  [17]. Decreasing  $H$  will decrease  $k_{LIN}$  at a faster rate than  $|k_{NS-LIN}|$ . If the spring restoring force is no longer fully compensated, the device will not turn OFF when  $F_{elec} = 0$  N. This issue can be resolved by only partially compensating the stiffness of the linear springs, *i.e.*, designing the relay such that  $k_{LIN} > |k_{NS-LIN}|$ .

## Partially Compensated Stiffness Relay

Suppose the nominal stiffness of one folded-flexure beam (linear spring) is  $k_{LIN_0}$  [17]:

$$\frac{1}{k_{LIN_0}} = \frac{1}{k_f} + \frac{1}{k_t} = \frac{1}{\gamma_f \frac{EWH^3}{L^3}} + \frac{1}{\gamma_t \frac{GWH^3}{L}} \quad (4.23)$$

where  $\gamma_f$  is the flexural constant,  $\gamma_t$  is the torsional constant, and  $G$  is the Shear Modulus (about 57 GPa).

If the thickness of the poly-Si<sub>0.4</sub>Ge<sub>0.6</sub> structure is reduced by 5 percent ( $\Delta H = -5\%$ ), then the stiffness of the folded-flexure beam becomes:

$$k_{LIN_{\Delta H}} = (1 + \Delta H)^3 k_{LIN_0} \quad (4.24)$$

With four folded flexures, the total nominal linear spring constant is  $4k_{LIN_0}$ .

The total linear stiffness still must be greater than or equal to zero for  $\Delta H = -5\%$ :

$$2k_{NS-LIN_{\Delta H=-5\%}} + 4k_{LIN_{\Delta H=-5\%}} \geq 0 \quad (4.25)$$

$$2 \left( \underbrace{\frac{\pi^2 \sigma_0 WH(1 + \Delta H)}{2L}}_{k_{NS-LIN_-}} + \underbrace{\frac{\pi^4 EW(1 + \Delta H)^3 H^3}{6L^3}}_{k_{NS-LIN_+}} \right) + 4k_{LIN_{\Delta H=-5\%}} \geq 0 \quad (4.26)$$

$$2((1 + \Delta H)k_{NS-LIN_{0-}} + (1 + \Delta H)^3 k_{NS-LIN_{0+}}) + 4(1 + \Delta H)^3 k_{LIN_0} \geq 0 \quad (4.27)$$

$$(1 + \Delta H)^2 k_{NS-LIN_{0+}} + 2(1 + \Delta H)^2 k_{LIN_0} \geq -k_{NS-LIN_{0-}} \quad (4.28)$$

Eq. 4.28 shows that, in order to account for the possibility of -5% process variation in  $H$ , the sum of the positive stiffness terms should be at least  $1/(100\% - 5\%)^2 \approx 110\%$  of the magnitude of the negative stiffness term  $k_{NS-LIN_{0-}}$ .

Fig. 4.22 shows the impact of process-induced variations on the switching voltages for a partially compensated stiffness relay design. It can be seen that by increasing the linear stiffness terms increased by about 10%, this design is robust to +/- 5% process variation.

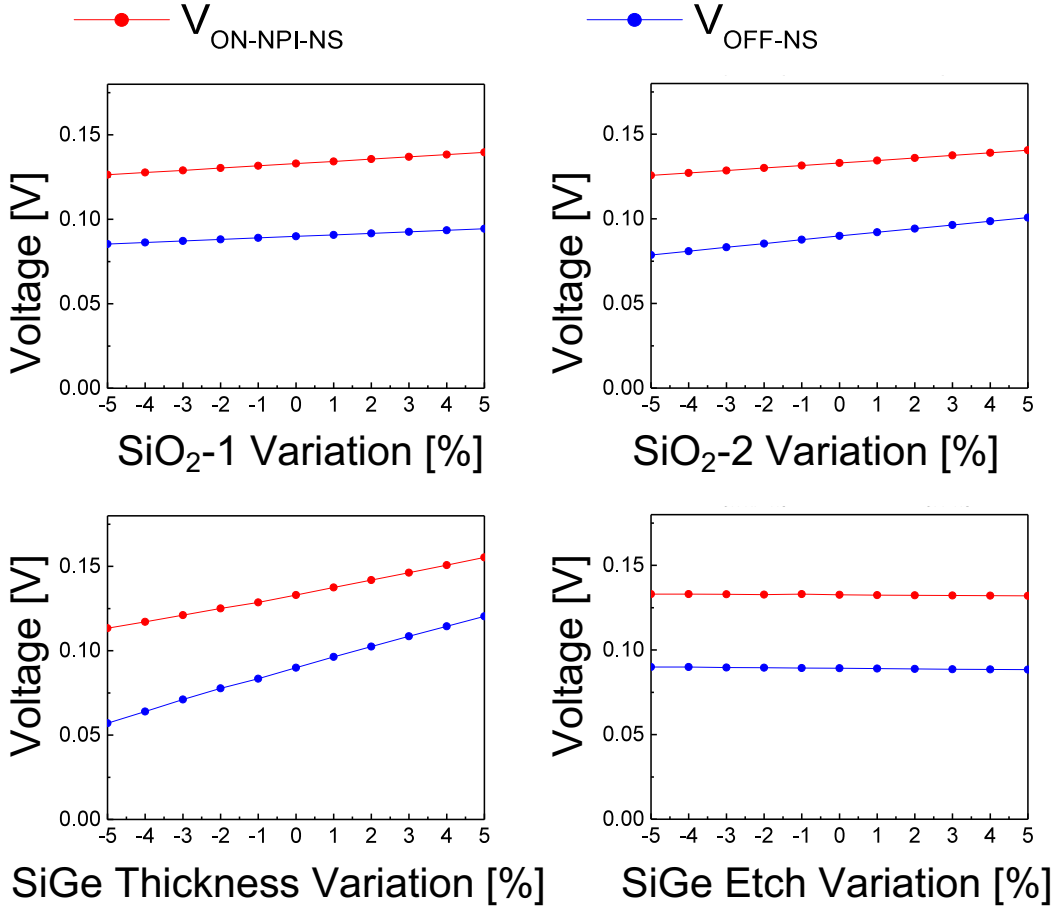


Figure 4.22: Impact of process-induced variations on the switching voltages for a scaled, partially compensated relay design.

### NPI-Mode Partially Compensated Stiffness Relay Analysis

In this subsection the operation of a scaled, partially compensated stiffness relay design is analyzed. The design parameters used for Coventorware simulations are as follows:  $\kappa_{NS-CUB} = 3.5 \times 10^{15} \text{ N/m}^3$ ,  $k_{LIN} + k_{NS-LIN} = 0.85 \text{ N/m}$ ,  $g_0 = 10 \text{ nm}$ ,  $g_d = 4.2 \text{ nm}$ ,  $A_{ACT} = 1 \mu\text{m}^2$ ,  $V_{ON-NPI} = 140 \text{ mV}$ ,  $\sigma_0 = -100 \text{ MPa}$ .

Fig. 4.23 shows how the spring restoring force depends non-linearly on gate displacement, to allow for lower turn-ON voltage and adequate spring-restoring force to avoid stuck-ON failure.

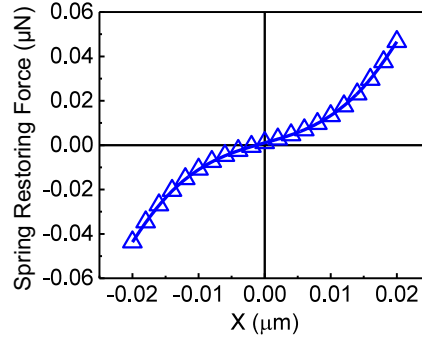


Figure 4.23: Spring restoring force vs. displacement of a partially compensated relay.  $\kappa_{NS-CUB} = 3.5 \times 10^{15} \text{ N/m}^3$ ,  $k_{LIN} + k_{NS-LIN} = 0.85 \text{ N/m}$ .

Fig. 4.24 plots the contact gap size vs. voltage across the gate and body electrodes  $V_{GB}$ ; the point at which the drain electrodes physically contact their corresponding source electrodes is indicated, corresponding to gate displacement  $x = g_d$ . Non-pull-in mode behavior is observed (*i.e.*, there is no sudden change in contact gap size). Note that the simulated native turn-ON voltage ( $V_{GB}$  required to turn ON the relay) is only 140 mV.

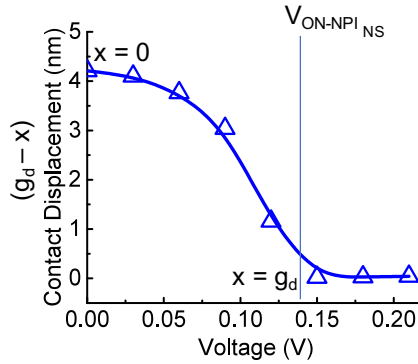


Figure 4.24: Device contact displacement for a partially compensated relay with an applied voltage across the gate and body. The turn-on voltage  $V_{ON-NPI_{NS}} = 0.140 \text{ V}$ .

## 4.6 Summary

A novel approach is proposed in this chapter to reduce relay switching energy without loss of spring restoring force in the ON state (necessary to ensure proper turn-OFF operation), by incorporating one or more structural elements with negative stiffness (fixed-fixed buckled

beams) to compensate the positive stiffness of the linear springs (folded-flexure beams) in a conventional relay design.

For a conventional relay design, the boundary between pull-in and non-pull-in operation corresponds to a contact gap-to-actuation gap ratio  $g_d/g_0 = 1/3$ . In contrast, the boundary between pull-in and non-pull-in operation for a compensated-stiffness relay corresponds to  $g_d/g_0 = 3/5$ . A compensated-stiffness relay design can achieve significantly lower hysteresis voltage and improved energy-delay trade-off, for high spring restoring force and body-biased operation.

To minimize  $V_{DD}$  for a body-biased compensated-stiffness relay, a high spring restoring force can be used together with a large actuation gap size. Ideally, a high value of  $\kappa_{NS-CUB}$  also is desirable for reducing the switching delay ( $\tau$ ). Because this is difficult to achieve in practice, an alternative is to increase the contact gap size ( $g_d$ ) to increase the spring restoring force in the ON state.

The impact of process-induced variations is assessed, and variation in structural layer thickness is identified as the most critical parameter to tightly control in order to achieve high manufacturing yield for the fully compensated stiffness relay design. A partially compensated stiffness relay design is projected to be robust against  $+/-5\%$  variation in the poly-Si<sub>0.4</sub>Ge<sub>0.6</sub> structural layer thickness.

# Chapter 5

## Conclusion

### Summary

Micro-electro-mechanical (MEM) relays have the ideal switching properties of abrupt turn-ON and turn-OFF behavior and zero OFF-state leakage current, which provide for ultra-low-voltage operation (sub-50 mV gate voltage swing). These properties make them attractive to use as switches for energy efficiency digital computing, *e.g.*, for the Internet of Things. This dissertation addresses remaining challenges and opportunities for millivolt relay integrated circuits (ICs) to find practical application.

This dissertation investigates approaches to reducing relay operating voltage, including reducing the number of contact dimples from 4 to 2, coating with an anti-stiction self-assembled monolayer (SAM) and body biasing are investigated and found to be effective, enabling the demonstration of a variety of relay logic circuits operating with sub-50 mV voltage signals, including an inverter, AND, OR, XOR and 2:1 multiplexer (MUX) circuit. Since the operating speed of a relay-based IC is dominated by relay mechanical switching delay, it is desirable to enhance the functionality per relay to minimize the number of mechanical delays and also provide for more compact implementation (smaller chip layout area). Accordingly, multi-functional MEM relays and dynamically reconfigurable MEM relay circuits are demonstrated, including a differential XOR/XNOR circuit, 2-bit 2:1 MUX and body-biased multiple-gate relay circuit.

Practical challenges and opportunities for low-voltage MEM relay IC operation are also examined. In order to test large-scale integrated circuits, it is ideal to be able to operate the relays under room ambient conditions. A new pulsed-voltage method is shown to reliably break down native oxide on tungsten contact electrode surfaces to achieve sub-1k $\Omega$  ON-state resistance with low variation. Degradation of  $R_{ON}$  for low-voltage relay operation under room ambient conditions is studied, including examining the effects of anti-stiction self-assembled molecular coating and body-biasing. The use of a liquid dielectric medium is explored as a method for improving  $R_{ON}$  stability in room ambient conditions. MEM relay

integrated circuits are demonstrated to operate over a wide range of temperatures, with switching voltage swings as low as 25 mV at 77 K and 200 mV at 400 K, showing promise for extreme environment applications.

Finally, this dissertation proposes a novel compensated-stiffness MEM relay design that incorporates fixed-fixed buckled beams with negative stiffness to reduce the switching voltage by  $> 50\%$ . Compensated stiffness relay designs are found to provide for improved trade-off between relay switching energy and turn-on delay for both pull-in-mode and non-pull-in-mode operation. The effects of process-induced variations on compensated stiffness relay switching voltages are studied and the structural layer thickness is identified as a key process parameter to control tightly. A partially compensated stiffness relay is proposed to mitigate the increased susceptibility to process-induced variations. To achieve improved energy-delay trade-off with a compensated stiffness relay, high  $\kappa_{NS-CUB}$  is identified as a key design criterion.

## Future Work

Some suggestions for future research directions are offered below, toward the goal of demonstrating large-scale integrated MEM-relay-based circuits operating with millivolt supply voltage for energy-efficient digital computing.

MEM relay integrated circuit design algorithms can be developed to automatically design and layout large-scale integrated circuits that take advantage of their capability to incorporate multiple source/drain pairs and multiple gate electrodes and to perform with dynamically reconfigurable functionality. A direction for future study could be to develop generalized algorithms to design integrated circuits with multi-functional relays as building blocks in order to minimize the number of logic stages and enhance the benefit of MEM relays.

Packaging or new contact materials for improved ON-state resistance stability should be developed to enable large-scale integrated MEM relay circuits to operate reliably under room ambient environment.

While a separate body bias voltage could be used for each relay to minimize its gate switching voltage and thereby enable the smallest supply voltage for the entire integrated circuit, this approach is impractical. Approaches to reduce process-induced variations in the native turn-ON voltage (magnitude of  $V_{GB}$  required to turn ON the relay) are needed to enable a single body bias voltage for all N-relays and a single body bias voltage for all P-relays to be used in a large-scale integrated circuit. Reduced process variation could be achieved with more precise control of thin-film thicknesses and residual stress.

The improved energy-delay trade-off of an ultimately scaled compensated-stiffness relay design makes it attractive for future ultra-low-power digital computing applications. How-

ever, significant challenges for minimizing process-induced variations and controlling the effective stiffness of fixed-fixed buckled beams remain to be overcome, to achieve high manufacturing yield. It is also worth noting that an experimental proof-of-concept has yet to be demonstrated.

# Bibliography

- [1] T. N. Theis and H. S. Philip Wong, “The End of Moore’s Law: A New Beginning for Information Technology,” *Computing in Science and Engineering*, vol. 19, no. 2, pp. 41–50, 2017, ISSN: 15219615. DOI: 10.1109/MCSE.2017.29.
- [2] A. Andrae and T. Edler, “On Global Electricity Usage of Communication Technology: Trends to 2030,” *Challenges*, vol. 6, pp. 117–157, Apr. 2015. DOI: 10.3390/challe6010117.
- [3] G. Yeap, *Practical Low Power Digital VLSI Design*, 1st. Boston, MA: Springer US, 1998, ISBN: 978-1-4613-7778-8. DOI: 10.1007/978-1-4615-6065-4. [Online]. Available: <http://link.springer.com/10.1007/978-1-4615-6065-4>.
- [4] K. K. Ng and S. Sze, “Physics and properties of semiconductors - A review,” in *Physics of Semiconductor Devices*. John Wiley Sons, Ltd, 2006, pp. 5–75, ISBN: 9780470068328. DOI: <https://doi.org/10.1002/9780470068328.ch1>. [Online]. Available: <https://onlinelibrary.wiley.com/doi/abs/10.1002/9780470068328.ch1>.
- [5] R. S. Muller, T. I. Kamins, and M. Chan, *Device electronics for integrated circuits*. Wiley, 2003.
- [6] I.-R. Chen, “Novel material integration for reliable and energy-efficient NEM relay technology,” PhD thesis, EECS Department, University of California, Berkeley, 2014. [Online]. Available: <http://www2.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-227.html>.
- [7] T.-J. K. Liu, “E3S EAB Meeting Update. Theme 2: Nanomechanics,” E3S EAB Meeting Update, 2018.
- [8] F. Chen, H. Kam, D. Marković, T.-J. K. Liu, V. Stojanović, and E. Alon, “Integrated circuit design with NEM relays,” in *Proceedings of the 2008 IEEE/ACM International Conference on Computer-Aided Design*, 2008, pp. 750–757.
- [9] M. Spencer, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T. J. K. Liu, D. Marković, E. Alon, and V. Stojanović, “Demonstration of integrated micro-electro-mechanical relay circuits for VLSI applications,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 308–320, 2011, ISSN: 00189200. DOI: 10.1109/JSSC.2010.2074370.

- [10] S. Dutta, “Floating-point unit (FPU) designs with nano-electromechanical (NEM) relays,” 2013. [Online]. Available: <http://dspace.mit.edu/handle/1721.1/84724>.
- [11] S. Saha, M. S. Baghini, M. Goel, and V. R. Rao, “Sub-50-mV nanoelectromechanical switch without body bias,” *IEEE Transactions on Electron Devices*, vol. 67, no. 9, pp. 3894–3897, 2020. DOI: 10.1109/TED.2019.2951615.
- [12] B. Osoba, B. Saha, L. Dougherty, J. Edgington, C. Qian, F. Niroui, J. H. Lang, V. Bulović, J. Wu, and T.-J. K. Liu, “Sub-50 mV NEM relay operation enabled by self-assembled molecular coating,” in *International Electron Devices Meeting*, vol. 1, 2016, pp. 655–658, ISBN: 9781509039029. DOI: 10.1109/IEDM.2016.7838489.
- [13] U. Zaghloul and G. Piazza, “Sub-1-Volt piezoelectric nanoelectromechanical relays with millivolt switching capability,” *IEEE Electron Device Letters*, vol. 35, no. 6, pp. 669–671, 2014, ISSN: 07413106. DOI: 10.1109/LED.2014.2318049.
- [14] F. Chen, M. Spencer, R. Nathanael, C. Wang, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. K. Liu, D. Marković, V. Stojanović, and E. Alon, “Demonstration of integrated micro-electro-mechanical switch circuits for VLSI applications,” in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 150–151. DOI: 10.1109/ISSCC.2010.5434010.
- [15] H. Fariborzi, F. Chen, V. Stojanović, R. Nathanael, J. Jeon, and T.-J. K. Liu, “Design and demonstration of micro-electro-mechanical relay multipliers,” in *IEEE Asian Solid-State Circuits Conference*, 2011, pp. 117–120. DOI: 10.1109/ASSCC.2011.6123618.
- [16] N. Sinha, Z. Guo, A. Tazzoli, A. DeHon, and G. Piazza, “1 Volt digital logic circuits realized by stress-resilient ALN parallel dual-beam MEMS relays,” in *2012 IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS)*, 2012, pp. 668–671. DOI: 10.1109/MEMSYS.2012.6170275.
- [17] H. Kam, T. J. K. Liu, V. Stojanović, D. Marković, and E. Alon, “Design, optimization, and scaling of MEM relays for ultra-low-power digital logic,” *IEEE Transactions on Electron Devices*, vol. 58, no. 1, pp. 236–250, 2011, ISSN: 00189383. DOI: 10.1109/TED.2010.2082545.
- [18] C. Qian, “Electro-mechanical devices for ultra-low-power electronics,” PhD thesis, EECS Department, University of California, Berkeley, 2017. [Online]. Available: <http://www2.eecs.berkeley.edu/Pubs/TechRpts/2017/EECS-2017-21.html>.
- [19] C. W.-Z. Low, “Novel processes for modular integration of silicon-germanium MEMS with CMOS electronics,” PhD thesis, EECS Department, University of California, Berkeley, 2007. [Online]. Available: <http://www2.eecs.berkeley.edu/Pubs/TechRpts/2007/EECS-2007-31.html>.
- [20] C. Qian, A. Peschot, I. Chen, Y. Chen, N. Xu, and T.-J. K. Liu, “Effect of body biasing on the energy-delay performance of logic relays,” *IEEE Electron Device Letters*, vol. 36, no. 8, pp. 862–864, 2015. DOI: 10.1109/LED.2015.2441116.

- [21] A. Peschot, C. Qian, D. J. Connelly, and T. K. Liu, "Body-biased operation for improved MEM relay energy efficiency," in *Fourth Berkeley Symposium on Energy Efficient Electronic Systems (E3S)*, 2015, pp. 1–3. DOI: 10.1109/E3S.2015.7336789.
- [22] C. Qian, A. Peschot, D. J. Connelly, and T. K. Liu, "Energy-delay performance optimization of NEM logic relay," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 18.1.1–18.1.4. DOI: 10.1109/IEDM.2015.7409724.
- [23] Y. Yoon, Y. Jin, C. Kim, S. Hong, and J. Yoon, "A low contact resistance 4-terminal MEMS relay: Theoretical analysis, design, and demonstration," *Journal of Microelectromechanical Systems*, vol. 27, no. 3, pp. 497–505, 2018. DOI: 10.1109/JMEMS.2018.2822402.
- [24] K. Tiri and I. Verbauwhede, "Design method for constant power consumption of differential logic circuits," in *Proceedings of the Conference on Design, Automation and Test in Europe - Volume 1*, ser. DATE '05, USA: IEEE Computer Society, 2005, 628633, ISBN: 0769522882. DOI: 10.1109/DATE.2005.113. [Online]. Available: <https://doi.org/10.1109/DATE.2005.113>.
- [25] J. Jeon, L. Hutin, R. Jevtic, N. Liu, Y. Chen, R. Nathanael, W. Kwon, M. Spencer, E. Alon, B. Nikolic, and T.-J. K. Liu, "Multiple-input relay design for more compact implementation of digital logic circuits," *IEEE Electron Device Letters*, vol. 33, pp. 281–283, Feb. 2012. DOI: 10.1109/LED.2011.2177436.
- [26] H. Kam, "MOSFET replacement devices for energy-efficient digital integrated circuits," PhD thesis, EECS Department, University of California, Berkeley, 2009. [Online]. Available: <http://www2.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-182.html>.
- [27] B. Osoba, S. F. Almeida, U. Sikder, Z. A. Ye, X. Hu, T. K. Esatu, and T.-J. K. Liu, "Study of MEM relay contact design and body-bias effects on on-state resistance stability," *Journal of Microelectromechanical Systems*, vol. 29, no. 6, pp. 1531–1536, 2020. DOI: 10.1109/JMEMS.2020.3030886.
- [28] Y. Chen, "Reliability studies of micro-relays for digital logic applications," PhD thesis, EECS Department, University of California, Berkeley, 2017. [Online]. Available: <http://www2.eecs.berkeley.edu/Pubs/TechRpts/2017/EECS-2017-13.html>.
- [29] Y. Chen, R. Nathanael, J. Yaung, L. Hutin, and T.-J. K. Liu, "Reliability of MEM relays for zero leakage logic," in *Reliability, Packaging, Testing, and Characterization of MOEMS/MEMS and Nanodevices XII*, R. Ramesham and H. R. Shea, Eds., International Society for Optics and Photonics, vol. 8614, SPIE, 2013, pp. 20–26. DOI: 10.1117/12.2005719. [Online]. Available: <https://doi.org/10.1117/12.2005719>.
- [30] Y. Chen, R. Nathanael, J. Jeon, J. Yaung, L. Hutin, and T.-J. K. Liu, "Characterization of contact resistance stability in MEM relays with tungsten electrodes," *Journal of Microelectromechanical Systems*, vol. 21, no. 3, pp. 511–513, 2012. DOI: 10.1109/JMEMS.2012.2186282.

- [31] I.-R. Chen, Y. Chen, L. Hutin, V. Pott, R. Nathanael, and T. K. Liu, "Stable ruthenium-contact relay technology for low-power logic," in *Transducers & Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems*, 2013, pp. 896–899. DOI: 10.1109/Transducers.2013.6626912.
- [32] Q. Ma, Q. Tran, T.-K. Chou, J. Heck, H. Bar, R. Kant, and V. Rao, "Metal contact reliability of RF MEMS switches," *Proc. SPIE*, vol. 6463, Jan. 2007. DOI: 10.1117/12.702177.
- [33] S. Lombardo, J. H. Stathis, B. P. Linder, K. L. Pey, F. Palumbo, and C. H. Tung, "Dielectric breakdown mechanisms in gate oxides," *Journal of Applied Physics*, vol. 98, no. 12, 2005, ISSN: 00218979. DOI: 10.1063/1.2147714.
- [34] M. Deloge, "Analysis of ultrathin gate-oxide breakdown mechanisms and applications to antifuse memories fabricated in advanced CMOS processes," *Electronique Lyon, INSA 2011*, PhD thesis, 2011. [Online]. Available: <http://www.theses.fr/2011ISAL0097>.
- [35] Y. Wu, J. Lin, B. Chen, and C. Huang, "Position-dependent nanoscale breakdown characteristics of thin silicon dioxide film subjected to mechanical strain," *IEEE Transactions on Device and Materials Reliability*, vol. 12, no. 1, pp. 158–165, 2012. DOI: 10.1109/TDMR.2011.2179804.
- [36] X. Hu, S. F. Almeida, Z. A. Ye, and T.-J. K. Liu, "Ultra-low-voltage operation of MEM relays for cryogenic logic applications," *International Electron Devices Meeting*, pp. 803–806, 2019, ISSN: 01631918. DOI: 10.1109/IEDM19573.2019.8993629.
- [37] Y. Chen, E. S. Park, I. Chen, L. Hutin, V. Subramanian, and T.-J. K. Liu, "Micro-relay reliability improvement by inkjet-printed microshell encapsulation," in *Transducers & Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems*, 2013, pp. 1974–1977. DOI: 10.1109/Transducers.2013.6627182.
- [38] S. D. Ko, J. Oen Lee, H. H. Yang, M. W. Kim, Y. H. Song, and J. B. Yoon, "An insulating liquid environment for reducing adhesion in a microelectromechanical system," *Applied Physics Letters*, vol. 99, no. 11, pp. 1–4, 2011, ISSN: 00036951. DOI: 10.1063/1.3640228.
- [39] J. Lee, M. Kim, S. Ko, H. Kang, W. Bae, M. Kang, K. Kim, D. Yoo, and J. Yoon, "3-terminal nanoelectromechanical switching device in insulating liquid media for low voltage operation and reliability improvement," in *IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 1–4. DOI: 10.1109/IEDM.2009.5424380.
- [40] C. N. Arutt, M. L. Alles, W. Liao, H. Gong, J. L. Davidson, R. D. Schrimpf, R. A. Reed, R. A. Weller, K. Bolotin, R. Nicholl, T. T. Pham, A. Zettl, D. Qingyang, J. Hu, M. Li, B. W. Alphenaar, J. T. Lin, P. D. Shurva, S. McNamara, K. M. Walsh, P. X. Feng, L. Hutin, T. Ernst, B. D. Homeijer, R. G. Polcawich, R. M. Proie, J. L. Jones, E. R. Glaser, C. D. Cress, and N. Bassiri-Gharb, "The study of radiation effects in

- emerging micro and nano electro mechanical systems (M and NEMs),” *Semiconductor Science and Technology*, vol. 32, no. 1, 2017, ISSN: 13616641. DOI: 10.1088/1361-6641/32/1/013005.
- [41] A. Wilson and D. Sharar, “Temperature-dependent adhesion mechanisms of metal and insulator probe-sample contact pairs,” Jul. 2018. DOI: 10.1109/ITHERM.2018.8419657.
- [42] “Intermolecular and surface forces,” in *Intermolecular and Surface Forces (Third Edition)*, J. N. Israelachvili, Ed., Third Edition, Boston: Academic Press, 2011, ISBN: 978-0-12-391927-4. DOI: <https://doi.org/10.1016/B978-0-12-391927-4.10024-6>. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/B9780123919274100246>.
- [43] T. Liu and C. J. Kim, “Turning a surface superrepellent even to completely wetting liquids,” *Science*, vol. 346, no. 6213, pp. 1096–1100, 2014, ISSN: 10959203. DOI: 10.1126/science.1254787.
- [44] S. Wang, X. Feng, J. Yao, and L. Jiang, “Controlling wettability and photochromism in a dual-responsive tungsten oxide film,” *Angewandte Chemie International Edition*, vol. 118, no. 8, pp. 1286–1289, 2006, ISSN: 0044-8249. DOI: 10.1002/ange.200502061.
- [45] S. Wang, Y. Song, and L. Jiang, “Photoresponsive surfaces with controllable wettability,” *Journal of Photochemistry and Photobiology C: Photochemistry Reviews*, vol. 8, no. 1, pp. 18–29, 2007. DOI: <https://doi.org/10.1016/j.jphotochemrev.2007.03.001>. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S1389556707000287>.
- [46] S. Salahuddin and S. Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” *Nano Letters*, vol. 8, no. 2, pp. 405–410, Feb. 2008. DOI: 10.1021/nl071804g. [Online]. Available: <https://doi.org/10.1021/nl071804g>.
- [47] K. Choe and C. Shin, “Adjusting the operating voltage of an nanoelectromechanical relay using negative capacitance,” *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 5270–5273, 2017. DOI: 10.1109/TED.2017.2756676.
- [48] C. Yoon, G. Choe, and C. Shin, “Energy-delay sensitivity analysis of a nanoelectromechanical relay with the negative capacitance of a ferroelectric capacitor,” *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 365–372, 2020. DOI: 10.1109/JEDS.2020.2983197.
- [49] C. Yoon and C. Shin, “Electrical characteristics of nanoelectromechanical relay with multi-domain HfO<sub>2</sub>-based ferroelectric materials,” *Electronics*, vol. 9, no. 8, pp. 1–12, 2020, ISSN: 20799292. DOI: 10.3390/electronics9081208.
- [50] C. Yoon, J. Min, J. Shin, and C. Shin, “Device design guideline for HfO<sub>2</sub>-based ferroelectric-gated nanoelectromechanical system,” *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 608–613, 2020. DOI: 10.1109/JEDS.2020.3001272.

- [51] S. Senturia, *Microsystem Design*. New York, NY: Kluwer Academic Publishers, 2002, ISBN: 0306476010.