Compact and Efficient Power Electronics System Design for Automotive, Solar, and Aerospace Applications

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Technical Report No. UCB/EECS-2021-88
http://www2.eecs.berkeley.edu/Pubs/TechRpts/2021/EECS-2021-88.html

May 14, 2021

Acknowledgement

I would like to thank my advisor, Professor Robert Pilawa, for his support and guidance through the years. Thank you to the Pilawa group team members for the collaborations and friendships throughout the years. I would also like to thank Profs. Seth Sanders, Duncan Callaway, and Alexandra von Meier for their valuable advice in writing this dissertation. Finally, I would like to thank my family and friends for always staying by me and keeping me motivated through the years.

Compact and Efficient Power Electronics System Design for Automotive, Solar, and Aerospace Applications

by

Derek Chou

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering — Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

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Spring 2021

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Abstract

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In this dissertation, methods of improving overall power electronic system density are developed and explored. Using a Level II single-phase bidirectional electric vehicle charger as a demonstration system, this work focuses on strategies that promote minimization of passive component sizes through the application of different electrical topologies, as well as the mechanical and thermal implications of such applications.

A conventional system design is presented as the baseline for improvement: in a single-phase ac-dc converter system, there exists two major functions that must be performed. First, the input ac current must be shaped to match both the shape and the phase of the input ac voltage, the power factor correction (PFC) function. Second, because the input ac current and voltage multiply and result in a twice-line frequency power pulsation, this pulsation must be managed with an energy buffer. The prototypical conventional system discussed in this work consists of a rectifier followed by a two-switch power converter shaping the input current through a physically-large boost inductor; the power ripple is then buffered by a physically-large electrolytic capacitor bank. Running these functions in reverse provides inverter (dc-ac) functionality, where the rectifier and boost PFC stage is now acting as a rectified sine-wave generator and unfolder inverter stage.

This work proposes the use of the flying-capacitor multilevel (FCML) topology in order to greatly shrink the boost inductor, which is then integrated with the series-stacked buffer (SSB) topology to greatly shrink the buffer capacitors. The FCML topology is verified at Level II charging power levels. In order to achieve the required power level, an interleaved 6-level FCML is designed and built. Mechanical design and thermal management implications are considered in the construction of the FCML prototype, which achieved Level II power levels with a custom-designed air-cooled heatsink prototype. The SSB topology is then added to the system in a full redesign that integrates all of the components into a package with high utilization of 3-D space. Again, the Level II power level necessitated a parallel design,

which we prefer to interleave, so the resultant bidirectional electric vehicle charger design has two FCML stages in parallel as the boost PFC stage as well as two SSB stages in parallel as the energy buffer stage. The system is then verified operational in both the PFC and the inverter modes. In the full system prototype, a power level of 6.1 kW is achieved, running in the dc-ac mode from 400 V_{dc} to 240 V_{ac} and a system density of 201 W/in^3 (12.3 W/cm^3) is reported, which includes the cold plate in a liquid-cooled thermal management system. All of the major power boards in this system are designed to be constructed with commercial parts and conventional manufacturing techniques. Therefore, they are able to be contract-manufactured, yet still achieve excellent power density figures. Finally, an exploration of the boundary condition of converter start-up is performed. The FCML topology can be heavily optimized to utilize switches with ratings lower than the dc bus voltage. This performs well at periodic steady-state, but requires extra circuitry to insulate the switches from excess voltage at start-up. An ac-side start-up technique is implemented and tested, demonstrating a start from a completely discharged state with the converter running in the ac-dc mode.

The hardware prototypes presented herein boast excellent power density figures owing mainly to the heavy degree of mechanical and thermal integration. Both air cooling and liquid cooling solutions are explored, as each have their merits in different electric power systems. Operating at Level II charging power levels, the prototypes in this work did not heat up beyond reasonable commercial part temperature limits. Overall, the FCML and SSB topologies are presented as a strategy to more fully utilize capacitors for their superior energy density as compared to inductors. Mechanical and thermal considerations are factored in at every stage of the design process, which provides more ways to balance the performance of the electrical system with the overall system density.

To my family and friends.

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Acknowledgments

I will start with thanking my advisor, Professor Robert C. N. Pilawa-Podgurski, who accepted me into his group based on perhaps only my acceptance to UIUC, my resume, and a single phone call discussing what the group did and how I could contribute. I made an equally rash decision to move all the way to Illinois from California, which kicked off an amazing journey which appears to have brought me back to California again for the time being – a strange twist of fate as a friend put it. I noticed immediately as I met Robert in person that he manages to give people the advice that they need to make meaningful progress in their studies, yet he also allows for an amazing amount of freedom in the pursuit of the Ph.D. I hadn't touched any serious academic publication writing nor any particularly research-oriented work in the field of power electronics prior to my graduate studies, yet here I am today writing my personal capstone publication in a world-class power electronics research group. Robert has encouraged me to dream big and also achieve big things while I'm at it, and for that and many other things, I am grateful of the time we have spent together.

I would like to thank Professors Seth Sanders, Duncan Callaway, and Alexandra von Meier for being on my committees for higher education and providing valuable guiding advice for the direction of research and the relevance to current events. Thank you to Professor Arijit Banerjee for a jovial time at Illinois and discussions about the power electronics course set as well as general topics of interest.

Thank you to all fellow members of the Pilawa group, past and present: Yutian Lei, Shibin Qin, Christopher Barth, Enver Candan, Andrew Stillwell, Joseph Liu, Pourya Assem, Zitao Liao, Thomas Foulkes, Yizhe Zhang, Nathan Pallo, Tomas Modeer, Nathan Brooks, Pei Han Ng, Samantha Coday, Maggie Blackwell, Rose Abramson, Kelly Fernandez, Joseph Schaadt, Rahul Iyer, Yong-Long Syu, Mads Graungaard, Ting Ge, Nathan Ellis, Raya Mahony, Amanda Jackson, Logan Horowitz, Rod Bayliss III, Yicheng Zhu, Francesca Giardine and many more. My immediate partners in the lab, Zitao and Kelly, have put up with my antics of precision and followed me through the successes and failures of progress. They have oftentimes helped me manage through the darkest times I have experienced. Thank you for the countless hours of hardware, software, and life debugging that we have gone through in the lab, the office, and outside. Thank you to Sam, Maggie, Rose, and Nathan Pallo in lab administrative and social functions, which kept the sanity and atmosphere during tough times. Thank you to my collaborators at the University of Illinois at Urbana-Champaign: Danny Lohan in Prof. James Allison's group, George Popovic, and Tarek Gebrael in Prof. Nenad Miljkovic's group, and the University of Arkansas at Fayetteville: Robert Murphree in Prof. Alan Mantooth's group. Thanks to the different funding sources for making this work possible, including from the Power Optimization of Electro-Thermal Systems (POETS) National Science Foundation Engineering Research Center with support through Toyota, as well as the Advanced Research Projects Agency - Energy (ARPAE), U.S. Department of Energy.

Thank you to the staff at UC Berkeley: Shirley Salanio of the graduate affairs office for always being easy to talk to and ever-present over email. Dennis Lee of the Etcheverry Hall machine shop for the extremely valuable machine shop training and mechanical know-how advice through the years.

And, thank you to two amazing solar vehicle teams at UC Berkeley and UIUC that I have had the privilege of working with throughout my entire undergraduate and graduate careers. The goals of member enrichment in addition to the intense but rewarding design, build, and test cycles have taught me countless skills in both engineering and non-engineering that I have applied to my studies and my life throughout the years. They provided the opportunities for a dizzying amount of travel across the United States and Australia. The names are too numerous to list, though I would give a shout out to a few long-standing members, who have provided "unfiltered technical" advice at the oddest hours of the day (and night!): Richard "Ducky" Lin, Tristan Lall, Jean-Étienne Tremblay, Byron Hopps, Amalia Dungey, Harrison Zheng, Daniel Gay, Devan Lai, Geoffrey Ding, Rami Hijab, and many more.

Certainly, thank you to my parents, Martin Chou and Summer Chen, for their unwavering support throughout this entire journey. Thank you to my sister, Derina Chou, also for your support throughout these years at the most unexpected hours of the day. I could not have done this without you all.

Chapter 1

Introduction

Design of energy delivery systems is becoming an increasingly complex and multi-disciplinary field. In emerging applications such as renewable energy delivery, electric vehicle powertrains and charging, and grid interface systems, the power electronics are becoming more sophisticated and more densely-packed than ever before. This work discusses considerations of such power electronics systems design given the prototypical application of an on-board single-phase ac-dc electric vehicle charger, as well as some techniques for keeping the heat losses manageable in extremely compact packaging. For a typical single-phase ac-dc electric vehicle on-board charger, there are two major energy processing steps: ac-dc rectification, and energy buffering of the twice-line-frequency energy mismatch. This work discusses methods of significantly reducing passive component sizes typical to these converters while maintaining a high efficiency. Furthermore, the implication of co-development of a thermal management system for such a compact converter is explored, as the electrical, mechanical, and thermal aspects heavily influence each other. These techniques are demonstrated in hardware prototypes achieving record power densities including a 7 kW, 400 V_{dc} / 240 V_{ac} single-phase air-cooled inverter / power factor correction (PFC) power stage, and 6 kW, 400 V_{dc} / 240 V_{ac} single-phase liquid-cooled inverter / PFC plus energy buffering system, among others.

1.1 Organization of this Dissertation

This work is organized as follows:

- Chapter 2: Electric Vehicle Charger System Architecture
  An on-board electric vehicle charger is an example power electronic system involving a multitude of interrelated pieces. This chapter presents a prototypical on-board single-phase ac-dc electric vehicle charger system architecture with a focus on the electrical system. Since the system may be run in reverse (dc-ac) as an inverter, the bidirectional nature of such a design is also discussed. A single-phase ac-dc rectifier or dc-ac inverter is comprised of two major stages: the power-processing power factor correc-

tion or inverter stage, and the energy buffering stage. A solution is proposed using a conventional design.

- Chapter 3: Theory of Improving Power Density of Power Electronic Systems
  The conventional design presented in the previous chapter has the major shortfall of possibly requiring the usage of physically large passive components for filtering purposes. Overarching concepts of improving power density in power electronic systems are introduced and discussed in this chapter. Recurring themes of improved passive component utilization and minimization are discussed. The general architecture of the flying capacitor multilevel (FCML) converter is introduced, as is the series-stacked buffer (SSB). A high power density approach to building a single-phase ac-dc rectifier or dc-ac inverter system is proposed.

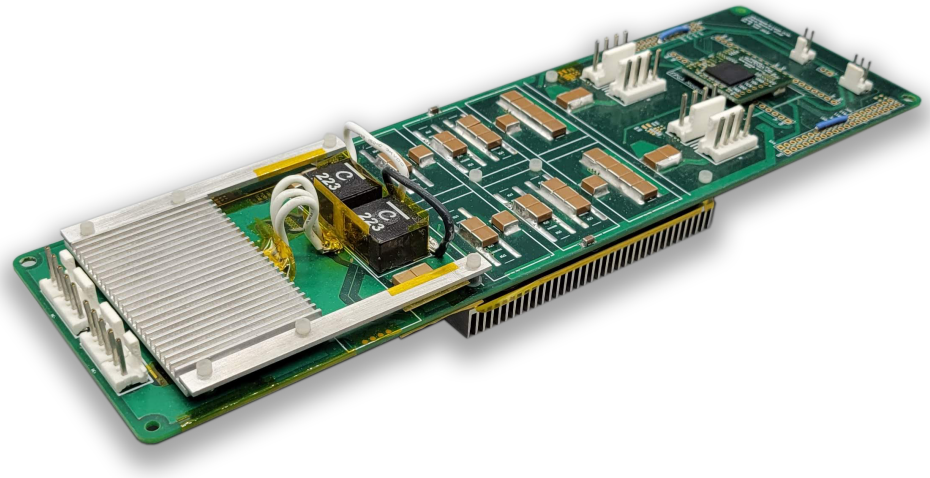

Figure 1.1: High power density 7 kW dual-interleaved 6-level FCML inverter / rectifier hardware prototype.

- Chapter 4: Validation of the Power Stage
  In this chapter [1], the electrical architecture and hardware of the inverter (dc-ac) or rectifier (ac-dc) power processing stage is verified at high power. A dual-interleaved 6-level GaN multilevel converter is designed and built to achieve extreme power density figures, and thermal considerations for such a converter are discussed. A custom-milled heatsink prototype is designed, built, and tested with this hardware prototype. The prototype built (Fig. 1.1) achieves a power level of 7 kW, and an efficiency exceeding 98% throughout most of its power output range, well within the Level II charging power range. The power stage achieves a volumetric power density figure of 785 W/in^3 (47.9 W/cm^3), which exceeds previous research demonstrations of power stage density by 2× [2], [3].

- Chapter 5: Electric Vehicle Charger System Design
  In this chapter [4], [5], the system architecture of the electric vehicle charger is integrated into a single design. Prior work on the power stage of Chapter 4 as well as a series-stacked energy buffer are combined into an electric vehicle charger system design. Design of this charger involves electrical, mechanical, and thermal considerations which influence each other. Therefore, all of the above factors were considered at every point of the design in an attempt to produce a more-optimal system power density, with the explicit knowledge that the design would not pursue the most extreme electrical efficiency, mechanical packaging, or thermal performance, but rather a harmonious combination of the three.

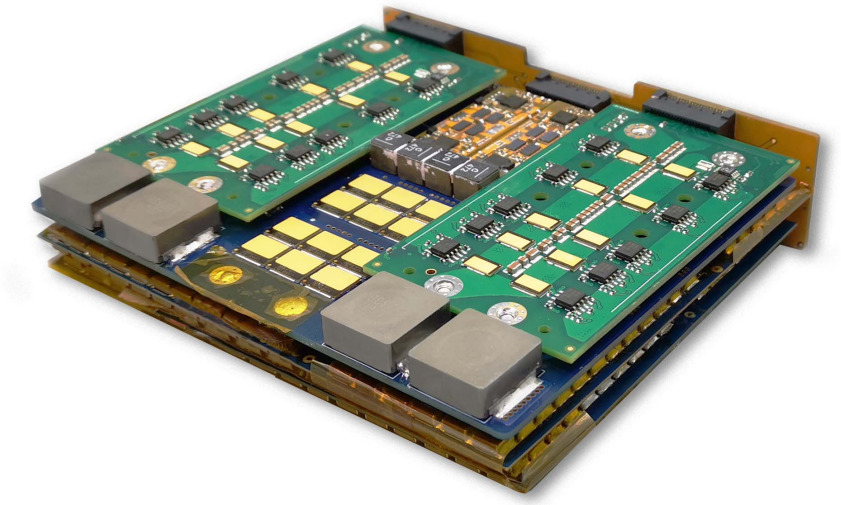

Figure 1.2: Electrical portion of the high power density electric vehicle charger system prototype incorporating dual-interleaved 6-level FCML modules, dual-interleaved series-stacked buffer modules, and unfolder / rectifier. (Image created in collaboration with Zitao Liao.)

- Chapter 6: Validation of the Electric Vehicle Charger System
  The electric vehicle charger system (Fig. 1.2) is constructed and validated in ac-dc PFC mode, as well as dc-ac inverter mode [4], [5]. A maximum power level of 6.1 kW is tested, well within the Level II charging power range. A custom-manufactured cold plate is used as the main thermal management system, which is verified along with the dual-interleaved FCML and dual-interleaved series-stacked energy buffer stage assemblies. The PCB assemblies are all designed to be compatible with conventional manufacturing techniques, thus improving the practicality overall. A system power density of 201 W/in^3 (12.3 W/cm^3) is reported. This density figure exceeds the industrial state-of-the-art by an order of magnitude, and matches leading research figures

while employing conventional manufacturing and assembly techniques in the bulk of the system [6]–[12].

- Chapter 7: On the Exploration of Converter Start-up
  Transient situations are of interest in a flying-capacitor multilevel converter due to its reliance on capacitor balancing. Depending on the design margin, capacitor balancing can be critical to proper converter behavior. For a highly-optimized FCML converter, the maximum operating bus voltages often exceed the switch voltage ratings, so the system relies on good capacitor voltage balancing to keep all of the core power semiconductors operating within these ratings. In this chapter, a start-up sequence for the electric vehicle system is proposed and explored. The addition of a pair of semiconductor switches and some filtering elements (Fig. 1.3) creates a voltage and current limiting structure not unlike a four-switch buck-boost converter, which is used to limit the voltage across the FCML converter switches during a start-up sequence.

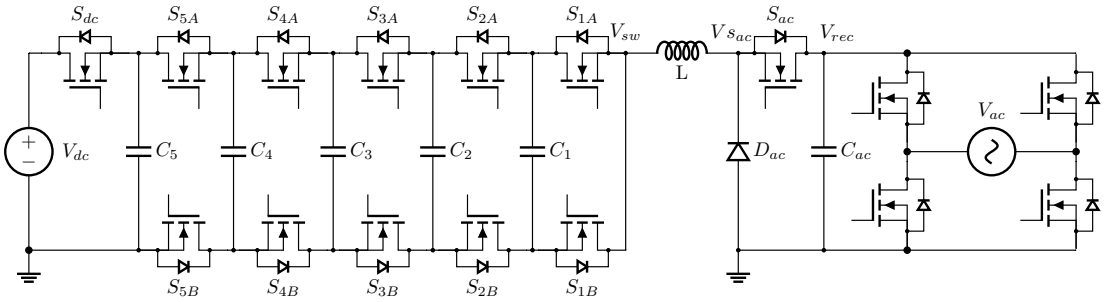

Figure 1.3: 6-level FCML and unfolder / rectifier schematic with added start-up switches and supporting circuitry.

- Chapter 8: Conclusions
  This chapter concludes this work and comments on the future direction of this research.

Chapter 2

Electric Vehicle Charger System Architecture

Electric vehicles have become an increasingly popular and feasible alternative to conventional gas-powered vehicles in the past decade. However, battery electric vehicles continue to face such challenges as range anxiety, long charging times, and public perception of safety. Improving such metrics would require infrastructure upgrades, improved charging architecture for increased charging rate, and improved energy density in the batteries themselves [13]. A conventional gasoline-powered automobile requires only minutes to refuel fully, while an electric vehicle would require hours to recharge fully [14]–[17]. Therefore, along with improving battery capacity and charging rate capabilities of the physical battery itself, it is desirable for electric vehicle chargers to handle higher charging power levels, to minimize battery charge times. This must be balanced with keeping charging hardware volume and weight to a minimum, as such energy conversion systems interfacing between grid ac and battery dc voltages are carried on-board for Level I or Level II charging power levels. Electric vehicle batteries may additionally be viewed as a mobile battery backup source for the grid, meaning that bi-directional operational capabilities are desirable to include in such an on-board system [14], [17], [18].

An on-board single-phase ac-dc electric vehicle charger is used as the prototypical power electronic system for this work. This work explores the implications and methods of improving power density in power electronic systems, taking a holistic approach which considers electrical, mechanical, and thermal aspects.

In this chapter, the high-level electrical architecture of an on-board charger is presented and discussed. The design of such converters can allow for bidirectional operation, so both the ac-dc rectifier and dc-ac inverter functionality is discussed. A conventional solution to the ac-dc or dc-ac conversion problem is presented.

2.1 Single-Phase ac-dc Rectifier and dc-ac Inverter Fundamentals

Given a single-phase ac grid-interfaced system that is connected to a dc battery (Figs. 2.1 and 2.2), we can define the grid voltage and grid current as sinusoidal functions, which then multiply together to form an ac power function:

$$V_{ac} \propto sin(\omega t) \tag{2.1}$$

$$I_{ac} \propto sin(\omega t) \tag{2.2}$$

$$P_{ac} = V_{ac} \cdot I_{ac} \propto sin^2(\omega t) = \frac{1}{2} - \frac{cos(2\omega t)}{2} \tag{2.3}$$

In steady-state conditions, the dc power is approximately constant. Therefore, the ac and dc power will almost always be mismatched except for singular points along the line cycle. Given the above, a single-phase grid-tied system charging a dc battery must perform two major functions:

- Provide power factor correction (PFC) support to keep grid voltage and current similarly-shaped and in-phase with each other in accordance with regulatory standards on total harmonic distortion that is experienced by the grid side of the converter.
- Provide energy buffering to mitigate the 120 Hz (twice-line frequency, ω) energy ripple that occurs as a natural result of ac-dc or dc-ac conversion.

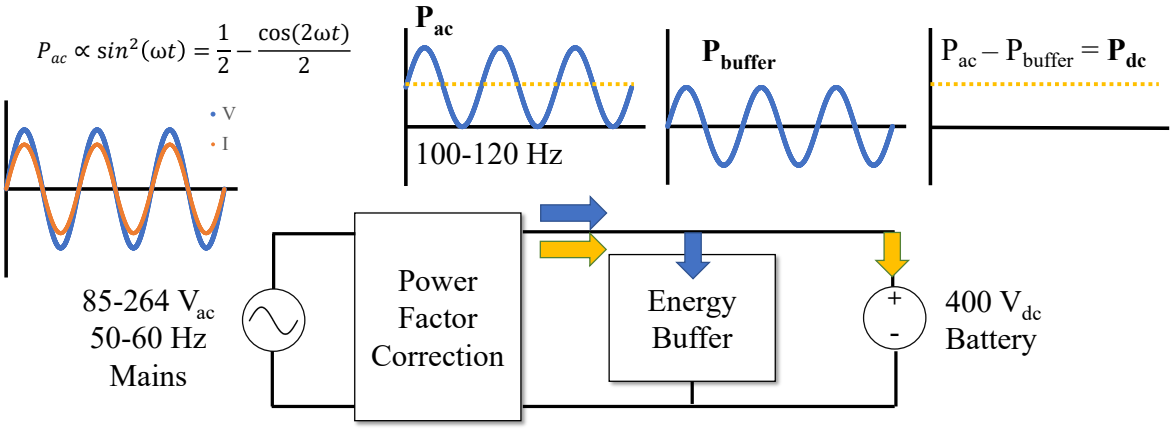

Figure 2.1: System architecture diagram detailing a single-phase ac-dc rectifier.

In a rectifier system (Fig. 2.1), the power factor correction stage shapes the current waveform of the input ac to be sinusoidal and in phase with the ac voltage. The energy

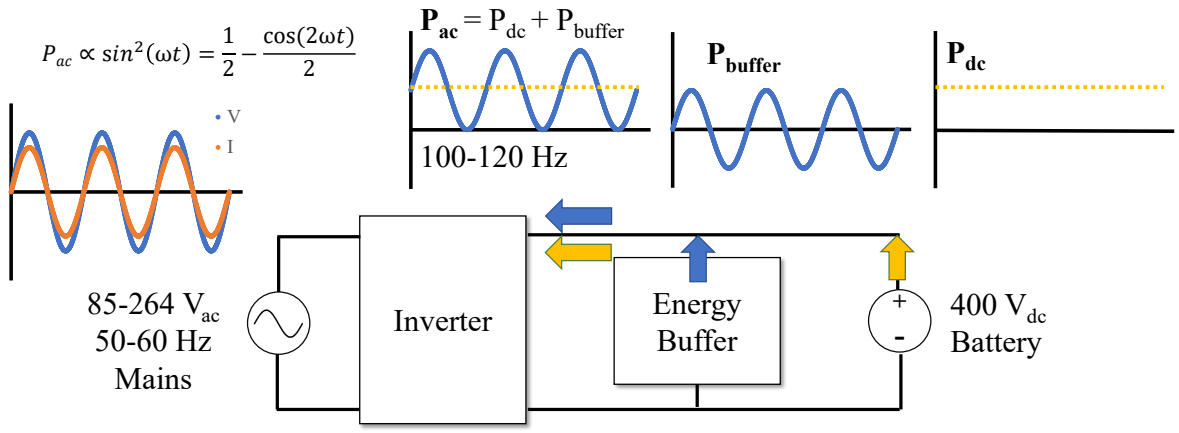

Figure 2.2: System architecture diagram detailing a single-phase dc-ac inverter.

buffer power, P_{buf} is subtracted from the ac power, P_{ac}, which ideally cancels out the twice-line frequency ripple of the ac power, to produce a constant dc power, P_{dc}.

In an inverter system (Fig. 2.2), the dc source provides a constant power, P_{dc}, which is then added to the energy buffer power, P_{buf}; this is run through an inverter stage which is synchronized with the grid ac voltage, pushing electric current at high power factor, P_{ac}.

2.2 Conventional Design of Single-Phase ac-dc and dc-ac Converter Systems

A conventional solution to constructing the system presented in Figs. 2.1 and 2.2 is shown in Fig. 2.3.

It consists of an ac full-bridge rectifier or unfolder stage connected to a boost PFC stage, the output of which is buffered with a large DC-link capacitor to smooth the ac power ripple. The two major functionalities of the above-discussed rectifier or inverter system are implemented here.

In the rectifier mode:

- The full-bridge rectifier stage is connected to a boost power factor correction stage, which provides the ac power processing capability.
- The energy buffer is a bank of dc-link capacitors, which smooths out the energy ripple to provide approximately dc power.

In the inverter mode:

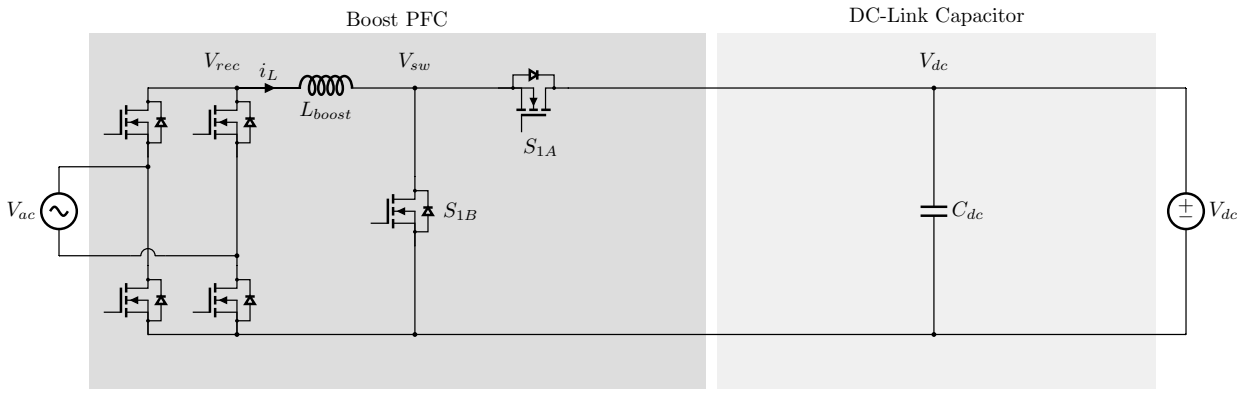

Figure 2.3: Conventional single-phase ac-dc rectifier or dc-ac inverter. Bidirectional capability is contingent on the usage of active switching devices.

- The boost PFC stage is run in reverse as a buck stage, to produce a rectified sine waveform, which is then fed to the full-bridge stage running in reverse as an unfolder stage, which produces a full sine waveform. This provides the ac power back to the grid.
- The energy buffer, the bank of dc-link capacitors, compensates for any power mismatch between the dc and ac sides.

Chapter 3

Theory of Improving Power Density of Power Electronic Systems

Major drawbacks to a conventional ac-dc or dc-ac system design such as the one presented in Chapter 2 include the relatively large passive component elements required to provide satisfactory power factor and dc voltage ripple filtering. The boost inductor of the boost PFC stage and the dc-link capacitor are commonly physically the largest elements in such a design.

This chapter discusses the fundamental principles dictating the physical size of converter systems. The energy storage capability of inductors and capacitors are discussed, and a proposed high power density solution is explained in two parts. The first, the flying-capacitor multilevel converter power stage, is implemented to reduce the boost inductor size [19], [20]. The second, the series-stacked buffer [21]–[23], is used to reduce the energy buffer capacitor size.

3.1 Energy Storage Density of Passive Components

Power converters leverage the usage of switches and temporary energy storage in capacitors and inductors to convert energy efficiently. In a conventional two-level buck converter design, this is commonly achieved with the usage of MOSFETs as the blocking switch elements, a large filter inductor as magnetic energy storage, and capacitors as the ripple filter elements. The drawbacks to such a design are apparent in the relatively large size of the magnetic element: since the inductor has a significantly lower energy storage density than that of capacitors, it tends towards being one of the largest physical elements in these designs [24]. For example, on a boost power factor correction stage, the boost inductor is larger than all of the power devices combined. Noted from the energy storage capability of inductors:

$$\Delta E \propto L \cdot (\Delta I)^2 \tag{3.1}$$

To realize a high energy storage usage, either a large current ripple must be allowed (and then filtered), or a large inductance value must be used. Since larger inductance values tend

to result in larger physical devices, the two above factors are frequently traded off with each other, as well as with the filter capacitor sizing, to obtain an optimal system design.

In a capacitor energy buffer implementation for single-phase ac-dc converters, a conventional solution is to use a bank of electrolytic capacitors. Capacitors have superior energy density compared to inductors [24], but the energy utilization percentage is poor as they are often limited by external constraints defining voltage and current ripple figures. The energy buffering capability that a capacitor bank can source is noted:

$$\Delta E \propto C \cdot (\Delta V)^2 \tag{3.2}$$

In an electrolytic capacitor energy buffer implementation, ΔV is commonly a small percent of the dc bus voltage, superimposed on top of a comparatively large dc bias. ΔV is commonly externally defined in the single-digit percent values, which drives up the required buffer capacitance value. The dc bias, $\frac{1}{2} \cdot C \cdot V_{bias}^2$, can be considered as unused potential buffering capability, as it does not change and therefore does not contribute to energy buffering in the system it is used in. This is further limited by the relatively high equivalent series resistance of electrolytic capacitors, which limits the available electric current buffering capability. Different capacitor technologies, such as film and ceramic capacitors, may be used to improve electric current buffering capability, but these technologies are not as volume- or cost-efficient as electrolytic capacitors.

This work aims to improve the power density of these implementations of energy conversion and buffering for a single-phase ac-dc converter system by utilizing the flying-capacitor multilevel converter in conjunction with the series-stacked energy buffer.

3.2 Flying Capacitor Multilevel Converter

The flying-capacitor multilevel converter (FCML) [19] is a well-explored converter topology with a high potential for dramatically reducing passive component volume and weight. This has been demonstrated in inverter [10], [25] and PFC applications [26], [27]. It takes advantage of the high energy density of capacitors when compared to inductors, [24] as the use of high energy density ceramic capacitors and reduced voltage stress on inductors can reduce the overall inductor size by a factor of $(N-1)^2$, where N is the number of levels in the FCML. An N-level FCML is shown in figure 3.1. Note that the converter topology lends itself to a highly modular design, as the switches and capacitors are arranged in repeating units. Not only does this allow for possibly improved design and manufacturing techniques, it also allows for losses to be spread out across the entire set of power devices, rather than concentrating all of the losses into two devices like a conventional two-level converter would. Thus, a high power processing capability can be realized even if the overall converter volume is reduced, as the heat loss density can be managed with this topology.

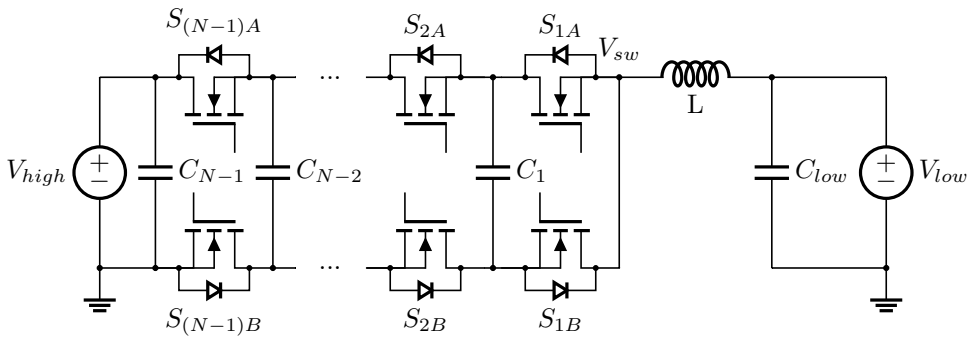

Figure 3.1: N-level FCML schematic.

3.3 Series-Stacked Buffer

The series-stacked buffer topology [21], [28]–[30] is considered as a remedy to the low energy utilization of the electrolytic dc-link capacitor bank. It is implemented to mimic the behavior of a notch filter at the line frequency, but again uses capacitors as the main energy storage element.

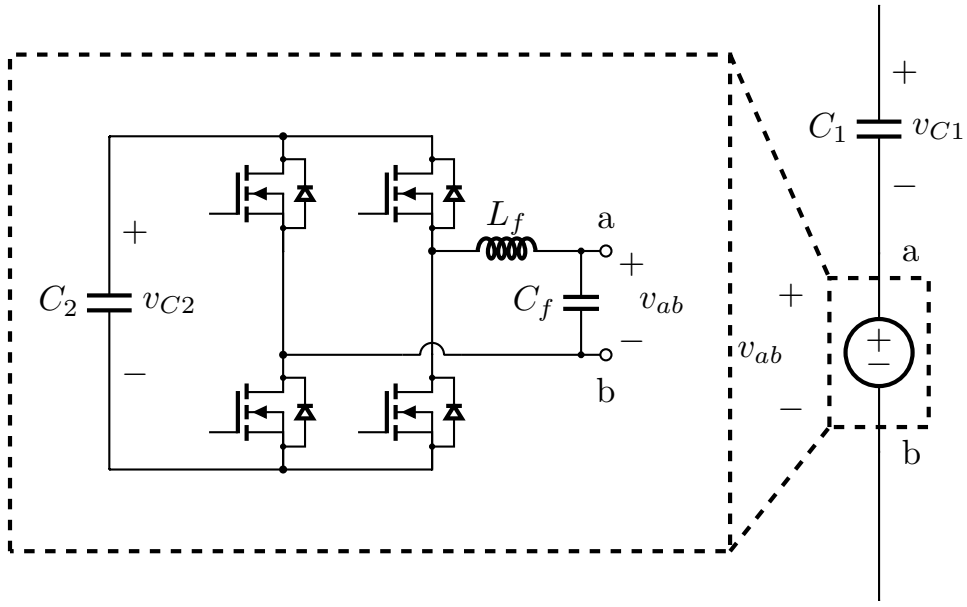

Figure 3.2: Series-stacked buffer (SSB) topology for buffering twice-line frequency ripple in single-phase ac-dc and dc-ac systems.

Fig. 3.2 shows an implementation of the series-stacked buffer topology. Capacitor C_1

is allowed to ripple at a much higher ΔV than would normally be allowed for a dc-link capacitor. This ripple is exactly canceled with voltage v_{ab}, which is generated by a full-bridge converter from a voltage source, in this case C_2. This entire structure is controlled to approximate an RLC circuit, which draws real power into the circuit to prevent the voltage across C_2 from decaying [21]. The increased voltage ripple across C_1 allows for the buffer dc-link capacitor to be greatly reduced in size, with the tradeoffs of needing to construct a converter to store and utilize the energy on C_2, as well as the physical size of C_2 itself.

3.4 Proposed Design of High Power Density ac-dc Rectifier / dc-ac Inverter Stage

A system architecture featuring the flying-capacitor multilevel (FCML) converter as the inverter or power factor correction (PFC) stage, and a series-stacked buffer (SSB) as the energy buffer stage, is used to improve gravimetric and volumetric power density as compared to conventional designs, as shown in Fig 3.3. A previous hardware demonstration of such a combination of the two topologies is presented in [10]. This work aims to improve upon the previous art by improving the manufacturability of system elements, increasing the maximum power level to Level II electric vehicle charger levels, and enhancing the integration of electrical, mechanical, and thermal aspects.

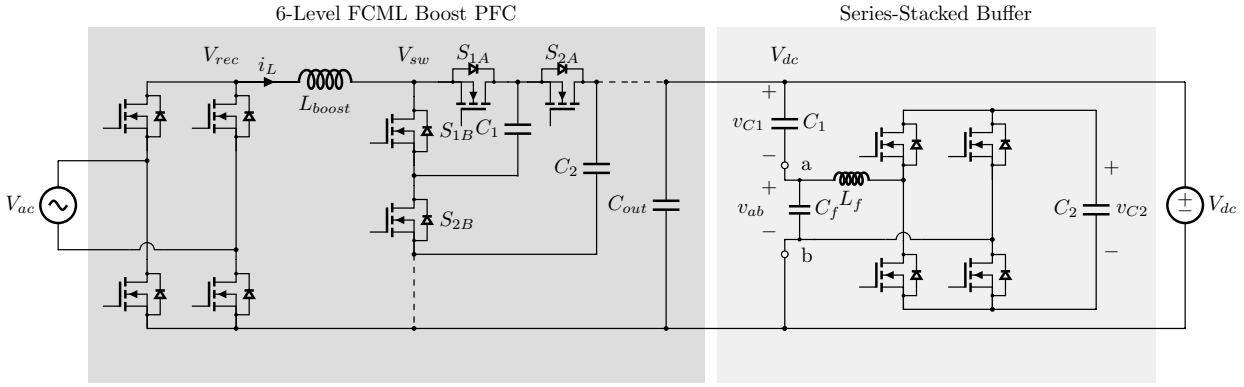

Figure 3.3: Proposed high power density single-phase ac-dc rectifier or dc-ac inverter

The above system topology allows for significantly higher power density because of the higher utilization of capacitors for energy transfer. In the FCML stage, the capacitors are used to hold a dc bias, which allows for lower-voltage semiconductor switches to be used. Since lower-voltage rated semiconductor switches can potentially have a higher figure-of-merit (defined as gate charge Q_g multiplied by the on-state resistance $R_{ds,on}$), the efficiency of such a converter could potentially be improved. Furthermore, compared to a conventional two-level boost PFC, the FCML topology has the benefit of dividing the total losses of

the switching elements into potentially many different elements, which can simplify thermal management.

In the SSB stage, the capacitor C_1 is allowed to ripple at a ΔV larger than would be allowed for a bank of dc-link electrolytic capacitors; this ripple is canceled with a waveform generated at v_{ab} with the full-bridge converter structure.

Previous industrial and research applications of both the inverter power stage as well as the integrated inverter plus energy buffer yield a comparison point for this work: State-of-the-art industrial designs [6]–[9], [11] achieve densities of up to about 10-50 W/in^3 (0.61-3.1 W/cm^3) for system density, while state-of-the-art research designs [10], [12] are achieving 80-250 W/in^3 (4.9-15.3 W/cm^3) with highly-specialized production and assembly techniques. If considering the power stage alone, research designs [2], [3], [31] appear to achieve up to 200-375 W/in^3 (12.2-22.9 W/cm^3) of power stage density.

3.5 Mechanical and Thermal Integration

Often cited as an addendum to conventional designs, mechanical and thermal integration of power electronic systems are becoming increasingly important at earlier stages of the design process [10], [32], [33]. In this work, the overall assembly maximizes the utilization of the 3-D space with a low-profile and modular design philosophy, enabled by the use of high energy density ceramic capacitors and the reduced inductor size in both FCML and SSB stages. The heat-generating components are placed in groups to allow for simple thermal circuit routing and higher thermal efficiency for automotive cooling systems. Overall, this work aims to achieve the state-of-the-art research design power densities while keeping provisions for the usage of more-conventional techniques of manufacturing and assembly.

Chapter 4

Validation of the Power Stage

This chapter discusses the design and implementation of a high power density Level II charger power stage converting between 400 V_{dc} and 240 V_{ac}, utilizing two interleaved flying-capacitor multilevel converter stages combined with a full H-bridge unfolder or active rectifier. The focus of this chapter is the ac-dc/dc-ac power stage, with the goal of a combined high efficiency and power density. Thus, power factor correction (PFC) control and twice-line-frequency buffering are not discussed or implemented in this chapter. Experimental results show a peak system efficiency of greater than 98.9%, a power output of 7 kW, and an effective switching frequency at the inductor switch nodes of 720 kHz.

4.1 Introduction

Conventional approaches to constructing the ac–dc stage for power conversion between grid ac and battery dc voltages encounter the problem of requiring large filter inductors and capacitors for energy buffering. A possible solution to this involves increasing the switching frequency of the active devices in the converter to reduce passive component sizes, but this reduces overall system efficiency and increases thermal management requirements. The bridgeless PFC topology [34], and converter interleaving [35] are examples of optimizations which reduce conduction path losses, but they still require the usage of high-frequency high-voltage blocking switches. Reducing the maximum power design specification can reduce the passive component sizes, but will increase the charging time requirement.

It has been shown that the flying capacitor multilevel (FCML) topology [19], [20], [36], [37] has the potential to dramatically reduce passive component volume and weight in inverter [10], [25] and PFC applications [26], [27], [38], [39]. The characteristic frequency multiplication and voltage division effects of the FCML topology allow for the usage of lower-voltage switching devices as well as smaller magnetic components. By leveraging the higher energy density of capacitors, the FCML topology has been shown to improve the power density of such converters by over an order of magnitude from the industrial state-of-the-art. This chapter aims to improve gravimetric and volumetric power density figures of

a Level II bidirectional electric vehicle charger ac-dc/dc-ac power stage. We note here that for single-phase ac-dc converters, twice-line frequency energy buffering is another important consideration, but is not the focus of this chapter, as it is discussed in the following chapters (5 and 6). Likewise, power factor correction (PFC) control, grid synchronization, and other high-level control considerations are not addressed in this chapter as they are also discussed in the following chapters (5 and 6). SAE J1772 standards describe Level II charging as less than 80 amperes of current at a standard 208 V or 240 V single-phase ac voltage, representing a maximum power of 19.2 kW [40]. However, since many of these chargers are designed to plug into household dryer outlets, the realistic current limit is lower, between 15–30 A, which represents a power level between 3.1–7.2 kW [41]. Table 4.1 details sample design criteria generated for the purposes of this system platform design.

Table 4.1: Level II charger design specifications.

Parameter	Notes	Value
DC Voltage	Nominal	400 V_{dc}
AC Voltage	Nominal	240 V_{ac}
Power Processed	Max	6.6 kW
Ambient Temperature	Max	60 °C
Physical Location		Under passenger seat

The key contributions of this chapter [1] are the combination of the converter topology, logic supply and gate drive, and heatsinking of the FCML and inverter devices.

The remainder of this chapter is organized as follows: Section 4.2 presents the overall system topology design and operational principles. Section 4.3 describes the hardware design and implementation of the system described in the previous section and Section 4.4 discusses experimental results obtained from the hardware prototype. Section 4.5 provides concluding remarks.

4.2 Principles of Operation

The hardware platform presented in this work is an interleaved implementation of the FCML converter topology, connected to a full H-bridge active rectifier or unfolder stage. Figure 4.1 is a schematic drawing of the core power conversion stage design. To operate the system as an inverter, the FCML dc–dc converter stage generates a rectified sine wave, which is then converted to a full sine wave by the full H-bridge unfolder. The interleaving operation of the FCML converter portion reduces voltage ripple at the rectified sine wave node, V_{rec}. To operate the system as a rectifier, the H-bridge acts as an active rectifier, and the FCML dc–dc conversion stage steps up the rectified sine wave voltage to the dc bus voltage.

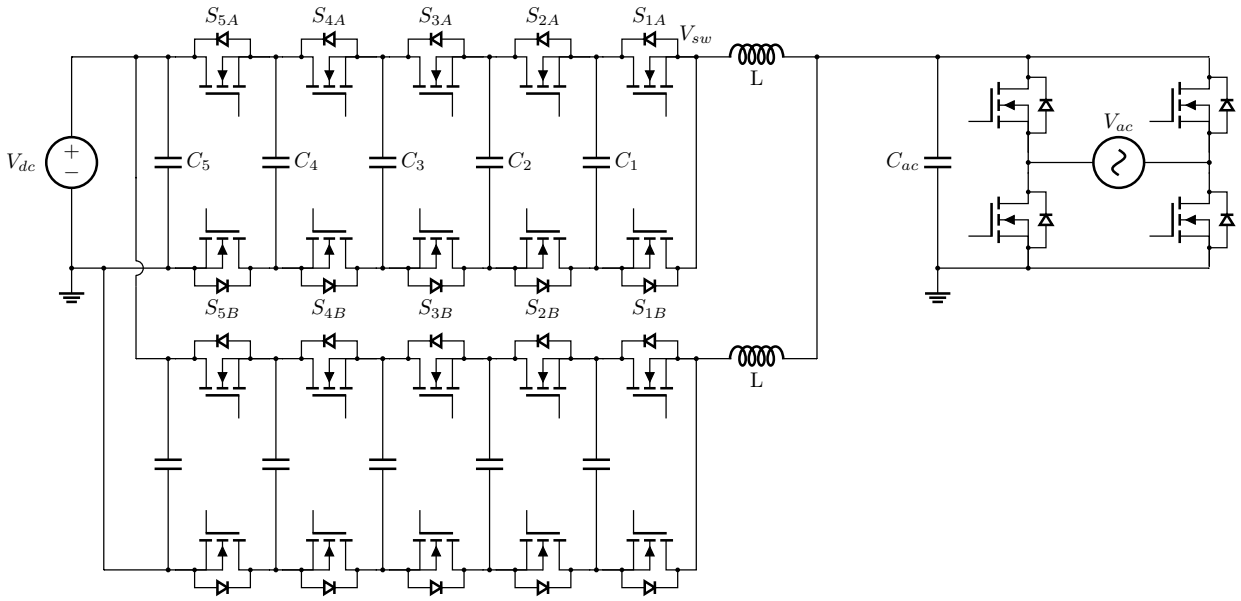

Figure 4.1: Schematic drawing of the bidirectional ac-dc converter, comprising dual interleaved 6-level flying capacitor multi-level stages, along with a single active rectifier/unfolder stage.

Multilevel DC-DC Conversion

The flying capacitor multilevel topology uses a combination of capacitors and inductors to transfer energy. A major advantage of this topology that is leveraged in this work is its ability to generate high effective switching frequency waveforms at the filter inductor switch-node (V_{sw}, Fig. 4.1). Detailed operational principles for the FCML converter topology can be found in [19], [10], and [42].

The hardware platform presented in this work consists of two interleaved 6-level FCML stages, phase-shifted 180 degrees with respect to each other to reduce current ripple the rectified sine wave node, V_{rec}. To illustrate the operation of a single FCML power stage, switching signals and voltage nodes of interest are shown in Fig. 4.2, for an example single 6-level FCML converter operating at 70% duty ratio. Switch control and capacitor balancing are achieved through usage of the phase-shifted PWM (PSPWM) method, which are described in more detail in [19], [43] and [44]. The 6-level topology was chosen for its inherent natural capacitor voltage balancing effect [45]. Of note is the frequency multiplication effect inherent to the FCML topology, where the frequency, f_{ind}, seen by the inductor switch-node, V_{sw}, is:

$$f_{ind} = f_{sw} \cdot (N - 1) \tag{4.1}$$

where N is the number of voltage levels in the FCML converter and f_{sw} is the individual switch switching frequency. In a 6-level FCML converter, the frequency seen by the inductor

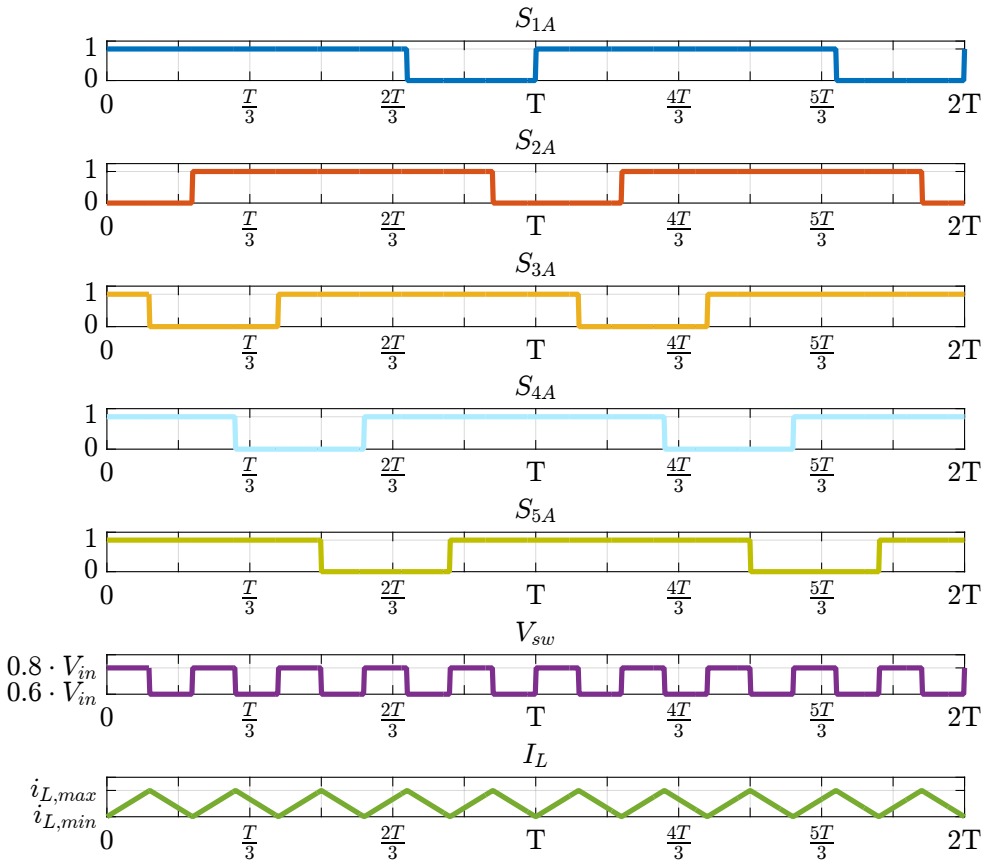

Figure 4.2: 6-level FCML control waveforms

is 5× the base switching frequency. Moreover, the inductors experience a maximum ripple voltage of the smallest voltage across the flying capacitors, $V_{DC}/(N-1)$. This results in an overall $(N-1)^2$ reduction in filtering inductor size, as compared to a conventional two-switch non-isolated converter design ($N = 2$) [46]. For a 6-level FCML converter, this is roughly a 25× decrease in the filter inductor size requirement for the same base switching frequency.

As noted, switching signals for each of the FCML stages are phase-shifted by 180 degrees. Therefore, the ac portions of the output current waveforms of the two inductors in the system partially (or fully, for certain duty ratios) cancel, resulting in a current waveform with very low ripple at the rectified sine wave node (V_{rec}, Fig. 4.1). Even though the interleaved stages may not be perfectly matched for current sharing, since they are constructed with the same components, the benefits of lower current ripple due to interleaved operation are still generally achieved. In this work, only the effects of natural current sharing between stages are explored; interleaved stage balancing, load shedding at light-load operating points, and other more advanced techniques may be implemented in software but are not explored further.

The FCML topology utilizes capacitors to block dc voltages, and the switches see only a fraction of the input voltage:

$$V_{switch} = \frac{V_{dc}}{N-1} \tag{4.2}$$

Since lower-voltage switching devices tend to have a more favorable figure of merit, defined as the product of gate charge by on-state resistance, the overall efficiency of the system can be improved through selection of such devices. The combination of frequency multiplication effects and increased design space for switching devices allows for some design versatility: the more-favorable figure-of-merit may be leveraged in the way of extreme reduction of filtering capacitors and inductors through high-frequency switching [47], or it may be optimized to provide a balance between switching and conduction losses. In this work, EPC2033 GaN devices are selected for usage in the FCML stage to provide a balance between switching and conduction losses, taking into account the somewhat increased conduction losses due to dynamic on-state resistance [48], [49].

4.3 Hardware Design and Implementation

The hardware prototype has been designed, constructed and tested, using the guidelines set forth in Table 4.1. Figure 4.3 shows annotated photographs of the converter as built, including the control, interleaved FCML, and active rectifier / unfolder stages, as well as of the converter with heatsinks attached. Table 4.2 provides a listing of the major components used in the converter prototype.

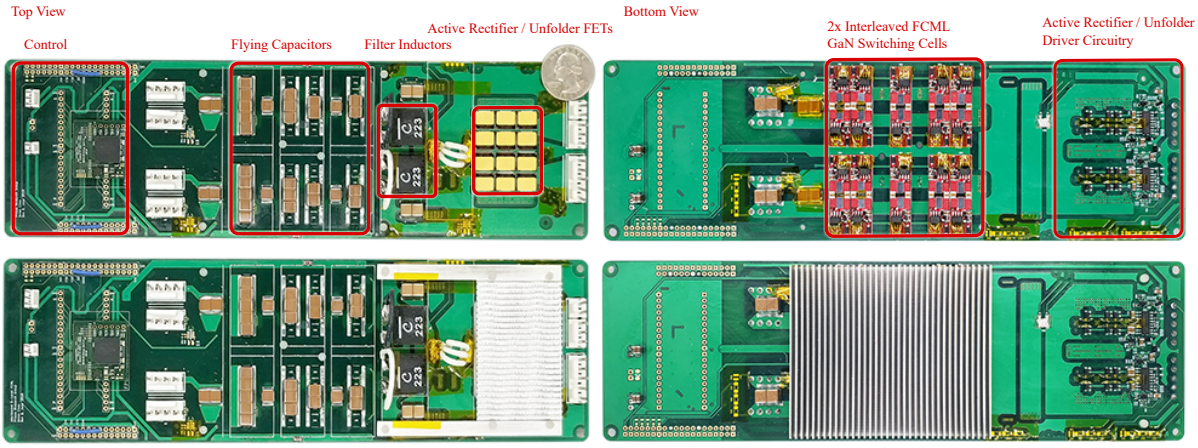

Figure 4.3: Converter prototype photographs, with and without heatsinks.

The main power devices in the FCML stage are EPC 2033 GaN FETs, driven by Silicon Labs Si8271 single-channel isolated gate drivers. To address the challenge of supplying a floating gate drive voltage to each GaN FET, several solutions may be used. In this

Table 4.2: Component listing

Component	Part No.	Parameters
Interleaved 6-Level FCML		
GaN FETs	EPC 2033	150 V, 7 $m\Omega$
Isolated Gate Drivers	Si8271GB-IS	Silicon Labs Si827x Series
Flying Capacitors	TDK C5750X6S225K250KA	2.2 μF × 2–5 (parallel, $\sim 2.6\mu$F effective)
Inductors	Coilcraft XAL1510-223	22 μH (2 total; 1 per phase)
Active Rectifier / Unfolder		
GaN FETs	GaN Systems GS66516T	650 V, 25 $m\Omega\times$ 3 (parallel)
Isolated Gate Drivers	Si8274GB1-IS1	Silicon Labs Si827x Series
Control		
FPGA	Altera 10M16SCU169C8G	MAX10 Series

work, individual gate drive power supplies are achieved through cascaded bootstrap stages with low-dropout (LDO) regulators attached to each bootstrap capacitor to provide a stable drive voltage to each FET (Fig. 4.4). Reverse conduction of the GaN devices can cause the bootstrap capacitors to be charged to a voltage higher than the input logic voltage. An electrostatic discharge (ESD) protection diode rated for 12 V standoff voltage and 13.5 V breakdown voltage is placed in parallel with the bootstrap capacitors of each stage, to protect the LDOs from any overvoltage conditions during higher-current operations of the converter. To ensure that the highest-side FET gets at least 5 V of gate drive voltage, the lowest-side gate driver bootstrap capacitor is fed 12 V of gate drive voltage, which is then regulated down to the 5 V gate drive voltage through an LDO. For each cascaded bootstrap stage, there is a small diode drop from the bootstrap diode, resulting in a voltage of about 6.1 V at the highest-side bootstrap capacitor. The method outlined here achieves a 40+% gate drive supply efficiency, which outperforms a similar solution using small isolated dc-dc converters, the ADuM5010, which would achieve less than 27% gate drive supply efficiency [50]. Reducing the gate drive voltage margin, or using small step-down switching converters can improve the gate drive supply efficiency, but is not explored further in this work. Reference [50] provides more information regarding a multitude of possible solutions to providing the necessary floating supplies for each gate driver.

The step-up / step-down conversion of the ac-dc / dc-ac stage is accomplished with two parallel 6-level FCML converters, using interleaved switching signals to reduce ripple at the converter rectified sine wave node, V_{rec}. In the FCML converter topology, there are many repeating switch pairs. Therefore, to streamline construction, the supplementary circuitry for each switch is built on a GaN "switching cell" daughterboard. As shown in Fig. 4.4, each "switching cell" consists of an EPC 2033 GaN device, a Silicon Labs Si8271 isolated gate driver, an LDO, bootstrap capacitors, a transient voltage suppression (TVS) diode, a bootstrap diode, and all supporting passive components for filtering and bypass. This

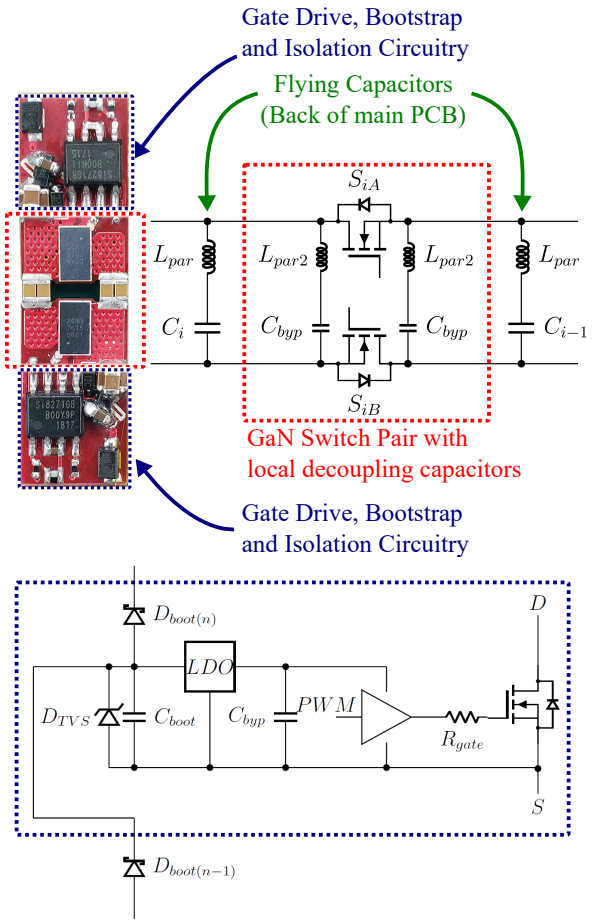

Figure 4.4: Top: Switching cell daughterboard pair design.
Bottom: Switching cell daughterboard schematics.

has the advantage of breaking up a large converter into a construction of many smaller switching units, with the additional benefit of reducing parasitic ringing effects through the local bypass capacitors. These smaller capacitors are connected in parallel with the larger flying capacitors on the opposite side of the larger circuit board. The parasitic inductances associated with the current commutation loops of the various components are highlighted in Fig. 4.4. Here, L_{par2} represents the inductance associated with the current commutation loop between the two GaN devices and the local decoupling capacitors, and L_{par} represents the inductance of commutation loop involving the larger flying capacitors on the backside of the PCB. Since the local bypass capacitors are physically very close to the switch pairs, the value of L_{par2} is less than L_{par}, reducing switch voltage overshoot during commutation [10], [25].

In the active rectifier / unfolder H-bridge stage, each of the switches in Fig.4.1 is three

GaN Systems GS66516T GaN FETs in parallel, designed to handle the high currents that are switched by the active rectifier / unfolder stage. Compared to a conventional silicon MOSFET implementation, the GaN Systems GS66516T 650 V, 25 mΩ GaN FETs have a significantly lower $R_{DS,on}$ for the same volume, and therefore provides an attractive power density increase [51], [52]. Silicon Labs Si8274 dual-channel complementary isolated gate drivers are used to drive the power switches, and a conventional bootstrap stage is used to power the high-side gate drivers and FETs. Deadtime between the switching devices in the H-bridge legs is generated internally by the Si8274 gate driver chip.

The frequency multiplication and voltage division effect of the FCML topology is evident in the size of the passive components selected for use in the system. The GaN FETs in the FCML power stage are switched at 144 kHz, resulting in a 720 kHz ripple frequency at the filter inductor. Each flying capacitor is $\sim 2.6\mu$F in value, and a single 22 μH inductor per FCML stage is used. The TDK online datasheet for the 2.2 μF 450 V X6S capacitors was consulted to account for the voltage de-rating effect of ceramic capacitors, where the effective capacitance is noted using manufacturer supplied data points [53], and using a linear interpolation where the voltage of a certain node falls between data points; the number of capacitors in parallel used per flying capacitor is shown in Table 4.3, referencing the capacitors in Fig. 4.1.

Table 4.3: Flying capacitor component detail using TDK 2.2 μF 450 V X6S capacitors in parallel.

Node	**V_{node}** (V)	**Capacitance / Capacitor** (nF)	**# Caps**	Total Capacitance (nF)
C_1	80	1471	2	2942
C_2	160	924	3	2772
C_3	240	665	4	2660
C_4	320	524	5	2622

Due to the expected losses of the main FCML power stage – over 4 W per device – custom heatsinks were designed for the power stage components. Simulations were done with SolidWorks thermal and flow simulation tools, as well as ANSYS, to calibrate heatsink performance (Fig 4.5). The FCML stage was expected to dissipate the most power, and therefore is designed and simulated with forced-air convection in mind. The unfolder / active rectifier stage was expected to dissipate minimal power, and so the heatsink designed for that stage assumes largely natural convection or incident but not forced airflow. Mechanical mounting holes and fixtures were designed concurrent to the PCB electrical design, to ensure that the devices could be heatsunk properly and not exceeding any mechanical stress limits. To stay within the manufacturer recommended pressure of 30 PSI per EPC GaN device [54], heatsink standoffs were milled to precise tolerances such that a gap filler material (Alphacool Eisschicht 17 W/mK, 1 mm thickness) would be compressed by $\sim 15\%$ when fully interfaced [46]. Furthermore, when attaching the heatsink to the converter, torque wrenches were used

to ensure that the heatsink was exerting the proper amount of force. Figure 4.6 shows the stackup of the thermal interfaces between the FCML GaN devices and heatsink. The unfolder stage utilizes GaN Systems GS66516T top-cooled GaN FETs, and has a similar stackup, though the devices are soldered directly to the main PCB, and so do not require a daughterboard PCB. The GaN Systems devices have a much larger surface area for cooling and a package construction that does not expose the bare die, and therefore are not as sensitive to pressure applied.

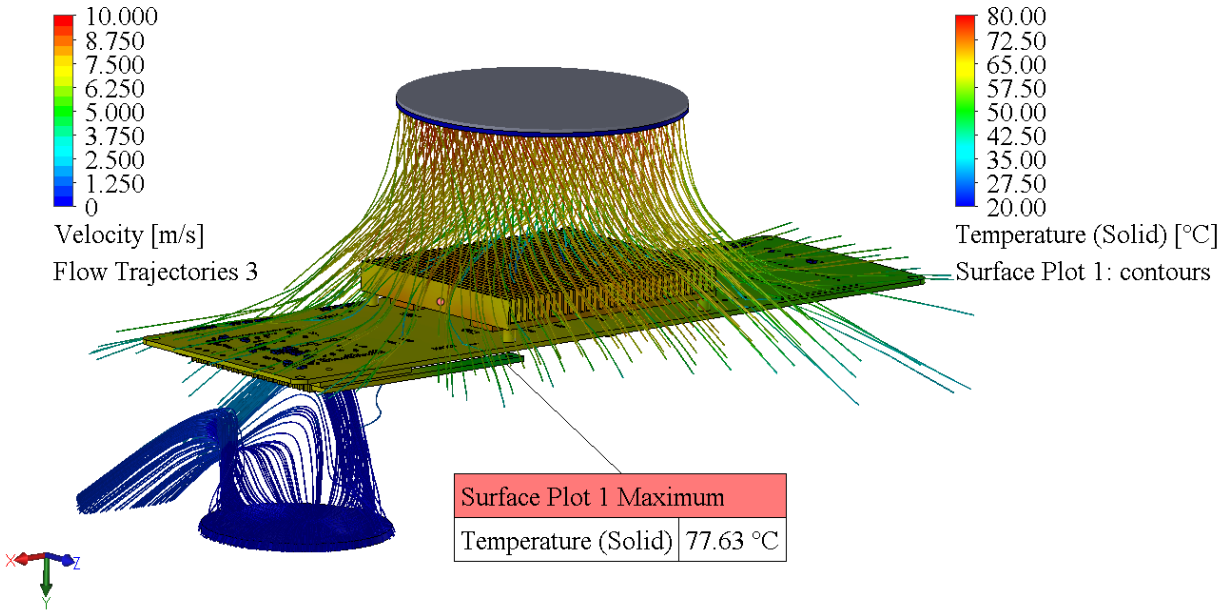

Figure 4.5: SolidWorks Flow Simulation model with estimated temperature assuming 25 °C ambient.

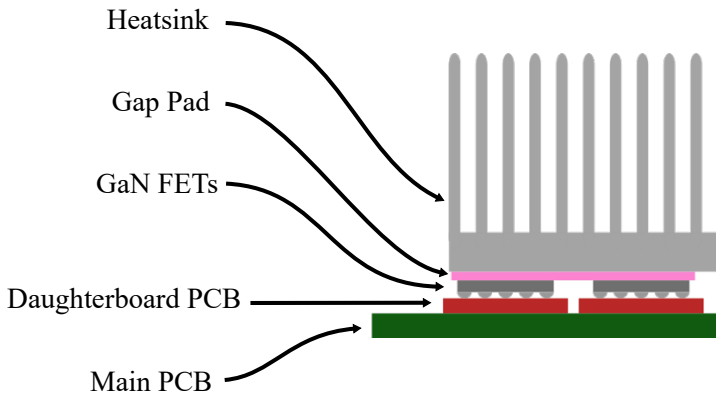

Figure 4.6: Diagram of stackup for heatsink interface. (Image created in collaboration with Kelly Fernandez)

Control of this converter is achieved with an Altera MAX10 series FPGA, which generates all of the interleaved complementary FCML PSPWM control signals with deadtime, as well as the unfolder / active rectifier H-bridge control signals. The PSPWM method combined with the 6-level FCML architecture achieves good natural flying capacitor voltage balancing [19], [50], [55]. To verify power stage operations, the system is run as an inverter, converting from 400 V_{dc} to 240 V_{ac}. The load is a reconfigurable resistor bank representing different power output levels. The board design also includes provisions for attaching further control systems, such as a microcontroller, to interface with the FPGA.

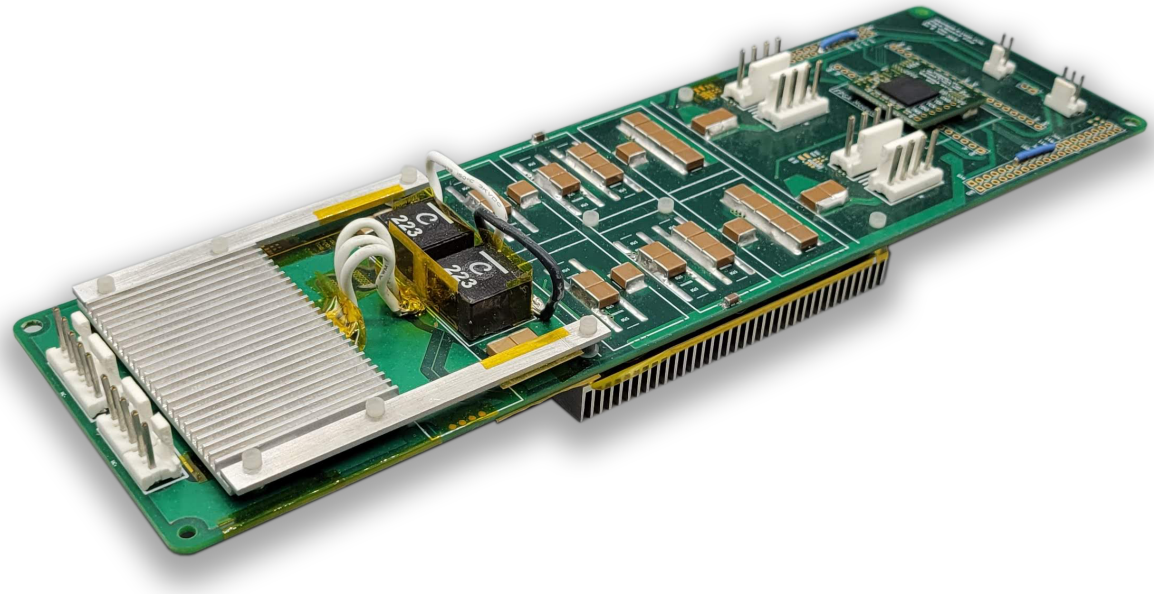

Figure 4.7: Power stage prototype.

4.4 Experimental Results

The full system (Fig. 4.7) has been tested to a power processing capability of 7 kW, converting from 400 V_{dc} to 240 V_{ac}. Table 4.4 details the performance of the converter as measured. The converter achieves a volumetric power stage density of 785 W/in^3 (47.9 W/cm^3) and a gravimetric power density of 24.6 kW/kg. Since the maximum height of the converter is dictated by the heatsinks and the inductors, and the component volume is much smaller than the volume bounded by the maximum component dimensions in each direction, the power density figure is calculated using the composite volume of a prism bounding the FCML stage, a prism bounding the inductors, and a prism bounding the unfolder stage, as shown in the side view of Fig. 4.8. Figure 4.9 shows the efficiency of the system as a function of output power, with liberal airflow ($\sim$ 150 CFM) and with heatsinks on the main power devices. Furthermore, Figure 4.10 is an estimated loss breakdown of the converter operating at full power (7 kW). Out of a total estimated 121 W of losses at full power, the FCML stage accounts for the bulk, about 71.5%, and the active rectifier / unfolder stage is about 15.9%. The inductors are about 8.1% while the PCB, gate drive, and control are about 4.5%. We note that the fan cooling solution is not included in the power density figure nor the loss breakdown, but also that the thermal management system may be adjusted to accommodate different operating conditions and environments. For this design, including the fan cooling losses may drop the maximum power efficiency by about 0.1$\sim$0.2%; this can be optimized

further or replaced with a completely different design. For example, a liquid cooling loop may be available and the design could be adjusted to accommodate such a system. The power stage efficiency was measured with a Keysight PA2201A Power Analyzer, and the efficiency plot accounts for all control and gate drive losses as measured through a Keysight E36312A supply; the full system achieves a peak efficiency of 98.9% at 3.3 kW and an efficiency of 98.3% at 7 kW. During testing, the heatsinks remained below 85 °C as measured by a FLIR T540 thermal camera, which is within the rated temperature of most commercially-available electronic parts.

Figure 4.8: Side view of converter prototype.

Table 4.4: Key Performance Specifications

Parameter	Value	Notes
dc Voltage	400 V_{dc}	Tested
ac Voltage	240 V_{ac}	Tested
ac Current	29.8 A	Tested
ac Power	7 kW	Tested
Efficiency	98.9%	Peak Eff. (At 3.3 kW)
	98.37%	At 7 kW
THD	$\leq$ 0.3%	Measured at 7 kW
Switching Frequency	144 kHz	Per switch
Effective Frequency	720 kHz	At inductor
Weight	284.6 g	Incl. heatsinks
Rect. Box Dimensions	10.3" x 3.05" x 0.535"	Excl. heatsinks
	(26.16 cm x 7.75 cm x 1.36 cm)	
Rect. Box Volume	16.8 in^3 (275.42 cm^3)	Excl. heatsinks
Rect. Box Volume	27.5 in^3 (450.64 cm^3)	Incl. heatsinks
Power Stage Volume	8.93 in^3 (146.4 cm^3)	Incl. heatsinks
Volumetric Power Density	785 W/in^3 (47.9 W/cm^3)	Power stage & heatsink
Gravimetric Power Density	24.6 kW/kg	Incl. heatsink

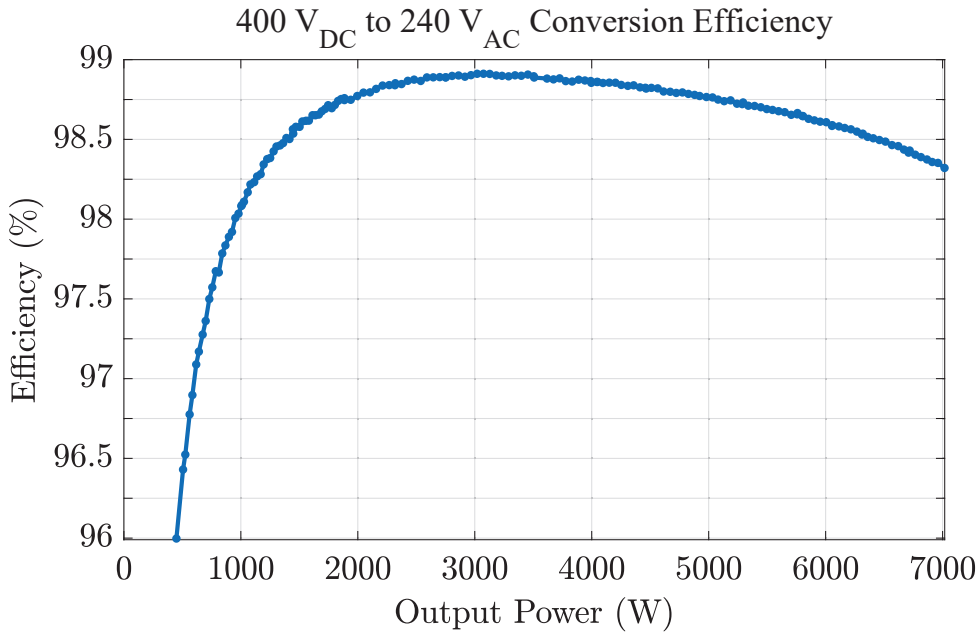

Figure 4.9: Converter efficiency plot, with heatsink, up to 7 kW, including all control and gate drive losses.

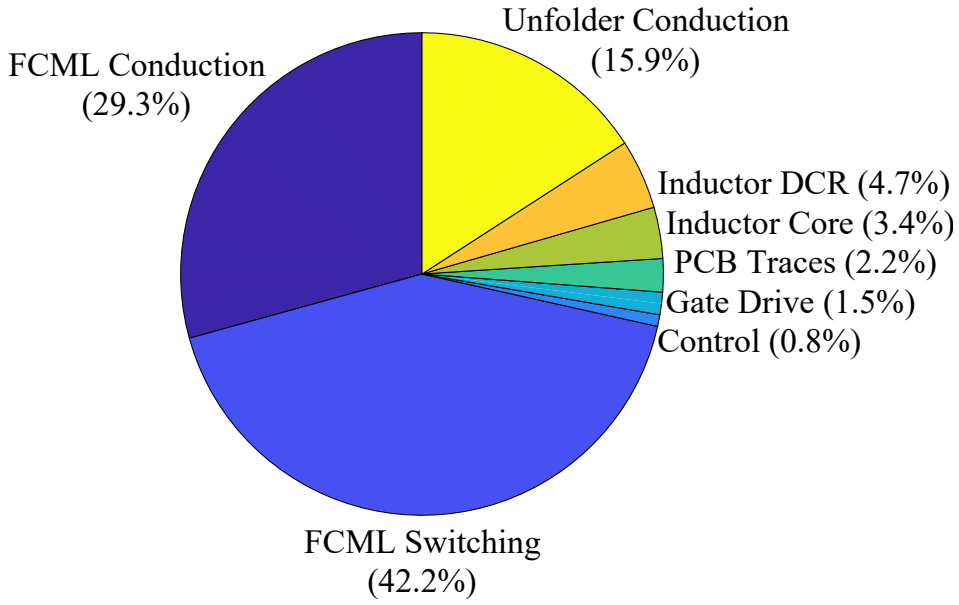

Figure 4.10: Estimated loss breakdown at 7 kW.

Figure 4.11 shows the multi-level voltage output at the switch-node, V_{sw} in Fig. 4.1, along with filtered output voltages and currents, V_{ac} and I_{ac}, respectively. The measured output total harmonic distortion (THD) is less than 0.3%: the inductors see a ripple frequency of 720 kHz with stepped voltages a fraction of the input voltage, and the ripple currents are interleaved to reduce output current and voltage ripple harmonics. Note that the output ripple currents between phases are not perfectly balanced, but are roughly equivalent and thus largely cancel out, as seen in Fig. 4.12. Further control may be applied to balance the loads between phases, but most of the benefits of interleaving are achieved from the naïve control method of simply applying the same control signals to each of the phase legs, phase-shifted by 180 degrees.

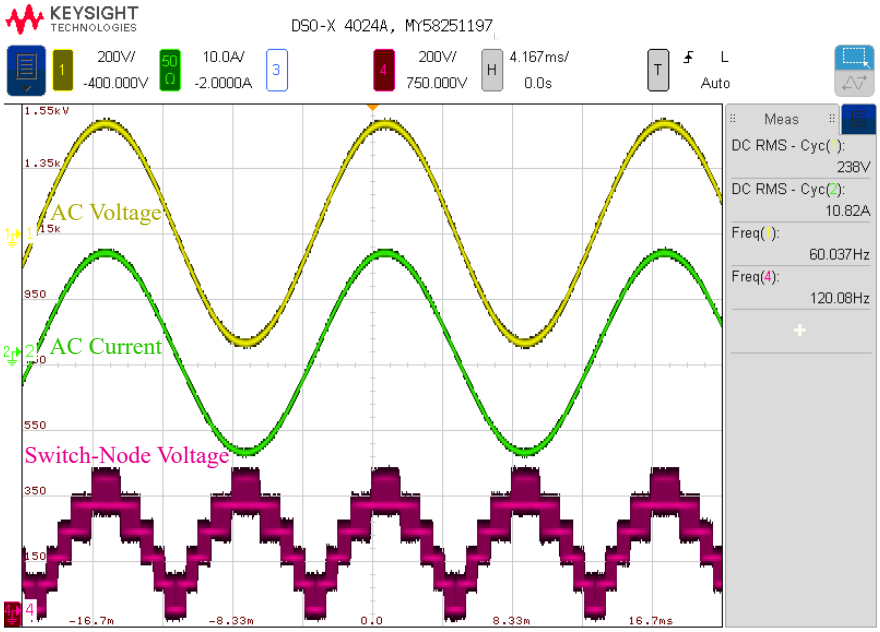

Figure 4.11: Typical oscilloscope traces of ac voltage and current as related to the FCML switch-node voltage waveform.

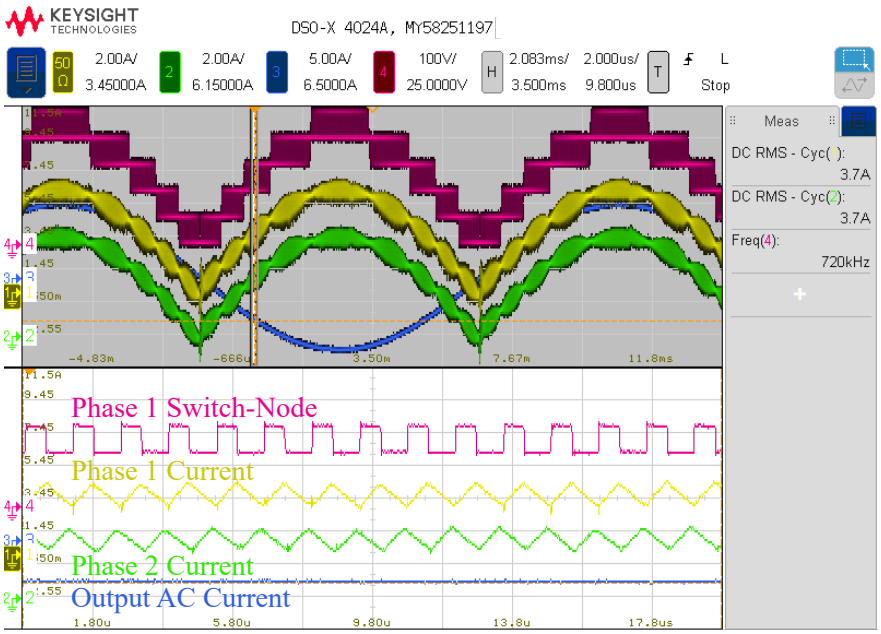

Figure 4.12: FCML interleaving operations, showing current waveform canceling.

4.5 Conclusions

This chapter demonstrates the power stage for a Level II charger converter platform with excellent power density figures, realized through an interleaved FCML power stage connected to an active rectifier / unfolder stage, both utilizing GaN technology. Control is achieved with an FPGA which generates all of the PSPWM and H-bridge output signals. Thermal management is achieved with custom-milled heatsinks and a carefully-maintained stackup height. A hardware prototype has been constructed, achieving a full system efficiency of greater than 98.9%, a power processing capability of 7 kW, an efficiency of 98.3% at full power, and an effective inductor frequency of 720 kHz. A gravimetric power density of 24.6 kW/kg is achieved, and a volumetric power density of 785 W/in^3 (47.9 W/cm^3) is achieved.

4.6 Acknowledgements

Support for this chapter was in part funded by the National Science Foundation Graduate Research Fellowship Program under Grant No. DGE-1144245, the Power Optimization of Electro-Thermal Systems (POETS) National Science Foundation Engineering Research Center with cooperative agreement EEC-1449548, and a direct industry supported project from Toyota, through POETS. Additionally, the information, data, and work presented

herein was partially funded by the Advanced Research Projects Agency - Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000900.

Chapter 5

Electric Vehicle Charger System Design

Level II on-board electric vehicle (EV) chargers interface with the ac grid to charge a high-voltage battery. This provides the capability to take advantage of widespread infrastructure providing single-phase ac grid voltages (120–240 V_{ac}) with power capabilities at kilowatt levels [56]. Since the charger is carried within the vehicle at all times, designs that are compact, highly efficient, and lightweight are highly desirable due to space and range constraints in EVs. In the following chapters (5, 6), we seek to improve the overall gravimetric and volumetric power density of the single-phase ac-dc stage of a level II EV charger, considering converter topology, mechanical design and assembly, and thermal management simultaneously. The FCML power stage is combined with the series-stacked energy buffer in an 3-D integrated design.

5.1 Introduction

In a conventional design, an ac-dc stage is usually implemented with a boost converter connected to a large electrolytic capacitor bank. The current through the boost inductor is controlled to regulate the ac current with a high power factor and low distortion with a Power-factor Correction (PFC) controller. The capacitor bank buffers the twice-line frequency pulsating power in single-phase ac-dc and dc-ac applications. The boost inductor and the electrolytic capacitor bank are some of the largest contributors to volume and weight in such designs.

A system architecture featuring the flying-capacitor multilevel (FCML) converter as the inverter or power factor correction (PFC) stage, and a series-stacked buffer (SSB) as the energy buffer stage, is used to improve gravimetric and volumetric power density as compared to conventional designs, as shown in Fig 5.1. It has been shown that the FCML topology [19], [20] has the potential to dramatically reduce passive component volume and weight in inverter [1], [10], [25] and PFC applications [26], [27] due to the use of high energy density

ceramic capacitors and reduced voltage stress on inductors; The active buffer topology of SSB as discussed in [21]–[23] reduces the needed capacitance for single-phase energy buffering by allowing a large voltage swing on the buffering capacitors, yet it also minimizes the loss from the extra power converters in the buffer as the converter only processes a small fraction of the total system power. The high power density and efficiency of the SSB have been demonstrated in the full single-phase system in [10], [27].

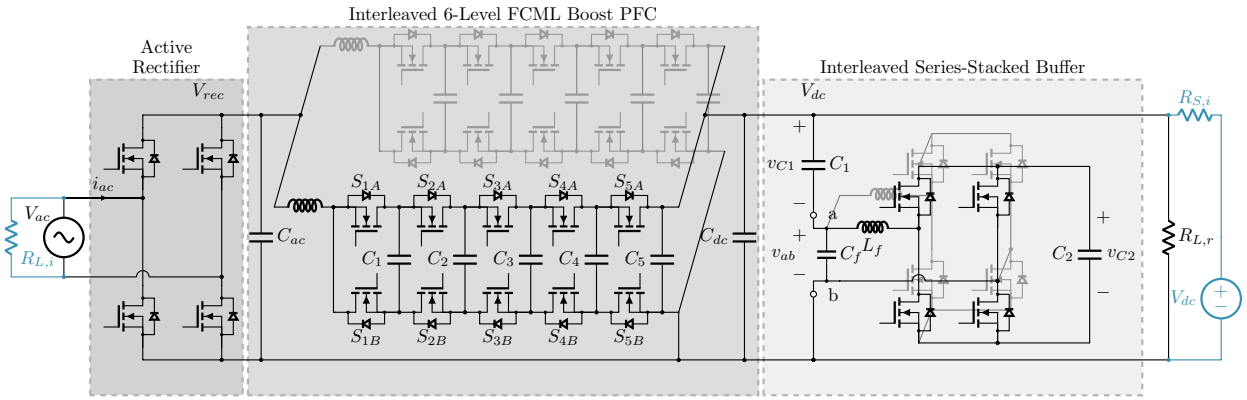

Figure 5.1: Schematic of the overall system with active rectifier (unfolder), interleaved FCML, and series-stacked buffer. The dc source and load in the inverter mode are shown in blue.

For mechanical packaging, the overall assembly aims to maximize the utilization of the 3-D space with a low-profile and modular design philosophy, enabled by the use of high energy density ceramic capacitors and the reduced inductor size in both FCML and SSB stages. The heat-generating components are placed on a single side to allow for simple thermal circuit routing and higher thermal efficiency for automotive cooling systems. In this chapter [4], [5], system architecture, control, thermal design are discussed.

The remainder of the chapter is organized as follows: Section 5.2 describes electrical system operations and electrical system design. Section 5.3 describes the integration of the electrical and mechanical designs. Section 5.4 details the thermal system design.

5.2 Electrical System Architecture and Operation

The overall system schematic drawing is shown in Fig. 5.1. From the ac side to the dc side, it consists of an active rectifier, an ac-dc (bi-directional) conversion stage with 2-phase interleaved FCML converters, and a series-stacked buffer (SSB) across the dc bus. The overall control diagram for both PFC and SSB is shown in Fig. 5.2, and the control for the inverter mode is shown in Fig. 5.3. For the analysis in this work, unity power factor is

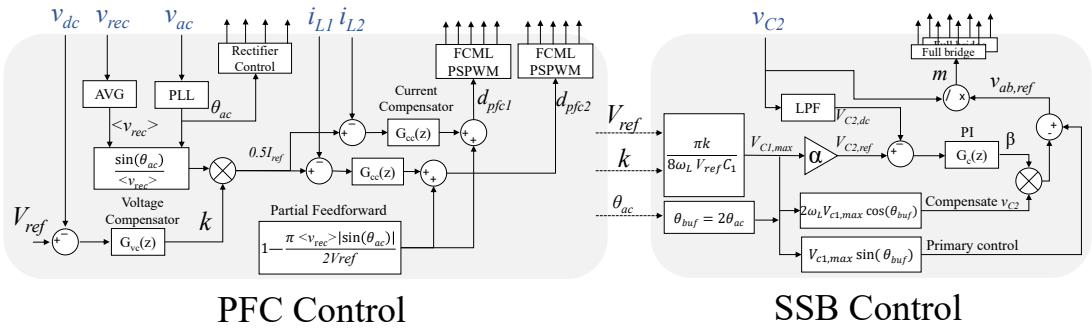

Figure 5.2: Overall control system of the interleaved PFC and SSB in rectifier mode. The sensed parameters are in blue font. (Plot created in collaboration with Zitao Liao)

considered for both rectifier and inverter mode. The ac voltage and current are described as:

$$v_{\text{ac}} = V_{\text{ac}} \sin(\omega_L t) \tag{5.1}$$

and

$$i_{\text{ac}} = I_{\text{ac}} \sin(\omega_L t), \tag{5.2}$$

where V_{ac} and I_{ac} are the magnitudes, and ω_L is the line frequency (60 Hz U.S. line frequency is considered in this work).

Rectifier mode

FCML PFC stage

In the ac-dc mode, the PFC stage regulates the input ac current to be in phase with the input voltage with low harmonics, which is implemented with two interleaved FCML boost converters. With the FCML, the inductor size is reduced by $(N-1)^2$ times compared with conventional two-level boost converters (where N is the number of levels) [19], [20]. The smaller inductor brings challenges of input current phase leading caused by limited loop gain and bandwidth of the current compensator, which can be solved with an additional feedforward term [26], [57]. The inductor current of each phase is regulated independently as shown in Fig. 5.2 to ensure equal current sharing between the two phases.

Series-Stacked Buffer

The schematic of the SSB is shown in Fig. 5.1. The main buffering capacitor C_1 is connected in series with a full-bridge converter. As v_{C1} ripples with the pulsating power, the full-bridge converter actively cancels the ripple on v_{C1} with generated v_{ab} such that the dc-bus is ripple

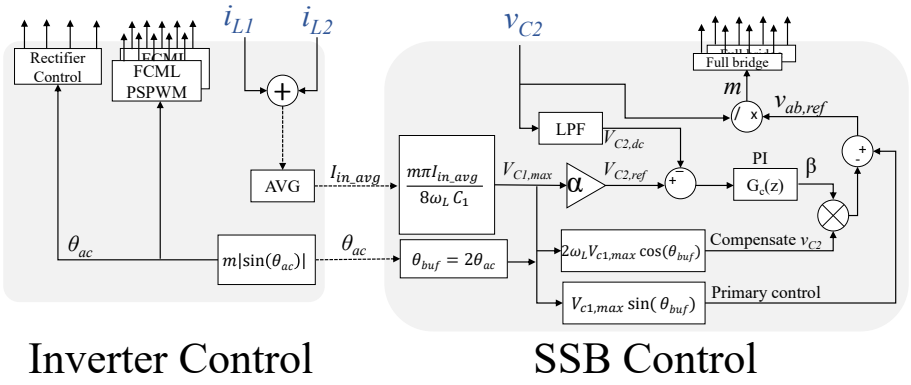

Figure 5.3: Overall control system in inverter mode. (Plot created in collaboration with Zitao Liao)

free. With the high voltage swing, the energy utilization of C_1 is increased to reduce the needed capacitance. Moreover, since the high dc-bus voltage is blocked by C_1 from the full-bridge converter, the full-bridge converter only processes a small fraction of the total system power, which results in high efficiency. The voltage of C_2 is regulated with a feedback loop that draws real power into the full-bridge converter to prevent the capacitor voltage from decaying, which will introduce a small amount of extra voltage ripple on the dc-bus. A detailed description of the operation and component sizing of the SSB architecture can be found in [23].

A control scheme [27], [30] that couples the SSB controller with the PFC control parameters is implemented to ensure the phase and power relation between the two stages. The voltage-loop factor k that scales the input current and the angle of the ac voltage are passed to the SSB controller to determine the magnitude and phase of the reference voltage for v_{ab}. If ac voltage is $V_{ac}\sin(\omega_L t)$, the ideal voltage v_{ab} is

$$v_{\mathrm{ab}} = \frac{P_{\mathrm{dc}}}{2\omega_L V_{\mathrm{dc}} C_1}\sin(2\omega_L t) = \frac{\pi k}{8\omega_L V_{\mathrm{dc}} C_1}\sin(2\omega_L t), \tag{5.3}$$

where P_{dc} is the dc load power, ω_L is the line angular frequency, V_{dc} is the average dc-bus voltage [27]. P_0 can then be calculated from the voltage-loop factor k such that the magnitude for v_{ab} is obtained.

Inverter Mode

In the inverter mode, the dc load is replaced with a dc-source, and the ac source is replaced with a resistor as shown in Fig. 5.1. For simplicity, the ac load considered in this work is resistive and the FCML inverter runs open-loop voltage control with the rectified sinusoidal duty ratio:

$$d_{\mathrm{inv}} = m|\sin(\omega_L t)|, \tag{5.4}$$

where m is the modulation depth (0 to 1) determining the peak ac voltage $V_{\text{ac}} = mV_{\text{dc}}$. The angle $\theta_{ac} = \omega_L t$ is passed to the rectifier/unfolder control to create a full sine wave.

Instead of sensing the inverter current to generate a current reference for the SSB as in [21], the same inductor current sensors in the PFC mode are used to calculate the system power such that the voltage-based control scheme in [27], [30] can be applied. Note that the inductor current direction is reversed compared to the PFC mode, which means the current sensing circuitry should be able to measure bi-directional current. In the actual hardware implementation, the current amplifier LT1999 with 1.5-V dc bias at zero current is used.

The load ac current of the two FCML phases are measured and averaged with moving-average filter at 120 Hz. If the peak ac current is I_{ac}, the 120 Hz average value is $\frac{2I_{\text{ac}}}{\pi}$. As shown in (5.3), the magnitude of v_{ab} can be calculated with the dc power level. In this case, the averaged ac current is used to calculate the load dc power as

$$P_{\text{dc}} = V_{\text{dc}} I_{\text{dc}} = \frac{V_{\text{ac}} I_{\text{ac}}}{2} = \frac{m V_{\text{dc}} I_{\text{ac, avg}} \pi}{4}. \tag{5.5}$$

The new expression for the SSB controller to generate the correct v_{ab} can thus be simplified to:

$$v_{\text{ab, inv}} = \frac{P_{\text{dc}}}{2\omega_L V_{dc} C_1} \sin(2\omega_L t) = \frac{m\pi I_{\text{ac, avg}}}{8\omega_L C_1} \sin(2\omega_L t). \tag{5.6}$$

Once the magnitude of v_{ab} is determined, the remainder of the SSB control is identical to the PFC mode.

5.3 Mechanical Design

In addition to being able to fit all of the electrical systems in a 2-D design space, the 3-D design space was considered. The board layout files were exported from the eCAD space to the mCAD space in order to maximize the utilization of 3-D space. Component models, relative board distances, and connector locations were all considered during the design process, and the design was done iteratively between eCAD and mCAD. Trade-offs such as moving components to different physical boards were made during this stage of the design process. For example, in Fig. 5.4, one can note that the series-stacked buffer and the unfolder stages are actually merged together on a single physical board. Furthermore, the FCML stages from before are split into their own modules. Power connectors are designed to be both mechanically secure as well as electrically active: power tap elements secured with M3 screws provide stability as well as the current-carrying capacity (about 15 A per tap element) required by the system. Finally, a connectors board was conceived to provide all of the logic and signals connectivity for the system. With this design, the power connectivity is prioritized as the core of the system, where the connectivity for logic-level signals and power is provided on the periphery.

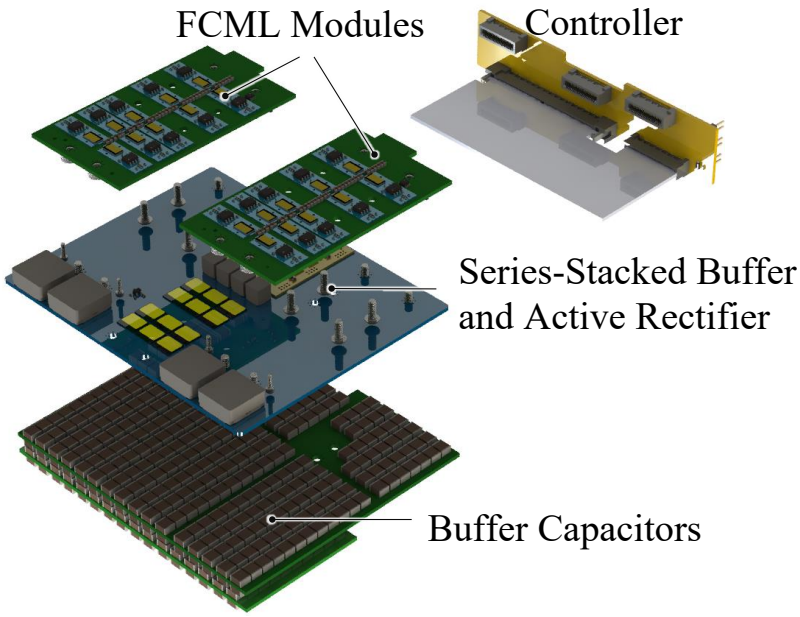

Figure 5.4: Exploded view render of the electric vehicle charger assembly.

5.4 Thermal Design

To manage the heat generated by components in the electrical system, a liquid cooling solution is proposed, to take advantage of possible existing liquid cooling loops in vehicles. This proposed solution is done in collaboration with a team at the University of Illinois at Urbana-Champaign [5]. The University of Illinois team was responsible for the overall mechanical design and manufacturing of the cold plate.

The heat is dissipated by indirect flow cooling of water into an aluminum single-inlet/single-outlet cold plate that we designed. The main heat-generating components are the GaN devices, estimated at upwards of 5 W each and the inductors upwards of 7.5 W each. The design of the cold plate was guided by thermo-fluidic CFD simulations performed in ANSYS IcePAK. The simulations, coupled with analytical models, enabled rapid iteration and convergence to a design that has an equitable trade-off between pressure drop and sufficient cooling for the power electronic components. The 0.125 inch diameter channel is directed such that the majority of the fluid is routed toward the most power dense components. Additional paths were added to reduce the temperature gradient across the cold plate. The cold plate shape was designed such that it matches the different heights once attached to the rest of the system, to ensure good thermal contact and minimize thermal resistances.

We manufactured the designed cold plate using 6063 aluminum alloy, owing to its high thermal conductivity and light weight. The fabricated cold plate has a weight of 300 $\pm$ 0.5 g and a volume of 0.17 $\pm$ 0.01 L. We manufactured it (Fig. 5.5) according to the following

steps:

- Rough milling to create the height differences and the cylindrical inlet/outlet.
- Milling finish to minimize roughness.
- Drilling to create the inlet/outlet and the interior channels.
- Plugging the holes with press-fitted aluminum and welding on the outside to close the holes on the edges and leave only the inlet/outlet open.

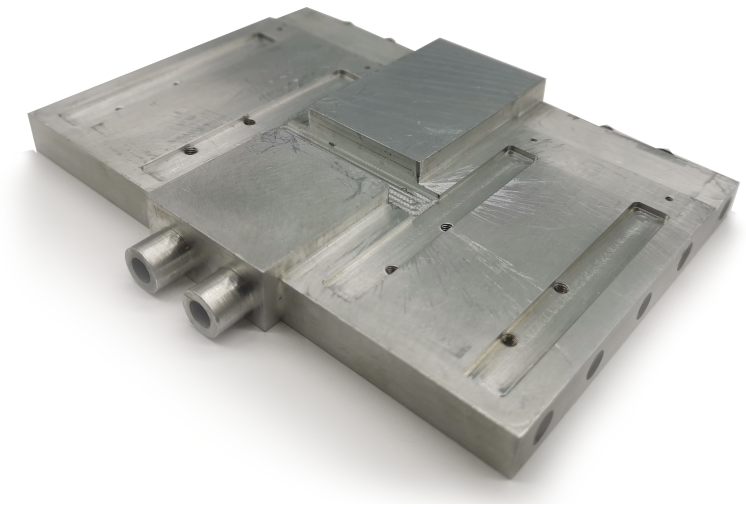

Figure 5.5: The manufactured cold plate. (Image created in collaboration with Zitao Liao)

Chapter 6

Validation of the Electric Vehicle Charger System

Building upon the Chapter 5's proposed electrical architecture, this chapter [4], [5] presents the hardware implementation of a bidirectional single-phase ac-dc converter, converting between low- and high-line ac (120–240 V_{ac}) and 400 V_{dc}. Discussions of electrical, mechanical design and assembly, and thermal management of an interleaved 6-level flying capacitor multilevel (FCML) power factor correction (PFC) stage with a twice-line-frequency series-stacked buffer (SSB) stage are included. Experimental results demonstrating dc-ac inverter operations at the kilowatt scale are provided. The main contributions of this chapter are as follows:

- Hardware demonstration of the interleaved FCML PFC/inverter with active buffers, with the highest reported power level of 6.1 kW. The bidirectional ac-dc control scheme for interleaved FCMLs, PFC and SSB operations is efficiently implemented in a single digital controller.
- Utilizing the optimization method in [23] and the interleaved operation and modulation, the SSB in this work has higher power density than all prior hardware demonstrations.
- Full liquid-cooling system, and hardware implementation with detailed measurement of critical temperatures.
- Compact electrical design and assembly with all contract-manufactured Printed Circuit Boards (PCBs), achieving 201 W/in^3 (12.3 W/cm^3) overall power density including liquid cooling systems.

This chapter is organized as follows: Section 6.1 details the hardware implementation of the charger system design presented in Chapter 5. Section 6.2 presents the experimental test results of the system in PFC and inverter mode, and Section 6.3 provides concluding remarks.

6.1 Hardware Implementation

This prototype was designed to balance electrical, mechanical, and thermal design aspects. The electrical design takes advantage of the modularity of the FCML structure, and was done with consideration to the mechanical and thermal layouts. The mechanical design takes advantage of 3-D space to pack components at a high density, and is also modular. Finally, the thermal management drove both the electrical and the mechanical aspects towards a single-sided cooled design so as to simplify thermal circuit routing. Optimization of the layout is a multi-objective problem, and a multitude of methodologies ([23], [58]–[60]) may be utilized to produce a satisfactory result. In this case, we assisted our design process with script calculations for losses, 3-D volume constraints, and electrical and mechanical clearance considerations. The resultant hardware prototype packs all of the heat-generating devices on a single side, with most of the ancillary circuitry on the periphery so that the core power conversion circuitry may be centralized.

Table 6.1: Overall system component listing

Subsystem	Component	Part No.	Parameters
Interleaved 6-Level FCML (per leg)	GaN FETs	GaN Systems GS61008T	100 V, 7 $m\Omega$
	Isolated Gate Drivers	Si8271GB-IS	Silicon Labs Si827x Series
	Flying Capacitors	TDK C5750X6S225K250KA	2.2 μF × 2–5 (parallel) ∼ 2.6μF effective
	Inductors	Vishay IHLP6767GZER100M11	10 μH
Active Rectifier / Unfolder	GaN FETs	GaN Systems GS66516T	650 V, 25 $m\Omega$× 3 (parallel)
	Isolated Gate Drivers	Si8274GB1-IS1	Silicon Labs Si827x
Interleaved Series-Stacked Buffer (per leg)	GaN FETs	EPC 2033	150 V, 7 $m\Omega$
	Isolated Gate Drivers	Si8274GB1-IM1	Silicon Labs Si827x
	Inductors	Coilcraft XAL7070-472	4.7 μH × 2 (series)
Buffer Capacitors	C_1	TDK C5750X6S225K250KA	0.43 μF × 850 (parallel) ∼ 366μF effective at 400 V bias
	C_2	TDK C5750X7S2A156M250KB	3 μF × 200 (parallel) ∼ 600μF effective at 100 V bias
Control	Microcontroller	TI F28379D controlCARD	C2000 Series Microcontroller

A hardware prototype has been constructed with the proposed architecture and control, as shown in Fig. 6.1. A modular FCML converter design was done to streamline manufacturing and debugging (Fig. 6.3). The hardware prototype consists of two interleaved FCML converters, a series-stacked buffer twice-line frequency buffer stage, an H-bridge unfolder, and energy buffering capacitors. To control the converter, a TI C2000 microcontroller was selected, which connects through a signal backplane board. Power is transferred through bolt-type connections between major power boards. An exploded-view detail render of the electrical portion of the prototype is shown in Fig. 6.2. For the thermal management system, the custom cold plate design (Fig. 5.5) discussed in Section 5.4 is used.

In the FCML stage, which sees a maximum dc voltage of 400 V_{dc}, each switch is required to block 80 V ($V_{dc}/5$). Therefore, 100 V rated GaN devices from GaN Systems were selected

as the main power devices.

For the H-bridge unfolder stage, 650 V rated GaN Systems devices were chosen to handle the 240 V_{ac} line voltage. For the series-stacked buffer, the switches must withstand 110 V, so 150 V GaN devices from EPC Co. are used. Key components used in the charger system and their characteristics are described in Table 6.1.

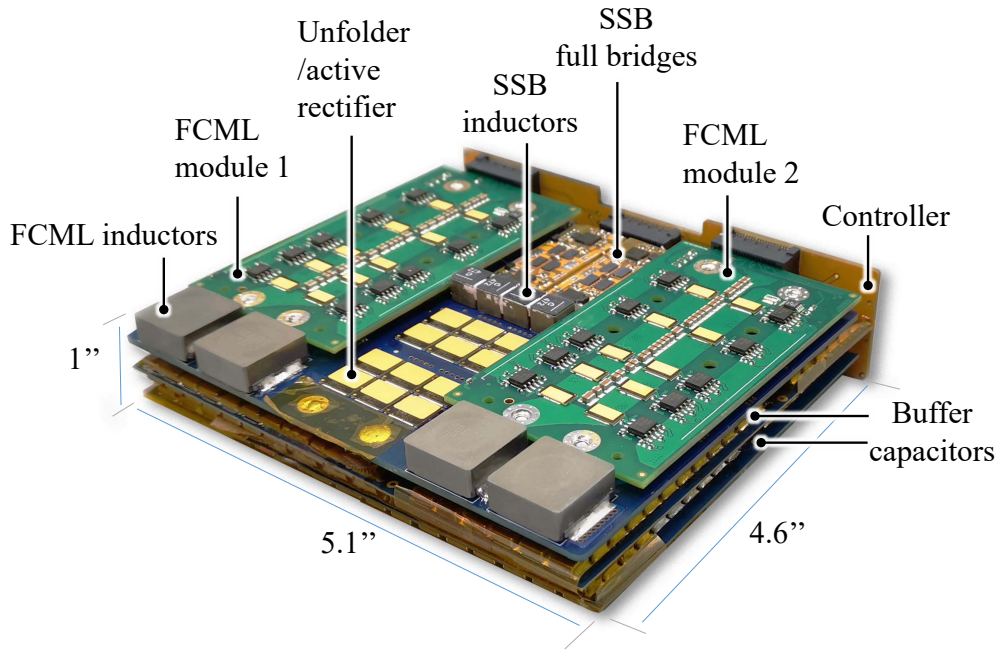

Figure 6.1: The EV charger assembly, not including thermal management. Key subsystems are labeled. (Image created in collaboration with Zitao Liao)

High power density FCML module

To aid in the construction of the full charger system, a high power density FCML module was designed. This module (Fig 6.3) contains the core power conversion stage of a 6-level FCML converter, minus the filter inductor element.

An air-cooled heatsink design (Fig. 6.4) was designed and manufactured to evaluate the performance of the FCML module with air cooling. While liquid cooling is attractive in automotive applications as this can utilize existing cooling loop infrastructure, air-cooled designs have seen increased interest for the flexibility of placement in the vehicle that it

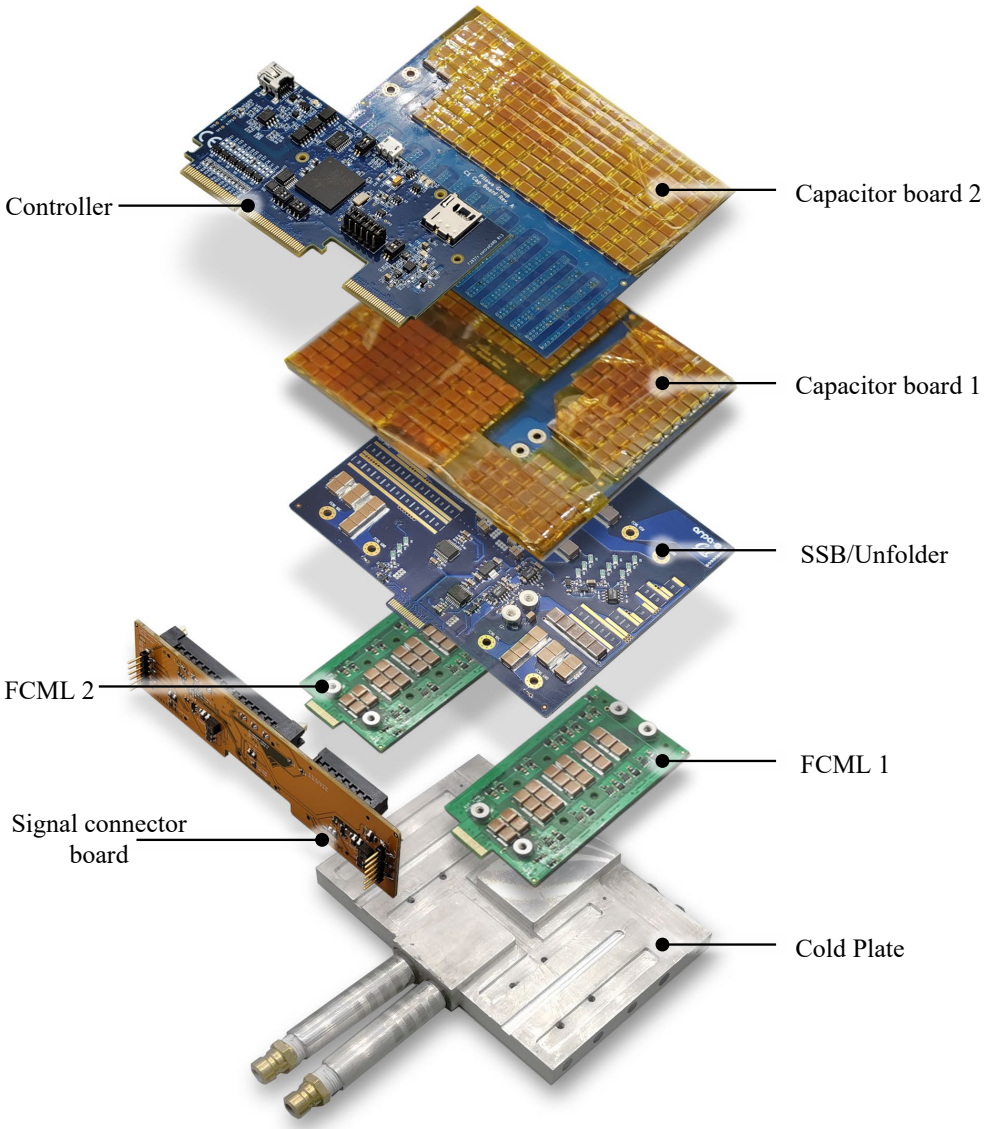

Figure 6.2: Exploded view of the hardware assembly. (Image created in collaboration with Zitao Liao)

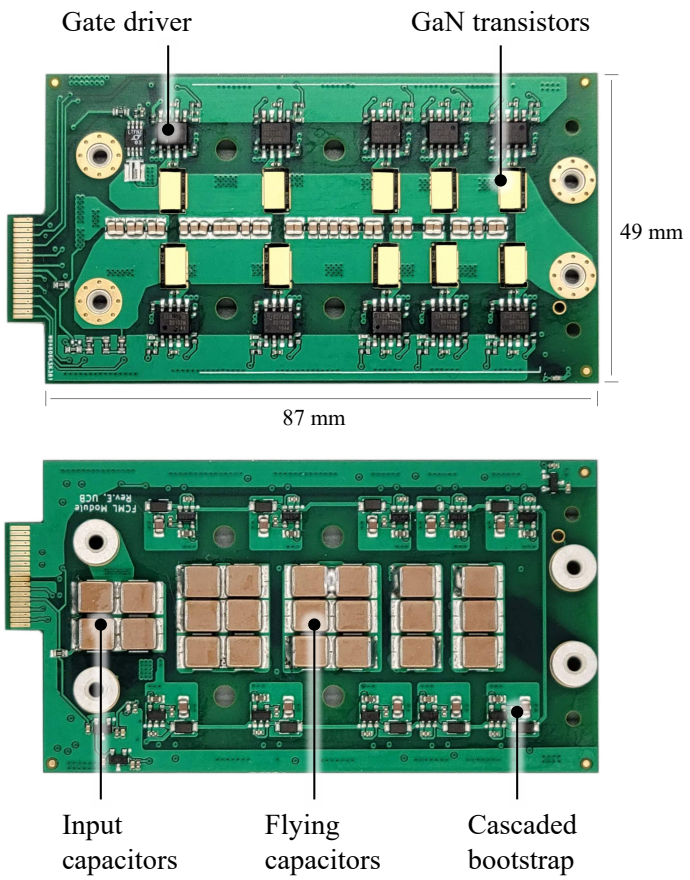

Figure 6.3: Single FCML module with key components annotated.

enables. A single FCML module was tested in the dc-dc mode converting from 400 V_{dc} to 260 V_{dc}, with an air-cooled heatsink to measure thermal performance; this test exceeded 4 kW. The efficiency of the FCML module running in dc-dc mode is shown in Fig. 6.5. The FCML module heatsink did not exceed a reading of 70 °C under a FLIR T540 thermal camera.

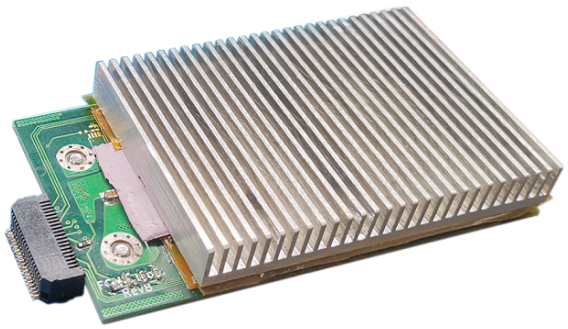

Figure 6.4: Single FCML module with air-cooled heatsink attached. (Image created in collaboration with Zitao Liao and Kelly Fernandez)

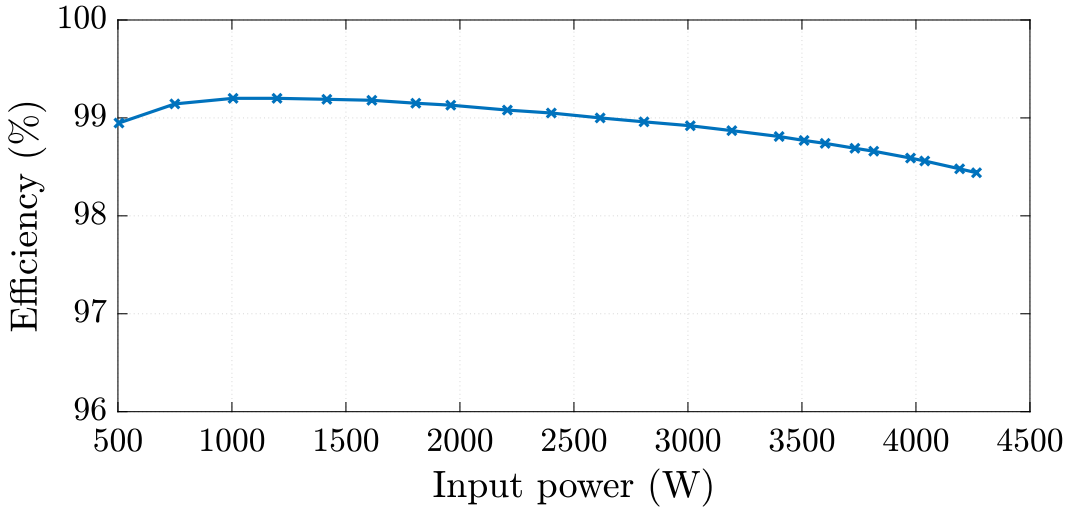

Figure 6.5: The efficiency of the FCML module, running from 400 V_{dc} to 260 V_{dc}. (Image created in collaboration with Zitao Liao and Kelly Fernandez)

Unfolder/Buffer Carrier Board

As the system was designed in a 3-D stacked manner, the unfolder / active rectifier and the series-stacked buffer are integrated onto a board (Fig. 6.6) which also holds mechanical hardpoints for mounting the FCML module boards and capacitor boards. In addition, all of the power inductors in the core power conversion and energy buffering stage are soldered onto this board, taking advantage of the 3-D packing to improve the overall system power density. The inductors are taller than all of the other components on this board, but when the FCML boards are stacked on top of the carrier board, the overall height is just about

level with the FCML GaN devices. Mechanical securement is achieved primarily with M3 button-head cap screws, with some M1.6 screws for supplementary adjustment.

This board also contains all of the ac and dc sensing circuitry required for proper control, implemented with resistor dividers and buffer op-amps which are connected to the ADCs on the microcontroller. The voltage across capacitor C_2 is sensed with an LT1990 differential amplifier IC.

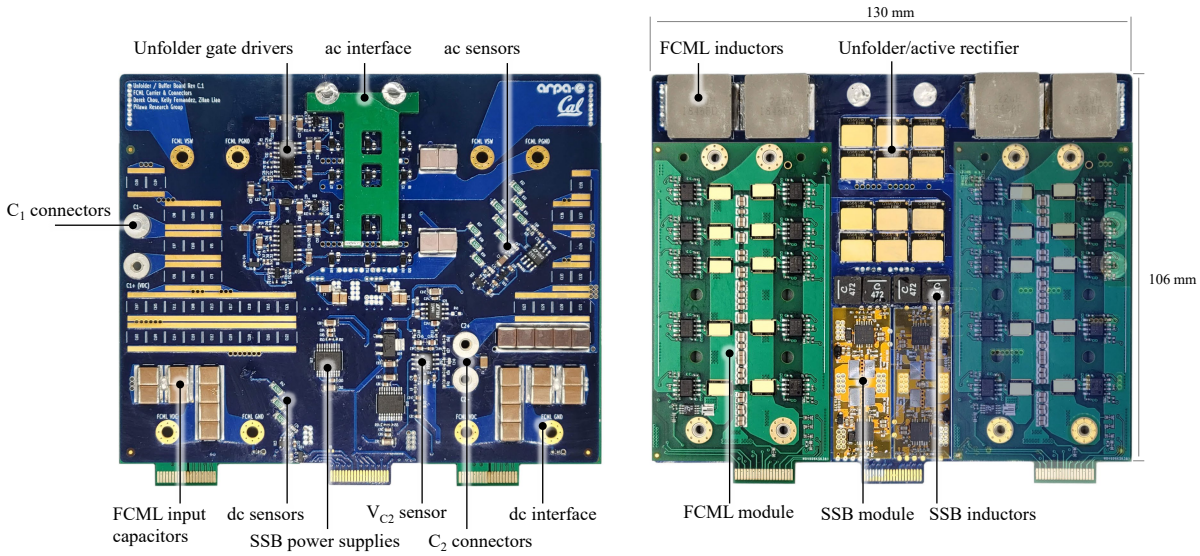

Figure 6.6: Unfolder/Buffer carrier board with core power conversion assembly stackup and detail.

Logic Level and Control Architecture

In an effort to match existing automotive standards, the electric vehicle charger system was designed to take a single 12 V_{dc} input and generate all necessary logic and control level power rails. For purposes of this section, all of the low-voltage power rails are referred to assuming dc voltages. Figure 6.7 details the low-voltage power distribution architecture. The 12 V input is passed through to each major power board (the FCML and SSB boards). A 6.5 V rail is generated from the 12 V rail with a Texas Instruments TPS561201 buck converter IC, which is also passed to each major power board. Furthermore, a 5 V rail is generated from the 12 V rail to power the TI F28379D ControlCARD.

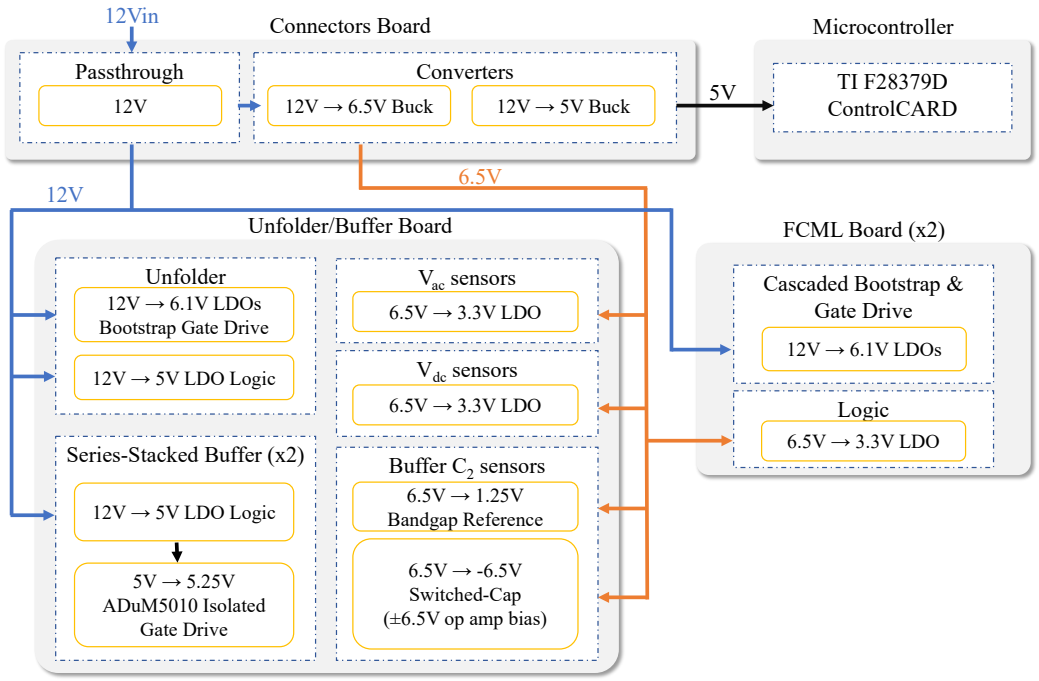

Figure 6.7: The low-voltage power distribution diagram of the electric vehicle charger.

On the FCML boards, the 12 V rail voltage is used to provide power to the cascaded bootstrap structures. The 6.5 V rail voltage is passed through LDOs to provide logic power voltage at 3.3 V logic levels.

On the Unfolder/Buffer board, there are three major structures of interest:

- The unfolder portion utilizes Si8274 gate drivers which run on 5 V logic. The gate drive structure is a conventional bootstrap with an LDO to regulate the 12 V down to 6.1 V suitable for driving the GaN Systems GS66516T FETs.
- The dual-interleaved series-stacked buffers portion require isolated gate drive supplies to drive the floating h-bridge switches. ADuM5010 supplies provide this isolated functionality.
- The ac and dc voltage sensing circuitry for V_{ac}, V_{dc}, V_{C2} requires a number of bias voltages, which are mostly generated with LDOs due to the low power, low noise requirements. The ±6.5 V bias required for the differential sensor for the floating capacitor C_2 is partially generated with a switched-capacitor converter.

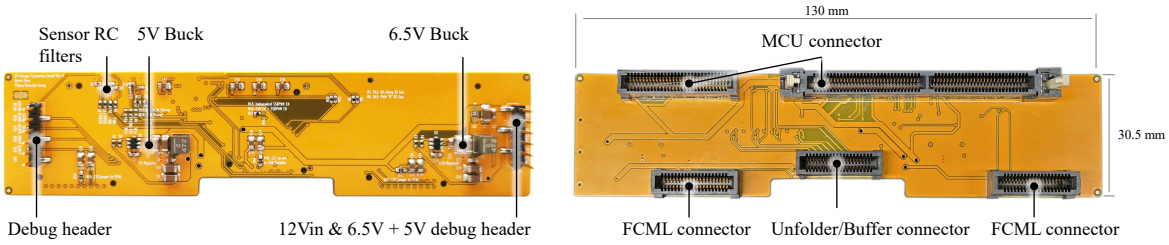

Figure 6.8: The signal connectors board of the electric vehicle charger system.

The signal connectors board (Fig. 6.8) plays an important role in system connectivity, as can be seen from the above low-voltage distribution architecture. It helps to constrain the Unfolder/Buffer board and FCML board spacing, while implementing the above 12 V to 6.5 V and 5 V distribution architecture. The logic and control supplies and sensors, implemented across all of the power boards as well as on the signal connectors board, are noted in Table 6.2.

Table 6.2: Logic-level components listing

Board Location	Component Function	Part No.	Parameters
Unfolder/Buffer Board	V_{C2} Sensor	LT1990	Differential Amplifier
	V_{C2} Sensor Bias	LT1144	Switched Capacitor Converter
	V_{C2} Sensor Reference	REF3012	Bandgap Reference
	V_{ac} and V_{dc} Sensors	LTC2051	Zero-Drift Amplifier
		LTC2050	Zero-Drift Amplifier
	Gate Drive LDOs	LP2985IM5-6.1	LP2985 6.1 V LDO
	SSB Isolated Power LDO	LM2937IMP-5.0	LM2937 Series 5.0 V LDO
	SSB Isolated Power Supplies	ADuM5010	Analog Devices isoPower
	Logic LDOs	TLV76050	TLV760 Series 5.0 V LDO
		TLV76033	TLV760 Series 3.3 V LDO
FCML Boards	Current Sensors	LT1999-20	Current Sense Amplifier
	Gate Drive LDOs	LP2985IM5-6.1	LP2985 6.1 V LDO
	Logic LDOs	TLV76050	TLV760 Series 5.0 V LDO
Signal Connectors Board	Logic Power	TPS561201	Step-Down Voltage Regulator

6.2 Experimental Results

In this section, the electric vehicle charger system is put through a multitude of tests to verify core functionality. A experimental bench setup (Fig. 6.9) is constructed to evaluate converter performance. This includes all of the test equipment and data acquisition hardware in addition to the thermal management, cold plate, and electronic and passive load elements.

A list of components used in the data acquisition and thermal management is noted in Table 6.3.

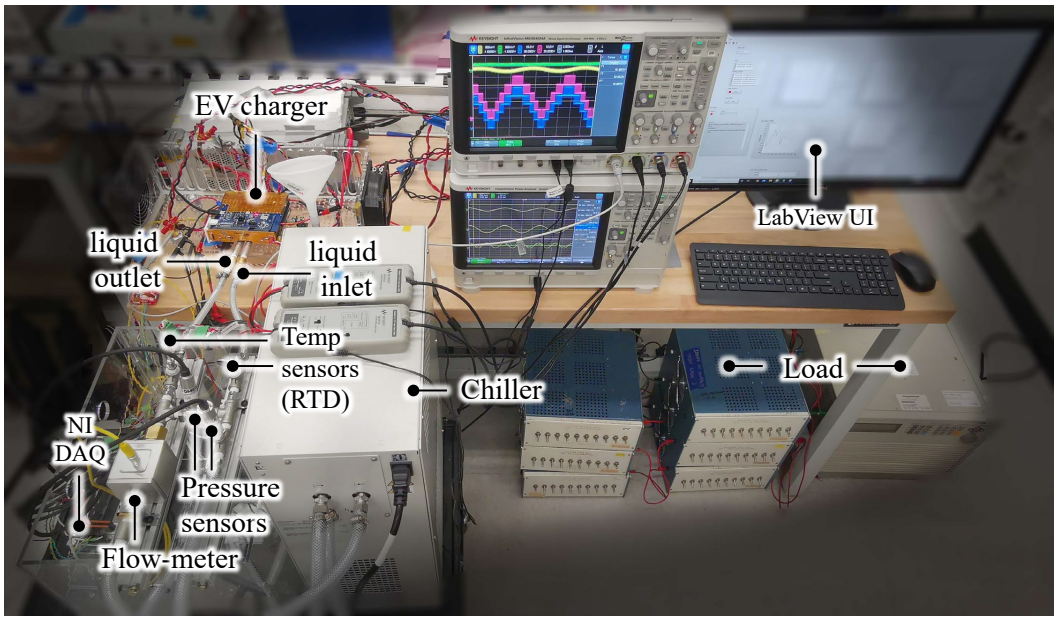

Figure 6.9: Experimental bench setup. (Image created in collaboration with Zitao Liao and Kelly Fernandez)

Table 6.3: Data Acquisition and Thermal Management Equipment. (Thermal data acquisition system created in collaboration with Kelly Fernandez and Raya Mahony)

Equipment	Description	Part Number
Chiller	Thermo Scientific Polar Series Accel 500	223422800
Flow meter	Kobold MIM Series Electromagnetic Flow Meter	MIM-1215HG5C3T0
RTDs	REOTEMP RTDs	AT-PX1123YLR4S1T2T
Data Acquisition Chasis	NI cDAQ-9189 CompactDAQ Chassis	785065-01
Analog Data Module	NI 9201	779013-01
RTD Data Module	NI 9216	785186-01

Bidirectional PFC and inverter control validation

The converter system is evaluated in the PFC mode as well as in the inverter mode. The converter was tested in the PFC mode with a 120 V_{ac} (low line) and a 240 V_{ac} (high line) input for a 400 V_{dc} output. The converter was also tested in the inverter mode with a 400 V_{dc} input and a 240 V_{ac} output up to 1 kW. For this series of tests, the system was tested without a heatsink. Figure 6.10 is the efficiency for the PFC and inverter cases; the high-line ac input PFC case achieves a peak efficiency exceeding 98.8%, the low-line ac input PFC case achieves a peak efficiency exceeding 97.6%, and the inverter case achieves a peak efficiency exceeding 98.4%. Figure 6.11 shows the THD on the ac side of the system running in PFC mode, and Fig 6.12 shows the measured power factor for 240 V_{ac} to 400 V_{dc}. In all test conditions, the input voltage and current are well in-phase (PF $\geq$ 0.99), and the switching node voltage shows good balancing between the flying capacitor voltages (v_{sw1}, Fig. 6.13) and good current balancing between interleaved FCML modules (i_{L1}, i_{L2}, Fig. 6.14). To validate the control for the SSB, film capacitors of smaller values than the full power specifications were used for C_1 (80 μF) and C_2 (68 μF) to simulate the voltage ripple effects at the full power level (6 kW). The dc bus ripple (Δv_{dc}) is about 15 V (3.75% of 400 V_{dc} – Fig. 6.13) at, 1.5 kW, high-line PFC input.

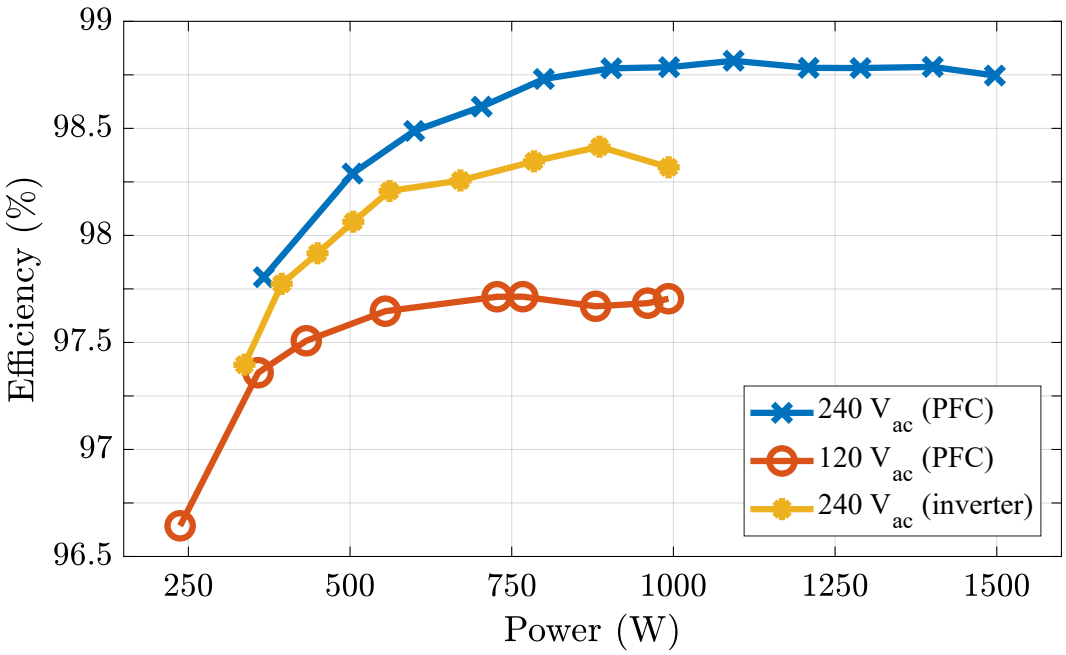

Figure 6.10: The efficiency of the system, PFC mode from 120 and 240 V_{ac} to 400 V_{dc}, and inverter mode from 400 V_{dc} to 240 V_{ac}.

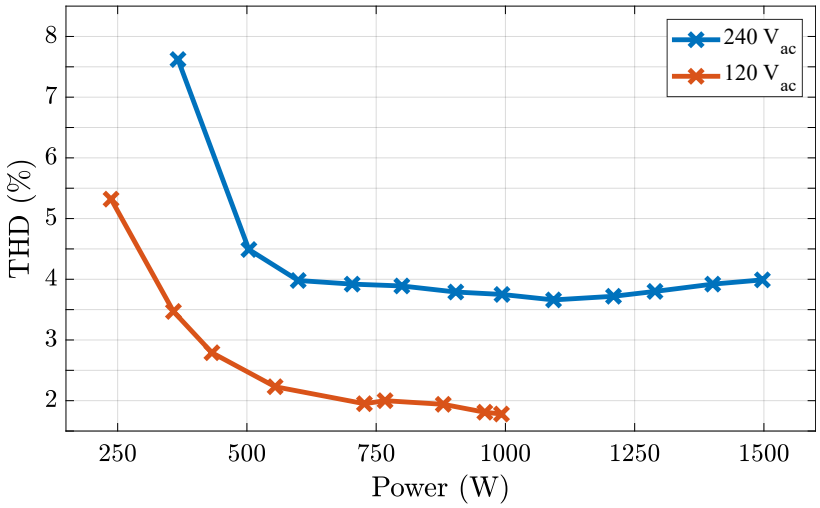

Figure 6.11: The THD of the system, PFC mode from 120 and 240 V_{ac} to 400 V_{dc}. (Plot created in collaboration with Zitao Liao)

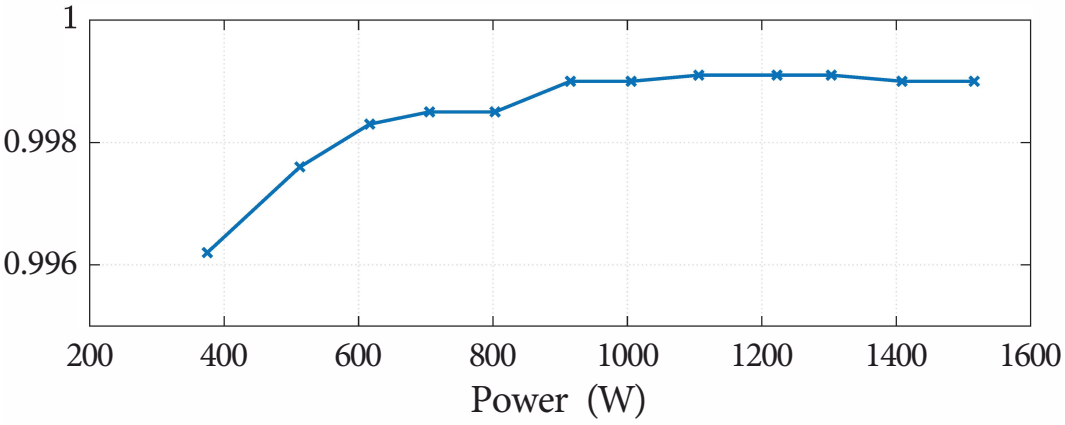

Figure 6.12: The measured power factor of the system, PFC mode 240 V_{ac} to 400 V_{dc}. (Plot created in collaboration with Zitao Liao)

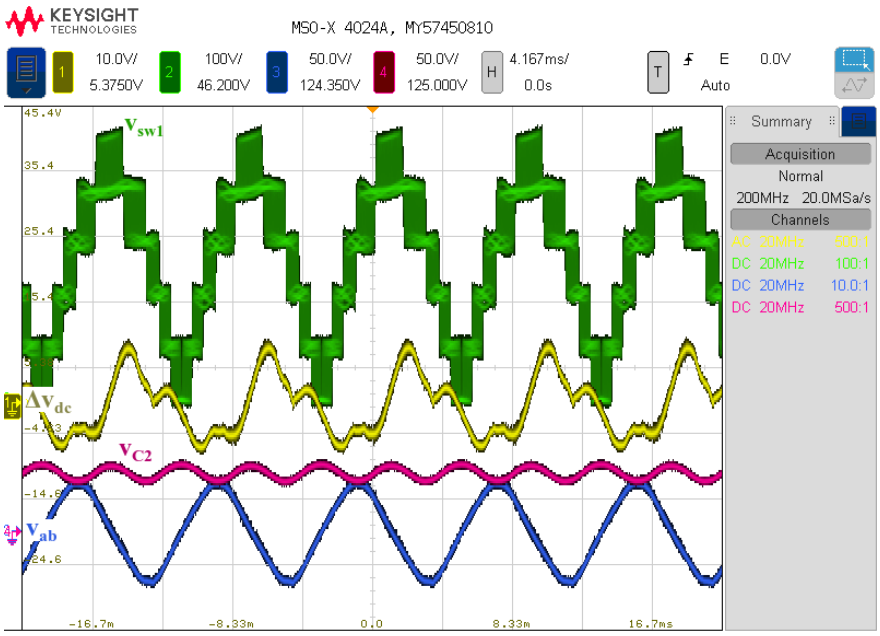

Figure 6.13: Typical SSB voltage waveforms for v_{c2} and v_{ab}, dc bus voltage ripple (ac coupled), and FCML switch-node of the system, PFC mode from 240 V_{ac} to 400 V_{dc}, 1.5 kW.

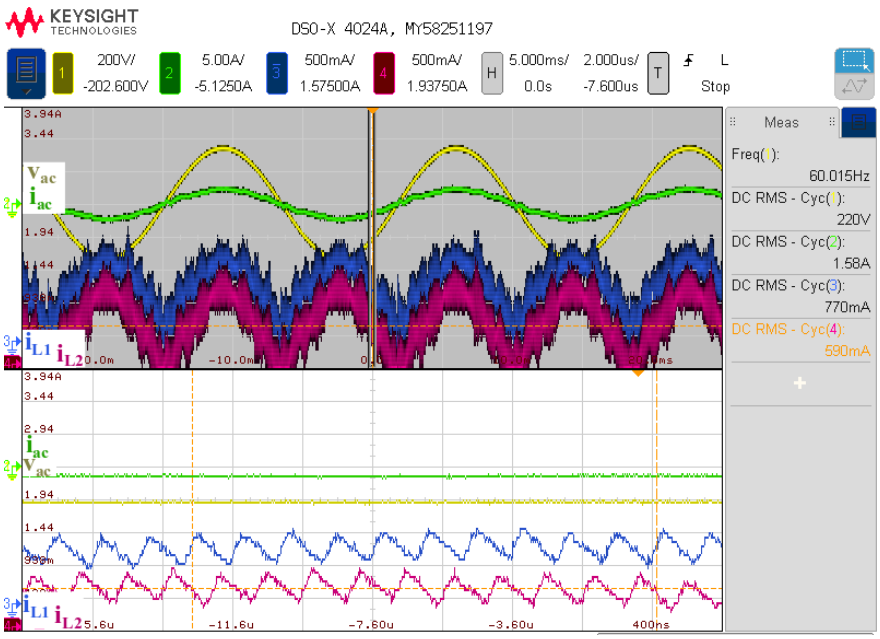

Figure 6.14: Typical current waveforms of the interleaved FCML, PFC mode from 240 V_{ac} to 400 V_{dc}, 375 W.

High power inverter mode results

The converter has been operated in the inverter mode at high power. A 400 V_{dc} input was used to produce a 240 V_{ac} output. The system was tested while connected to the cold plate system set at 25 °C.

Figure 6.16 shows the efficiency for the inverter stage up to 6.1 kW output. We note that the peak efficiency values are well above 98.5% for most of the range, with a peak above 99%. To capture such high conversion efficiencies, a high precision power analyzer (Keysight PA2201) was used. Oscilloscope traces of typical converter waveforms are shown in Fig. 6.15. The switch nodes of the FCMLs (v_{sw1} and v_{sw2}) are filtered to generate the ac voltage. The SSB twice-line frequency buffering waveform (v_{ab}) works to cancel the 120 Hz ripple on the dc bus. And the v_{C2} waveform demonstrates the SSB feedback control which draws enough real power into the circuit branch to keep the voltage on C_2 from decaying. An estimated loss breakdown of the converter operating at 6.1 kW is given in Fig. 6.17. Out of the 138.2 W of losses at 6.1 kW operating power, the FCML power stage is estimated to account for 66% of the losses; the SSB buffer stage is next at 17.1%, the unfolder is 9.7%, and the remainder is attributed to logic, control, and pcb traces. Using these loss figures and normalizing to the power processed, the operational efficiency of the converter is estimated at full power: the unfolder is estimated at 99.7%, the FCML power stage at 98.5%, and the SSB buffer stage at 99.6%. The key tested specifications and performance metrics are listed in Table 6.4.

Table 6.4: Key performance specifications for the 6.1 kW inverter test

Parameter	Value
DC Voltage	400 V_{dc}
AC Voltage	240 $V_{ac,rms}$
AC Current	25 A
AC Power	6.1 kW
Peak Efficiency	99.01% at 1.1 kW
Full Load Efficiency	97.7% at 6.1 kW
Switching Frequency	150 kHz
Effective Frequency @ v_{sw}	750 kHz
PCBA Rect. Box Dimensions	5.1" × 4.6" × 1.0" (12.95 cm × 11.68 cm × 2.54 cm)
Cold Plate Dimensions	5.1" × 3.6" × 0.375" (12.95 cm × 9.14 cm × 0.95 cm)
Without cold plate	
Weight	0.8 kg
Volume	23.46 in^3 (384.4 cm^3)
Volumetric Power Density (w/o. cold plate)	260 W/in^3 (15.9 W/cm^3)
Gravimetric Power Density	7.6 kW/kg
With cold plate	
Weight	1.1 kg
Volume	30.35 in^3 (497 cm^3)
Volumetric Power Density	201 W/in^3 (12.3 W/cm^3)
Gravimetric Power Density	5.5 kW/kg

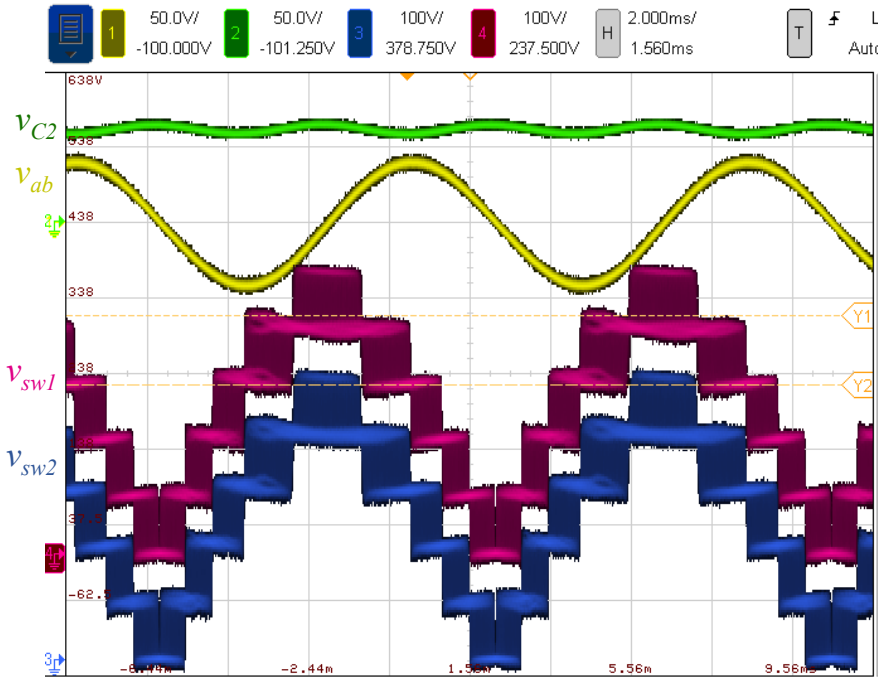

Figure 6.15: Typical SSB voltage waveforms for v_{c2} and v_{ab}, and FCML switching node voltages from 400 V_{dc} to 240 V_{ac}, 6.1 kW.

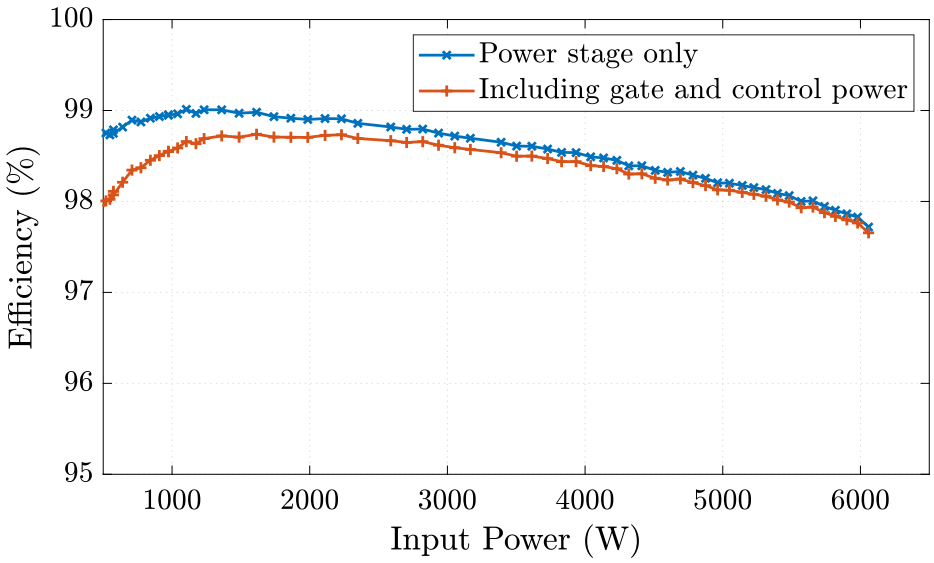

Figure 6.16: The efficiency of the 6.1 kW inverter test, 400 V_{dc} to 240 V_{ac}

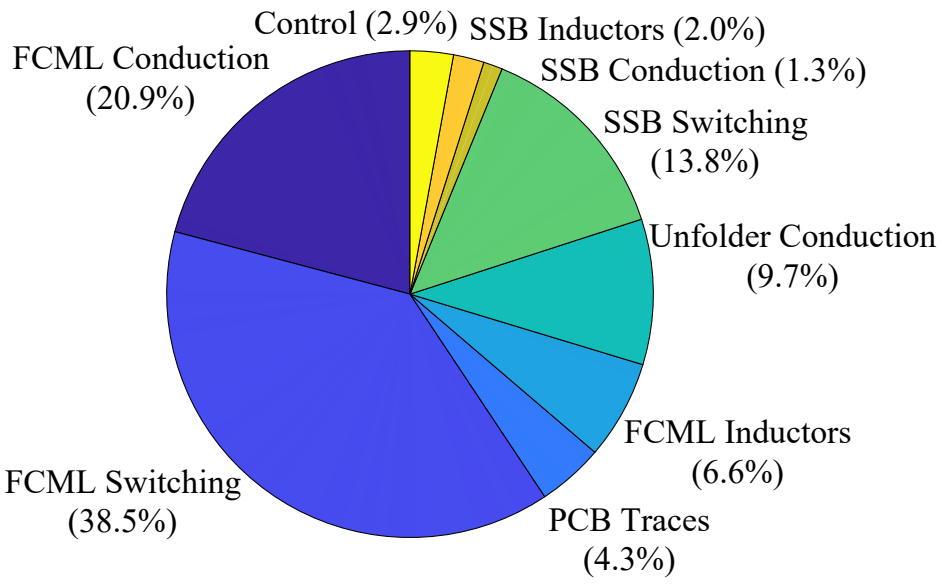

Figure 6.17: Estimated loss breakdown at 6.1 kW.

6.3 Conclusions

This chapter presents a Level II single-phase EV charger system featuring an interleaved flying-capacitor multilevel converter (FCML) stage and the series-stacked buffer topology. The charger converts between low- and high-line ac (120–240 V_{ac}) and 400 V_{dc} The design process of the overall system architecture, digital control, mechanical assembly, and thermal management is detailed. The hardware has been run at kilowatt levels demonstrating dc-ac inverter operation from 400 V_{dc} to 240 V_{ac}, building on the PFC and inverter demonstration of the architecture and control described in Chapters 4 and 5 and [4]. A peak power stage efficiency over 99% is observed (98.7% with control and logic losses included), and a maximum power of 6.1 kW is tested.

6.4 Acknowledgement

The information, data, or work presented in this chapter was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000900 in the CIRCUITS program monitored by Dr. Isik Kizilyalli. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

Chapter 7

On the Exploration of Converter Start-up

Transient situations are of interest in a flying-capacitor multilevel converter due to its reliance on capacitor balancing. Depending on the design margin, capacitor balancing can be critical to proper converter behavior. For a highly-optimized FCML converter such as the one used in Chapters 5–6, the maximum operating bus voltages exceed the switch voltage ratings, so the system relies on good capacitor voltage balancing to keep all of the core power semiconductors operating within these ratings. However, during the boundary condition of converter start-up, this periodic steady-state balancing is unlikely to be enforced without modification of the topology. This will result in undue voltage stress being applied across the switches during start-up, which requires either the semiconductor switches to be rated for higher voltages than the periodic steady-state voltage stresses, or it requires additional circuitry to block this excess transient voltage. In this chapter, a start-up sequence utilizing minimal additional hardware for the electric vehicle charger system is proposed and explored. Successful start-up for an operating condition converting from 110 V_{ac} to 400 V_{dc} is demonstrated, with the output ramping from a cold start of 0 V to a fully operational 400 V_{dc}.

This chapter is organized as follows. Section 7.1 discusses the FCML start-up from a high level. Section 7.2 provides a proposed solution to keeping the FCML switches within their rated voltage during the start-up procedure, whereby Section 7.3 runs through some hardware testing of the proposed solution. Section 7.4 provides some concluding remarks and future direction.

7.1 Flying Capacitor Multilevel Converter Start-up

In ideal conditions during periodic steady-state operation, the flying capacitor multilevel topology allows for power switches rated lower than the bus voltage to be used, due to the voltage division effect that is achieved in the FCML topology [19]. However, this relies on the fact that the capacitors are charged to fractions of the high side voltage (V_{dc} in Fig. 7.1).

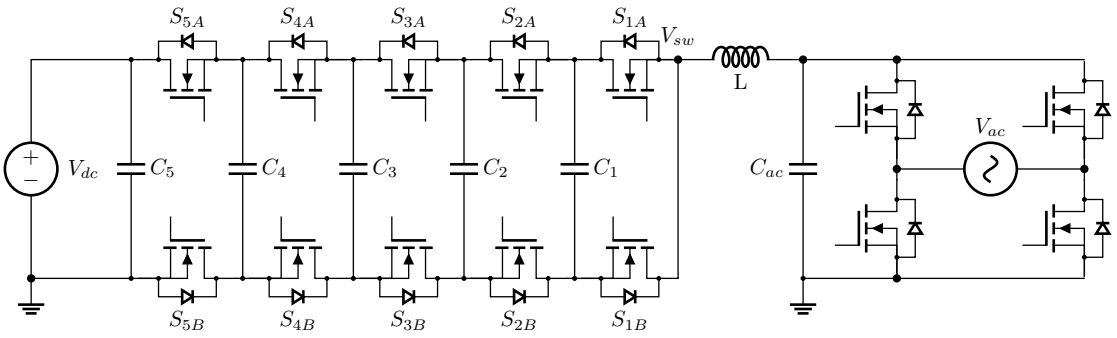

Figure 7.1: 6-level FCML and unfolder / rectifier schematic.

During the boundary start-up condition, this is unlikely to be true without some sort of pre-charge.

If we reduce an N-level FCML structure to a diode and capacitor network including the drain-source capacitances of the switches in the off-state (Fig. 7.2) and apply a voltage across V_{high} or across V_{low}, the resultant steady-state voltages are unfavorable for highly-optimized switch ratings. In this figure, we are noting that the N-level FCML contains switches of up to designations $S_{(N-1)A}$ and $S_{(N-1)B}$. For a 6-level converter, this would be S_{5A} and S_{5B}. The flying capacitors are designated in a similar fashion.

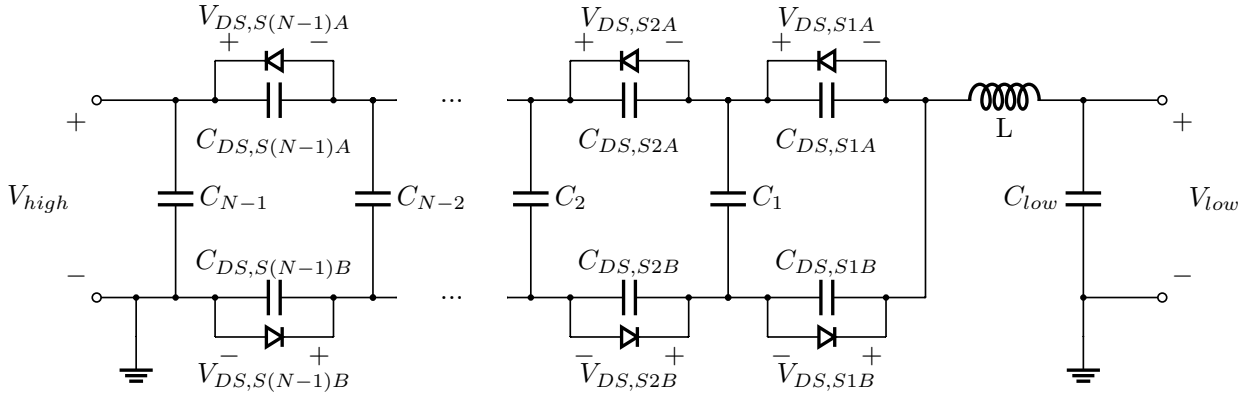

Figure 7.2: Schematic of N-level FCML start-up boundary condition, assuming all switches are inactive.

Since the flying capacitors as well as C_{low} are likely many orders of magnitude larger, in the $\sim \mu F$ range, compared to the drain-source capacitance, in the $\sim pF$ range, we can assume that the flying capacitors will not be charged to any significant voltage, due to the capacitor voltage divider network distributing charge mainly on the switch drain-source capacitances. We can then simplify the network in Fig. 7.2 to the network in Fig. 7.3. In

this schematic, the flying capacitors $C_{(N-1)}$ ... C_1 appear as virtual shorts in the start-up condition. Furthermore, the inductor L will also appear as a virtual short after some settling time when connecting either a source at V_{high} or V_{low}.

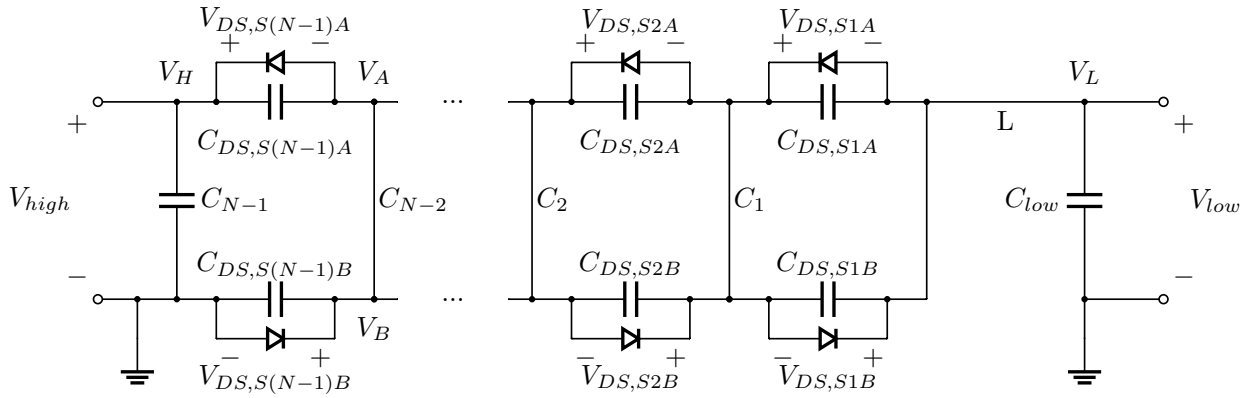

Figure 7.3: Schematic of N-level FCML start-up boundary condition, assuming all switches are inactive, with assumption that the flying capacitors C_{N-2} ... C_1 have a much higher capacitance value than the drain-source capacitances of the power semiconductor switches.

Analyzing for connecting a source V_{high} across C_{N-1} in Fig. 7.3 and assuming that $V_{low} =$ 0 V and that C_{low} is much larger than all of the semiconductor drain-source capacitances, we note that the voltages of interest are $V_{DS,S(N-1)A}$ and $V_{DS,S(N-1)B}$ since C_{N-2} creates a virtual short across the entire parallel network of all capacitors down to C_2, C_1 – this means that $V_A \approx V_B$. Also, the reverse conduction modes of the B switches in the stack past $S_{(N-1)B}$ (noted here, $S_{(N-2)B}$ ... S_2, S_1) ensures that any voltage evolved at $S_{(N-1)B}$ will cause reverse conduction that approximately connects the node V_B to the node V_L. Therefore the high-side switch sees approximately the full V_{high} voltage:

$$V_{DS,S(N-1)A} \approx V_{high} - (N-2) \cdot V_r \tag{7.1}$$

Where V_r is the reverse conduction voltage of the semiconductor switches and N is the number of levels in the N-level FCML. It also follows that the low-side switch has a maximum voltage:

$$V_{DS,S(N-1)B} \approx (N-2) \cdot V_r \tag{7.2}$$

Since the design parameter for the periodic steady-state voltage of $V_{S(N-1)A}$ is $V_{high}/(N-1)$, this full-voltage application can be quite catastrophic for the converter.

For the case of applying a voltage at V_{low}, the conduction modes in the switches in the FCML structure are reversed, with the A switches experiencing reverse conduction and causing the majority of the voltage V_{low} to be applied to the first low switch in the stack.

C_{N-1} (which is connected directly to V_{high}) is charged through the reverse conduction modes of the A switches which approximately connect V_L to V_H:

$$V_{high} \approx V_{low} - (N-1) \cdot V_r \tag{7.3}$$

Since C_{N-2} is a virtual short, it follows that:

$$V_{DS,S(N-1)B} \approx V_{low} - (N-2) \cdot V_r \tag{7.4}$$

and

$$V_{DS,S(N-1)A} = -V_r \tag{7.5}$$

Again since the design parameter for the periodic steady-state voltage of $V_{S(N-1)B}$ is $V_{high}/(N-1)$, this full-voltage application can be catastrophic for the converter, and is made worse especially as $V_{low,max}$ approaches V_{high}.

Given the above analysis, although the FCML switch ratings would ideally be designed for the periodic steady-state operation where the flying capacitors are charged to the proper fractional voltages, the boundary condition in which the flying capacitors are starting uncharged essentially requires that the switches be over-rated to withstand start-up, or that some external circuitry be added to insulate the FCML switches from the higher voltages.

Testing the periodic steady-state operation of the FCML converter plus unfolder rectifier in either ac-dc or dc-ac mode, power supplies are often started at a low voltage in comparison to the final operating points. They are then ramped to the proper levels. During the ramping process, the high-frequency switching operation of the FCML stage coupled with the natural balancing feature of the topology keeps the switches operating within the proper voltage ratings [19], [61]. Further methods such as modifying the base phase-shifted PWM operation or applying active balancing techniques can be applied to increase the speed of balancing but do not address the start-up condition [45], [62], [63]. A standard start-up structure consisting of a small switch connecting a current-limiting resistor, along with a larger, high-current switch is explored in [10], [62], [64]–[66]. More-advanced start-up structures and control are explored in [3], [67], [68], which can involve circuitry to charge the flying capacitors or ways of controlling the FCML structure itself to provide a soft start. In this work, we aim to start from the ac line voltage with minimal addition of extra components and control, and ideally with only semiconductor switches.

7.2 Proposed Solution

To block the voltages V_{dc} and V_{ac} from the FCML stage, floating MOSFET switches (Fig. 7.4) are inserted into the circuit, labeled as S_{ac} and S_{dc} in Fig. 7.5. The start-up switch is implemented as an isolated 10.5 V_{dc} supply connected to an Si8271 gate driver, which drives four parallel 650 V silicon MOSFETs [51]. The addition of the pair S_{ac} and D_{ac} and some

filtering elements (Fig. 7.5) creates a voltage and current limiting structure not unlike a four-switch buck-boost converter, which is used to limit the voltage across the FCML converter switches during a start-up sequence. Table 7.1 lists the components used in the floating MOSFET implementation, as well as the diode used in the start-up switch implementation.

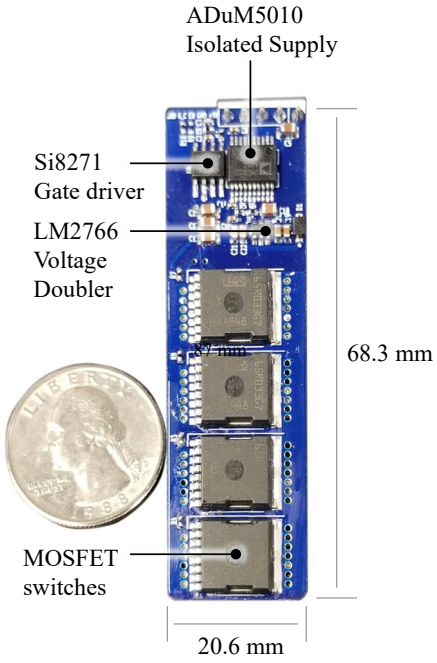

Figure 7.4: MOSFETs and supporting circuitry for floating switch implementation.

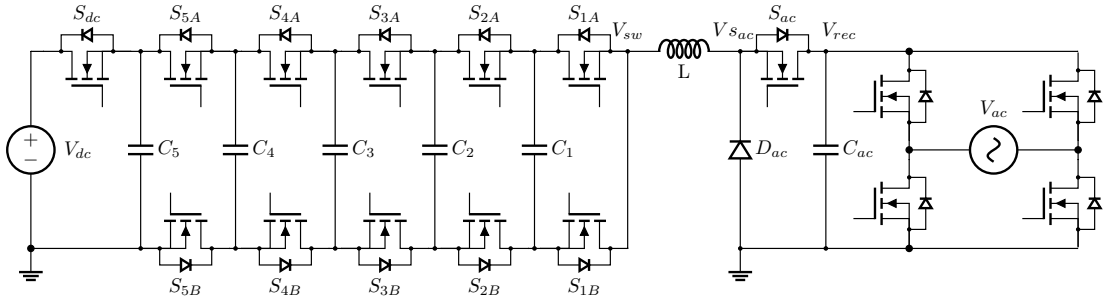

Figure 7.5: 6-level FCML and unfolder / rectifier schematic with added start-up switches and supporting circuitry.

Table 7.1: Component listing

Component	Part No.	Parameters
MOSFETs	Infineon IPT65R033G7	650 V, 33 $m\Omega$ × 4 (parallel)
Diode	ON Semiconductor MUR160G	600 V, 1A
Isolated Gate Driver	Si8271GB-IS	Silicon Labs Si827x Series
Isolated Power Supply	ADuM5010	Analog Devices isoPower
Voltage Doubler	TI LM2766	Switched Capacitor Voltage Converter

When the EV charger system (configured as Fig. 7.5) is connected to an ac source, the 650 V MOSFETs block the full ac line voltage. A start-up sequence is proposed below using the modified hardware of Fig. 7.5. A logic diagram for soft-starting the FCML stage is shown in Fig. 7.6. The proposed start-up sequence is as follows:

- Determine phase angle of ac voltage. Wait for phase-locked loop (PLL) lock. Power factor correction duty ratio calculations are active for the FCML stage during this phase.
- When the PLL is locked onto the ac line waveform, ramp the duty ratio % of S_{ac} until the voltage V_{dc} is greater than or equal to the maximum line voltage on the ac side. For a single-phase sinusoidal input, this will be $V_{ac,rms} \cdot \sqrt{2}$
- Turn on S_{ac} fully (100% duty ratio).
- Ramp the voltage boost ratio such that the voltage V_{dc} is equivalent to the target dc voltage.
- Once the target dc voltage is reached, turn on S_{dc}, start the series-stacked buffer, and ramp the output power to the desired level.

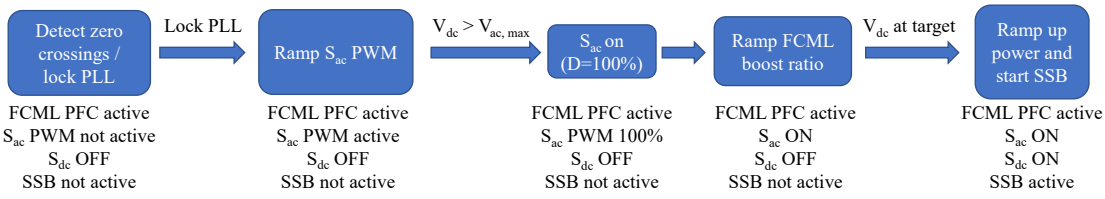

Figure 7.6: FCML ac-dc converter ac side start-up logic.

7.3 Hardware Results

In this section, hardware results detailing a demonstration of FCML start-up are presented. It is important to note that the series-stacked buffer start-up is not explored here; that particular aspect of system start-up is noted as a key future step in this work. Instead, a ∼2.7 mF electrolytic capacitor bank is used to buffer the 120 Hz twice-line frequency ripple of the ac power and to decouple the effect of dc bus induced FCML flying capacitor imbalance [45]. The electric vehicle charger system of Chapters 5 and 6 is adapted to include the switch hardware shown in Fig. 7.4. In the first demonstration, a dc voltage is applied at the V_{rec} node to verify the ramping functionality of the FCML boost stage. In the second demonstration, an ac voltage is applied at the V_{ac} source to showcase that the FCML power factor correction (PFC) can work together with the start-up switch hardware to safely ramp up the voltages on all of the capacitors of the FCML while keeping the 100 V switches within their rated voltage. Fig. 7.7 is a schematic of the start-up demonstration configuration. In a system with a battery connected, there would also be a switch in between V_{dc} and the core FCML stage (S_{5A} in this schematic); this switch is omitted for the purposes of this exploration; a 1 kΩ power resistor is used instead as a static load. The switching frequency of the FCML was 150 kHz, so the start-up switch frequency was set at 27.97 kHz, a number relatively prime with 150 kHz to prevent any undue interactions between the two portions of the circuit.

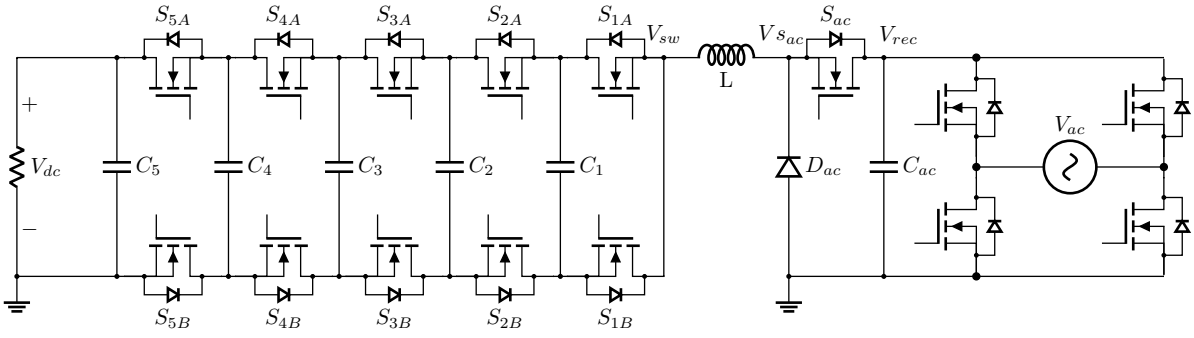

Figure 7.7: 6-level FCML and unfolder / rectifier demonstration with added ac-side start-up switch and supporting circuitry.

170 V_{dc} to 400 V_{dc} Start-up Test

The converter assembly was configured as defined in Fig. 7.7 and tested in the dc-dc mode to verify capacitor balancing and boost ratio ramping. A dc voltage of 170 V was applied at the node V_{rec}, and the FCML stage was set to start at a constant boost ratio of 1.1×, with the active rectifier circuitry inactive.

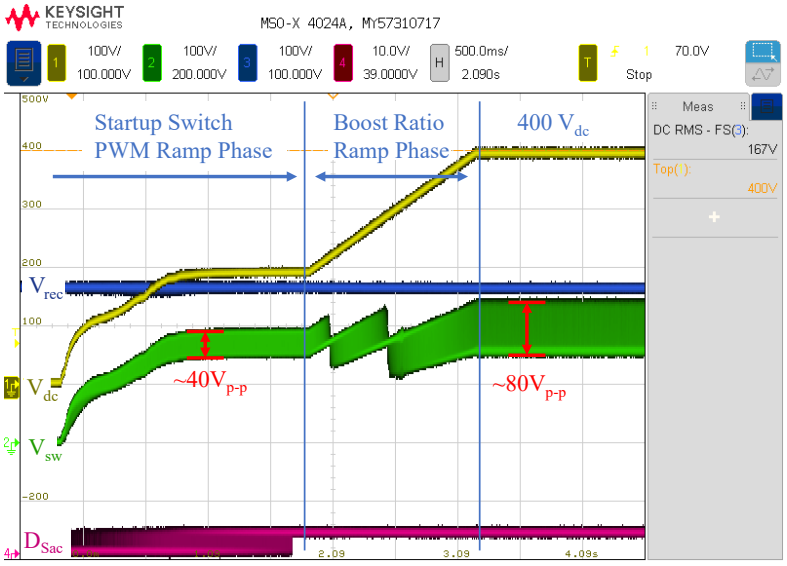

Figure 7.8: dc start-up waveforms from 170 V_{dc} to 400 V_{dc}

After the start-up switch S_{ac} duty ratio was ramped from 0 to 100%, the FCML boost ratio was ramped until the output reached 400 V_{dc}. Figure 7.8 shows the evolution of the dc output voltage with respect to the start-up states. As can be seen from the V_{sw} node trace, the envelope of green is indicative of the voltage stress across the switches, as the converter selects between combinations of different capacitors. If these bands are well-defined, then one can deduce that the capacitors are well-balanced, as the PSPWM method selects between charging and discharging all of the flying capacitors over a full switching cycle.

If we inspect the detailed operation of V_{sw}, the switch node of the FCML stage, the characteristic PWM voltage waveform is observed. As the FCML topology divides the possible selections of its switch node voltages between multiples of $V_{dc}/(N-1)$, this means that for a 6-level converter, the voltages that can be selected for V_{sw} are multiples of $V_{dc}/5$. For a 400 V_{dc} bus, the flying capacitors will be charged to 80, 160, 240, and 320 V.

During operation, if a voltage between multiples of $V_{dc}/5$ is desired, the PSPWM operation ensures that the switch states will select between two adjacent multiples, at some effective duty ratio that averages to the desired voltage. For example, for a desired output voltage of 10% of V_{dc}, the voltage will toggle between 0 and $V_{dc}/5$ at an effective duty ratio of 50% [47]. And, for a desired output voltage of 85% of V_{dc}, the voltage would toggle between V_{dc} and $4V_{dc}/5$ with an effective duty ratio of 25%. The ripple frequency on the inductor would be equivalent to $(N-1)\times$ the base switching frequency. Sweeping through duty ratios as seen above would change the overall selection of output voltage and therefore also the effective duty ratio. For the FCML converter running in boost mode as in Fig. 7.8, as we

ramp through multiples of $V_{dc}/5$, the effective duty ratio seen at the inductor sweeps through inflection points selecting different voltage level multiples of $V_{dc}/5$ as the dc voltage ramps up.

110 V_{ac} to 400 V_{dc} Start-up Test

Following the dc-dc mode verification, the converter assembly was kept in the same configuration as defined in Fig. 7.7 and tested in the ac-dc mode to verify capacitor balancing and boost ratio ramping in conjunction with the PFC control loop. This time, an ac voltage of 110 V_{ac} was applied at the source V_{ac}, and the FCML PFC stage was set to start with a target dc voltage just above the maximum sensed ac voltage, roughly a boost ratio of 1.1×. After the start-up switch duty ratio ramp is completed, this boost ratio target is increased until the target dc output voltage of 400 V_{dc} is reached. The active rectifier was also set to an active state to prevent excessive losses. This demonstration implements the PLL lock, start-up switch ramp, and boost ratio ramp phases of the logic block diagram of Fig. 7.6. Figure 7.9 shows the ramp to 400 V_{dc} from a cold start of 0 V_{dc}, from the ac input. It is important to note that the voltage and current loops have not been optimized for this start-up demonstration, and these loops could be tuned to ramp the output dc voltage more quickly.

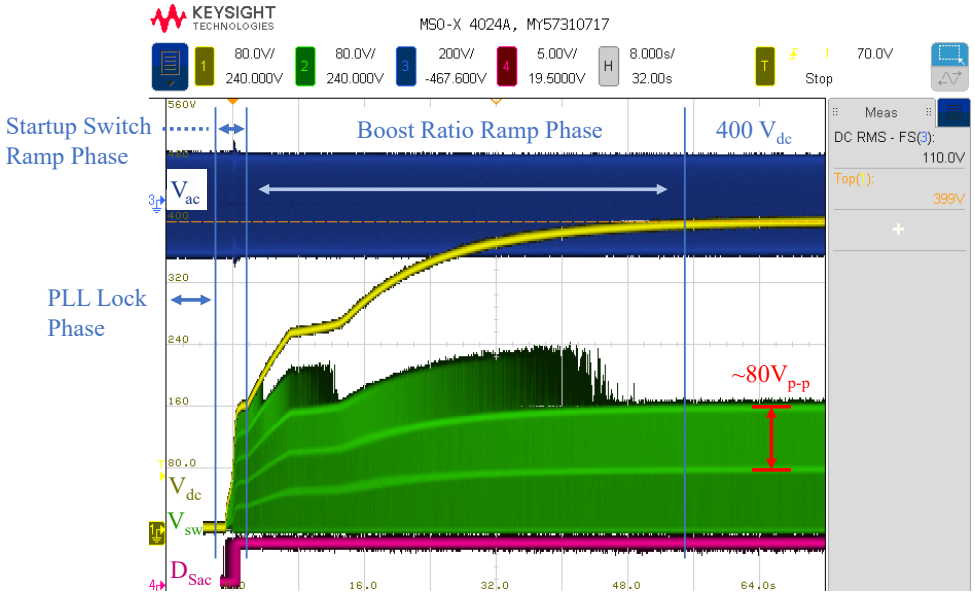

Figure 7.9: ac start-up waveforms from 110 V_{ac} to 400 V_{dc}.

Fig. 7.10 shows the detailed operation at V_{ac} = 110 and V_{dc} = 400. Here, we note the characteristic stepped PWM voltage waveform at the switch node V_{sw}. This is the

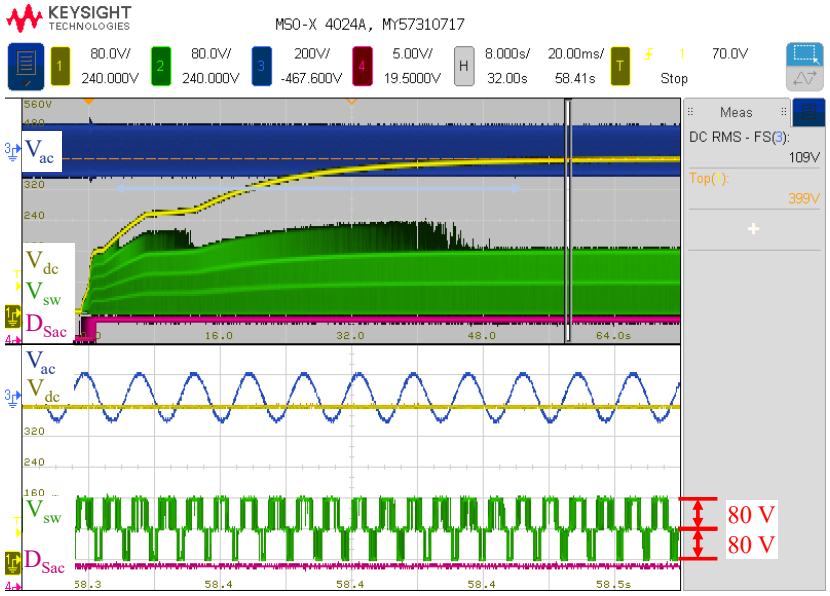

Figure 7.10: ac start-up waveforms from 110 V_{ac} to 400 V_{dc}, stepped waveform detail.

converter selecting between voltage states to create a switch node voltage that averages to the equivalent of the rectified 110 V_{ac} waveform.

For a 400 V_{dc} output, the flying capacitors in the FCML stage are charged to 80, 160, 240, and 320 V. Therefore, for a 110 V_{ac} input, which has a maximum of about 156 V, the FCML switch node will sweep through operation modes that select between 0, 80, and 160 V. We observe in Fig. 7.10 that the duty ratio PWM operation sweeps between these voltage levels to match the 110 V_{ac} input.

7.4 Conclusions and Future Work

This chapter presents a methodology for starting a FCML-based EV charger system from the ac line voltage, whereby the only necessary additional components are a pair of semiconductor switches for the ac side, implemented with a floating MOSFET and a regular diode, and a single switch for the dc side, implemented with a floating MOSFET. The FCML converter is analyzed in the start-up state, noting that with fully-discharged flying capacitors, the switches are required to be over-rated to withstand start-up conditions. A hardware prototype is adapted to demonstrate a cold start with live 110 V_{ac} line voltage, whereby the output is ramped from 0 V_{dc} to 400 V_{dc} while keeping all of the flying capacitors in the FCML stage balanced and therefore all of the 100 V-rated switches within their voltage ratings.

Noting that the control loops were not tuned to provide the optimal start-up speed, work could be done to explore the required modifications to both the PFC control loops implemented in Chapters 5 and 6. Also, the integration of the start-up switches and full EV charger system requires an electrical platform hardware revision to integrate fully into the assembly. Finally, as the controller for this start-up method is made in addition to the PFC and inverter control of Chapters 5 and 6, the overall software architecture could require some optimization to continue to fulfill control loop timing constraints.

It is important to note that the series-stacked buffer converter start-up is not integrated into this chapter. This is because the default start-up state of the bulk capacitor C_1 in the series stacked buffer (as shown in Chapter 3, Fig. 3.2) is that it is charged to the full bus voltage, V_{dc}, while the energy storage capacitor C_2, is not charged at all. Therefore, the full-bridge converter in the SSB is actually able to withstand a 400 V_{dc} bus and ramp up gracefully to the proper operating point once the FCML is started.

Chapter 8

Conclusions

8.1 Conclusions

In this work, methods to improve overall power converter system density are explored. A single-phase ac-dc Level II electric vehicle charger is used as an example power electronics system which has several key components that could be minimized. Such a charger is usually required to incorporate two major functions in the ac-dc rectification mode: power factor correction (PFC) and twice-line frequency buffering. Looking to a future of more-electric vehicles and renewable energy usage, bidirectional functionality is also desirable: batteries in electric vehicles could provide ancillary grid support as backup energy storage and release on demand. Therefore, the power stage and energy buffer stage can be run in reverse, with the PFC stage running as an inverter stage to push energy from a dc battery into an ac sink. Opportunities for improvement are identified as including the boost stage inductor and the energy buffer stage capacitor: The boost PFC stage conventionally uses two power semiconductor switches to control the current in a physically-large inductor, and the energy buffer is conventionally implemented with a low-cost but physically-large electrolytic capacitor bank.

To address the physical size of the boost inductor and of the energy buffer capacitors, several major ideas are applied. High utilization of capacitor energy density in high power density converter topologies leads to an overall smaller assembly size. The flying-capacitor multilevel (FCML) topology is proven to perform at the Level II charging power level in Chapter 4 in a hardware demonstration of an interleaved 6-level design. With this hardware, mechanical and thermal analysis and integration techniques are also demonstrated. Chapters 5 and 6 are the realization of the electric vehicle charger system design and integration. The FCML topology is integrated with the series-stacked buffer (SSB) topology in a full system prototype featuring two interleaved FCML modules with two interleaved SSB modules. Mechanical and thermal design for the charger system focused on a high utilization of 3-D space, while keeping assembly processes within conventional bounds to be able to contract-manufacture all of the major power boards. The full system is verified in both the power factor correction (PFC) and the inverter modes. It is then run to high power

in the inverter mode as a system functionality test and performance test for the cold plate liquid cooling loop designed and built for this application. The prototype achieves a power density of 201 W/in^3 (12.3 W/cm^3) at 6.1 kW, and maintains an efficiency of above 98% for the majority of its operational range. Finally, Chapter 7 takes the hardware platform from Chapters 5 and 6 and adapts it to demonstrate a practical aspect – converter start-up – with minimal addition of extra hardware. By adding two floating high-voltage switches as well as a single rectifier diode, capability to start from a completely discharged state is realized. A demonstration of line-voltage ac side start-up into a static load is performed, noting a soft-start behavior in the FCML stage as the capacitor voltages ramped up to the expected values.

8.2 Future Work

As alluded to in Chapter 7, there are many of threads of exploration that have been generated by this body of work. The work of Chapter 4 is notably less conventionally manufacturable than the work of Chapters 5 and 6, but even the newest (to date) revision hardware prototypes were not designed for any particular ease in assembly; instead, the focus of achieving a maximum power density within reason while retaining ability to contract-manufacture each module circuit board with conventional means resulted in a non-trivial full system assembly. It is possible that this is unavoidable due to the increasing amount of integration of power electronics, and that future models may actually be even more difficult to assemble. However, it is also possible that the integration can be managed by streamlining module-to-module assembly.

Exploration of the different methods of thermal management is limited to only conventional air-cooled heatsinks and liquid-cooled aluminum cold plates in this work. This provides a baseline for the expected performance of a high power density prototype, but there is even more performance to be gained from several direct liquid and evaporation cooling methods currently under investigation. It is important to mention that the thermal interface material (TIM) is an oft-noted bottleneck in thermal performance. While this work did not aggressively test the thermal boundaries of the power semiconductors used, thermal constraints often limit high-performance power converters that do not have any sort of specially-designed thermal management. Despite promising figures without a heatsink, only after the attachment of either an air-cooled heatsink or the liquid-cooled cold plate did the converters presented achieve the high power density figures reported herein. Since TIM is required to take up any mechanical alignment mismatch between devices and thermal management, tightening the mechanical tolerance in the assembly to minimize any added material will equate to higher converter thermal management efficiency. With tighter mechanical tolerances comes a requirement of overall more stringent mechanical and thermal design and verification.

The integration of the interleaved FCML and SSB stages has provided an excellent demonstration of a high power density converter able to be constructed with conventional

manufacturing techniques while still achieving excellent power density figures. This work has focused mostly on the hardware aspect of the power converter platform, but control and boundary condition handling are also an active area of study. Since the boost PFC inductor has shrunken by about 25× as compared with a conventional design, the control bandwidth requirement for the PFC stage has increased significantly. There are many switches in this combined FCML/SSB topology with precise switch timing requirements that could necessitate the usage of field-programmable gate arrays (FPGAs) in the near future to manage the control signal complexity, with application-specific integrated circuits (ASICs) designed to generate these signals perhaps on the longer time horizon. The microcontroller used in this work was run at its maximum rated frequency, and while the control loop may not have been completely optimal, the bandwidth requirements were sizable and the interrupt timing was tight enough to require some amount of instruction execution timing analysis and optimization. Furthermore, only the periodic steady-state operation of the electric vehicle charger system were extensively tested. The ac side start-up behavior has been explored, but performance in other transient situations, for example, step-loading behavior, light-load behavior and control, etc. remains unexplored. An integrated SSB start-up solution with the FCML converter has not been explicitly demonstrated yet, and exploration of fault behavior of the FCML converter is ongoing.

Overall, this work has provided demonstrations of the electrical, mechanical, and thermal integration of the FCML and SSB topologies. Practical implementations of high power density strategies are already making it to the broader market in some high performance applications, and the topologies presented here are showing great promise in further pushing the boundaries of power density.

Bibliography

[1] D. Chou, K. Fernandez, and R. C. N. Pilawa-Podgurski, "An Interleaved 6-Level GaN Bidirectional Converter for Level II Electric Vehicle Charging," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 594–600. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8721971.

[2] H. Kim, H. Chen, D. Maksimović, *et al.*, "Sic-mosfet composite boost converter with 22 kw/l power density for electric vehicle application," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 134–141. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7930684.

[3] N. Pallo, S. Coday, J. Schaadt, P. Assem, and R. C. N. Pilawa-Podgurski, "A 10-Level Flying Capacitor Multi-Level Dual-Interleaved Power Module for Scalable and Power-Dense Electric Drives," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 893–898. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9124531.

[4] Z. Liao, D. Chou, K. Fernandez, Y. Syu, and R. C. N. Pilawa-Podgurski, "Architecture and Control of An Interleaved 6-Level Bidirectional Converter With an Active Energy Buffer for Level-II Electric Vehicle Charging," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4137–4142. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9236108.

[5] D. Chou, Z. Liao, K. Fernandez, *et al.*, "An Interleaved 6-level GaN Bidirectional Converter with an Active Energy Buffer for Level II Electric Vehicle Charging," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Jun. 2021.

[6] H. J. Chae, W. Y. Kim, S. Y. Yun, Y. S. Jeong, J. Y. Lee, and H. T. Moon, "3.3kW on board charger for electric vehicle," in *8th International Conference on Power Electronics - ECCE Asia*, 2011, pp. 2717–2719. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5944762.

[7] B. Whitaker, A. Barkley, Z. Cole, *et al.*, "A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2606–2617, 2014. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6587577.

[8] J.-S. Lai, L. Zhang, Z. Zahid, N.-H. Tseng, C.-S. Lee, and C.-H. Lin, "A high-efficiency 3.3-kW bidirectional on-board charger," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, 2015, pp. 1–5. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7361609.

[9] Z. Liu, B. Li, F. C. Lee, and Q. Li, "High-Efficiency High-Density Critical Mode Rectifier/Inverter for WBG-Device-Based On-Board Charger," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9114–9123, 2017. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7951033.

[10] Y. Lei, C. Barth, S. Qin, *et al.*, "A 2 kW, single-phase, 7-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, Nov. 2017. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7811253.

[11] *98.6% Efficiency, 6.6-kW Totem-Pole PFC Reference Design for HEV/EV Onboard Charger*, Texas Instruments, Mar. 2018. [Online]. Available: https://www.ti.com/tool/TIDA-01604.

[12] D. Neumayr, D. Bortis, and J. W. Kolar, "The essence of the little box challenge-part A: Key design challenges & solutions," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 2, pp. 158–179, 2020. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9135030.

[13] K. Huang, P. Kanaroglou, and X. Zhang, "The design of electric vehicle charging network," *Transportation Research Part D: Transport and Environment*, vol. 49, pp. 1–17, 2016. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1361920915300778.

[14] P. K. H. Dost, P. Spichartz, and C. Sourkounis, "Charging behavior of users utilizing battery electric vehicles and extended range electric vehicles within the scope of a field test," *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 580–590, Jan. 2018. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8054733.

[15] S. Habib, M. M. Khan, K. Hashmi, M. Ali, and H. Tang, "A comparative study of electric vehicles concerning charging infrastructure and power levels," in *2017 International Conference on Frontiers of Information Technology (FIT)*, Dec. 2017, pp. 327–332. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8261059.

[16] F. H. Malik and M. Lehtonen, "Minimization of queuing time of electric vehicles at a fast charging station," in *2017 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe)*, Sep. 2017, pp. 1–6. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8260126.

[17] P. Y. Kong and G. K. Karagiannidis, "Charging schemes for plug-in hybrid electric vehicles in smart grid: A survey," *IEEE Access*, vol. 4, pp. 6846–6875, 2016. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7586042.

[18] D. R. Pinto, V. T. Arioli, G. R. T. Hax, R. T. Borges, and W. W. Teixeira, "Analysis of the impact on power quality during the recharge of electric vehicles and vehicle-to-grid functionality," in *2017 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe)*, Sep. 2017, pp. 1–6. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8260270.

[19] T. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, Jun. 1992, 397–403 vol.1. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=254717.

[20] Jih-Sheng Lai and Fang Zheng Peng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509–517, 1996. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=502161.

[21] S. Qin, Y. Lei, C. Barth, W. Liu, and R. C. N. Pilawa-Podgurski, "A High Power Density Series-Stacked Energy Buffer for Power Pulsation Decoupling in Single-Phase Converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4905–4924, 2017. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7547303.

[22] Z. Liao, Y. Lei, and R. C. N. Pilawa-Podgurski, "Analysis and design of a high power density flying-capacitor multilevel boost converter for high step-up conversion," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4087–4099, 2019. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8416764.

[23] Z. Liao, D. J. Lohan, N. C. Brooks, J. T. Allison, and R. C. N. Pilawa-Podgurski, "A systematic design methodology for series-stacked energy decoupling buffers based on loss–volume pareto optimization," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2192–2205, 2020. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9064556.

[24] C. B. Barth, T. Foulkes, I. Moon, Y. Lei, S. Qin, and R. C. N. Pilawa-Podgurski, "Experimental Evaluation of Capacitors for Power Buffering in Single-Phase Power Converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7887–7899, 2019. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8516319.

[25] T. Modeer, C. Barth, N. Pallo, W. H. Chung, T. Foulkes, and R. Pilawa-Podgurski, "Design of a GaN-based, 9-level flying capacitor multilevel inverter with low inductance layout," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar.

2017, pp. 2582–2589. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7931062.

[26] S. Qin, Y. Lei, Z. Ye, D. Chou, and R. C. N. Pilawa-Podgurski, "A High-Power-Density Power Factor Correction Front End Based on Seven-Level Flying Capacitor Multilevel Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1883–1898, Sep. 2019. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8444977.

[27] Z. Liao, N. C. Brooks, Z. Ye, and R. C. N. Pilawa-Podgurski, "A High Power Density Power Factor Correction Converter with a Multilevel Boost Front-End and a Series-Stacked Energy Decoupling Buffer," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 7229–7235. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8557924.

[28] S. Qin, Y. Lei, C. Barth, W.-C. Liu, and R. Pilawa-Podgurski, "Architecture and control of a high energy density buffer for power pulsation decoupling in grid-interfaced applications," in *Control and Modeling for Power Electronics (COMPEL), 2015 IEEE 16th Workshop on*, Jul. 2015, pp. 1–8. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7236439.

[29] S. Qin, Y. Lei, C. Barth, W.-C. Liu, and R. C. Pilawa-Podgurski, "A high-efficiency high energy density buffer architecture for power pulsation decoupling in grid-interfaced converters," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, Sep. 2015, pp. 149–157. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7309682.

[30] N. C. Brooks, Z. Liao, and R. C. N. Pilawa-Podgurski, "A Digital Implementation of PLL-Based Control for the Series-Stacked Buffer in Front-End PFC Rectifiers," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2018, pp. 1–7. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8460145.

[31] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Design of a GaN-Based Interleaved Nine-Level Flying Capacitor Multilevel Inverter for Electric Aircraft Applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12 153–12 165, 2020. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9075380.

[32] N. Pallo, C. Kharangate, T. Modeer, *et al.*, "Modular heat sink for chip-scale GaN transistors in multilevel converters," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2798–2805. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8341414.

[33] Efficient Power Conversion Corporation. "Assembling eGaN® FETs." (), [Online]. Available: http://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf.

[34] G. Anand and S. S. K. Singh, "Design of single stage integrated bridgeless-boost pfc converter," in *2014 International Conference on Medical Imaging, m-Health and Emerging Communication Systems (MedCom)*, 2014, pp. 458–463. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7006052.

[35] M. Ancuti, M. Svoboda, S. Musuroi, A. Hedes, N. Olarescu, and M. Wienmann, "Boost interleaved PFC versus bridgeless boost interleaved PFC converter performance/efficiency analysis," in *2014 International Conference on Applied and Theoretical Electricity (ICATE)*, 2014, pp. 1–6. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6972651.

[36] S. M. Ahsanuzzaman, Y. Ma, A. A. Pathan, and A. Prodić, "A low-volume hybrid step-down dc-dc converter based on the dual use of flying capacitor," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 2497–2503. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7468216.

[37] S. da Silva Carvalho, S. M. Ahsanuzzaman, and A. Prodić, "A low-volume multi-phase interleaved Dc-Dc converter for high step-down applications with auto-balancing of phase currents," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 142–148. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7930685.

[38] Q. Huang, Q. Ma, P. Liu, A. Q. Huang, and M. de Rooij, "3kW Four-Level Flying Capacitor Totem-Pole Bridgeless PFC Rectifier with 200V GaN Devices," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 81–88. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8913025.

[39] Y. Xu, J. Wang, K. Xiong, and G. Yin, "A novel 5-level flying capacitor bridgeless PFC converter based on cost-effective low-voltage eGaN FETs," *Chinese Journal of Electrical Engineering*, vol. 6, no. 3, pp. 56–64, 2020. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9215143.

[40] *Sae electric vehicle and plug in hybrid electric vehicle conductive charge coupler*, Oct. 2017. [Online]. Available: https://doi.org/10.4271/J1772_201710.

[41] G. Electric, *DRYER WATTAGE AND ELECTRICAL RATING*, 2021. [Online]. Available: https://products.geappliances.com/appliance/gea-support-search-content?contentId=34592.

[42] Y. Lei, W. Liu, and R. C. N. Pilawa-Podgurski, "An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2227–2240, Mar. 2018. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7891047.

[43] X. Yuang, H. Stemmler, and I. Barbi, "Self-balancing of the clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter under sub-harmonic pwm modulation," *IEEE Transactions on Power Electronics*, vol. 16, no. 2, pp. 256–263, Mar. 2001. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=911150 .

[44] A. Shukla, A. Ghosh, and A. Joshi, "Capacitor voltage balancing schemes in flying capacitor multilevel inverters," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, Jun. 2007, pp. 2367–2372. [Online]. Available: https://ieeexplore.ieee.org /stamp/stamp.jsp?tp=&arnumber=4342381.

[45] Z. Ye, Y. Lei, Z. Liao, and R. C. N. Pilawa-Podgurski, "Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jul. 2017, pp. 1–7. [Online]. Available: https://ieeexplore.ieee.org/stamp/stam p.jsp?tp=&arnumber=8013368.

[46] C. B. Barth, T. Foulkes, W. H. Chung, *et al.*, "Design and control of a GaN-based, 13-level, flying capacitor multilevel inverter," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2016, pp. 1–6. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7556770.

[47] D. Chou, Y. Lei, and R. C. N. Pilawa-Podgurski, "A Zero-Voltage-Switching, Physically Flexible Multilevel GaN DC–DC Converter," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 1064–1073, Jan. 2020. [Online]. Available: https://ieeexplore.ieee.or g/stamp/stamp.jsp?tp=&arnumber=8710006.

[48] Efficient Power Conversion Corporation. "EPC2033 - Enhancement Mode Power Transistor Datasheet." (), [Online]. Available: http://epc-co.com/epc/Portals/0/epc/docu ments/datasheets/EPC2033_datasheet.pdf.

[49] T. Foulkes, T. Modeer, and R. C. N. Pilawa-Podgurski, "Developing a standardized method for measuring and quantifying dynamic on-state resistance via a survey of low voltage GaN HEMTs," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2018, pp. 2717–2724. [Online]. Available: https://ieeexplor e.ieee.org/stamp/stamp.jsp?tp=&arnumber=8341401.

[50] Z. Ye, W. C. Liu, P. Shenoy, and R. C. N. Pilawa-Podgurski, "Design and implementation of a low-cost and compact floating gate drive power circuit for GaN-based flying capacitor multi-level converters," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 2925–2931. [Online]. Available: http://ieeexplore .ieee.org/stamp/stamp.jsp?arnumber=7931112.

[51] Infineon Technologies. "IPT65R033G7." (), [Online]. Available: https://www.infineon .com/dgdl/Infineon-IPT65R033G7-DS-v02_01-EN.pdf?fileId=5546d46253f650570154 190220f14f1f.

[52] GaN Systems. "GS66516T Top-side cooled 650 V E-mode GaN transistor Preliminary Datasheet." (), [Online]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS66516T-DS-Rev-180422.pdf.

[53] TDK. "C5750X6S2W225K250KA." (), [Online]. Available: https://product.tdk.com/en/search/capacitor/ceramic/mlcc/info?part_no=C5750X6S2W225K250KA.

[54] Y. M. John Worman, "Thermal Performance of EPC eGaN FETs," Efficient Power Conversion (EPC) Co., Tech. Rep., 2011. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf.

[55] B. P. McGrath and D. G. Holmes, "Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter," in *2007 IEEE Power Electronics Specialists Conference*, Jun. 2007, pp. 1810–1816. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4453867.

[56] *Sae electric vehicle and plug in hybrid electric vehicle conductive charge coupler*, 2010. [Online]. Available: https://doi.org/10.4271/J1772_201001.

[57] Min Chen and Jian Sun, "Feedforward current control of boost single-phase PFC converters," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 338–345, Mar. 2006. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1603665.

[58] J. L. Bernal-Agustín and R. Dufo-López, "Efficient design of hybrid renewable energy systems using evolutionary algorithms," *Energy Conversion and Management*, vol. 50, no. 3, pp. 479–489, 2009. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0196890408004524.

[59] J.-n. Chou, "Optimal turning maneuvers for six-degree-of-freedom high angle-of-attack aircraft models," Retrospective Theses and Dissertations, Ph.D. dissertation, Iowa State University, 1995. [Online]. Available: https://lib.dr.iastate.edu/rtd/10891.

[60] T. Zhou and W. Sun, "Optimization of wind-pv hybrid power system based on interactive multi-objective optimization algorithm," in *Proceedings of 2012 International Conference on Measurement, Information and Control*, vol. 2, 2012, pp. 853–856.

[61] T. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 3, pp. 356–364, 1997. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=585833.

[62] A. Stillwell, E. Candan, and R. C. N. Pilawa-Podgurski, "Active voltage balancing in flying capacitor multi-level converters with valley current detection and constant effective duty cycle control," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11 429–11 441, 2019. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8664674.

[63] Z. Xia, B. L. Dobbins, and J. T. Stauth, "Natural balancing of flying capacitor multilevel converters at nominal conversion ratios," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–8. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8769724.

[64] H. Sepahvand, M. Khazraei, K. A. Corzine, and M. Ferdowsi, "Start-up procedure and switching loss reduction for a single-phase flying capacitor active rectifier," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 3699–3710, 2013. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6217303.

[65] E. Candan, D. Heeger, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "A series-stacked power delivery architecture with hot-swapping for high-efficiency data centers," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 571–578. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7309740.

[66] A. Stillwell, "Beyond PWM: Active balancing, start-up and ZVS for multi-level converters with applications in renewable energy systems," Ph.D. dissertation, University of Illinois at Urbana-Champaign, 2019. [Online]. Available: https://www.ideals.illinois.edu/handle/2142/105675.

[67] D. Reusch, F. C. Lee, and M. Xu, "Three level buck converter with control and soft startup," in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 31–35. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5316265.

[68] P. Papamanolis, D. Neumayr, and J. W. Kolar, "Behavior of the flying capacitor converter under critical operating conditions," in *Proceedings of the 26th IEEE International Symposium on Industrial Electronics (ISIE 2017), Edinburgh, Scotland*, Jun. 2017. [Online]. Available: https://www.pes.ee.ethz.ch/uploads/tx_ethpublications/9_Behavior_of_the_Flying_Capacitor_Converter_Under_Critical_Operating_Conditions_Papamanolis_ISIE_2017.pdf.